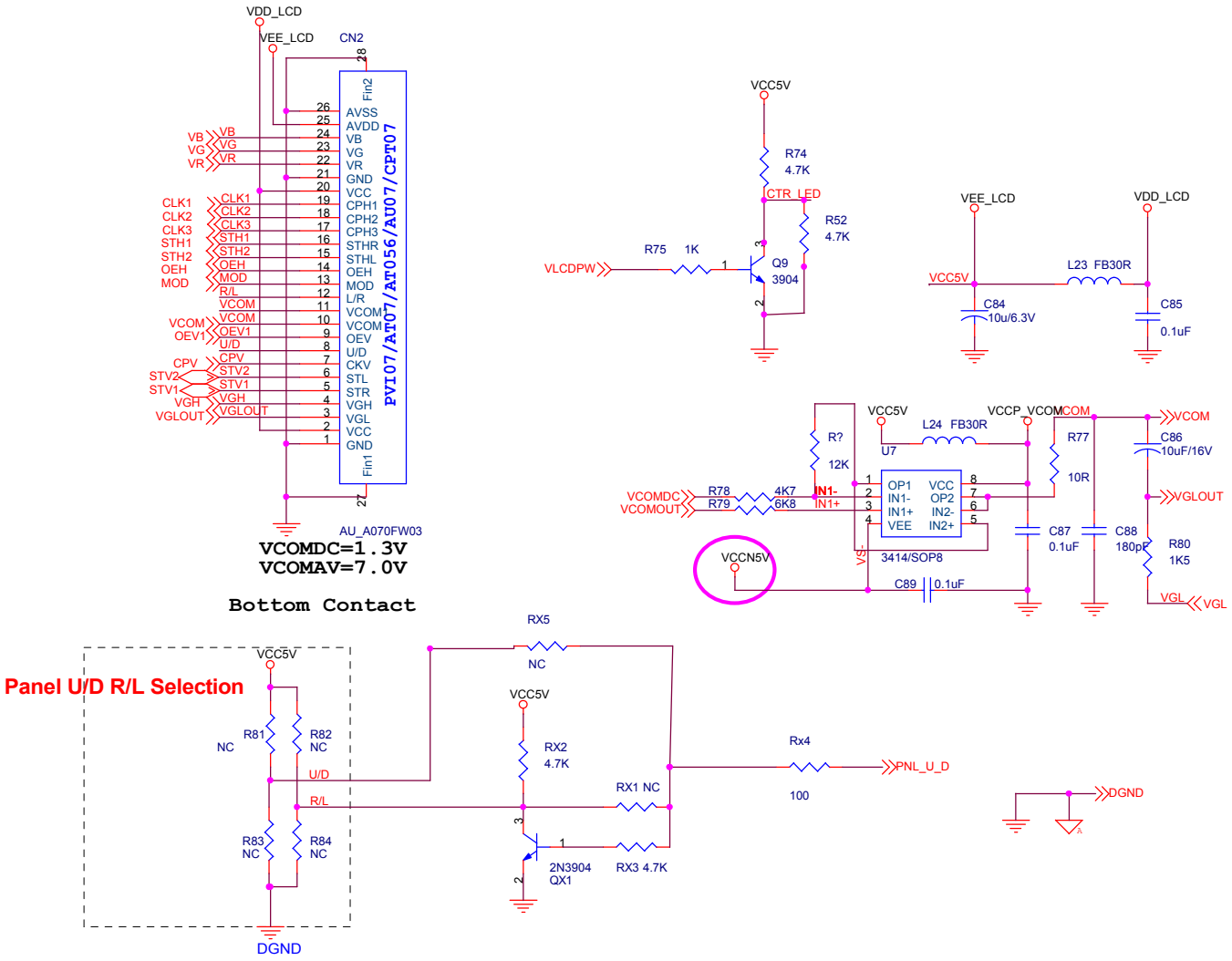
Service Manual

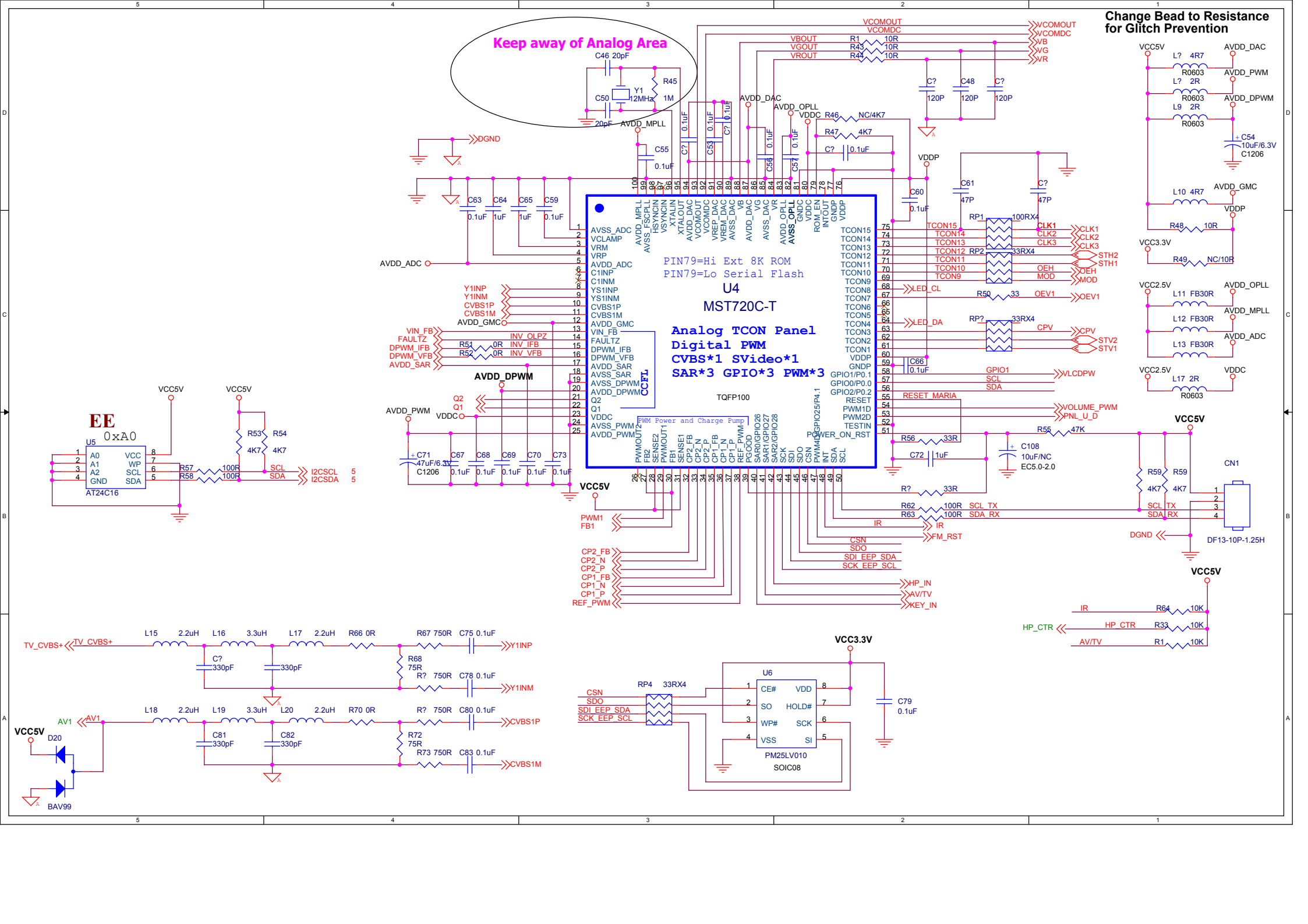
1. Schematic Circuit Diagram

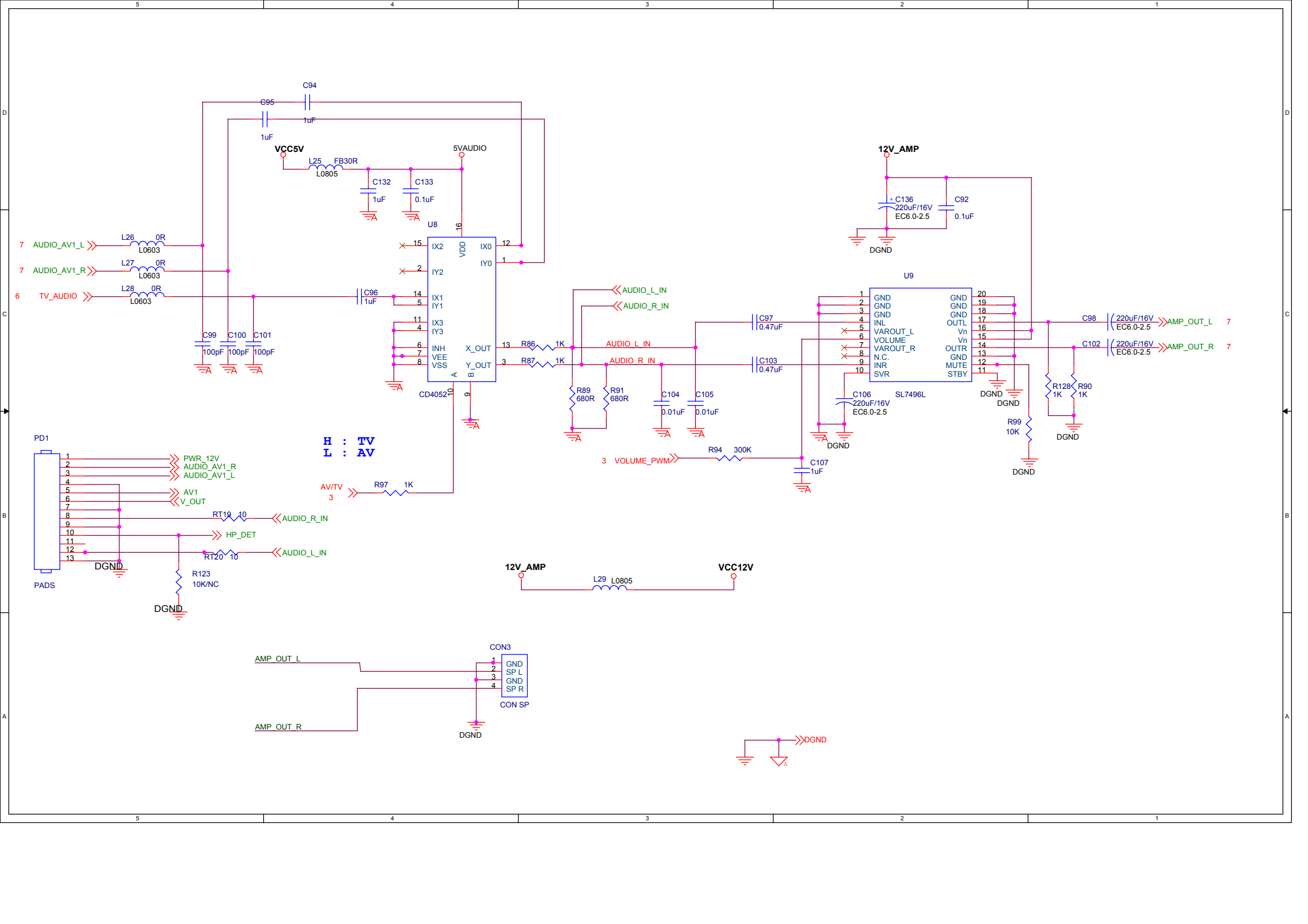
2. Critical Commpoents List

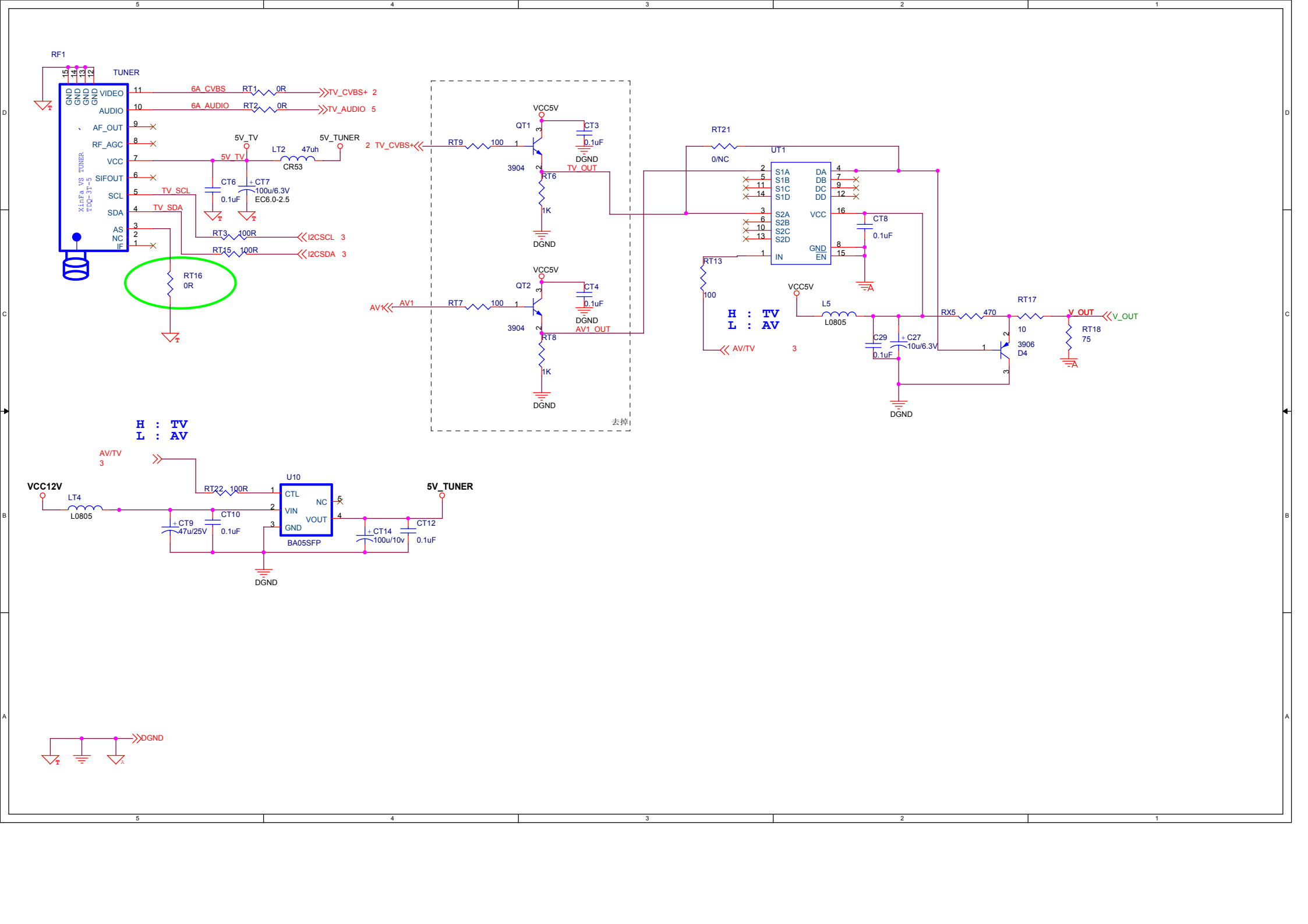
3. IC Date Sheet & IC Description

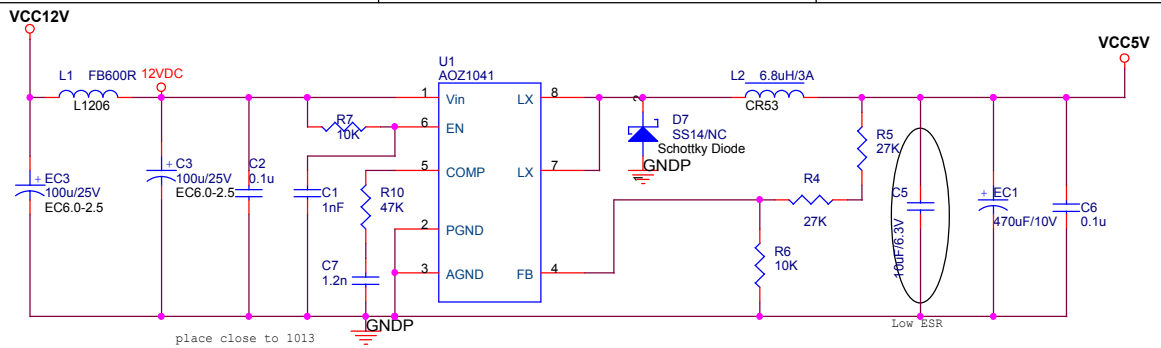
4. Service Tools and Equipment

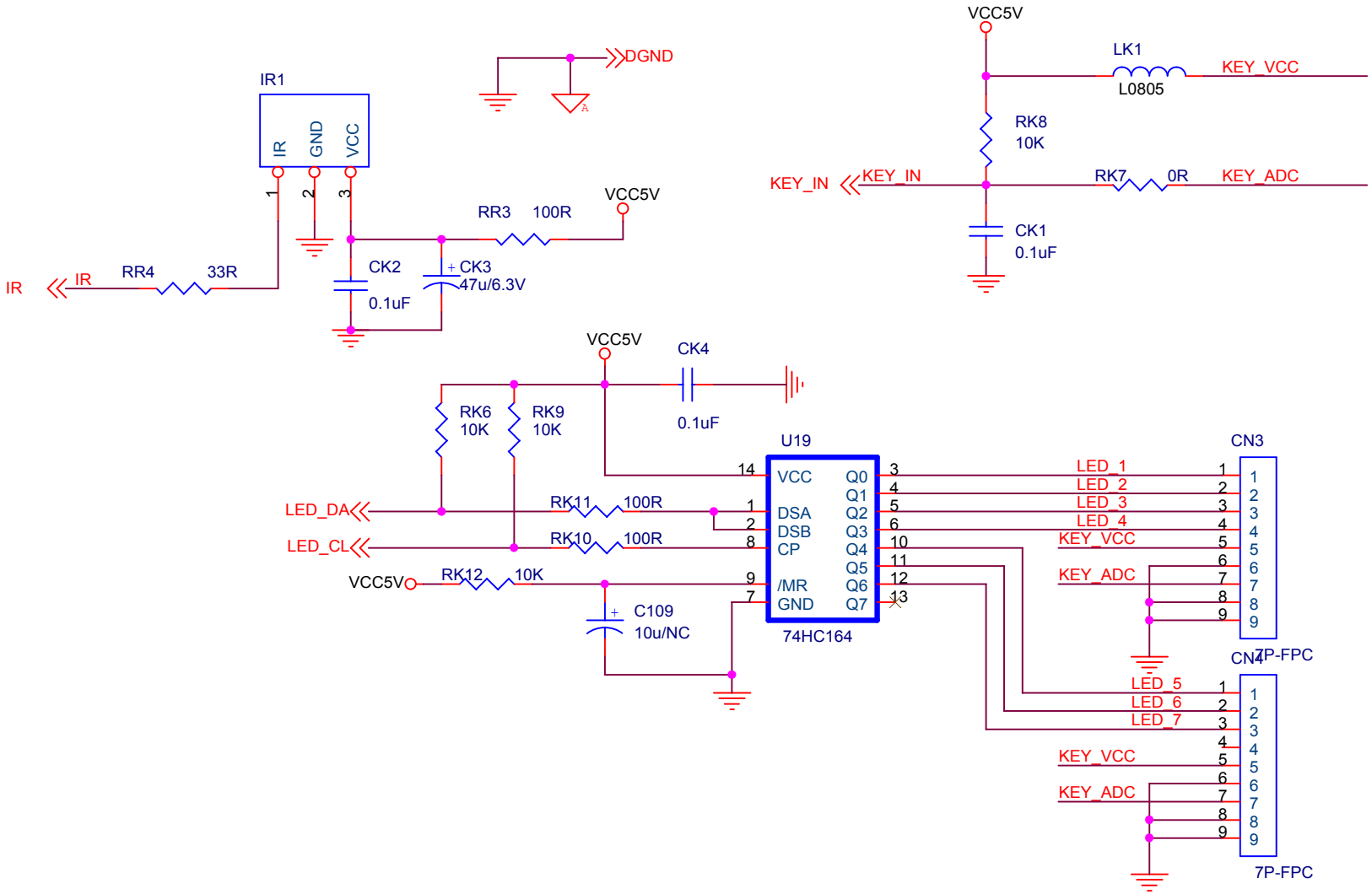

VDD_LCD
VEE_LCD
CN2
Fin2
AVSS
AVDD
VB
VG
VR
GND
VCC
CPH1
CPH2
CPH3
STHR
STHL
OEH
MOD
L/R
VCOM
VCOM
OEV
U/D
CKV
STL
STR
VGH
VGL
VCC
GND
Fin1
PVI07/AT07/AT056/AU07/CPT07
AU_A070FW03
VCOMDC=1.3V
VCOMAV=7.0V
Bottom Contact
VCC5V
R74
4.7K
CTR_LED
R52
4.7K
R75
1K
VLCDPW
Q9
3904
VEE_LCD
VDD_LCD
VCC5V
L23 FB30R
C84
10u/6.3V
C85
0.1uF
R?
12K
VCC5V
L24 FB30R
VCCP_VCOM
COM
VCOM
C86
10uF/16V
U7
R77
10R
VCOMDC
VCOMOUT
R78
4K7
R79
6K8
IN1-
IN1+
OP1
IN1-
IN1+
VEE
VCC
OP2
IN2-
IN2+
VGLOUT
C87
0.1uF
C88
180pF
R80
1K5
VCCN5V
VS-
3414/SOP8
C89
0.1uF
VGL
VGL
Panel U/D R/L Selection
VCC5V
R81
NC
R82
NC
U/D
R/L
R83
NC
R84
NC
DGND
RX5
NC
VCC5V
RX2
4.7K
RX1 NC
2N3904
QX1
RX3 4.7K
Rx4
100
PNL_U_D
DGND

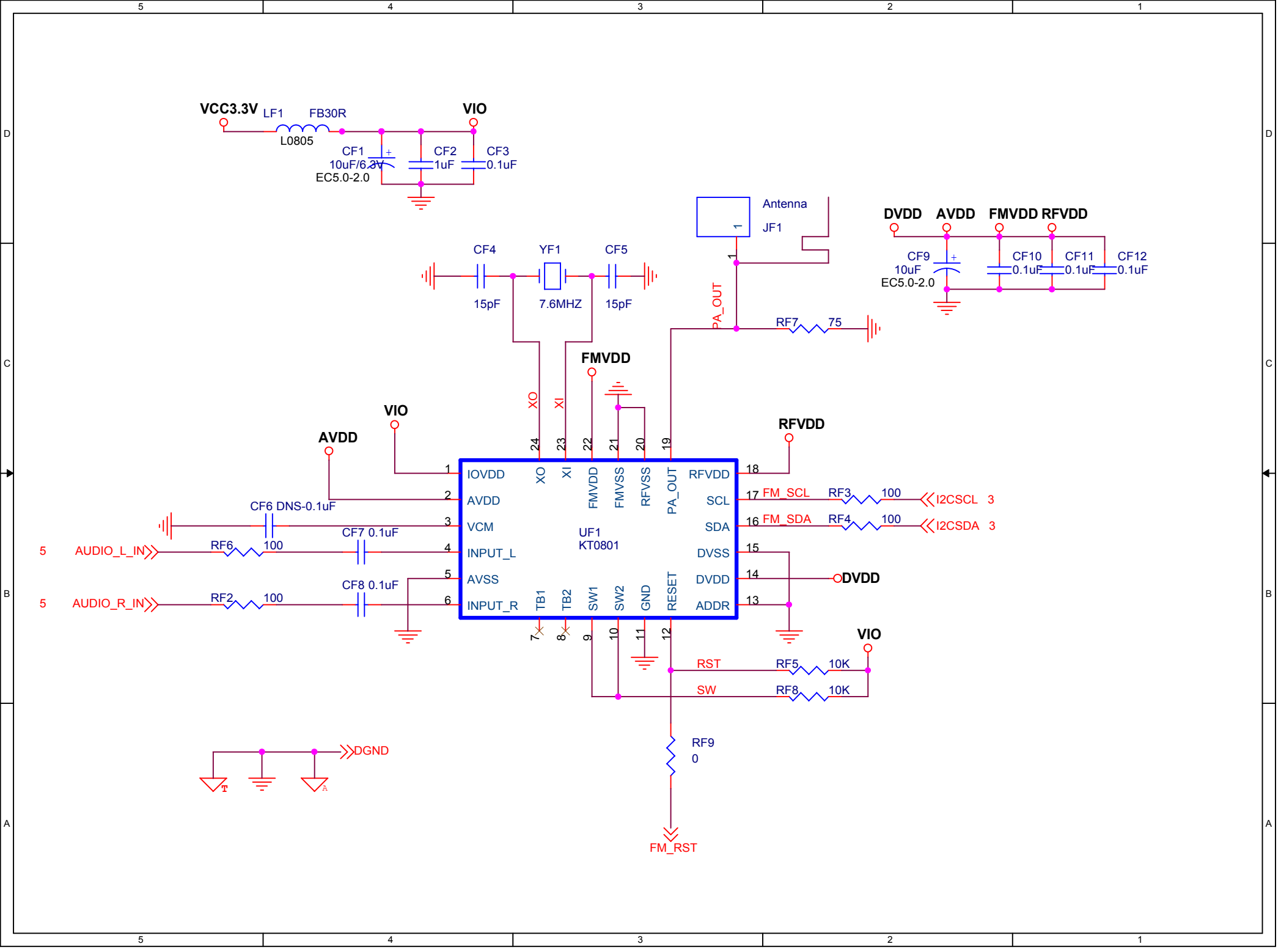

Keep away of Analog Area
Change Bead to Resistance for Glitch Prevention
U4
MST720C-T
TQFP100
PIN79=Hi Ext 8K ROM
PIN79=Lo Serial Flash
Analog TCON Panel
Digital PWM
CVBS*1 SVideo*1
SAR*3 GPIO*3 PWM*3
CCFL
PWM Power and Charge Pump
EE
0xA0
AT24C16
U5
U6
PM25LV010
SOIC08
CN1
DF13-10P-1.25H
BAV99
D20
VCC5V
VCC3.3V
VCC2.5V
AVDD_DPWM
AVDD_PWM
AVDD_ADC
AVDD_DAC
AVDD_OPLL
AVDD_MPLL
AVDD_GMC
AVDD_DPWM
VDDP
VDDC
DGND
TV_CVBS+
Y1INP
Y1INM
CVBS1P
CVBS1M
I2CSCL
I2CSDA
SCL
SDA
IR
HP_IN
AV/TV
KEY_IN
FM_RST
HP_CTR
VLCDPW
VOLUME_PWM
PNL_U_D
RESET_MARIA
LED_CL
LED_DA
CPV
OEH
MOD
OEV1
CLK1
CLK2
CLK3
STH2
STH1
STV2
STV1
SCL_TX
SDA_RX
CSN
SDO
SDI_EEP_SDA
SCK_EEP_SCL

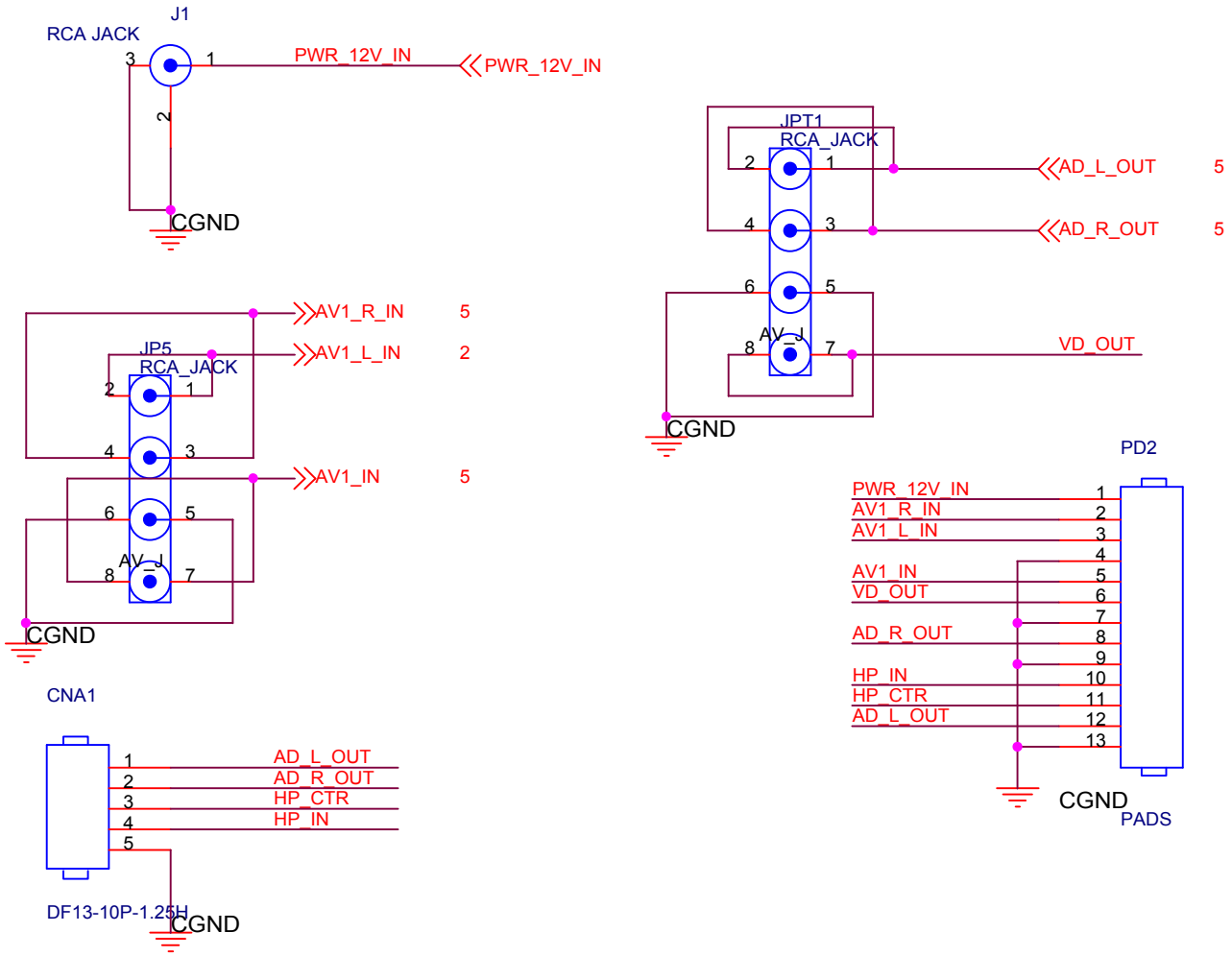

C94
C95
1uF
1uF
VCC5V
5VAUDIO
L25 FB30R
L0805
C132
1uF
C133
0.1uF
U8
7 AUDIO_AV1_L
L26 0R
L0603
7 AUDIO_AV1_R
L27 0R
L0603
6 TV_AUDIO
L28 0R
L0603
C96
1uF
C99
100pF
C100
100pF
C101
100pF
IX2
IX0
VDD
IY2
IY0
IX1
IY1
IX3
IY3
INH
X_OUT
VEE
Y_OUT
VSS
CD4052
AUDIO_L_IN
AUDIO_R_IN
R86 1K
R87 1K
AUDIO_L_IN
AUDIO_R_IN
R89
680R
R91
680R
C104
0.01uF
C105
0.01uF
12V_AMP
C136
220uF/16V
EC6.0-2.5
C92
0.1uF
DGND
U9
C97
0.47uF
C103
0.47uF
GND
INL
VAROUT_L
VOLUME
VAROUT_R
N.C.
INR
SVR
SL7496L
GND
OUTL
Vn
Vn
OUTR
GND
MUTE
STBY
C106
220uF/16V
EC6.0-2.5
C98
220uF/16V
EC6.0-2.5
AMP_OUT_L 7
C102
220uF/16V
EC6.0-2.5
AMP_OUT_R 7
R128
1K
R90
1K
R99
10K
DGND
DGND
DGND
DGND
PD1
PWR_12V
AUDIO_AV1_R
AUDIO_AV1_L
AV1
V_OUT
RT19 10
AUDIO_R_IN
HP_DET
RT20 10
AUDIO_L_IN
PADS
DGND
R123
10K/NC
DGND
H : TV
L : AV
AV/TV
3
R97 1K
3 VOLUME_PWM
R94 300K
C107
1uF
12V_AMP
L29 L0805
VCC12V
CON3
GND
SP L
GND
SP R
CON SP
AMP_OUT_L
AMP_OUT_R
DGND
DGND

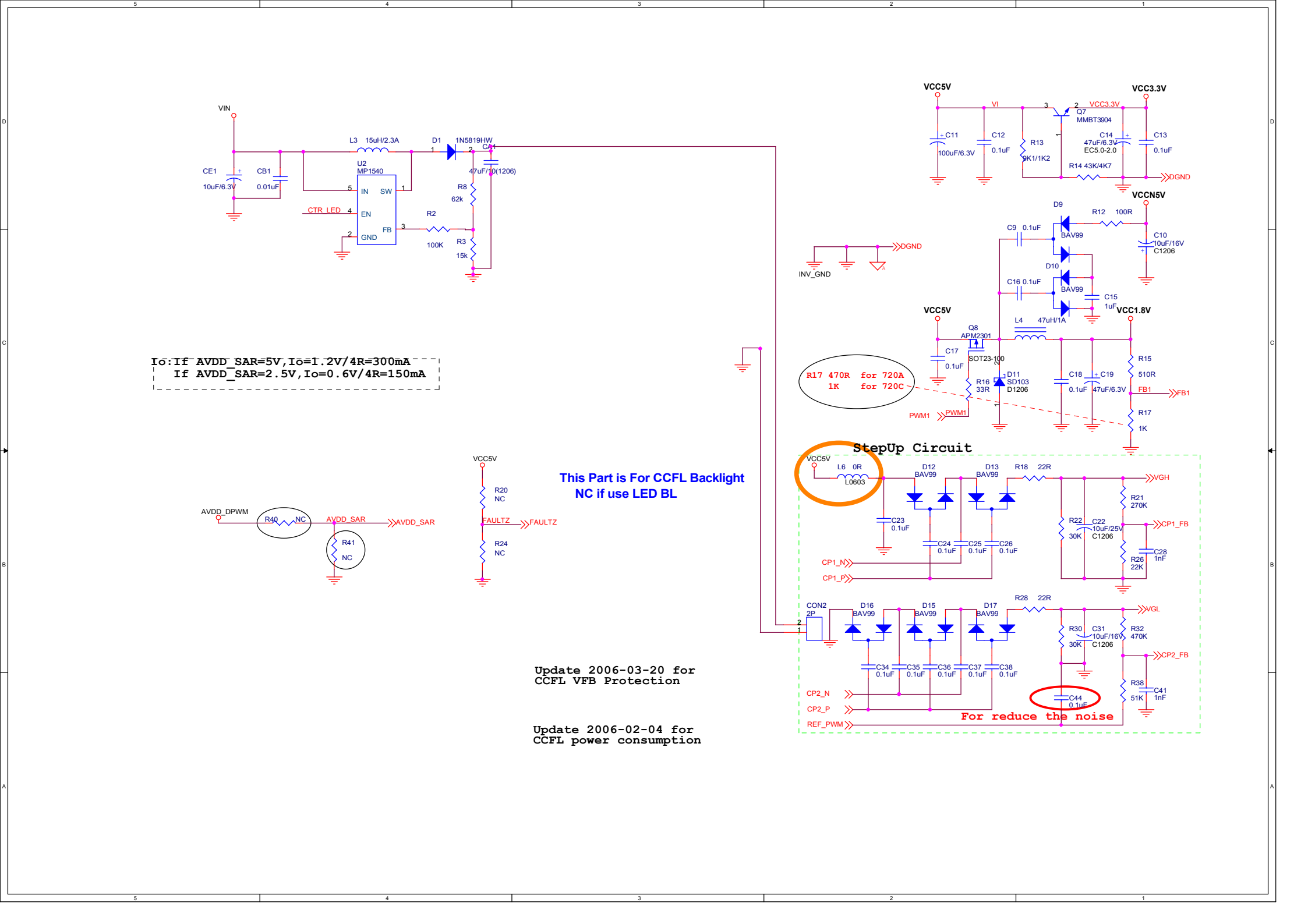

RF1
TUNER
GND
GND
GND
GND
VIDEO
AUDIO
AF_OUT
RF_AGC
VCC
SIFOUT
SCL
SDA
AS
NC
IF
XinFa VS TUNER
TDQ-3T-5
6A_CVBS
RT1
0R
TV_CVBS+ 2
6A_AUDIO
RT2
0R
TV_AUDIO 5
5V_TV
5V_TUNER
LT2
47uh
CR53
CT6
0.1uF
CT7
100u/6.3V
EC6.0-2.5
TV_SCL
TV_SDA
RT3
100R
I2CSCL 3
RT15
100R
I2CSDA 3
RT16
0R
2 TV_CVBS+
RT9
100
QT1
3904
CT3
0.1uF
DGND
TV_OUT
RT6
1K
DGND
VCC5V
AV1
RT7
100
QT2
3904
CT4
0.1uF
DGND
AV1_OUT
RT8
1K
DGND
去掉
RT21
0/NC
UT1
S1A
S1B
S1C
S1D
S2A
S2B
S2C
S2D
IN
DA
DB
DC
DD
VCC
GND
EN
CT8
0.1uF
RT13
100
H : TV
L : AV
AV/TV
3
VCC5V
L5
L0805
C29
0.1uF
C27
10u/6.3V
DGND
RX5
470
RT17
10
3906
D4
V_OUT
V_OUT
RT18
75
H : TV
L : AV
AV/TV
3
VCC12V
LT4
L0805
RT22
100R
U10
CTL
VIN
GND
NC
VOUT
BA05SFP
CT9
47u/25V
CT10
0.1uF
CT14
100u/10v
CT12
0.1uF
5V_TUNER
DGND
DGND


VCC12V
L1 FB600R
L1206
12VDC
U1
AOZ1041
Vin
EN
COMP
PGND
AGND
LX
LX
FB
1
6
5
2
3
8
7
4
R7
10K
C1
1nF
R10
47K
C7
1.2n
EC3
100u/25V
EC6.0-2.5
C3
100u/25V
EC6.0-2.5
C2
0.1u
GNDP
place close to 1013
D7
SS14/NC
Schottky Diode
GNDP
L2 6.8uH/3A
CR53
R5
27K
R4
27K
R6
10K
C5
10uF/6.3V
Low ESR
EC1
470uF/10V
C6
0.1u
VCC5V


DGND
IR1
IR
GND
VCC
1
2
3
VCC5V
RR3 100R
IR
IR
RR4 33R
CK2
0.1uF
CK3
47u/6.3V
VCC5V
LK1
L0805
KEY_VCC
RK8
10K
KEY_IN
KEY_IN
RK7 0R
KEY_ADC
CK1
0.1uF
VCC5V
CK4
0.1uF
RK6
10K
RK9
10K
U19
VCC
DSA
DSB
CP
/MR
GND
Q0
Q1
Q2
Q3
Q4
Q5
Q6
Q7
74HC164
LED_DA
RK11 100R
LED_CL
RK10 100R
VCC5V
RK12 10K
C109
10u/NC
CN3
LED_1
LED_2
LED_3
LED_4
KEY_VCC
KEY_ADC
7P-FPC
CN4
LED_5
LED_6
LED_7
KEY_VCC
KEY_ADC
7P-FPC


VCC3.3V
LF1
FB30R
L0805
VIO
CF1
10uF/6.3V
EC5.0-2.0
CF2
1uF
CF3
0.1uF
Antenna
JF1
DVDD
AVDD
FMVDD
RFVDD
CF9
10uF
EC5.0-2.0
CF10
0.1uF
CF11
0.1uF
CF12
0.1uF
CF4
15pF
YF1
7.6MHZ
CF5
15pF
PA_OUT
RF7
75
FMVDD
XO
XI
VIO
AVDD
RFVDD
IOVDD
AVDD
VCM
INPUT_L
AVSS
INPUT_R
XO
XI
FMVDD
FMVSS
RFVSS
PA_OUT
RFVDD
SCL
SDA
DVSS
DVDD
ADDR
UF1
KT0801
CF6 DNS-0.1uF
CF7 0.1uF
CF8 0.1uF
AUDIO_L_IN
AUDIO_R_IN
RF6
100
RF2
100
FM_SCL
RF3
100
I2CSCL
FM_SDA
RF4
100
I2CSDA
DVDD
VIO
TB1
TB2
SW1
SW2
GND
RESET
RST
RF5
10K
SW
RF8
10K
RF9
0
FM_RST
DGND


J1
RCA JACK
PWR_12V_IN
PWR_12V_IN
CGND
JPT1
RCA_JACK
AD_L_OUT
5
AD_R_OUT
5
AV_J
VD_OUT
CGND
AV1_R_IN
5
AV1_L_IN
2
JP5
RCA_JACK
AV1_IN
5
AV_J
CGND
PD2
PWR_12V_IN
AV1_R_IN
AV1_L_IN
AV1_IN
VD_OUT
AD_R_OUT
HP_IN
HP_CTR
AD_L_OUT
CGND
PADS
CNA1
AD_L_OUT
AD_R_OUT
HP_CTR
HP_IN
DF13-10P-1.25H
CGND


VIN
L3 15uH/2.3A
D1 1N5819HW
CE1 10uF/6.3V
CB1 0.01uF
U2 MP1540
IN SW
EN
FB
GND
CTR_LED
R2 100K
R8 62k
R3 15k
CA1 47uF/10(1206)
VCC5V
VCC3.3V
VI
Q7 MMBT3904
C11 100uF/6.3V
C12 0.1uF
R13 9K1/1K2
C14 47uF/6.3V EC5.0-2.0
C13 0.1uF
R14 43K/4K7
DGND
VCCN5V
D9
R12 100R
C9 0.1uF
BAV99
C10 10uF/16V C1206
D10
C16 0.1uF
C15 1uF
INV_GND
VCC5V
VCC1.8V
Q8 APM2301
SOT23-100
L4 47uH/1A
C17 0.1uF
D11 SD103 D1206
R16 33R
C18 0.1uF
C19 47uF/6.3V
R15 510R
FB1
R17 1K
PWM1
R17 470R for 720A
1K for 720C
Io:If AVDD_SAR=5V,Io=1.2V/4R=300mA
If AVDD_SAR=2.5V,Io=0.6V/4R=150mA
StepUp Circuit
VCC5V
L6 0R L0603
D12 BAV99
D13 BAV99
R18 22R
VGH
R21 270K
C23 0.1uF
C24 0.1uF
C25 0.1uF
C26 0.1uF
R22 30K
C22 10uF/25V C1206
CP1_FB
R26 22K
C28 1nF
CP1_N
CP1_P
CON2 2P
D16 BAV99
D15 BAV99
D17 BAV99
R28 22R
VGL
R30 30K
C31 10uF/16V C1206
R32 470K
C34 0.1uF
C35 0.1uF
C36 0.1uF
C37 0.1uF
C38 0.1uF
CP2_FB
R38 51K
C41 1nF
CP2_N
CP2_P
REF_PWM
C44 0.1uF
For reduce the noise
AVDD_DPWM
R40 NC
AVDD_SAR
R41 NC
VCC5V
R20 NC
FAULTZ
R24 NC
This Part is For CCFL Backlight
NC if use LED BL
Update 2006-03-20 for
CCFL VFB Protection
Update 2006-02-04 for
CCFL power consumption

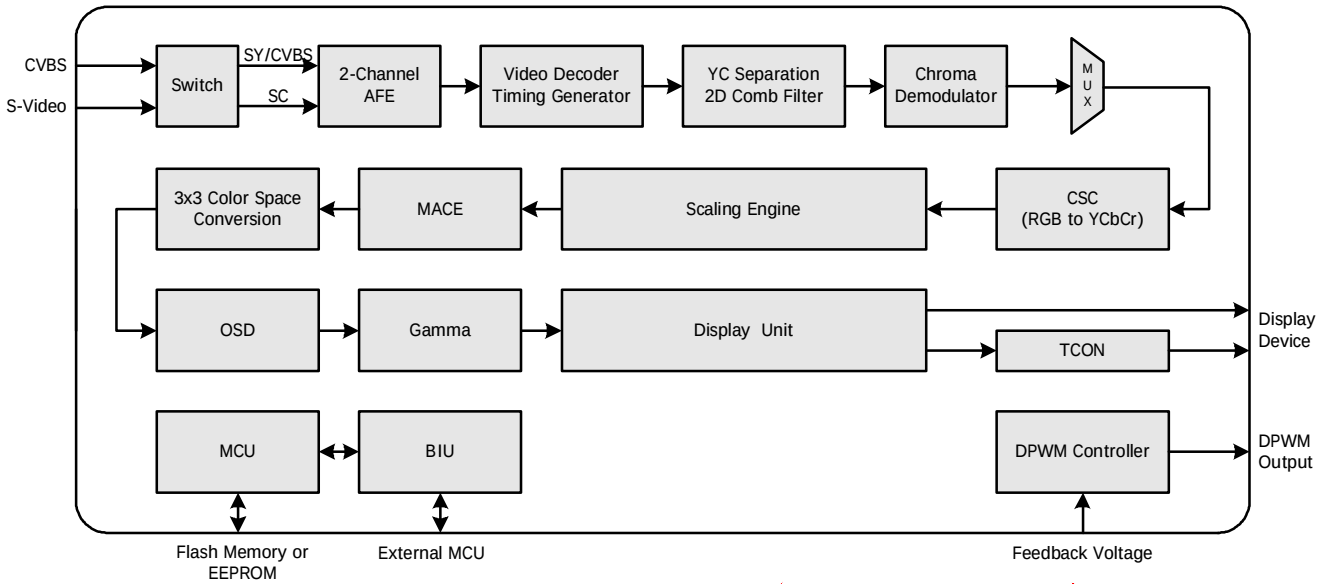
Critical Components List

Components	Designator	Function
MST720	**U4**	**SCALER+MCU+Video Decode**
PM25LV010	**U6**	**FLASH**
KT0801	**UF1**	FM transmit
TPA6011	**UD1**	**Speaker Audio Amplifier**
24C16	**U12**	**E2ROM**
AOZ1041	**U1**	**dropout voltage regulators**

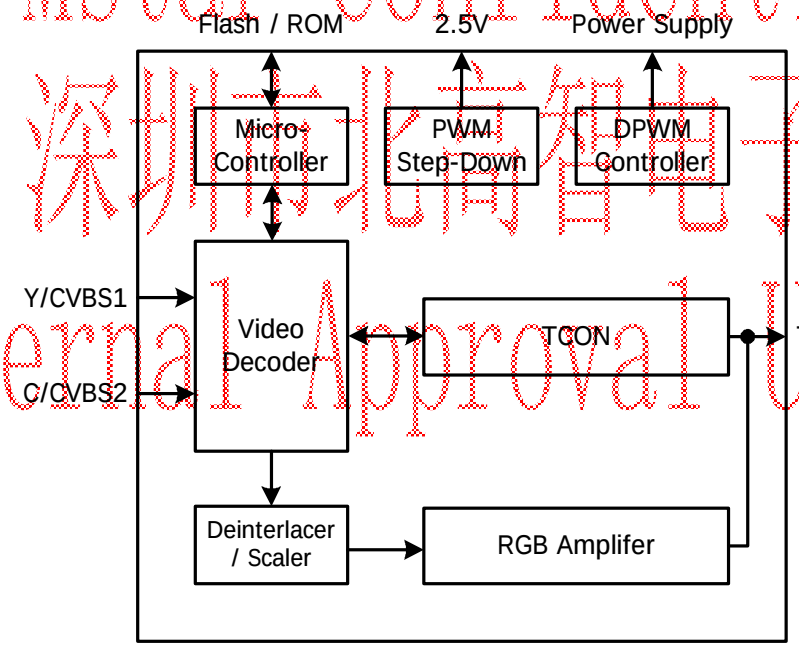
FEATURES

- Video Decoder
  - Supports NTSC, PAL and SECAM video input formats
  - 2D NTSC and PAL comb-filter for Y/C separation of CVBS input
  - Single CVBS and S-video input
  - Supports Closed-caption and V-chip
  - ACC, AGC, and DCGC (Digital Chroma Gain Control)
- Color Engine
  - Brightness, contrast, saturation, and hue adjustment
  - 9-tap programmable multi-purpose FIR (Finite Impulse Response) filter
  - Differential 3-band peaking engine
  - Luminance Transient Improvement (LTI)
  - Chrominance Transient Improvement (CTI)
  - Black Level Extension (BLE)
  - White Level Extension (WLE)
  - Favor Color Compensation (FCC)
  - 3-channel gamma curve adjustment
- Scaling Engine/TCON
  - Supports analog panels with the resolution of 960x234, 1200x234, 1400x234, and more
  - Supports various displaying modes
  - Supports horizontal panorama scaling
- Digital PWM Controller
  - Integrated general purpose digital PWM control loop
  - Programmable startup operating frequency and period with output voltage regulation
  - Programmable output current regulation; 40KHz~70KHz switching frequency, sync. to HSYNC possible
  - Burst-mode or continuous-mode for output current regulation; 150Hz~300Hz burst-mode frequency, sync. to VSYNC possible
  - Programmable protection level for input voltage and fault detection
- Miscellaneous
  - Built-in MCU
  - 3-wire serial bus interface for configuration setup
  - Built-in step-down PWM circuits for input 2.5V
  - Built-in VCOM DC level adjusting circuits
  - Built-in internal OSD with 256 programmable fonts, 16-color palettes, and 12-bit color resolution
  - 3-channel low-power 8-bit DAC integration for RGB output, dynamic range 0.1-4.9V
  - Built-in VCOM DC/AC level adjustment circuit
  - Spread spectrum clocks
  - Optional 3.3V / 5V output pads with programmable driving current
  - 100-pin LQFP package

BLOCK DIAGRAM



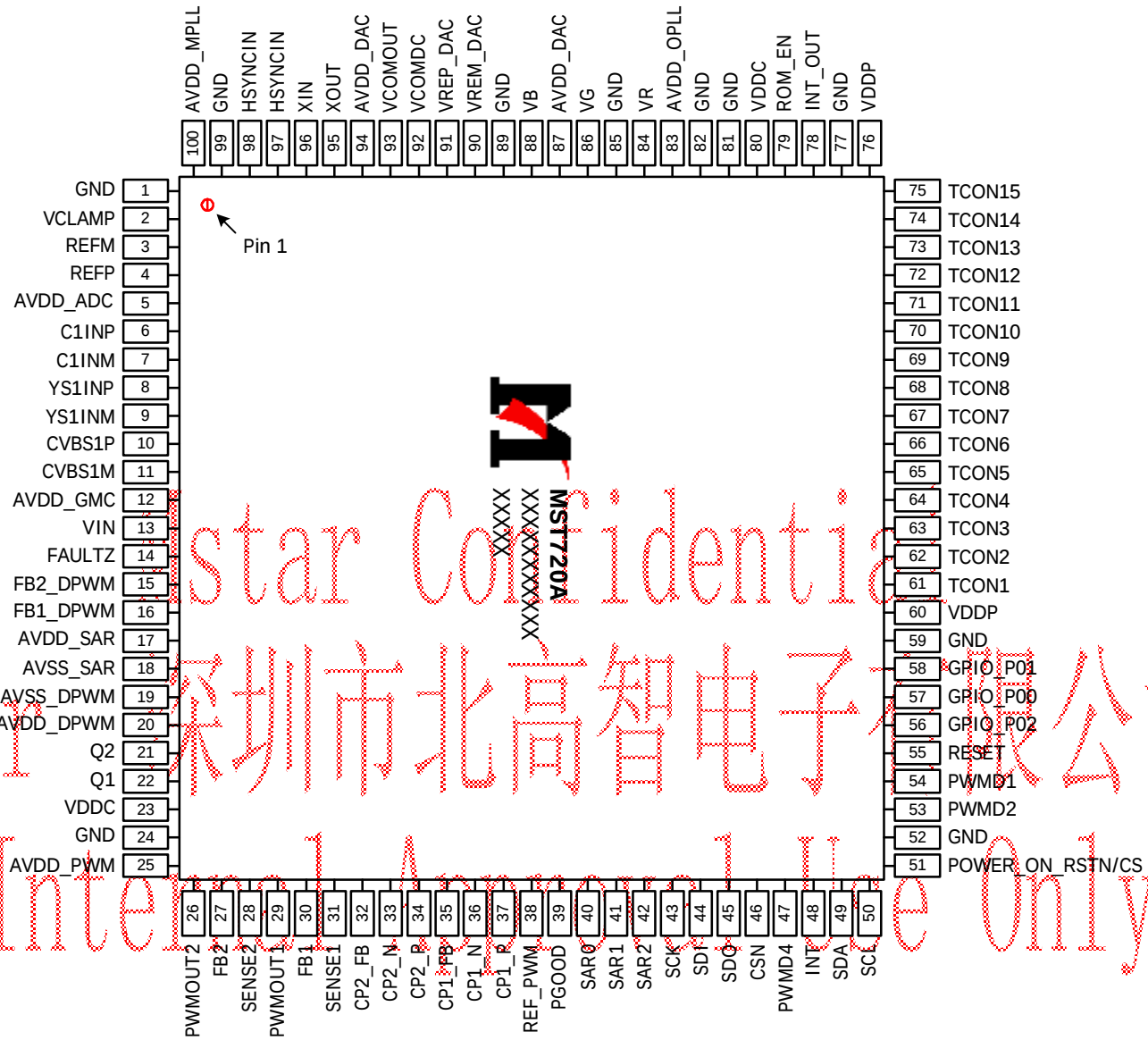
SYSTEM APPLICATION DIAGRAM



GENERAL DESCRIPTION

The MST720A is a high quality ASIC for NTSC/PAL/SECAM car TV application. It receives analog NTSC/PAL/SECAM CVBS and S-Video inputs from TV tuners, DVD or VCR sources, including weak and distorted signals. Automatic gain control (AGC) and 8-bit 3-channel A/D converters provide high resolution video quantization. With automatic video source and mode detection, users can easily switch and adjust variety of signal sources. Multiple internal adaptive PLLs precisely extract pixel clock from video source and perform sharp color demodulation. Built-in line-buffer supports adaptive 2-D comb-filter, 2-D sharpening, and synchronization stabler in a condense manner. The output format of MST720A supports 3.5″~7″ analog TFT-LCD modules.

PIN DIAGRAM (MST720A)



PIN DESCRIPTION

Analog Interface

Pin Name	Pin Type	Function	Pin
VCLAMP		CVBS/YC Mode Clamp Voltage Bypass	2
REFM		Internal ADC Bottom De-coupling Pin	3
REFP		Internal ADC Top De-coupling Pin	4
C1INP	Analog Input	Analog Chroma Input for TV S-Video1 / Analog Composite Input of TV CVBS4	6
C1INM	Analog Input	Reference Ground for Analog Chroma Input of TV S-Video1 / Analog Composite Input of TV CVBS4	7
YS1INP	Analog Input	Analog Luma Input of TV S-Video1 / Analog Composite Input of TV CVBS3	8
YS1INM	Analog Input	Reference Ground for Analog Luma Input of TV S-Video1 / Analog Composite Input of TV CVBS3	9
CVBS1P	Analog Input	Analog Composite Input for TV CVBS1	10
CVBS1M	Analog Input	Reference Ground for Analog Composite Input of TV CVBS1	11
HSYNCIN	Schmitt Trigger Input w/ 5V-tolerant	HSYNC / Composite Sync for VGA Input	98
VSYNCIN	Schmitt Trigger Input w/ 5V-tolerant	VSYNC for VGA Input	97

Analog Panel Output Interface

Pin Name	Pin Type	Function	Pin
VR	Analog Output	Red Channel Output 4.0 Vp-p	84
VG	Analog Output	Green Channel Output 4.0 Vp-p	86
VB	Analog Output	Blue Channel Output 4.0 Vp-p	88
REFM_DAC		DAC Bottom Reference Voltage Decoupling Cap. 1uF to Ground	90
REFP_DAC		DAC Top Reference Voltage Decoupling Cap. 1uF to Ground	91
TCON[15:1]	Output	TCON Output	75-61

VCOM Interface

Pin Name	Pin Type	Function	Pin
VCOMDC	Analog Output	Reference DC Voltage Output for Common Amplifier	92
VCOMOUT	Analog Output	Pulse Output for Common Voltage.	93

Switching Power and PWM Interface

Pin Name	Pin Type	Function	Pin
PWMOUT2	Output	Switching Pulse Output for DC-DC Converter	26
FB2	Analog Input	Error Voltage Feedback Input Pin for PWM2; voltage = 1.2V	27
SENSE2	Analog Input	Sense Circuit Connection for PWM2	28
PWMOUT1	Output	Switching Pulse Output for DC-DC Converter	29
FB1	Analog Input	Error Voltage Feedback Input Pin for PWM1; voltage = 1.2V	30
SENSE1	Analog Input	Sense Circuit Connection for PWM1	31
CP2_FB	Analog Input	Error Voltage Feedback Input Pin for CP2; voltage = 1.2V	32
CP2_N	Output	Charge Pump Negative Pulse for DC-DC Negative Voltage Converter	33
CP2_P	Output	Charge Pump Positive Pulse for DC-DC Negative Voltage Converter	34
CP1_FB	Analog Input	Error Voltage Feedback Input Pin for CP1; voltage = 1.2V	35
CP1_N	Output	Charge Pump Negative Pulse for DC-DC Positive Voltage Converter	36
CP1_P	Output	Charge Pump Positive Pulse for DC-DC Positive Voltage Converter	37
REF_PWM	Output	PWM Reference; voltage = 2.4V	38
PGOOD	Output	Power Good Detector	39

Internal MCU Interface with Serial Flash Memory

Pin Name	Pin Type	Function	Pin
SAR2	Analog Input	SAR Low Speed ADC Input 2	42
SAR1	Analog Input	SAR Low Speed ADC Input 1	41
SAR0	Analog Input	SAR Low Speed ADC Input 0	40
SCK	Output	SPI Interface Sampling Clock	43
SDI	Output	SPI Interface Data-In	44
SDO	Input w/ 5V-tolerant	SPI Interface Data-Out	45
CSN	Output	SPI Interface Chip Select	46
GPIO_P00	I/O w/ 5V-tolerant	General Purpose Input/Output; 4mA driving strength	57
GPIO_P01	I/O w/ 5V-tolerant	General Purpose Input/Output; 4mA driving strength	58
GPIO_P05	I/O w/ 5V-tolerant	General Purpose Input/Output; 4mA driving strength	56
INT	Input	Interrupt Input for IR Receiver	48
SDA	I/O w/ 5V-tolerant	3-Wire Serial Bus Data	49

Pin Name	Pin Type	Function	Pin
SCL	Input w/ 5V-tolerant	3-Wire Serial Bus Clock	50
POWER_ON_RSTN/CS	Input w/ 5V-tolerant	Power On Reset Signal / Chip Selection for 3-wire Serial	51

Digital PWM Interface

Pin Name	Pin Type	Function	Pin
Q1	Output	DPWM Output 1	22
Q2	Output	DPWM Output 2	21
FB1_DPWM	Analog Input	Input for 1st Feedback Loop	16
FB2_DPWM	Analog Input	Input for 2nd Feedback Loop	15
FAULTZ	Analog Input	Fault Detection (Low Enable)	14
VIN	Analog Input	System Input Voltage Detection	13

Misc. Interface

Pin Name	Pin Type	Function	Pin
RESET	Schmitt Trigger Input w/ 5V-tolerant	Hardware Reset; active high	55
XIN	Analog Input	Crystal Oscillator Input	96
XOUT	Analog Output	Crystal Oscillator Output	95
PWMD4	Output	Pulse Width Modulation Output; 4mA driving strength	47
PWMD2	Output	Pulse Width Modulation Output; 4mA driving strength	53
PWMD1	Output	Pulse Width Modulation Output; 4mA driving strength	54
INT_OUT	Output	Mode Detection Interrupt Output	78
ROM_EN	Input	Internal ROM Enable. 0: Disable. 1: Enable.	79

Power Pins

Pin Name	Pin Type	Function	Pin
AVDD_ADC	2.5V Power	ADC Power	5
AVDD_GMC	5V Power	GMC Power	12
AVDD_SAR	5V Power	SAR Power	17
AVDD_DPWM	5V Power	DPWM Power	20
AVDD_PWM	5V Power	PWM Power	25
AVDD_OPLL	2.5V Power	OPLL Power	83
AVDD_DAC	5V Power	Voltage DAC Power	87, 94

Pin Name	Pin Type	Function	Pin
AVDD_MPLL	2.5V Power	MPLL Power	100
VDDC	2.5V Power	Digital Core Power	23, 80
VDDP	3.3V/5V Power	Digital Input/Output Power	60, 76
AVSS_SAR	Ground	SAR Ground	18
AVSS_DPWM	Ground	DPWM Ground	19
GND	Ground	Ground	1, 24, 52, 59, 81, 82, 85, 89, 99

ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
5.0V Supply Voltages	V_{VDD_50}	-0.3		5.5	V
3.3V Supply Voltages	V_{VDD_33}	-0.3		3.6	V
2.5V Supply Voltages	V_{VDD_25}	-0.3		2.75	V
Input Voltage (5V tolerant inputs)	$V_{IN5Vtol}$	-0.3		5.0	V
Input Voltage (non 5V tolerant inputs)	V_{IN}	-0.3		V_{VDD_33}	V
Ambient Operating Temperature (commercial use)	T_A	0		70	°C
Ambient Operating Temperature (extended temp. range)	T_A	-20		80	°C
Storage Temperature	T_{STG}	-40		125	°C
Junction Temperature	T_J			125	°C
Thermal Resistance (Junction to Air) Natural Conversion	θ_{JA}		TBD		°C/W
Thermal Resistance (Junction to Case) Natural Conversion	θ_{JC}		TBD		°C/W

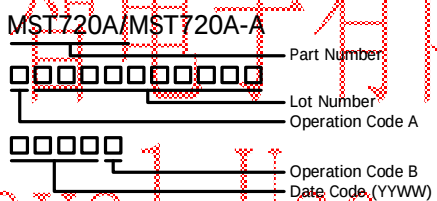
Note: Stress above those listed under Absolute Maximum Rating may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions outside of those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
MST720A	0°C to +70°C	LQFP	100
MST720A-A	-20°C to +80°C	LQFP	100
MST720A-LF	0°C to +70°C	LQFP	100
MST720A-A-LF	-20°C to +80°C	LQFP	100

Note: Product suffix "-LF" represents lead-free version and "-A" represents extended temperature range.

MARKING INFORMATION



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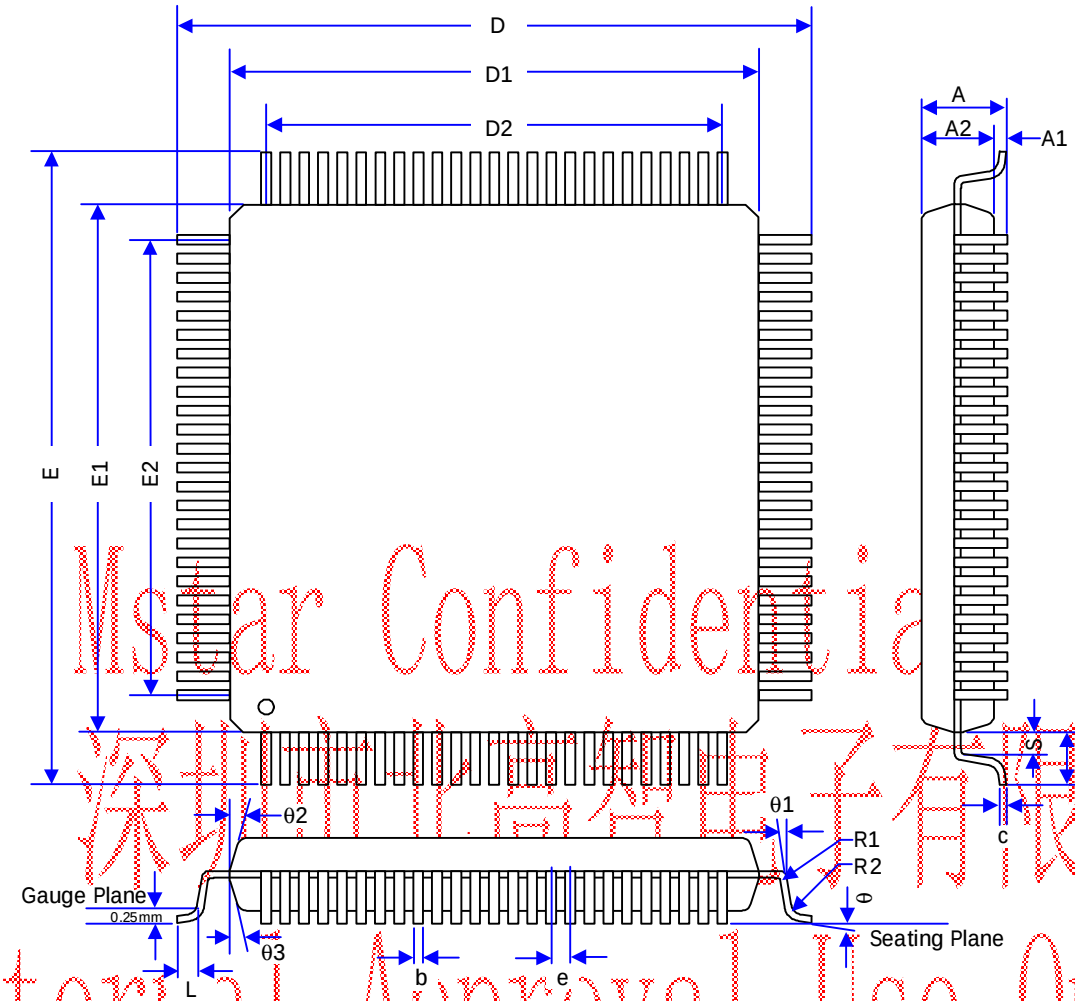
Electrostatic charges accumulate on both test equipment and human body and can discharge without detection. MST720A comes with ESD protection circuitry; however, the device may be permanently damaged when subjected to high energy discharges. The device should be handled with proper ESD precautions to prevent malfunction and performance degradation.

REVISION HISTORY

Document	Description	Date
MST720A_ds_v01	Ÿ Initial release	Nov 2005

MECHANICAL DIMENSIONS



Symbol	Millimeter			Inch		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	-	-	1.60	-	-	0.063
A1	0.05	-	0.15	0.002	-	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
D	16.00 BSC.			0.630 BSC.		
D1	14.00 BSC.			0.551 BSC.		
D2	12.00			0.472		
E	16.00 BSC.			0.630 BSC.		
E1	14.00 BSC.			0.551 BSC.		
E2	12.00			0.472		
R1	0.08	-	-	0.003	-	-
R2	0.08	-	0.20	0.003	-	0.008

Symbol	Millimeter			Inch		
	Min.	Nom.	Max.	Min.	Nom.	Max.
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	-	-	0°	-	-
θ2	11°	12°	13°	11°	12°	13°
θ3	11°	12°	13°	11°	12°	13°
b	0.17	0.20	0.27	0.007	0.008	0.011
c	0.09	-	0.20	0.004	-	0.008
e	0.50 BSC.			0.020 BSC.		
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 Ref			0.039 Ref		
S	0.20	-	-	0.008	-	-

General Description

The AOZ1041 is a high efficiency, simple to use, 1.5A buck regulator. The AOZ1041 works from a 4.5V to 16V input voltage range, and provides up to 1.5A of continuous output current with an output voltage adjustable down to 0.8V.

The AOZ1041 comes in an SO-8 package and is rated over a -40°C to +85°C ambient temperature range.

Features

- 4.5V to 16V operating input voltage range
- 130 mΩ internal PFET switch for high efficiency: up to 95%
- Internal Schottky Diode
- Internal soft start
- Output voltage adjustable to 0.8V
- 1.5A continuous output current
- Fixed 500kHz PWM operation
- Cycle-by-cycle current limit
- Short-circuit protection
- Thermal shutdown
- Small size SO-8 package

Applications

- Point of load dc/dc conversion
- PCIe graphics cards
- Set top boxes
- DVD drives and HDD
- LCD panels
- Cable modems
- Telecom/Networking/Datacom equipment

Typical Application

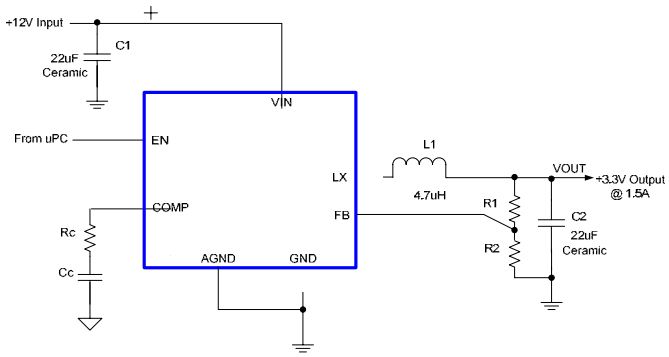
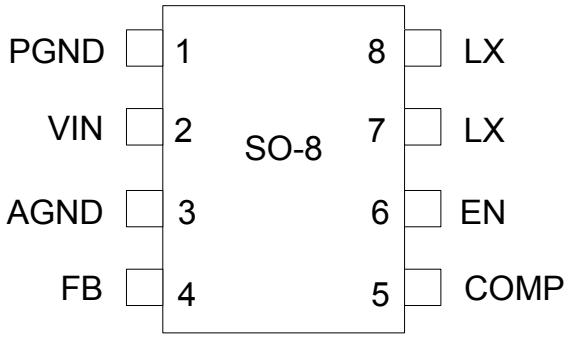


Figure 1. 3.3V/1.5A Buck Down Regulator

Ordering Information

Part Number	Ambient Temperature Range	Package	Environmental
AOZ1041AI	-40°C to +85°C	SO-8	RoHS Compliant

Pin Configuration



Pin Number	Pin Name	Pin Function
1	PGND	Power ground. Electrically needs to be connected to AGND.
2	VIN	Supply voltage input. When VIN rises above the UVLO threshold the device starts up.
3	AGND	Reference connection for controller section. Also used as thermal connection for controller section. Electrically needs to be connected to PGND
4	FB	The FB pin is used to determine the output voltage via a resistor divider between the output and GND.
5	COMP	External loop compensation pin.
6	EN	The enable pin is active high. Connect EN pin to VIN if not used. Do not leave the EN pin floating.
7,8	LX	PWM output connection to inductor. Thermal connection for output stage.

Absolute Maximum Ratings[1]

Supply Voltage (V_{IN}) 18V
LX to AGND ..... -0.7V to V_{IN}+0.3V
EN to AGND ..... -0.3V to V_{IN}+0.3V
FB to AGND ..... -0.3V to 6V
COMP to AGND ..... -0.3V to 6V
PGND to AGND ..... -0.3V to +0.3V
Junction Temperature (T_J) ..... +150°C
Storage Temperature (T_S) ..... -65°C to +150°C

Recommend Operating Ratings[2]

Supply Voltage (V_{IN}) ..... 4.5V to 16V
Output Voltage Range ..... 0.8V to V_{IN}
Ambient Temperature (T_A) ..... -40°C to +85°C
Package Thermal Resistance
SO-8 (Θ_{JA}) ..... 87°C/W

Electrical Characteristics

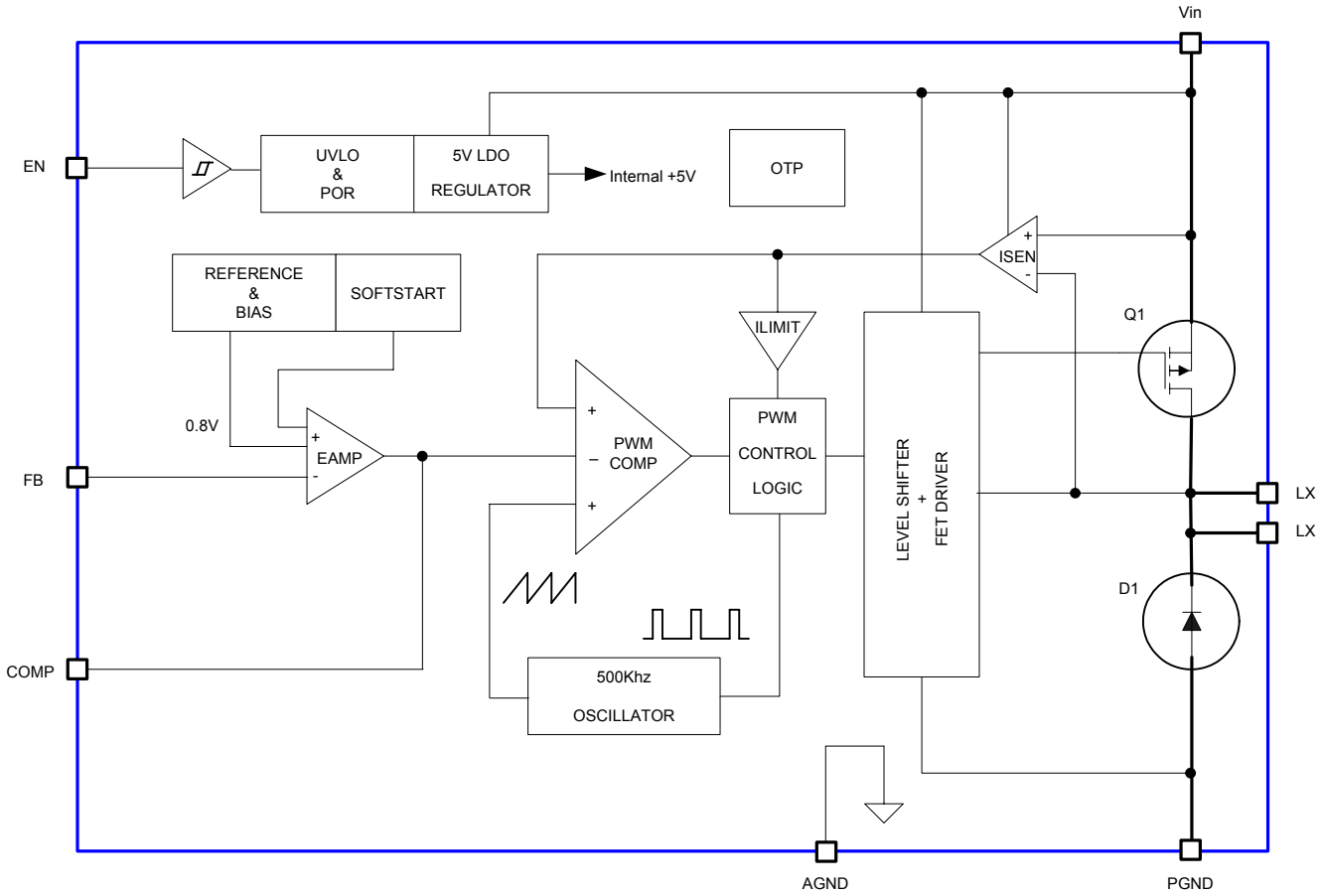
T_A = 25°C, V_{IN} = V_{EN} = 12V, V_{OUT} = 3.3V unless otherwise specified. Specifications in **BOLD** indicate a ambient temperature range of -40°C to +85°C.

Parameter	Symbol	Conditions	MIN	TYP	MAX	UNITS
Supply Voltage	V_{IN}		4.5		16	V
Input under-voltage lockout threshold	V_{UVLO}	V_{IN} rising V_{IN} falling		4.00 3.70		V V
Supply current (Quiescent)	I_{IN}	I_{OUT} = 0, VFB = 1.2V, V_{EN} >1.2V		2	3	mA
Shutdown supply current	I_{OFF}	V_{EN} = 0V		3	20	µA
Feedback Voltage	V_{FB}		0.782	0.8	0.818	V
Load regulation				0.5		**%**
Line regulation				1		**%**
Feedback voltage input current	I_{FB}				200	nA
EN input threshold	V_{EN}	Off threshold On threshold	 2.0		0.8	V V
EN input hysteresis	V_{HYS}			100		mV
Modulator						
Frequency	f_O		380	480	580	kHz
Maximum Duty Cycle	D_{MAX}		100			%
Minimum Duty Cycle	D_{MIN}				6	%
Error amplifier voltage gain				500		V/V
Error amplifier transconductance				200		µA/V
Protection						
Current Limit	I_{LIM}		2.0		3.6	A
Over-temperature shutdown limit		T_J rising T_J falling		155 100		°C °C
Soft Start Interval	t_{SS}			4		ms
Output Stage						
High-side switch on-resistance		V_{IN} = 12V V_{IN} = 5V		97 166	130 200	mΩ mΩ

Notes:

1. Exceeding the Absolute Maximum ratings may damage the device.
2. The device is not guaranteed to operate beyond the Maximum Operating ratings.
3. Devices are inherently ESD sensitive, handling precautions are required. Human body model rating: 1.5KΩ in series with 100pF.

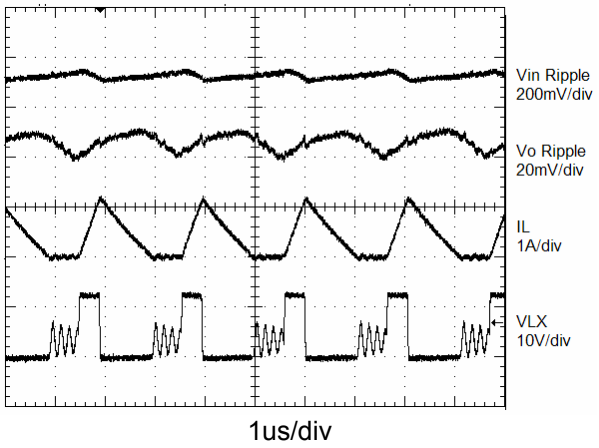
Functional Block Diagram



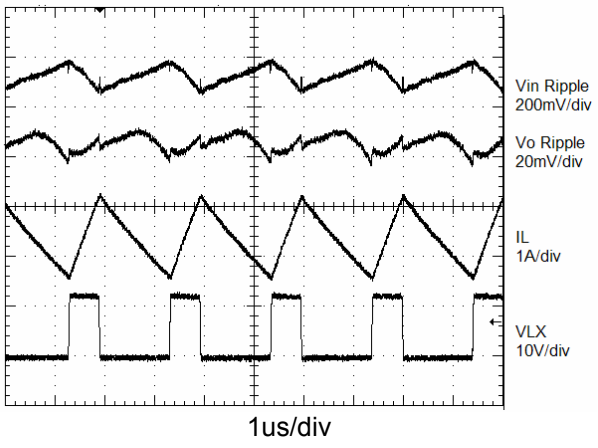
Typical Performance Characteristics

Circuit of figure 1. T_A = 25°C, V_{IN} = V_{EN} = 12V, V_{OUT} = 3.3V unless otherwise specified.

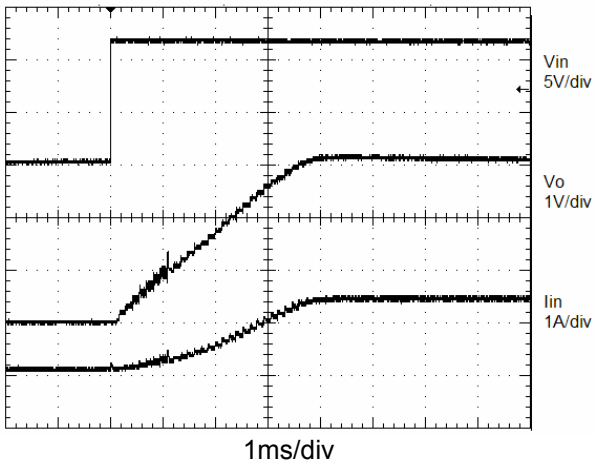
Light load (DCM) operation



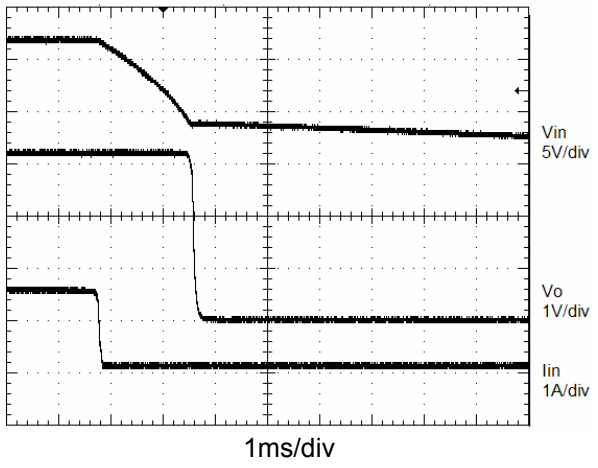
Full load (CCM) operation



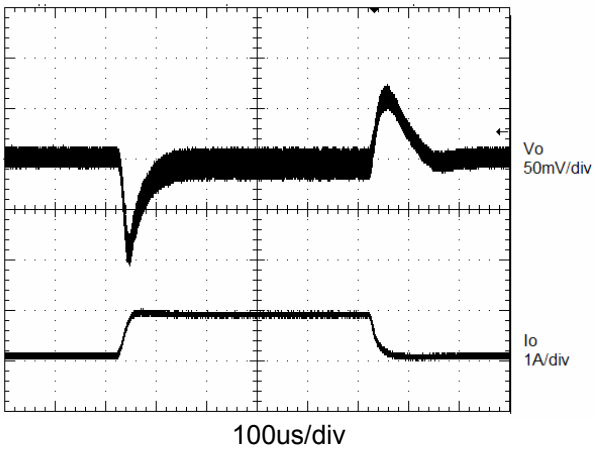
Start up to full load



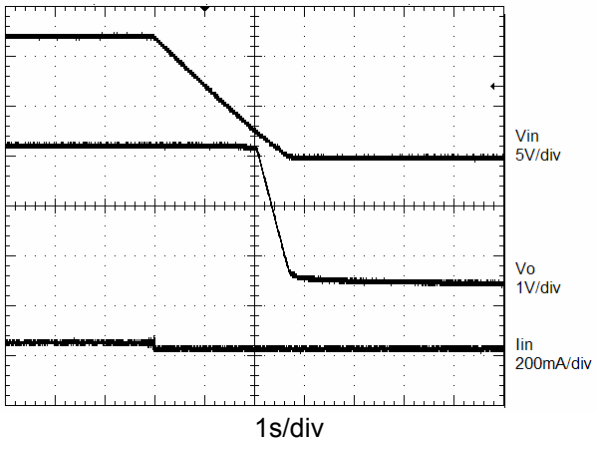
Full load to turn off



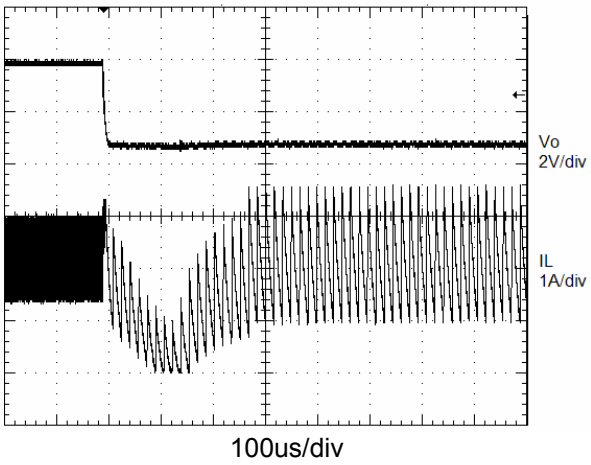
Load transient



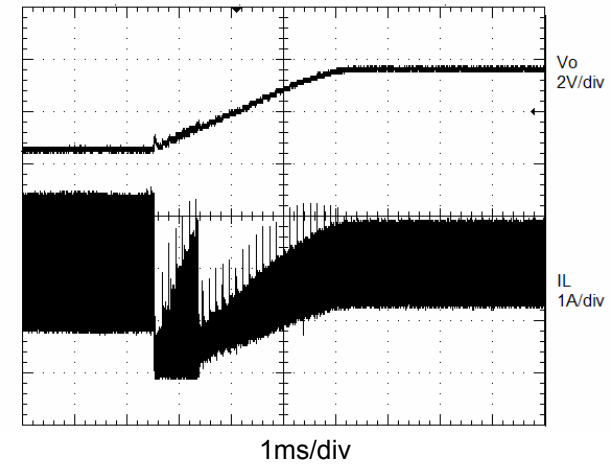
Light load to turn off



Short circuit protection



Short circuit recovery



Efficiency vs. load current

Detailed Description

The AOZ1041 is a current-mode step down regulator with integrated high side PMOS switch and a low side freewheeling Schottky diode. It operates from a 4.5V to 16V input voltage range and supplies up to 1.5A of load current. The duty cycle can be adjusted from 6% to 100% allowing a wide range of output voltage. Features include enable control, Power-On Reset, input under voltage lockout, output over voltage protection, fixed internal soft-start and thermal shut down.

The AOZ1041 is available in SO-8 package.

Enable and Soft Start

The AOZ1041 has internal soft start feature to limit in-rush current and ensure the output voltage ramps up smoothly to regulation voltage. A soft start process begins when the input voltage rises to 4.0V and voltage on EN pin is HIGH. In soft start process, the output voltage is ramped to regulation voltage in typically 4ms. The 8ms soft start time is set internally.

The EN pin of the AOZ1041 is active high. Connect the EN pin to VIN if enable function is not used. Pull it to ground will disable the AOZ1041. Do not leave it open. The voltage on EN pin must rise above 2.0 V to enable the AOZ1041. When voltage on EN pin falls below 0.8V, the AOZ1041 is disabled. If an application circuit requires the AOZ1041 to be disabled, an open drain or open collector circuit should be used to interface to EN pin.

Steady-State Operation

Under steady-state conditions, the converter operates in fixed frequency and Continuous-Conduction Mode (CCM).

The AOZ1041 integrates an internal P-MOSFET as the high-side switch. Inductor current is sensed by amplifying the voltage drop across the drain to source of the high side power MOSFET. Output voltage is divided down by the external voltage divider at the FB pin. The difference of the FB pin voltage and reference is amplified by the internal transconductance error amplifier. The error voltage, which shows on the COMP pin, is compared against the current signal, which is sum of inductor current signal and ramp compensation signal, at PWM comparator input. If the current signal is less than the error voltage, the internal high-side switch is on. The inductor current flows from the input through the inductor to the output. When the current signal exceeds the error voltage, the high-side switch is off. The inductor current is freewheeling through the internal Schottky diode to output.

The AOZ1041 uses a P-Channel MOSFET as the upper switch. It saves the bootstrap capacitor normally seen in a circuit which is using an NMOS switch. It allows 100% turn-on of the upper switch to achieve linear regulation mode of operation. The minimum voltage drop from V_{IN} to V_O is the load current times DC resistance of MOSFET plus DC resistance of buck inductor. It can be calculated by equation below:

$$V_{O\_MAX} = V_{IN} - I_O \times R_{DS(ON)}$$

Where V_{O_MAX} is the maximum output voltage;
V_{IN} is the input voltage from 4.5V to 16V;
I_O is the output current from 0A to 1.5A;
$R_{DS(ON)}$ is the on resistance of internal MOSFET, the value is between 97mΩ and 200mΩ depending on input voltage and junction temperature;

Switching Frequency

The AOZ1041 switching frequency is fixed and set by an internal oscillator. The practical switching frequency could range from 380 kHz to 580 kHz due to device variation.

Output Voltage Programming

Output voltage can be set by feeding back the output to the FB pin by using a resistor divider network. In the application circuit shown in Figure 1. The resistor divider network includes R_1 and R_2. Usually, a design is started by picking a fixed R_2 value and calculating the required R1 with equation below.

$$V_O = 0.8 \times (1 + \frac{R_1}{R_2})$$

Some standard value of R_1, R_2 and most used output voltage values are listed in Table 1.

Table 1.

Vo (V)	R1 (kΩ)	R2 (kΩ)
0.8	1.0	open
1.2	4.99	10
1.5	10	11.5
1.8	12.7	10.2
2.5	21.5	10
3.3	31.1	10
5.0	52.3	10

Combination of R1 and R2 should be large enough to avoid drawing excessive current from the output, which will cause power loss.

Since the switch duty cycle can be as high as 100%, the maximum output voltage can be set as high as the input voltage minus the voltage drop on upper PMOS and inductor.

Protection Features

The AOZ1041 has multiple protection features to prevent system circuit damage under abnormal conditions.

Over Current Protection (OCP)

The sensed inductor current signal is also used for over current protection. Since the AOZ1041 employs peak current mode control, the COMP pin voltage is proportional to the peak inductor current. The COMP pin voltage is limited to be between 0.4V and 2.5V internally. The peak inductor current is automatically limited cycle by cycle.

When the output is shorted to ground under fault conditions, the inductor current decays very slow during a switching cycle because of V_o=0V. To prevent catastrophic failure, a secondary current limit is designed inside the AOZ1041. The measured inductor current is compared against a preset voltage which represents the current limit, between 2.5A and 3.6A. When the output current is more than current limit, the high side switch will be turned off and EN pin will be pulled down. The converter will initiate a soft start once the over-current condition disappears.

Power-On Reset (POR)

A power-on reset circuit monitors the input voltage. When the input voltage exceeds 4V, the converter starts operation. When input voltage falls below 3.7V, the converter will be shut down.

Thermal Protection

An internal temperature sensor monitors the junction temperature. It shuts down the internal control circuit and high side PMOS if the junction temperature exceeds 155ºC. The regulator will restart automatically under the control of soft-start circuit when the junction temperature decreases to 100ºC.

Application Information

The basic AOZ1041 application circuit is show in Figure 1. Component selection is explained below.

Input capacitor

The input capacitor must be connected to the V_{IN} pin and PGND pin of the AOZ1041 to maintain steady input voltage and filter out the pulsing input current. The voltage rating of input capacitor must be greater than maximum input voltage plus ripple voltage.

The input ripple voltage can be approximated by equation below:

$$\Delta V_{IN} = \frac{I_O}{f \times C_{IN}} \times (1 - \frac{V_O}{V_{IN}}) \times \frac{V_O}{V_{IN}}$$

Since the input current is discontinuous in a buck converter, the current stress on the input capacitor is another concern when selecting the capacitor. For a buck circuit, the RMS value of input capacitor current can be calculated by:

$$I_{CIN\_RMS} = I_O \times \sqrt{\frac{V_O}{V_{IN}}(1 - \frac{V_O}{V_{IN}})}$$

if we let *m* equal the conversion ratio:

$$\frac{V_O}{V_{IN}} = m$$

The relation between the input capacitor RMS current and voltage conversion ratio is calculated and shown in Fig. 2 below. It can be seen that when V_O is half of V_{IN}, C_{IN} is under the worst current stress. The worst current stress on C_{IN} is $0.5 \cdot I_O$.

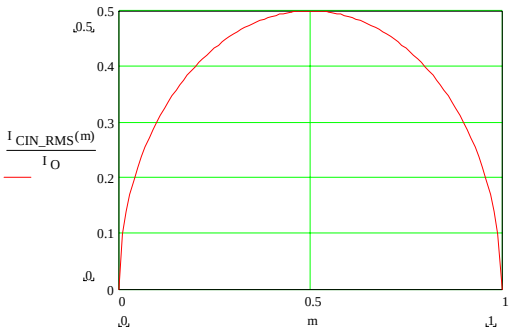


Figure 2. I_{CIN} vs. voltage conversion ratio

For reliable operation and best performance, the input capacitors must have current rating higher than $I_{CIN-RMS}$ at worst operating conditions. Ceramic capacitors are preferred for input capacitors because of their low ESR and high current rating. Depending on the application circuits, other low ESR tantalum capacitor may also be used. When selecting ceramic capacitors, X5R or X7R type dielectric ceramic capacitors should be used for their better temperature and voltage characteristics. Note that the ripple current rating from capacitor manufactures are based on certain amount of life time. Further de-rating may be necessary in practical design.

Inductor

The inductor is used to supply constant current to output when it is driven by a switching voltage. For given input and output voltage, inductance and switching frequency together decide the inductor ripple current, which is,

$$\Delta I_L = \frac{V_O}{f \times L} \times (1 - \frac{V_O}{V_{IN}})$$

The peak inductor current is:

$$I_{Lpeak} = I_O + \frac{\Delta I_L}{2}$$

High inductance gives low inductor ripple current but requires larger size inductor to avoid saturation. Low ripple current reduces inductor core losses. It also reduces RMS current through inductor and switches, which results in less conduction loss. Usually, peak to peak ripple current on inductor is designed to be 20% to 30% of output current.

When selecting the inductor, make sure it is able to handle the peak current without saturation even at the highest operating temperature.

The inductor takes the highest current in a buck circuit. The conduction loss on inductor need to be checked for thermal and efficiency requirements.

Surface mount inductors in different shape and styles are available from Coilcraft, Elytone and Murata. Shielded inductors are small and radiate less EMI noise. But they cost more than unshielded inductors. The choice depends on EMI requirement, price and size.

Table below lists some inductors for typical output voltage design.

Table 2.

Vout	L1	Manufacture
5.0 V	Unshielded, 4.7uH LQH55DN4R7M03	MURATA
	Shielded, 4.7uH LQH66SN4R7M03	MURATA
	Shield, 5.8uH ET553-5R8	ELYTONE
	Un-shielded, 4.7uH DO3316P-472MLD	Coilcraft
3.3 V	Unshielded, 4.7uH LQH55DN3R3M03	MURATA
	Shield, 4.7uH LQH66SN3R3M03	MURATA
	Shield, 3.3uH ET553-3R3	ELYTONE
	Un-shielded, 4.7uH DO3316P-472MLD	Coilcraft
	Un-shielded, 4.7uH DO1813P-472HC	Coilcraft
1.8 V	Unshielded, 2.2uH LQH55DN1R5M03	MURATA
	Shield, 2.2uH LQH66SN1R5M03	MURATA
	Shield, 2.2uH ET553-2R2	ELYTONE
	Un-shielded, 2.2uH DO3316P-222MLD	Coilcraft
	Un-shielded, 2.2uH DO1813P-222HC	Coilcraft

Output Capacitor

The output capacitor is selected based on the DC output voltage rating, output ripple voltage specification and ripple current rating.

The selected output capacitor must have a higher rated voltage specification than the maximum desired output voltage including ripple. De-rating needs to be considered for long term reliability.

Output ripple voltage specification is another important factor for selecting the output capacitor. In a buck converter circuit, output ripple voltage is determined by inductor value, switching frequency, output capacitor value and ESR. It can be calculated by the equation below:

$$\Delta V_O = \Delta I_L \times (ESR_{CO} + \frac{1}{8 \times f \times C_O})$$

where C_O is output capacitor value and ESR_{CO} is the Equivalent Series Resistor of output capacitor. When low ESR ceramic capacitor is used as output capacitor, the impedance of the capacitor at the switching frequency dominates. Output ripple is mainly caused by capacitor value and inductor ripple current. The output ripple voltage calculation can be simplified to:

$$\Delta V_O = \Delta I_L \times \frac{1}{8 \times f \times C_O}$$

If the impedance of ESR at switching frequency dominates, the output ripple voltage is mainly decided by capacitor ESR and inductor ripple current. The output ripple voltage calculation can be further simplified to:

$$\Delta V_O = \Delta I_L \times ESR_{CO}$$

For lower output ripple voltage across the entire operating temperature range, X5R or X7R dielectric type of ceramic, or other low ESR tantalum are recommended to be used as output capacitors.

In a buck converter, output capacitor current is continuous. The RMS current of output capacitor is decided by the peak to peak inductor ripple current. It can be calculated by:

$$I_{CO\_RMS} = \frac{\Delta I_L}{\sqrt{12}}$$

Usually, the ripple current rating of the output capacitor is a smaller issue because of the low current stress. When the buck inductor is selected to be very small and inductor ripple current is high, output capacitor could be overstressed.

Loop Compensation

The AOZ1041 employs peak current mode control for easy use and fast transient response. Peak current mode control eliminates the double pole effect of the output L&C filter. It greatly simplifies the compensation loop design.

With peak current mode control, the buck power stage can be simplified to be a one-pole and one-zero system in frequency domain. The pole is dominant pole can be calculated by:

$$f_{P1} = \frac{1}{2\pi \times C_O \times R_L}$$

The zero is a ESR zero due to output capacitor and its ESR. It is can be calculated by:

$$f_{Z1} = \frac{1}{2\pi \times C_O \times ESR_{CO}}$$

Where C_O is the output filter capacitor;
R_L is load resistor value;
ESR_{CO} is the equivalent series resistance of output capacitor;

The compensation design is actually to shape the converter control loop transfer function to get desired gain and phase. Several different types of compensation network can be used for AOZ1041. For most cases, a series capacitor and resistor network connected to the COMP pin sets the pole-zero and is adequate for a stable high-bandwidth control loop.

In the AOZ1041, FB pin and COMP pin are the inverting input and the output of internal error amplifier. A series R and C compensation network connected to COMP provides one pole and one zero. The pole is:

$$f_{P2} = \frac{G_{EA}}{2\pi \times C_C \times G_{VEA}}$$

Where G_{EA} is the error amplifier transconductance, which is $200 \cdot 10^{-6}$ A/V;
G_{VEA} is the error amplifier voltage gain, which is 500 V/V;
C_C is compensation capacitor;

The zero given by the external compensation network, capacitor C_C and resistor R_C, is located at:

$$f_{Z2} = \frac{1}{2\pi \times C_C \times R_C}$$

To design the compensation circuit, a target crossover frequency f_C for close loop must be selected. The system crossover frequency is where control loop has unity gain. The crossover is the

also called the converter bandwidth. Generally a higher bandwidth means faster response to load transient. However, the bandwidth should not be too high because of system stability concern. When designing the compensation loop, converter stability under all line and load condition must be considered.

Usually, it is recommended to set the bandwidth to be equal or less than 1/10 of switching frequency. The AOZ1041 operates at a fixed 500kHz switching frequency. It is recommended to choose a crossover frequency equal or less than 50kHz.

$$f_C = 50kHz$$

The strategy for choosing R_C and C_C is to set the cross over frequency with R_C and set the compensator zero with C_C. Using selected crossover frequency, f_C, to calculate R_C:

$$R_C = f_C \times \frac{V_O}{V_{FB}} \times \frac{2\pi \times C_O}{G_{EA} \times G_{CS}}$$

where f_C is desired crossover frequency. For best performance, fc is set to be about 1/10 of switching frequency;
V_{FB} is 0.8V;
G_{EA} is the error amplifier transconductance, which is $200 \cdot 10^{-6}$ A/V;
G_{CS} is the current sense circuit transconductance, which is 6.68 A/V;

The compensation capacitor C_C and resistor R_C together make a zero. This zero is put somewhere close to the dominate pole f_{p1} but lower than 1/5 of selected crossover frequency. C_C can is selected by:

$$C_C = \frac{1.5}{2\pi \times R_C \times f_{P1}}$$

Equation above can also be simplified to:

$$C_C = \frac{C_O \times R_L}{R_C}$$

An easy-to-use application software which helps to design and simulate the compensation loop can be found at www.aosmd.com.

Thermal management and layout consideration

In the AOZ1041 buck regulator circuit, high pulsing current flows through two circuit loops. The first loop starts from the input capacitors, to the VIN pin, to the LX pins, to the filter inductor, to the output capacitor and load, and then return to the input capacitor through ground. Current flows in the first loop when the high side switch is on. The second loop starts from inductor, to the output capacitors and load, to the PGND pin of the AOZ1041, to the LX pins of the AOZ1041. Current flows in the second loop when the low side diode is on.

In PCB layout, minimizing the two loops area reduces the noise of this circuit and improves efficiency. A ground plane is strongly recommended to connect input capacitor, output capacitor, and PGND pin of the AOZ1041.

In the AOZ1041 buck regulator circuit, the two major power dissipating components are the AOZ141 and output inductor. The total power dissipation of converter circuit can be measured by input power minus output power.

$$P_{total} = V_{IN} \cdot I_{IN} - V_O \cdot I_O$$

The power dissipation of inductor can be approximately calculated by output current and DCR of inductor.

$$P_{indcutor} = I_O^{\,2} \cdot R_{inductor} \cdot 1.1$$

The actual junction temperature can be calculated with power dissipation in the AOZ1041 and thermal impedance from junction to ambient.

$$T_{junction} = (P_{total} - P_{inductor}) \cdot \Theta_{JA}$$

The maximum junction temperature of AOZ1041 is 150ºC, which limits the maximum load current capability. Please see the thermal de-rating curves for the maximum load current of the AOZ1041 under different ambient temperature.

The thermal performance of the AOZ1041 is strongly affected by the PCB layout. Extra care should be taken by users during design to ensure that the IC will operate under the recommended environmental conditions.

Several layout tips are listed below for the best electric and thermal performance:

1. Do not use thermal relief connection to the VIN and the PGND pin. Pour a maximized copper

area to the PGND pin and the VIN pin to help thermal dissipation.

2. Input capacitor should be connected to the VIN pin and the PGND pin as close as possible.
3. A ground plane is preferred. If a ground plane is not used, separate PGND from AGND and connect them only at one point to avoid the PGND pin noise coupling to the AGND pin.
4. Make the current trace from LX pins to L to Co to the PGND as short as possible.
5. Pour copper plane on all unused board area and connect it to stable DC nodes, like VIN, PGND or SGND.
6. Keep sensitive signal trace away from switching node, LX. The copper pour area connected to the LX pin should be as small as possible to avoid the switching noise on the LX pin coupling to other part of circuit.
7. The AOZ1041-EVA document provides an example of proper layout techniques.

KTMicro, Inc.

Monolithic Digital Stereo FM Transmitter Radio-Station-on-a-Chip™

KT0801

▪ Features

Professional Grade System-on-a-Chip (SoC) High-Fidelity Stereo Audio FM Transmitter:
- **SNR ≥ 68 dB**
- **Stereo Separation > 50dB**
- **International compatible 76MHz ~ 108MHz**

Minimal External Component Requirement:
- **Crystal optional (in lieu of direct feeding of an external clock)**

Ultra-Low Power Consumption:
- **< 12.6 mA operation current**
- **< 1 μA standby current**

Dual Reference Clock Setup:
- **Supports both 7.6MHz and 15.2MHz**

Small Form factor:
- **24-pin 4x4x0.9 mm QFN (Pb-free and RoHS Compliant)**

Simple Interface:
- **Single 1.8V (in lieu of 1.6~3.6V regulator feed)**
- **Industry standard 2-wire I^2C MCU interface compatible**

Advanced Digital Audio Signal Processing:
- **On-chip 20-bit ΔΣ Audio ADC**
- **On-chip DSP core**
- **On-chip 24dB PGA**
- **Automatic calibration against process and temperature**

On-Chip LDO (low-drop-out) regulator:
- **Accommodates 1.6V ~ 3.6V supply**

Programmable transmit level

Programmable pre-emphasis (50/75 μs)

Applications

MP3 Players
Cellular Phones
PDAs
Portable Personal Media player
Laptop Computers
Wireless Speakers

Rev. 1.1

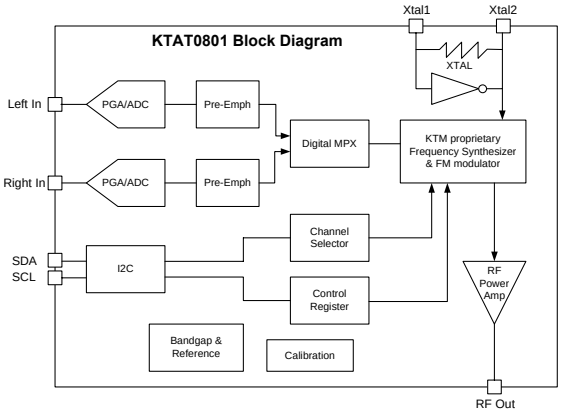


Figure 1: KT0801 System Diagram

▪ General Description

The KT Micro KT0801 Monolithic Digital FM Transmitter is designed to process high-fidelity stereo audio signal and transmit modulated FM signal over a short range. The modulated stereo FM signal can be intercepted and played back using any FM radio worldwide.

The KT0801 features dual 20-bit ΔΣ audio ADCs, a high-fidelity digital stereo audio processor and a fully integrated radio frequency (RF) transmitter. An on-chip low-drop-out regulator (LDO) allows the chip to be integrated in a wide range of low-voltage battery-operated systems with power supply ranging from 1.6V to 3.6V.

The KT0801 is configured as an I^2C slave and programmed through the industry standard 2-wire MCU interface.

Thanks to its high integration level, the KT0801 is mounted in a generic 24-pin 4x4 QFN package and only requires a single low-voltage supply and a small-form-factor crystal (7.6MHz or 15.2MHz) or an external clock to operate.

No external tuning is required that makes design-in effort minimum.

KT Micro Inc., 22391 Gilberto, Suite D
Rancho Santa Margarita, CA 92688
Tel: 949.713.4000 **www.ktmicro.com**
Fax: 949.713.404

▪ Operation Condition

Table 1: Operation Condition

Parameter	Symbol	Operating Condition	Min	Typ	Max	Units
1.8V Analog Supply[1]	VDD	Relative to GND	1.6	1.8	2.0	V
IO/Regulator Supply	IOVDD	Relative to GND	1.6		3.6	V
Operating Temp	T_A	Ambient Temperature	-30	25	85	°C
Note: 1. When LDO enabled, no external voltage should be applied to this 1.8V supply.						

▪ Specifications and Features

Table 2: FM Transmitter Functional Parameters (Unless otherwise noted TA = -30~85 °C, IOVDD=1.6~3.6 V with LDO enabled, F_{in} = 1 kHz)

Parameter	Symbol	Test/Operating Condition	Min	Nom	Max	Units
FM Frequency Range	F_{tx}	Pin 19	76		108	MHz
Current Consumption	I_{VDD}	Pin 1 with PA (power amp.) at default power mode	-	10	12.6	mA
Standby Current	I_{stand}	Pin 1	-	0.1	1	µA
Signal to Noise Ratio	SNR	V_{in} = 0.7 V_{p-p}, G_{in} = 0	-	68	-	dB
Total Harmonic Distortion	THD	V_{in} = 0.7 V_{p-p}, G_{in} = 0	-	0.1		%
Left/Right Channel Balance	BAL	V_{in} = 0.7 V_{p-p}, G_{in} = 0	-0.2	-	0.2	dB
Stereo Separation (Left<->Right)	SEP	V_{in} = 0.7 V_{p-p}, G_{in} = 0	50	60	-	dB
Sub Carrier Rejection Ratio	SCR	V_{in} = 0.7 V_{p-p}, G_{in} = 0	-	-	-60	dB
Input Swing[1]	V_{in}	Single-ended input	-	0.3	1.2	V_{RMS}
PGA Range for Audio Input	G_{in}		-12	0	12	dB
PGA Gain Step for Audio Input	G_{step}			4		dB
Required Input Common-Mode Voltage when DC-coupled	V_{cm}	Pin 4, 6	0	0.8	1.8	V
Power Supply Rejection[2]	PSRR	IOVDD = 1.9 ~ 3.6 V	40	-	-	dB
Ground Bounce Rejection[2]	GSRR	IOVDD = 1.9 ~ 3.6 V	40	-	-	dB
Input Resistance (Audio Input)	R_{in}	Pin 4, 6	120	150	180	kΩ
Input Capacitance (Audio Input)	C_{in}	Pin 4, 6	0.5	0.8	1.2	pF
Audio Input Frequency Band	F_{in}	Pin 4, 6	20	-	15k	Hz
Transmit Level	V_{out}	Spectrum analyzer (50 Ω)	93	99	104	dBµV
Channel Step	STEP		-	100		kHz
Pre-emphasis Time Constant	T_{pre}	SIG_PROC<1> = 1	-	50	-	µs
		SIG_PROC<0> = 0	-	75	-	µs
Crystal/External Clock	CLK	Dual-frequency setup	-	7.6 or 15.2	-	MHz
2-wire I^2C Clock	SCL	Pin 17	0	100	400	kHz
High Level Input Voltage	V_{IH}	Pin 3, 9, 10, 12, 13, 16, 17, 24	0.75 x IOVDD	-	IOVDD + 0.25	V
Low Level Input Voltage	V_{IL}	Pin 3, 9, 10, 12, 13, 16, 17, 24	- 0.25	-	0.25 x IOVDD	V

Notes:
1. Maximum is given on the condition of PGA gain = -12dB.
2. Fin = 20 ~ 15k Hz.

Package and Pin List

A 24-pin QFN package is used. The chip IO pin-out is listed in Table 3.

Table 3 KT0801 Pin-Out

Pin Index	Name	I/O Type	Function
1	IOVDD	Power	1.6~3.3V external logic IOVDD or Regulator high supply input.
2, 14, 18, 22	VDD	Power	1.8V supply. No external voltage shall be applied with regulator enabled. All four pins shall be shorted on the PCB.
3	HF	Digital Input	"1" to enable 15.2MHz XTAL mode. Default "0", 7.6MHz XTAL mode.
4	INL	Analog Input	Left channel audio input.
5, 11, 15, 20, 21	GND	Ground	Ground.
6	INR	Analog Input	Right channel audio input.
7	NC1	N/A	Reserved. Do not connect.
8	NC2	N/A	Reserved. Do not connect.
9	SW1	Digital Input	Control bit. Chip enable, supply mode and clock source.
10	SW2	Digital Input	Control bit. Chip enable, supply mode and clock source.
12	RSTB	Digital Input	Reset (active low).
13	ADDR	Digital Input	Set the 4th I2C address bit (MSB being the 1st bit).
16	SDA	Digital I/O	Serial data I/O.
17	SCL	Digital I/O	Serial clock input.
19	PA_OUT	Analog Output	FM RF output.
23	XI	Analog I/O	Crystal input.
24	XO/RCLK	Analog I/O	Crystal input or external reference clock input.

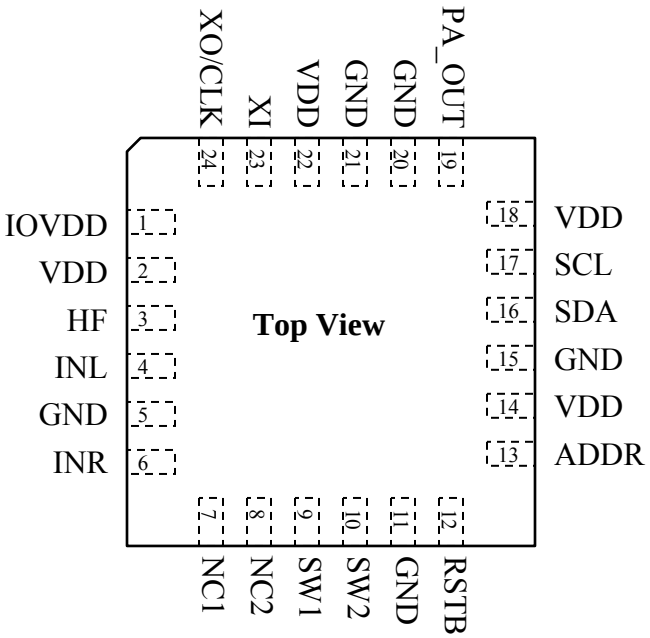


Figure 2: KT0801 Pin-out: 4x4 24-Pin QFN Package.

▪ I²C Compatible 2-Wire Serial Interface

General Descriptions

The serial interface consists of a serial controller and registers. An internal address decoder transfers the content of the data into appropriate registers. Both the write and read operations are supported according to the following protocol:

The write operation is accomplished via a 3-byte sequence:

Serial address with write command
Register address
Register data

The read operation is accomplished via a 4-byte sequence:

Serial address with write command
Register address
Serial address with read command
Register data

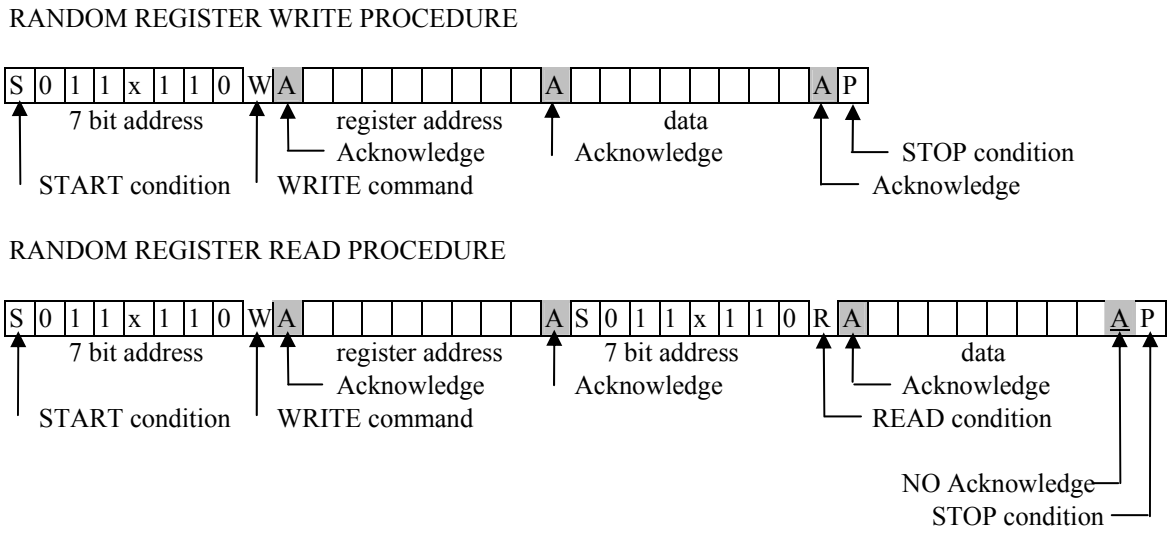


Figure 3: Serial Interface Protocol

The x is the optional 4th MSB bit address code that is set by the ADDR pin and is provided to allow a dual-transmitter-single-controller configuration that will enable multi-channel surround sound applications. ADDR must be externally tied to ground or IOVDD for low or high setup, respectively. The serial controller supports slave mode only. Any register can be addressed randomly.

Slave Mode Protocol

With reference to the clocking scheme shown in Figure 4, the serial interface operates in the following manner:

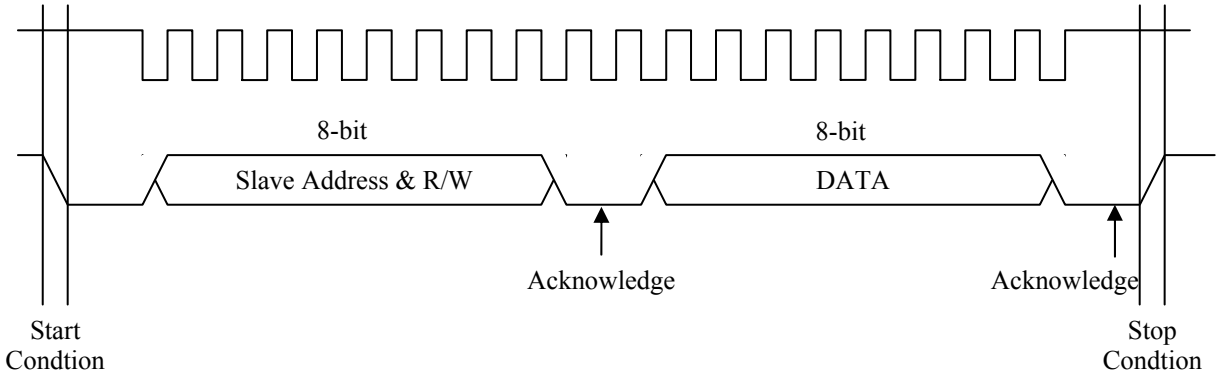


Figure 4: Serial Interface Slave Mode Protocol

A START condition is defined as a HIGH to LOW transition on the data line while the SCLK line is held high. After this has been transmitted by the controller (Master), the bus is considered busy. The next byte of data transmitted after the start condition contains the address of the slave in the first 7 bits and the 8th bit tells whether the master is receiving data from the slave or transmitting data to the slave. When ADDR is set to "0" (i.e. tied to ground), the I^2C write address is 0x6C and the read address is 0x6D.

Data transfer with acknowledge is obligatory. The transmitter must release the SDA line during the acknowledge pulse. The receiver must then pull the SDA line LOW so that it remains stable during the HIGH period of the acknowledge clock pulse. A receiver that has been addressed is obligated to generate an acknowledge signal after each byte of data has been received.

▪ Register Bank

The register bank stores channel frequency codes, calibration parameters, operation status, mode and power controls, which can be accessed by the internal digital controller, state machines and external micro controllers through the serial interface.

All registers are 8 bits wide. Control logics are active high unless specifically noted.

CH_SEL0 (Address: 0x00, Default: 0x81)

Bits	Type	Default	Label	Description
7:0	RW	0x81	CHSEL[7:0]	FM Channel Selection[7:0]

CHSEL[10:0] definition : Channel selection code. 0 to 108 MHz with 100 kHz step. 0x000 corresponds to 0Hz; 0x001 corresponds to 100 kHz, and so on.

CH_SEL1 (Address: 0x01, Default: 0x03)

Bits	Type	Default	Label	Description
7:6	RW	0x0	RFGAIN[1:0]	Transmission Range Adjust 00: Lowest Range 01: Low Range 10: High Range 11: Highest Range

Bits	Type	Default	Label	Description
5:3	RW	0x0	PGA[2:0]	Input Audio Gain Control 111: 12dB 110: 8dB 101: 4dB 100: 0dB 000: 0dB 001: -4dB 010: -8dB 011: -12dB
2:0	RW	0x3	CHSEL[10:8]	FM Channel Selection[10:8]

SIG_PROC (Address: 0x02, Default: 0x00)

Bits	Type	Default	Label	Description
7:4	RW	0x0	NA	Reserved
3	RW	0	MUTE	Software control of Mute 1: MUTE Enable 0: MUTE Disable
2	RW	0	PLTADJ	Pilot Tone Amplitude Adjustment 1: Amplitude high 0: Amplitude low
1	RW	0	NA	Reserved
0	RW	0	PHTCNST	Pre-Emphasis Time-Constant Set 1: 50uS (Europe, Australia) 0: 75uS (USA, Japan)

PA_PWR (Address: 0x13, Default: 0x00)

Bits	Type	Default	Label	Description
7	RW	0	PA_HI_PW	PA (Power amplifier) power (combined with CH_SEL1<7:6> to set up transmission range) 1: Enable high power 0: Disable high power
6:0	RW	0x0	NA	Reserved

Chip Enable and Mode Control (Pin 9 and 10)

There are 2 external Pins SW1 and SW2 (Pin 9 and 10) which enable chip and define the supply voltage level and clock source of the chip. The definition is shown in Table 4.

Table 4: Pin SW1 and SW2 vs. Chip Supply and Clock Source

Input SW1/2	Chip Mode	Chip Supply	Clock Source
00	Disabled	N/A	External
01	Bypass XTAL	Lo-V (1.6~2.0V)	External
10	LDO Disabled	Lo-V (1.6~2.0V)	XTAL
11	LDO Enabled	Hi-V (1.6~3.6V)	XTAL

Application note 1: In low supply mode (1.6 ~ 2.0V) and operate with LDO disabled, tie SW2 to ground and use SW1 as the chip enable. For high supply mode and operate with LDO enabled, short SW2 to SW1 and use both as chip enable.

Application note 2: In low supply mode, IOVDD (Pin 1) shall be tied to the system supply which is equal to the logic level "High" from the MCU/system.

▪ Typical Application Circuits

The KTAT08001 can be integrated in a wide range of systems by requiring only a single power supply. Figure 5 shows a configuration with zero external components. Figure 6 and Figure 7 show two typical configurations in 1.8V and 3.3Vsystems, respectively.

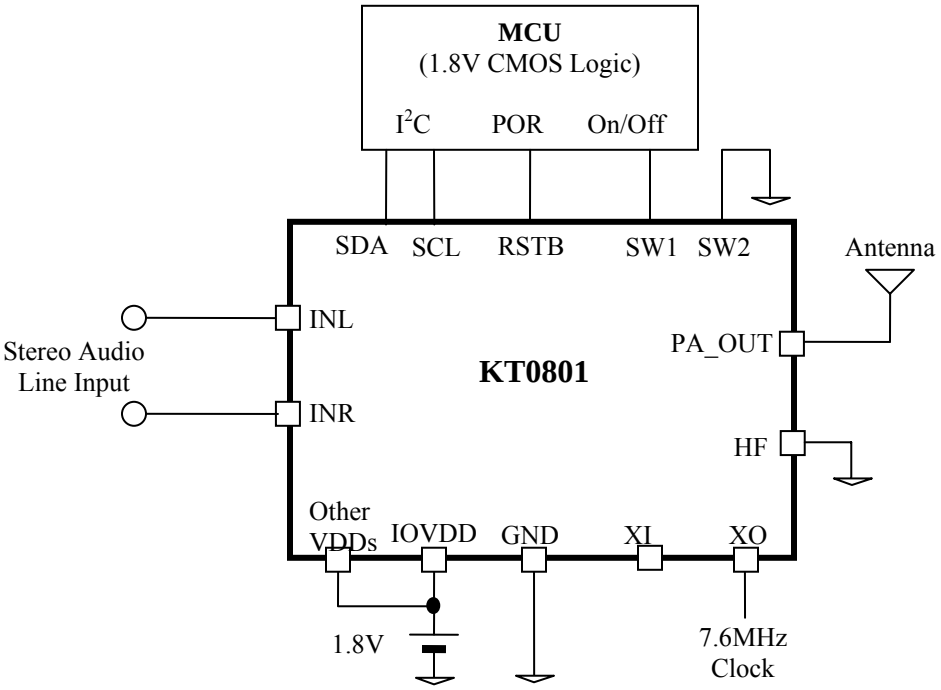


Figure 5: Zero external components configuration in 1.8V systems.

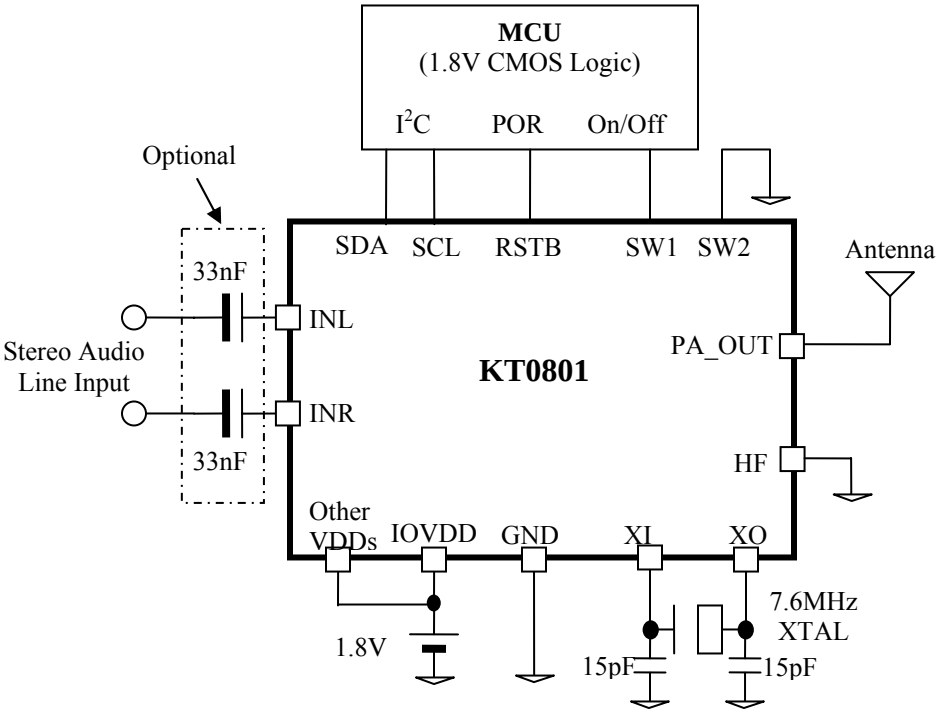


Figure 6: Typical Application configuration in 1.8V systems.

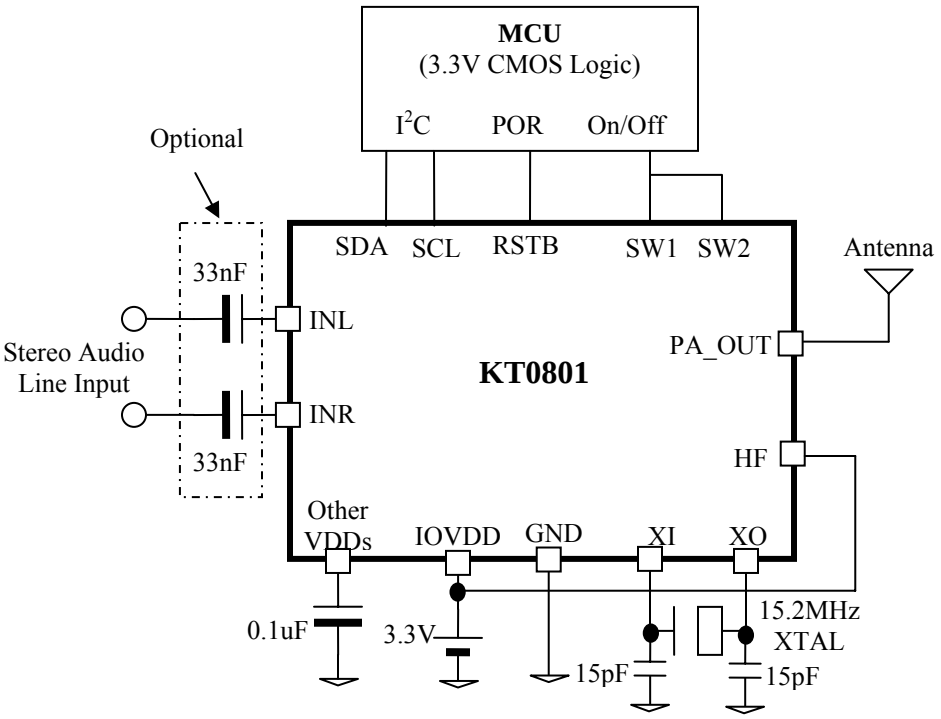
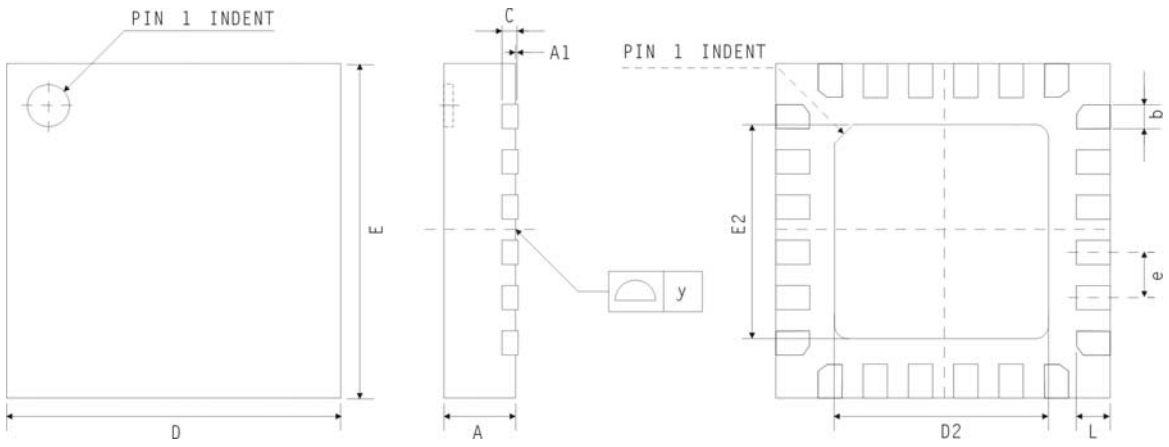


Figure 7: Typical Application configuration in 3.3V system.

▪ Package Outline



Symbols	(MILLIMETERS)		
	MIN	NOM	MAX
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
b	0.20	0.25	0.30
C	0.19	0.20	0.25
D	3.95	4.00	4.05
D2	2.65	2.70	2.75
E	3.95	4.00	4.05
E2	2.65	2.70	2.75
e	-	0.5	-
L	0.30	0.40	0.50
y	0.00	-	0.076

PS25LV512 / PS25LV010

512 Kbit / 1 Mbit 3.0 Volt-only, Serial Flash Memory With 33 MHz SPI Bus Interface

FEATURES

• Single Power Supply Operation
- Voltage range: 3.0V - 3.6V

• Memory Organization
- PS25LV512: 64K x 8 (512 Kbit)
- PS25LV010: 128K x 8 (1 Mbit)

• Cost Effective Sector/Block Architecture
- Uniform 4 Kbyte sectors
- Uniform 32 Kbyte blocks (8 sectors per block)
- Two blocks with 32 Kbytes each (512 Kbit)
- Four blocks with 32 Kbytes each (1 Mbit)
- 128 pages per block

• Serial Peripheral Interface (SPI) Compatible
- Supports SPI Modes 0 (0,0) and 3 (1,1)

• High Performance Read
- 33MHz clock rate (max) for NORMAL READ
- 33MHz clock rate (max) for FAST READ

• Page Mode for Program Operations
- 256 bytes per page

• Block Write Protection
- The Block Protect (BP1, BP0) bits allow part or entire of the memory to be configured as read-only.

• Hardware Data Protection
- Write Protect (WP#) pin will inhibit write operations to the status register

• Page Program (up to 256 Bytes)
- Typical 3 ms per page program time

• Sector, Block and Chip Erase
- Typical 60 ms sector/block/chip erase time

• Single Cycle Reprogramming for Status Register
- Build-in erase before programming

• High Product Endurance
- Guarantee 10,000 program/erase cycles per single sector
- Minimum 10 years data retention

• Industrial Standard Pin-out and Package
- 8-pin JEDEC SOIC
- Optional lead-free (Pb-free) packages

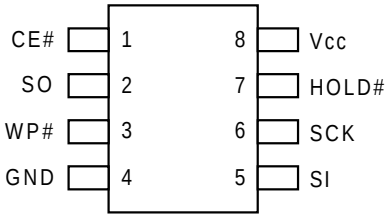
GENERAL DESCRIPTION

The PS25LV512/010 are 512 Kbit/1 Mbits 3.0 Volt-only serial Flash memories. These devices are designed to use a single low voltage, range from 3.0 Volt to 3.6 Volt, power supply to perform read, erase and program operations. The devices can be programmed in standard EPROM programmers as well.

The device is optimized for use in many commercial applications where low-power and low-voltage operation are essential. The PS25LV512/010 is enabled through the Chip Enable pin (CE#) and accessed via a 3-wire interface consisting of Serial Data Input (SI), Serial Data Output (SO), and Serial Clock (SCK). All write cycles are completely self-timed.

Block Write protection for top 1/4, top 1/2 or the entire memory array (1M) or entire memory array (512K) is enabled by programming the status register. Separate write enable and write disable instructions are provided for additional data protection. Hardware data protection is provided via the WP pin to protect against inadvertent write attempts to the status register. The HOLD pin may be used to suspend any serial communication without resetting the serial sequence.

CONNECTION DIAGRAMS

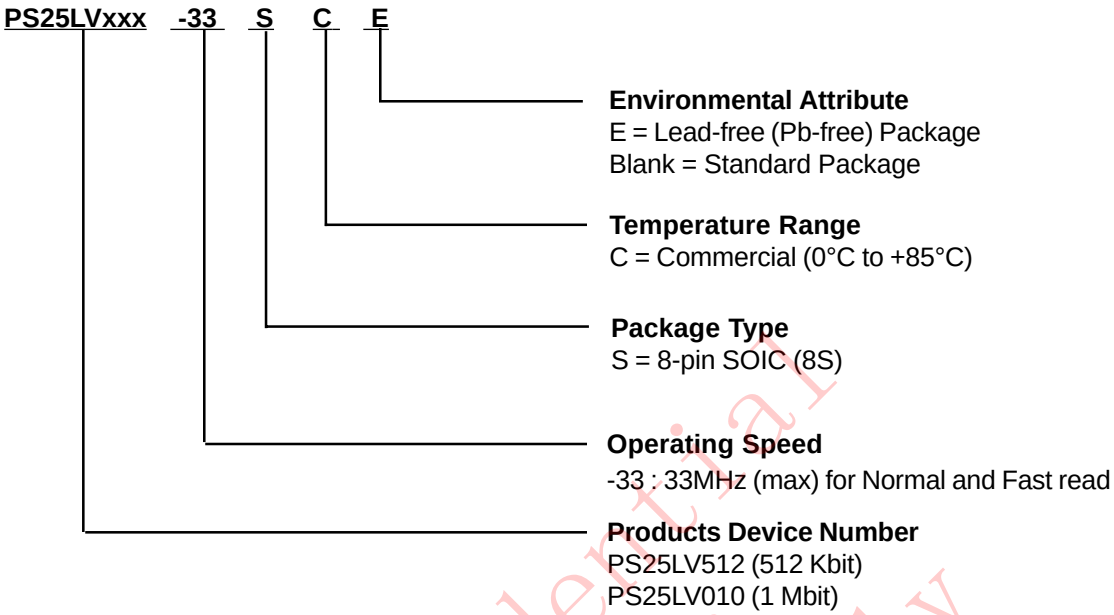


8-Pin SOIC

PIN DESCRIPTIONS

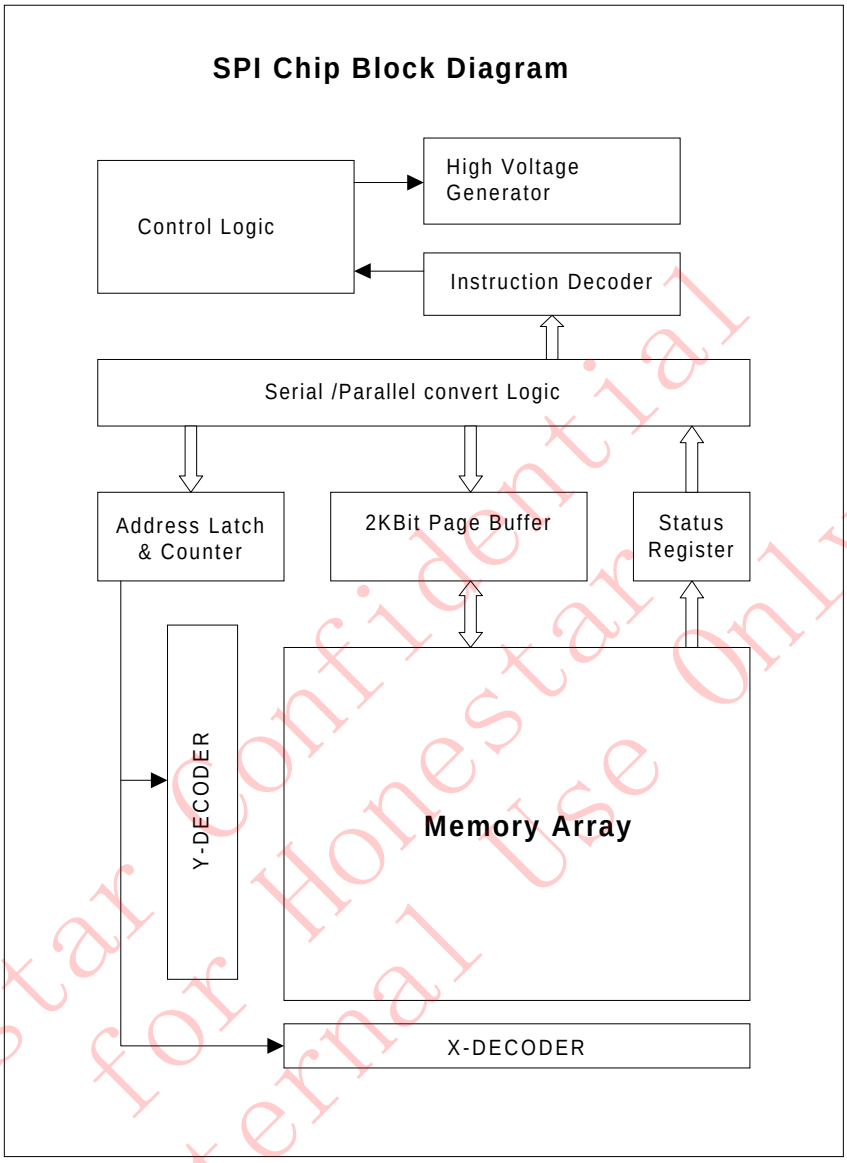
SYMBOL	TYPE	DESCRIPTION
CE#	INPUT	Chip Enable: CE# goes low activates the device's internal circuitries for device operation. CE# goes high deselects the device and switches into standby mode to reduce the power consumption. When the device is not selected, data will not be accepted via the serial input pin (SI), and the serial output pin (SO) will remain in a high impedance state.
SCK	INPUT	Serial Data Clock
SI	INPUT	Serial Data Input
SO	OUTPUT	Serial Data Output
GND		Ground
Vcc		Device Power Supply
WP#	INPUT	Write Protect: When the WP# pin brought to low and WPEN bit is "1", all write operations to the status register are inhibited.
HOLD#	INPUT	Hold: Pause serial communication with the master device without resetting the serial sequence.

PRODUCT ORDERING INFORMATION



Part Number	Operating Frequency (MHz)	Package	Temperature Range
PS25LV512-33SC	33	8S	Commercial (0^{o}C to + 85^{o}C)
PS25LV512-33SCE			
PS25LV010-33SC			
PS25LV010-33SCE			

BLOCK DIAGRAM



SERIAL INTERFACE DESCRIPTION

PS25LV512/010 can be driven by a microcontroller on the SPI bus as shown in Figure 1. The serial communication term definitions are in the following section.

MASTER: The device that generates the serial clock.

SLAVE: Because the Serial Clock pin (SCK) is always an input, the PS25LV512/010 always operates as a slave.

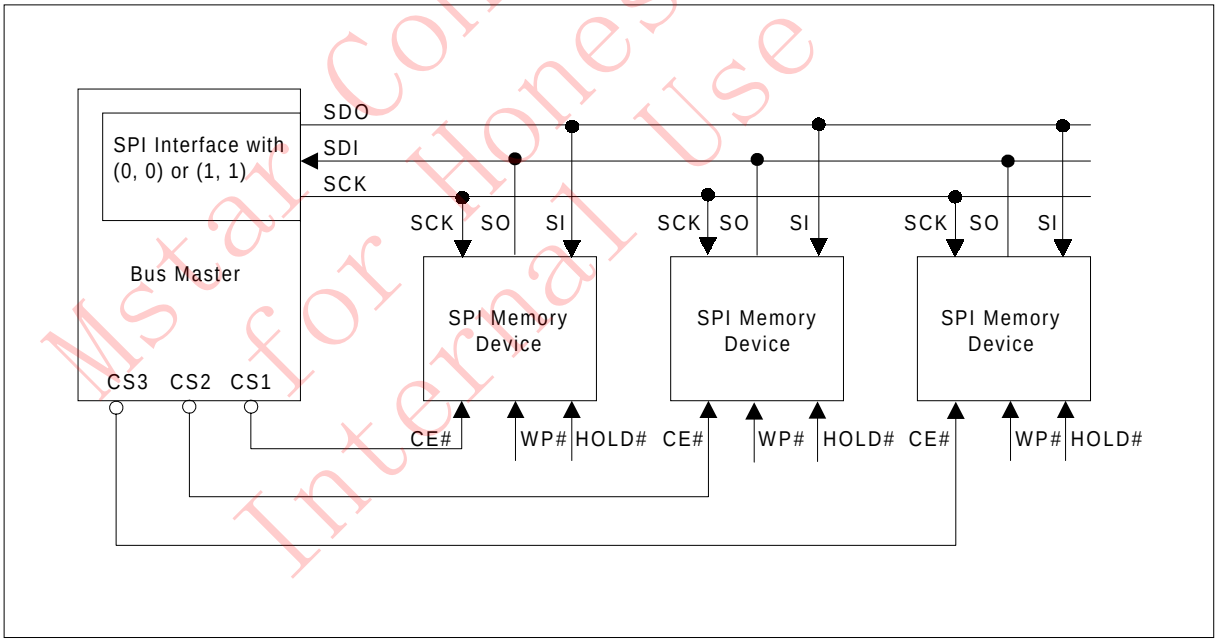
TRANSMITTER/RECEIVER: The PS25LV512/010 has separate pins designated for data transmission (SO) and reception (SI).

MSB: The Most Significant Bit (MSB) is the first bit transmitted and received.

SERIAL OP-CODE: After the device is selected with CE# going low, the first byte will be received. This byte contains the op-code that defines the operations to be performed.

INVALID OP-CODE: If an invalid op-code is received, no data will be shifted into the PS25LV512/010, and the serial output pin (SO) will remain in a high impedance state until the falling edge of CE# is detected again. This will reinitialize the serial communication.

Figure 1. Bus Master and SPI Memory Devices



Note: 1. The Write Protect (WP#) and Hold (HOLD#) signals should be driven, High or Low as appropriate.

SERIAL INTERFACE DESCRIPTION (CONTINUED)

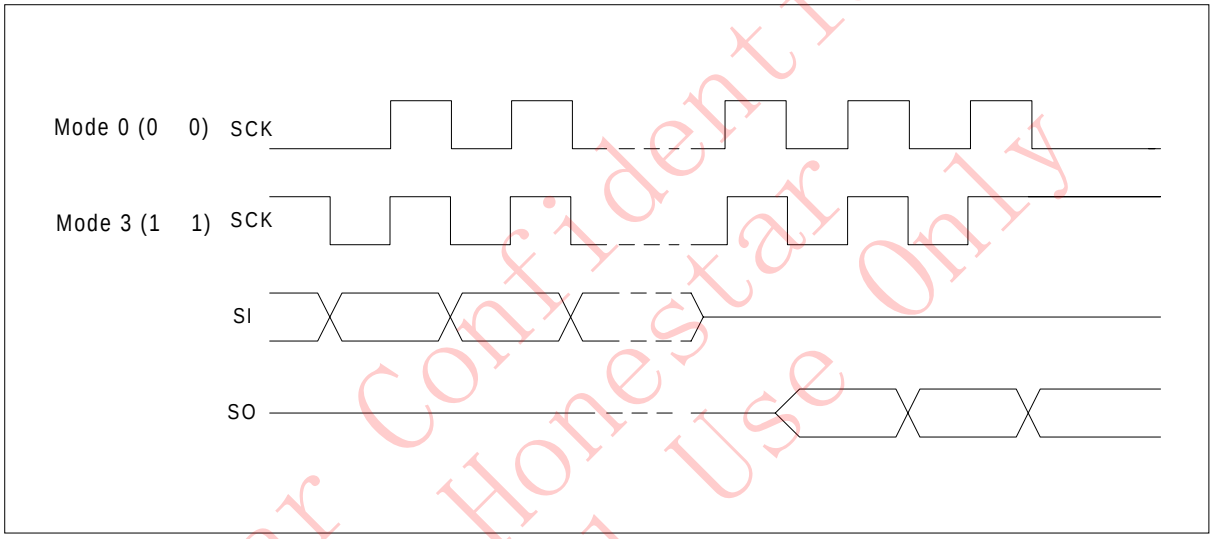
SPI MODES

These devices can be driven by microcontroller with its SPI peripheral running in either of the two following modes:
Mode 0 = (0, 0)
Mode 3 = (1, 1)

For these two modes, input data is latched in on the rising edge of Serial Clock (SCK), and output data is available from the falling edge of Serial Clock (SCK).

The difference between the two modes, as shown in Figure 2, is the clock polarity when the bus master is in Stand-by mode and not transfering data:
- Clock remains at 0 (SCK = 0) for Mode 0 (0, 0)
- Clock remains at 1 (SCK = 1) for Mode 3 (1, 1)

Figure 2. SPI Modes



DEVICE OPERATION

The PS25LV512/010 is designed to interface directly with the synchronous serial peripheral interface (SPI) of the 6800 type series of microcontrollers.

The PS25LV512/010 utilizes an 8-bit instruction register. The list of instructions and their operation codes are contained in Table 1. All instructions, addresses, and data are transferred with the MSB first and start with a high-to-low transition.

Write is defined as program and/or erase in this specification. The following commands, PAGE PROGRAM, SECTOR ERASE, BLOCK ERASE, CHIP ERASE, and WRSR are write instructions for PS25LV512/010.

Table 1. Instruction Set for the PS25LV512/010

Instruction Name	Instruction Format	Hex Code	Operation
WREN	0000 0110	06h	Set Write Enable Latch
WRDI	0000 0100	04h	Reset Write Enable Latch
RDSR	0000 0101	05h	Read Status register
WRSR	0000 0001	01h	Write Status Register
READ	0000 0011	03h	Read Data from Memory Arrary
FAST_READ	0000 1011	0Bh	Read Data from Memory at Higher Speed
PG_ PROG	0000 0010	02h	Program Data Into Memory Array
SECTOR_ERASE	1101 0111	D7h	Erase One Sector in Memory Array
BLOCK_ERASE	1101 1000	D8h	Erase One Block in Memory Array
CHIP_ERASE	1100 0111	C7h	Erase Entire Memory Array
RDID	1010 1011	ABh	Read Manufacturer and Product ID

READ PRODUCT ID (RDID): The RDID instruction allows the user to read the manufacturer and product ID of the device. The instruction code is followed by three dummy bytes, each bit being latched-in on Serial Data Input (SI) during the rising edge of Serial Clock (SCK). Then the first manufacturer ID (9Dh) is shifted out on Serial Data Output (SO), followed by the device ID (7Bh = PS25LV512; 7Ch = PS25LV010) and the second manufacturer ID (7Fh), each bit been shifted out during the falling edge of Serial Clock (SCK).

Table 2. Product Identification

Product Identification	Data
Manufacturer ID	9Dh
Device ID:	
PS25LV512	7Bh
PS25LV010	7Ch

WRITE ENABLE (WREN): The device will power up in the write disable state when Vcc is applied. All write instructions must therefore be preceded by the WREN instruction.

WRITE DISABLE (WRDI): To protect the device against inadvertent writes, the WRDI instruction disables all write commands. The WRDI instruction is independent of the status of the WP# pin.

READ STATUS REGISTER (RDSR): The RDSR instruction provides access to the status register. The READY/BUSY and write enable status of the device can be determined by the RDSR instruction. Similarly, the Block Write Protection bits indicate the extent of protection employed. These bits are set by using the WRSR instruction. During internal write cycles, all other commands will be ignored except the RDSR instruction.

Table 3. Status Register Format

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WPEN	X	X	X	BP1	BP0	WEN	RDY

Table 4. Read Status Register Bit Definition

Bit	Definition
Bit 0 (RDY)	Bit 0 = 0 indicates the device is READY. Bit 0 = 1 indicates the write cycle is in progress and the device is BUSY.
Bit 1 (WEN)	Bit 1 = 0 indicates the device is not WRITE ENABLED. Bit 1 = 1 indicates the device is WRITE ENABLED.
Bit 2 (BP0)	See Table 5.
Bit 3 (BP1)	See Table 5.
Bits 4-6 are 0s when device is not in an internal write cycle.	
Bit 7 (WPEN)	WPEN = 0 blocks the function of Write Protect pin (WP#). WPEN = 1 activates the Write Protect pin (WP#). See Table 6 for details.
Bits 0-7 are 1s during an internal write cycle.	

WRITE STATUS REGISTER (WRSR): The WRSR instruction allows the user to select one of four levels of protection for the PS25LV010. The PS25LV010 is divided into four blocks where the top quarter (1/4), top half (1/2), or all of the memory blocks can be protected (locked out) from write. The PS25LV512 is divided into 2 blocks where all of the memory blocks can be protected (locked out) from write. Any of the locked-out blocks will therefore be READ only. The locked-out block and the corresponding status register control bits are shown in Table 5.

The three bits, BP0, BP1, and WPEN, are nonvolatile cells that have the same properties and functions as the regular memory cells (e.g., WREN, RDSR).

Table 5. Block Write Protect Bits

Level	Status Register Bits		PS25LV512		PS25LV010	
	BP1	BP0	Array Addresses Locked Out	Locked-out Block(s)	Array Addresses Locked Out	Locked-out Block(s)
0	0	0	None	None	None	None
1(1/4)	0	1			018000 - 01FFFF	Block 4
2(1/2)	1	0			010000 - 01FFFF	Block 3, 4
3(All)	1	1	000000-00FFFF	All Blocks (1 - 2)	000000 - 01FFFF	All Blocks (1 - 4)

The WRSR instruction also allows the user to enable or disable the Write Protect (WP#) pin through the use of the Write Protect Enable (WPEN) bit. Hardware write protection is enabled when the WP# pin is low and the WPEN bit is "1". Hardware write protection is disabled when either the WP# pin is high or the WPEN bit is "0." When the device is hardware write protected, writes to the Status Register, including the Block Protect bits and the WPEN bit, and the locked-out blocks in the memory array are disabled. Write is only allowed to blocks of the memory which are not locked out. The WRSR instruction is self-timed to automatically erase and program BP0, BP1, and WPEN bits. In order to write the status register, the device must first be write enabled via the WREN instruction. Then, the instruction and data for the three bits are entered. During the internal write cycle, all instructions will be ignored except RDSR instructions. The PS25LV512/010 will automatically return to write disable state at the completion of the WRSR cycle.

Note: When the WPEN bit is hardware write protected, it cannot be changed back to "0", as long as the WP# pin is held low.

Table 6. WPEN Operation

WPEN	WP	WEN	ProtectedBlocks	UnprotectedBlocks	Status Register
0	X	0	Protected	Protected	Protected
0	X	1	Protected	Writable	Writable
1	Low	0	Protected	Protected	Protected
1	Low	1	Protected	Writable	Protected
X	High	0	Protected	Protected	Protected
X	High	1	Protected	Writable	Writable

READ: Reading the PS25LV512/010 via the SO (Serial Output) pin requires the following sequence. After the CE# line is pulled low to select a device, the READ instruction is transmitted via the SI line followed by the byte address to be read (Refer to Table 7). Upon completion, any data on the SI line will be ignored. The data (D7-D0) at the specified address is then shifted out onto the SO line. If only one byte is to be read, the CE# line should be driven high after the data comes out. The READ instruction can be continued since the byte address is automatically incremented and data will continue to be shifted out. For the PS25LV512/010, when the highest address is reached, the address counter will roll over to the lowest address allowing the entire memory to be read in one continuous READ instruction.

FAST_READ: The device is first selected by driving CE# low. The FAST READ instruction is followed by a 3-byte address (A23-A0) and a dummy byte, each bit being latched-in during the rising edge of SCK (Serial Clock). Then the memory contents, at that address, is shifted out on SO (Serial Output), each bit being shifted out, at a maximum frequency f_{FR}, during the falling edge of SCK (Serial Clock).

The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out. When the highest address is reached, the address counter will roll over to the lowest address allowing the entire memory to be read with a single FAST READ instruction. The FAST READ instruction is terminated by driving CE# high.

PAGE PROGRAM (PG_PROG): In order to program the PS25LV512/010, two separate instructions must be executed. First, the device must be write enabled via the WREN instruction. Then the PAGE PROGRAM instruction can be executed. Also, the address of the memory location(s) to be programmed must be outside the protected address field location selected by the Block Write Protection Level. During an internal self-timed programming cycle, all commands will be ignored except the RDSR instruction.

The PAGE PROGRAM instruction requires the following sequence. After the CE# line is pulled low to select the device, the PAGE PROGRAM instruction is transmitted via the SI line followed by the address and the data (D7-D0) to be programmed (Refer to Table 7). Programming will start after the CE# pin is brought high. The low-to-high transition of the CE# pin must occur during the SCK low time immediately after clocking in the D0 (LSB) data bit.

The READY/BUSY status of the device can be determined by initiating a RDSR instruction. If Bit 0 = 1, the program cycle is still in progress. If Bit 0=0, the program cycle has ended. Only the RDSR instruction is enabled during the program cycle. A single PROGRAM instruction programs 1 to 256 consecutive bytes within a page if it is not write protected. The starting byte could be anywhere within the page. When the end of the page is reached, the address will wrap around to the beginning of the same page. If the data to be programmed are less than a full page, the data of all other bytes on the same page will remain unchanged. If more than 256 bytes of data are provided, the address counter will roll over on the same page and the previous data provided will be replaced. The same byte cannot be reprogrammed without erasing the whole sector/block first. The PS25LV512/010 will automatically return to the write disable state at the completion of the PROGRAM cycle.

Note: If the device is not write enabled (WREN) the device will ignore the Write instruction and will return to the standby state, when CE# is brought high. A new CE# falling edge is required to re-initiate the serial communication.

Table 7. Address Key

Address	PS25LV512	PS25LV010
A_N	A_{15} - A_0	A_{16} - A_0
Don't Care Bits	A_{23} - A_{16}	A_{23} - A_{17}

SECTOR_ERASE, BLOCK_ERASE: Before a byte can be reprogrammed, the sector/block which contains the byte must be erased. In order to erase the PS25LV512/010, two separate instructions must be executed. First, the device must be write enabled via the WREN instruction. Then the SECTOR ERASE or BLOCK ERASE instruction can be executed.

Table 8. Block Addresses

Block Address	PS25LV512 Block	PS25LV010 Block
000000 to 007FFF	Block 1	Block 1
008000 to 00FFFF	Block 2	Block 2
010000 to 017FFF	N/A	Block 3
018000 to 01FFFF	N/A	Block 4

The BLOCK ERASE instruction erases every byte in the selected block if the block is not locked out. Block address is automatically determined if any address within the block is selected. The BLOCK ERASE instruction is internally controlled; it will automatically be timed to completion. During this time, all commands will be ignored, except RDSR instruction. The PS25LV512/010 will automatically return to the write disable state at the completion of the BLOCK ERASE cycle.

CHIP_ERASE: As an alternative to the SECTOR and BLOCK ERASE, the CHIP ERASE instruction will erase every byte in all blocks that are not locked out. First, the device must be write enabled via the WREN instruction. Then the CHIP ERASE instruction can be executed. The CHIP ERASE instruction is internally controlled; it will automatically be timed to completion. The CHIP ERASE cycle time maximum is 100 miliseconds. During the internal erase cycle, all instructions will be ignored except RDSR. The PS25LV512/010 will automatically return to the write disable state at the completion of the CHIP ERASE.

HOLD: The HOLD# pin is used in conjunction with the CE# pin to select the PS25LV512/010. When the device is selected and a serial sequence is underway, HOLD# pin can be used to pause the serial communication with the master device without resetting the serial sequence. To pause, the HOLD# pin must be brought low while the SCK pin is low. To resume serial communication, the HOLD# pin is brought high while the SCK pin is low (SCK may still toggle during HOLD). Inputs to the SI pin will be ignored while the SO pin is in the high impedance state.

HARDWARE WRITE PROTECT: The PS25LV512/010 has a write lockout feature that can be activated by asserting the write protect pin (WP#). When the lockout feature is activated, locked-out sectors will be READ only. The write protect pin will allow normal read/write operations when held high. When the WP# is brought low and WPEN bit is "1", all write operations to the status register are inhibited. WP# going low while CE# is still low will interrupt a write to the status register. If the internal status register write cycle has already been initiated, WP# going low will have no effect on any write operation to the status register. The WP# pin function is blocked when the WPEN bit in the status register is "0". This will allow the user to install the PS25LV512/010 in a system with the WP# pin tied to ground and still be able to write to the status register. All WP# pin functions are enabled when the WPEN bit is set to "1".

ABSOLUTE MAXIMUM RATINGS (1)

Temperature Under Bias		-65°C to +125°C
Storage Temperature		-65°C to +125°C
Surface Mount Lead Soldering Temperature	Standard Package	240°C 3 Seconds
	Lead-free Package	260°C 3 Seconds
Input Voltage with Respect to Ground on All Pins (2)		-0.5 V to V_{CC} + 0.5 V
All Output Voltage with Respect to Ground		-0.5 V to V_{CC} + 0.5 V
V_{CC} (2)		-0.5 V to +6.0 V

Notes:
1. Stresses under those listed in “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only. The functional operation of the device or any other conditions under those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating condition for extended periods may affected device reliability.
2. Maximum DC voltage on input or I/O pins are V_{CC} + 0.5 V. During voltage transitioning period, input or I/O pins may overshoot to V_{CC} + 2.0 V for a period of time up to 20 ns. Minimum DC voltage on input or I/O pins are -0.5 V. During voltage transitioning period, input or I/O pins may undershoot GND to -2.0 V for a period of time up to 20 ns.

DC AND AC OPERATING RANGE

Part Number	**PS25LV512/010**
Operating Temperature	0°C to 85°C
Vcc Power Supply	3.0 V - 3.6 V

DC CHARACTERISTICS

Applicable over recommended operating range from:
T_{AC} = 0°C to +85°C, V_{CC} = +3.0 V to +3.6 V (unless otherwise noted).

Symbol	Parameter	Condition		Min	Typ	Max	Units
I_{CC1}	Vcc Active Read Current	V_{CC} = 3.6V at 33 MHz, SO = Open			10	15	mA
I_{CC2}	Vcc Program/Erase Current	V_{CC} = 3.6V at 33 MHz, SO = Open			15	30	mA
I_{SB1}	Vcc Standby Current CMOS	V_{CC} = 3.6V, CE# = V_{CC}				50	µA
I_{SB2}	Vcc Standby Current TTL	V_{CC} = 3.6V, CE# = V_{IH} to V_{CC}			0.05	3	mA
I_{LI}	Input Leakage Current	V_{IN} = 0V to V_{CC}				1	µA
I_{LO}	Output Leakage Current	V_{IN} = 0V to V_{CC}, T_{AC} = 0°C to 85°C				1	µA
V_{IL}	Input Low Voltage			-0.5		0.8	V
V_{IH}	Input HIgh Voltage			0.7V_{CC}		V_{CC} + 0.3	V
V_{OL}	Output Low Voltage	2.7V < V_{CC} < 3.6V	I_{OL} = 2.1 mA			0.45	V
V_{OH}	Output High Voltage		I_{OH} = -100 µA	V_{CC} - 0.2			V

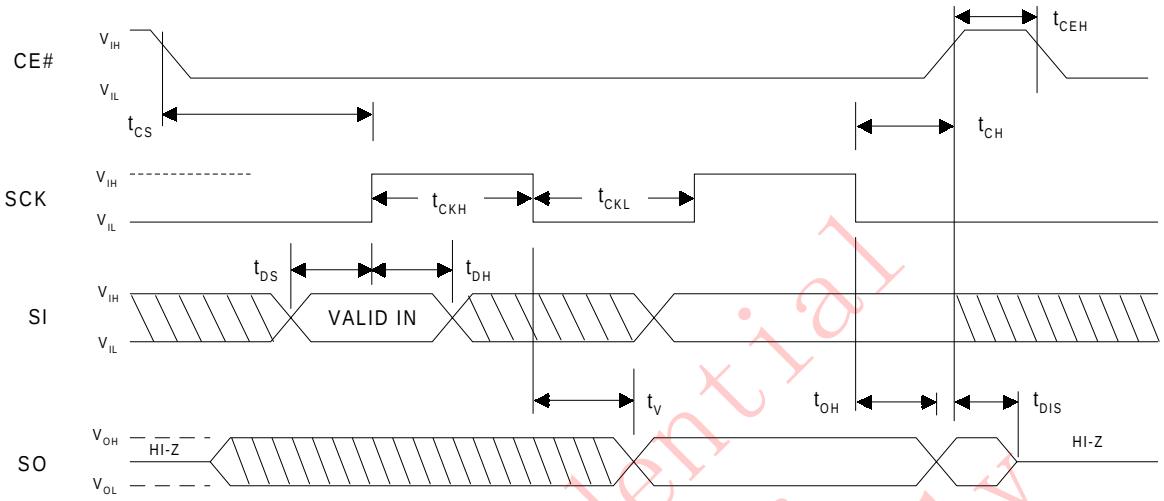
AC CHARACTERISTICS

Applicable over recommended operating range from T_A = 0°C to +85°C, V_{CC} = +3.0 V to +3.6 V
C_L = 1TTL Gate and 30 pF (unless otherwise noted).

Symbol	Parameter	Min	Typ	Max	Units
f_{FR}	Clock Frequency for FAST_READ	0		33	MHz
f_R	Clock Frequency for READ instructions	0		33	MHz
t_{RI}	Input Rise Time			20	ns
t_{FI}	Input Fall Time			20	ns
t_{CKH}	SCK High Time	15			ns
t_{CKL}	SCK Low Time	15			ns
t_{CEH}	CE High Time	25			ns
t_{CS}	CE Setup Time	25			ns
t_{CH}	CE Hold Time	25			ns
t_{DS}	Data In Setup Time	5			ns
t_{DH}	Data in Hold Time	5			ns
t_{HS}	Hold Setup Time	15			ns
t_{HD}	Hold Time	15			ns
t_V	Output Valid			15	ns
t_{OH}	Output Hold Time	0			ns
t_{LZ}	Hold to Output Low Z			200	ns
t_{HZ}	Hold to Output High Z			200	ns
t_{DIS}	Output Disable Time			100	ns
t_{EC}	Secter/Block/Chip Erase Time		60	100	ms
t_{pp}	Page Program Time		2	5	ms
t_w	Write Status Register time		40	100	ms

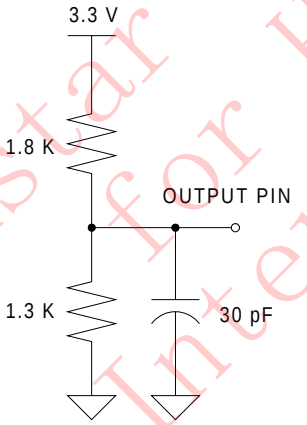
AC CHARACTERISTICS (CONTINUED)

AC WAVEFORMS(1)

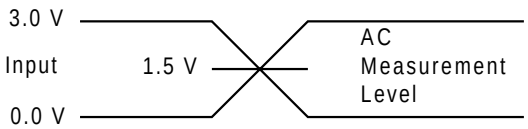


Note: 1. For SPI Mode 0 (0,0)

OUTPUT TEST LOAD

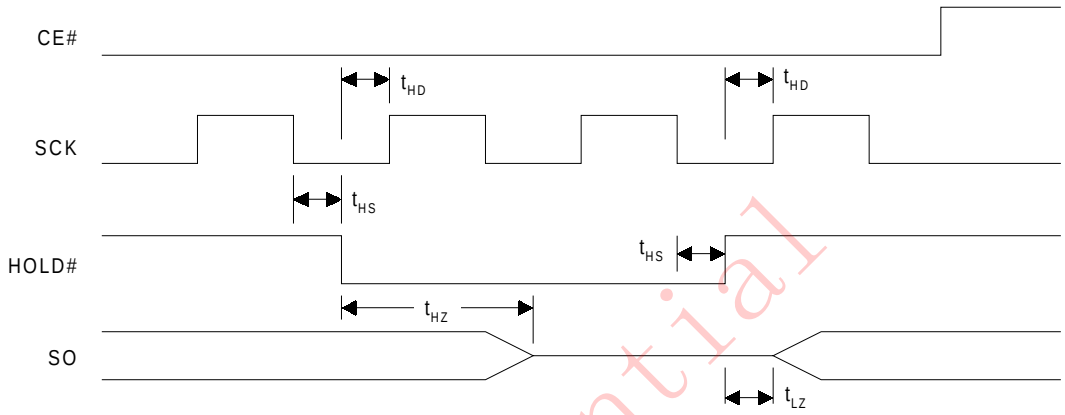


INPUT TEST WAVEFORMS AND MEASUREMENT LEVEL



AC CHARACTERISTICS (CONTINUED)

HOLD Timing



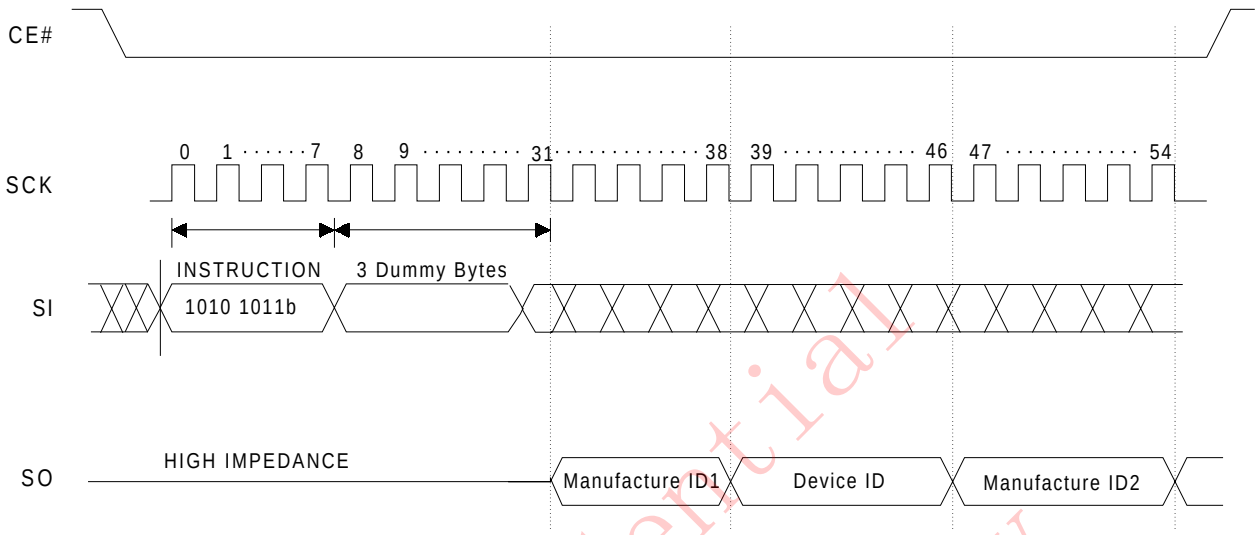
PIN CAPACITANCE (f = 1 MHz, T = 25°C)

	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0 V
C_{OUT}	8	12	pF	V_{OUT} = 0 V

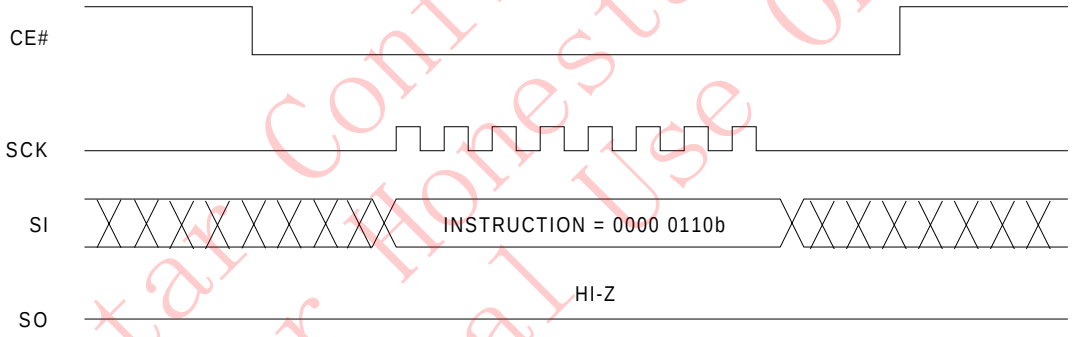
Note: These parameters are characterized but not 100% tested.

TIMING DIAGRAMS

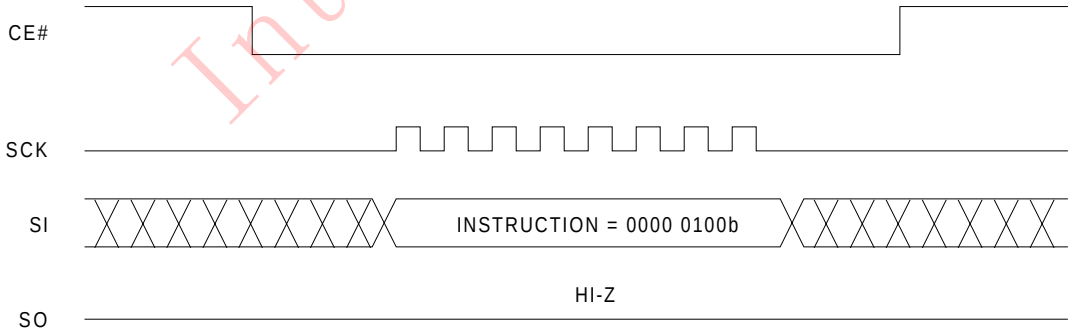
RDID Timing



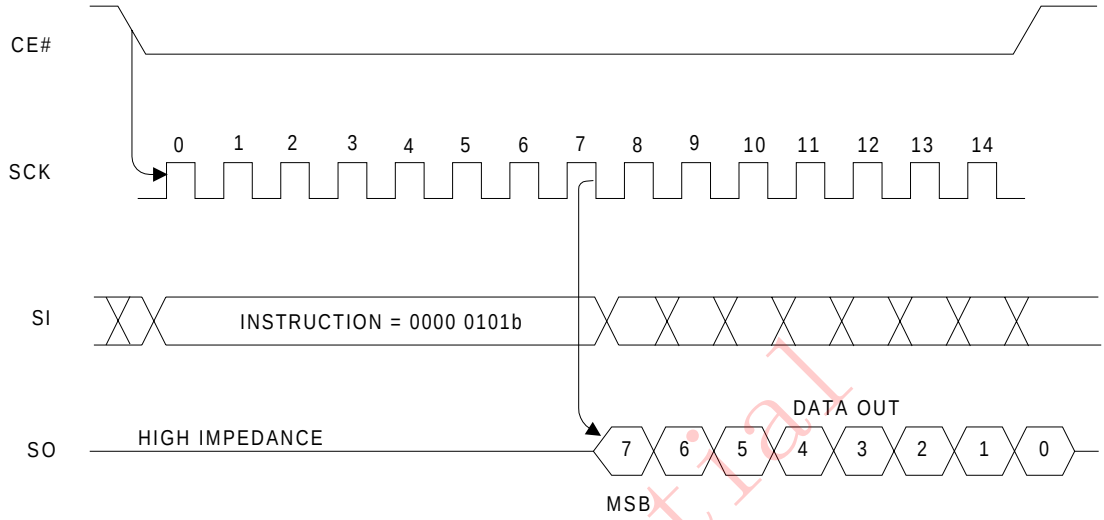
WREN Timing



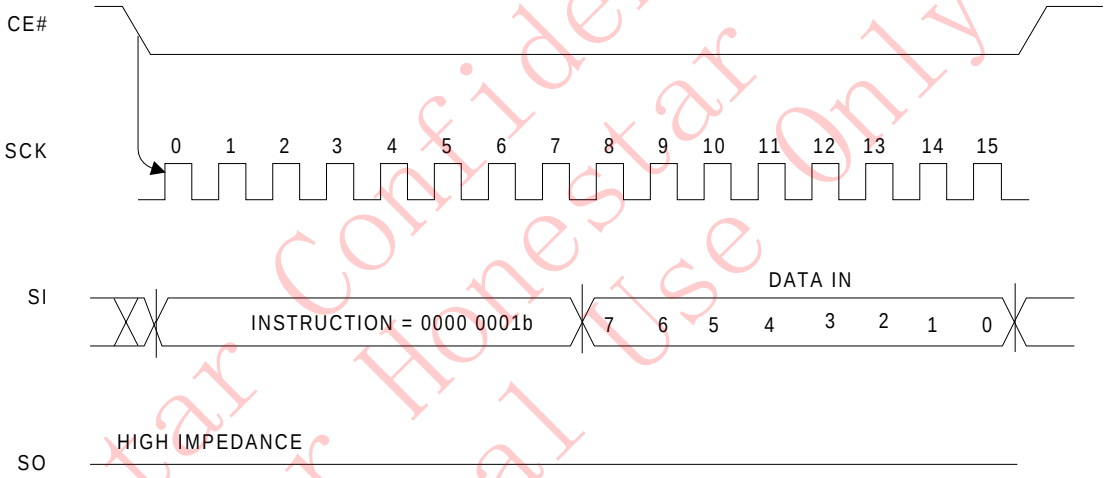
WRDI Timing



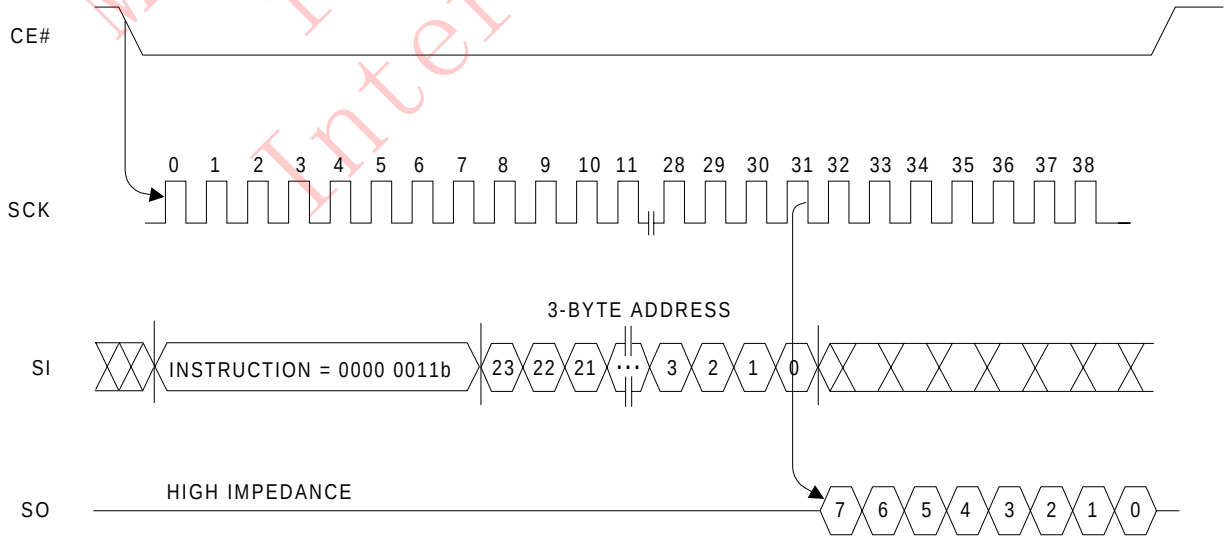
RDSR Timing



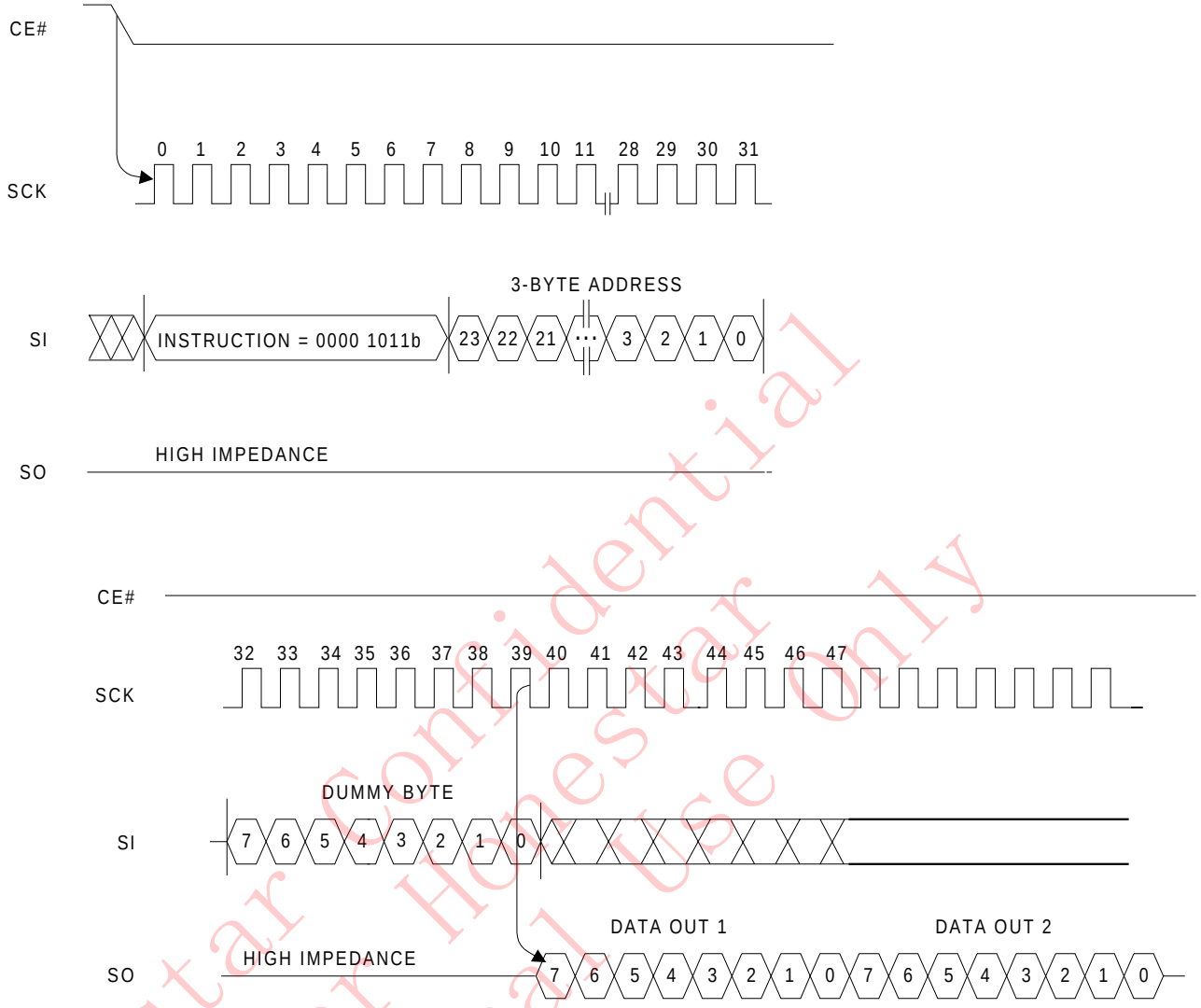
WRSR Timing



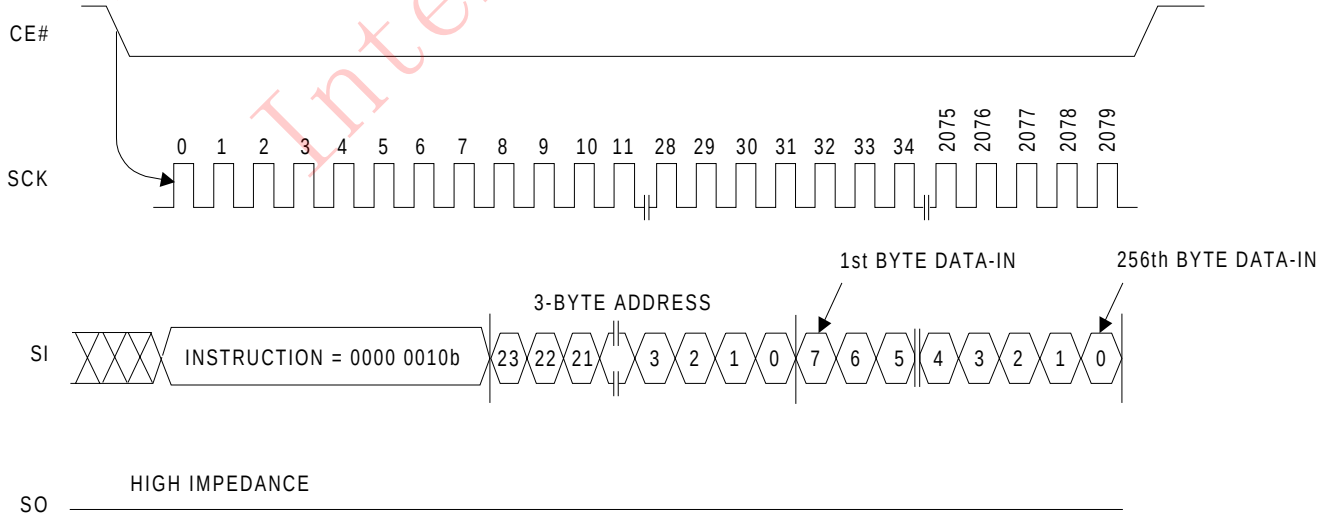
READ Timing



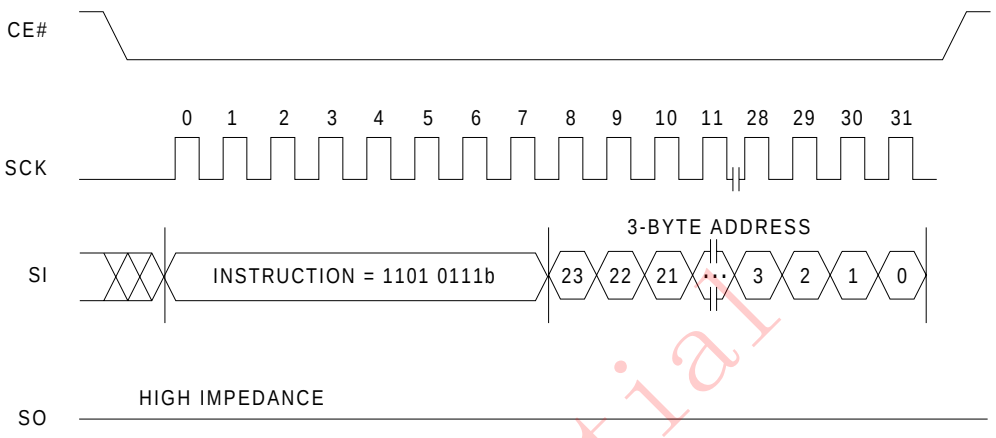
FAST READ Timing



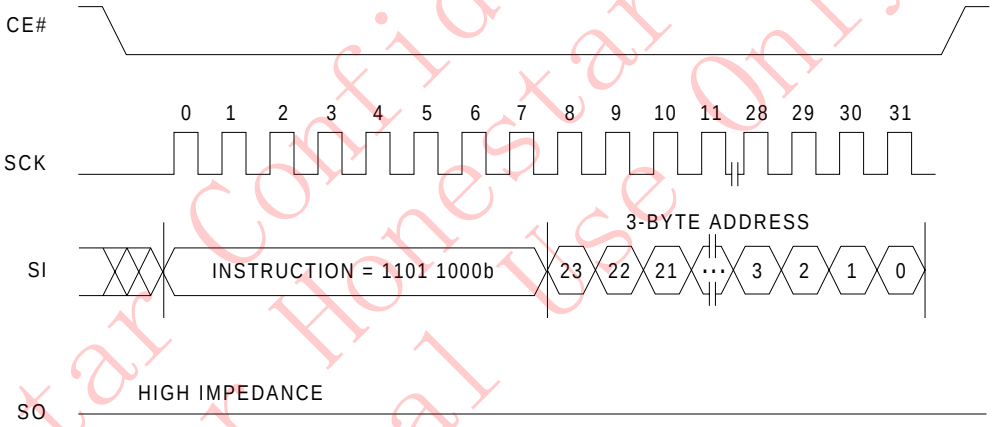
PAGE PROGRAM Timing



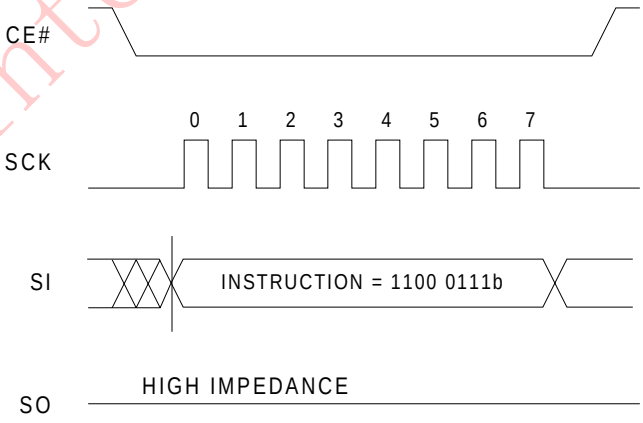
SECTOR ERASE Timing



BLOCK ERASE Timing



CHIP ERASE Timing



PROGRAM/ERASE PERFORMANCE

Parameter	Unit	Typ	Max	Remarks
Sector Erase Time	ms	60	100	From writing erase command to erase completion
Block Erase Time	ms	60	100	From writing erase command to erase completion
Chip Erase Time	ms	60	100	From writing erase command to erase completion
Page Programming Time	ms	3	5	From writing program command to program completion

Note: These parameters are characterized and are not 100% tested.

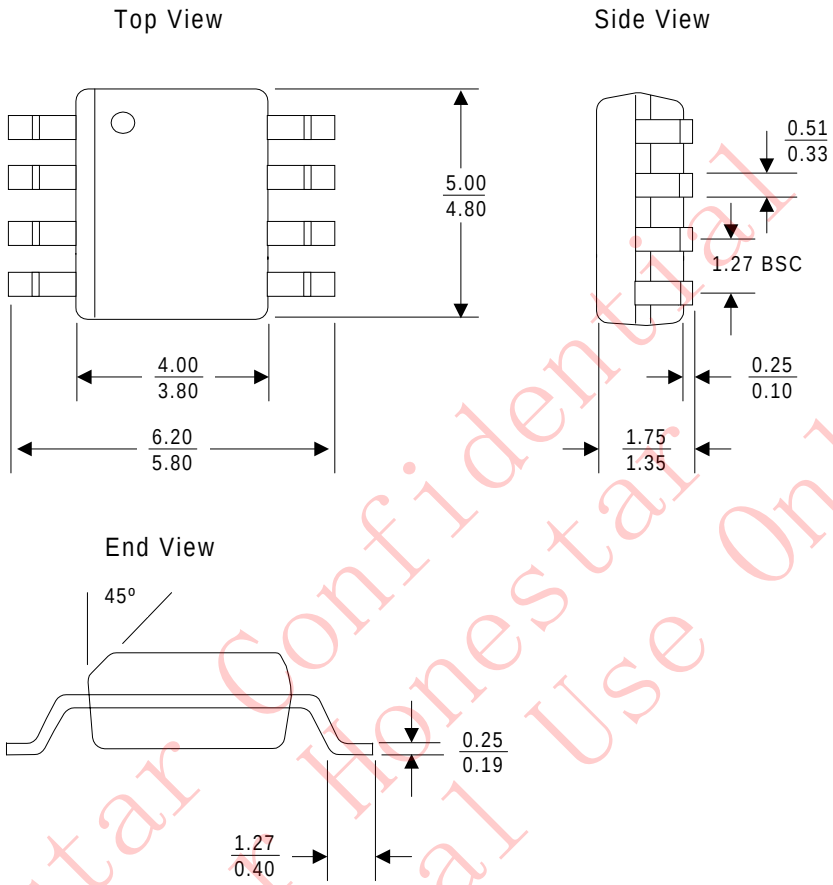
RELIABILITY CHARACTERISTICS (1)

Parameter	Min	Typ	Unit	Test Method
Endurance	10,000 (2)		Cycles	JEDEC Standard A117
Data Retention	10		Years	JEDEC Standard A103
ESD - Human Body Model	2,000		Volts	JEDEC Standard A114
ESD - Machine Model	200		Volts	JEDEC Standard A115
Latch-Up	100 + I_{CC1}		mA	JEDEC Standard 78

Note: 1. These parameters are characterized and are not 100% tested.
2. Preliminary specification only and will be formalized after cycling qualification test.

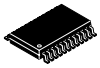
PACKAGE TYPE INFORMATION

8S
8-Pin JEDEC Small Outline Integrated Circuit (SOIC) Package (measure in millimeters)



REVISION HISTORY

Date	Revision No.	Description of Changes	Page No.
September, 2005	1.0	Normal Production Spec	All



SLOS392 – FEBRUARY 2002

2-W STEREO AUDIO POWER AMPLIFIER WITH ADVANCED DC VOLUME CONTROL

FEATURES

- **Advanced DC Volume Control With 2-dB Steps From –40 dB to 20 dB**
  - **Fade Mode**
  - **Maximum Volume Setting for SE Mode**
  - **Adjustable SE Volume Control Referenced to BTL Volume Control**
- **2 W Into 3-Ω Speakers**
- **Stereo Input MUX**
- **Differential Inputs**

APPLICATIONS

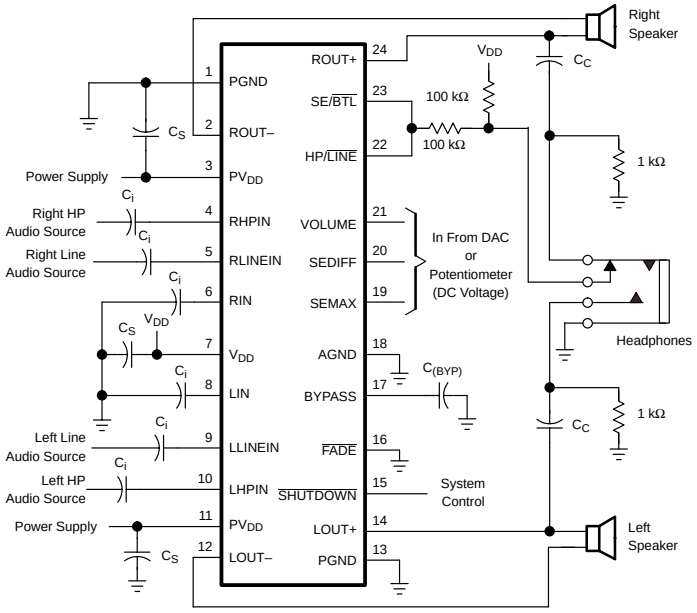
- **Notebook PC**
- **LCD Monitors**
- **Pocket PC**

DESCRIPTION

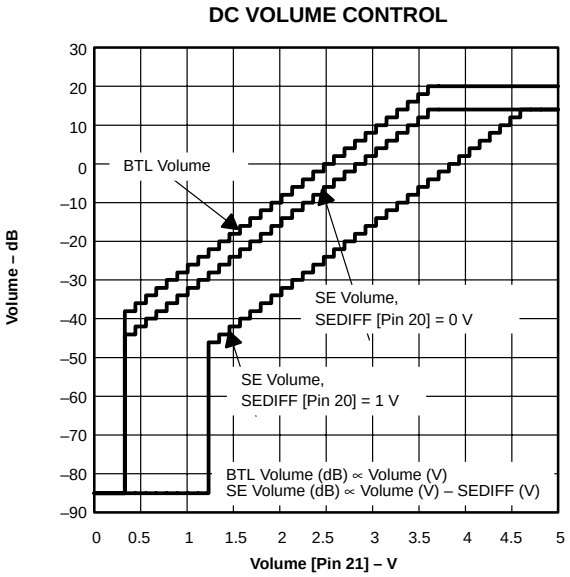
The TPA6011A4 is a stereo audio power amplifier that drives 2 W/channel of continuous RMS power into a 3-Ω load. Advanced dc volume control minimizes external components and allows BTL (speaker) volume control and SE (headphone) volume control. Notebook and pocket PCs benefit from the integrated feature set that minimizes external components without sacrificing functionality.

To simplify design, the speaker volume level is adjusted by applying a dc voltage to the VOLUME terminal. Likewise, the delta between speaker volume and headphone volume can be adjusted by applying a dc voltage to the SEDIFF terminal. To avoid an unexpected high volume level through the headphones, a third terminal, SEMAX, limits the headphone volume level when a dc voltage is applied. Finally, to ensure a smooth transition between active and shutdown modes, a fade mode ramps the volume up and down.

APPLICATION CIRCUIT



DC VOLUME CONTROL



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

AVAILABLE OPTIONS

T_A	PACKAGE
	24-PIN TSSOP (PWP)
–40°C to 85°C	TPA6011A4PWP

NOTE: The PWP package is available taped and reeled. To order a taped and reeled part, add the suffix R to the part number (e.g., TPA6011A4PWPR).

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage, V_{DD}, PV_{DD} . . . . . –0.3 V to 6 V
Input voltage, V_I . . . . . –0.3 V to V_{DD}+0.3 V
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range, T_A . . . . . –40°C to 85°C
Operating junction temperature range, T_J . . . . . –40°C to 150°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
PWP	2.7 mW	21.8 mW/°C	1.7 W	1.4 W

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V_{DD}, PV_{DD}		4.0	5.5	V
High-level input voltage, V_{IH}	SE/$\overline{\text{BTL}}$, HP/$\overline{\text{LINE}}$, $\overline{\text{FADE}}$	0.8×V_{DD}		V
	$\overline{\text{SHUTDOWN}}$	2		V
Low-level input voltage, V_{IL}	SE/$\overline{\text{BTL}}$, HP/$\overline{\text{LINE}}$, $\overline{\text{FADE}}$		0.6×V_{DD}	V
	$\overline{\text{SHUTDOWN}}$		0.8	V
Operating free-air temperature, T_A		–40	85	°C

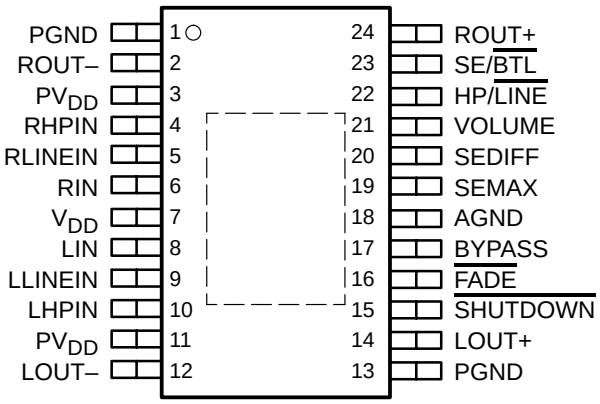
electrical characteristics, T_A = 25°C, V_{DD} = PV_{DD} = 5.5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\lvert V_{OO} \rvert$	Output offset voltage (measured differentially)	V_{DD} = 5.5 V, Gain = 0 dB, SE/$\overline{BTL}$ = 0 V			30	mV
		V_{DD} = 5.5 V, Gain = 20 dB, SE/$\overline{BTL}$ = 0 V			50	mV
PSRR	Power supply rejection ratio	V_{DD} = PV_{DD} = 4.0 V to 5.5 V	–42	–70		dB
$\lvert I_{IH} \rvert$	High-level input current (SE/$\overline{BTL}$, $\overline{FADE}$, HP/$\overline{LINE}$, $\overline{SHUTDOWN}$, SEDIFF, SEMAX, VOLUME)	V_{DD}=PV_{DD} = 5.5 V, V_I = V_{DD} = PV_{DD}			1	µA
$\lvert I_{IL} \rvert$	Low-level input current (SE/$\overline{BTL}$, $\overline{FADE}$, HP/$\overline{LINE}$, $\overline{SHUTDOWN}$, SEDIFF, SEMAX, VOLUME)	V_{DD} = PV_{DD} = 5.5 V, V_I = 0 V			1	µA
I_{DD}	Supply current, no load	V_{DD}=PV_{DD} = 5.5 V, SE/$\overline{BTL}$ = 0 V, $\overline{SHUTDOWN}$ = 2 V	6.0	7.5	9.0	mA
		V_{DD}=PV_{DD} = 5.5 V, SE/$\overline{BTL}$ = 5.5 V, $\overline{SHUTDOWN}$ = 2 V	3.0	5	6	
I_{DD}	Supply current, max power into a 3-Ω load	V_{DD}= 5 V = PV_{DD}, SE/$\overline{BTL}$ = 0 V, $\overline{SHUTDOWN}$ = 2 V, R_L = 3Ω, P_O = 2 W, stereo		1.5		A_{RMS}
$I_{DD(SD)}$	Supply current, shutdown mode	$\overline{SHUTDOWN}$ = 0.0 V		1	20	µA

operating characteristics, T_A = 25°C, V_{DD} = PV_{DD} = 5 V, R_L = 3 Ω, Gain = 6 dB (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
P_O	Output power	THD = 1%, f=1 kHz			2		W
THD+N	Total harmonic distortion + noise	P_O=1 W, R_L=8 Ω, f=20 Hz to 20 kHz			<0.4%		
V_{OH}	High-level output voltage	R_L = 8 Ω, Measured between output and V_{DD}				700	mV
V_{OL}	Low-level output voltage	R_L = 8 Ω, Measured between output and GND				400	mV
V_{Bypass}	Bypass voltage (Nominally V_{DD}/2)	Measured at pin 17, No load, V_{DD} = 5.5 V		2.65	2.75	2.85	V
B_{OM}	Maximum output power bandwidth	THD=5%			>20		kHz
	Supply ripple rejection ratio	f = 1 kHz, Gain = 0 dB, $C_{(BYP)}$ = 0.47 µF	BTL		–63		dB
			SE		–57		dB
	Noise output voltage	f = 20 Hz to20 kHz, Gain = 0 dB, $C_{(BYP)}$ = 0.47 µF	BTL		36		μV_{RMS}
Z_I	Input impedance (see figure 25)	VOLUME = 5.0 V			14		kΩ

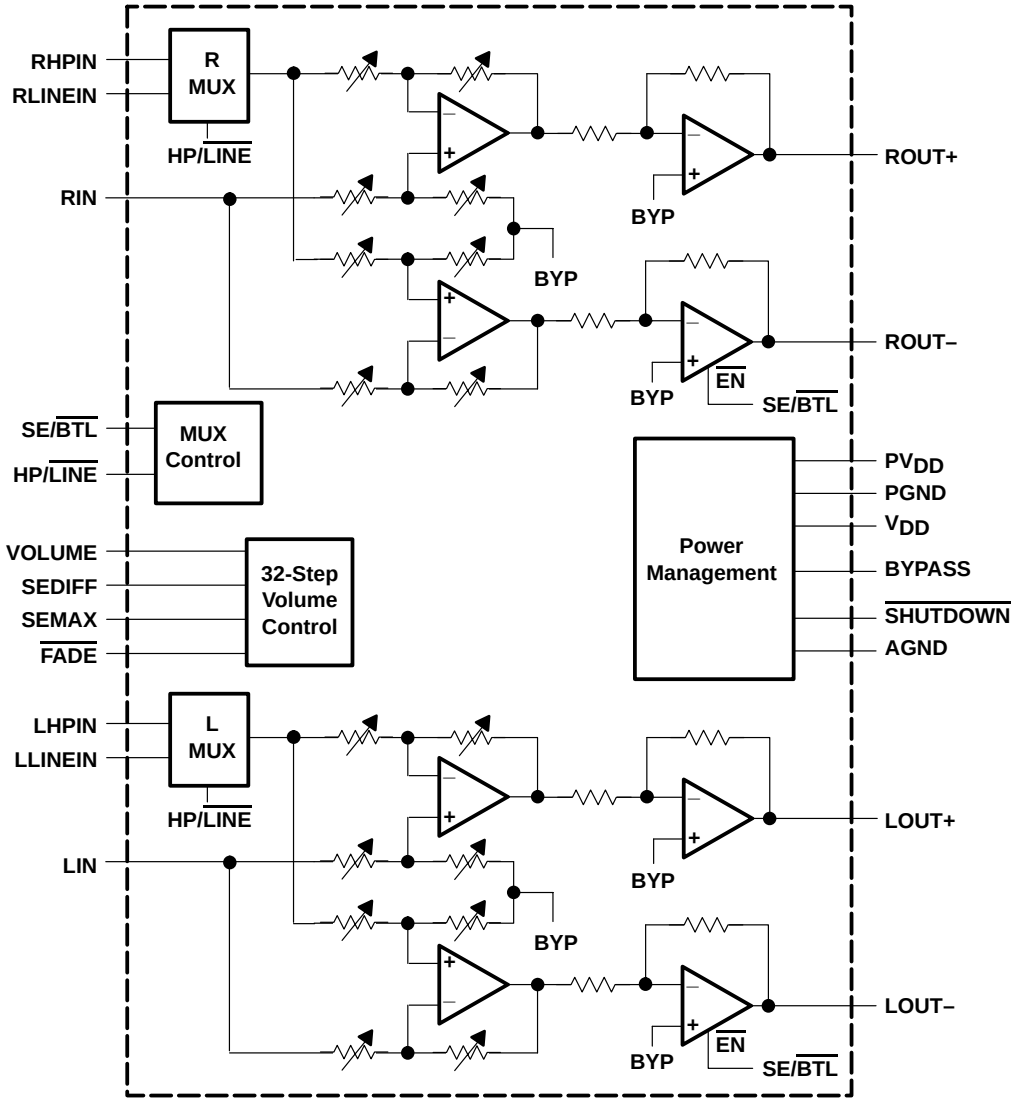
PWP PACKAGE
(TOP VIEW)



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
PGND	1, 13	–	Power ground
LOUT–	12	O	Left channel negative audio output
PV_{DD}	3, 11	–	Supply voltage terminal for power stage
LHPIN	10	I	Left channel headphone input, selected when HP/$\overline{\text{LINE}}$ is held high
LLINEIN	9	I	Left channel line input, selected when HP/$\overline{\text{LINE}}$ is held low
LIN	8	I	Common left channel input for fully differential input. AC ground for single-ended inputs.
V_{DD}	7	–	Supply voltage terminal
RIN	6	I	Common right channel input for fully differential input. AC ground for single-ended inputs.
RLINEIN	5	I	Right channel line input, selected when HP/$\overline{\text{LINE}}$ is held low
RHPIN	4	I	Right channel headphone input, selected when HP/$\overline{\text{LINE}}$ is held high
ROUT–	2	O	Right channel negative audio output
ROUT+	24	O	Right channel positive audio output
$\overline{\text{SHUTDOWN}}$	15	I	Places the amplifier in shutdown mode if a TTL logic low is placed on this terminal
$\overline{\text{FADE}}$	16	I	Places the amplifier in fade mode if a logic low is placed on this terminal; normal operation if a logic high is placed on this terminal
BYPASS	17	I	Tap to voltage divider for internal midsupply bias generator used for analog reference
AGND	18	–	Analog power supply ground
SEMAX	19	I	Sets the maximum volume for single ended operation. DC voltage range is 0 to V_{DD}.
SEDIFF	20	I	Sets the difference between BTL volume and SE volume. DC voltage range is 0 to V_{DD}.
VOLUME	21	I	Terminal for dc volume control. DC voltage range is 0 to V_{DD}.
HP/$\overline{\text{LINE}}$	22	I	Input MUX control. When logic high, RHPIN and LHPIN inputs are selected. When logic low, RLINEIN and LLINEIN inputs are selected.
SE/$\overline{\text{BTL}}$	23	I	Output MUX control. When this terminal is high, SE outputs are selected. When this terminal is low, BTL outputs are selected.
LOUT+	14	O	Left channel positive audio output.

functional block diagram



NOTE: All resistor wipers are adjusted with 32 step volume control.

Table 1. DC Volume Control (BTL Mode, V_{DD} = 5 V)

VOLUME (PIN 21)		GAIN OF AMPLIFIER (Typ)
FROM (V)	TO (V)	
0.00	0.26	–85†
0.33	0.37	–40
0.44	0.48	–38
0.56	0.59	–36
0.67	0.70	–34
0.78	0.82	–32
0.89	0.93	–30
1.01	1.04	–28
1.12	1.16	–26
1.23	1.27	–24
1.35	1.38	–22
1.46	1.49	–20
1.57	1.60	–18
1.68	1.72	–16
1.79	1.83	–14
1.91	1.94	–12
2.02	2.06	–10
2.13	2.17	–8
2.25	2.28	–6†
2.36	2.39	–4
2.47	2.50	–2
2.58	2.61	0
2.70	2.73	2
2.81	2.83	4
2.92	2.95	6
3.04	3.06	8
3.15	3.17	10
3.26	3.29	12
3.38	3.40	14
3.49	3.51	16
3.60	3.63	18
3.71	5.00	20†

† Tested in production. Remaining gain steps are specified by design.

NOTE: For other values of V_{DD}, scale the voltage values in the table by a factor of $V_{DD}/5$.

Table 2. DC Volume Control (SE Mode, V_{DD} = 5 V)

SE_VOLUME = VOLUME – SEDIFF or SEMAX		GAIN OF AMPLIFIER (Typ)
FROM (V)	TO (V)	
0.00	0.26	–85†
0.33	0.37	–46
0.44	0.48	–44
0.56	0.59	–42
0.67	0.70	–40
0.78	0.82	–38
0.89	0.93	–36
1.01	1.04	–34
1.12	1.16	–32
1.23	1.27	–30
1.35	1.38	–28
1.46	1.49	–26
1.57	1.60	–24
1.68	1.72	–22
1.79	1.83	–20
1.91	1.94	–18
2.02	2.06	–16
2.13	2.17	–14
2.25	2.28	–12
2.36	2.39	–10
2.47	2.50	–8
2.58	2.61	–6†
2.70	2.73	–4
2.81	2.83	–2
2.92	2.95	0†
3.04	3.06	2
3.15	3.17	4
3.26	3.29	6†
3.38	3.40	8
3.49	3.51	10
3.60	3.63	12
3.71	5.00	14

† Tested in production. Remaining gain steps are specified by design.

NOTE: For other values of V_{DD}, scale the voltage values in the table by a factor of $V_{DD}/5$.

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
THD+N	Total harmonic distortion plus noise (BTL)	vs Frequency	1, 2 3
		vs Output power	6, 7, 8
THD+N	Total harmonic distortion plus noise (SE)	vs Frequency	4, 5
		vs Output power	9
		vs Output voltage	10
	Closed loop response		11, 12
I_{CC}	Supply current	vs Temperature	13
		vs Supply voltage	14, 15, 16
P_D	Power Dissipation	vs Output power	17, 18
P_O	Output power	vs Load resistance	19
	Crosstalk	vs Frequency	20, 21
	HP/$\overline{\text{LINE}}$ attenuation	vs Frequency	22
PSRR	Power supply ripple rejection (BTL)	vs Frequency	23
PSRR	Power supply ripple rejection (SE)	vs Frequency	24
Z_I	Input impedance	vs BTL gain	25
V_n	Output noise voltage	vs Frequency	26

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION + NOISE (BTL)
vs
FREQUENCY

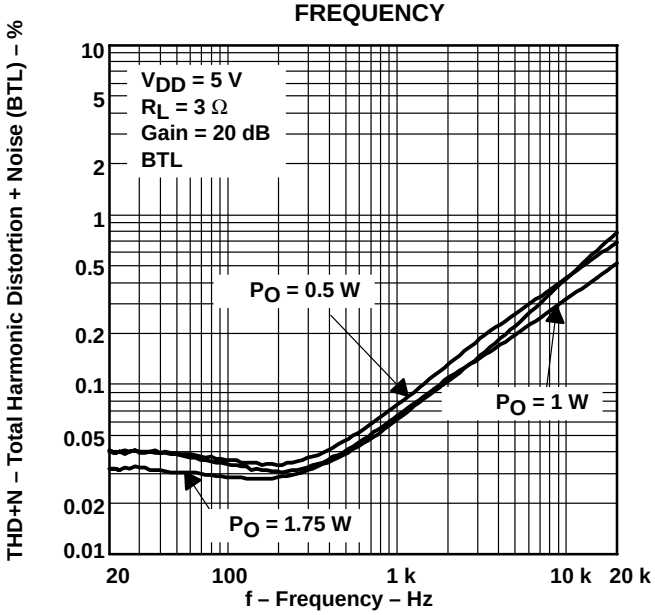


Figure 1

TOTAL HARMONIC DISTORTION + NOISE (BTL)
vs
FREQUENCY

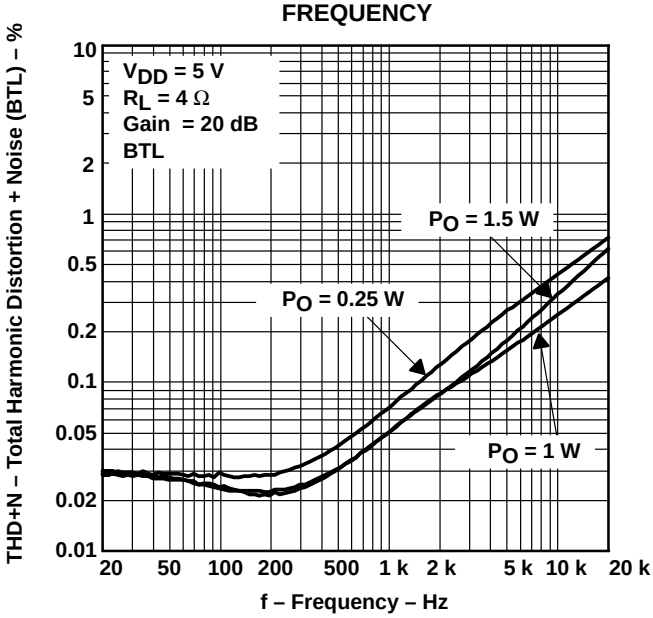


Figure 2

TOTAL HARMONIC DISTORTION + NOISE (BTL)
vs
FREQUENCY

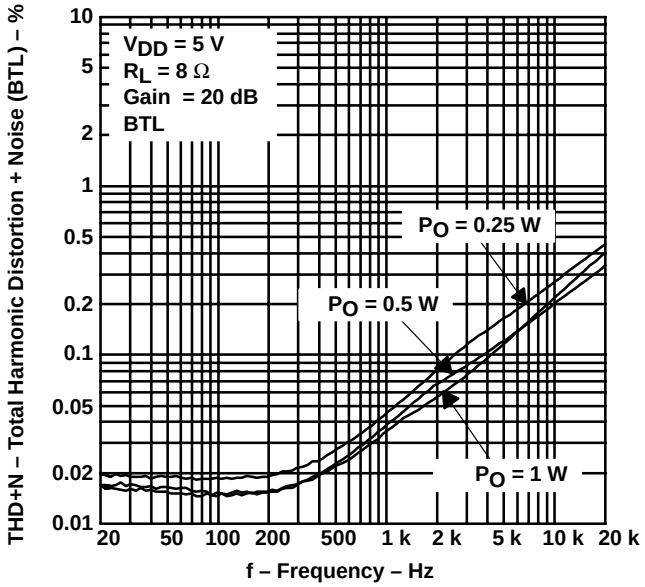


Figure 3

TOTAL HARMONIC DISTORTION + NOISE (SE)
vs
FREQUENCY

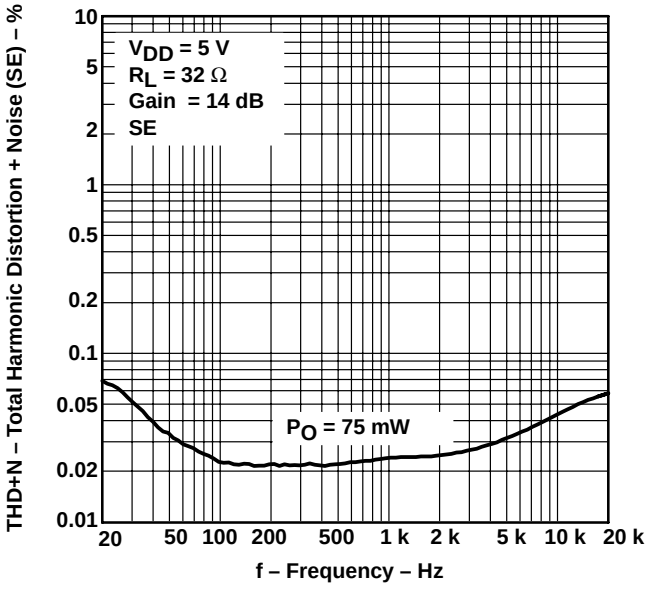


Figure 4

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION + NOISE (SE)
vs
FREQUENCY

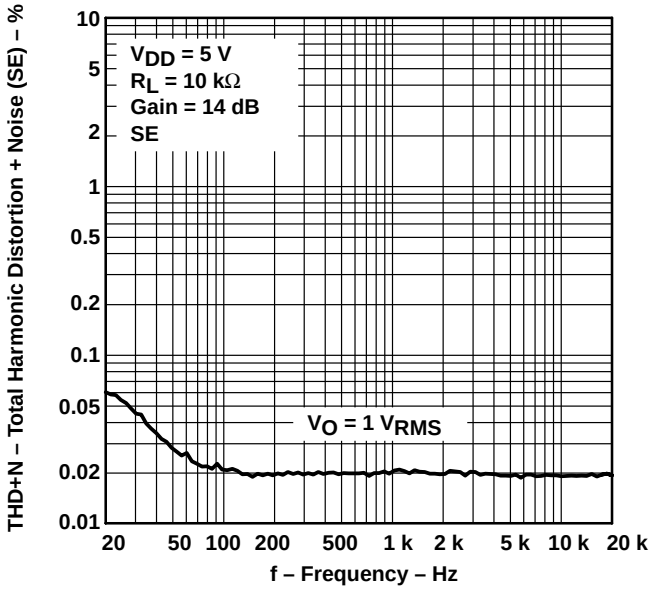


Figure 5

TOTAL HARMONIC DISTORTION + NOISE (BTL)
vs
OUTPUT POWER

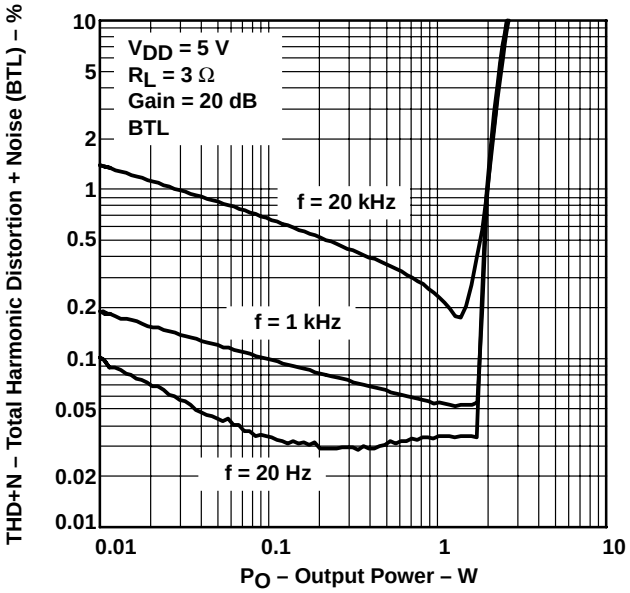


Figure 6

TOTAL HARMONIC DISTORTION + NOISE (BTL)
vs
OUTPUT POWER

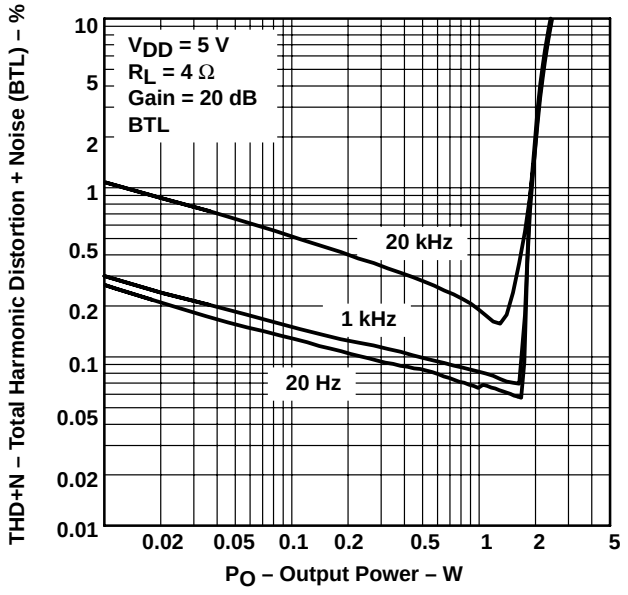


Figure 7

TOTAL HARMONIC DISTORTION + NOISE (BTL)
vs
OUTPUT POWER

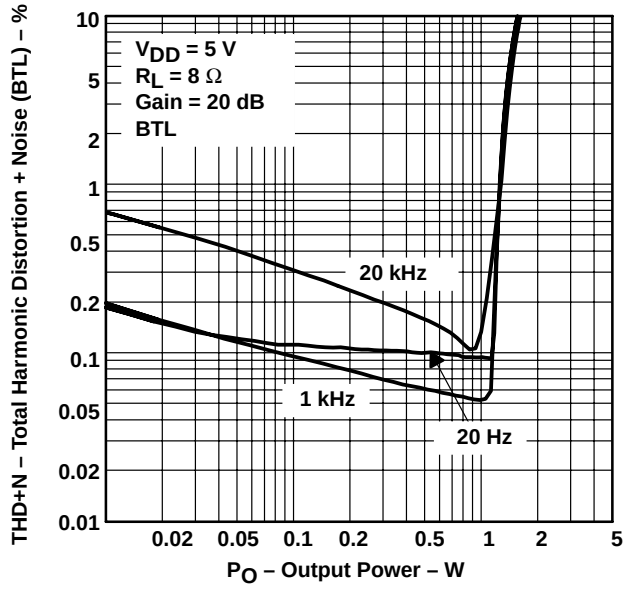


Figure 8

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION + NOISE (SE)
vs
OUTPUT POWER

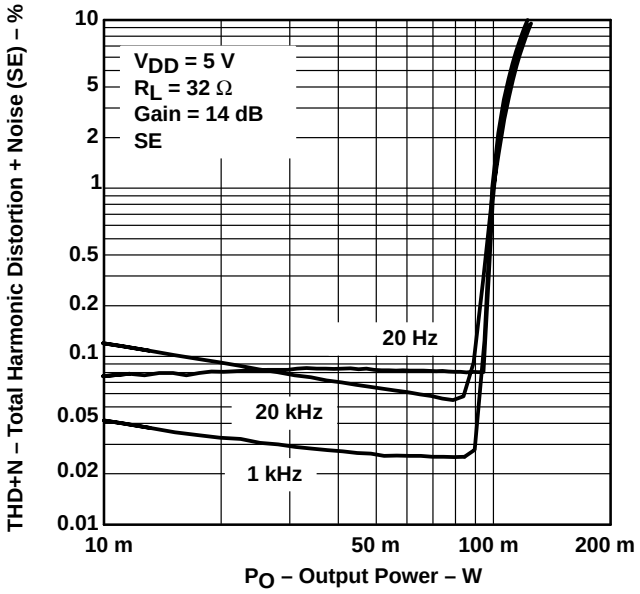


Figure 9

TOTAL HARMONIC DISTORTION + NOISE (SE)
vs
OUTPUT VOLTAGE

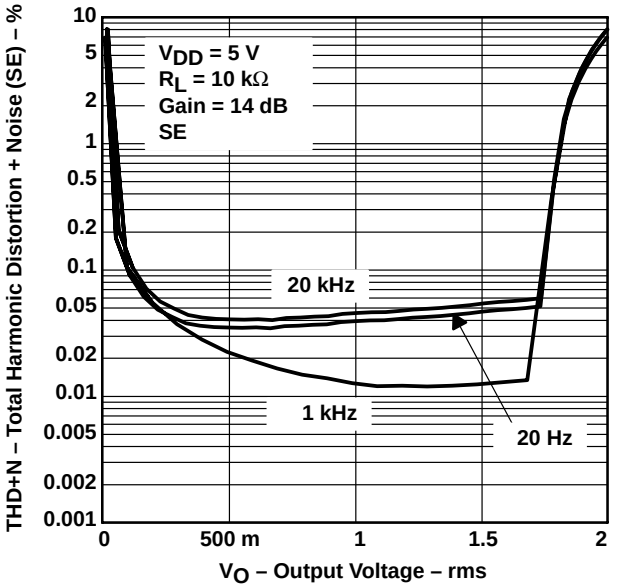


Figure 10

CLOSED LOOP RESPONSE

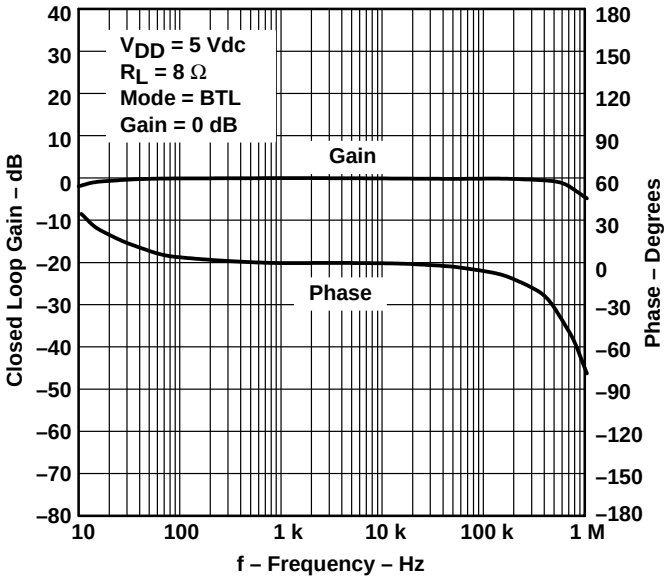


Figure 11

CLOSED LOOP RESPONSE

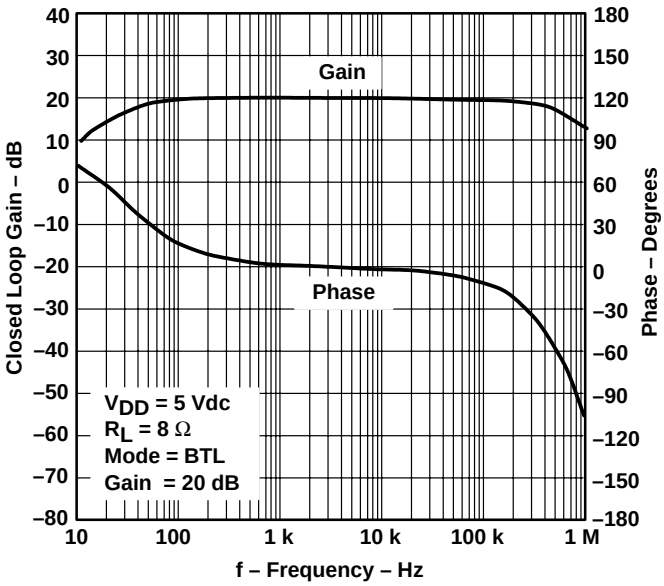


Figure 12

TYPICAL CHARACTERISTICS

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

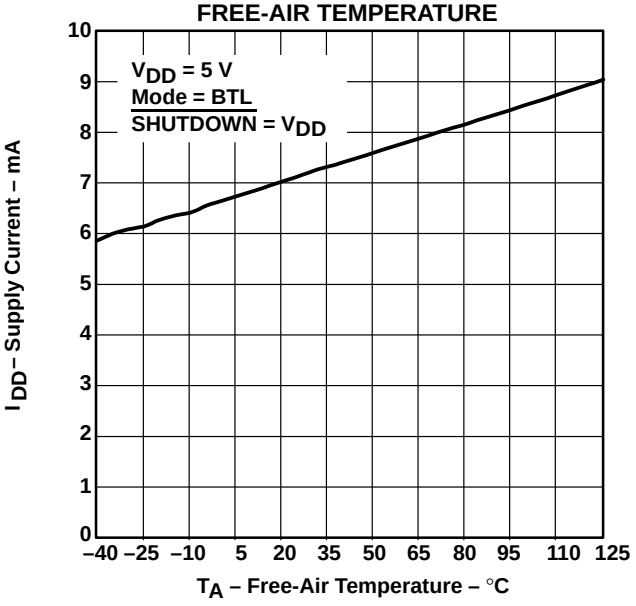


Figure 13

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

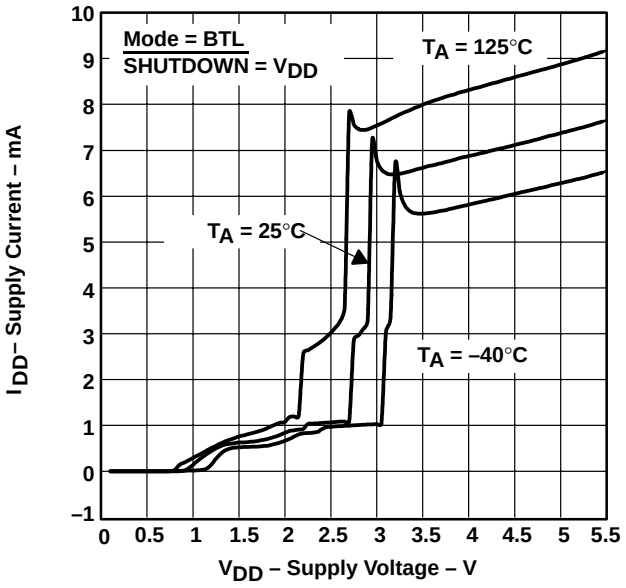


Figure 14

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

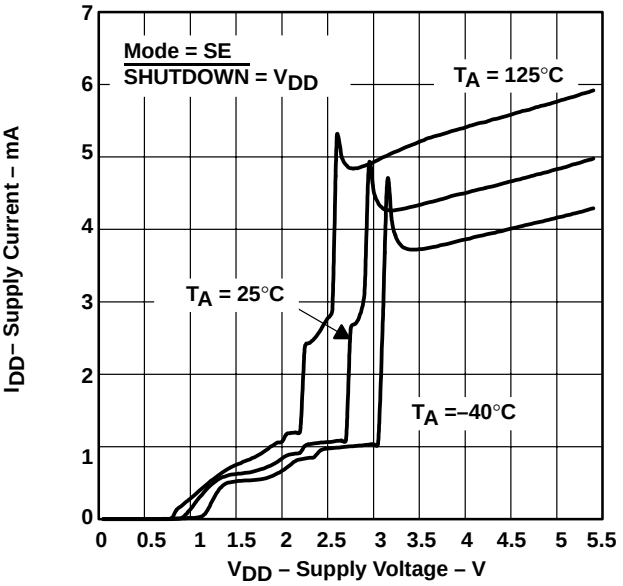


Figure 15

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

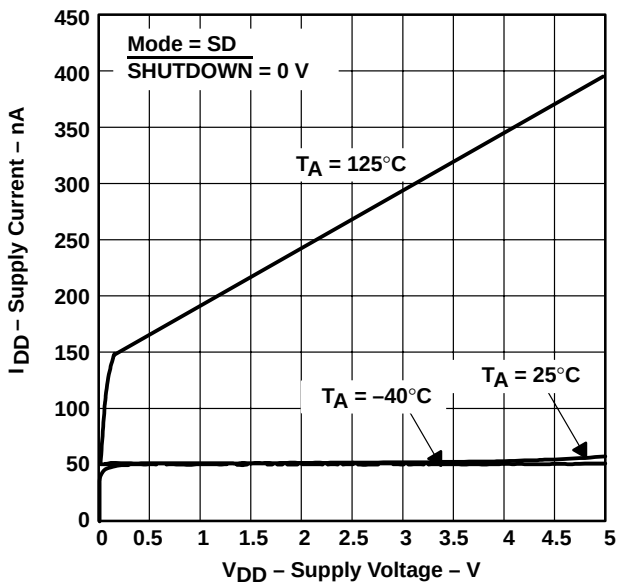


Figure 16

TYPICAL CHARACTERISTICS

**POWER DISSIPATION (PER CHANNEL)
vs
OUTPUT POWER**

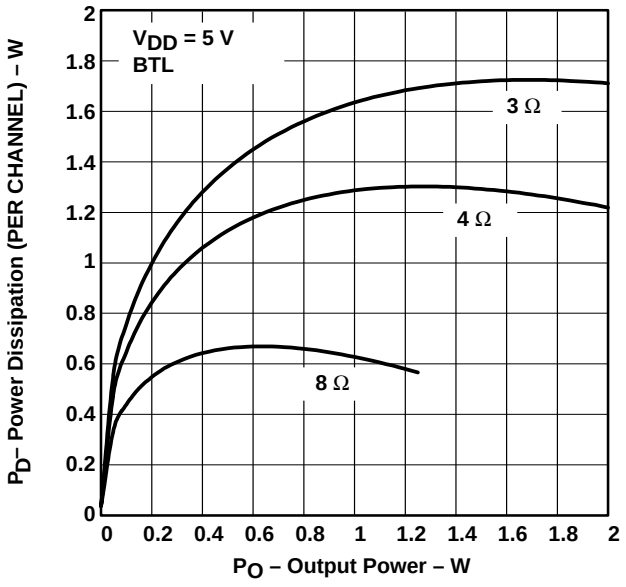


Figure 17

**POWER DISSIPATION (PER CHANNEL)
vs
OUTPUT POWER**

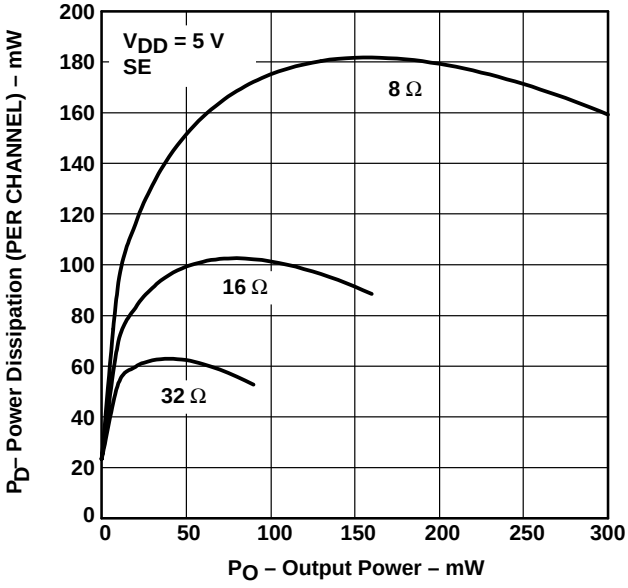


Figure 18

**OUTPUT POWER
vs
LOAD RESISTANCE**

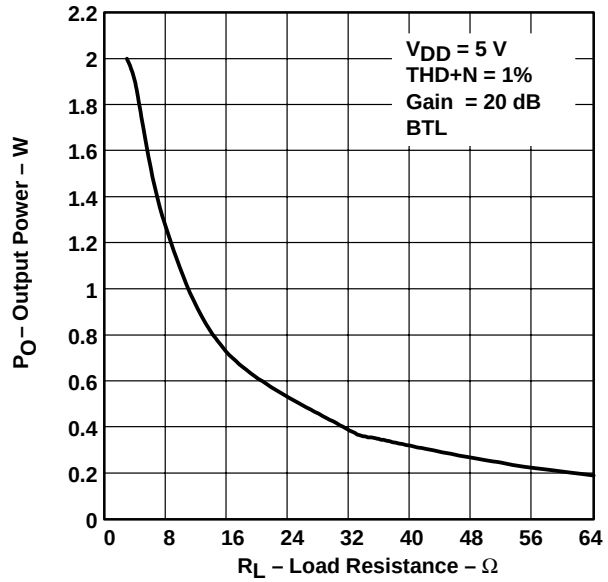


Figure 19

**CROSSTALK
vs
FREQUENCY**

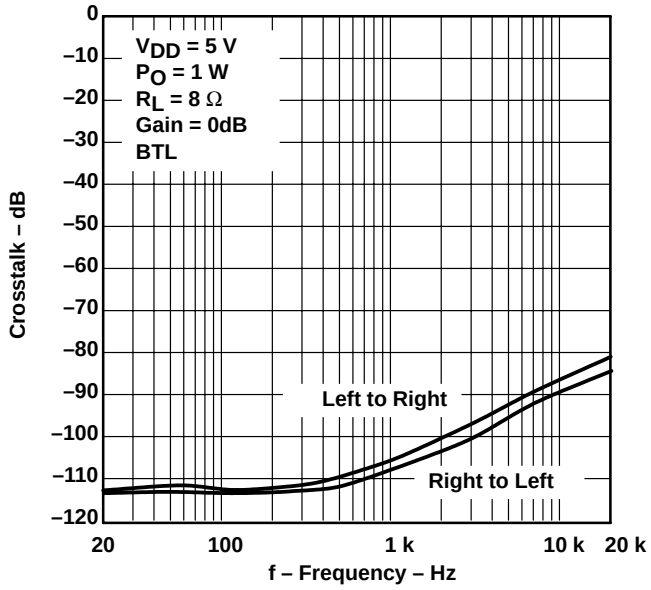


Figure 20

TYPICAL CHARACTERISTICS

CROSSTALK
vs
FREQUENCY

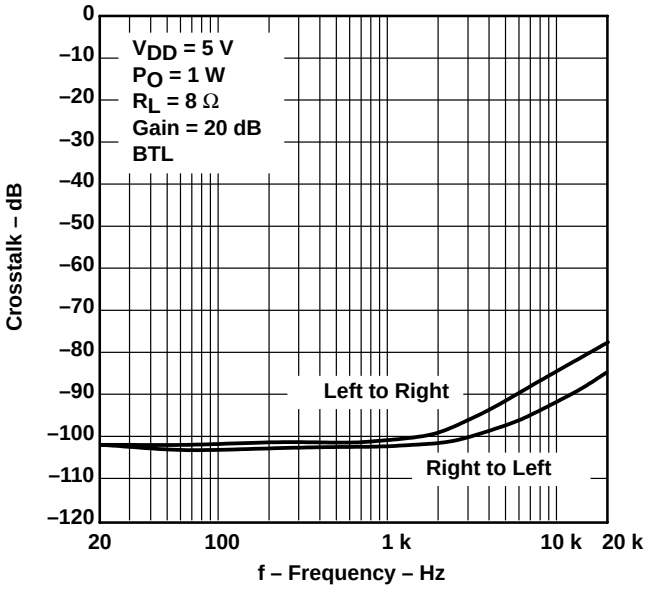


Figure 21

HP/LINE ATTENUATION
vs
FREQUENCY

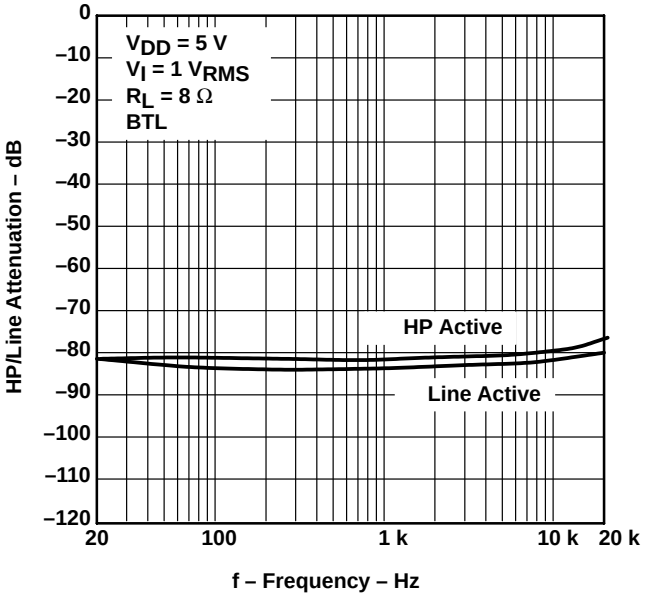


Figure 22

POWER SUPPLY REJECTION RATIO (BTL)
vs
FREQUENCY

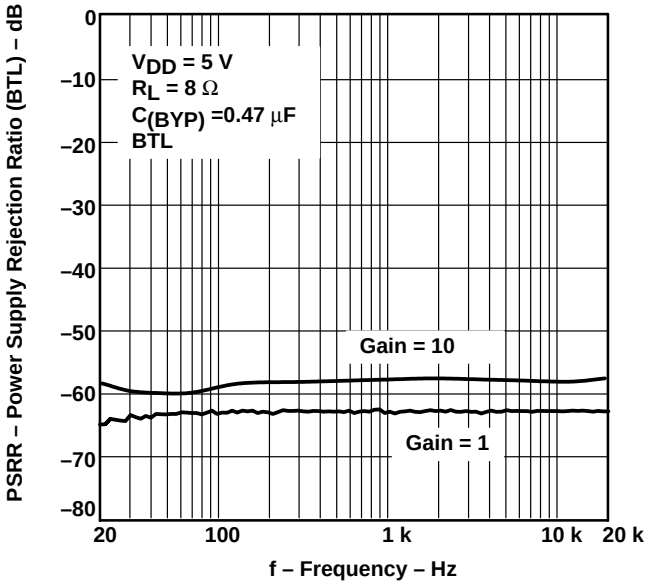


Figure 23

POWER SUPPLY REJECTION RATIO (SE)
vs
FREQUENCY

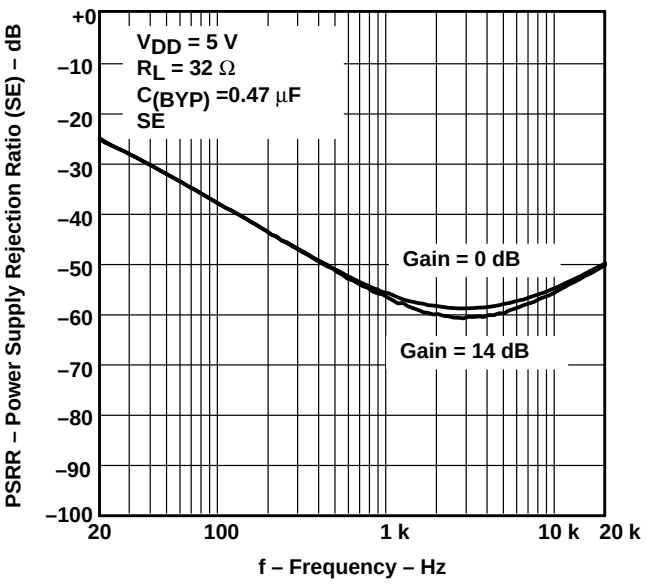


Figure 24

TYPICAL CHARACTERISTICS

INPUT IMPEDANCE
vs
BTL GAIN

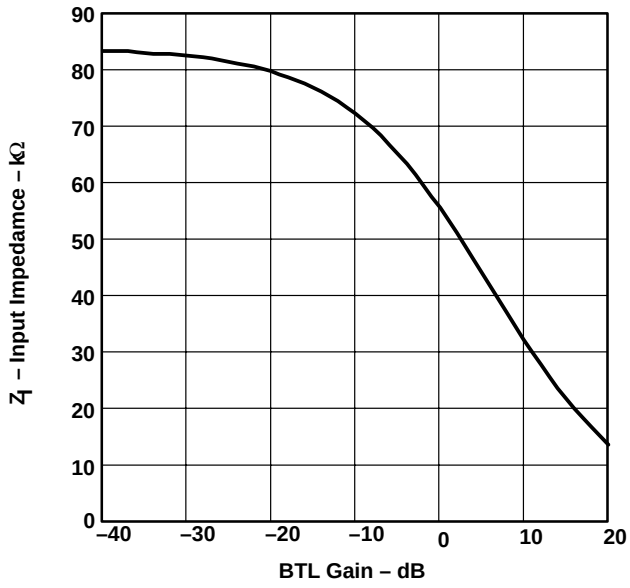


Figure 25

OUTPUT NOISE VOLTAGE
vs
FREQUENCY

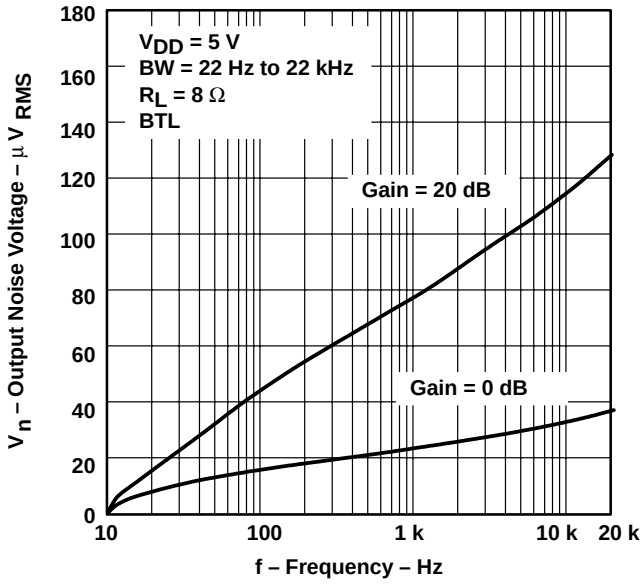
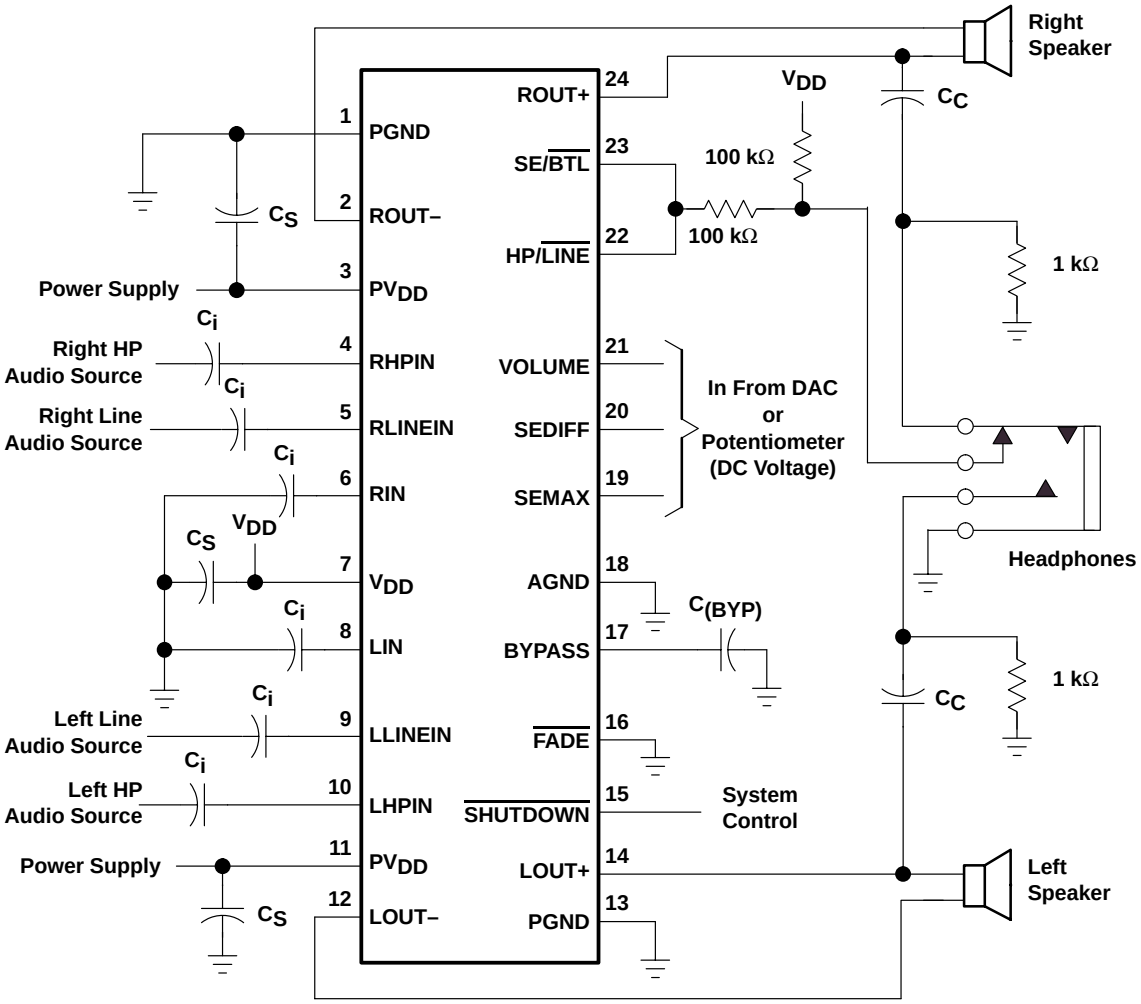


Figure 26

APPLICATION INFORMATION

selection of components

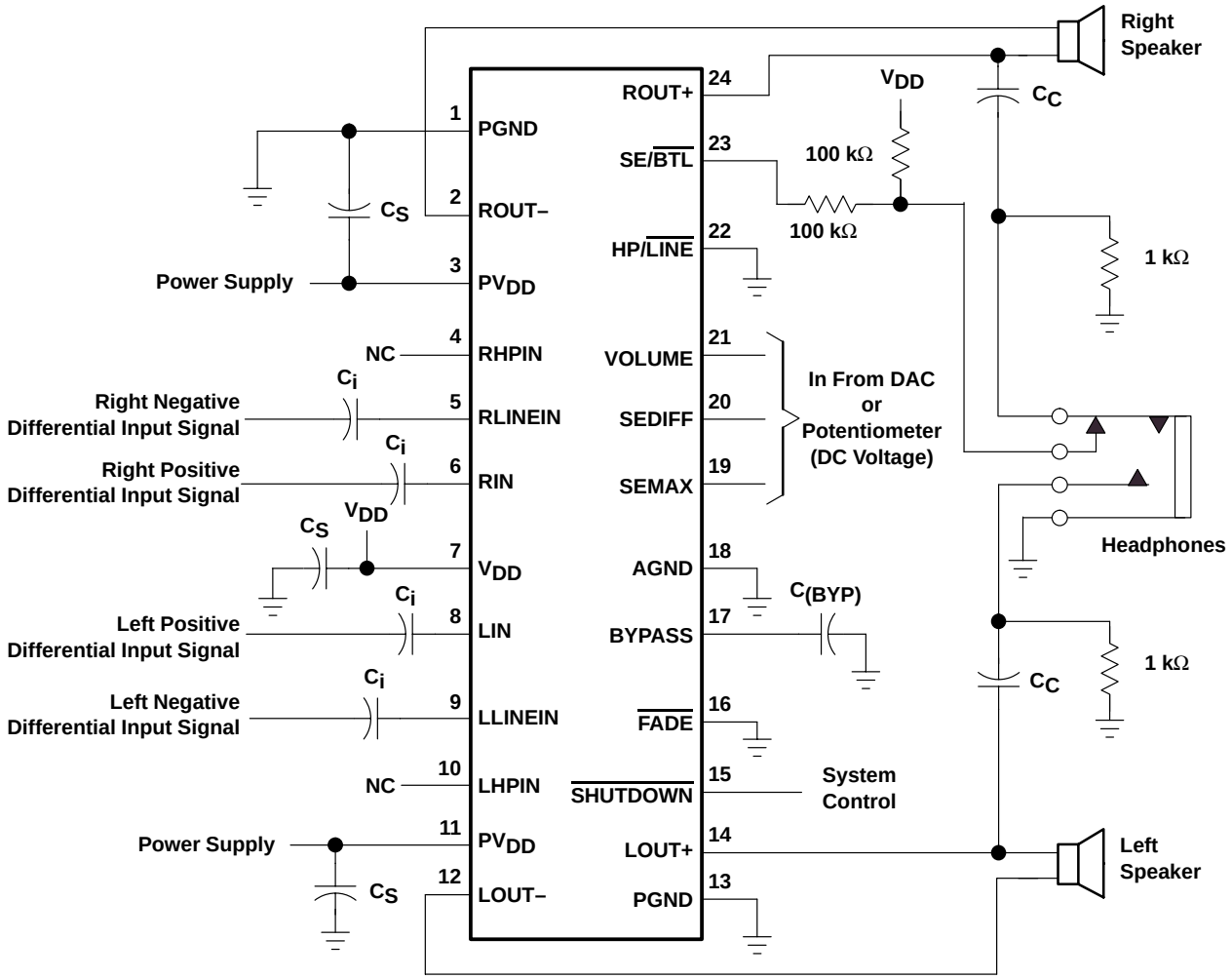
Figure 27 and Figure 28 are schematic diagrams of typical notebook computer application circuits.



NOTE A: A 0.1-μF ceramic capacitor should be placed as close as possible to the IC. For filtering lower-frequency noise signals, a larger electrolytic capacitor of 10 μF or greater should be placed near the audio power amplifier.

Figure 27. Typical TPA6011A4 Application Circuit Using Single-Ended Inputs and Input MUX

APPLICATION INFORMATION



NOTE A: A 0.1-µF ceramic capacitor should be placed as close as possible to the IC. For filtering lower-frequency noise signals, a larger electrolytic capacitor of 10 µF or greater should be placed near the audio power amplifier.

Figure 28. Typical TPA6011A4 Application Circuit Using Differential Inputs

SE/$\overline{\text{BTL}}$ operation

The ability of the TPA6011A4 to easily switch between BTL and SE modes is one of its most important cost saving features. This feature eliminates the requirement for an additional headphone amplifier in applications where internal stereo speakers are driven in BTL mode but external headphone or speakers must be accommodated. Internal to the TPA6011A4, two separate amplifiers drive OUT+ and OUT–. The SE/$\overline{\text{BTL}}$ input controls the operation of the follower amplifier that drives LOUT– and ROUT–. When SE/$\overline{\text{BTL}}$ is held low, the amplifier is on and the TPA6011A4 is in the BTL mode. When SE/$\overline{\text{BTL}}$ is held high, the OUT– amplifiers are in a high output impedance state, which configures the TPA6011A4 as an SE driver from LOUT+ and ROUT+. I_{DD} is reduced by approximately one-third in SE mode. Control of the SE/$\overline{\text{BTL}}$ input can be from a logic-level CMOS source or, more typically, from a resistor divider network as shown in Figure 29. The trip level for the SE/$\overline{\text{BTL}}$ input can be found in the *recommended operating conditions* table on page 4.

APPLICATION INFORMATION

SE/$\overline{\text{BTL}}$ operation (continued)

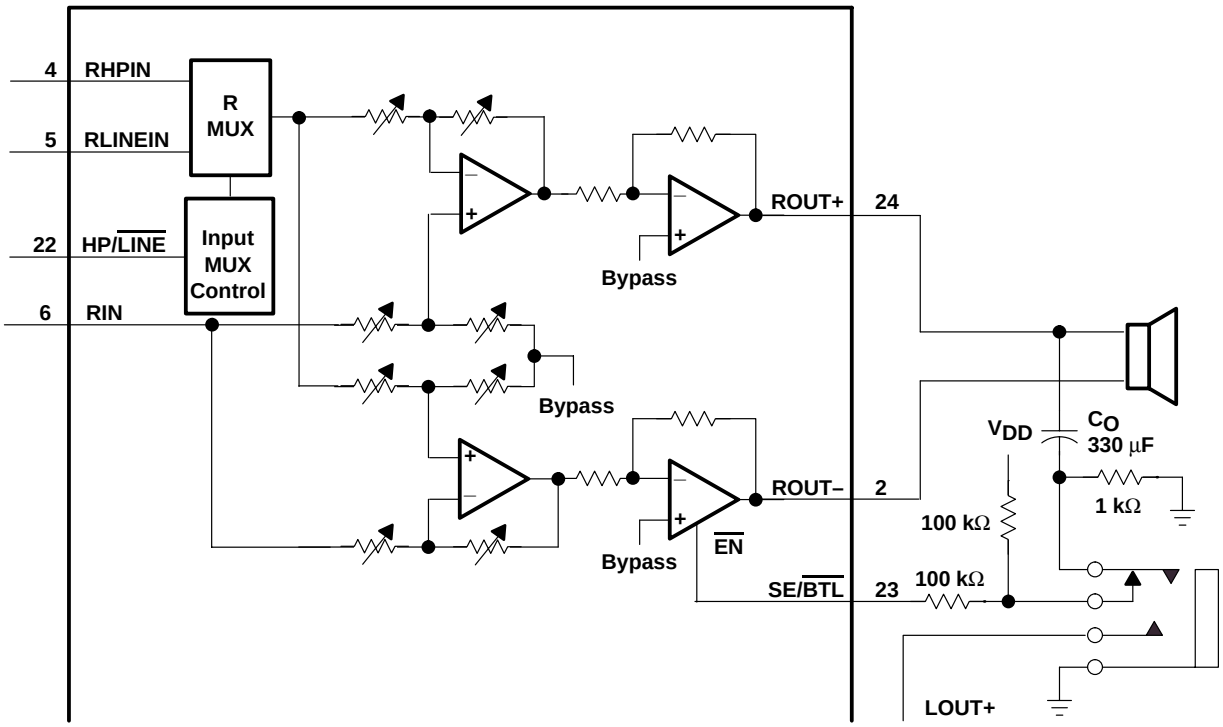


Figure 29. TPA6011A4 Resistor Divider Network Circuit

Using a 1/8-in. (3,5 mm) stereo headphone jack, the control switch is closed when no plug is inserted. When closed the 100-kΩ/1-kΩ divider pulls the SE/$\overline{\text{BTL}}$ input low. When a plug is inserted, the 1-kΩ resistor is disconnected and the SE/$\overline{\text{BTL}}$ input is pulled high. When the input goes high, the OUT– amplifier is shut down causing the speaker to mute (open-circuits the speaker). The OUT+ amplifier then drives through the output capacitor (C_o) into the headphone jack.

HP/$\overline{\text{LINE}}$ operation

The HP/$\overline{\text{LINE}}$ input controls the internal input multiplexer (MUX). Refer to the block diagram in Figure 29. This allows the device to switch between two separate stereo inputs to the amplifier. For design flexibility, the HP/$\overline{\text{LINE}}$ control is independent of the output mode, SE or BTL, which is controlled by the aforementioned SE/$\overline{\text{BTL}}$ pin. To allow the amplifier to switch from the LINE inputs to the HP inputs when the output switches from BTL mode to SE mode, simply connect the SE/$\overline{\text{BTL}}$ control input to the HP/$\overline{\text{LINE}}$ input.

When this input is logic high, the RHPIN and LHPIN inputs are selected. When this terminal is logic low, the RLINEIN and LLINEIN inputs are selected. This operation is also detailed in Table 3 and the trip levels for a logic low (V_{IL}) or logic high (V_{IH}) can be found in the *recommended operating conditions* table on page 4.

APPLICATION INFORMATION

shutdown modes

The TPA6011A4 employs a shutdown mode of operation designed to reduce supply current (I_{DD}) to the absolute minimum level during periods of nonuse for battery-power conservation. The $\overline{\text{SHUTDOWN}}$ input terminal should be held high during normal operation when the amplifier is in use. Pulling $\overline{\text{SHUTDOWN}}$ low causes the outputs to mute and the amplifier to enter a low-current state, I_{DD} = 20 μA. $\overline{\text{SHUTDOWN}}$ should never be left unconnected because amplifier operation would be unpredictable.

Table 3. HP/$\overline{\text{LINE}}$, SE/$\overline{\text{BTL}}$, and Shutdown Functions

INPUTS†			AMPLIFIER STATE	
HP/$\overline{\text{LINE}}$	SE/$\overline{\text{BTL}}$	$\overline{\text{SHUTDOWN}}$	INPUT	OUTPUT
X	X	Low	X	Mute
Low	Low	High	Line	BTL
Low	High	High	Line	SE
High	Low	High	HP	BTL
High	High	High	HP	SE

† Inputs should never be left unconnected.
X = don't care
NOTE: The *Low* and *High* trip levels can be found in the *recommended operating conditions* table.

$\overline{\text{FADE}}$ operation

For design flexibility, a fade mode is provided to slowly ramp up the amplifier gain when coming out of shutdown mode and conversely ramp the gain down when going into shutdown. This mode provides a smooth transition between the active and shutdown states and virtually eliminates any pops or clicks on the outputs.

When the $\overline{\text{FADE}}$ input is a logic low, the device is placed into fade-on mode. A logic high on this pin places the amplifier in the fade-off mode. The voltage trip levels for a logic low (V_{IL}) or logic high (V_{IH}) can be found in the *recommended operating conditions* table on page 4.

When a logic low is applied to the $\overline{\text{FADE}}$ pin and a logic low is then applied on the $\overline{\text{SHUTDOWN}}$ pin, the channel gain steps down from gain step to gain step at a rate of two clock cycles per step. With a nominal internal clock frequency of 58 Hz, this equates to 34 ms (1/24 Hz) per step. The gain steps down until the lowest gain step is reached. The time it takes to reach this step depends on the gain setting prior to placing the device in shutdown. For example, if the amplifier is in the highest gain mode of 20 dB, the time it takes to ramp down the channel gain is 1.05 seconds. This number is calculated by taking the number of steps to reach the lowest gain from the highest gain, or 31 steps, and multiplying by the time per step, or 34 ms.

After the channel gain is stepped down to the lowest gain, the amplifier begins discharging the bypass capacitor from the nominal voltage of V_{DD}/2 to ground. This time is dependent on the value of the bypass capacitor. For a 0.47-μF capacitor that is used in the application diagram in Figure 27, the time is approximately 500 ms. This time scales linearly with the value of bypass capacitor. For example, if a 1-μF capacitor is used for bypass, the time period to discharge the capacitor to ground is twice that of the 0.47-μF capacitor, or 1 second. Figure 30 below is a waveform captured at the output during the shutdown sequence when the part is in fade-on mode. The gain is set to the highest level and the output is at V_{DD} when the amplifier is shut down.

When a logic high is placed on the $\overline{\text{SHUTDOWN}}$ pin and the $\overline{\text{FADE}}$ pin is still held low, the device begins the start-up process. The bypass capacitor will begin charging. Once the bypass voltage reaches the final value of V_{DD}/2, the gain increases in 2-dB steps from the lowest gain level to the gain level set by the dc voltage applied to the VOLUME, SEDIFF, and SEMAX pins.

APPLICATION INFORMATION

$\overline{\text{FADE}}$ operation (continued)

In the fade-off mode, the amplifier stores the gain value prior to starting the shutdown sequence. The output of the amplifier immediately drops to $V_{DD}/2$ and the bypass capacitor begins a smooth discharge to ground. When shutdown is released, the bypass capacitor charges up to $V_{DD}/2$ and the channel gain returns immediately to the value stored in memory. Figure 31 below is a waveform captured at the output during the shutdown sequence when the part is in the fade-off mode. The gain is set to the highest level, and the output is at V_{DD} when the amplifier is shut down.

The power-up sequence is different from the shutdown sequence and the voltage on the $\overline{\text{FADE}}$ pin does not change the power-up sequence. Upon a power-up condition, the TPA6011A4 begins in the lowest gain setting and steps up 2 dB every 2 clock cycles until the final value is reached as determined by the dc voltage applied to the VOLUME, SEDIFF, and SEMAX pins.

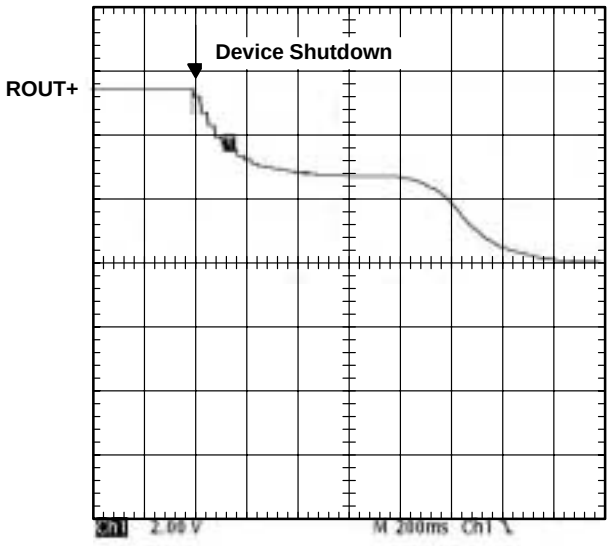


Figure 30. Shutdown Sequence in the Fade-on Mode

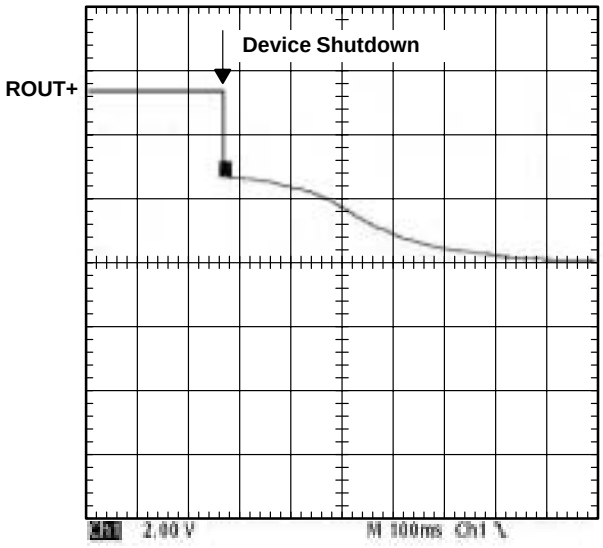


Figure 31. Shutdown Sequence in the Fade-off Mode

APPLICATION INFORMATION

VOLUME, SEDIFF, and SEMAX operation

Three pins labeled VOLUME, SEDIFF, and SEMAX control the BTL volume when driving speakers and the SE volume when driving headphones. All of these pins are controlled with a dc voltage, which should not exceed V_{DD}.

When driving speakers in BTL mode, the VOLUME pin is the only pin that controls the gain. Table 1 shows the gain for the BTL mode. The voltages listed in the table are for V_{DD} = 5 V. For a different V_{DD}, the values in the table scale linearly. If V_{DD} = 4 V, multiply all the voltages in the table by 4 V/5 V, or 0.8.

The TPA6011A4 allows the user to specify a difference between BTL gain and SE gain. This is desirable to avoid any listening discomfort when plugging in headphones. When switching to SE mode, the SEDIFF and SEMAX pins control the singe-ended gain proportional to the gain set by the voltage on the VOLUME pin. When SEDIFF = 0 V, the difference between the BTL gain and the SE gain is 6 dB. Refer to the section labeled *bridged-tied load versus single-ended load* for an explanation on why the gain in BTL mode is 2x that of single-ended mode, or 6dB greater. As the voltage on the SEDIFF terminal is increased, the gain in SE mode decreases. The voltage on the SEDIFF terminal is subtracted from the voltage on the VOLUME terminal and this value is used to determine the SE gain.

Some audio systems require that the gain be limited in the single-ended mode to a level that is comfortable for headphone listening. Most volume control devices only have one terminal for setting the gain. For example, if the speaker gain is 20 dB, the gain in the headphone channel is fixed at 14 dB. This level of gain could cause discomfort to listeners and the SEMAX pin allows the designer to limit this discomfort when plugging in headphones. The SEMAX terminal controls the maximum gain for single-ended mode.

The functionality of the SEDIFF and SEMAX pin are combined to set the SE gain. A block diagram of the combined functionality is shown in Figure 32. The value obtained from the block diagram for SE_VOLUME is a dc voltage that can be used in conjunction with Table 2 to determine the SE gain. Again, the voltages listed in the table are for V_{DD} = 5V. The values must be scaled for other values of V_{DD}.

Tables 1 and 2 show a range of voltages for each gain step. There is a gap in the voltage between each gain step. This gap represents the hysteresis about each trip point in the internal comparator. The hysteresis ensures that the gain control is monotonic and does not oscillate from one gain step to another. If a potentiometer is used to adjust the voltage on the control terminals, the gain increases as the potentiometer is turned in one direction and decreases as it is turned back the other direction. The trip point, where the gain actually changes, is different depending on whether the voltage is increased or decreased as a result of the hysteresis about each trip point. The gaps in tables 1 and 2 can also be thought of as indeterminate states where the gain could be in the next higher gain step or the lower gain step depending on the direction the voltage is changing. If using a DAC to control the volume, set the voltage in the middle of each range to ensure that the desired gain is achieved.

A pictorial representation of the volume control can be found in Figure 33. The graph focuses on three gain steps with the trip points defined in Table 1 for BTL gain. The dotted line represents the hysteresis about each gain step.

APPLICATION INFORMATION

VOLUME, SEDIFF, and SEMAX operation (continued)

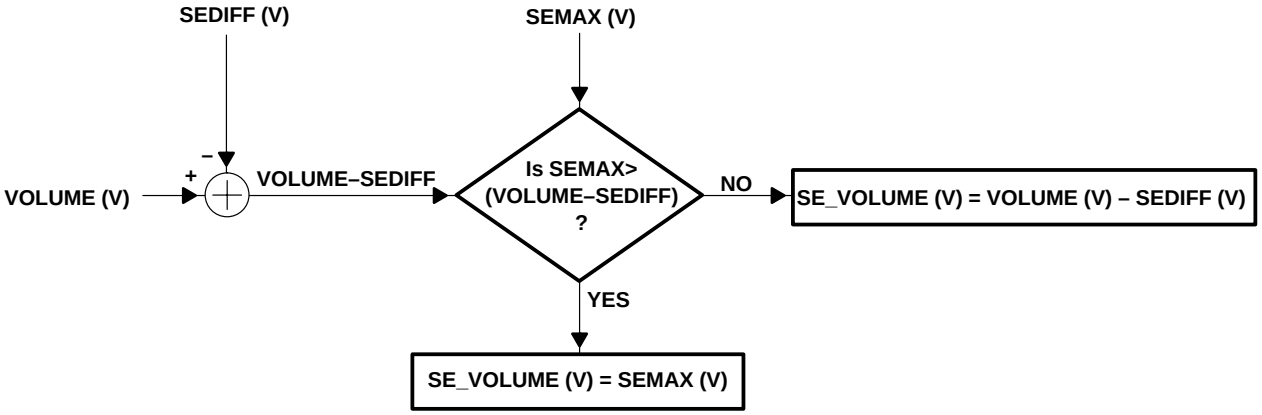


Figure 32. Block Diagram of SE Volume Control

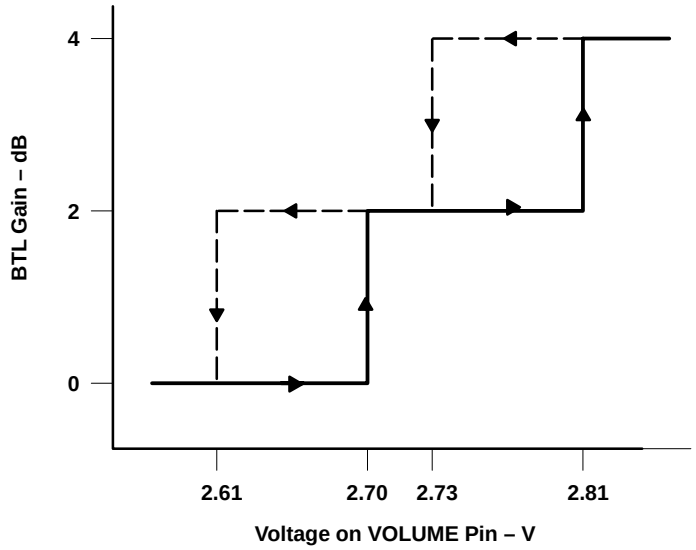


Figure 33. DC Volume Control Operation

APPLICATION INFORMATION

input resistance

Each gain setting is achieved by varying the input resistance of the amplifier, which can range from its smallest value to over six times that value. As a result, if a single capacitor is used in the input high-pass filter, the –3 dB or cutoff frequency also changes by over six times. If an additional resistor is connected from the input pin of the amplifier to ground, as shown in the figure below, the variation of the cutoff frequency is much reduced.

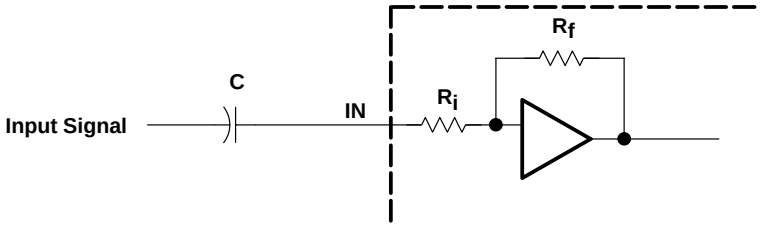


Figure 34. Resistor on Input for Cut-Off Frequency

The input resistance at each gain setting is given in Figure 34.

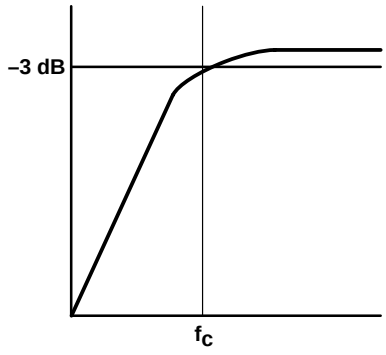
The –3-dB frequency can be calculated using equation 1.

$$f_{-3\ dB} = \frac{1}{2\pi CR_i} \quad (1)$$

input capacitor, C_i

In the typical application an input capacitor (C_i) is required to allow the amplifier to bias the input signal to the proper dc level for optimum operation. In this case, C_i and the input impedance of the amplifier (R_i) form a high-pass filter with the corner frequency determined in equation 2.

$$f_{c(highpass)} = \frac{1}{2\pi R_i C_i} \quad (2)$$



APPLICATION INFORMATION

input capacitor, C_i (continued)

The value of C_i is important to consider as it directly affects the bass (low frequency) performance of the circuit. Consider the example where R_i is 70 kΩ and the specification calls for a flat-bass response down to 40 Hz. Equation 2 is reconfigured as equation 3.

$$C_i = \frac{1}{2\pi R_i f_c} \quad (3)$$

In this example, C_i is 56.8 nF, so one would likely choose a value in the range of 56 nF to 1 μF. A further consideration for this capacitor is the leakage path from the input source through the input network (C_i) and the feedback network to the load. This leakage current creates a dc offset voltage at the input to the amplifier that reduces useful headroom, especially in high gain applications. For this reason, a low-leakage tantalum or ceramic capacitor is the best choice. When polarized capacitors are used, the positive side of the capacitor should face the amplifier input in most applications as the dc level there is held at $V_{DD}/2$, which is likely higher than the source dc level. Note that it is important to confirm the capacitor polarity in the application.

power supply decoupling, $C_{(S)}$

The TPA6011A4 is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure the output total harmonic distortion (THD) is as low as possible. Power supply decoupling also prevents oscillations for long lead lengths between the amplifier and the speaker. The optimum decoupling is achieved by using two capacitors of different types that target different types of noise on the power supply leads. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 0.1 μF placed as close as possible to the device V_{DD} lead, works best. For filtering lower-frequency noise signals, a larger aluminum electrolytic capacitor of 10 μF or greater placed near the audio power amplifier is recommended.

midrail bypass capacitor, $C_{(BYP)}$

The midrail bypass capacitor ($C_{(BYP)}$) is the most critical capacitor and serves several important functions. During start-up or recovery from shutdown mode, $C_{(BYP)}$ determines the rate at which the amplifier starts up. The second function is to reduce noise produced by the power supply caused by coupling into the output drive signal. This noise is from the midrail generation circuit internal to the amplifier, which appears as degraded PSRR and THD+N.

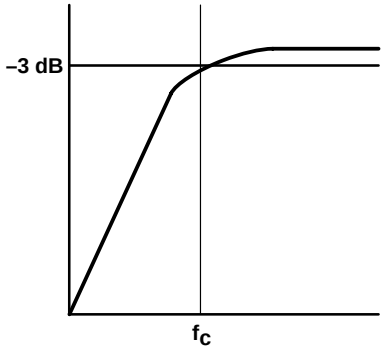
Bypass capacitor ($C_{(BYP)}$) values of 0.47-μF to 1-μF ceramic or tantalum low-ESR capacitors are recommended for the best THD and noise performance. For the best pop performance, choose a value for $C_{(BYP)}$ that is equal to or greater than the value chosen for C_i. This ensures that the input capacitors are charged up to the midrail voltage before $C_{(BYP)}$ is fully charged to the midrail voltage.

APPLICATION INFORMATION

output coupling capacitor, $C_{(C)}$

In the typical single-supply SE configuration, an output coupling capacitor ($C_{(C)}$) is required to block the dc bias at the output of the amplifier, thus preventing dc currents in the load. As with the input coupling capacitor, the output coupling capacitor and impedance of the load form a high-pass filter governed by equation 4.

$$f_{c(high)} = \frac{1}{2\pi R_L C_{(C)}} \quad (4)$$



The main disadvantage, from a performance standpoint, is the load impedances are typically small, which drives the low-frequency corner higher, degrading the bass response. Large values of $C_{(C)}$ are required to pass low frequencies into the load. Consider the example where a $C_{(C)}$ of 330 µF is chosen and loads vary from 3 Ω, 4 Ω, 8 Ω, 32 Ω, 10 kΩ, and 47 kΩ. Table 4 summarizes the frequency response characteristics of each configuration.

Table 4. Common Load Impedances Vs Low Frequency Output Characteristics in SE Mode

R_L	$C_{(C)}$	Lowest Frequency
3 Ω	330 µF	161 Hz
4 Ω	330 µF	120 Hz
8 Ω	330 µF	60 Hz
32 Ω	330 µF	15 Hz
10,000 Ω	330 µF	0.05 Hz
47,000 Ω	330 µF	0.01 Hz

As Table 4 indicates, most of the bass response is attenuated into a 4-Ω load, an 8-Ω load is adequate, headphone response is good, and drive into line level inputs (a home stereo for example) is exceptional.

using low-ESR capacitors

Low-ESR capacitors are recommended throughout this applications section. A real (as opposed to ideal) capacitor can be modeled simply as a resistor in series with an ideal capacitor. The voltage drop across this resistor minimizes the beneficial effects of the capacitor in the circuit. The lower the equivalent value of this resistance, the more the real capacitor behaves like an ideal capacitor.

APPLICATION INFORMATION

bridged-tied load versus single-ended lode

Figure 35 shows a Class-AB audio power amplifier (APA) in a BTL configuration. The TPA6011A4 BTL amplifier consists of two Class-AB amplifiers driving both ends of the load. There are several potential benefits to this differential drive configuration, but, initially consider power to the load. The differential drive to the speaker means that as one side is slewing up, the other side is slewing down, and vice versa. This in effect doubles the voltage swing on the load as compared to a ground referenced load. Plugging $2 \times V_{O(PP)}$ into the power equation, where voltage is squared, yields 4× the output power from the same supply rail and load impedance (see equation 5).

$$V_{(rms)} = \frac{V_{O(PP)}}{2\sqrt{2}} \qquad (5)$$

$$\text{Power} = \frac{V_{(rms)}^2}{R_L}$$

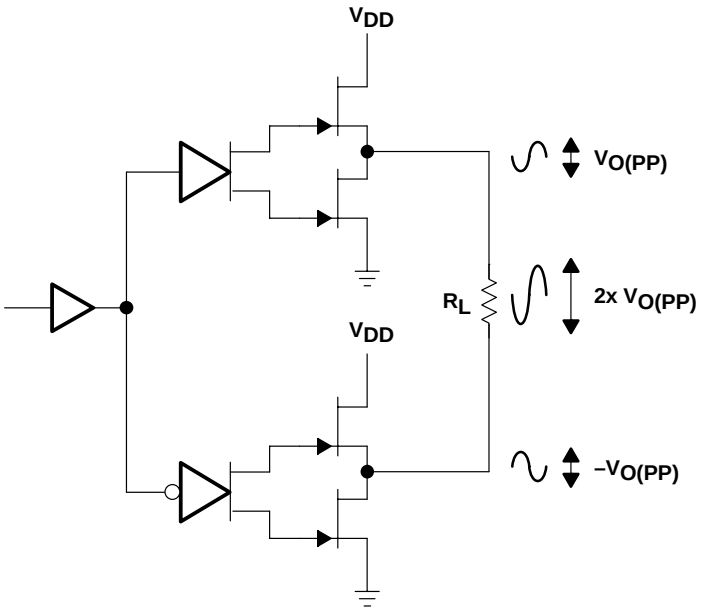


Figure 35. Bridge-Tied Load Configuration

In a typical computer sound channel operating at 5 V, bridging raises the power into an 8-Ω speaker from a singled-ended (SE, ground reference) limit of 250 mW to 1 W. In sound power that is a 6-dB improvement, which is loudness that can be heard. In addition to increased power there are frequency response concerns. Consider the single-supply SE configuration shown in Figure 36. A coupling capacitor is required to block the dc offset voltage from reaching the load. These capacitors can be quite large (approximately 33 μF to 1000 μF), so they tend to be expensive, heavy, occupy valuable PCB area, and have the additional drawback of limiting low-frequency performance of the system. This frequency limiting effect is due to the high-pass filter network created with the speaker impedance and the coupling capacitance and is calculated with equation 6.

$$f_{(c)} = \frac{1}{2\pi R_L C_C} \qquad (6)$$

APPLICATION INFORMATION

bridged-tied load versus single-ended lode (continued)

For example, a 68-μF capacitor with an 8-Ω speaker would attenuate low frequencies below 293 Hz. The BTL configuration cancels the dc offsets, which eliminates the need for the blocking capacitors. Low-frequency performance is then limited only by the input network and speaker response. Cost and PCB space are also minimized by eliminating the bulky coupling capacitor.

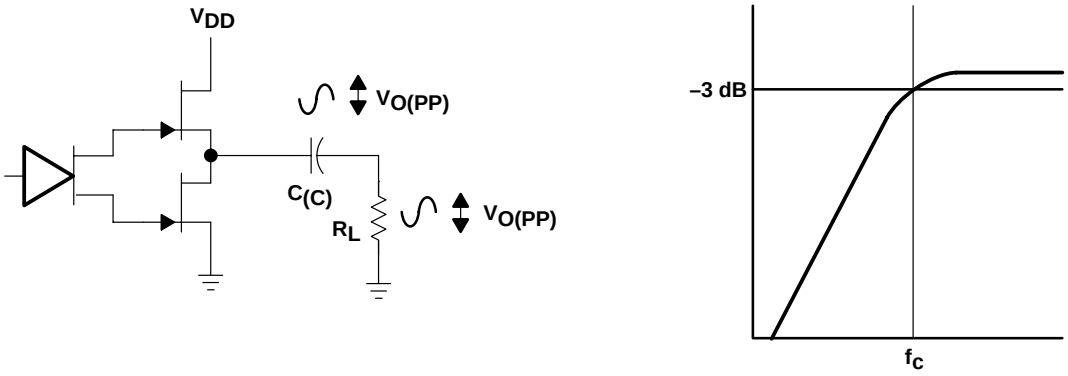


Figure 36. Single-Ended Configuration and Frequency Response

Increasing power to the load does carry a penalty of increased internal power dissipation. The increased dissipation is understandable considering that the BTL configuration produces 4× the output power of the SE configuration. Internal dissipation versus output power is discussed further in the *crest factor and thermal considerations* section.

single-ended operation

In SE mode (see Figure 36), the load is driven from the primary amplifier output for each channel (OUT+).

The amplifier switches single-ended operation when the SE/$\overline{\text{BTL}}$ terminal is held high. This puts the negative outputs in a high-impedance state, and effectively reduces the amplifier's gain by 6 dB.

BTL amplifier efficiency

Class-AB amplifiers are inefficient. The primary cause of these inefficiencies is voltage drop across the output stage transistors. There are two components of the internal voltage drop. One is the headroom or dc voltage drop that varies inversely to output power. The second component is due to the sinewave nature of the output. The total voltage drop can be calculated by subtracting the RMS value of the output voltage from V_{DD}. The internal voltage drop multiplied by the RMS value of the supply current (I_{DD}rms) determines the internal power dissipation of the amplifier.

An easy-to-use equation to calculate efficiency starts out as being equal to the ratio of power from the power supply to the power delivered to the load. To accurately calculate the RMS and average values of power in the load and in the amplifier, the current and voltage waveform shapes must first be understood (see Figure 37).

APPLICATION INFORMATION

BTL amplifier efficiency (continued)

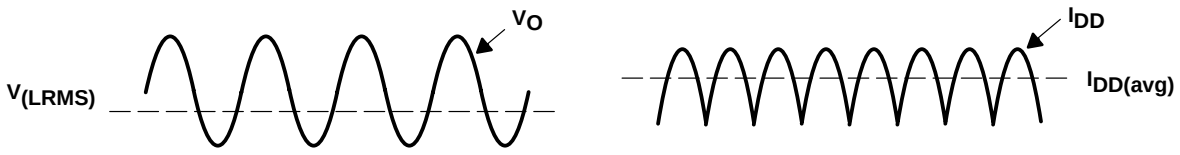


Figure 37. Voltage and Current Waveforms for BTL Amplifiers

Although the voltages and currents for SE and BTL are sinusoidal in the load, currents from the supply are very different between SE and BTL configurations. In an SE application the current waveform is a half-wave rectified shape, whereas in BTL it is a full-wave rectified waveform. This means RMS conversion factors are different. Keep in mind that for most of the waveform both the push and pull transistors are not on at the same time, which supports the fact that each amplifier in the BTL device only draws current from the supply for half the waveform. The following equations are the basis for calculating amplifier efficiency.

$$\text{Efficiency of a BTL amplifier} = \frac{P_L}{P_{SUP}} \tag{7}$$

Where:

$$P_L = \frac{V_L rms^2}{R_L}, \text{ and } V_{LRMS} = \frac{V_P}{\sqrt{2}}, \text{ therefore, } P_L = \frac{V_P^2}{2R_L}$$

$$\text{and } P_{SUP} = V_{DD}\, I_{DD}avg \quad \text{and} \quad I_{DD}avg = \frac{1}{\pi}\int_0^{\pi} \frac{V_P}{R_L} \sin(t)\, dt = \frac{1}{\pi} \times \frac{V_P}{R_L} [\cos(t)]_0^{\pi} = \frac{2V_P}{\pi R_L}$$

Therefore,

$$P_{SUP} = \frac{2\, V_{DD}\, V_P}{\pi\, R_L}$$

substituting P_L and P_{SUP} into equation 7,

$$\text{Efficiency of a BTL amplifier} = \frac{\frac{V_P^2}{2\, R_L}}{\frac{2\, V_{DD}\, V_P}{\pi\, R_L}} = \frac{\pi\, V_P}{4\, V_{DD}}$$

Where:

$$V_P = \sqrt{2\, P_L\, R_L}$$

Therefore,

$$\eta_{BTL} = \frac{\pi \sqrt{2\, P_L\, R_L}}{4\, V_{DD}} \tag{8}$$

P_L = Power delivered to load
P_{SUP} = Power drawn from power supply
V_{LRMS} = RMS voltage on BTL load
R_L = Load resistance
V_P = Peak voltage on BTL load
$I_{DD}avg$ = Average current drawn from the power supply
V_{DD} = Power supply voltage
η_{BTL} = Efficiency of a BTL amplifier

APPLICATION INFORMATION

BTL amplifier efficiency (continued)

Table 5 employs equation 8 to calculate efficiencies for four different output power levels. Note that the efficiency of the amplifier is quite low for lower power levels and rises sharply as power to the load is increased resulting in a nearly flat internal power dissipation over the normal operating range. Note that the internal dissipation at full output power is less than in the half power range. Calculating the efficiency for a specific system is the key to proper power supply design. For a stereo 1-W audio system with 8-Ω loads and a 5-V supply, the maximum draw on the power supply is almost 3.25 W.

Table 5. Efficiency vs Output Power in 5-V, 8-Ω BTL Systems

Output Power (W)	Efficiency (%)	Peak Voltage (V)	Internal Dissipation (W)
0.25	31.4	2.00	0.55
0.50	44.4	2.83	0.62
1.00	62.8	4.00	0.59
1.25	70.2	4.47†	0.53

† High peak voltages cause the THD to increase.

A final point to remember about Class-AB amplifiers (either SE or BTL) is how to manipulate the terms in the efficiency equation to utmost advantage when possible. Note that in equation 8, V_{DD} is in the denominator. This indicates that as V_{DD} goes down, efficiency goes up.

crest factor and thermal considerations

Class-AB power amplifiers dissipate a significant amount of heat in the package under normal operating conditions. A typical music CD requires 12 dB to 15 dB of dynamic range, or headroom above the average power output, to pass the loudest portions of the signal without distortion. In other words, music typically has a crest factor between 12 dB and 15 dB. When determining the optimal ambient operating temperature, the internal dissipated power at the average output power level must be used. From the TPA6011A4 data sheet, one can see that when the TPA6011A4 is operating from a 5-V supply into a 3-Ω speaker, that 4-W peaks are available. Use equation 9 to convert watts to dB.

$$P_{dB} = 10 \text{Log} \frac{P_W}{P_{ref}} = 10 \text{Log} \frac{4\text{ W}}{1\text{ W}} = 6\text{ dB} \quad (9)$$

Subtracting the headroom restriction to obtain the average listening level without distortion yields:

6 dB – 15 dB = –9 dB (15-dB crest factor)
6 dB – 12 dB = –6 dB (12-dB crest factor)
6 dB – 9 dB = –3 dB (9-dB crest factor)
6 dB – 6 dB = 0 dB (6-dB crest factor)
6 dB – 3 dB = 3 dB (3-dB crest factor)

APPLICATION INFORMATION

crest factor and thermal considerations (continued)

To convert dB back into watts use equation 10.

$$P_W = 10^{PdB/10} \times P_{ref} \quad (10)$$

= 63 mW (18-db crest factor)
= 125 mW (15-db crest factor)
= 250 mW (12-db crest factor)
= 500 mW (9-db crest factor)
= 1000 mW (6-db crest factor)
= 2000 mW (3-db crest factor)

This is valuable information to consider when attempting to estimate the heat dissipation requirements for the amplifier system. Comparing the worst case, which is 2 W of continuous power output with a 3-dB crest factor, against 12-dB and 15-dB applications significantly affects maximum ambient temperature ratings for the system. Using the power dissipation curves for a 5-V, 3-Ω system, the internal dissipation in the TPA6011A4 and maximum ambient temperatures is shown in Table 6.

Table 6. TPA6011A4 Power Rating, 5-V, 3-Ω Stereo

PEAK OUTPUT POWER (W)	AVERAGE OUTPUT POWER	POWER DISSIPATION (W/Channel)	MAXIMUM AMBIENT TEMPERATURE
4	2 W (3 dB)	1.7	–3°C
4	1 W (6 dB)	1.6	6°C
4	500 mW (9 dB)	1.4	24°C
4	250 mW (12 dB)	1.1	51°C
4	125 mW (15 dB)	0.8	78°C
4	63 mW (18 dB)	0.6	96°C

Table 7. TPA6011A4 Power Rating, 5-V, 8-Ω Stereo

PEAK OUTPUT POWER (W)	AVERAGE OUTPUT POWER	POWER DISSIPATION (W/Channel)	MAXIMUM AMBIENT TEMPERATURE
2.5	1250 mW (3-dB crest factor)	0.55	100°C
2.5	1000 mW (4-dB crest factor)	0.62	94°C
2.5	500 mW (7-dB crest factor)	0.59	97°C
2.5	250 mW (10-dB crest factor)	0.53	102°C

The maximum dissipated power ($P_{D(max)}$) is reached at a much lower output power level for an 8-Ω load than for a 3-Ω load. As a result, this simple formula for calculating $P_{D(max)}$ may be used for an 8-Ω application.

$$P_{D(max)} = \frac{2V_{DD}^2}{\pi^2 R_L} \quad (11)$$

However, in the case of a 3-Ω load, the $P_{D(max)}$ occurs at a point well above the normal operating power level. The amplifier may therefore be operated at a higher ambient temperature than required by the $P_{D(max)}$ formula for a 3-Ω load.

APPLICATION INFORMATION

crest factor and thermal considerations (continued)

The maximum ambient temperature depends on the heat-sinking ability of the PCB system. The derating factor for the PWP package is shown in the *dissipation rating table*. Use equation 12 to convert this to Θ_{JA}.

$$\Theta_{JA} = \frac{1}{\text{Derating Factor}} = \frac{1}{0.022} = 45^{\circ}\text{C/W} \quad (12)$$

To calculate maximum ambient temperatures, first consider that the numbers from the dissipation graphs are per channel, so the dissipated power needs to be doubled for two channel operation. Given Θ_{JA}, the maximum allowable junction temperature, and the total internal dissipation, the maximum ambient temperature can be calculated using equation 13. The maximum recommended junction temperature for the TPA6011A4 is 150°C. The internal dissipation figures are taken from the Power Dissipation vs Output Power graphs.

$$T_A \text{ Max} = T_J \text{ Max} - \Theta_{JA} P_D \quad (13)$$

$$= 150 - 45(0.6 \times 2) = 96^{\circ}\text{C (15-dB crest factor)}$$

NOTE:

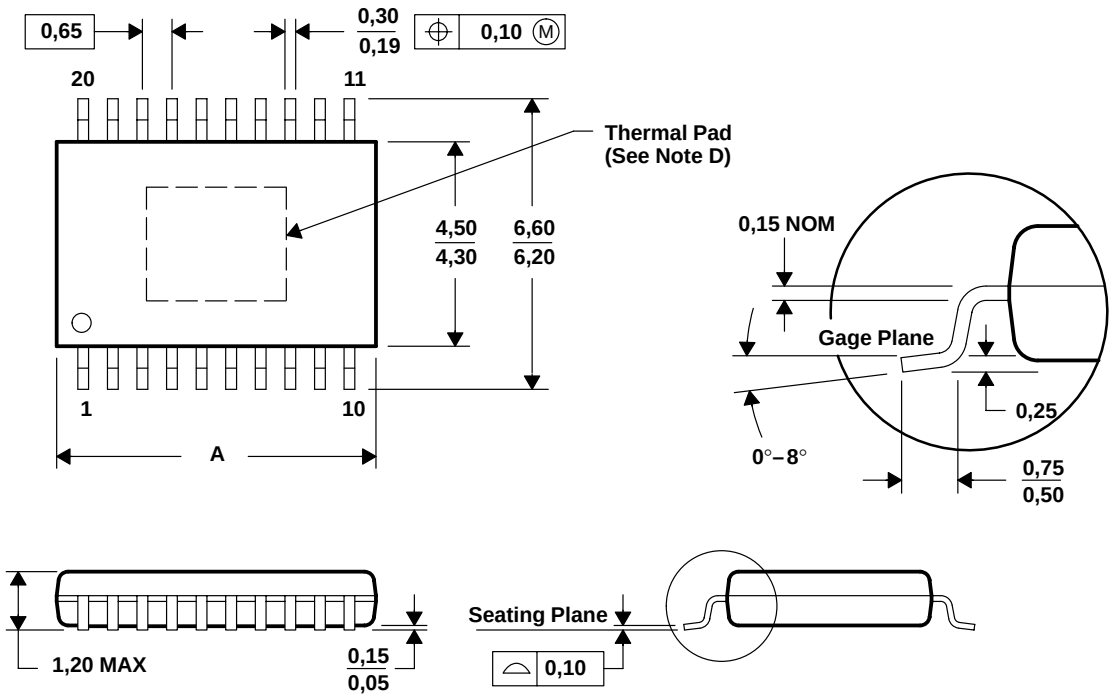
Internal dissipation of 0.6 W is estimated for a 2-W system with 15-dB crest factor per channel.

Tables 6 and 7 show that some applications require no airflow to keep junction temperatures in the specified range. The TPA6011A4 is designed with thermal protection that turns the device off when the junction temperature surpasses 150°C to prevent damage to the IC. Table 6 and 7 were calculated for maximum listening volume without distortion. When the output level is reduced the numbers in the table change significantly. Also, using 8-Ω speakers increases the thermal performance by increasing amplifier efficiency.

MECHANICAL DATA

PWP (R-PDSO-G)** **PowerPAD™ PLASTIC SMALL-OUTLINE**

20 PINS SHOWN



DIM \ PINS **	14	16	20	24	28
A MAX	5,10	5,10	6,60	7,90	9,80
A MIN	4,90	4,90	6,40	7,70	9,60

4073225/F 10/98

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions.
D. The package thermal performance may be enhanced by bonding the thermal pad to an external thermal plane. This pad is electrically and thermally connected to the backside of the die and possibly selected leads.
E. Falls within JEDEC MO-153

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Service Tools and Equipment

Application	Name
General	DVD testing disk
	General tools(screwdriver ect.)
	AV Cable
	DVD player
Special	Signal Generator
	Oscillograph
	Probe