AKAI

Multisystem LCD TV set

LTA-32N658HCP
LTA-32N680HCP
LTC-26N680HCP
LTC-32N680HCP

Service manual

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LCD COLOUR TV

SERVICE MANUAL

MODEL:

LTC-26N680HCP

LTC-32N680HCP

LTA-32N680HCP

LTA-32N658HCP

CHASSIS NO.: LS02/PS02

Please read this manual carefully before service.

Catalog

Chapter 1: Specifications and Composition

1. Models for LS02/PS02 chassis :

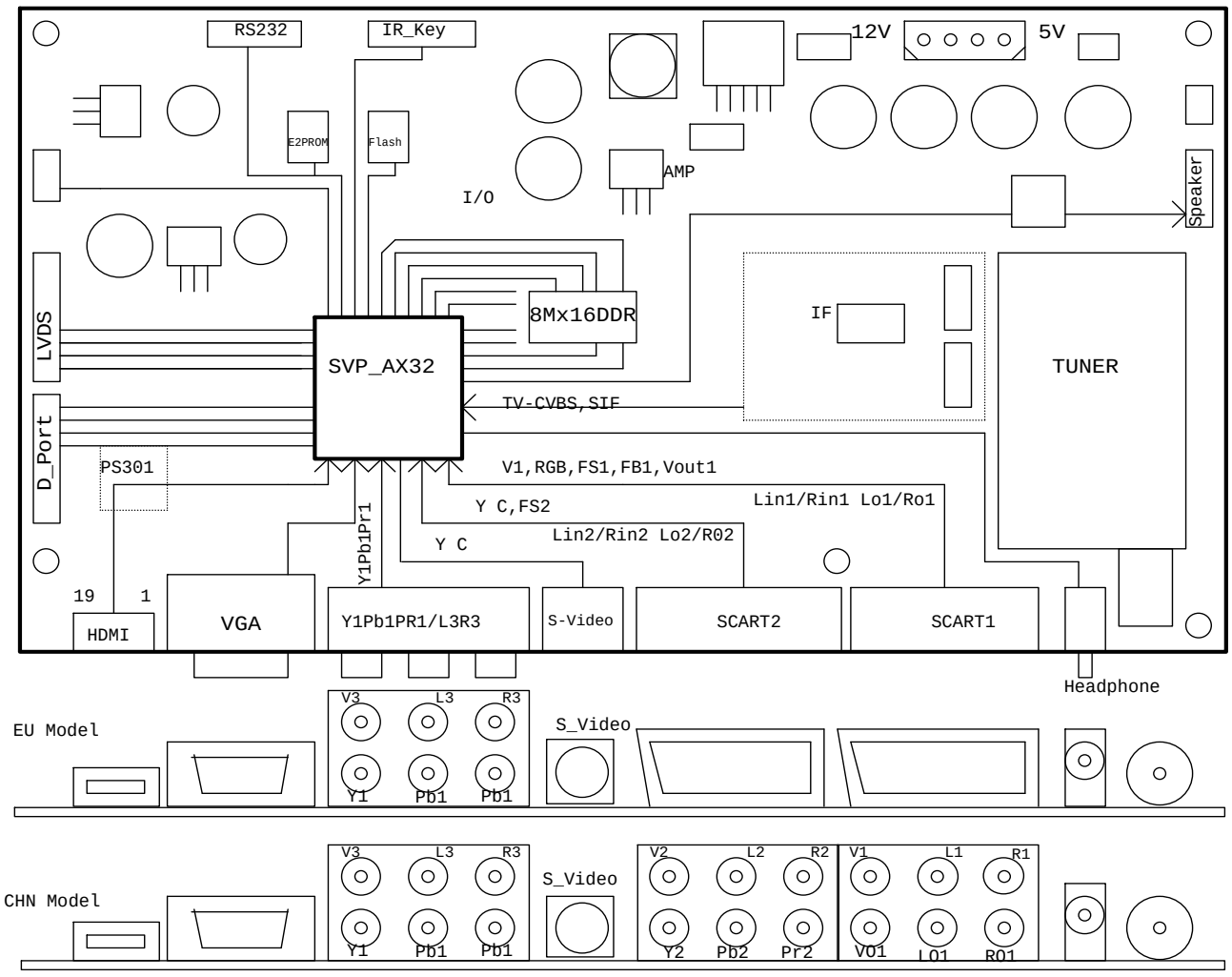
Region	Europe	America	Other regions
Original Models	LT26GHxxE LT37GHxxE LT32GHxxE LT42GHxxE LT47GHxxE xx:01,19,29,30,41 etc. PT32GHxxE PT42GHxxE PT50GHxxE xx:218,528,26,18,36	LT26GHxxU LT37GHxxU LT32GHxxU LT42GHxxU LT47GHxxU xx:01,19,29,30,41 etc. PT32GHxxU PT42GHxxU PT50GHxxU xx:218,528,26,18,36	LT26GHxxA LT37GHxxA LT32GHxxA LT42GHxxA LT47GHxxA xx:01,19,29,30,41 etc. PT32GHxxA T42GHxxA PT50GHxxA xx:218,528,26,18,36

2. Main Feature

Region		Europe	America	Other regions
RF signal	Color system	PAL、SECAM	NTSC、PAL M/ N	PAL、NTSC、SECAM
	Sound system	D/K、B/G、I、L/L'	M/N	D/K、B/G、I、M
Video or Y/C signal		PAL、NTSC、SECAM	PAL、NTSC、SECAM	PAL、NTSC、SECAM
Program presetting		100 （0-235）	181（AIR：2-69；CABLE：1-125）	236 （0-235）
Audio output（THD≤7%）		5W+5W	5W+5W	5W+5W
Power source		100V～240V	100V～240V	100V～240V
Teletxt		100 pages	X	100 pages
CCD		X	Yes	X
VCHIP		X	Yes	X
Sound demodulator		NICAM、IGR	BTSC	NICAM、IGR
SCART		Yes	X	X
VGA		Yes	Yes	Yes
YPbPr		Yes	Yes	Yes
HDMI		Yes	Yes	Yes
Earphone		Yes	Yes	Yes
OSD language		English, French, German, Italian, Portuguese etc.	English, French, Portuguese, Spanish etc.	English, French, German, Spanish etc.
Auto Off without Signal Reception		5 minutes		
Program booking		5 program booking. Turn to the corresponding program at the booking time.		
Swap		Customer could rearrange the channels according to personal habit		
Plug and Play		LCD TV could be used as computer screen, no need for the installation of software, which is Plug and Play in real sense		

3. Unit IC Compositions：

LCD TV with LS02/PS02 chassis is made up of switch power, system control circuit, video processing circuit, audio processing circuit, Power Amplifier circuit, AV input circuit, LCD screen module. Block circuit diagram is shown as below:


RS232
IR_Key
12V
5V
E2PROM
Flash
AMP
I/O
Speaker
LVDS
8Mx16DDR
IF
TUNER
SVP_AX32
TV-CVBS,SIF
D_Port
PS301
V1,RGB,FS1,FB1,Vout1
Y C,FS2
Lin1/Rin1 Lo1/Ro1
Y1Pb1Pr1
Y C
Lin2/Rin2 Lo2/R02
19
1
HDMI
VGA
Y1Pb1PR1/L3R3
S-Video
SCART2
SCART1
Headphone
EU Model
V3
L3
R3
S_Video
Y1
Pb1
Pb1
CHN Model
V3
L3
R3
S_Video
V2
L2
R2
V1
L1
R1
Y1
Pb1
Pb1
Y2
Pb2
Pr2
VO1
LO1
RO1

4. Introduction of PCB module

LCD TV with LS02/PS02 Chassis is made up of power board, side AV board, remote control reception board, key board, and mainboard. The table below is the introduction of the function of all printed board modules.

No.	Parts	Description
1	Mainboard module	Mainboard module is the core of LCD TV signal processing. Under the control of the system control circuit, It undertakes the task of converting the external input signal into the unified digital signal that the LCD screen could identify. Mainboard controls the whole machine through IIC bus, decode VIDEO signal, controls the Video (brightness, contrast, chroma, hue, definition etc), white balance adjusts, generates OSD, de-interlaces signal, converts signal frequency, and finishes signal A/D and D/A conversion, video enhancement, LVDS signal coding and output; it has Scart , S-Video, AV , YPbPr, HDMI and PC interface, Tuner input, sound demodulation, sound processing, sound power amplifier, and online update.
2	Remote reception module	The remote reception board module is constituted by an indicator-light and a remote reception. Customer could manipulate the LCD TV by using remote controller very conveniently. By the color of the indicator light, the operation mode of the LCD TV could be judged (red is standby, green is power on).
3	Built-in power board module	Convert the 100V～240V （50/60HZ）AC into DC, output have +12V, +5V, +3.3V and the +5V_STB in standby state.
4	Keyboard module	Keyboard module has 7 function keys (program +/-, volume +/-, AV/TV, menu ,power), customer could use the key to operate the TV freely.
5	LCD screen module	LCD screen has built-in inverter that convert DC into high voltage AC signal to turn on the backlight CCFL (Cold Cathode Fluorescent Light); the LCD screen process the video signal from signal board and reappear.
6	Side AV board	Side AV board is used for earphone output.

Chapter 2: Function Introduction of Main IC

1. Main ICs and functional modules of LS02/PS02 chassis

No.	Item no.	Model	Main function
1	U8	AFT7/W003 AFT7/W103 AFT7/W300	Tuner,output sound IF and video signal
2	U1	SVP-AX32LF/SVP-AX68LF	SVP AX family video processors provide the highest performance, target the converging HDTV-ready and PC-ready LCD TV, PDP TV applications where high precession processing of video, which Embed in ADC converter、 3D comb filter、HDMI processor、video decoder、LVDS transmitter etc.
3	U3	AT24C64-SO8-DNS	EEPROM
4	U5	W25X80-VSSIG	8M-bit Serial Flash, Store the Control program.
5	U7	HY5DU281622FTP-4	8M×16bits DDR SDRAM
6	U9	TDA9886T	Multistandard alignment-free IF-PLL demodulators
7	U11	74HC4052	Audio signal switch of AV terminal
8	U15	74LVC14A	VGA line and field synchronizing signal waveform shaping
9	U16	AT24C64	EEPROM
10	U17	IRF7404/AO4459	Field Effect Transistor
11	U22	MP1411DH	DC-DC converter
12	U20、U24	AP1117E33	LDO,5V to 3.3V DC converter
13	U23	AP1122EL	LDO,5V to 1.2V DC converter
14	U27	TDA7266SA	Audio amplifier (BTL output)
15	U32	PS201	HDMI two-to-one switch

2. Function introduction of ICs or functional module of LCD TV with LS02/PS02 chassis

1. Tuner (Asian TV:AFT7/W003;European TV: AFT7/W103;American TV: AFT7/W300)

No.	Terminal name	Description
1	AGC	AGC voltage supply
2	NC	No Connected
3	SAS	Address Selection Line
4	SCL	Serial Clock Line
5	SDA	Serial Data Line
6	NC	No Connected

7	BP	+B For PLL & Mixer
8	ADC/NC	ADC Input/ No Connected
9	NC	No Connected
10	NC	No Connected
11	IF1	IF Output
12	ANT	VHF/UHF Signal Input

2. Video processing IC SVP-AX32LF/SVP-AX68LF

The SVP^{TM}CX video processor is a highly integrated system-on-a-chip device, targeting the converging HDTV-ready and PC-ready LCD TV, PDP TV applications where high precision processing of video and data are the requirements. SVPTMCX contains 6th generation dual-purposed triple 10-bit high-precision and high speed video ADCs for both PC and video inputs, the high-performance multi-format 3D digital comb video decoder that supports NTSC, PAL, and SECAM*, a HDTV sync separator, motion adaptive de-interlacing engine, and the video format conversion engine, supporting multi-window display in many different output modes. Trident's DCRe^{TM} – Digital Cinema Reality engine, is integrated inside the SVPTMCX family to provide the most natural cinema-realistic images. The DCRe^{TM} technology integrates advanced 3D-comb video decoding, advanced motion adaptive de-interlacing, object-based digital noise reduction, advanced 7th generation scaler, film mode support, average picture level (APL), edge smoothing and dynamic sharpness enhancement. Trident's patented Unified Memory Architecture (UMA) that allows frame rate conversion, 3D comb video decoding, and video enhancement processing to share the same memory buffer that is made up of high-speed and cost-effective PC graphic memory. All these advanced digital processing techniques combined with a true 10-bit video data processing for the most optimal video fidelity to provide the most natural and cinema quality video images. Designed for maximum system design flexibility, SVPTMCX integrates all video interfaces to support converging digital video, analog video, and PC data applications. The users of Trident's single chip SVP™CX series video processor(s) will benefit from many features while maintaining a price competitive advantage over the existing solution(s)

Main features:

- ●Integrated 7th Generation Motion and Edge Adaptive De-interlacing
- ● Integrated ADC
- ● PC auto tune
- ●Built-in 8-bit LVDS Transmitter
- ●Advanced 7th generation cubic-4 image scaling engine
- ● Advanced Chroma Processing and Dynamic Contrast Function
- ● Green color stretch, blue color stretch, skin color enhancement
- ●Integrated 7th Generation Motion Adaptive 3D Digital Comb Video Decoder with Programmable Filter
- ●60Hz～100Hz interlaced scanning and 50Hz～75Hz progressive scanning
- ● frame rate conversion
- ● 14D： dynamic picture enhancements
- ● Advanced Film Mode Recovery-3:2/2:2 pull down
- ● Build-in A/D conversion function

- Teletext function
- Supports 16bits DDR memory interface
- Multi-screen display mode
- OSD and VBI/Closed caption and advanced OSD engine

Pin function description:

Table1: Pin Assignments for CPU-related and GPIO pins

Name	Type	Pin No.	Pin Description	Power Supply
SCL	I	154	I2C slave SCL, serial clock;	VDDC/ VDDH
SDA	I/O	153	Shared I2C slave SDA serial data: ○ SVP video engine I2C slave ○ embedded 8051CPU peripheral I2C slave **Bootstrap pin "TUNE2" is used for I2C slave device ID:** SVP video engine I2C slave: ○ **if pull-up, I2C device ID is 0x7E/7F;** ○ **if pull-down, I2C device ID is 0x7C/7D;** Embedded 8051CPU peripheral I2C slave: ○ **if pull-up, I2C device ID is 0x6A/6B;** ○ **if pull-down, I2C device ID is 0x62/63;**	VDDC/ VDDH
SPI_SI	O	171	Serial data output to SI pin of SPI flash memory	VSB12/ VSB33
SPI_SO	I	172	Serial data input from SO pin of SPI flash memory	VSB12/ VSB33
SPI_SCK	O	173	Serial clock to SCK pin of SPI flash memory	VSB12/ VSB33
SPI_CEN	O	174	Chip enable (active low) to CE# pin of SPI flash memory	VSB12/ VSB33
RXD0	I/O	155	○ UART0 RXD ○ Port P30	VDDC/ VDDH
TXD0	I/O	156	○ UART0 TXD	VDDC/

Name	Type	Pin No.	Pin Description	Power Supply
			○ Port P31	VDDH
IRIN	I/O	175	○ InfraRed input ○ Port P32 ○ Interrupt IE0#	VSB12/ VSB33
POWERLOW	I/O	176	○ Power voltage down detection monitor input ○ Port P33 ○ Interrupt IE1#	VSB12/ VSB33
PSYNC	I/O	157	○ Port P34 HSYNC output from display engine; VSYNC output from display engine; DE output from display engine; DSS1_VSYNC output; DSS1_HSYNC output;	VDDC/ VDDH
PWM2	I/O	168	○ PWM2 ○ port P35 HSYNC output from display engine; VSYNC output from display engine; DSS1_VSYNC output; DSS1_HSYNC output; FIELD output from display engine; HDMI_MUTE from HDMI audio;	VDDC/ VDDH
PPWR	I/O	177	○ Panel power on sequence control ○ Port P36*	VSB12/ VSB33
PDOWN	I/O	182	○ Power switch control output ○ Port P37* ○ Input as external trigger of timer 2	VSB12/ VSB33
RXD1	I/O	158	○ UART1 RXD ○ Port P20	VDDC/ VDDH
TXD1	I/O	159	○ UART1 TXD ○ Port P21	VDDC/ VDDH
MSCL	I/O	160	○ I2C master (software) SCL ○ Port P22;	VDDC/ VDDH
MSDA	I/O	161	○ I2C master (software) SDA ○ Port P23	VDDC/ VDDH
TUNE0	I/O	89	○ Tune0 ○ Port P24	VDDC/ VDDH
TUNE1	I/O	90	○ Tune1 ○ Port P25	VDDC/ VDDH
TUNE2	O (output only)	91	○ **Bootstrap pin for I2C slave device ID** SVP video engine I2C slave: ○ **if pull-up, I2C device ID is 0x7E/7F;** ○ **if pull-down, I2C device ID is 0x7C/7D;** Embedded 8051CPU peripheral I2C slave: ○ **if pull-up, I2C device ID is 0x6A/6B;** ○ **if pull-down, I2C device ID is 0x62/63;** ○ **Tune2** ○ **Port P26(output only)** HSYNC output from display engine; VSYNC output from display engine; DSS1_VSYNC output; DSS1_HSYNC output;	VDDC/ VDDH

Name	Type	Pin No.	Pin Description	Power Supply
			FIELD output from display engine; DE output from display engine; HDMI_MUTE from HDMI audio;	
MUTE	I/O	92	o Mute output for audio control, o Port P27	VDDC/ VDDH
KEY	I/O; AI	183	o Analog Key input, low speed ADC input AN0 o Port P10	VSB12/ VSB33
SENSOR1	I/O; AI	184	o Analog power sensor, low speed ADC input AN1; o Port P11	VSB12/ VSB33
SENSOR2	I/O; AI	185	o Environment light sensor, low speed ADC input AN2 o Port P12	VSB12/ VSB33
FS3	I/O; AI	186	o Function select3, low speed ADC input AN3 o Port P13	VSB12/ VSB33
FS4	I/O; AI	187	o Function select4, low speed ADC input AN4 o Port P14	VSB12/ VSB33
AFT	I/O; AI	188	o Tuner AFC, low speed ADC input AN5 o Port P15 o Interrupt IE2#	VSB12/ VSB33
PWM0	I/O; AI	189	o PWM0 o Port P16 o Interrupt IE3# o low speed ADC input AN6	VSB12/ VSB33
PWM1	I/O; AI	190	o PWM1 o Port P17 o Interrupt IE4# o low speed ADC input AN7	VSB12/ VSB33
GPIO00	I/O	88	o Port P00 o Interrupt IE5# o Input / output for I2S AUD_SCK optionally	VDDC/ VDDH
GPIO01	I/O	163	o JTAG_TCK to SVP-AX (power on default as input) o Port P01 o I2S input / output master Clock o SPDIF master clock input / output	VDDC/ VDDH
GPIO02	I/O	165	o JTAG_TMS to SVP-AX, (power on default as input); o Port P02 o I2S input / output SCK;	VDDC/ VDDH
GPIO03	I/O	166	o JTAG_TDI to SVP-AX, power on default as input; o Port P03 o I2S input / output SD o SPDIF data input / output	VDDC/ VDDH
GPIO04	I/O	164	o JTAG_TDO from SVP-AX, (power on default as output) o Port P04 o I2S input / output WS	VDDC/ VDDH
TPWM	I/O	167	Tuning pulse width modulator. High resolution (18 bit) PWM / PFM output, used for VST (voltage synthesis tuning) application, such as panel backlight control; o HSYNC output from display engine; o VSYNC output from display engine;	VDDC/ VDDH

Table2 Pin Assignments for Analog Support Interface

Name	Type	Pin No.	Pin Description	Power supply
XTALI	AI	194	Input for Clock Synthesizer. Supports 24.576 MHz Oscillator or crystal powered by analog PLL	PAVDD1 and VSB12 (left bar)
XTALO	AI/O	195	Used in conjunction with XTALI for 24.576 MHz crystal output powered by analog PLL	PAVDD1 and VSB12 (left bar)
MLF1	AI	197	Low pass filter node for memory clock PLL powered by analog PLL	PAVDD1 and VSB12 (left bar)
PLF2	AI	200	Low pass filter node for video clock PLL powered by analog PLL	PAVDD2 and VSB12 (left bar)

Table3 Pin Assignments for Analog Input Interface

Name	Type	Pin No.	Pin Description
CVBS	AI	52	Composite video input
Y_G1	AI	33	Y input 1 of component or G input 1 of RGB
Y_G2	AI	36	Y input 2 of Component or G input 2 of RGB
Y_G3	AI	42	Y input 3 of component or G input 3 of RGB
CVBS_OUT1	AO	61	CVBS Output 1
CVBS_OUT2	AO	60	CVBS Output 2
C	AI	45	C input of S-Video
PB_B1	AI	34	PB Input 1 of component or B input 1 of RGB
PB_B2	AI	37	PB Input 2 of component or B input 2 of RGB
PB_B3	AI	43	PB Input 3 of component or B input 3 of RGB
PR_R1	AI	35	PR Input 1 of component or R input 1 of RGB
PR_R2	AI	38	PR Input 2 of component or R input 2 of RGB
PR_R3	AI	44	PR Input 3 of component or R input 3 of RGB
FS1	AI	55	SCART Function select1
FS2	AI	54	SCART Function select2
FB1	AI	57	SCART FB input for Port 1
FB2	AI	56	SCART FB input for Port 2
PC_G	AI	29	Analog input for PC: G
PC_B	AI	28	Analog input for PC: B
PC_R	AI	30	Analog input for PC: R
AIN_HS	I	26	Hsync Input (PC RGB Input)
AIN_VS	I	27	Vsync Input (PC RGB Input)

Table4 Pin Assignments for Capture Interface (TV&RGB)

Name	Type	Pin No.	Pin Description	Power Supply
DP[15:0]	I/O	234, 235, 236, 237, 238, 239, 240, 241, 247, 248, 249, 250, 251, 252, 253, 254	Digital Input port [15:0], used as 16-bit CCIR601 digital input Digital input port [15:6], used as 10/8-bit CCIR656 digital input DP[6]: XRAM address mapped (SVP_GPIO3, input and output) DP[5]: XRAM address mapped (SVP_GPIO2, output only) DP[4]: XRAM address mapped (SVP_GPIO1, output only) HSYNC output from display engine; VSYNC output from display engine; DP[3]: XRAM address mapped (SVP_GPIO4, input and output)	VDDC/ VDDH

Name	Type	Pin No.	Pin Description	Power Supply
			HSYNC output from display engine; VSYNC output from display engine; DP[1]: HSYNC output from display engine; VSYNC output from display engine; DP[0]: HSYNC output from display engine; VSYNC output from display engine;	
DP_CLK	I/O	242	o Digital port CLK input o Pixel clock output	VDDC/ VDDH
DP_VS	I/O	256	o Vsync Input of Digital Port o VSYNC output from display engine o DSS1_VSYNC output	VDDC/ VDDH
DP_HS	I/O	255	o Hsync Input of Digital Port o HSYNC output from display engine o DSS1_HSYNC output	VDDC/ VDDH

Table5 Pin Assignments for Frame Buffer Memory

Name	Type	Pin No.	Pin Description	Power supply
MD[15~0]	I/O	127, 126, 124, 123, 121, 120, 118, 117, 106, 105, 103, 102, 99, 98, 96, 95	Memory Data	VDDC/VDDM
MA[11~0]	I/O	132, 146, 133, 134, 135, 136, 137, 138, 150, 149, 148, 147	Memory Address	VDDC/VDDM
RASN	O	141	RAS#	VDDC/VDDM
CASN	O	140	CAS#	VDDC/VDDM
WEN	O	139	WE#, write enable	VDDC/VDDM
MCK0P	O	130	Memory Clock +	VDDC/VDDM
MCK0N	O	129	Memory Clock -	VDDC/VDDM
DQM[1~0]	O	111, 109	Read/write bytes enable	VDDC/VDDM
CLKE	O	131	Memory Clock Enable	VDDC/VDDM
DQS[1~0]	IO	115	Memory Data Strobe	VDDC/VDDM
MVREF	PWR	108	DDR Voltage Reference	VDDC/VDDM
BA0	O	144	Bank Address Select	VDDC/VDDM
BA1	O	145	Bank Address Select	VDDC/VDDM

Table6 Miscellaneous Pin Assignments

Name	Type	Pin No.	Pin Description	Power Supply
RESET	I	178	System reset active high, with Schmitt Trigger. RESET forces the chip to a known state.	VSB12/VSB33
TESTMODE	I	179	Reserved (Connected to GND)	VSB12/VSB33

Table7 LVDS Output Pin Assignments

Name	Type	Pin No.	Pin Description
TA1P	AO	226	LVDS 1st channel Differential positive data out
TA1M	AO	227	LVDS 1st channel Differential negative data out
TB1P	AO	224	LVDS 1st channel Differential positive data out
TB1M	AO	225	LVDS 1st channel Differential negative data out
TC1P	AO	222	LVDS 1st channel Differential positive data out
TC1M	AO	223	LVDS 1st channel Differential negative data out
TD1P	AO	218	LVDS 1st channel Differential positive data out
TD1M	AO	219	LVDS 1st channel Differential negative data out
TCLK1P	AO	220	LVDS 1st channel Differential positive CLK out
TCLK1M	AO	221	LVDS 1st channel Differential negative CLK out
TA2P	AO	212	LVDS 2nd channel Differential positive data out
TA2M	AO	213	LVDS 2nd channel Differential negative data out
TB2P	AO	210	LVDS 2nd channel Differential positive data out
TB2M	AO	211	LVDS 2nd channel Differential negative data out
TC2P	AO	208	LVDS 2nd channel Differential positive data out
TC2M	AO	209	LVDS 2nd channel Differential negative data out
TD2P	AO	204	LVDS 2nd channel Differential positive data out
TD2M	AO	205	LVDS 2nd channel Differential negative data out
TCLK2P	AO	206	LVDS 2nd channel Differential positive CLK out
TCLK2M	AO	207	LVDS 2nd channel Differential negative CLK out

Table8 HDMI Interface Pin Assignments

Name	Type	Pin No.	Pin Description
PVCC	PWR	2	TMDS PLL Supply Voltage
AVCC	PWR	3, 7, 11, 15	TMDS Analog Supply Voltage
RXC-	AO	4	HDMI Differential CLK-
RXC+	AO	5	HDMI Differential CLK+
TMDS_GND	PWR	1	TMDS GND
RX0-	AI	8	HDMI Differential Input Pair 0-
RX0+	AI	9	HDMI Differential Input Pair 0+
RX1-	AI	12	HDMI Differential Input Pair 1-
RX1+	AI	13	HDMI Differential Input Pair 1+
RX2-	AI	16	HDMI Differential Input Pair 2-
RX2+	AI	17	HDMI Differential Input Pair 2+
AVDD33_Audio	PWR	25	ACR PLL Regulator Supply Voltage
AVSS33_Audio	GND	24	ACR PLL GND
PWR5V	I	21	TMDS Port Transmitter Detect (5V tolerance)
DSCL	I	19	DDC I2C Clock for DDC (5V Tolerance)
DSDA	I/O	20	DDC I2C Data for DDC (5V tolerance)

Table9 Analog Audio Input/Output Interface Pin Assignments

Name	Type	Pin No.	Pin Description
SIFP	AI	50	SIF Audio Input
SIFN	AI	51	Reference ground for SIF audio input
AL1	AI	73	Audio line input left channel 1
AR1	AI	74	Audio line input right channel 1
AL2	AI	75	Audio line input left channel 2
AR2	AI	76	Audio line input right channel 2
AL3	AI	77	Audio line input left channel 3
AR3	AI	78	Audio line input right channel 3
AL4	AI	79	Audio line input left channel 4
AR4	AI	80	Audio line input right channel 4
AOL1	AO	81	SCART Audio Output left channel 1
AOR1	AO	82	SCART Audio Output right channel 1
HPHOL	AO	63	○ Headphone output left channel ○ SCART audio output left channel 2
HPHOR	AO	64	○ Headphone output right channel ○ SCART audio output right channel 2
SPKOL	AO	66	Main Audio/Speaker output left channel
SPKOR	AO	67	Main Audio/Speaker output right channel
VREFP	AI	71	Input Analog reference voltage positive. Intended for 3.3V
VREFN	AI	69	Input Analog reference voltage negative. Intended for system analog ground.
VCM	AO	70	Output Analog common-mode voltage
VCC33A	PWR	72	Power for main analog, 3.3V
GND33A	GND	68	Ground for main analog
VCC33A_HP	PWR	62	Power for head phone amplifier, 3.3V
GND33A_HP	GND	65	Ground for head phone amplifier, 3.3V

Table10 Digital Audio Interface Pin Assignments

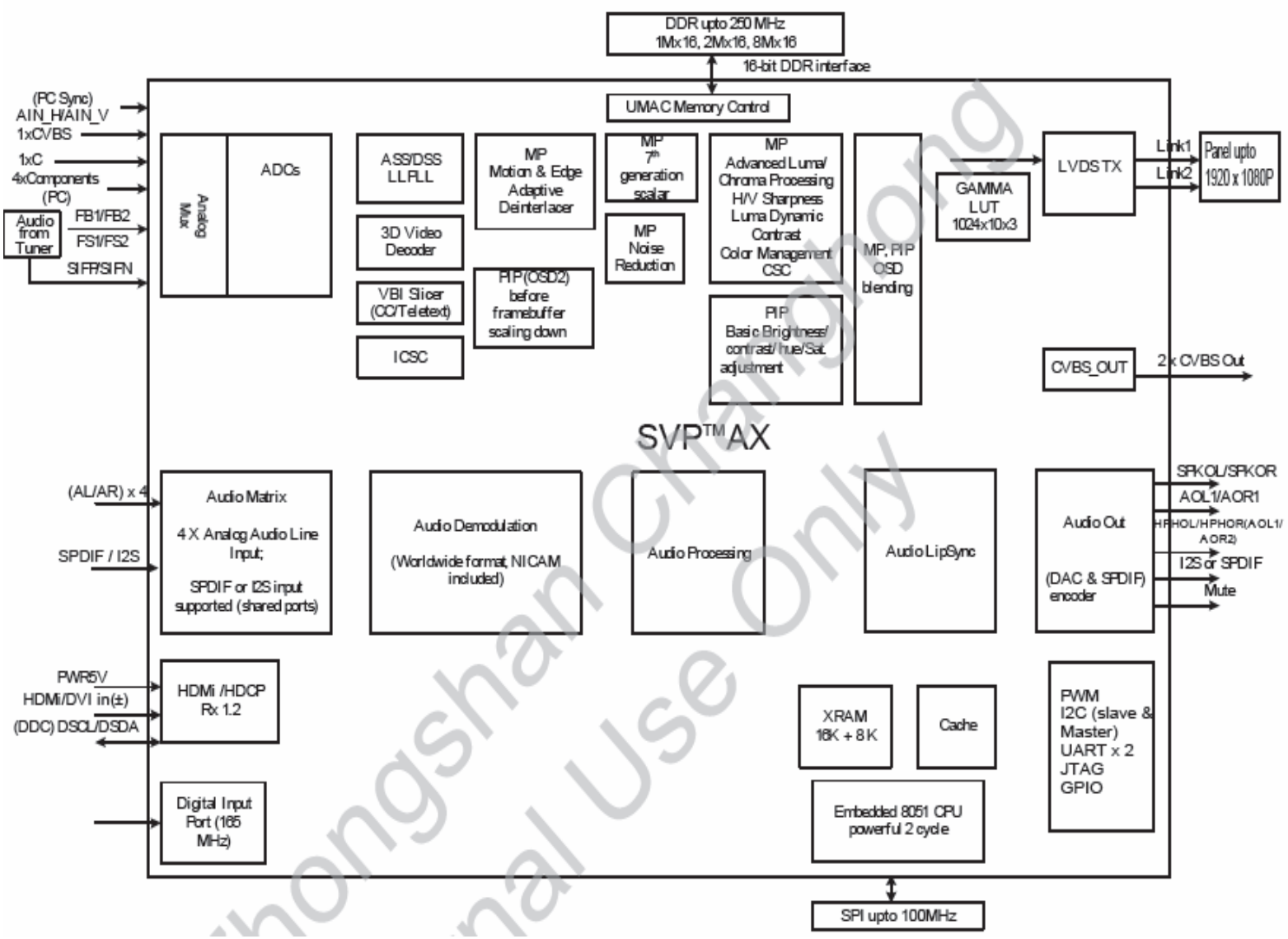
Name	Type	Pin No.	Pin Description	Power supply
AUD_MCLK	I/O	85	○ I2S audio input/output master clock ○ SPDIF master clock input / output ○ XRAM address mapped (SVP_GPIO3, output only)	VDDC / VDDH
AUD_SD	I/O	86	○ I2S audio input/output data ○ SPDIF data input/output ○ XRAM address mapped (SVP_GPIO2, input/output)	VDDC / VDDH
AUD_WS	I/O	87	○ I2S audio input/output word select ○ XRAM address mapped (SVP_GPIO1, input/output)	VDDC / VDDH

Table11 Pin Assignments for Power and Ground

Name	Type	Pin No.	Pin Description
VSB12 (top bar)	PWR	192	1.2V, Standby power for core
VSB12_PLL (left bar)	PWR	193	1.2V, Standby power for KMNPLL 1.2v
VSB33	PWR	180	3.3V, Standby power for I/O
PAVDD1	PWR	198	Standby Power for analog PLL MCLK (3.3 V)

Name	Type	Pin No.	Pin Description
PAVSS1	GND	196	Ground for analog PLL
PAVSS2	GND	199	Ground for analog PLL
PAVDD2	PWR	201	Standby Power for analog PLL PCLK (3.3 V)
VDDC	PWR	23, 83, 100, 122, 151, 169, 233, 244	1.2V Digital Core Power
VDDH	PWR	93, 162, 246	3.3V Digital I/O Power
VSSR	GND	112	Digital Ground
VDDR	PWR	114	Digital Power for Memory
VDDM	PWR	116	DDR memory Interface Power
AVSS3_BG_ASS	GND	58	ADC Ground
AVDD3_BG_ASS	PWR	59	ADC Power
PAVDD1, 2	PWR	198, 201	Power for ANAPLL/APLL/LLPLL, 1.2V
PAVSS1, 2	GND	196, 199	Ground for ANAPLL/APLL/LLPLL
AVDD_ADC4, 3, 2, 1	PWR	47, 32, 40, 49	Power for analog ADC (1.2 V)
AVSS_ADC1 and AVSS_ADC234	GND	48, 31, 39, 46	Ground for analog ADC1 and ADC234
AVDD3_ADC1, 2		53, 41	Power for analog ADC (3.3 V)
LVDS_VDDO	PWR	202, 217, 228	LVDS Output Buffer VDD, 3.3 V
LVDS_VSSO	GND	203, 214, 229	LVDS Output Buffer GND
LVDS_VDDP	PWR	216	LVDS PLL VDD, 1.2 V
LVDS_VSSP	GND	215	LVDS PLL GND

SVP-CX32LF/ SVP-CX68LF internal block diagram:



3. AT24C64-SO8-DNS brief introduction:

The AT24C64A provides 65,536 bits of serial electrically erasable and programmable read only memory (EEPROM) organized as 8192 words of 8 bits each. The device's cascadable feature allows up to 8 devices to share a common two-wire bus. The device is optimized for use in many industrial and commercial applications where low power and low voltage operation are essential. The AT24C64A is available in space saving 8-lead JEDEC PDIP, 8-lead JEDEC SOIC, 8-lead EIAJ SOIC, 8-lead MAP and 8-lead TSSOP packages and is accessed via a 2-wire serial interface. In addition, the entire family is available in 2.7V (2.7V to 5.5V) and 1.8V (1.8V to 5.5V) versions.

Main features:

• Low-Voltage and Standard-Voltage Operation

– 2.7 (VCC = 2.7V to 5.5V)

– 1.8 (VCC = 1.8V to 5.5V)

• Low-Power Devices (ISB = 6μA @ 5.5V) Available

• Internally Organized 4096 x 8, 8192 x 8

• Two-wire Serial Interface

• Schmitt Trigger, Filtered Inputs for Noise Suppression

• Bidirectional Data Transfer Protocol

• 100 kHz (1.8V) and 400 kHz (2.5V) Clock Rate for AT24C32A

• 400 kHz (1.8V) Clock Rate for AT24C64A

• Write Protect Pin for Hardware Data Protection

• 32-byte Page Write Mode (Partial Page Writes Allowed)

• Self-timed Write Cycle (5 ms Max)

• High Reliability

– Endurance: 1 Million Write Cycles

– Data Retention: 100 Years

• Automotive Grade, Extended Temperature and Lead-free/Halogen-free Devices Available

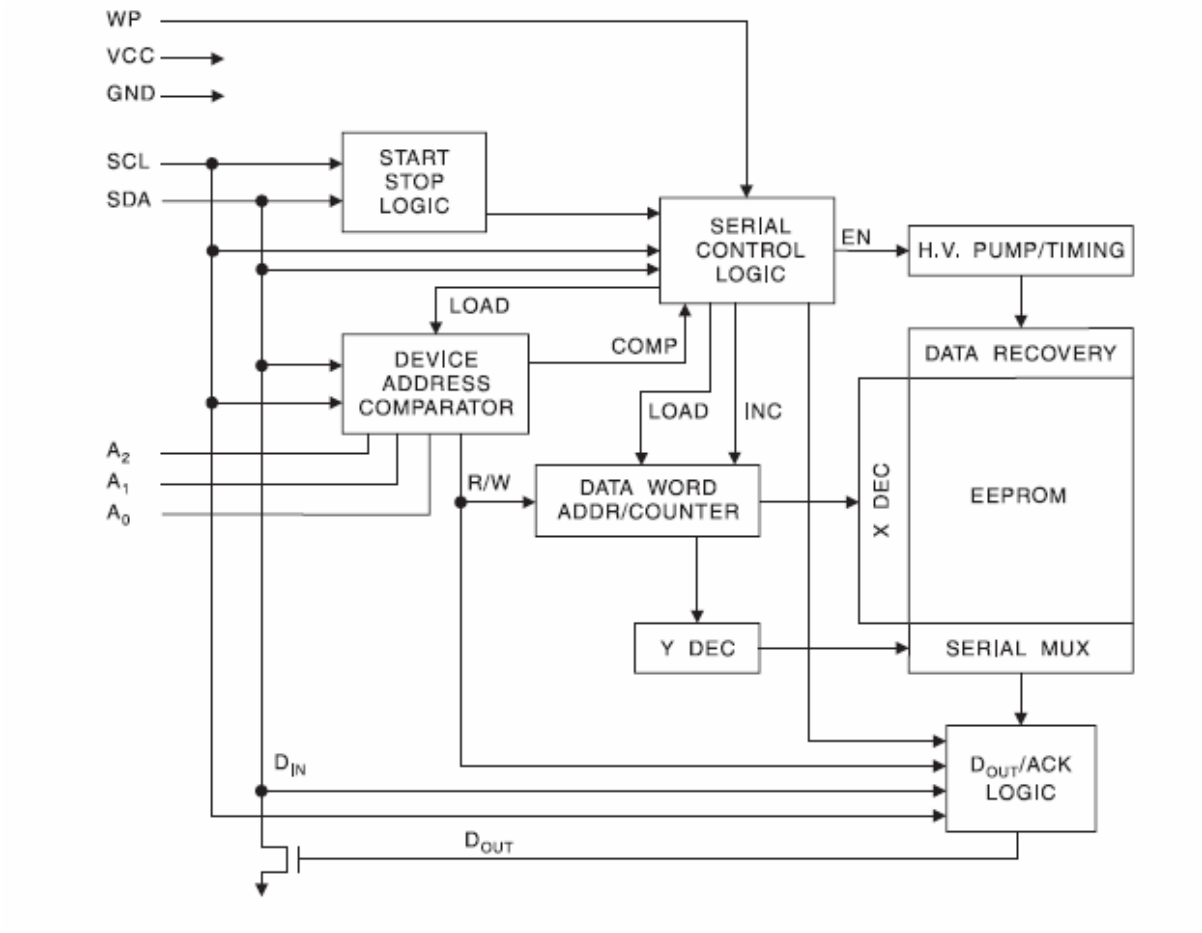
• 8-lead JEDEC PDIP, 8-lead JEDEC SOIC, 8-lead EIAJ SOIC, 8-lead MAP and 8-lead TSSOP Packages

• Die Sales: Wafer Form, Waffle Pack, and Bumped Wafers

Pin Configuration

Pin NO.	Pin Name	Function
1-3	A0 – A2	Address Inputs
4	GND	Ground
5	SDA	Serial Data
6	SCL	Serial Clock Input
7	WP	Write Protect
8	VCC	Power Supply

AT24C64-SO8-DNS internal functional block diagram：



4．W25X80-VSSIG brief introduction

W25X80-VSSIG main features:

■Family of Serial Flash Memories

● 8M-bit/1M-byte(1,048,576)

● 256-bytes per programmable page

● Uniform 4K-byte Sectors/64K-byte Blocks

■ SPI with Single or Dual Outputs

● Clock ,Chip Select, Data I/O, Data Out

● Optional Hold function for SPI flexibility

■ Data Transfer up to 150M-bits/second

- Clock operation to 75MHz
- Fast Read Dual Out instruction
- Auto-increment Read capability

■ Flexible Architecture with 4KB sectors

- Sector Erase(4K-bytes)
- Block Erase(64K-byte)
- Page program up to 256 bytes<2ms

■ Low Power Consumption, Wide Temperature Range

- Single 2.7 to 3.6V supply
- 5mA active current,1uA Power-down (typ)

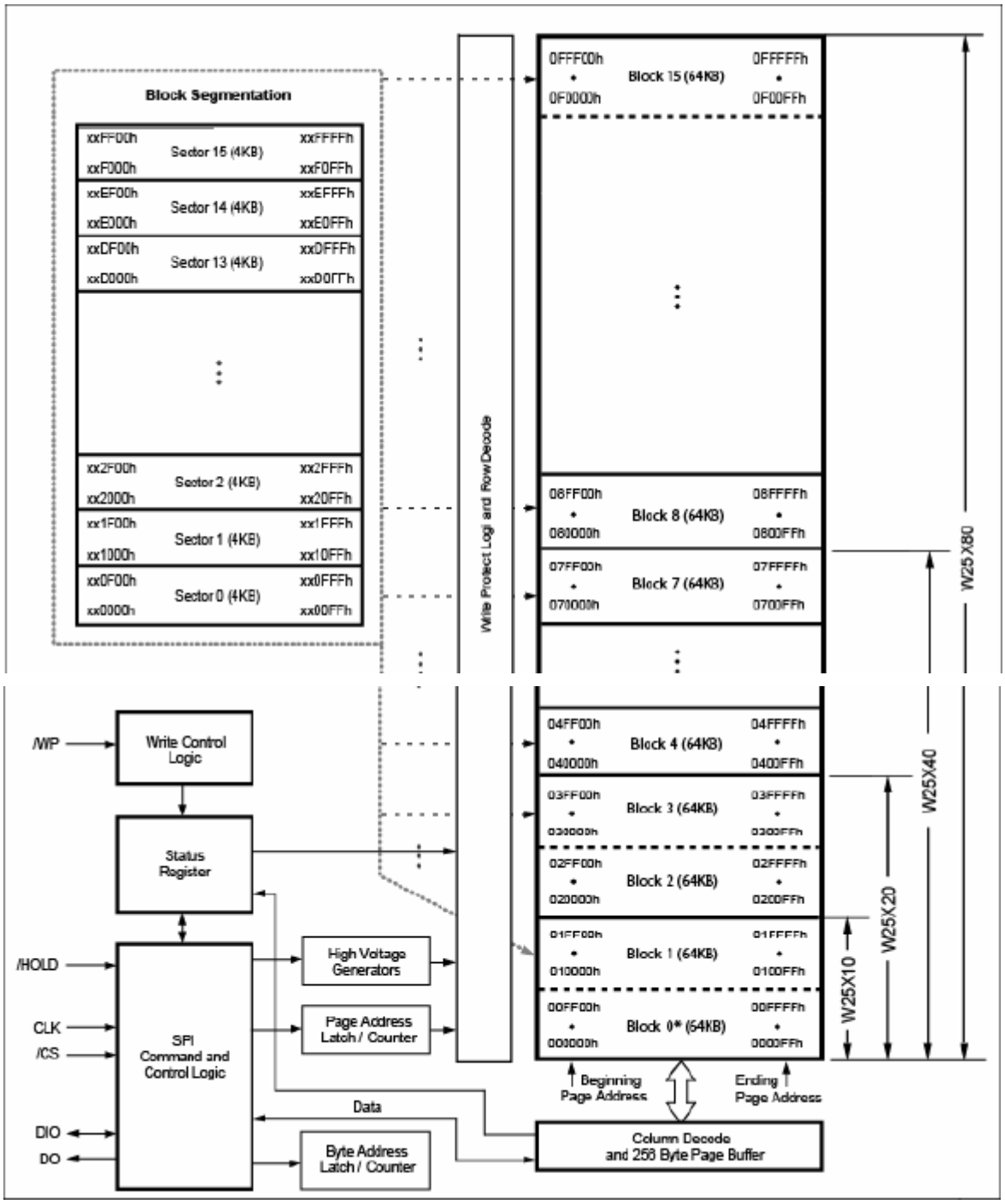
■ Software and Hardware Write Protection

- White-Protect all or portion of memory
- Enable/Disable protection with /WP pin
- Top or bottom array protection

Pin introduction:

Pin NO.	Pin Name	I/O	Function
1	/CS	I	Chip Select Input
2	DO	O	Data Output
3	/WP	I	White Protect input
4	GND		Ground
5	DIO	I/O	Data Input/Output
6	CLK	I	Serial Clock Input
7	/HOLD	I	Hold input
8	VCC		Power Supply

W25X80-VSSIG internal block diagram:



5. HY5DU281622FTP-4 brief introduction:

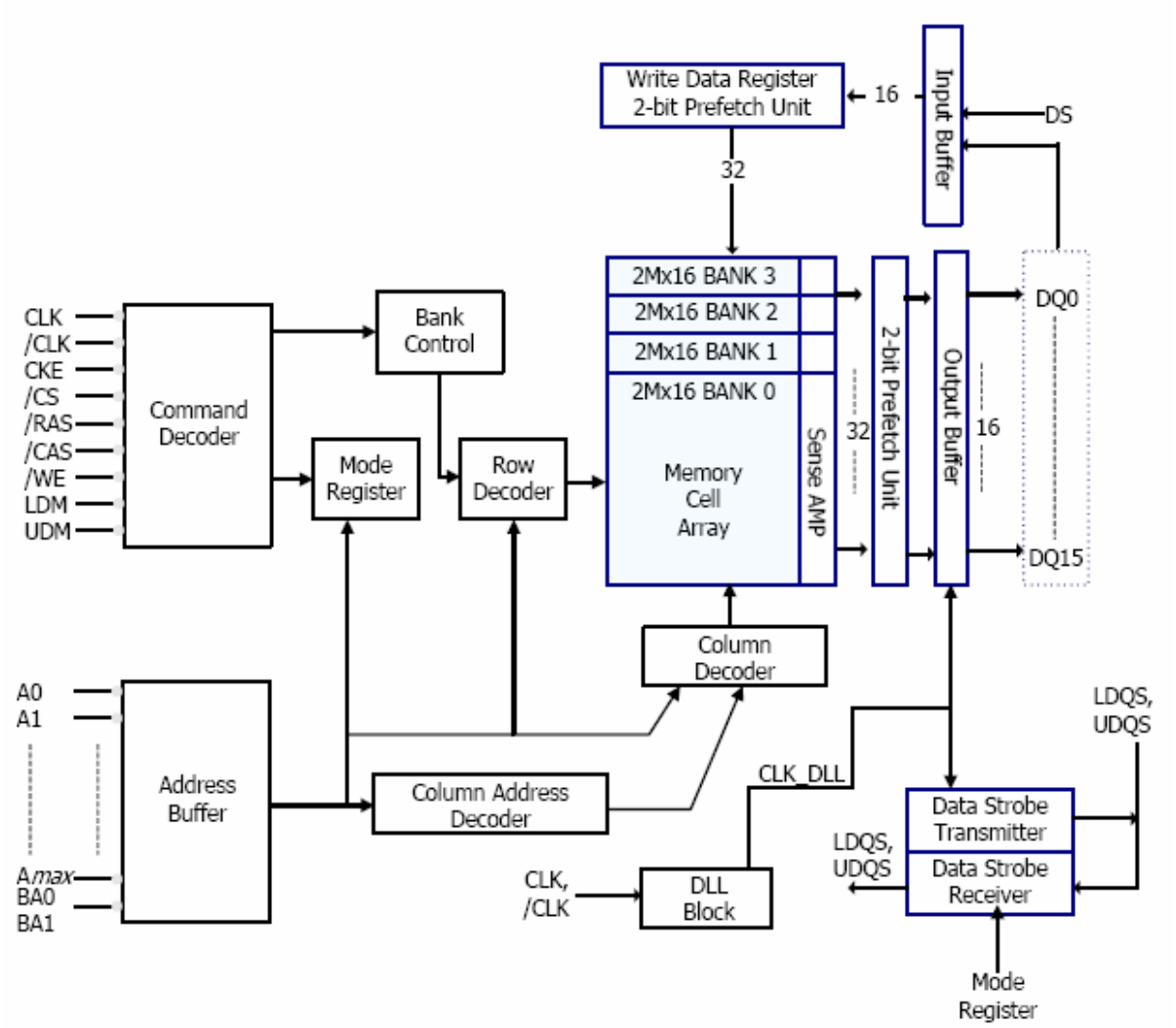
The HY5DU281622FT(P) is a 134,217,728-bit CMOS Double Data Rate(DDR) Synchronous DRAM, ideally suited for the main memory applications which requires large memory density and high bandwidth. This Hynix 128Mb DDR SDRAMs offer fully synchronous operations referenced to both rising and falling edges of the clock. While all addresses and control inputs are latched on the rising edges of the CK (falling edges of the /CK), Data,
Data strobes and Write data masks inputs are sampled on both rising and falling edges of it.

The data paths are internally pipelined and 2-bit prefetched to achieve very high bandwidth. All input and output voltage levels are compatible with SSTL_2.
main features:
• VDD, VDDQ = 2.3V min ~ 2.7V max
(Typical 2.5V Operation +/- 0.2V for DDR266, 333)
• VDD, VDDQ = 2.4V min ~ 2.7V max
(Typical 2.6V Operation +0.1/- 0.2V for DDR400,400Mbps/pin product and 500Mbps/pin product)
• All inputs and outputs are compatible with SSTL_2 interface
• Fully differential clock inputs (CK, /CK) operation
• Double data rate interface
• Source synchronous - data transaction aligned to bidirectional data strobe (DQS)
• x16 device has two bytewide data strobes (UDQS,LDQS) per each x8 I/O
• Data outputs on DQS edges when read (edged DQ)
Data inputs on DQS centers when write (centered DQ)
• On chip DLL align DQ and DQS transition with CK transition
• DM mask write data-in at the both rising and falling edges of the data strobe
• All addresses and control inputs except data, data strobes and data masks latched on the rising edges of the clock
• Programmable CAS latency 2/2.5 (DDR266, 333) and 3/4 (DDR400, 400Mbps/pin product and 500Mbps/pin product) supported
• Programmable burst length 2/4/8 with both sequential and interleave mode
• Internal four bank operations with single pulsed/RAS
• Auto refresh and self refresh supported
• tRAS lock out function supported
• 4096 refresh cycles/64ms
• JEDEC standard 400mil 66pin TSOP-II with 0.65mm pin pitch
• Lead free (*ROHS Compliant)

Pin introduction:

PIN	TYPE	DESCRIPTION
CK, /CK	Input	Clock: CK and /CK are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of /CK. Output (read) data is referenced to the crossings of CK and /CK (both directions of crossing).
CKE	Input	Clock Enable: CKE HIGH activates, and CKE LOW deactivates internal clock signals, and device input buffers and output drivers. Taking CKE LOW provides PRECHARGE POWER DOWN and SELF REFRESH operation (all banks idle), or ACTIVE POWER DOWN (row ACTIVE in any bank). CKE is synchronous for POWER DOWN entry and exit, and for SELF REFRESH entry. CKE is asynchronous for SELF REFRESH exit, and for output disable. CKE must be maintained high throughout READ and WRITE accesses. Input buffers, excluding CK, /CK and CKE are disabled during POWER DOWN. Input buffers, excluding CKE are disabled during SELF REFRESH. CKE is an SSTL_2 input, but will detect an LVCMOS LOW level after V*DD* is applied.
/CS	Input	Chip Select: Enables or disables all inputs except CK, /CK, CKE, DQS and DM. All commands are masked when Chip Select is registered high. Chip Select provides for external bank selection on systems with multiple banks. Chip Select is considered part of the command code.
BA0, BA1	Input	Bank Address Inputs: BA0 and BA1 define to which bank an ACTIVE, Read, Write or PRECHARGE command is being applied.
A0 ~ A11	Input	Address Inputs: Provide the row address for ACTIVE commands, and the column address and AUTO PRECHARGE bit for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 is sampled during a precharge command to determine whether the PRECHARGE applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by BA0, BA1. The address inputs also provide the op code during a MODE REGISTER SET command. BA0 and BA1 define which mode register is loaded during the MODE REGISTER SET command (MRS or EMRS).
/RAS, /CAS, /WE	Input	Command Inputs: /RAS, /CAS and /WE (along with /CS) define the command being entered.
DM (LDM,UDM)	Input	Input Data Mask: DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH along with that input data during a WRITE access. DM is sampled on both edges of DQS. Although DM pins are input only, the DM loading matches the DQ and DQS loading. For the x16, LDM corresponds to the data on DQ0-Q7; UDM corresponds to the data on DQ8-Q15.
DQS (LDQS,UDQS)	I/O	Data Strobe: Output with read data, input with write data. Edge aligned with read data, centered in write data. Used to capture write data. For the x16, LDQS corresponds to the data on DQ0-Q7; UDQS corresponds to the data on DQ8-Q15.
DQ	I/O	Data input / output pin: Data bus
V*DD* / V*SS*	Supply	Power supply for internal circuits and input buffers.
V*DDQ* / V*SSQ*	Supply	Power supply for output buffers for noise immunity.
V*REF*	Supply	Reference voltage for inputs for SSTL interface.
NC	NC	No connection.

HY5DU281622FTP-4 internal block diagram:



6. TDA9885T/TDA9886T brief introduction:

The TDA9885 is an alignment-free multistandard (PAL and NTSC) vision and sound IF signal PLL demodulator for negative modulation only and FM processing.

The TDA9886 is an alignment-free multistandard (PAL, SECAM and NTSC) vision and sound IF signal PLL demodulator for positive and negative modulation, including sound AM and FM processing.

Features:

· 5 V supply voltage

· Gain controlled wide-band Vision Intermediate Frequency (VIF) amplifier, AC-coupled

· Multistandard true synchronous demodulation with active carrier regeneration: very linear demodulation ,good inter modulation figures, reduced harmonics, and excellent pulse response

· Gated phase detector for L and L-accent standard

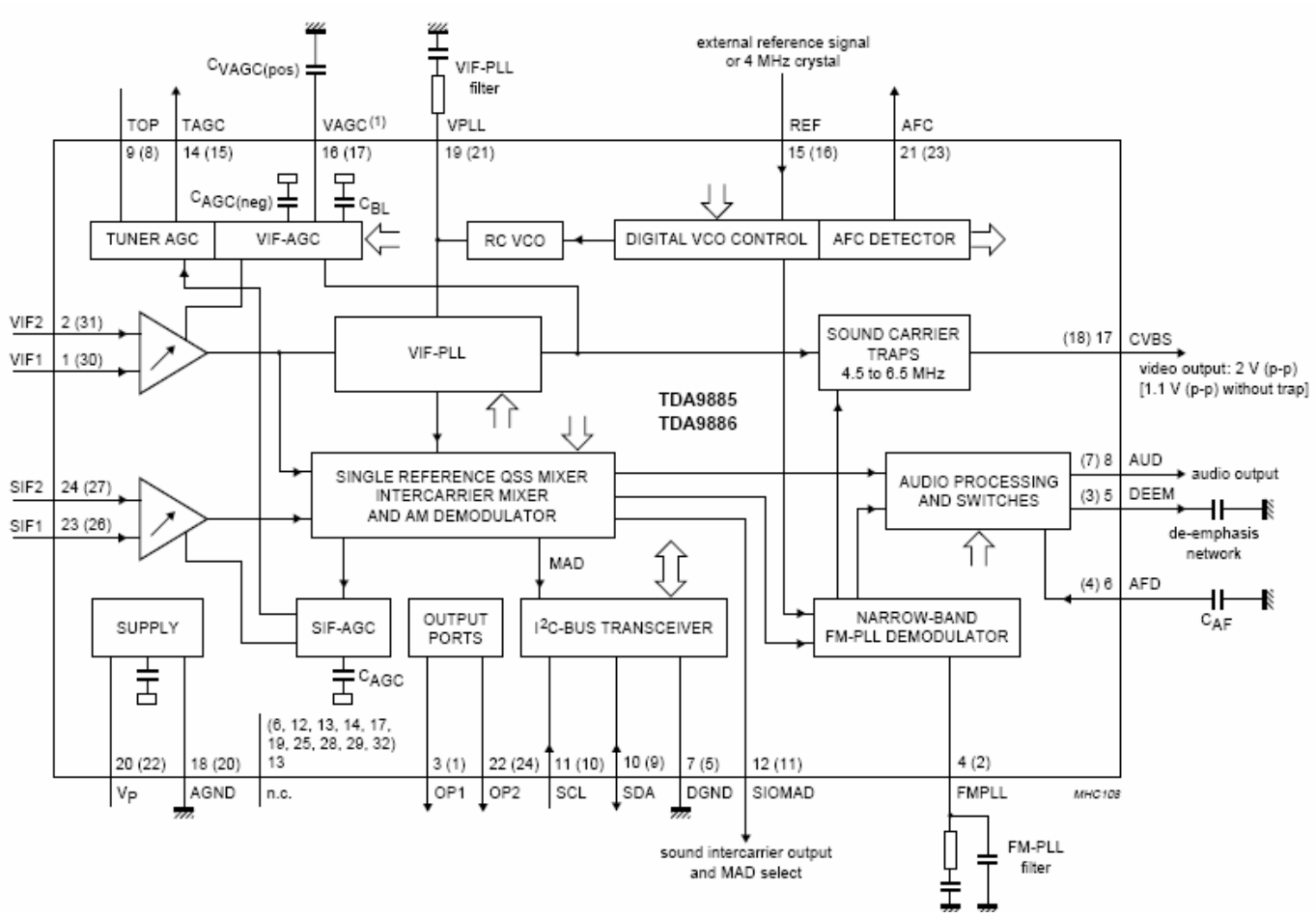
· Fully integrated VIF Voltage Controlled Oscillator (VCO), alignment-free, frequencies switchable for all
negative and positive modulated standards via I2C-bus
· Digital acquisition help, VIF frequencies of 33.4, 33.9,38.0, 38.9, 45.75, and 58.75 MHz
· 4 MHz reference frequency input: signal from Phase-Locked Loop (PLL) tuning system or operating as crystal oscillator
· VIF Automatic Gain Control (AGC) detector for gain control, operating as peak sync detector for negative modulated signals and as a peak white detector for positive modulated signals
· External AGC setting via pin OP1
· Precise fully digital Automatic Frequency Control (AFC) detector with 4-bit digital-to-analog converter, AFC bits readable via I2C-bus
· Take Over Point (TOP) adjustable via I2C-bus or alternatively with potentiometer
· Fully integrated sound carrier trap for 4.5, 5.5, 6.0, and 6.5 MHz, controlled by FM-PLL oscillator
· Sound IF (SIF) input for single reference Quasi Split Sound (QSS) mode, PLL controlled
· SIF-AGC for gain controlled SIF amplifier, single reference QSS mixer able to operate in high performance single reference QSS mode and in intercarrier mode, switchable via I2C-bus
· AM demodulator without extra reference circuit
· Alignment-free selective FM-PLL demodulator with high linearity and low noise
· Four selectable I2C-bus addresses
· I2C-bus control for all functions
· I2C-bus transceiver with pin programmable Module
Address (MAD).

Pin function

SYMBOL	PIN				DESCRIPTION
	TDA9885T TDA9885TS	TDA9886T TDA9886TS	TDA9885HN	TDA9886HN	
VIF1	1	1	30	30	VIF differential input 1
VIF2	2	2	31	31	VIF differential input 2
n.c.	–	–	32	32	not connected
OP1	3	3	1	1	output port 1; open-collector
FMPLL	4	4	2	2	FM-PLL for loop filter
DEEM	5	5	3	3	de-emphasis output for capacitor
AFD	6	6	4	4	AF decoupling input for capacitor
DGND	7	7	5	5	digital ground
n.c.	–	–	6	6	not connected
AUD	8	8	7	7	audio output
TOP	9	9	8	8	tuner AGC TakeOver Point (TOP) for resistor adjustment
SDA	10	10	9	9	I^2C-bus data input and output
SCL	11	11	10	10	I^2C-bus clock input
SIOMAD	12	12	11	11	sound intercarrier output and MAD select with resistor

n.c.	–	–	12	12	not connected
n.c.	13	13	13	13	not connected
n.c.	–	–	14	14	not connected
TAGC	14	14	15	15	tuner AGC output
REF	15	15	16	16	4 MHz crystal or reference signal input
VAGC	–	16	–	17	VIF-AGC for capacitor
n.c.	16	–	17	–	not connected
CVBS	17	17	18	18	composite video output
n.c.	–	–	19	19	not connected
AGND	18	18	20	20	analog ground
VPLL	19	19	21	21	VIF-PLL for loop filter
V_P	20	20	22	22	supply voltage
AFC	21	21	23	23	AFC output
OP2	22	22	24	24	output port 2; open-collector
n.c.	–	–	25	25	not connected
SIF1	23	23	26	26	SIF differential input 1 and MAD select with resistor
SIF2	24	24	27	27	SIF differential input 2 and MAD select with resistor
n.c.	–	–	28	28	not connected
n.c.	–	–	29	29	not connected

TDA9886T internal block diagram:



7. 74HC4052 brief introduction:

The M74HCT4052 is a dual four-channel analog MULTIPLEXER/DEMULTIPLEXER fabricated with silicon gate C2MOS technology and it is pin to pin compatible with the equivalent metal gate CMOS4000B series. It contains 8 bidirectional and digitally controlled analog switches.

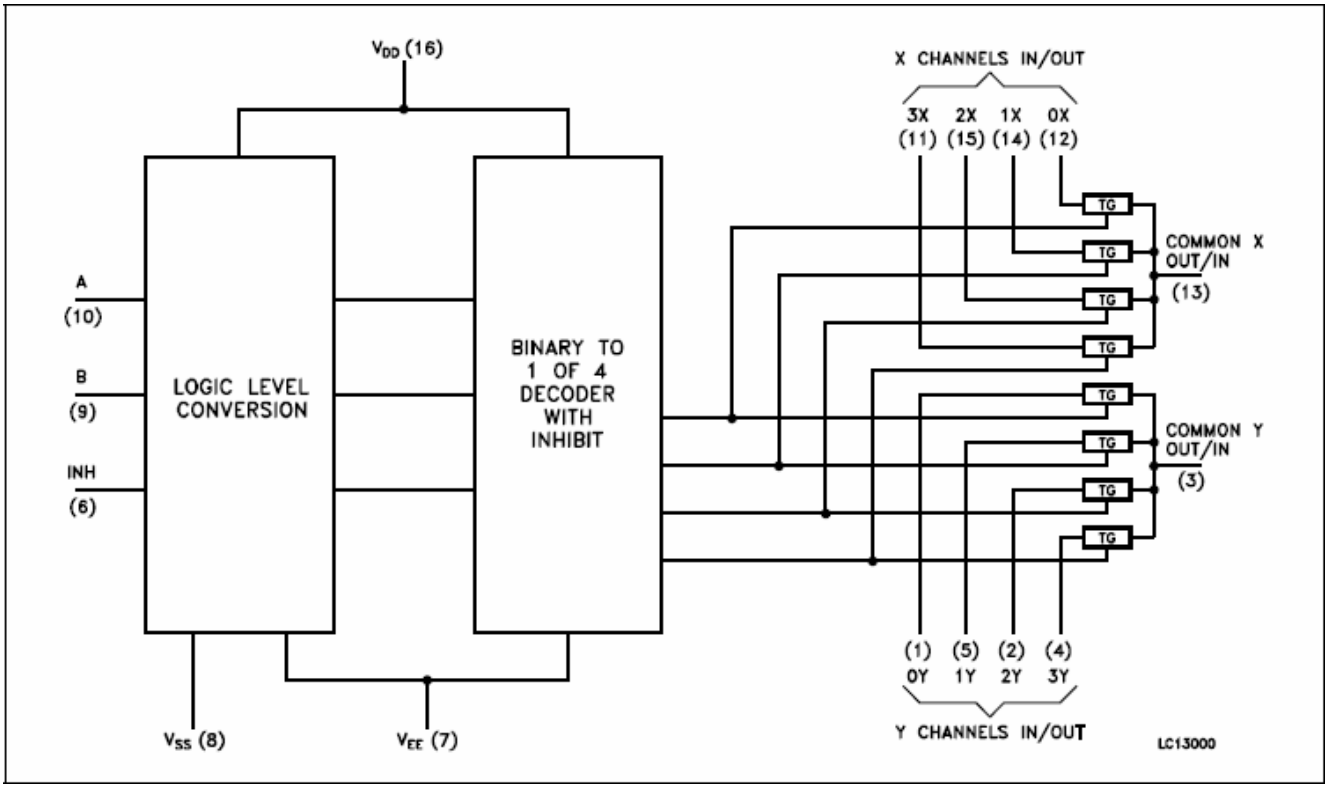
Feature:

• Low power dissipation:
ICC = 4mA (MAX.) at TA=25°C
•Logic level translation to enable
TTL logic signal to communicate
With ±5V analog signal
• Low "ON" resistance:
70W TYP. (VCC - VEE = 4.5V)
50W TYP. (VCC - VEE = 9V)
•Wide analog input voltage range: ±6V
•Fast switching: tpd = 13ns (TYP.) at TA = 25 °C
• Low crosstalk between switches
• High ON/OFF output voltage ratio
•Wide operating supply voltage range (VCC - VEE) = 2V TO 12V
• Low sine wave distortion: 0.02% at VCC - VEE = 9V
•Compatible with TLL outputs: VIH = 2V(MIN.) VIL = 0.8V (MAX.)
• PIN and function compatible with 74 series 4052

Pin introduction:

Pin	SYMBOL	Function description
1,5,2,4	2Y0 to 2Y3	Independent Input Outputs
6	INH	INHIBIT Input
7	VEE	Negative Supply Voltage
10,9	A,B	Select Inputs
12,14,15,11	1Y0 to 1Y3	Independent Input Outputs
3	2-COM	Common X Output/Input
13	1-COM	Common Y Output/Input
8	GND	Ground
16	VCC	Positive Supply Voltage

74HCT4052 internal block diagram:



8. 74LVC14A brief introduction:

The 74LVC14A is a high-performance, low-power, low-voltage, Si-gate CMOS device, superior to most advanced CMOS compatible TTL families. Inputs can be driven from either 3.3 or 5 V devices. This feature allows the use of these devices as translators in a mixed 3.3 and 5V environment.

The 74LVC14A provides six inverting buffers with Schmitt-trigger action. It is capable of transforming slowly changing input signals into sharply defined, jitter-free output signals.

Feature:

· Wide supply voltage range from 1.2 to 3.6 V
· CMOS low power consumption
· Direct interface with TTL levels
· Inputs accept voltages up to 5.5 V
· Complies with JEDEC standard no. 8-1A
· Specified from -40 to +85 °C and -40 to +125 °C.

Pin introduction:

PIN	SYMBOM	DESCRIPTION
1,3,5,9,11 and 13	1A to 6A	Data input
2,4,6,8,10 and 12	1Y to 6Y	Data output
7	GND	Ground
14	VCC	supply voltage

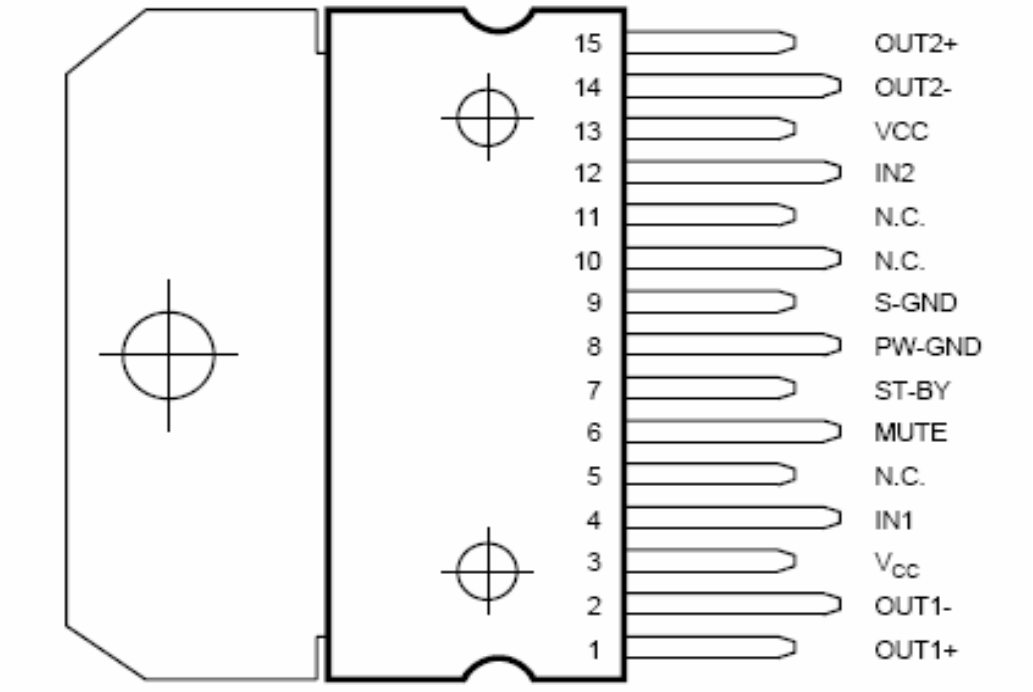
14.TDA7266SA brief introduction:

The TDA7266SA is a dual bridge amplifier specially designed for TV and Portable Radio applications.

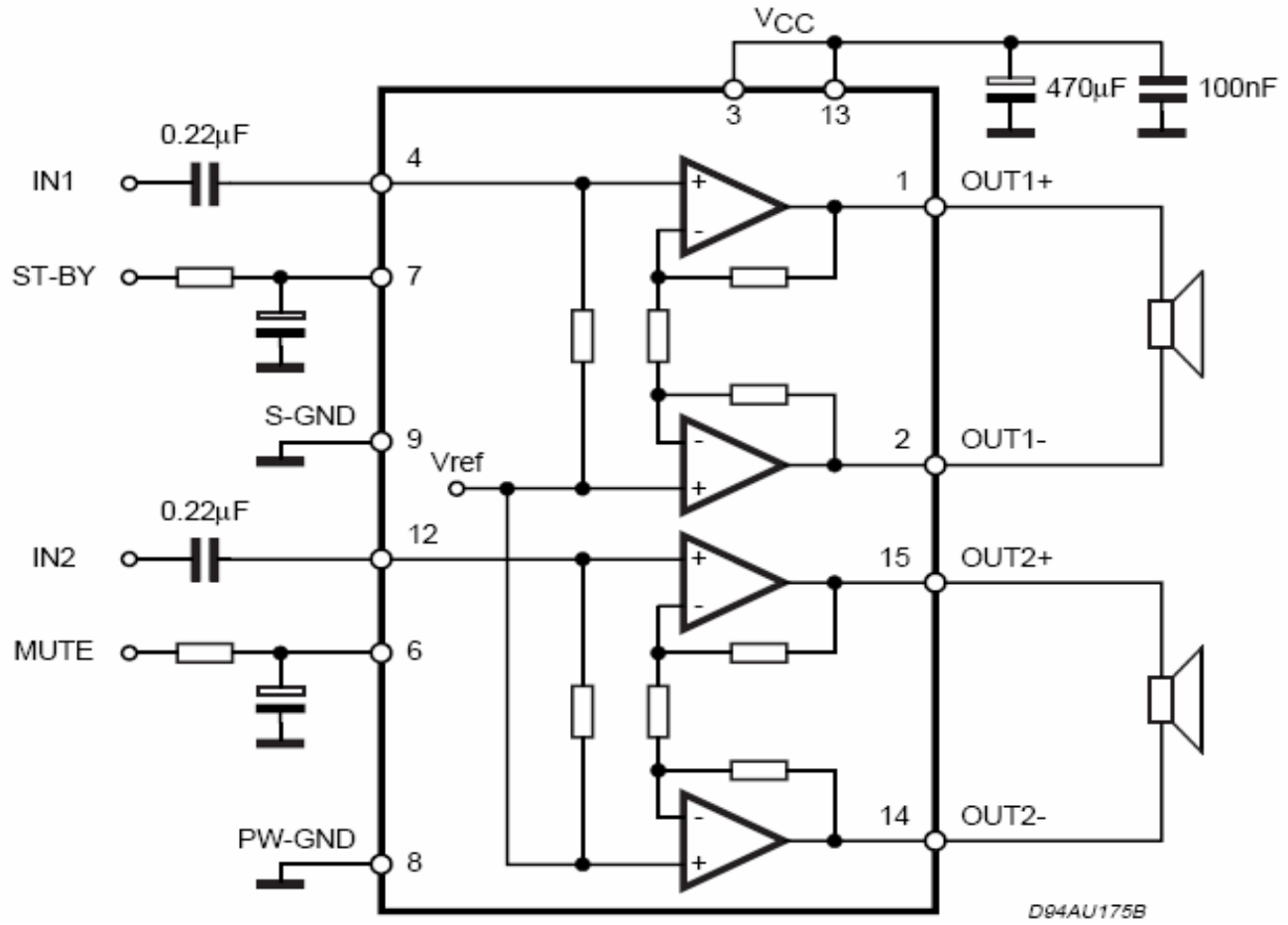
Feature:

• WIDE SUPPLY VOLTAGE RANGE (3-18V)
• MINIMUM EXTERNAL COMPONENTS
– NO SWR CAPACITOR
– NO BOOTSTRAP
– NO BOUCHEROT CELLS
– INTERNALLY FIXED GAIN
• STAND-BY & MUTE FUNCTIONS
• SHORT CIRCUIT PROTECTION
• THERMAL OVERLOAD PROTECTION

PIN CONNECTION：



TDA7266SA internal block diagram:



Chapter 3: Analysis of Signal process Flowchart and key point measure date

This chapter mainly introduces the receipt and dispose of AV signal the power supply system and system control process of this TV.

1. Video signal flow

RF signal is demodulated by tuner, then the obtained video signal and signals inputted from COMPONENT terminal, AV, S-VIDEO, 2-way SCART interface and VGA interface are all sent into video-processing IC SVP-AX32LF/SVP-AX68LF for decoding. The different format input signals are changed into uniform LVDS signals, and are sent to LCD screen. In addition, TV video signal is processed by SVP-AX32LF/SVP-AX68LF to generate 2 CVBS signal, which are used in SCART video output.

Signal inputted from HDMI interface is into video decoding IC SVP-AX32LF/SVP-AX68LF for decoding. After procession, the obtained uniform LVDS differential signal is sent into LCD Screen.

2.Sound process flow

RF signal is demodulated by tuner, and then the obtained SIF signal (SIF-2 signal) and audio signal inputted from Scart1 interface are are first sent into 74HCT4052D for choosing passages. The output audio signal of 74HC4052 is sent into power amplifier TDA7266DNS, and the amplified signal is finally sent into speaker or earphone.

Signals from HDTV terminal, AV terminal, Scart2 interface and PC Audio are first sent into 74HCT4052 for choosing passages, and then sent into SVP-AX32LF/SVP-AX68LF for demodulation and sound process. The output audio signal of SVP-AX32LF/SVP-AX68LF is sent into power amplifier TDA7266DN, and finally the amplified signals are sent into speaker or earphone.

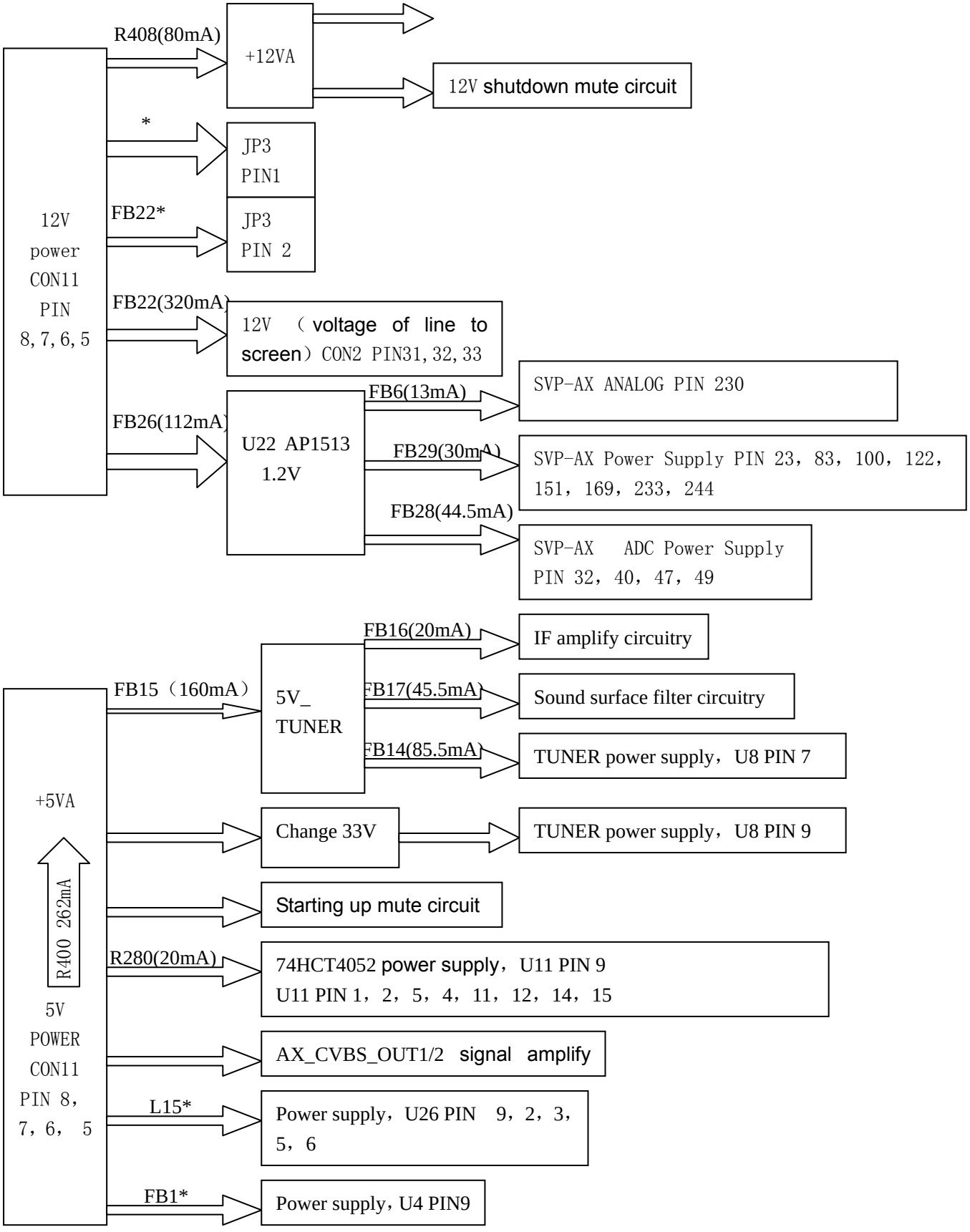
After the demodulation and sound effect processing of SVP-AX32LF/SVP-AX68LF, there is an audio output which is used for sound output of Scart1 terminal.

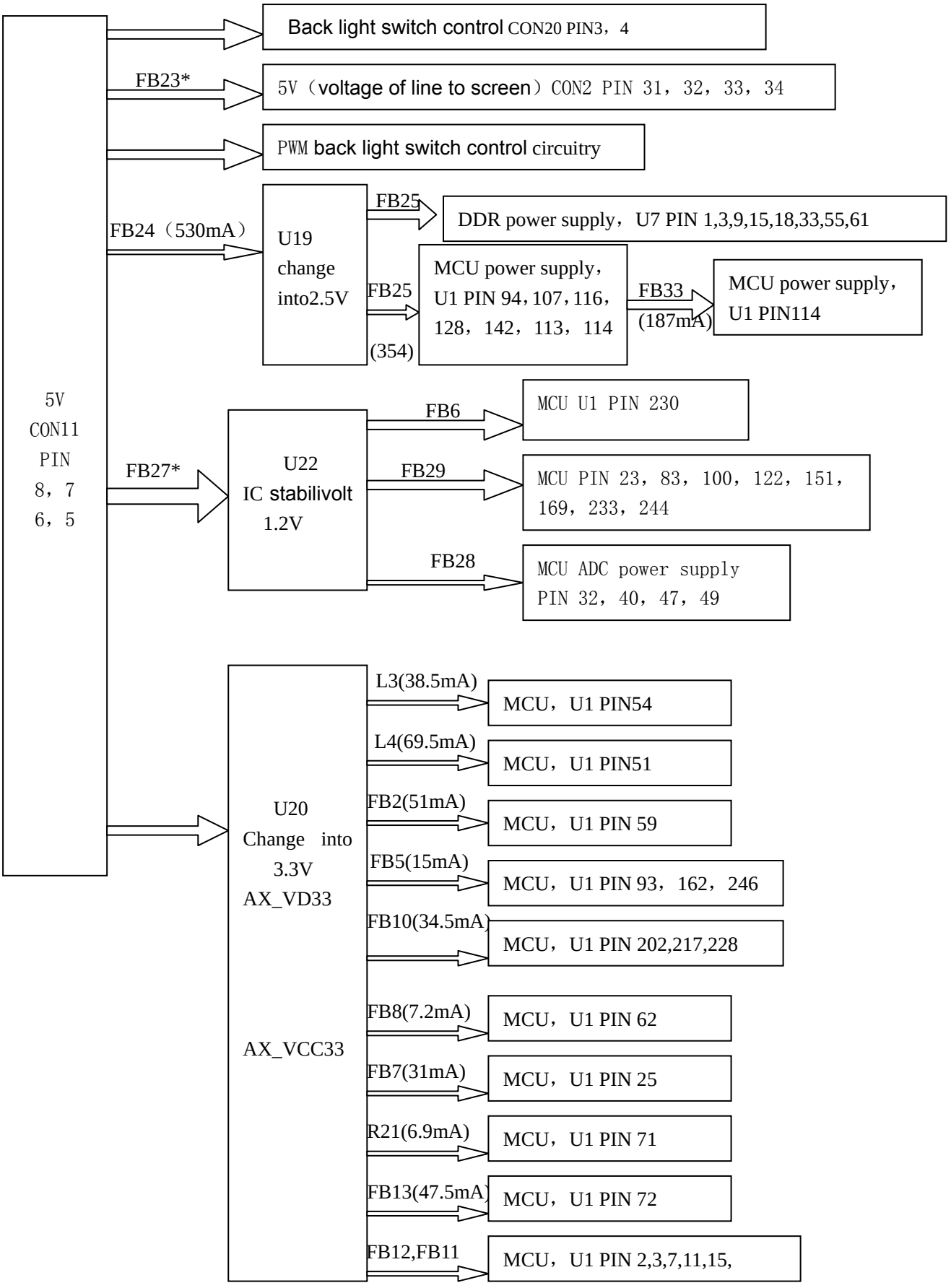
3. Power supply system

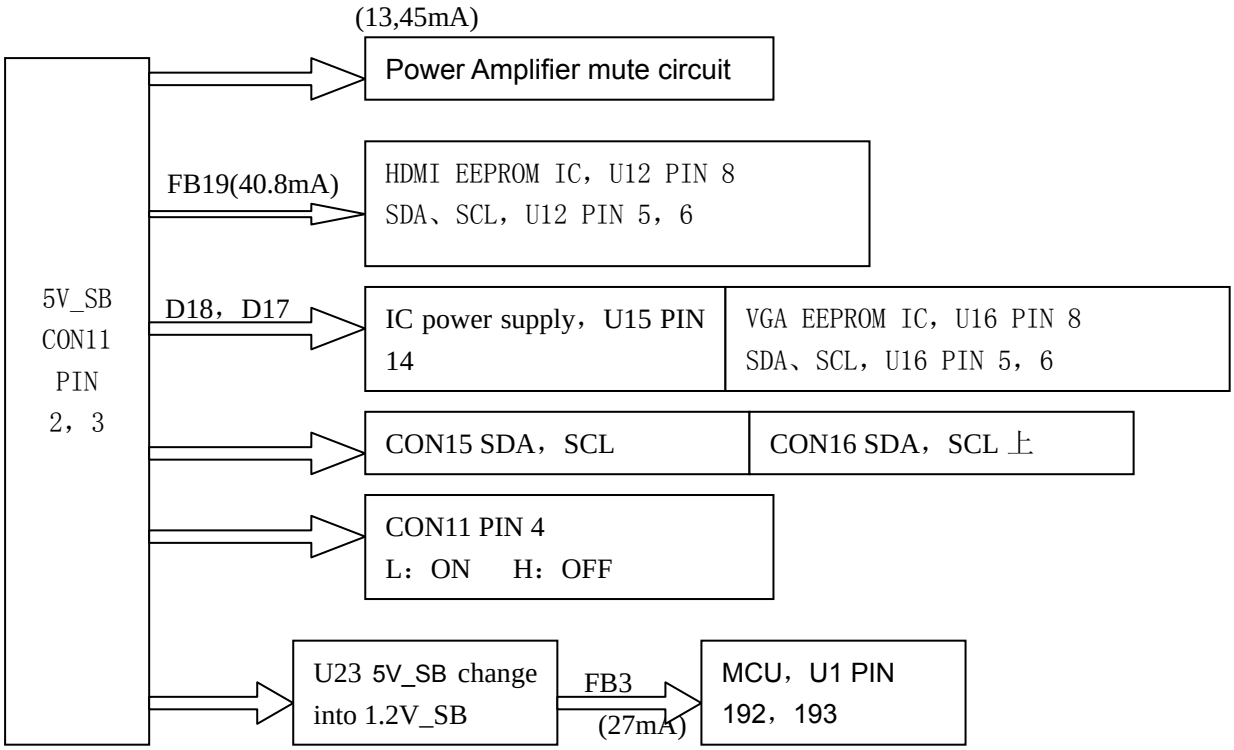
There are 3 ways of voltage output in the power panel:+12V、+5V and +5V-SB. +12V output is provided for power amplifier TDA7266, and is also changed into +1.2V output by MP1411 to supply SVP-AX IC; +5V output is changed into 3.3V output，2.5Voutput and 1.2V output by DC/DC (such as AX_VD33) to satisfy the needs ICs. +12V and +5V outputs will be cut off in standby state. While +5-SB output is the power supply of MCU, infrared receiver and EEPROM etc, and will be cut off when the AC is turn off.

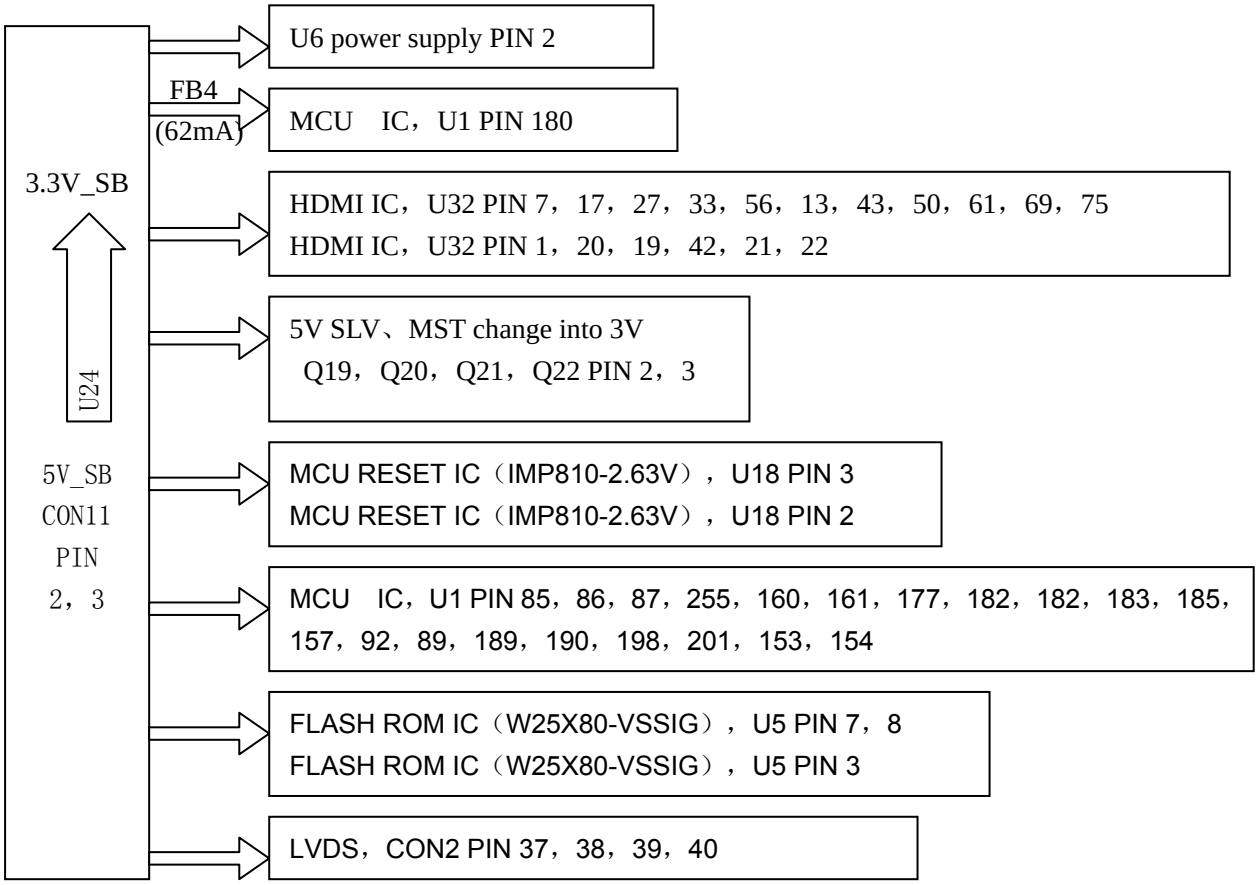
5V output will be divided into two ways: one way is changed into 5VA power supplies through DC/DC converter for TUNER, 74HCT4052 IC etc and peripheral circuits; the other way of 5V voltage supply power especially for MCU, infrared receiver and EEPROM etc, and will still operating in standby state.

(1) The composition and distribution of the TV power supply（Next page）


12V power CON11 PIN 8,7,6,5
R408(80mA)
+12VA
12V shutdown mute circuit
*
JP3 PIN1
FB22*
JP3 PIN 2
FB22(320mA)
12V （voltage of line to screen）CON2 PIN31,32,33
FB26(112mA)
U22 AP1513 1.2V
FB6(13mA)
SVP-AX ANALOG PIN 230
FB29(30mA)
SVP-AX Power Supply PIN 23，83，100，122，151，169，233，244
FB28(44.5mA)
SVP-AX ADC Power Supply PIN 32，40，47，49
+5VA
R400 262mA
5V POWER CON11 PIN 8，7，6， 5
FB15（160mA）
5V_ TUNER
FB16(20mA)
IF amplify circuitry
FB17(45.5mA)
Sound surface filter circuitry
FB14(85.5mA)
TUNER power supply，U8 PIN 7
Change 33V
TUNER power supply，U8 PIN 9
Starting up mute circuit
R280(20mA)
74HCT4052 power supply，U11 PIN 9
U11 PIN 1，2，5，4，11，12，14，15
AX_CVBS_OUT1/2 signal amplify
L15*
Power supply，U26 PIN 9，2，3，5，6
FB1*
Power supply，U4 PIN9


5V
CON11
PIN
8，7
6，5
Back light switch control CON20 PIN3，4
FB23*
5V（voltage of line to screen）CON2 PIN 31，32，33，34
PWM back light switch control circuitry
FB24（530mA）
U19
change
into2.5V
FB25
DDR power supply，U7 PIN 1,3,9,15,18,33,55,61
FB25
(354)
MCU power supply，
U1 PIN 94，107，116，
128，142，113，114
FB33
(187mA)
MCU power supply，
U1 PIN114
FB27*
U22
IC stabilivolt
1.2V
FB6
MCU U1 PIN 230
FB29
MCU PIN 23，83，100，122，151，
169，233，244
FB28
MCU ADC power supply
PIN 32，40，47，49
U20
Change into
3.3V
AX_VD33
AX_VCC33
L3(38.5mA)
MCU，U1 PIN54
L4(69.5mA)
MCU，U1 PIN51
FB2(51mA)
MCU，U1 PIN 59
FB5(15mA)
MCU，U1 PIN 93，162，246
FB10(34.5mA)
MCU，U1 PIN 202,217,228
FB8(7.2mA)
MCU，U1 PIN 62
FB7(31mA)
MCU，U1 PIN 25
R21(6.9mA)
MCU，U1 PIN 71
FB13(47.5mA)
MCU，U1 PIN 72
FB12,FB11
MCU，U1 PIN 2,3,7,11,15,


(13,45mA)
Power Amplifier mute circuit
FB19(40.8mA)
HDMI EEPROM IC，U12 PIN 8
SDA、SCL，U12 PIN 5，6
5V_SB
CON11
PIN
2，3
D18，D17
IC power supply，U15 PIN 14
VGA EEPROM IC，U16 PIN 8
SDA、SCL，U16 PIN 5，6
CON15 SDA，SCL
CON16 SDA，SCL 上
CON11 PIN 4
L：ON H：OFF
U23 5V_SB change into 1.2V_SB
FB3
(27mA)
MCU，U1 PIN 192，193


U6 power supply PIN 2
FB4
(62mA)
MCU IC，U1 PIN 180
3.3V_SB
U24
HDMI IC，U32 PIN 7，17，27，33，56，13，43，50，61，69，75
HDMI IC，U32 PIN 1，20，19，42，21，22
5V SLV、MST change into 3V
Q19，Q20，Q21，Q22 PIN 2，3
5V_SB
CON11
PIN
2，3
MCU RESET IC（IMP810-2.63V），U18 PIN 3
MCU RESET IC（IMP810-2.63V），U18 PIN 2
MCU IC，U1 PIN 85，86，87，255，160，161，177，182，182，183，185，157，92，89，189，190，198，201，153，154
FLASH ROM IC（W25X80-VSSIG），U5 PIN 7，8
FLASH ROM IC（W25X80-VSSIG），U5 PIN 3
LVDS，CON2 PIN 37，38，39，40

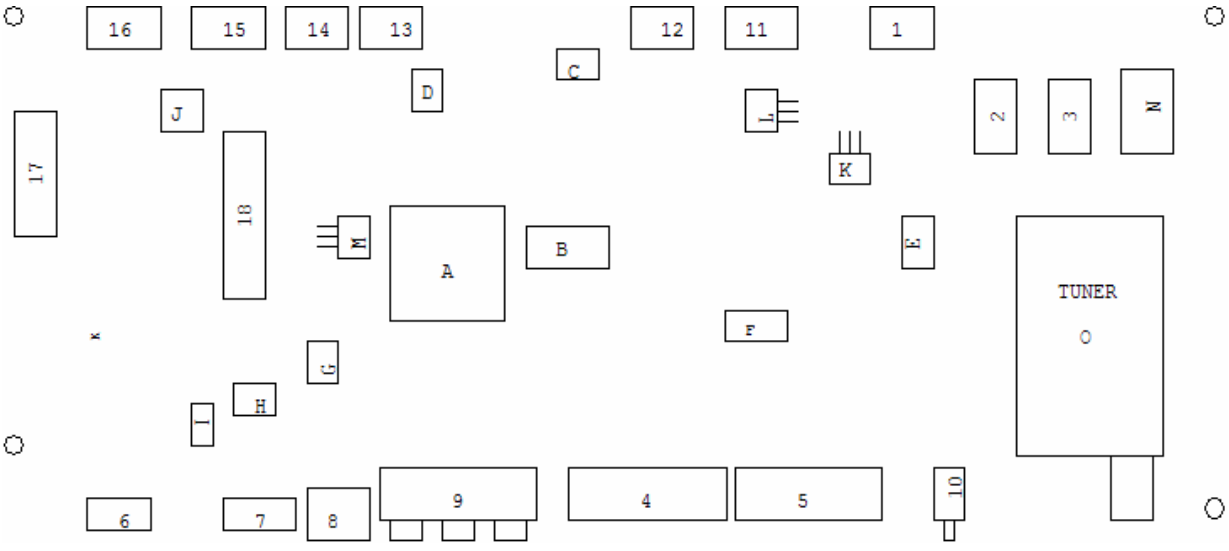
(2)

Position number	Component model	Pin 1(V)	Pin 2(V)	Pin 3(V)
U19	AP1117D25	GND	2.5V	5V
U20	AP1117E33	GND	3.3V	5V
U23	AZP1122EL	GND	1.2V	5V
U24	AP1117E33	GND	3.3V	5V

(3) Pin sequence of power cord of power panel

Position number	Pin	Pin description
CON1	1	12VA
	2	12VA
	3	GND
	4	GND
CON23	1	5V-SB
	2,3,7,8	GND
	4,5	5V
	6	5V-SB
	9,10	12V

4. Position and definition of the main components and sockets on mainboard(see next page)



(1) Socket definition

Serial number	Position number	Connecting object	Function description
1	CON1	Power panel	+12V，+12V ，GND，GND
2	CON4	Speaker	L+,L-,R+,R-
3	CON5	Earphone Board	
4	CON8	SCART1 input	
5	CON9	SCART2 input	
6	CON10 CON27	HDMI input	
7	CON13	VGA audio signal input	
8	CON12	S terminal input	
9	CON14	VGA input	
10	CON21	AV Input	
11	CON15	Standby	
12	CON16	Standby	
13	CON18	Keyboard	+3.3V、GND、KEY1、KEY2
14	CON19	Remote control receiving board	+3.3V、REMOTE、GND、indicator1、indicator1
15	CON17	Standby	
16	CON20	Back light control line	GND，GND，back light switch control，back light brightness control
17	CON23	Power panel	5V-SB,GND,GND,5V,5V,5V-SB,GND,GND,12V,12V

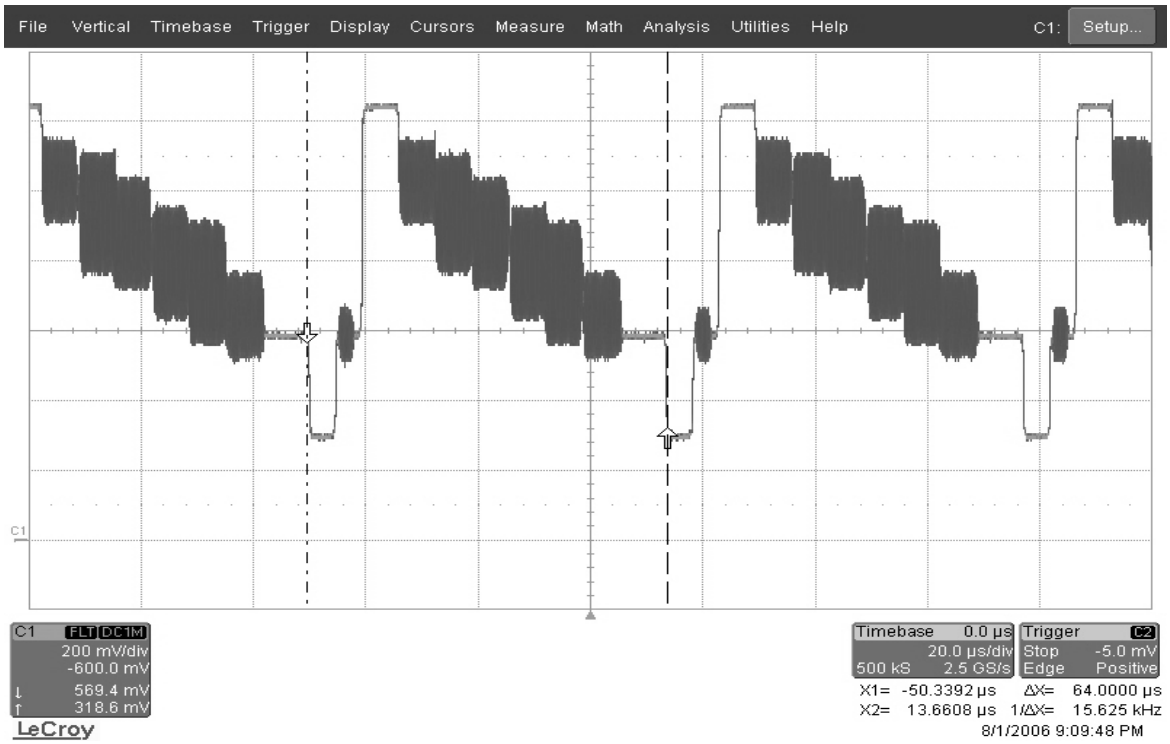
(2) Main components descriptions

Serial number	Position number	component	Function description
A	U1	SVP-AX32LF/SVP-AX68LF	Video decoder, image processor, A/D and D/A conversion
B	U7	HY5DU281622FTP-4	8M×16bits DDR
C	U3	AT24C64	EEPROM
D	U5	W25X80-VSSIG	8M-bit Serial Flash, Store the Control program.
E	U9	TDA9886T	Alignment-free multistandard vision,sound AM and FM processing
F	U11	74HC4052	Audio input switch of AV terminal
G	U12、U16	AT24C02	EEPROM
H	U15	74LVC14A	VGA line and field synchronizing signal waveform shaping
I	U17	IRF7404	Thermoelectric Cooler Controller
J	U19	AP1117D25	5V to 2.5V DC-DC Converter
K	U24	AP1117E33	5V to 3.3V DC conversion

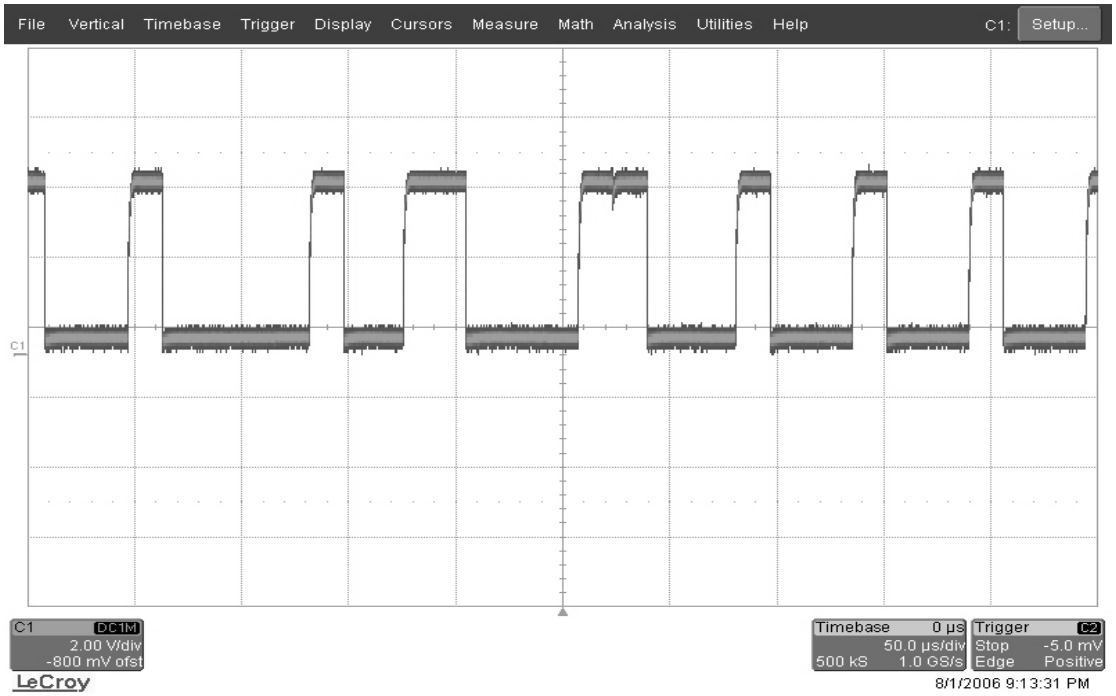
L	U23	AP1122EL	5V to 1.2V DC conversion
M	U27	TDA7266SA	Audio amplifier (BTL output)
N	U8	AFT7/W003 AFT7/W103 AFT7/W300	Tuner output sound IF and video signal

5. Waveforms at key points

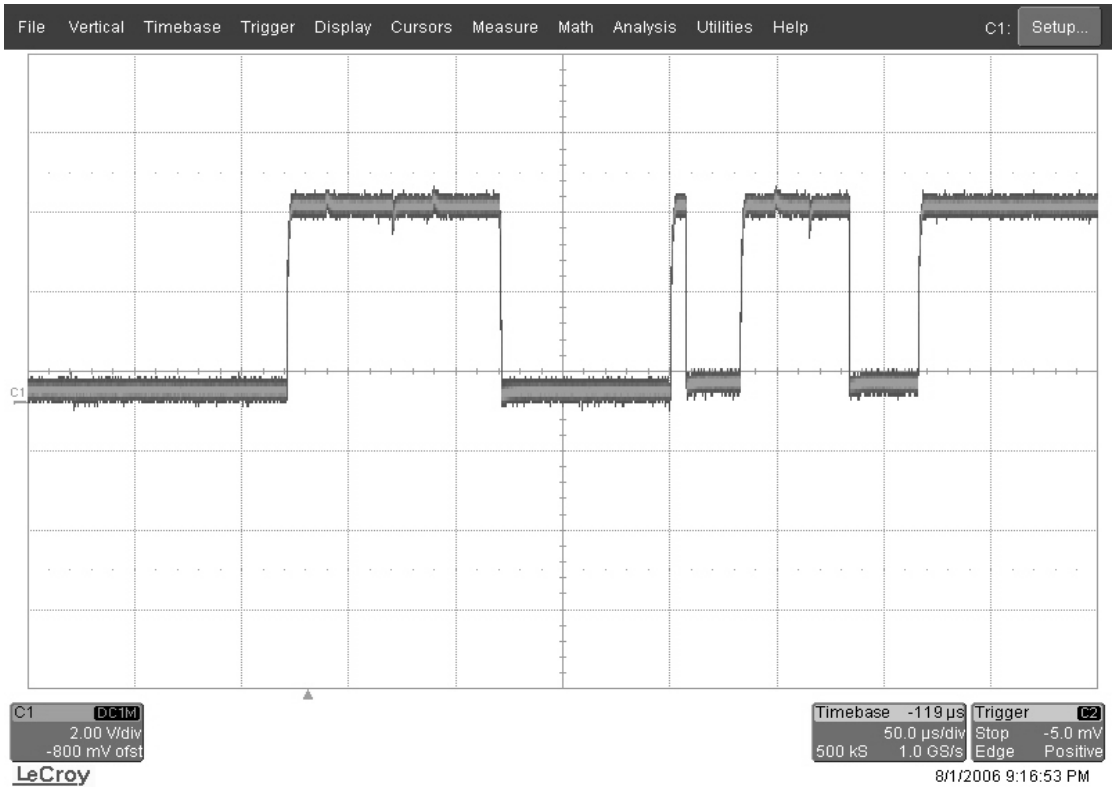
(1)RF inputting color bar signal, Composite Video Signal waveform at pin 11 of tuner U8, and the waveform at pin 52 of U1（SVP-AX32LF/SVP-AX68LF） is like this:



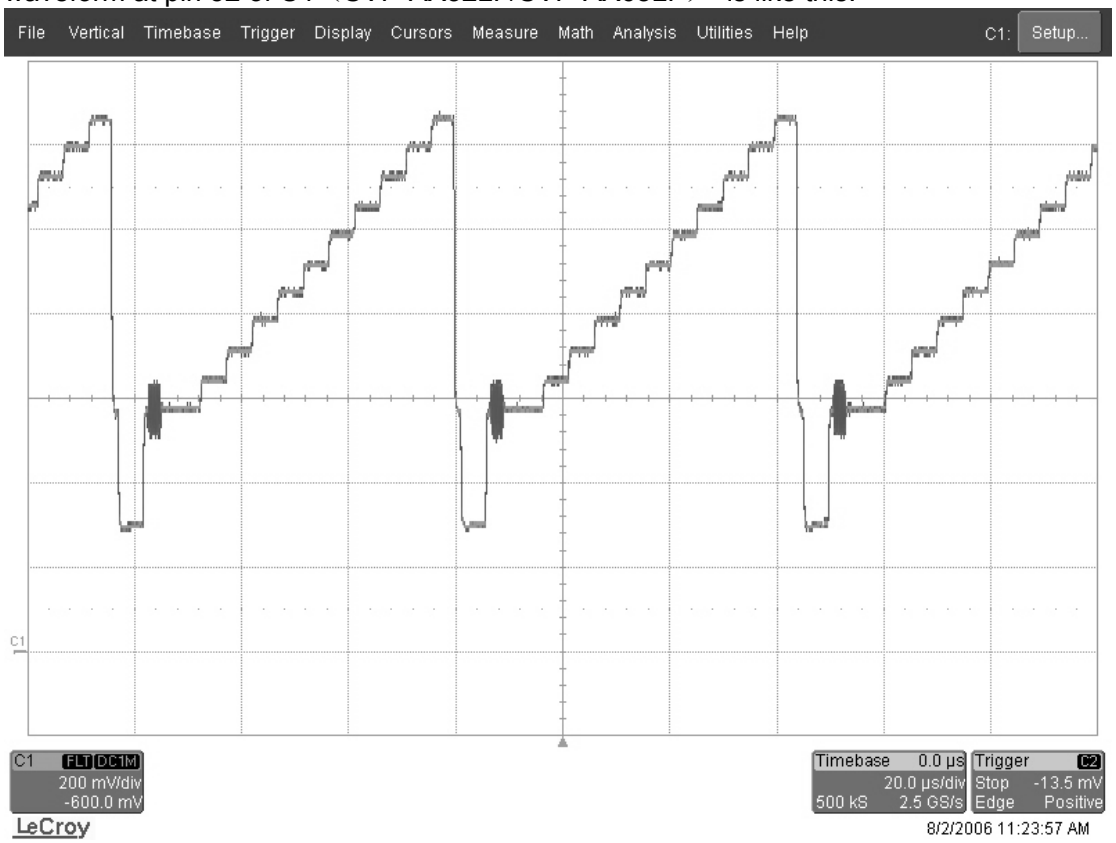
(2)RF inputting color bar signal, clock signal SCL, pin 11 of U9, pin 6 of U3, pin 6 of U12, pin 6 of U16, pin 154 of U1, pin 4 of tuner U15:



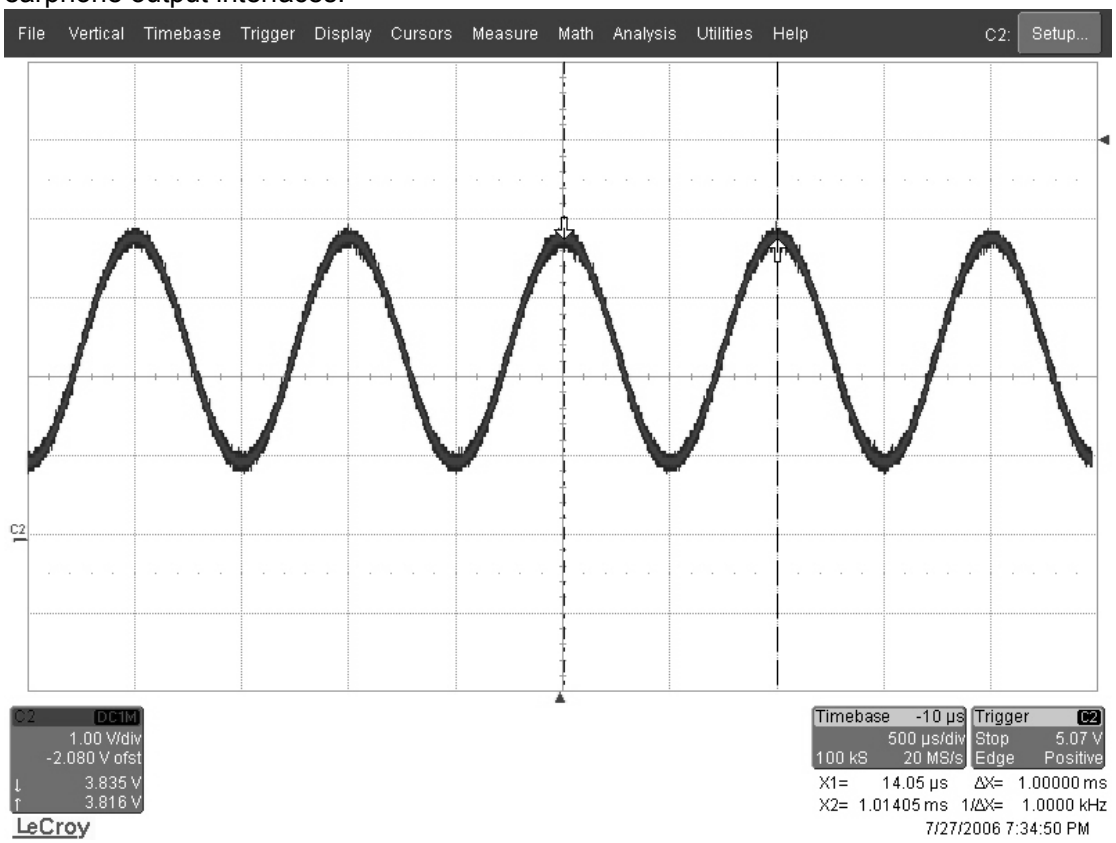
(3) RF inputting color bar signal, clock signal SDA, pin 10 of U9, pin 5 of U3, pin 5 of U12, pin 5 of U16, pin 153 of U1, pin 5 of tuner U15:



(4)RF inputting grey signal, Composite Video Signal waveform at pin 11 of tuner U15, and the waveform at pin 52 of U1（SVP-AX32LF/SVP-AX68LF） is like this:



(7)Inputting sound signal with 1KHz frequency, with the processing of U33 and power amplifier TDA7266DNS, waveform at pin 1, 2, 14, 15 of U33, and waveform at CON4 speaker and CON5 earphone output interfaces:



Chapter 4: Maintenance Procedure and Examples of Typical troubleshooting

1. Failure phenomenon: The picture is normal, but OSD has line in it.
   The reason and the processing: Check the pin of U7 and pin 95-150 of U1 for pseudo soldering, and have pseudo soldering touched up.
2. Failure phenomenon: There is no sound but no picture; there is no OSD when start up, and the back light is bright.
   The reason and processing: Check the connecting line to screen, and have it connect well
3. Failure phenomenon: There are no picture, no sound, and no flower dot in TV mode, but AV is normal.
   The reason and processing: Check the tuner and its peripheral circuits (including bus and power supply). If the peripheral circuits work well but there is no output from tuner, then the tuner must failure.
4. Failure phenomenon: LCD television cannot be controlled (including no starting up with red light on, remote control and local key having no effect, etc).
   The reason and processing: LCD television has crash phenomenon, restart after power off.
5. Failure phenomenon: +5V SB voltage has output, but there are no picture, no sound, and back light and indicating light are not on.
   The reason and processing: Check other groups of voltage; if they have no outputs, then check Flash to find if it is installed well or damaged.

When you meet the following common problems, you might diagnose and get the solutions without contacting with the technicians.

Symptoms	Possible Reason	Solutions
No picture, no sound, and no indicator light on	1.The power cord is not plugged in 2.The power is off	1.Plug the power cord in 2.Turn the power on
Picture and sound with abnormity	1.Contrast, sharpness, and color are set improperly 2.Color system is set improperly 3.Sound system is set improperly	1.Adjust the value of Contrast, sharpness, and color 2.Set the Color system to the country broadcasting standard 3.Set the Sound system to the country broadcasting standard
Picture is spotted or with snow	Signal source is low-grade or the signal cord is in a lower quality	Use the qualified signal cord
No picture, no sound and indicator light is green	Contrast, brightness, color and volume are all in the minimum value or TV is in mute mode.	Adjust the value of contrast, brightness, color and volume
	The signal cable is not correctly connected.	Connect the signal cable correctly
Blue screen, AV or SVIDEO is displayed	There is no signal input or the video cable is not connected or incorrectly connected	Connect the video cable correctly
Picture is unclear or shaking or with black horizontal strips (in VGA mode)	VGA picture is not correctly adjusted.	Enter into “SETUP” menu, select “Auto Tracking” item to perform automatic calibration and adjust “Phase” to solve the problem
VGA picture is not centered		
No sound	There is no audio signal input or audio cable is not connected correctly	Connect the audio cable correctly
VGA picture display with improper color	The color temp is adjusted incorrectly by user	Readjust the color temp, or select the original color setting
HDMI source, with snow pixel of full screen	The source generate is not standard	Plug the HDMI cable again
The remote control does not work	Batteries are improperly installed or exhausted	1.Make sure the positive and the negative polarities are correct. 2.Check if there is a loose contact between the batteries and the springs 3.Replace the batteries

Chapter 5: Spare Part Lists

This listing of maintenance and repair parts are presented for reference only, modification of parameters will not be informed. For accurate models or specifications, please consult the newest data of our company.

Number	Name	Part number	Print plate number	Proportion of easy damage (‰)
1.	Main Board			1
2.	Remote receiving board part			0.5
3.	Keyboard part			0.5
4.	Inner power module	FSP205-4E03 JSK4200-014	Inner power module	5
5.	LCD screen	LG.PHILIPS	LCD screen	0.1
6.	Electronic tuner	AFT7/W003 (IF：38MHz) AFT7/W103 (IF：38.9 MHz) AFT7/W300 (IF：45.75 MHz)	Electronic tuner	0.5
7.	Dynamic speaker	YDT613-A9-10W-8Ω	Dynamic speaker	2
8.	Dynamic speaker	YDG52-A3-10W-8Ω	Dynamic speaker	2
9.	Remote control emitter	GK23J6	Remote control emitter	1

Chapter 6: Factory Setup and notice

1. Enter factory menu

Switch on TV set, and make LCD at operating state:

① Press 【MUTE】 key on remote control;

② Press "MENU" key on remote control, and switch to "SOUND" option with 【V+】,【V-】key;

③ Move cursor to "Balance" option with 【P+】(or【P-】)and【V+】(or【V-】)key to enter setting status;

④ Press number key "3"、"1"、"3"、"8" on remote control to enter password.

Entering factory mode is finished.

If you want to quit facory mode, Pls. press【Power】key to switch off the TV .

(1) Factory menu display is presented like bellow:

chassis：LS02/PS02
SEP 18 10:37:05
Version：ELT-01-Asian-M32-257.25WL
IIC off
Clear EEPROM
Panel Control
Factory Setting
System Control
Min/Max CONTROL
White Balance（Hex）
Hotel Option
Source Select
EnterISP
Channel Table ChangHong

Notes："chassis：LS02/PS02"is the TV chassis number，"Sep 18 10:37:05"is the latest upgrading time for software， and"Version：ELT-01-Asian-M32-257.25WL"is the version number of current software.

(2)The detailed setting items are given bellow:

Contents of first page：

Setting item	Setting content	Setting method	Remark
IIC Off	Stop I^2C bus communication	"OK" or "V+" , "V-" key	Used for updating program
Clear EEPROM	E^2 PROM initialization	Press "OK"key first，then press "V-" key	Only done in first setting station
Panel Control	Screen back light brightness control(or select the panel type)	Press "V+" , "V-" keys to enter submenu	
Factory Setting	Factory Setting	Press "V+" , "V-" keys to enter submenu	
System Control	System Control	Press "V+" key to enter submenu	
Min/Max Control	Analog datum setting of picture and sound	Press "V+" key to enter submenu	Only set sub brightness Bri Mid
White Balance	White balance parameters setting	Press "V+" key to enter submenu	
Hotel Option	Hotel mode	Press "V+" key to enter submenu	Used for hotel TV
Source Select			
EnterISP			

Channel Table	ChangHong		
Exit Menu			

Use 【P+】and 【P-】keys on remote control to make up or down option, and use【V+】and【V-】keys to set.

Contents of sub pages：

Panel Control

Setting item	Setting value	Remark
LVDS Mapping	0x09	Polarity of LVDS signal
SSC	Off	
SSCDELTA	00	

Factory Setting

Setting item	Setting value	Remark
Model Type	Asian(Europe)	
Tuner Select	Asian Tuner(Eu Tuner)	
Sound system	BG(I,,DK,L,M)	
AutoDetsoundSys	On(Off)	
overmodulation	On(Off)	
IIR	Big/Small	
Factory Out	>>	Output the factory settings

System Control

Setting item	Setting value	Remark
Default Lang	English	Default OSD language
EQ Enable	On(Off)	
Aging Mode	On(Off)	
Logo	On(Off)	
TV_ANSTEREOSYS	01	
TV_DISSTEREOSYS_FM	04	
TV_DISSTEREOSYS	01	
TV_DIDUALSYS_FM	04	
TV_DIDUALSYS	06	
TV_FMSYS	02	
HDMI_I2CSYS	83	
OTHER_LRSYS	C1	

Min/Max Control

Setting item	Setting value	Setting item	Setting value
Con Min	30H	Vol Min	00H
Con Mid	70H	Vol Mid 1	01H
Con Max	A2H	Vol Mid 2	14H
Bri Min	00H	Vol Mid 3	28H
Bri Mid	88H	Vol Mid 4	4BH
Bri Max	A2H	Vol Max	64H
Col Min	00H	Tre Min	00H
Col Mid	40H	Tre Mid	30H
Col Max	70H	Tre Max	60H

Tnt Min	20H	Bas Min	00H
Tnt Mid	80H	Bas Mid	30H
Tnt Max	E0H	Bas Max	60H
Shp Min	00H		
Shp Mid	60H		
Shp Max	A0H		

White Balance

Normal		Warm	
R Gain	7DH	R Gain	7DH
G Gain	80H	G Gain	80H
B Gain	9AH	B Gain	9AH
R Offset	80H	R Offset	84H
G Offset	80H	G Offset	80H
B Offset	74H	B Offset	74H
Cool			
R Gain	7DH		
G Gain	80H		
B Gain	9AH		
R Offset	80H		
G Offset	80H		
B Offset	90H		

Hotel Option

Setting item	Setting value	Remark
Hotel Enable	ON	Hotel mode presetting（On——users can enter into Hotel mode，Off——users can't enter into Hotel mode）

Source Select

TV	ON	SVIDEO2	OFF
AV1	ON	SVIDEO3	OFF
AV2	ON	COMP1	ON
AV3	ON	COMP2	ON
SCART1	OFF	COMP3	OFF
SCART2AV	OFF	PC	ON
SCART2YC	OFF	HDMI1	ON
SCARTAV3	OFF	HDMI2	ON
SVIDEO	ON	YCBCR	OFF

EnterISP

Enter software upgrading mode.

Channel Table

Presetting TV channel ,only for factory test.

Exit Menu

Notes：

A. In "Min/Max CONTROL" setting item, "Bri Mid" item is used to set sub-brightness of picture;

B. White balance needs to be set in “Normal” mode;
C. Set CLEAR E^2PROM will clear the memory data, So do not set it unless it is needed; other setting items do not need setting.

2. Setting method of factory menu

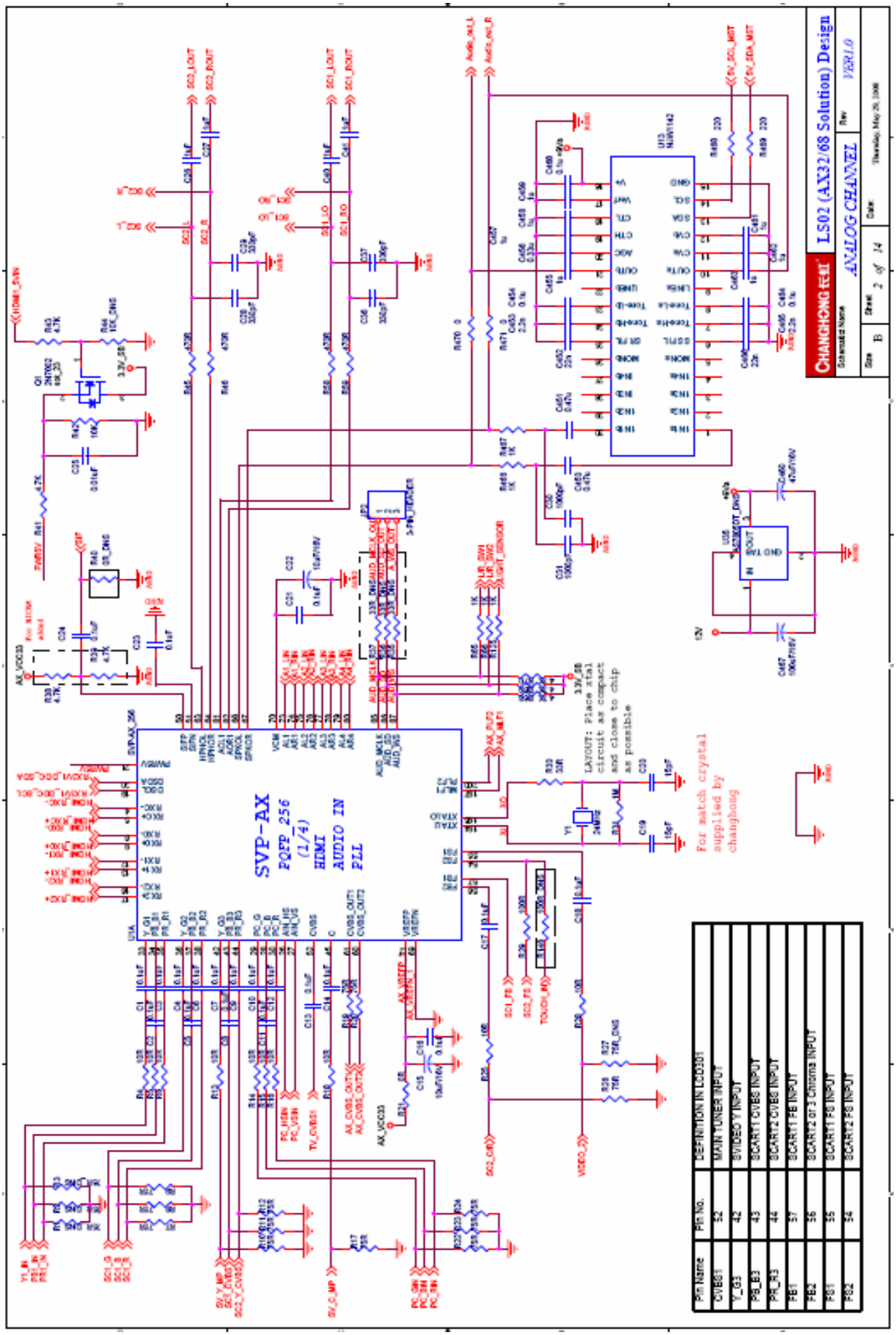
(1) Choose setting item

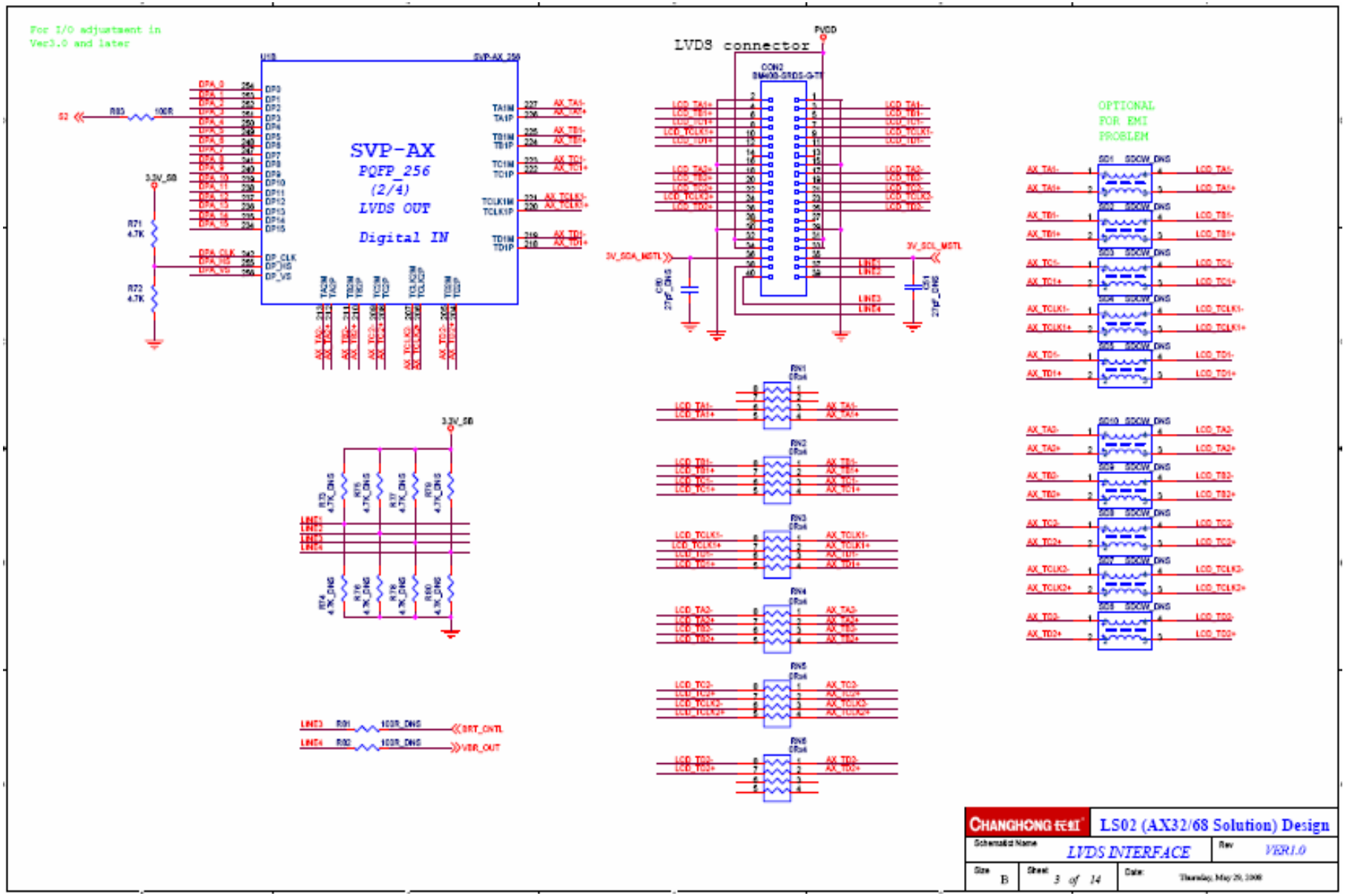
Operators can choose setting item orderly with【P+】and【P-】key, font having background display represents the item has been chosen. Press【V+】key to enter sub directory. Use 【P+】and 【P-】keys on remote control to make up or down option, and use【V+】and 【V-】keys to set.

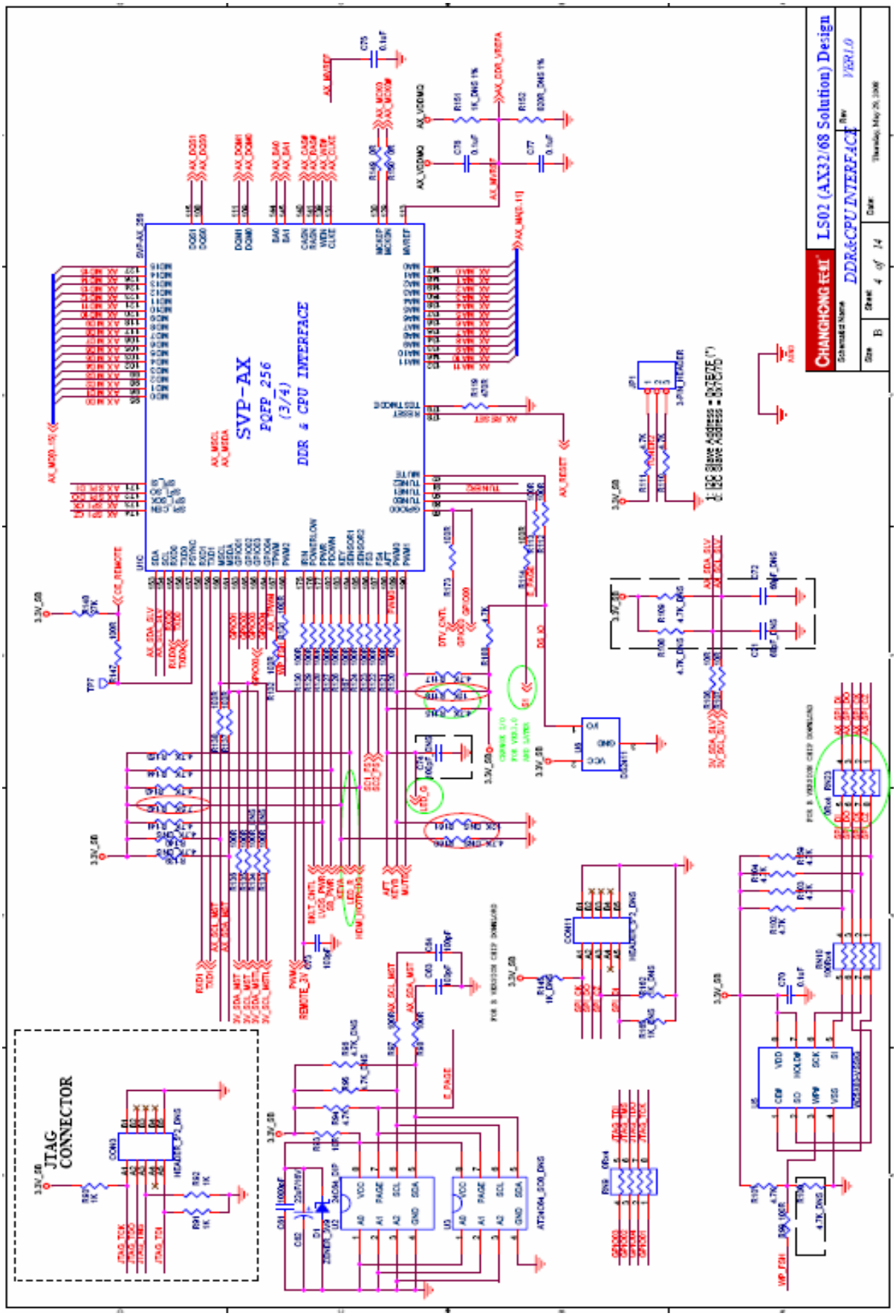
(2)All the menu functions are opened in factory mode, item checking and effect testing can be done by using menu if it is needed.

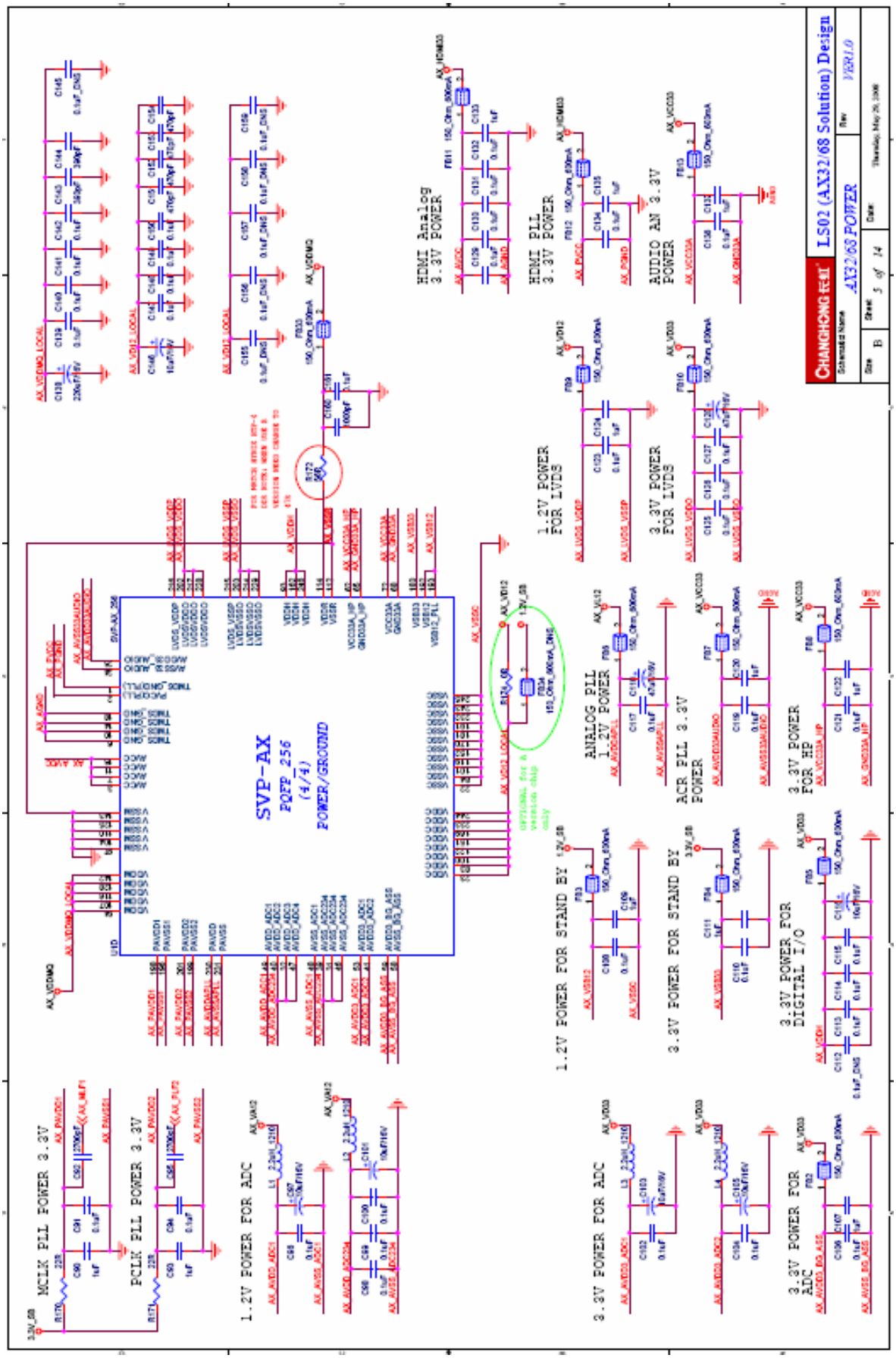
(3)Switching TV signal in factory mode can be done by directly pressing the number key. Press【MENU】key to back to the parent of working directory, press【DISPLAY】key to quit factory mode.

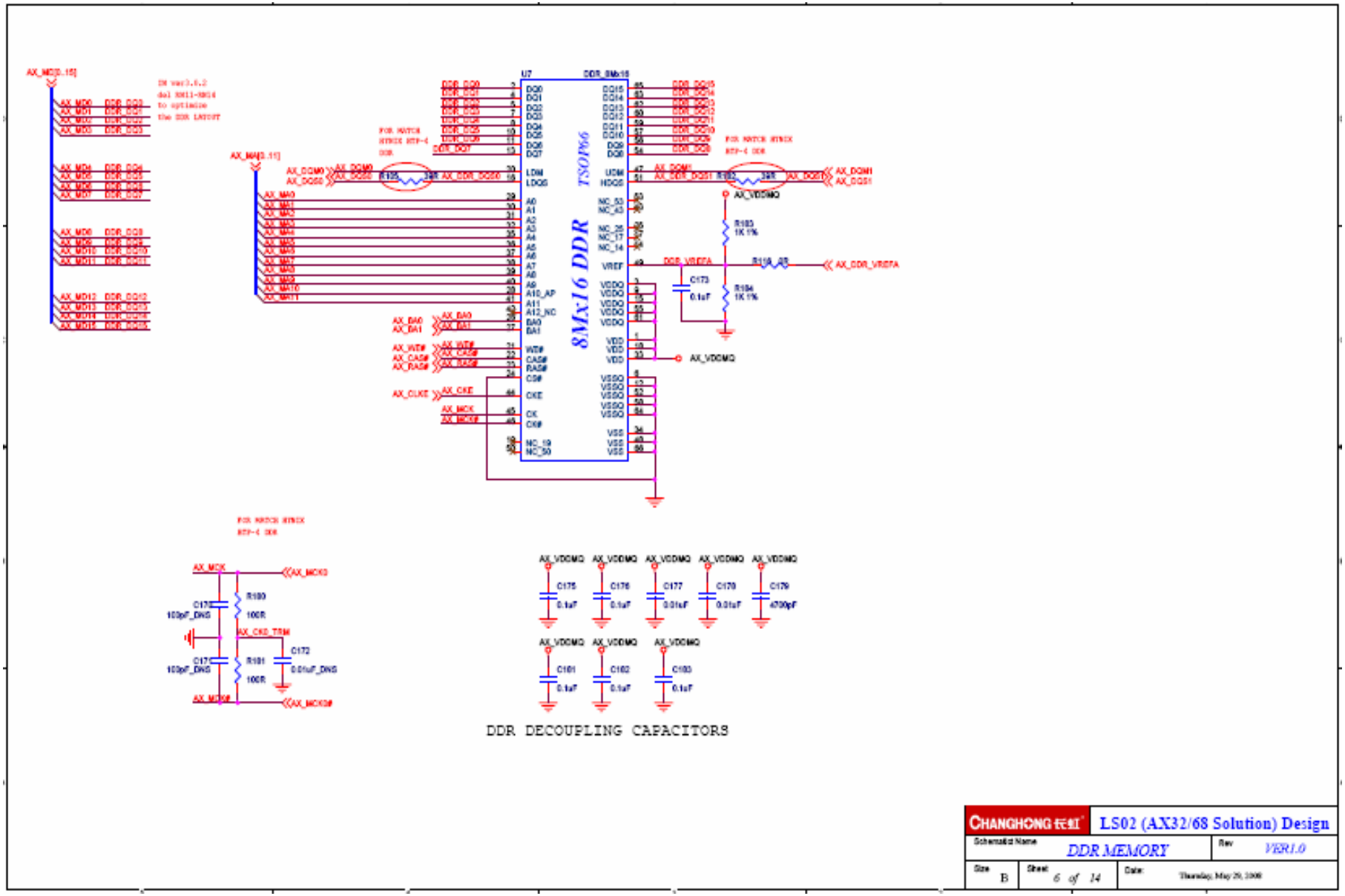
Appendix ： LS02/PS02 module Circuit Schematic Diagram

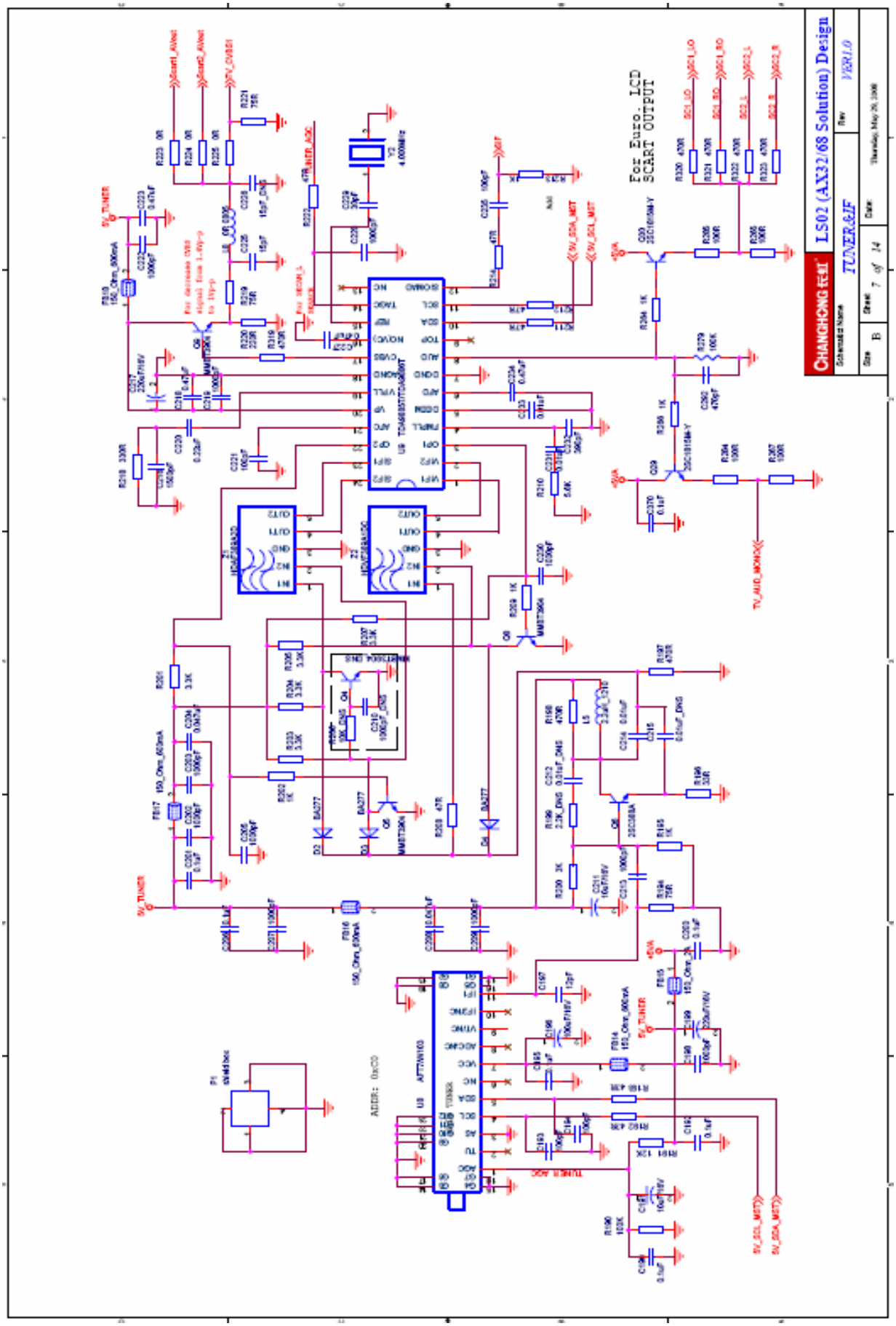


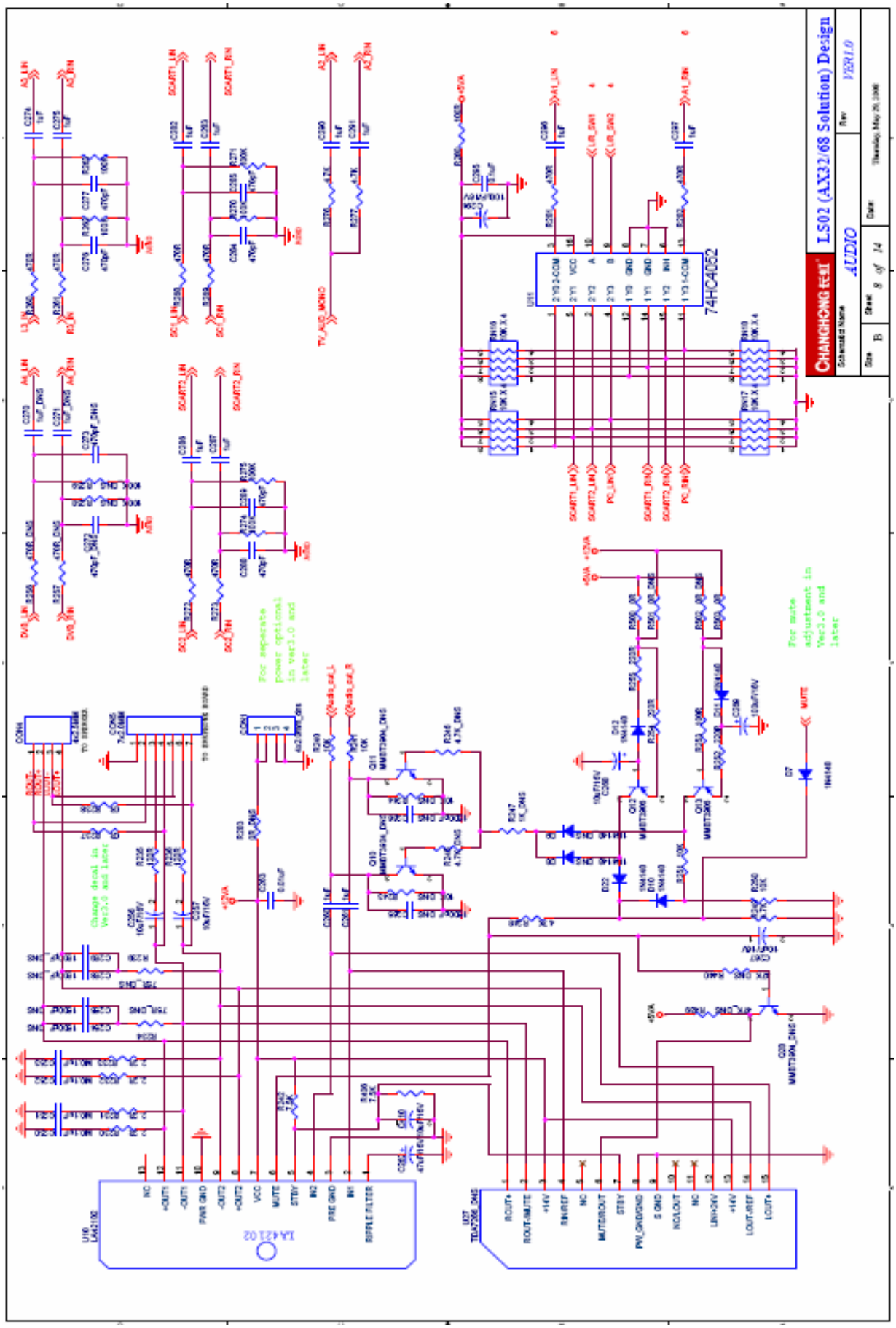

For I/O adjustment in Ver3.0 and later
SVP-AX
PQFP_256
(2/4)
LVDS OUT
Digital IN
LVDS connector
OPTIONAL FOR EMI PROBLEM
CHANGHONG 长虹
LS02 (AX32/68 Solution) Design
Schematic Name
LVDS INTERFACE
Rev
VER1.0
Size
B
Sheet
3 of 14
Date:
Thursday, May 29, 2008

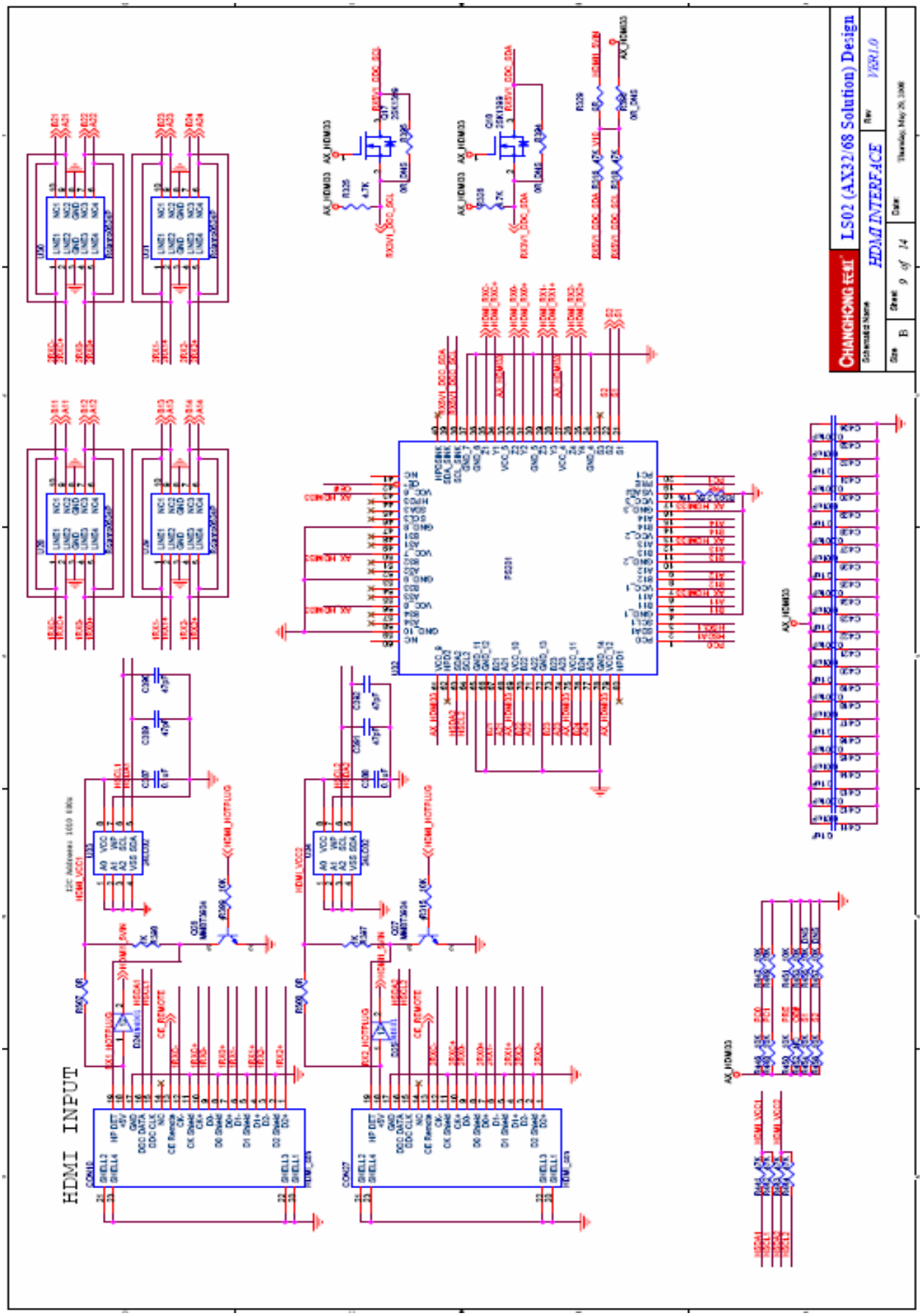

SVP-AX
PQFP_256
(3/4)
DDR & CPU INTERFACE
JTAG
CONNECTOR
LS02 (AX32/68 Solution) Design
DDR&CPU INTERFACE
CHANGHONG ELE

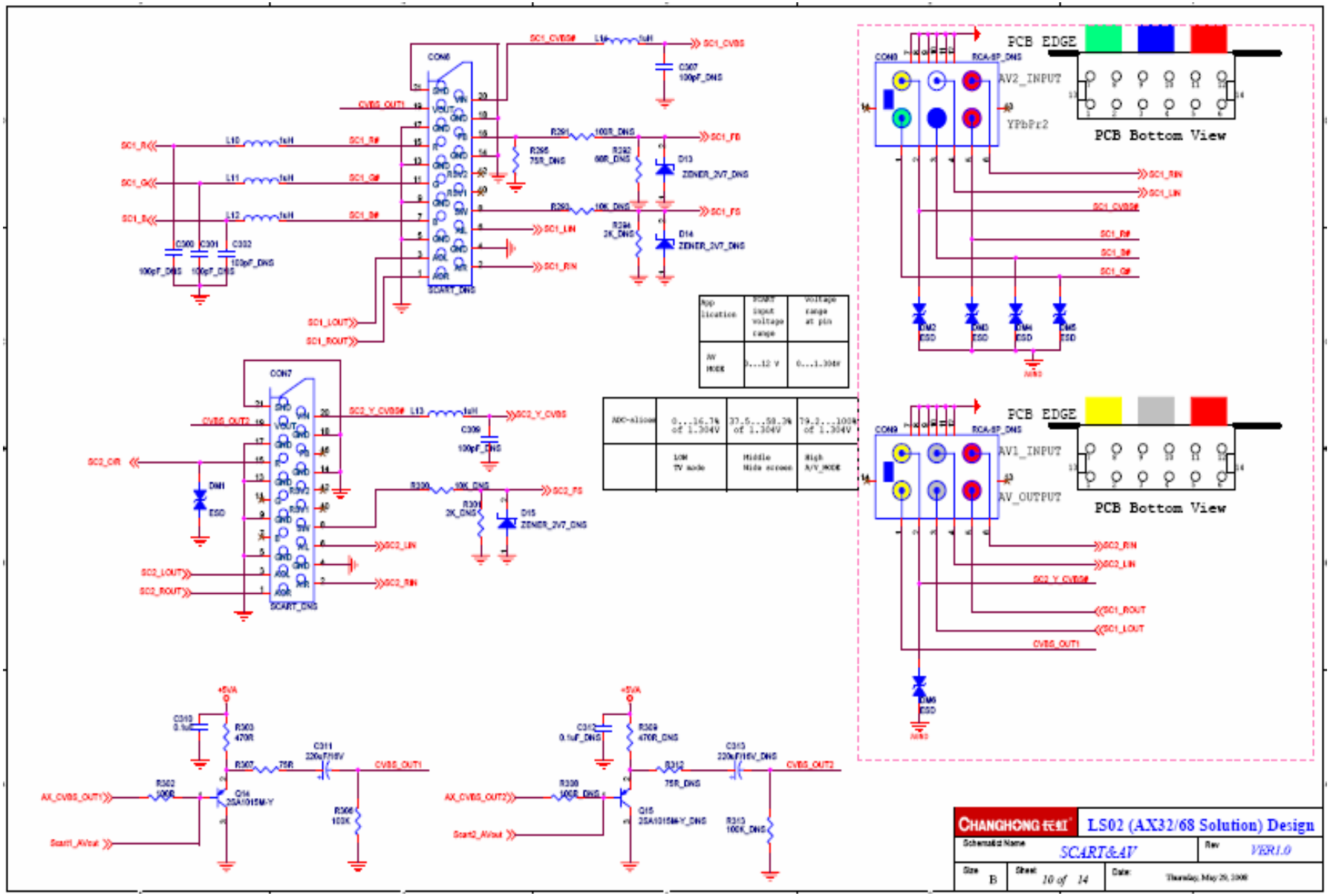

SVP-AX
PQFP 256
(4/4)
POWER/GROUND
MCLK PLL POWER 3.3V
PCLK PLL POWER 3.3V
1.2V POWER FOR ADC
3.3V POWER FOR ADC
1.2V POWER FOR STAND BY
3.3V POWER FOR STAND BY
3.3V POWER FOR DIGITAL I/O
3.3V POWER FOR ADC
3.3V POWER FOR HP
ANALOG PLL 1.2V POWER
ACR PLL 3.3V POWER
1.2V POWER FOR LVDS
3.3V POWER FOR LVDS
HDMI Analog 3.3V POWER
HDMI PLL 3.3V POWER
AUDIO AM 3.3V POWER
CHANGHONG ELEC
LS02 (AX32/68 Solution) Design
AX32/68 POWER
VER1.0


8Mx16 DDR
TSOP66
U7
DDR_8Mx16
AX_MD[0..15]
AX_MA[0..11]
AX_VDDMQ
AX_DDR_VREFA
DDR_VREFA
AX_BA0
AX_BA1
AX_WE#
AX_CAS#
AX_RAS#
AX_CKE
AX_MCK
AX_MCK#
AX_CKE_TRM
AX_MCK0
AX_MCK0#
DDR DECOUPLING CAPACITORS
CHANGHONG 长虹
LS02 (AX32/68 Solution) Design
Schematic Name
DDR MEMORY
Rev
VER1.0
Size
B
Sheet
6 of 14
Date:


LS02 (AX32/68 Solution) Design
TUNER-IF
Rev
V0R1.0
Sheet
7 of 14
Date:
Thursday, May 29, 2008
For Euro. LCD
SCART OUTPUT
5V_TUNER
+5VA
TV_AUDIO_MONO
5V_SCL_MST
5V_SDA_MST
SCL_LO
SCL_RO
SCL_L
SCL_R
IF
TUNER_AGC
ADDR: 0xC0


LS02 (AX32/68 Solution) Design
AUDIO
CHANGHONG
74HC4052
TDA7266_DMS
LA42102
For separate power optional in Ver3.0 and later
For mute adjustment in Ver3.0 and later
Change decal in Ver3.0 and later


HDMI INPUT
CHANGHONG ELE
LS02 (AX32/68 Solution) Design
HDMI INTERFACE
VER1.0



App lication	SCART input voltage range	Voltage range at pin
AV MODE	0...12 V	0...1.304V

ADC-slicer	0...16.7% of 1.304V	37.5...58.3% of 1.304V	79.2...100% of 1.304V
	LOW TV mode	Middle Wide screen	High A/V_MODE

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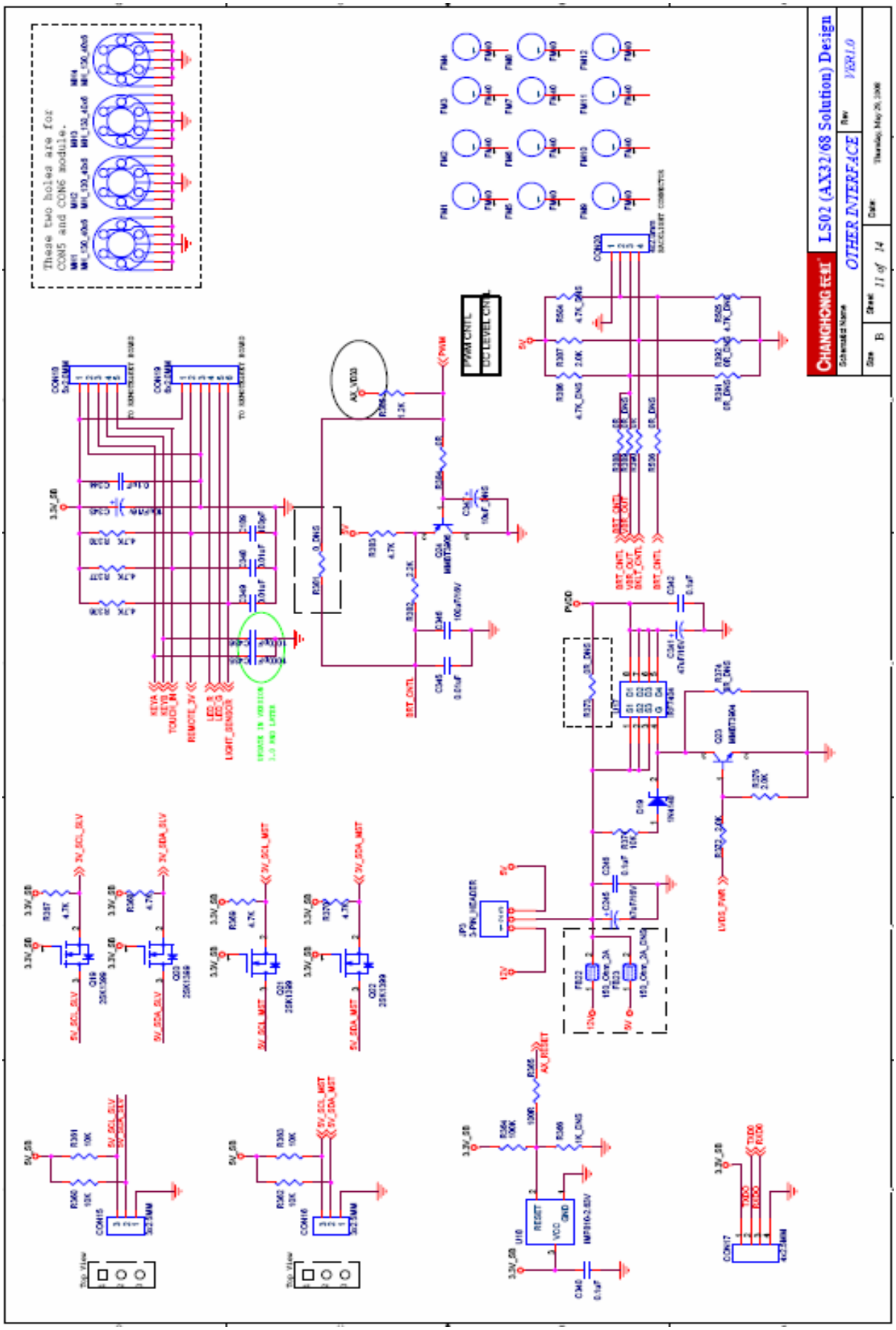
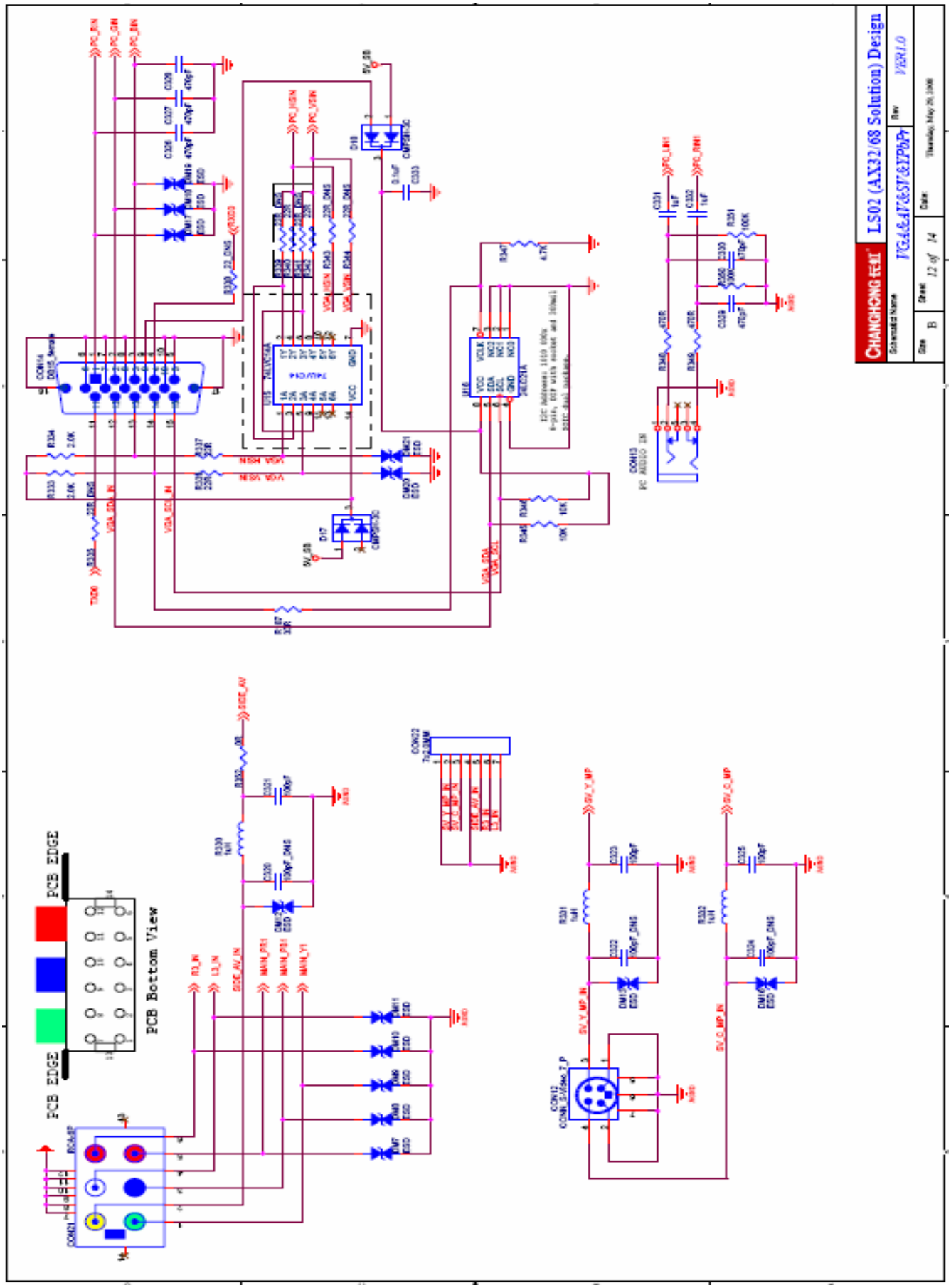
LS02 (AX32/68 Solution) Design

Schematic Name	SCART&AV	Rev	VER1.0
Size B	Sheet 10 of 14	Date: Thursday, May 29, 2008	


These two holes are for CON5 and CON6 module.
CHANGHONG ELEC
LS02 (AX32/68 Solution) Design
OTHER INTERFACE
VER1.0
Sheet 11 of 14
Thursday, May 29, 2008


CHANGHONG
LS02 (AX32/68 Solution) Design
PCB EDGE
PCB Bottom View
PCB EDGE