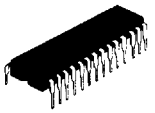
LC7523, 7523M

SANYO SEMICONDUCTOR CORP



3029A

3073A

CMOS LSI

Electronic Volume Control for Graphic Equalizer

Functions

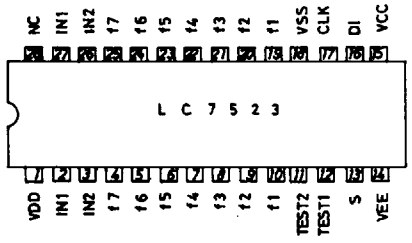
- On-chip electronic volume control for graphic equalizer with 7 bands each of right/left.
- 2dB/step variable in each band.
- Max. boost of +12dB, max. cut of −12dB, and 13 positions in each band.
- Simultaneous drive of right/left band.
- Band setting by serial data input. 2 control lines
- CMOS LSI of 12V breakdown voltage.

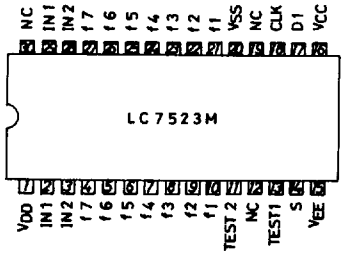
Features

By using 3 chips of the LC7523 (or LC7523M), a controller (LC7060 or general-purpose microcomputer LC6502C), and a display LSI (LC7560→LCD, LC7565→FLT, LED), an electronic graphic equalizer system with the following features can be formed.

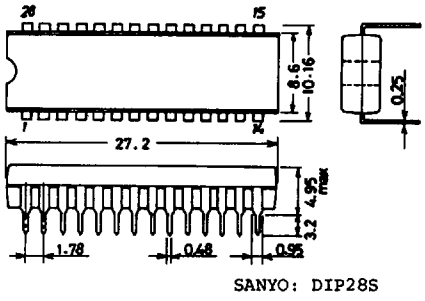
- The gain in each band can be increased/decreased with one touch.
- Since the preset memory contents can be called with one touch, your desired frequency characteristic to the music can be selected.
  (Example) User option 2 modes + maker option 3 modes + last channel memory
- '0dB in each band (flat function)', 'The frequency characteristic in each band is reversed with respect to 0dB (reverse function)'. — These functions can be software-controlled with one touch.
- Spectrum analyzing display can be used to provide recording equalization easily.
- Since 2 control lines can be also used for a display LSI, wiring between microcomputer and LSI is facilitated.
- The package is available in two types : shrink package DIP28 and miniflat package MFP30.

Pin Assignment



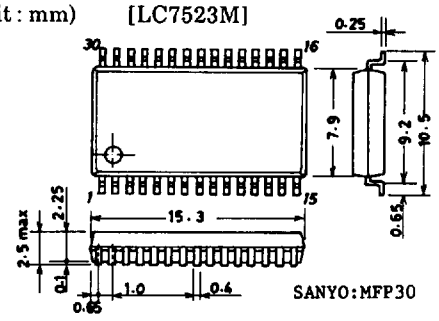


Case Outline 3029A
(unit : mm) [LC7523]



SANYO: DIP28S

Case Outline 3073A
(unit : mm) [LC7523M]



SANYO:MFP30

Absolute Maximum Ratings at Ta = 25°C, V_{SS} = 0V

				unit
Maximum Supply Voltage	V_{DD}-V_{EE} max	V_{DD}, V_{EE}, *1	12	V
	V_{CC} max	V_{CC}, *1	V_{SS} − 0.3 to V_{CC} + 7	V
Maximum Input Voltage	V_I 1	CLK, DI	V_{SS} − 0.3 to V_{CC} + 0.3	V
	V_I 2	f1 to f7, IN1, IN2, S, TEST1	V_{EE} − 0.3 to V_{DD} + 0.3	V
Allowable Power Dissipation	Pd max	Ta ≦ 75°C	200	mW
Operating Temperature	Topg		−30 to +75	°C
Storage Temperature	Tstg	*2	−40 to +125	°C

Recommended Operating Conditions at Ta = 25°C, V_{SS} = V_{EE} = 0V

				unit
Supply Voltage	V_{DD}	V_{DD}	8.0	V
	V_{EE}	V_{EE}	0	V
	V_{CC}	V_{CC}	5.0	V

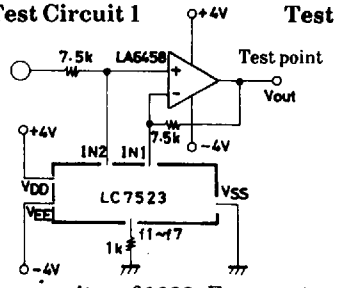
Allowable Operating Conditions at Ta = 25°C, V_{SS} = 0V

				unit
Supply Voltage	V_{DD}-V_{EE}	V_{DD}, V_{EE},	4.5 to 11.0	V
	V_{CC}	V_{CC}	4.0 to 5.5	V
Input 'H'-Level Voltage	V_{IH} 1	CLK, DI, *3	0.8V_{CC} to V_{CC}	V
	V_{IH} 2	S	0.9 (V_{DD} − V_{EE}) + V_{EE} to V_{DD}	V
	V_{IH} 3	IN1, IN2, f1 to f7	up to V_{DD}	Vp
Input 'L'-Level Voltage	V_{IL} 1	CLK, DI	0.2V_{CC}	V
	V_{IL} 2	S, TEST1	V_{EE} to 0.1 (V_{DD} − V_{EE}) + V_{EE}	V
	V_{IL} 3	IN1, IN2, f1 to f7	V_{EE} or more	Vp
Input Pulse Width	$t_{\phi w}$	CLK	1 or more	μs
Setup Time	t_{setup}	DI	1 or more	μs
Hold Time	t_{hold}	DI	1 or more	μs
Operating Frequency	f_{opg}	CLK	up to 330	kHz

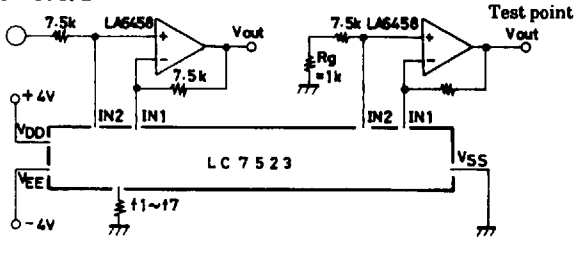
Electrical Characteristics at Ta = 25°C

			min	typ	max	unit
Total Harmonic Distortion	THD1	Test Circuit 1, Vout = 1V, flat mode, f = 20kHz		0.005	0.010	%
	THD2	Test Circuit 1, Vout = 1V, flat mode, f = 1kHz		0.0015	0.003	%
	THD3	Test Circuit 1, Vout = 1V, boost mode, f = 20kHz		0.04	0.10	%
	THD4	Test Circuit 1, Vout = 1V, boost mode, f = 1kHz		0.04	0.10	%
Crosstalk	CT	Test Circuit 2, f = 20kHz, Vout = 1V	55			dB
Current Dissipation	I_{DD}	V_{DD} − V_{EE} = 10V			1	mA
	I_{CC}	V_{CC} = 5V			1	mA
Analog SW OFF Leak Current	I_{off}	f1 to f7			10	μA

Test Circuit 1



Test Circuit 2

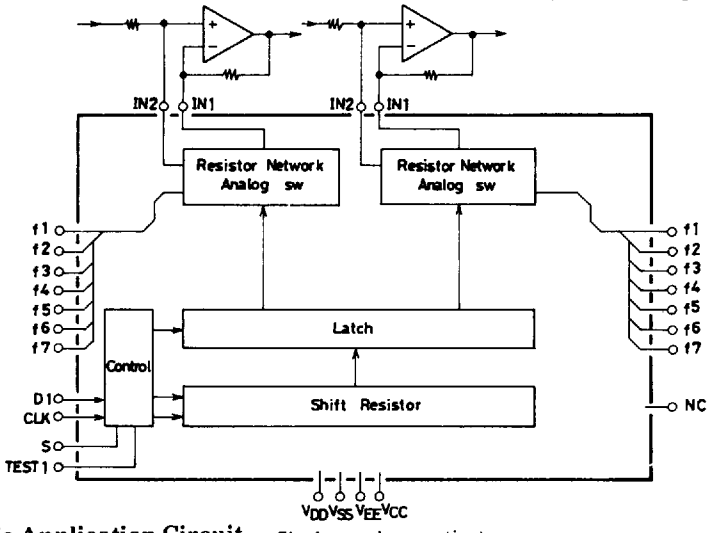


*1 : Connect a capacitor of 1000pF or greater across each power supply pin and V_{SS} pin.

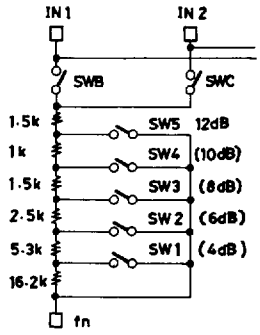
*2 : When mounting the MFP package on the board, do not dip it in solder.

*3 : When the control signal on the microcomputer side rises earlier than V_{DD} on the LC7523, connect a resistor of 2kΩ or greater halfway through DI, CLK lines.

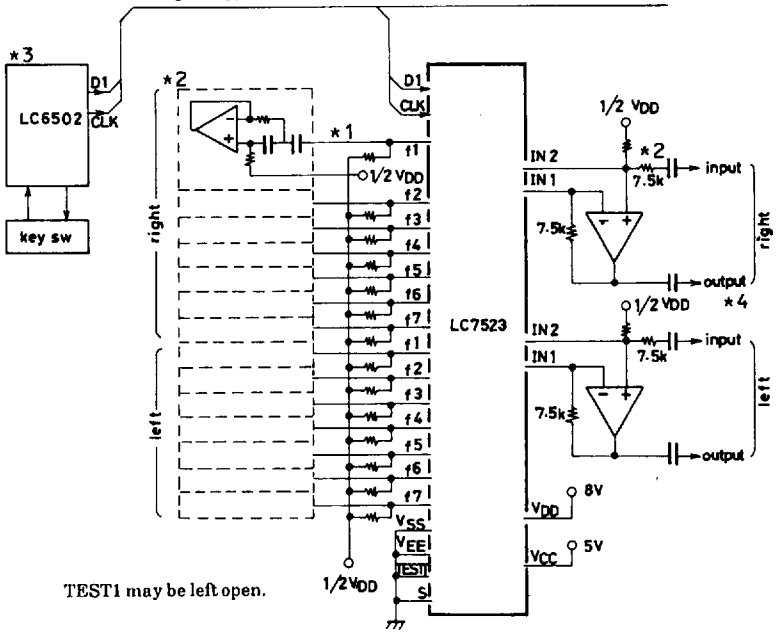
Equivalent Circuit Block Diagram



Resistance Equivalent Circuit (for one band)



Sample Application Circuit (Single-supply operation)



TEST1 may be left open.

*1 : It is recommended that $1/2V_{DD}$ is applied to pins f1 to f7 through resistors of 1MΩ so that noise is minimized at the select mode.

*2 : The optimum conditions for 2dB/step are as follows :
V_{DD} = 8V, feedback resistance of OP amp : 7.5kΩ, equivalent LC resonance impedance : 1kΩ
(For V_{DD} = 14V, the LC7522 is recommended.)

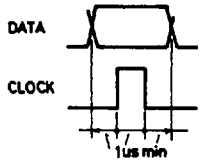
*3 : The LC7060 is available as a standard controller.

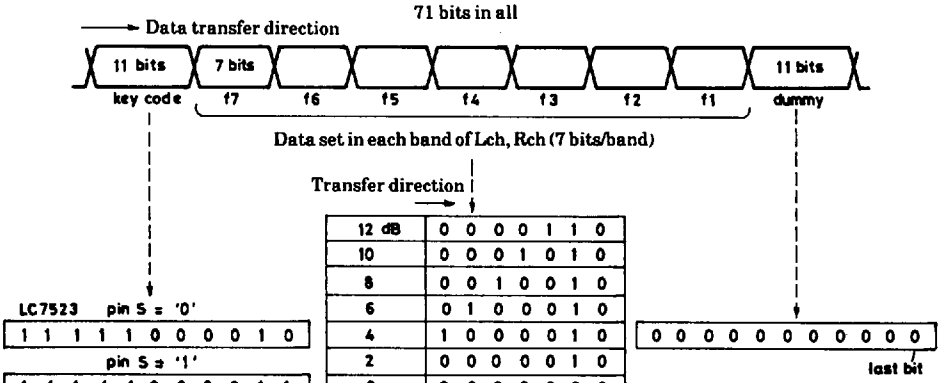
*4 : The LC7560 (LCD driver), LC7565 (FLT, LED driver) are available as spectrum analyzing display drivers for graphic equalizer output signal.

Data Code

Note 1. When power is applied, data '0' must be first transferred for 60 clocks (initial clock) or more. If data transfer is stopped halfway, the transfer of the remaining data must be completed or data transfer must be started after the initial clocks have been transferred.

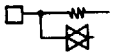
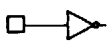
Note 2. When the DI, CLK pins are shared with the LC7560, etc., the maximum initial clocks for such device must be transferred.





12 dB	0 0 0 0 1 1 0
10	0 0 0 1 0 1 0
8	0 0 1 0 0 1 0
6	0 1 0 0 0 1 0
4	1 0 0 0 0 1 0
2	0 0 0 0 0 1 0
0	0 0 0 0 0 0 0
-2	0 0 0 0 0 0 1
-4	1 0 0 0 0 0 1
-6	0 1 0 0 0 0 1
-8	0 0 1 0 0 0 1
-10	0 0 0 1 0 0 1
-12	0 0 0 0 1 0 1

Pin Description

Pin Name	Pin Configuration	Description
V_{DD}		Power supply pin. Power supply for audio signal.
V_{SS}		Power supply pin. 0V.
V_{EE}		Power supply pin. Power supply for audio signal, connected to V_{SS} at single-supply operation.
V_{CC}		Power supply pin. +5V typ. Must not rise earlier than V_{DD}.
DI		Used to input data from CPU. Schmitt inverter type.
CLK		Used to input clock from CPU. Schmitt inverter type.
IN1		Audio signal input pin. Normally, IN1 is connected to inverting input of OP amp.
IN2		Normally, IN2 is connected to noninverting input of OP amp. Provided in Lch/Rch.
f1 to f7		Band filter connecting pin. f1 to f7 × 2(right/left) = 14 (total) pins.
S		Select pin at 2-chip used mode. To accept data under key code 7C3, S must be set to '1'.→Connected to V_{DD}. To accept data under key code 7C2, S must be set to '0'.→Connected to V_{EE}.
TEST1		IC test pin. Left open or connected to V_{EE}.
TEST2		May be left open during operation or connected to V_{SS} through a resistor of 1MΩ.
NC		No connection pin. Nothing must be connected to this pin.