SANYO

COLOUR TELEVISION
TRAINING MANUAL

A3-A CHASSIS

A3-A CHASSIS CIRCUIT ANALYSIS

CPU	:M34300N4-622SP
Band Switch	:LA7910
System switch	:LA7910
VIF/Chroma	:LA7681
Vertical Out	:LA7837
Power Supply Circuit	

REFERENCE NO.WM-520082

<Contents>

[Part 1 CPU and V/S Tuning]

1.System Outline

The system employs a CPU developed for the A3 chassis (VIF/SIF/CHROMA/DEF-ONE CHIP IC) with the following functions.

1-1 CPU and Main ICs

CPU : M34300N4-622SP MITSUBISHI
CMOS
ROM 4K bytes
CRT character display (16 characters × 2 rows)
EEPROM (128 × 8 bits)
Dual in line -42s

Band switching : LA7910 SANYO
System switching : LA7910 SANYO

1-2 Features

(1) 32-programme function (AV position × 3)
(2) Tuning band switching (3 bands or UHF only)
(3) Manual tuning preset
(4) Fine tuning
(5) Teletext control
(6) Analogue control (colour,volume,brightness,contrast,memory)
(7) TV/AV switching
(8) Mute
(9) Off-timer
(10) 48-function remote control
(11) On-screen display
(Programme number, AV,analogue control data, off-timer,etc.)
(12) Special functions

Fig.1 shows a block diagram of CPU peripheral circuits

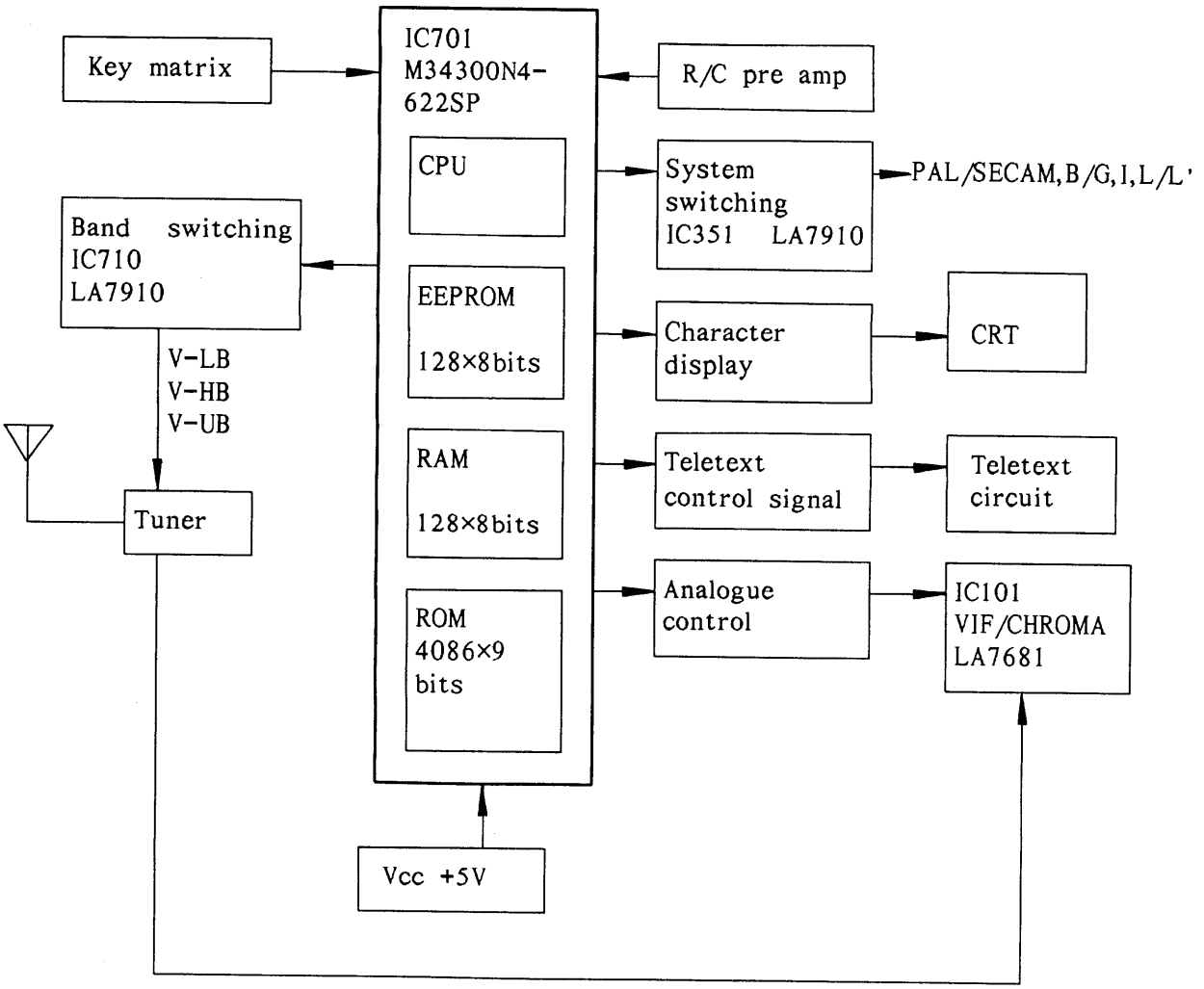


Fig.1 CPU peripheral circuits

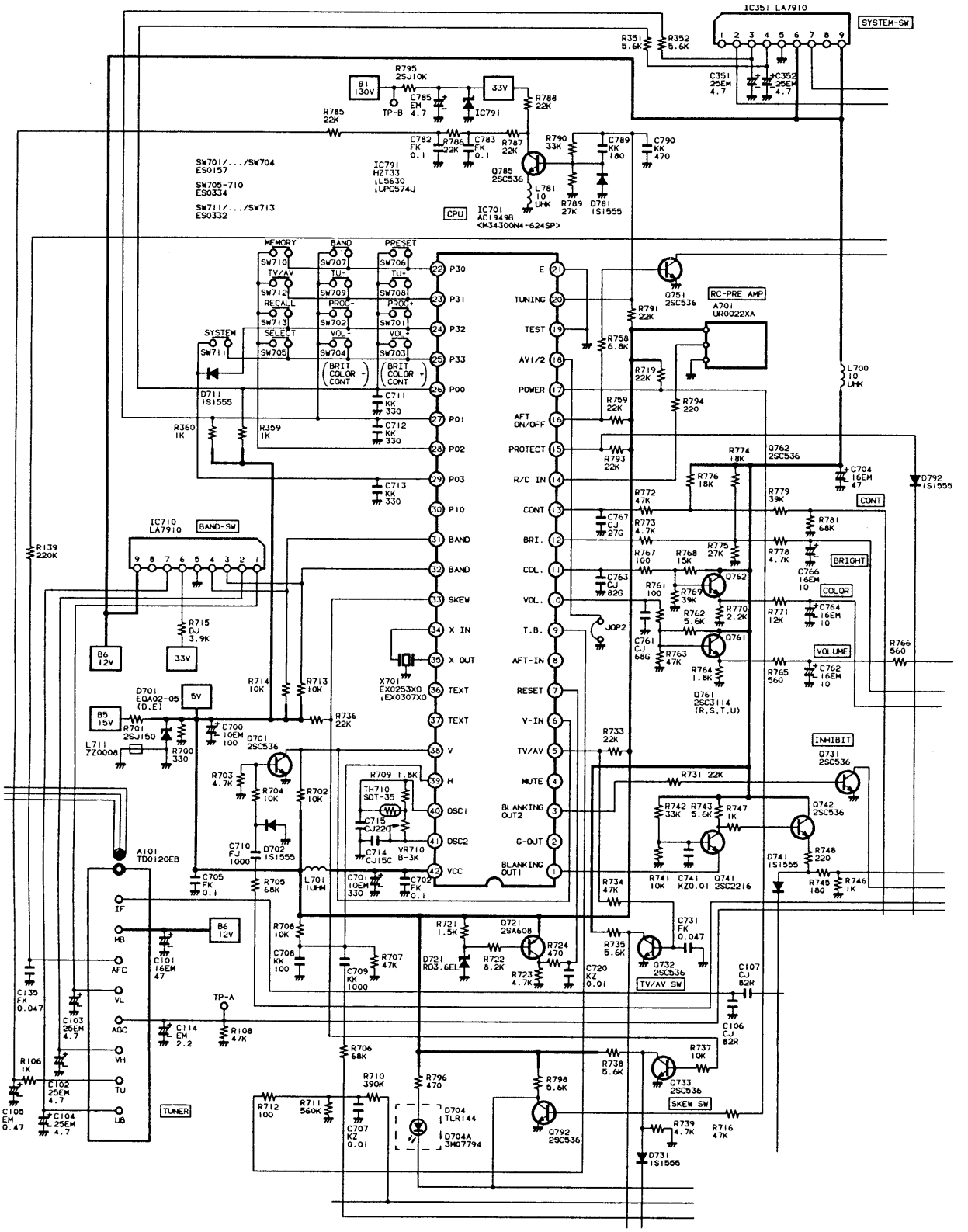


Fig.2 Schematic diagram of CPU

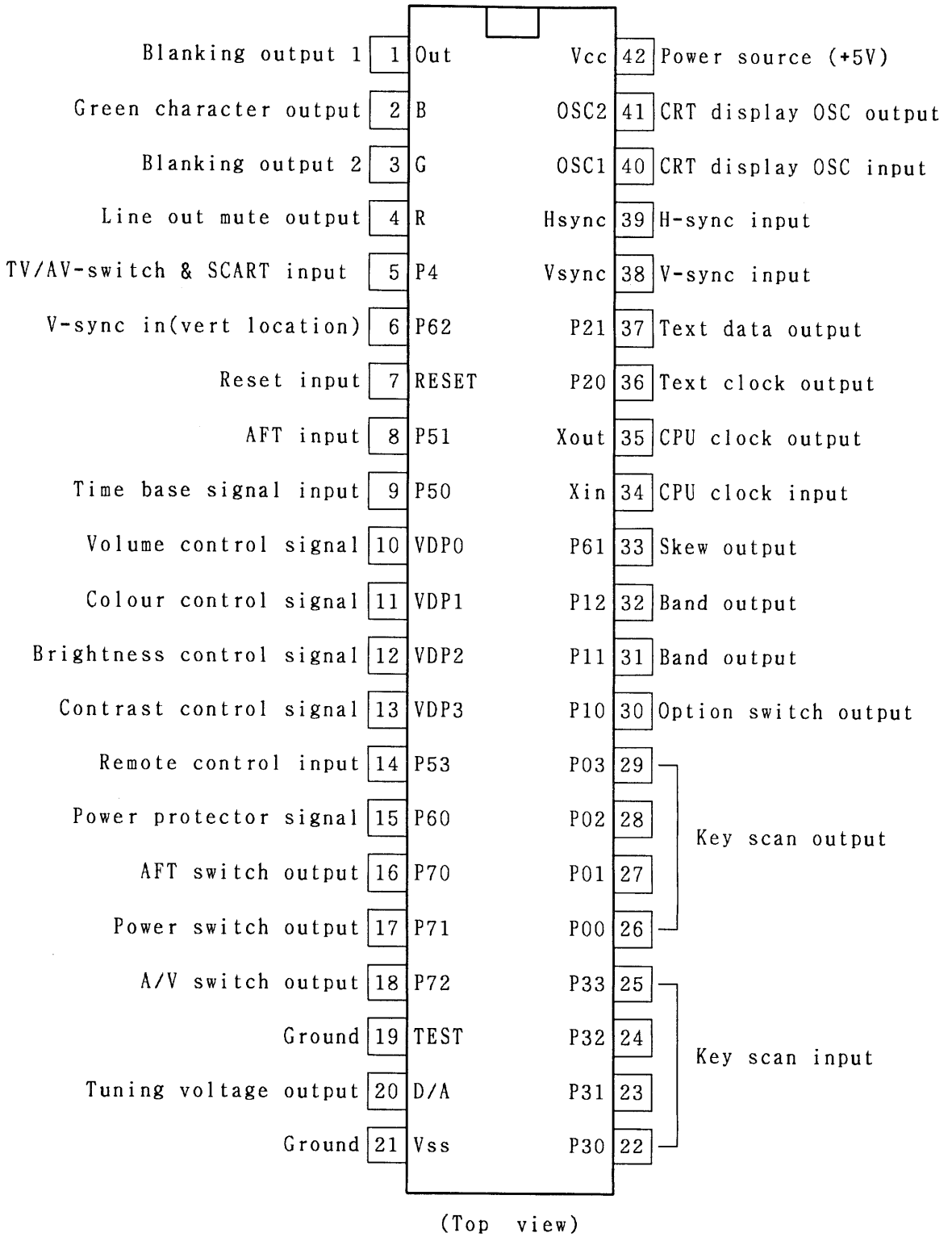


Fig.3 CPU M34300N4-622SP pin allotment

CPU pin descriptions

Pin No.	Function	Description	Note
1	CRT display blanking-out-1 output	H:active	H:>2.4V L:<0.4V
2	CRT display green character signal output	H:active	H:>2.4V L:<0.4V
3	CRT display blanking-out-2 output	H:active	H:>2.4V L:<0.4V
4	Line out mute output	H:mute ON L:mute OFF	H:>2.4V L:<0.4V
5	TV/AV switch & SCART input	Out H:TV,AV2 mode L:AV1 mode In H:SCART in,no L:SCART in,yes	H>2.4V or $0.7V_{DD}$ L<0.4V or $0.4V_{DD}$
6	Vertical sync signal input		H:>$0.7V_{DD}$ L:<$0.4V_{DD}$
7	Reset input	L:active	H:>$0.9V_{DD}$ L:<$0.4V_{DD}$
8	AFT signal input		H:>$0.7V_{DD}$ L:<$0.4V_{DD}$
9	Time base signal	H: Time base signal:yes L: Time base signal:no	H:>$0.9V_{DD}$ L:<$0.4V_{DD}$
10	Volume control output	H:active	L<0.4V
11	Colour control output	H:active	L<0.4V
12	Brightness control output	H:active	L<0.4V
13	Contrast control output	H:active	L<0.4V
14	Remote control input	L:active	H:>$0.7V_{DD}$ L:<$0.4V_{DD}$
15	Abnormal power source signal input	H:abnormal L:normal (Note 1)	H:>$0.7V_{DD}$ L:<$0.4V_{DD}$
16	AFT switch signal output	H:AFT ON L:AFT OFF	H:>$0.7V_{DD}$ L:<$0.4V_{DD}$
17	Power switch output & R/C switch input	Out H:Power OFF L:Power ON In H:R/C L:without R/C	H:>2.4V L:<0.4V or $0.4V_{DD}$
18	AV switch	In H:AV-1 L:AV-2 Out H:TV,AV-1 mode L:AV-2 mode	H:>2.4V L:<0.4V or $0.4V_{DD}$
19	Test terminal		Connected to GND
20	Tuning voltage out	L: active 14 bits PWM output	H:>2.4V, L:0.4V
21	Vss	Ground	

Note 1: When "L" is maintained for 1.2 seconds, power is switched off.

Pin No.	Function	Description	Note
22 23 24 25	Key switch input	L:active	H>0.7V_{DD} L<0.4V_{DD}
26 27	Key switch scan out & system switch out	L:active System switch : See Note 2	L<3V
28 29	Key switch scan out	L:active	
30 31 32	Option switch output Tuning band output	L:active See Note 3	L<3V
33	Skew output	H:OFF L:ON	L<0.4V_{DD}
34 35	CPU clock input CPU clock output		4 MHz ceramic OSC
36	Text control output	Clock output	H:>2.4V L:<0.4V
37	Text control output	Data output	H:>2.4V L:<0.4V
38 39	CRT display vertical sync signal CRT display horizontal sync signal	L: active	H:>2.4V L:<0.4V
40 41	CRT display OSC input CRT display OSC output		5 MHz OSC
42	V_{DD}		4.5V~5.5V

< Note 2 : System switching >

System	French systems				4-system			
	L'	L	B/G	I	3-system			
Switch	S-1	S-1	S-2	S-3	S-1	S-2	S-3	S-4
Pin 26	L	L	H	H	L	L	H	H
Pin 2	L	H	L	H	L	H	L	H

<Note 3 : Band switching output>

	Band		
	V_L	V_H	UHF
Pin 31	L	L	H
Pin 32	L	H	L

2.Key Input Circuit

This circuit sends the timing signal output from pins 26 to 29 of the CPU to pins 22 to pin 25. Fig.4 shows the key input circuit.
When a key is pressed, key scan signals are sent to either of pins 22 to pin 25. The CPU decodes the input key scan signal, judges which key was pressed, and then performs the operation that corresponds to that key scan signal.
As shown in Fig.5, an option switch is also included in this system.

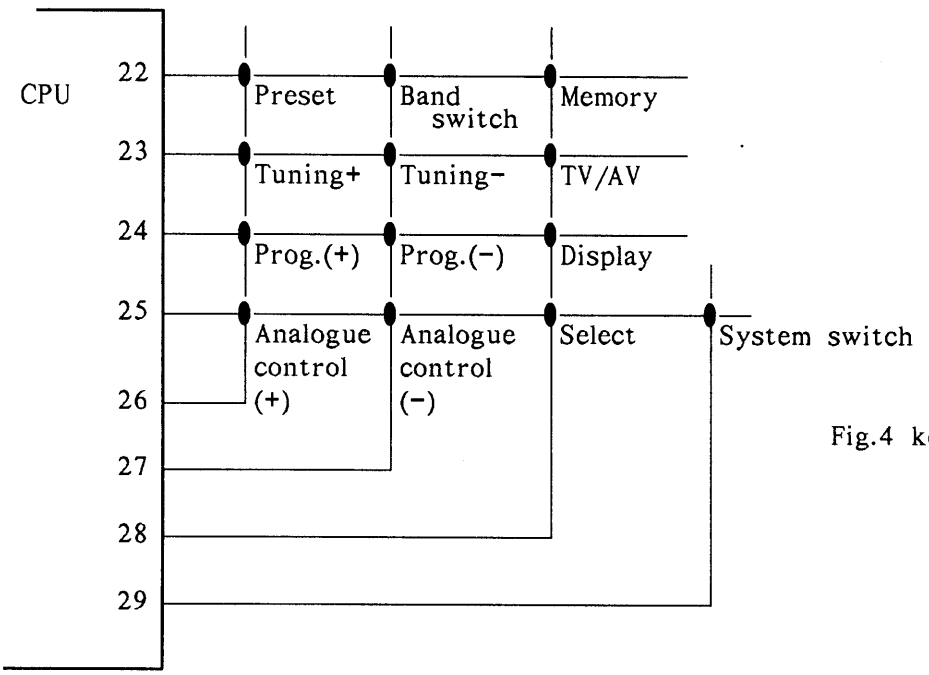
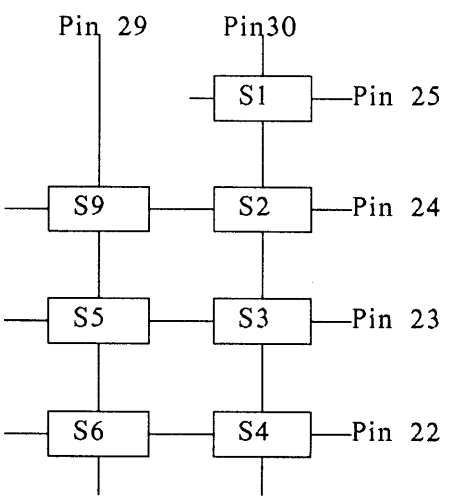
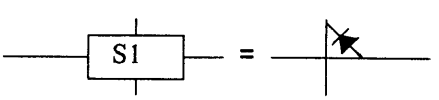


Fig.4 key matrix



	Diode	
Sw.	Connected	Open
S1	UHF only	3 Bands
S2	4 systems	3 systems
S3	System display:no	System display:yes
S4	System L/L'	System B/G,I/I'
S5	AV mode system memory : no	AV mode system memory : yes
S6	Text : yes	Text: no
S9	Digital AFT : no	Digital AFT : yes
S8	CPU pin 18:ground=AV-2,	off=AV-1
S7	CPU pin 17:ground=R/C,	off=no R/C

Fig.5 Option switch matrix



The TV receiver can be designed to allow selection of desired modes by connecting diode to the option switch instead of the keys mentioned above. The signal at this circuit is taken one time only, at the time of initialization, which is when the main switch is turned on.

The CPU then decodes this according to the program, and enters the switch condition in the memory of the necessary RAM. The data of this RAM are read and executed during the execution of the main program.

3.Key Functions

3-1 Main Switch

When the TV power cord is connected and the main switch is turned on, the CPU terminals operate as shown in the timing chart of Fig.6.

First, the power supply for CPU peripheral circuits rises to +5 V. The terminal at pin 17 then rises temporarily to 5 V and immediately drops to 0 V. At the cut-off of Q792,the base of Q552 goes high, energizing Q552 and grounding R565 and D562. This energizes Q551 and Q554 and supplies B4-24 V and B6-12 V to the set. During this time, the CPU reads and starts to output tuning data from internal memory.

Audio mute also goes active to mute the audio signal. The CRT starts operation about 600 ms after the main switch is turned on, and displays text on-screen.

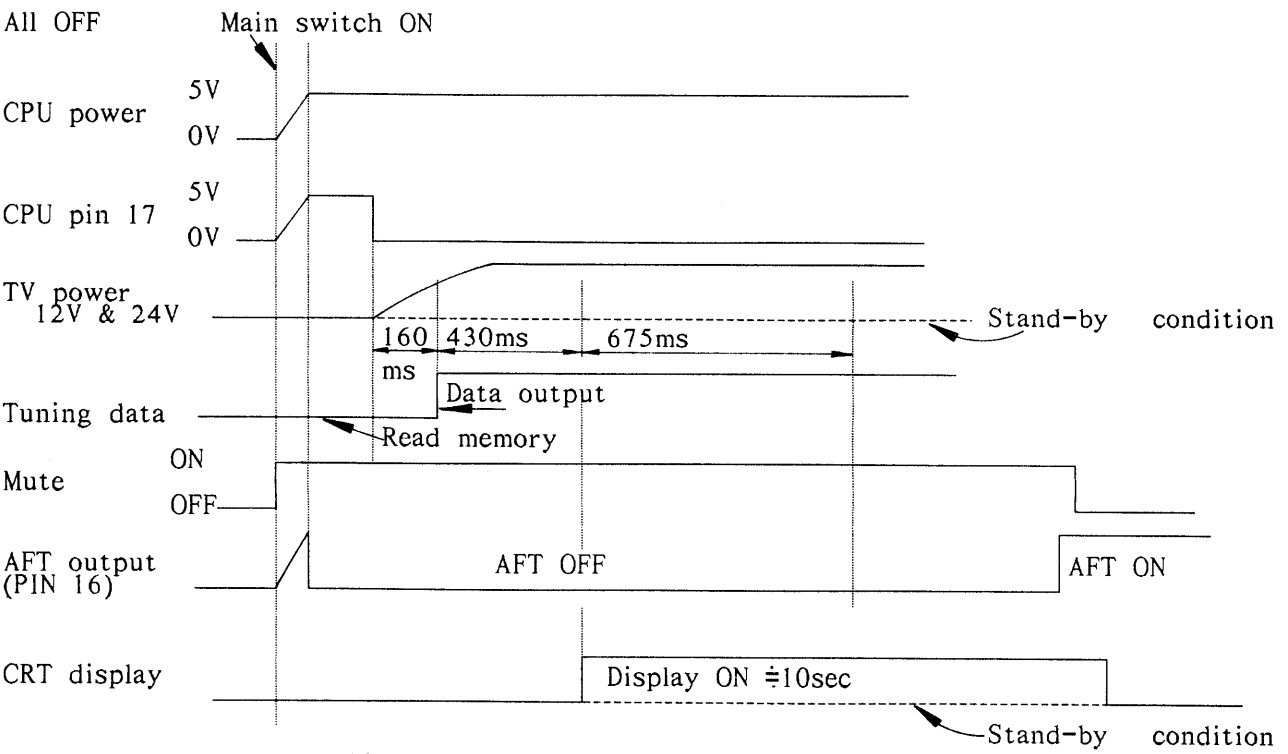


Fig.6 Timing chart for power ON

As described later, the CPU is equipped with a variety of special functions.

When the main switch is turned on and the CPU is placed in stand-by condition to allow operation using the power button of the remote control transmitter, the timing for the voltage of each terminal is as shown by the dotted line above. The +12 V and 24 V power supplies for the TV then remain OFF awaiting the input of the remote control transmitter's power button.

3-2 Remote Control of the Main Power Supply

There are two methods used for remote control of the main power, and the control system differs slightly from the stand-by condition described above.

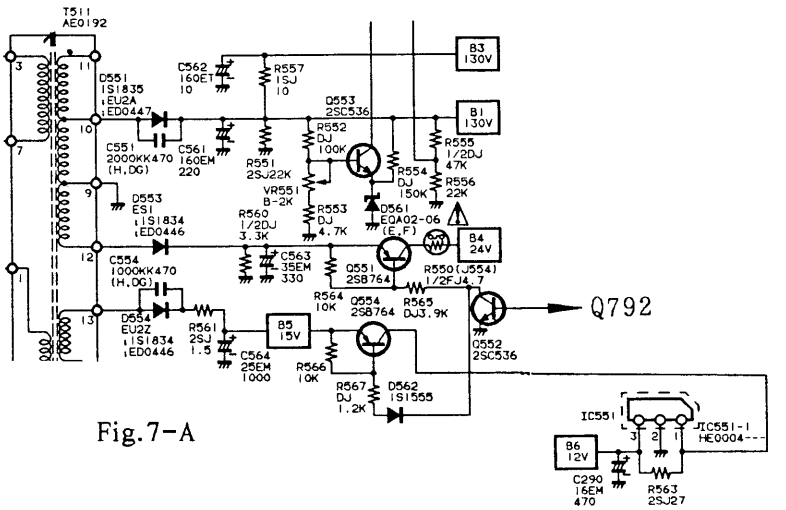


Fig.7-A

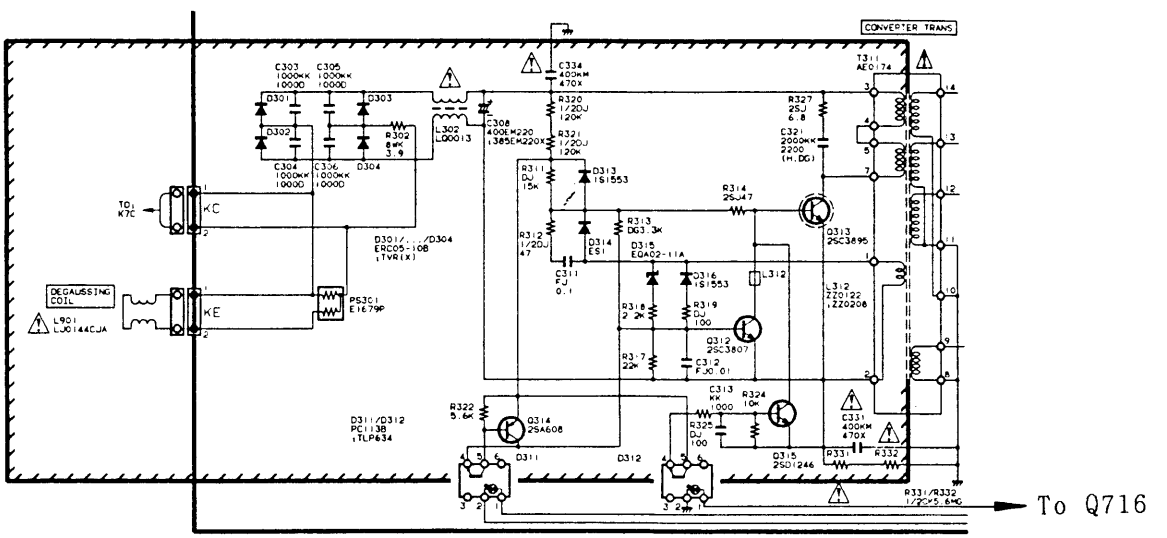


Fig.7-B

With the control system shown in Fig.7-A, when CPU power control pin 17 is at 5 V (high), Q792 (POW. OFF) is ON, the base of Q552 is turned OFF by ground potential, and Q551 (B4-24V) and Q554 (B6-12V) are cut-off, stopping the 24V and 12V supply to the TV. The power switching circuit, however, remains operating to supply +130V, 15V, etc. Considerable power is thus consumed by this circuit during stand-by.

This is improved in the power control circuit shown in Fig.7-B, in which the photocoupler which is inserted in series with the base of Q315 in the switching circuit goes ON when Q716 is energized, thus sending base current to Q315. Q315 goes ON, grounding the base of the power switching transistor Q313 and stopping the oscillation of Q312. The power switching circuit does not operate, the secondary side outputs of the converter transformer all become zero, and virtually the only power consumed during stand-by is that of the CPU. This extremely small power consumption differs considerably from that of Fig.7-A.

Fig.8 shows the timing chart for when the power button of the remote control transmitter is used to turn on the power from the stand-by condition.

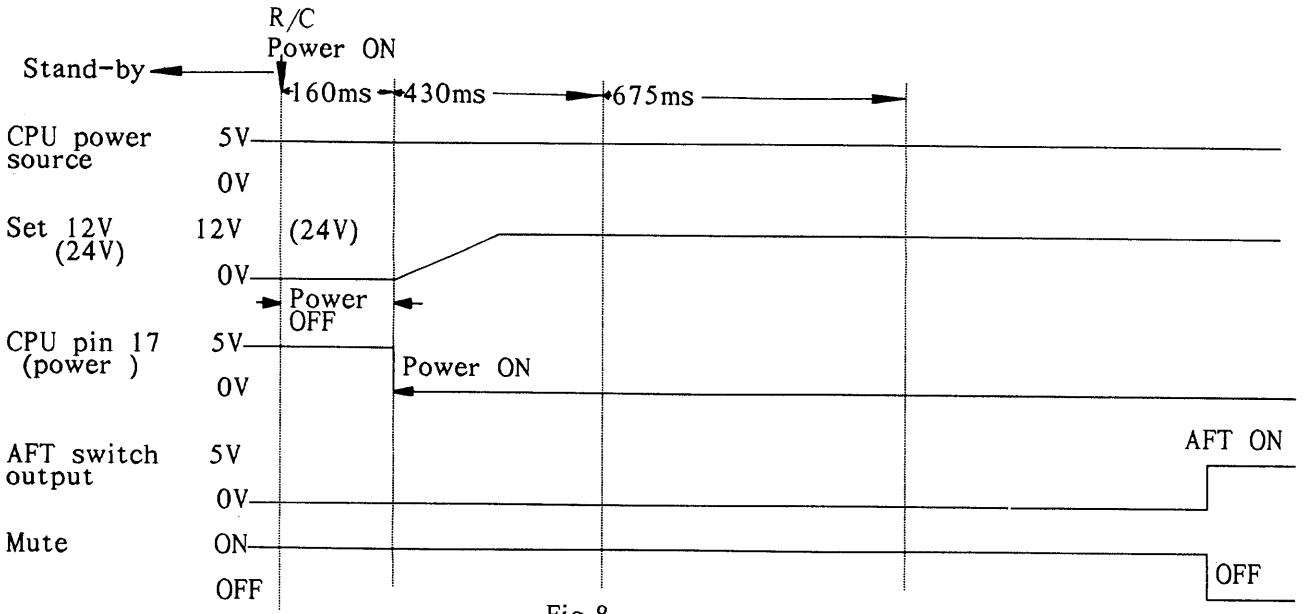

R/C
Power ON
Stand-by
160ms
430ms
675ms
CPU power source
5V
0V
Set 12V (24V)
12V
(24V)
0V
Power OFF
CPU pin 17 (power)
5V
0V
Power ON
AFT switch output
5V
0V
AFT ON
Mute
ON
OFF
OFF

Fig.8

4.CPU Clock Oscillation

Clock oscillation for CPU operation is via a ceramic oscillator connected to pins 34 and 35. The oscillation frequency is 4 MHz.

5.CRT Display Clock Oscillation

Clock oscillation for the CRT display is via an L/C oscillating circuit connected to pins 40 and 41. TH710 SDT-35 is a thermistor for temperature compensation with an oscillation frequency of 5 MHz, which is adjusted by VR710(3K) to compensate the position of text on the CRT. For text display (size, type, position, etc.), the blanking signal from pin 1 of the CPU and the text signal are synchronized and output to Q641 of the CRT PCB via Q741 and Q742 buffers, and the text symbol is displayed. The reference signal for text position is made up of the vertical and horizontal sync signals input to CPU pin 39,together with the clock oscillation circuits connected to pins 40 and 41.
To position the text vertically, display begins from the trailing edge of the vertical sync signal to the nth line of the horizontal sync signal. The value of n is determined by the CPU program.
Left/right positioning begins from the trailing edge of the horizontal sync signal to the nth oscillation pulse (pins 40, 41). Here also, the value of n is determined by the CPU program.

6.Band Switching and Tuning

6-1 Band Switching

The band switching signal is output to CPU pins 31 and 32. Band switching operates only when the preset button is pressed to set the preset mode. It does not operate outside the preset mode.
Each time the preset button is pressed, the levels of pins 31 and 32 change as shown in the table below, cycling through VL-VH-UHF-VL.
The output of pins 31 and 32 alters the output voltage of pins 1, 2, and 7 of band switching IC LA7910, to switch the tuner's receiving band.

	CPU	
Band	Pin 31	Pin 32
VL	L	L
VH	L	H
UHF	H	L

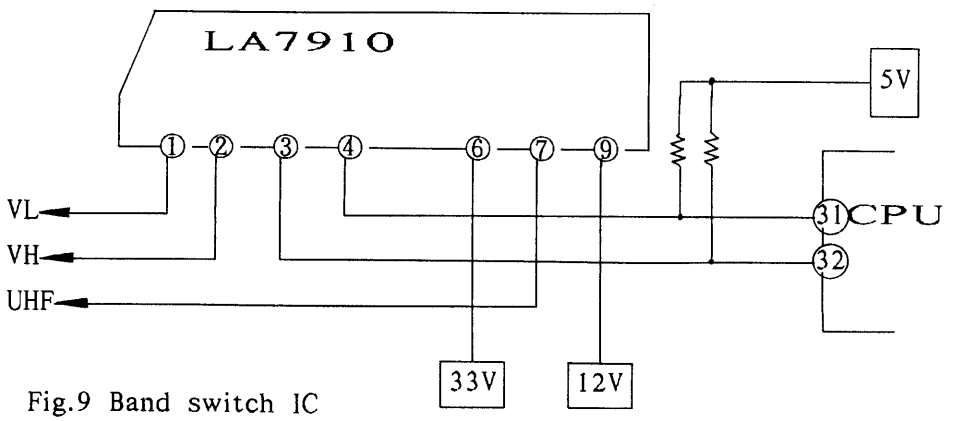


Fig.9 Band switch IC

Input from CPU		Output from LA7910		
Pin No.3	Pin No.4	VL(No.1)	VH(No.2)	UHF(No.7)
L	L	H	-	-
H	L	-	H	-
L	H	-	-	H
H	H	-	-	-
L: less than 0.8V H: more than 3V		- : High impedance H : 12V		

LA7910 in/out level

There is also an A2 chassis in which band switching IC LA7910 is replaced by individually connected transistors for each band (VL, VH, UHF). See Fig.10.

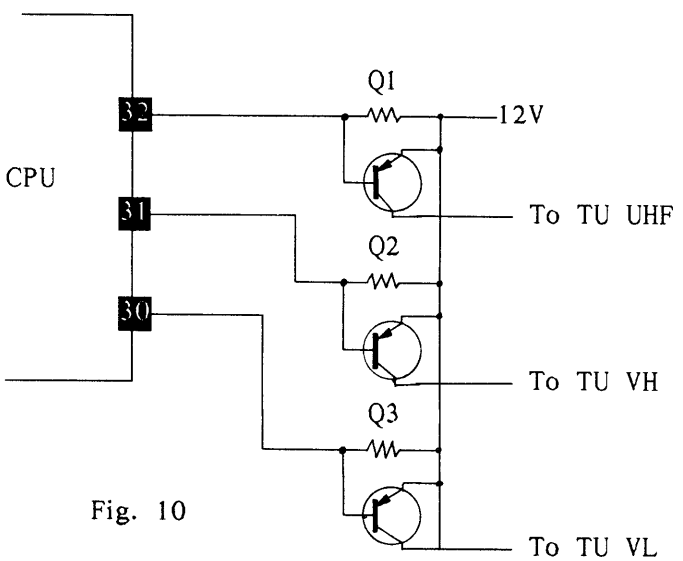


Fig. 10

CPU			UHF	VH	VL
32	31	30	Q1	Q2	Q3
L	H	H	H-12V	L:OFF	L:OFF
H	L	H	L:OFF	H-12V	L:OFF
H	H	L	L:OFF	L:OFF	H-12V

The timing of band switching operations is shown in the figure below.

When the band voltage is switched, tuning voltage pin 20 is completely lowered and the tuning voltage of the tuner connected to Q785 starts operation from the minimum level. Linear AFT is also turned off at the same time, and the audio circuit is muted to cut pulse noise generated during switching.

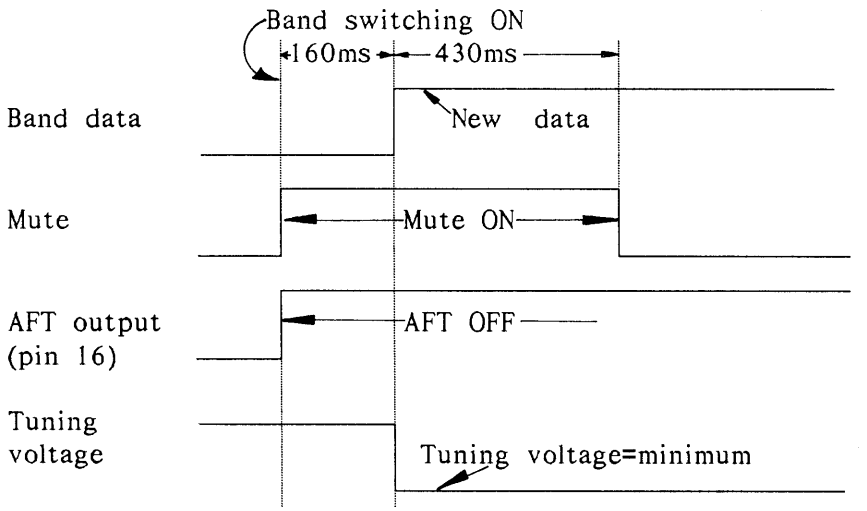


Fig.11 Timing chart for band switching

6-2 Tuning

When the preset button on the set is pressed to place it into the preset mode and one of the tuning keys is pressed, the tuning voltage of the tuner goes up or down. The tuning voltage is output to CPU pin 20, from which it passes through the low pass filter of C789, R790, and R789, and is applied to the tuner tuning pin via Q785. Muting operates while the tuning key is pressed. The entire tuning voltage range is divided into 16,383 steps. When the button is pressed, the values change for the first 300 ms as follows: VL=15 steps, VH=8 steps, and UHF=4 steps. Following this, the tuning voltages change in proportions of 64 steps/80ms, 64 steps/32ms, and 64 steps/16ms respectively.

For VL to go from minimum to maximum voltage, it takes 20 seconds to change 16,383 steps at the rate of 8 steps/10 ms (16383/8 x 0.01s); for VH it takes 40 seconds, and for UHF it takes 80 seconds.

The output of CPU pin 20 is the same as that described in the next section, 6-3 Fine Tuning, in which the waveform is output with the pulse modulated according to 14-bit digital data for 122Hz with a 500-ns minimum pulse width. However, the rate of change for output amount differs from tnat for fine tuning, with 64 steps/80ms for VL tuning as compared to 4 steps/100ms for VL fine tuning.

6-3 Fine Tuning

The fine tuning key of the remote control changes the tuning voltage output from CPU pin 20 and applies it to the tuner as shown in the table below.

Band	Step changes/100ms	Min~max time
VL	4	410 sec
VH	2	820 sec
UHF	1	1,640 sec

Total steps : 16,383

When the tuning key is pressed, linear AFT goes OFF (CPU pin 16 goes high). Fine tuning does not operate in the AV mode. In the preset mode, the bar display on the CRT changes according to the tuning voltage.

In the actual output waveform of the CPU tuning voltage, voltage changes are repeatedly modulated within a pulse width of 122 Hz and output with a minimum pulse width of 500ns.

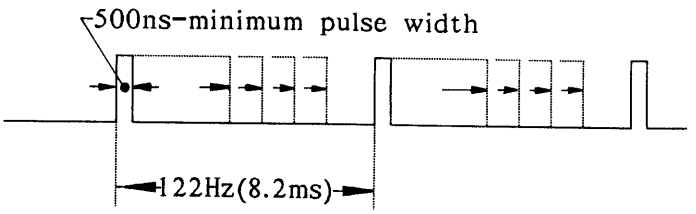


Fig.12

This output passes through the low pass filter C790, C789, and R790 to control tuning voltage transistor Q785 and change the voltage at the TU pin of the tuner. The output waveform changes as shown by the broken lines in Fig.12.

7. System Switching

When the system switching key connected to CPU pins 25 to 29 is pressed, the levels of CPU pins 26 and 27 change sequentially as shown in the table below.

The table shows the conditions when the key input option switch is set to S2 OPEN, S4 OPEN (no diode connected).

	CPU		LA7910	
	Pin 26	Pin 27	Pin 2	Pin 7
S1	L	L	-	-
S2	L	H	H	-
S3	H	L	-	H

- : High impedance
H : 12V

The output from pins 26 and 27 is input to pins 3 and 4 of system switching IC 351 LA7910. This input changes the levels of LA7910 pins 2 and 7 as shown in the table. When pin 2 is high, Q357 is ON, and AN3565N(SECAM decoder IC) pin 8 is high, the system is PAL. When pin 7 is high, Q351 is ON, and AN3565N pin 8 is grounded, the system is SECAM.

When pins 2 and 7 are both open, AN3565N pin 8 opens and the system (PAL or SECAM) is automatically judged by the IC according to the input signal.

The output waveforms of pins 26 and 27 described above are as shown below.

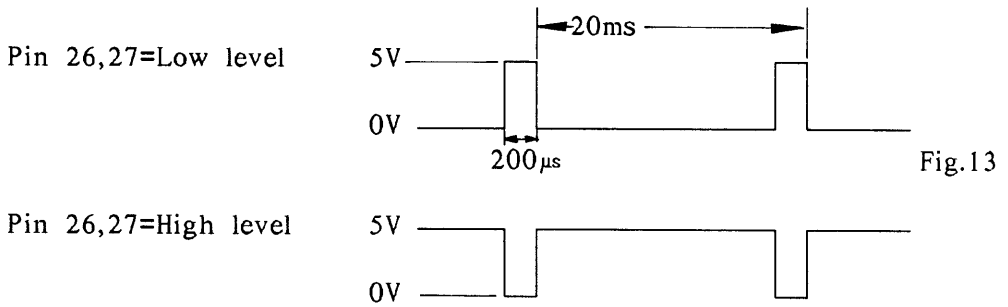


Fig.13

8.Analogue Control(Volume,colour,brightness,contrast control)

These controls are adjusted by pressing the select key for the desired control item, then using the -/+ keys.

CPU pin 10 : Volume control output
CPU pin 11 : Colour control output
CPU pin 12 : Brightness control output
CPU pin 13 : Contrast control output

The output that results from pressing the -/+ keys sends a waveform to the appropriate pin with the wave form pulse width modulated in up to 65 steps according to 7-bit data. The frequency is 1 kHz, and the minimum pulse width is 16 μs.

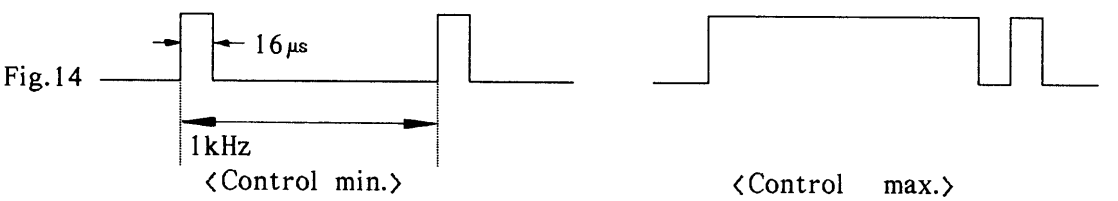


Fig.14

The 65 steps that bring this data from minimum to maximum value take about seven seconds. The pulse output that reaches pins 10 to 13 passes through the low pass filter that is connected to each pin, after which the volume control output applies DC control to the audio IC, and the colour, brightness, and contrast control outputs apply DC control to the chroma IC. The control indications shown below are displayed on the CRT in accordance with the output level.

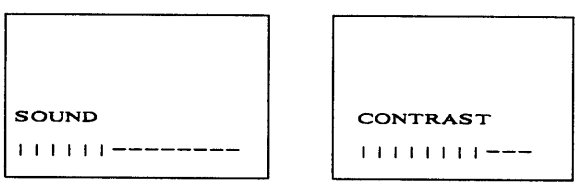


Fig.15

The control items are switched by pressing the CPU select key, which cycles through COLOUR---BRIGHTNESS---CONTRAST---VOLUME--repeatedly, and the level of control is adjusted for whichever control item is displayed on-screen.

9. Linear AFT

The AFT circuit and its operation have not changed from previous chassis. In the A3 chassis, AFT operation is performed by the tuning circuit connected to pin 43 of IC101 LA7680 and consisting of T131, C131, C132, C133, C134, and L131. Because the tuner voltage holding accuracy of the voltage synthesizer used in this chassis is not as high as that of a frequency synthesizer, AFT must be constantly applied after tuning. However, since errors may occur with AFT applied when the tuning voltage is changed by changing channels or switching tuning bands, AFT must be turned off during these operations. Thus for band switching, the AFT ON/OFF signal is sent to CPU pin 16.

When pin 16 goes high, Q751 goes ON, and AFT operation is stopped by forcefully grounding the L/C of the AFT tuning circuit at VIF CPU pin 16.
Conversely, when pin 16 is low (0.4 V or less), Q751 goes OFF, and the AFT circuit of IC101 operates normally to apply the AFT voltage output (IC101 pin 44) to the tuner AFT pin.

Note: The digital AFT circuit is not used in the A3 chassis (CPU pin 8).

10. TV/AV Switching

10-1 SCART 21-Pin Switching

When an external control signal is connected to pin 8 of the 21-pin socket, the video circuit can be remotely switched using the switching TR or IC.

10-2 Remote Control or TV/AV Key Switching

Addition of the option switch (see Key Inputs) allows switching between AV1 and TV or between AV2 and TV. Either switching cycle can be controlled by remote control key or a key on the set to cycle TV-AV1-TV-AV1... or TV-AV1-AV2-TV...

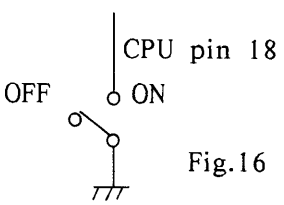


Fig.16

<Option switch S8>

	CPU Pin 5 Output
TV mode	H (5V)
AV mode	L (0V)

<Option switch S8 : ON>

The output of CPU pin 5 turns the switching TR ON/OFF.
When CPU pin 5 is low (SCART pin 8 is high), TV/AV switch Q732 goes OFF and Q810 goes ON. At the same time, the TV pin of switching IC801 (LC 4066B) connected to the external AV input is opened, the pin connected to the external AV is closed, the audio signal is input to audio output IC pin 2, and the video signal is input to pins 38 and 33 of video signal processing IC101 via Q802.

When the option switch is OFF (CPU pin 18 is OFF), two AV inputs are possible. Switching is then done according to the changes in CPU pin levels that are made by pressing the TV/AV key on the set, as shown in the table below.

	CPU Pin 5	CPU Pin 18
TV	H (5V)	H (5V)
AV 1	L (0V)	H (5V)
AV 2	H (5V)	L (0V)

<Option switch OFF>

In either case, the mute signal is output for about 600 ms after the TV/AV key is pressed to switch modes, in order to prevent noise during switching.

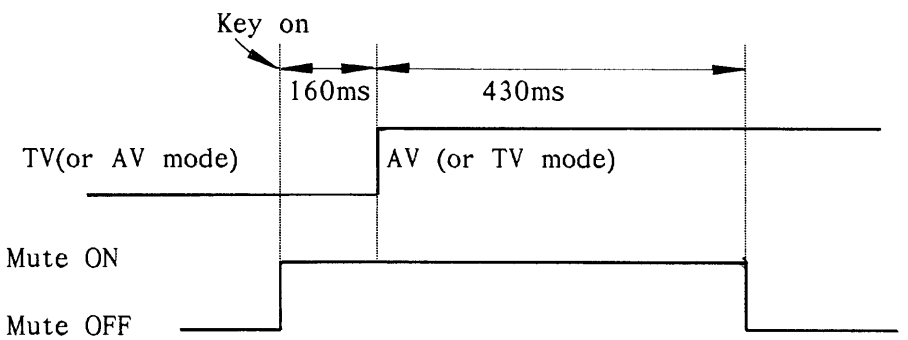


Fig.17

11. Other CPU Functions

11-1 Memory

(1) The memory function is used to store the control values for volume, colour, brightness, and contrast during ordinary TV reception, so they can be read from memory and reproduced during later TV reception by pressing the normal key of the remote control transmitter.

(2) The tuning voltage, band voltage, and system data are also stored in memory during preset.

11-2 Off-Timer

When the off-timer key is pressed, "-00" is displayed on the CRT. Then each time the key is pressed, this display cycles through "-30" "-60" "-90" "-120" "-00"... The first time the off-timer key is pressed, the time remaining on the timer is shown. Each subsequent press of the key increases the time by 30 minutes. This timer setting is cancelled when the power is turned off.

11-3 Normal

When the normal key is pressed, the control values which have been stored for volume, colour, brightness, and contrast are read from memory and set accordingly.

11-4 Sound Mute

11-4-1 During Channel Switching

When the sync signal from VIF IC pin 30 is input to CPU time base signal pin 9, it is applied simultaneously to audio output IC pin 3 via Q 181. Then as soon as the sync signal stops, muting is applied to the audio circuit.
This prevents popping noise when changing channels or switching bands.

VIF IC pin 30 is high when the horizontal sync signal is normal, and low when the phase of the horizontal sync signal shifts. Thus pin 30 goes low in the absence of a sync signal or when horizontal sync deteriorates, muting transistor Q181 goes OFF, and pin 3 of audio IC171 AN5265 goes high (12V), to set the audio IC volume at minimum and prevent audio output.

11-4-2 During Remote Control

When the mute button of the remote control transmitter is pressed, the signal is decoded by the remote control receptor and the audio control signal which is output to CPU pin 10 is set to the minimum level in order to cut audio output.

11-5 Skew Output

When the programme number for VCR1, 2, 3 or the AV mode is selected, CPU pin 33 goes low. This cuts off skew signal switching transistor Q733, then passes through D731 and is applied to VIF/DEF IC101 pin 32, where it shortens (by 1/2) the normal time constant of the AFC (automatic frequency control) for the horizontal sync signal within the IC in order to quickly trace unstable input in the horizontal sync of playback from sources such as a VCR, and prevent jitter in the horizontal direction of the image.

11-6 Overload Protector

When an abnormality during TV reception causes CPU pin 15 to go continually low (less than 0.8V) for approximately one second, the overload protector shifts the TV into stand-by condition. In the actual circuit design, pin 15 is connected to the 9V power supply of the set in order to protect the set from being damaged by operation when a malfunction in a component along the 9V line, or along the 12V line, has caused an extreme drop in voltage.

11-7 Teletext Control

A clock frequency of 14 kHz output from pin 36 and 7 bits of data from pin 37 are input to the Teletext decoder CPU to control the Teletext CPU. A partial list of the text control signals that are derived from the 7-bit signal of pin 37 is shown in the table below.

Pin 36 clock output

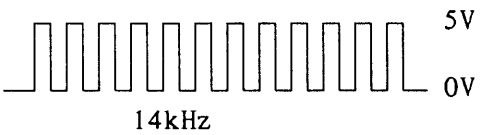


Fig.18

Pin 37 output

Bit	0	1	2	3	4	5	

Fig.19

Bit 0=1:Text mode, Bit 0=0:TV mode

Bit 1 2 3 4 5 6	
0 0 0 0 0 0	Red
1 0 0 0 0 0	Green
0 1 0 0 0 0	Yellow
0 0 1 0 0 0	Status
.	.
.	.
.	.
.	.
0 1 0 1 1 0	Size
1 1 0 1 1 0	Up
0 0 1 1 1 0	Down
.	.
1 1 1 1 1 0	Text

12.Special Function

This CPU is equipped with special functions that allow the set's initial condition and subsequent operating conditions to be set. This is not possible, however, in preset, AV, text, and text-TV-mix modes. The descriptions and setting procedures for these special functions are given below.

You can set the special functions to input the special codes using the special key and the programme selector of the remote control transmitter.

The codes and functions are as follows.

Code	Function
01	Reset all special functions
70	Search for channel scanning
71	Memory delete for channel scanning (Used to delete a programme position from the channel scanning positions.)
72	Memory add for channel scanning (Used to add a programme position to the channel scanning positions.)
90	Private position (Set and reset) (Used to restrict the viewing of some programme positions.)

NOTE: Special functions are not cancelled when the power is turned off or when the AC power plug is disconnected from the mains.

Setting the Private Position (Special code 90)

- The private position is used to restrict the viewing of programme positions that you do not want others to watch.
- Any positions can be set as private positions.

Example

Setting Programme Position 15 as a Private Position

1. Select programme position "15" using the programme selector.

2. Press and hold the special key of the remote control transmitter for more than 2.5 seconds. "SP--" will be displayed on the screen.

3. Input special code 90 using the programme selector of the remote control transmitter.

4. Press the memory button in the front control section of the TV set. The picture will then disappear, and "X 15" will be displayed on the screen.

The private position setting is now completed.
When position 15 is selected using the programme selector after the private position setting has been completed, only the characters "X 15" will appear.

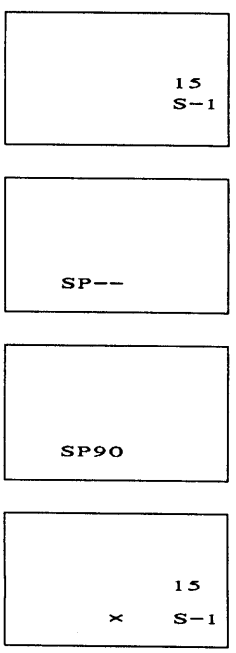


Fig.20

Watching a Programme in the Private Position :

1. Select the private position (position 15) using the programme selector .
2. Press and hold the special key of the remote control transmitter for more than 2.5 seconds. ' SP--' will be displayed on the screen.
3. Input special code 90 using the programme selector of the remote control transmitter. The programme in the private position will then appear. Next, press the special key, and "SP90" will disappear.

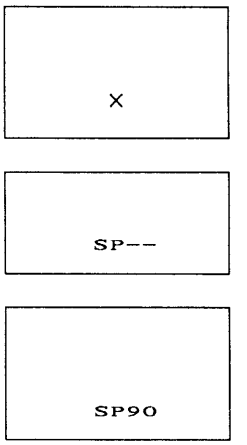


Fig.21

NOTE: If you watch a programme on the private position, then select another programme position, you will have to repeat the above procedures before you can watch a programme in the private position again.
As many private positions as you want can be set.

Resetting the Private Position

●This is done in the same manner as the private position setting.

For example, to reset programme position 15 in the private position:

1. Select programme position "15" (private position) using the programme selector. ("X 15" will be displayed on the screen.)
2. Press and hold the special key of the remote control transmitter for more than 2.5 seconds. ("SP--" will be displayed on the screen.)
3. Input special code 90 using the programme selector of the remote control transmitter.
4. Press the memory button of the front control section of the TV set. Position 15 is now reset in the private position.

Channel Search (special code 70)

● When special code 70 is input, all the programme positions are automatically scanned, and the active programme positions are stored in memory. Once this programming is completed, the TV receiver will select only the stored programme positions when the channel scanning key is pressed.

Inputting special code 70

1. Press and hold the special key of the remote control transmitter for more than 2.5 seconds. ("SP--" will be displayed on the screen.)
2. Input special code 70 using the programme selector of the remote control transmitter.
3. Press the memory button. The programme positions are then automatically scanned, and the active programme positions are stored in memory. The channel scanning will then stop at the position where it started scanning. The channel scanning is now completed.

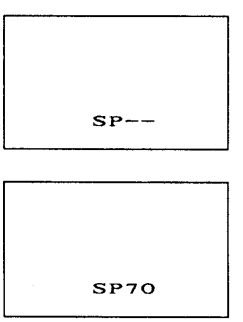


Fig.22

Memory Delete for Channel Scanning (Special Code 71)

This function is used to delete a programme position from the channel scanning positions, so it will not be scanned when the channel scanning key is pressed.

For example, to delete position 2 from the channel scanning positions:

1. Select programme position 2 using the programme selector.
2. Press and hold the special key for more than 2.5 seconds, and input code 71 using the programme selector of the remote control transmitter.
3. Press the memory button of the front control section of the TV set.
   Position 2 is now deleted from the channel scanning positions.
   Position 2 will be passed over when the channel scanning key is pressed.

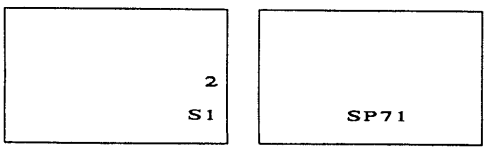


Fig.23

Channel Scanning Memory Add (Special code 72)

This function is used to add a programme position to the channel scanning positions, so it will be scanned when the channel scanning key is pressed.

For example, to add position 2 to the channel scanning positions:

1. Select programme position 2 using the programme selector.
2. Press and hold the special key for more than 2.5 seconds, and input special code 72 using the programme selecter of the remote control transmitter.

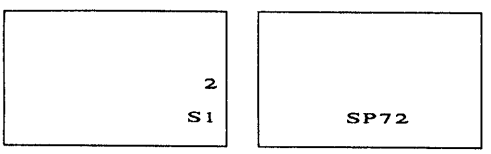


Fig.24

3. Press the memory button,of the front control section of the TV set.
   Position 2 is now added to the channel scanning positions.
   Position 2 will be scanned when the channel scanning key is pressed.

Resetting All Special Functions (Special code 01)

When special code 01 is input, all the special functions are reset.

How To Input Special Code:

1. Press and hold the special key for more than 2.5 seconds, and input special code 01 using the programme selector.
2. Press the memory button of the front control section of the TV set.
   All the special functions are now re-set.

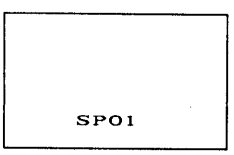


Fig.25

NOTE: The special functions can also be cancelled by inputting code 00. When special functions are cancelled using code 00, the start condition for TV power is changed to the standby start condition, meaning that the picture will not appear even when the mains ON/OFF switch is set to the on position. To turn on the TV set from the standby mode,press power on/off button of the remote control. Code 00 is input in the same manner as code 01.

Other Special Functions

The start condition for TV power can be changed by inputting code 50 or 51.

When code 50 is input:

Even if the mains ON/OFF Switch is set to the on position, the picture will not appear. (The TV set remains in the standby mode). To turn on the TV set from the standby mode, press the power ON/OFF button of the remote control.

Inputting Code 50 :

1. Press and hold the special key for more than 2.5 seconds, and input code 50 using the programme selector.
2. Press the memory button on the front control section of the TV set.

NOTE: To return the TV's power starting condition to its original condition, input code 51. Code 51 is input in the same manner as that for special keys.

13. CPU Repair

When installing a new CPU, keep in mind that the data of the EEPROM inside the CPU must be initialized the first time it is used. Use the following procedure to initialize.

(1) Connect the antenna to the TV.
(2) Install the new CPU.
(3) Turn on the power switch.
(4) Select position 1 using the direct access of the remote control.
(5) Select the special function mode by pressing and holding the recall key for more than 2.5 seconds. ("SP--" will be displayed on the screen.)
(6) Use the numeric keys to input 00 or 01 (see note below).
(7) Press the memory key.
(8) Press the preset button, then select a channel and store it in an appropriate position.
(9) Press the preset button again to return to the normal reception mode.

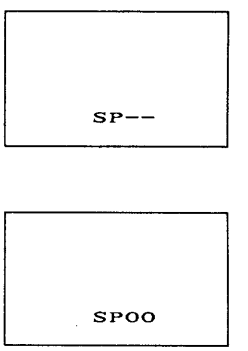


Fig.26

This completes the initializing procedure. If you should make a mistake during this initializing, turn off the power and repeat the procedure from step (3).

Note: Inputting 00 will set the stand-by starting condition, so that when the main switch is pressed the set will enter stand-by condition and wait for the power key of the remote control transmitter to be pressed.
Inputting 01 will start the TU in whatever condition it was in when the power was last turned off.

[Part 2 VIF/CHROMA/DEF ONE CHIP IC LA7680]

This part describes the functions of SANYO LA7680 PAL/SECAM colour TV signal processing one chip IC ,according to the pin allotment respectively.
Fig.1 and Fig.2 show the block diagram and the pin allotment.

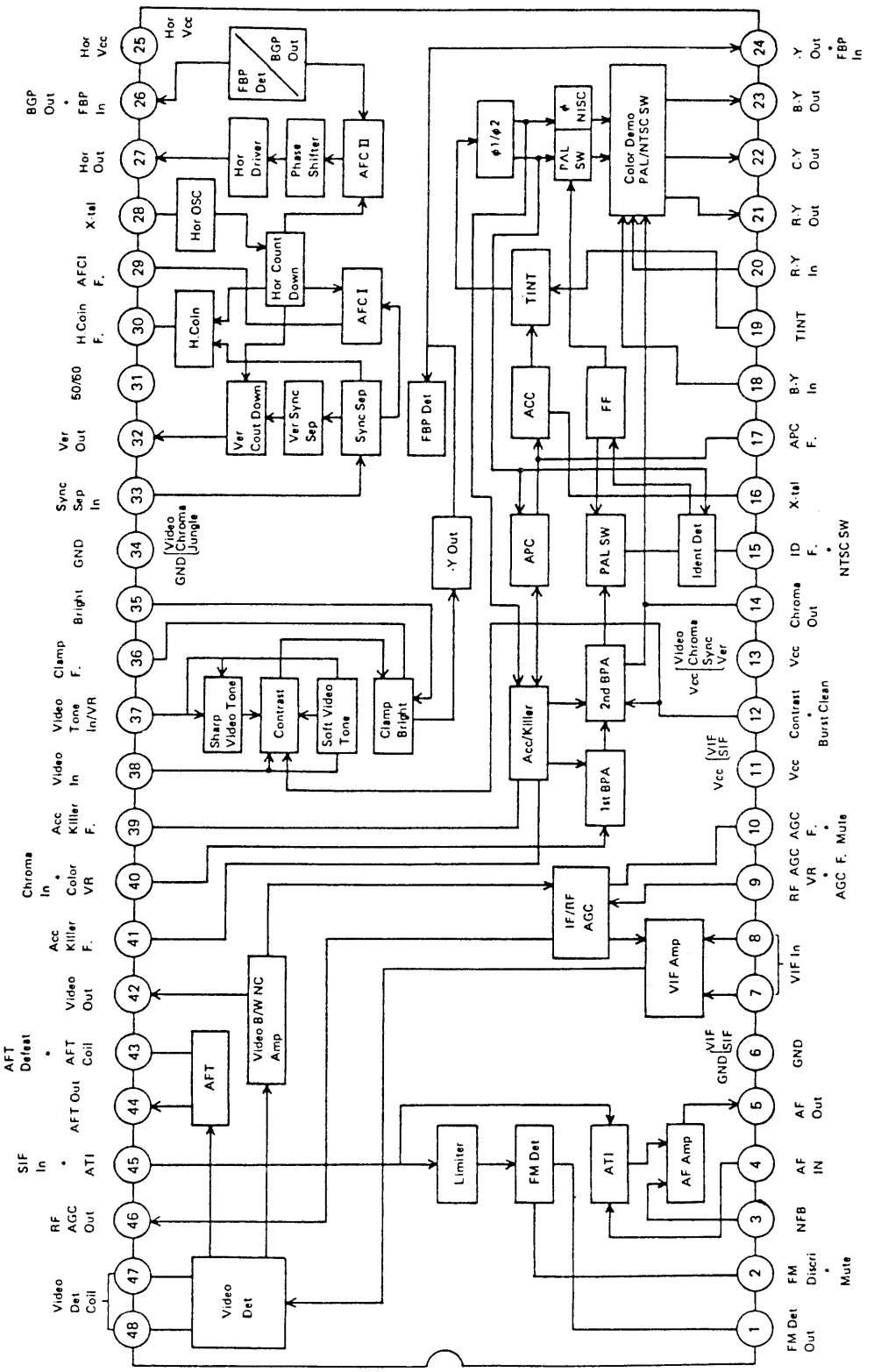


Fig.1 Pin allotment

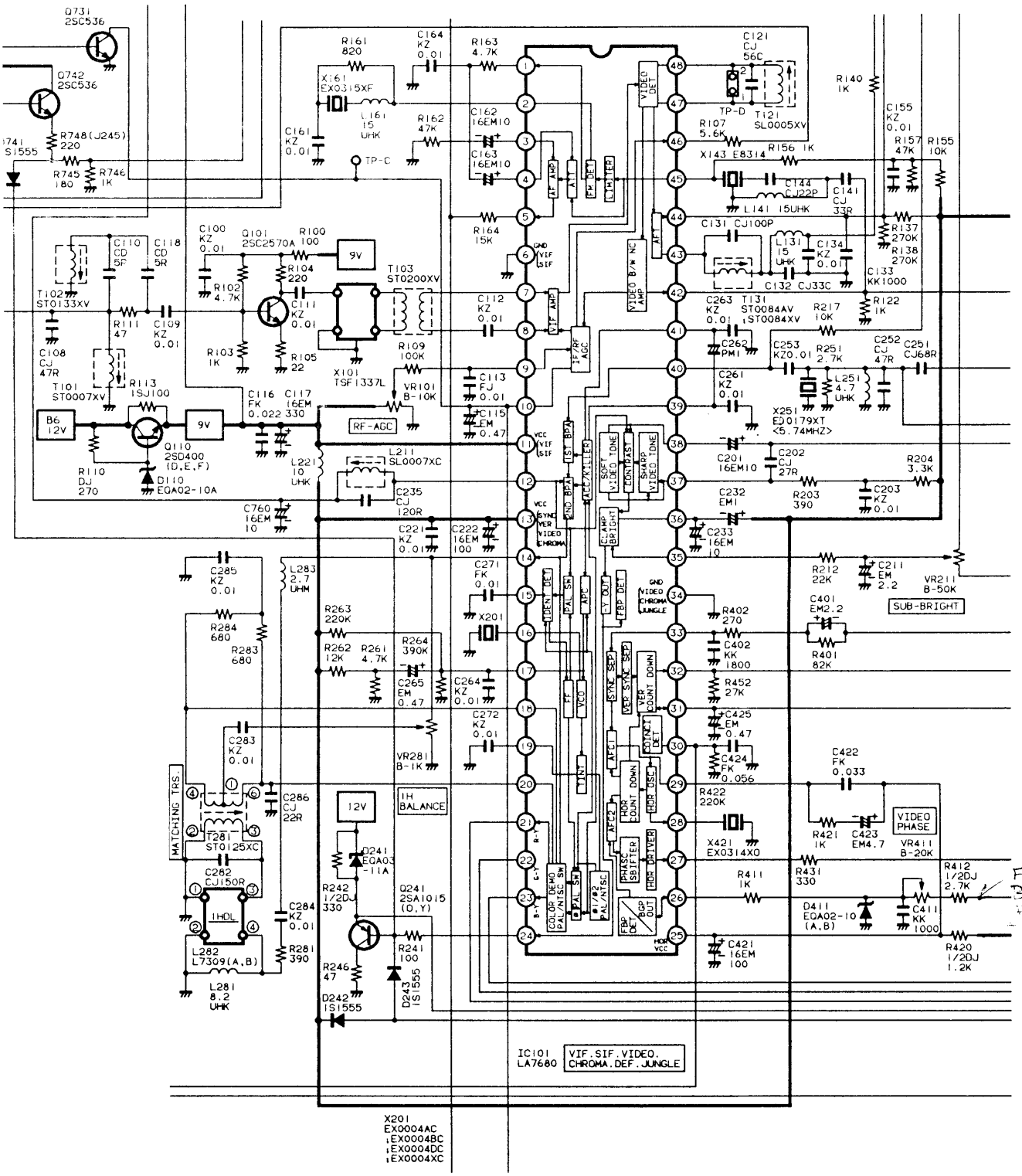


Fig.2 IC101 LA7680 peripheral circuit

1. VIF/SIF/AGC

1-1 FM Detector output (Pin 1)

The 1-pin output is based on the emitter follower circuit. Therefore, its output impedance is rather low. The capacitor of 1000pF should be inserted for carrier filtration between this pin and the GND. In sound multiplex system, the capacitor value should be changed to 560pF (-3dB at 60kHz).

The "de-emphasis" circuit would require a series resistance of 5.6kΩ and a capacitance of 0.01uF between that resistance and the GND.

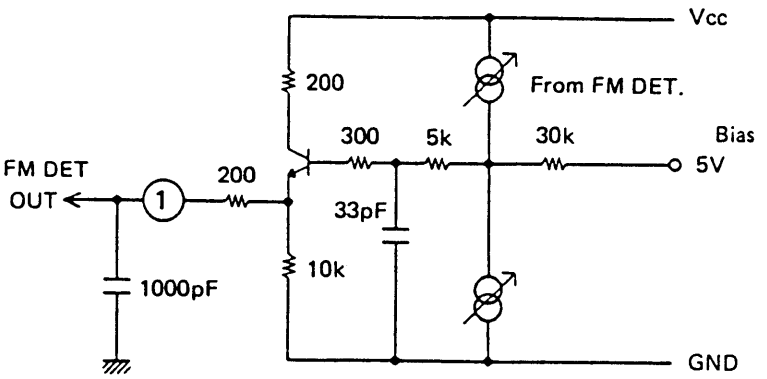


Fig.3

1-2 FM Discriminater & Mute (Pin 2)

The FM detector is based on a "quadrature detection circuit". This detector uses two signals: one with limited amplitude from the limiter AMP and the other with 90° of phase difference from the phase shifter. These two signals are used by the multiplier for FM detection. The output level and the bandwidth can be determined by the two damping resistors (R1 and R2) for the coil and the ceramic discriminater.

The MUTE function for the FM detector can be activated by lowering the DC pin voltage across the damping resistance to less than 1V.

Example ceramic discriminater circuit

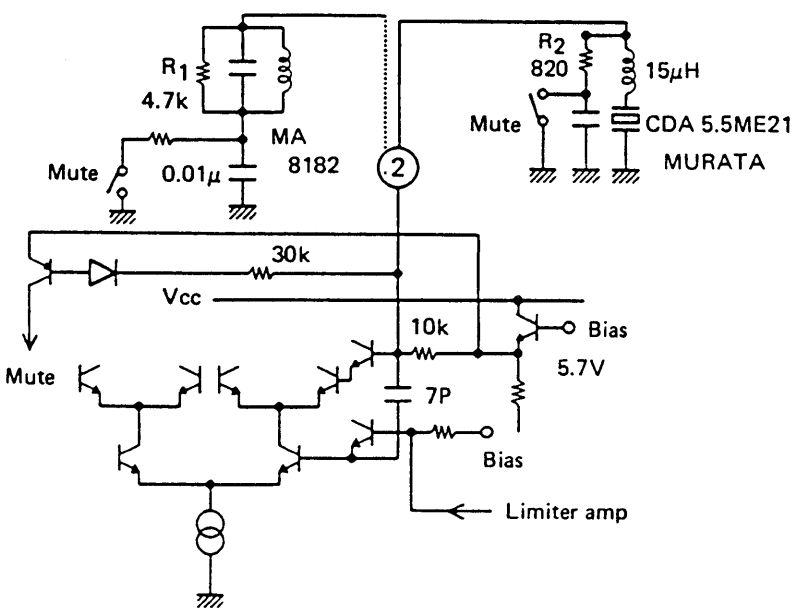


Fig.4

1-3 Negative Feed Back of AF Amp (Pin 3)

This pin is for audio pre amp Negative Feed Back (N.F.B).

The output signal from pin 1 enters the A.F. amp circuit through the D.C. att. circuit and then amplified. The gain can be determined by the R1 value. If it is 1kΩ, the gain would be about 20dB. The pin 3 D.C. voltage is about 4.2V.

The output signals from pin 3 and pin 5 (audio output) are in phase with each other. Therefore, the output signals from pin 5 are inverted and then feeded back to pin 3 as AC signals.

If external AC feedback to pin 3 is not used, increase the R1 value in order for the pin 5 output not to reach saturation region (for example, R1=12kΩ).

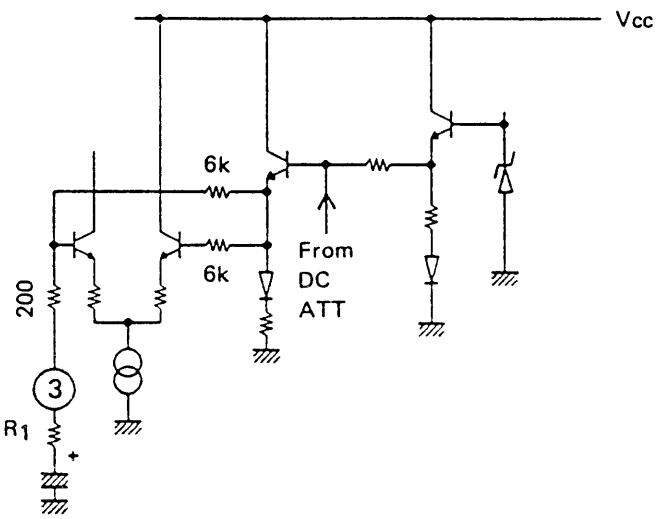


Fig.5

1-4 Audio Frequency Input (Pin 4)

The input impedance is set to 30kΩ.

This pin circuit is internally DC-based. Therefore, the input signals should be accepted via a coupling capacitor. If the internal signals from pin 1 are received, the polarities of the capacitor should be set as shown below.

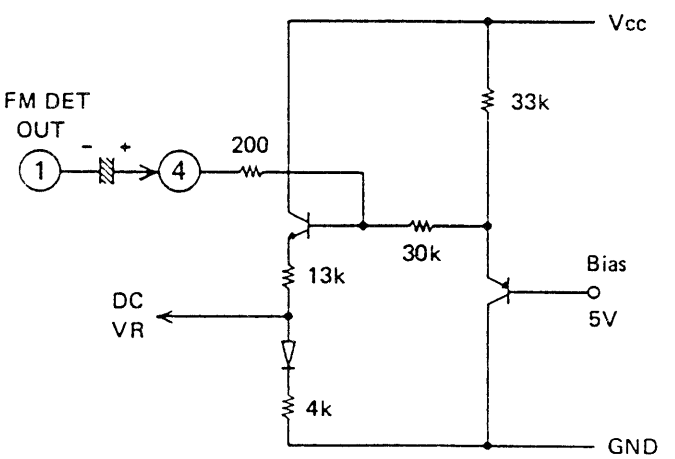


Fig.6

1-5 Audio Output(Pin 5)

This pin is for A.F.amp output. The pin output is based on emitter-follower circuit and has a series resistance of 100Ω. Some driving conditions would require lower output impedance. In these cases connect an external resistor R1 as shown below. The sound output power can be determined by the ratio of R2 and R3. The DC output voltage at pin 5 is about 4V.

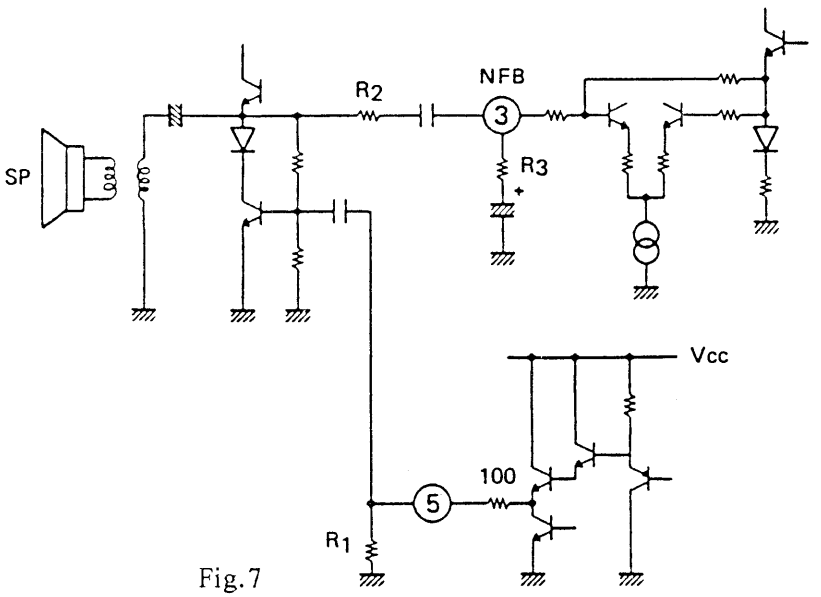
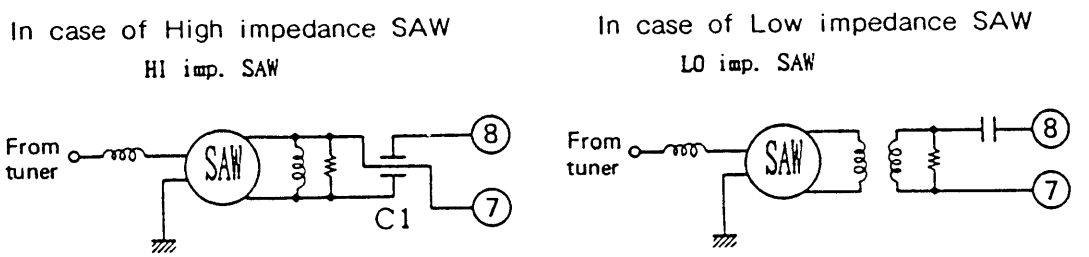


Fig.7

1-6 VIF Amp Input (Pins 7 and 8)

These pins are for VIF amp input. The signal input to this pin uses the balanced transmission circuit. The capacitor should be used for DC shutout. Its capacitance should be 0.01uF or more. The input impedance Ri is about 1.8kΩ and the input capacitance, about 4pF. The IC pin wiring should use the C1 and crossed on a printed circuit board. This may improve the electrical field characteristics.



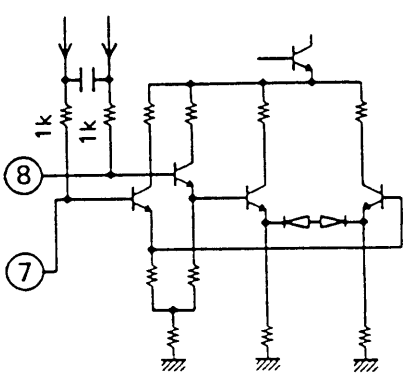


Fig.8

1-7 RF AGC Volume (Pin 9)

The AGC voltage smoothed by pin 10 (first AGC filter) is again smoothed by the C1 of the pin 9. The gain control is carried out by this double smoothing.

C1 is used for determining the AGC time constant and should be a polyester film capacitor. By applying DC current externally to pin 9, the operating point of the RF AGC AMP can be changed and the RF AGC out signal from pin 46 can be adjusted.

The operating range of the RF AGC amp can vary depending on the value of a resistor R1 in series with pin 9. However, it should be 100kΩ. The C1 capacitor (polyester film capacitor) should be placed as close as possible to pin 9.

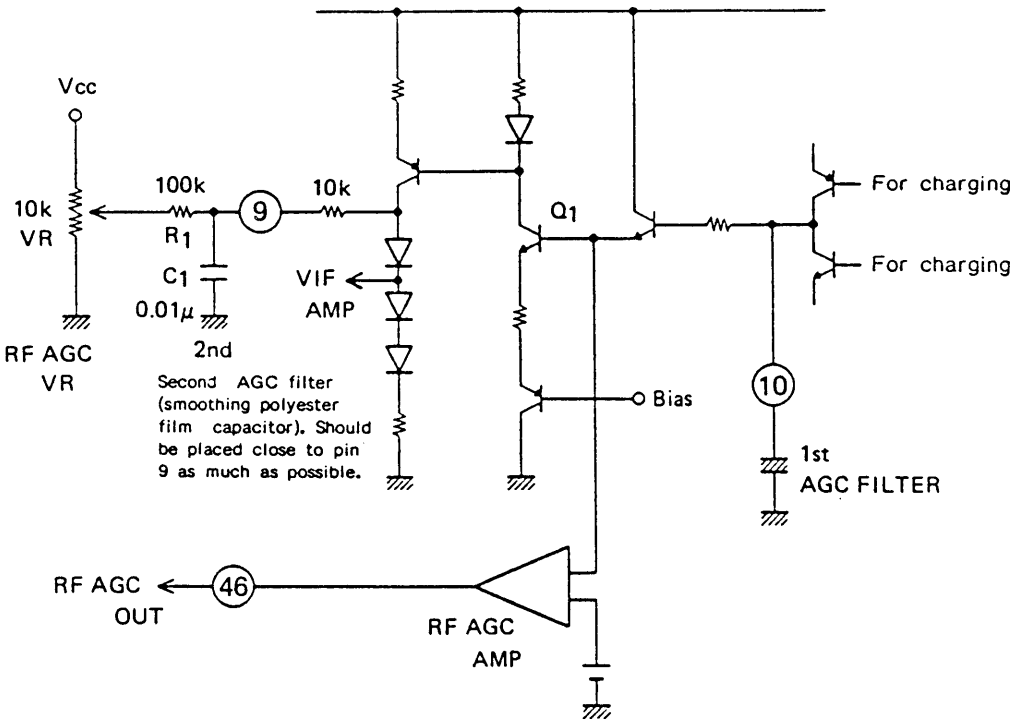


Fig.9

1-8 AGC Filter (Pin 10)

The peak signal detected by the AGC detector is smoothed by the C1 capacitor, an external capacitance to pin 10 and then generates the AGC voltage.

To determine the AGC time constant, add a capacitor between 0.22 and 0.47uF externally. Note that the external capacitor with small leakage current should be used. For example: OS capacitor, tantalum electrolytic capacitor, etc. (for limiting the ringing of synchronization signal leading edge at rather a low temperature.)

By lowering the pin 10 voltage to less than 1V, the mute function can be activated for the FM detector and the video output circuits at the same time.

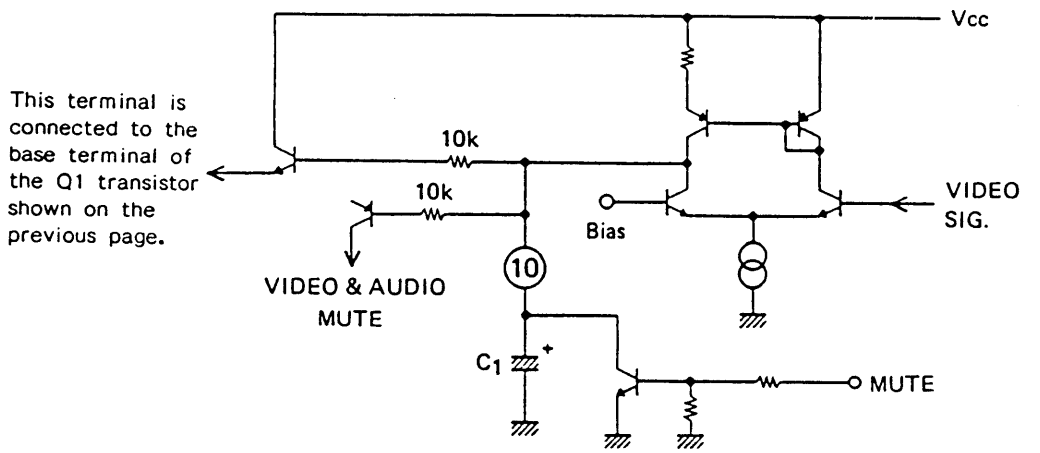


Fig.10

1-9 Video Output (Pin 42)

This pin is for video output and based on emitter-follower circuit. The value of the biasing resistor R1 should be 1kΩ or more. Changing the R2 value would affect peaking and f characteristics. Video output voltage at no signal=4.5V. Voltage of a synchronization signal leading edge=2.3V. Video amplitude=2Vp-p.

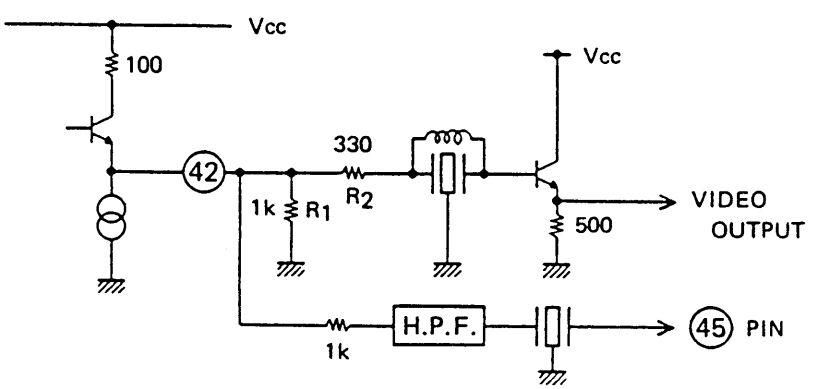


Fig.11

1-10 AFT Coil (Pin 43)

The AFT circuit is based on "quadrature detection circuit". This circuit uses two signals: one is the CW signal from the video detector and the other is the signal with a 90° of phase difference from the pin 43 phase shifter. These two signals are input to the multiplier for phase detection.

To activate the AFT defeat function, connect the pin to the GND through the R1 resistor. Note that the R1 resistance should be less than 20kΩ. The AFT improves as the C1 value increases. The recommended C1 value should be in the range between 68pF and 100pF.

The AFT improves as the Q of the L1 increases. The recommended Q0 is 90.

C2 is needed to form a sound trap circuit. This circuit prevents the AFT circuit from mulfunctioning. C1:C2=5:1 is desired. If the AFT defeat switch is not used, R1 and C3 are not required.

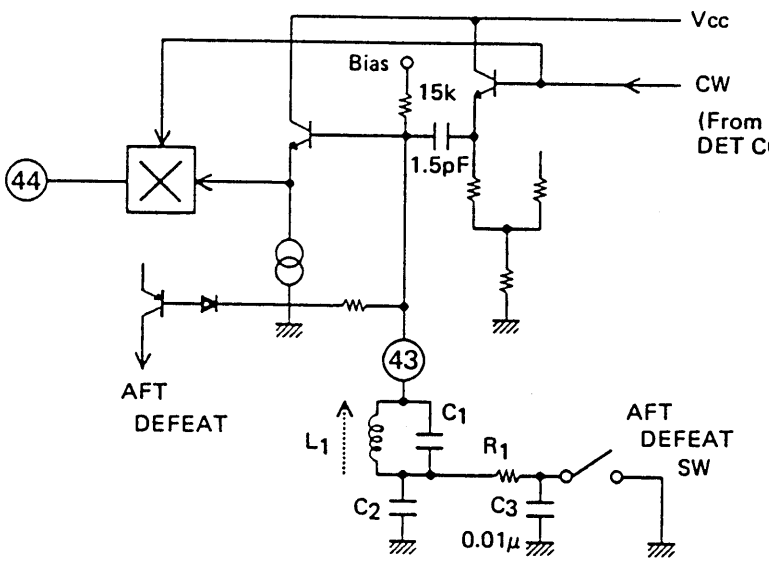


Fig.12

1-11 AFT Out (Pin 44)

The AFT circuit uses the collector of the current mirror circuit for output and includes an on-chip load resistance.

The direct voltage of pin 44 at no signal is about 4.5V (typical). The AFT sensitivity can be changed by the value of external resistors R1 and R2.

The recommended ratio of R1 and R2 is 1:1 to maintain good temperature characteristics.

C1 is a capacitor for carrier filtration. This capacitor should be placed as close as possible to the pin. The values of R3 and C2 can determine the AFT loop time constant.

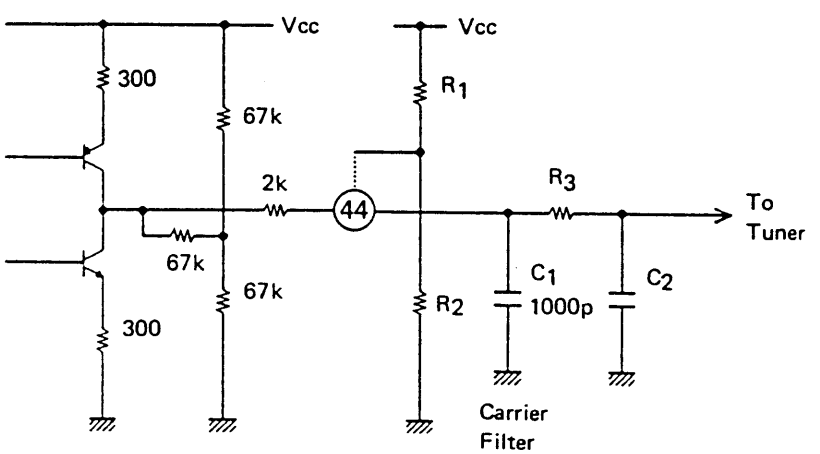
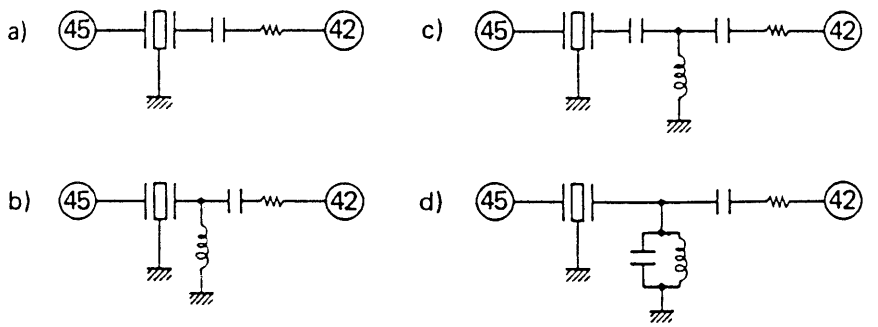


Fig.13

1-12 SIF Input and D.C. Att. (Pin 45)

Pin 45 is an unbalanced SIF input pin. Its input impedance is about 3kΩ. This pin serves as the D.C.att. input pin alternatively. The input is controlled by a PNP type transistor and its input impedance is very high.

If external components are added as shown below, the buzz characteristics can be improved. The c) circuit shows the best high pass filter characteristics.



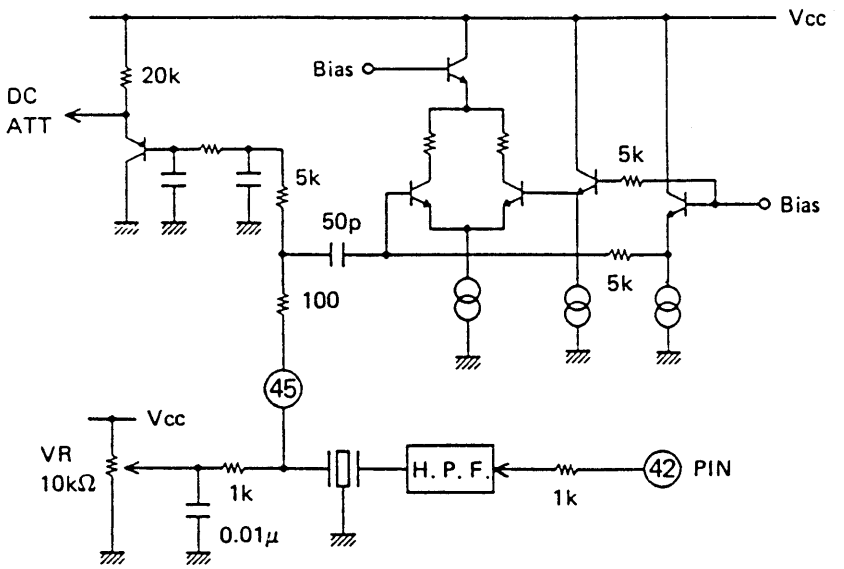


Fig.14

1-13 RF AGC Out (Pin 46)

This pin output is based on emitter-follower circuit. The time constant can be determined by external components, R and C. The maximum direct voltage of this pin is 8V. Select the values of R1 and R2 with tuner specification in mind, to determine the direct voltage.

C1 is used as a carrier leakage filter capacitor for preventing unpredictable oscillation. The values of R1, R2 and C2 can determine the RF AGC loop time constant.

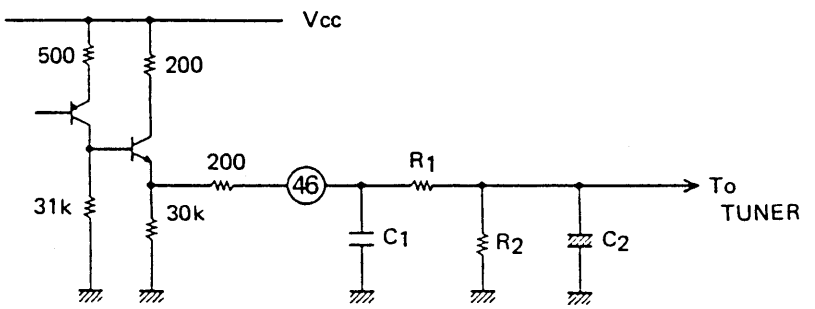


Fig.15

1-14 Video Detector Coil (Pins 47 and 48)

The best value for the Q0 of the video detector coil is about 60. If the value of damping resistor R1 is increased, better 1.07MHz beating is improved. At the same time,the video output is degraded quickly in distortion.

The recommended value for damping resistor R1 is about 3kΩ to 4.7kΩ.

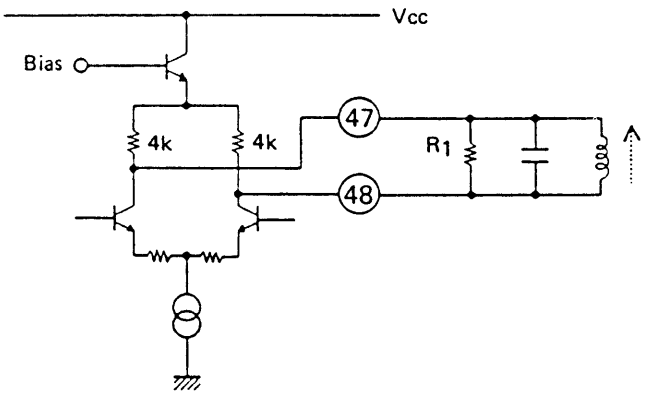


Fig.16

2. Video/Chroma

2-1 Chroma Input and Color Control --alternative pin (Pin 40)

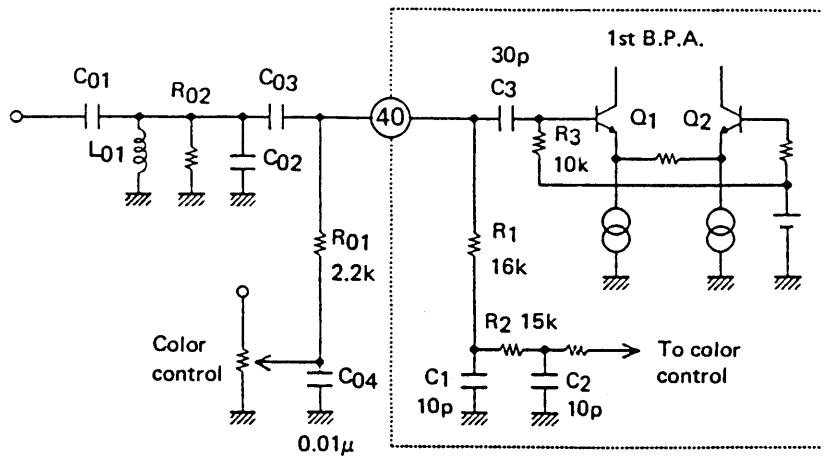


Fig.18
Chroma input and color control circuit
(Pin 40 receives a chroma signal with color control voltage superimposed on.)

2-1-1 Chroma Input

C01, L01 and C02 form a band-pass filter. R01 and R02 are damping resistors for the band-pass filtration. Note that the input impedance of pin 40 is about 7kΩ.
C3 is a capacitor for DC shutout and used for cutting color control voltage.
The standard input to pin 40 is 100mVp-p at burst signal level. If the signal level is too high, divide damping resistor R01 and then connect the dividing point with the pin.

2-1-2 Color Control

The input voltage (chroma signal + DC voltage) to pin 40 goes to the low-pass filter circuit (R1, C1, R2 and C2) and its output is used as the color control voltage. The low-pass filter circuit eliminates the chroma signal from the input voltage to the pin and finally picks up the DC voltage only. This DC voltage is used as the color control voltage. The control neutral voltage is 1/2 Vcc.

2-2 ACC/Killer Filter (Pins 39 and 41)

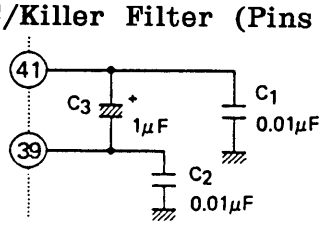


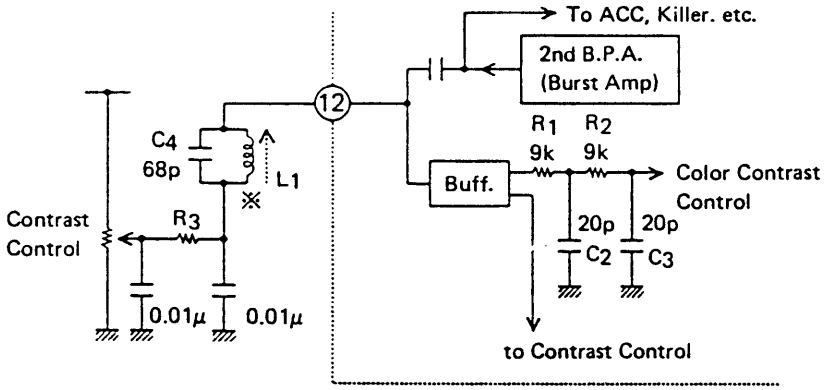
Fig.19

Pins 39 and 41 filter pins for smoothing burst detection output voltage. The ACC and the Killer circuit are operated by differential voltage between these pins.Note that pin 41 can be used for white balance adjustment.

Pin 41 holds the burst detection voltage during burst ON. In other cases, pin 39 holds the burst detection voltage. As the amplitude of the burst signal goes up from 0, the differential voltage between pin 39 and pin 41 goes up from 0 to some hundreds mV. In this case, the voltage of pin 41 gets higher. Capacitor C3 between pin 39 and pin 41 is needed for removing ACC vertical sag. The standard values for C1, C2 and C3 are shown in the above example circuit.
To adjust white balance, set the pin 41 pin voltage level to less than 1.5V (Vcc=9V. Normally ground level) and the pin 32 vertical out to high level.

2-3 Contrast Control/Burst Cleaning Coil (Pin 12)

Fig.20 Contrast control/burst cleaning circuit



* Burst cleaning coil -- Mitsumi MA8051

Pin 12 is for receiving (video/color) contrast control voltage (DC) and a burst cleaning pin.

2-3-1 Contrast Control

The contrast control voltage is input to pin 12 through R3 and L1. It is then divided into the Video contrast control signal and the color contrast control signal by the buffer circuit. The color contrast control signal is DC voltage without burst signal. The burst signal is removed by the low-pass filter circuit (R1, R2, C2 and C3). The video control control signal is DC voltage without burst signal. The burst signal is also eliminated by the low-pass filter circuit.

2-3-2 Burst Cleaning

The tank circuit (L1 and C4) is added to pin 12 for burst cleaning. R3 for contrast control and burst cleaning coil L1 are connected as shown in the above diagram. Its junction is connected to the ground through the 0.01μF capacitor The resonance level of the tank circuit is determined by L1 and C4. Its resonance frequency (f) is calculated as follows:

$$f = 1/2\pi\sqrt{L_1 \cdot C_4}$$

To adjust the resonance level, input ACC allowable signal to the chroma input pin, and change the L1 value while monitoring the pin 14 chroma output. When the resonance frequency is detected, the amplitude of the chroma output signal is reduced to a minimum level. At this time, the amplitude of the burst signal has increased to a maximum level.

2-4 Chroma Out (Pin 14)

Pin 14 is for outputting chroma signals and its output is based on open emitter circuit.

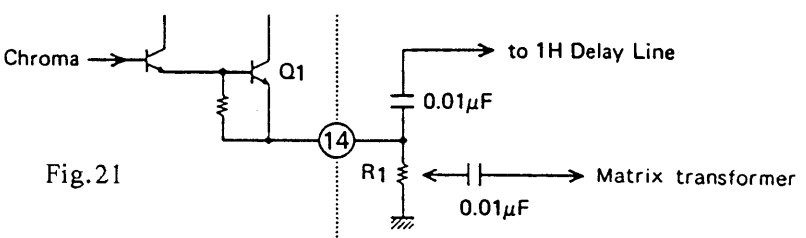


Fig.21

(1)PAL standard: The DC voltage level at pin 14 is about 6Vdc (VCC 9V), irrespective of contrast and color control voltages. The chroma signal is superimposed on the DC level output signal. Since the maximum supply current of Q1 is 10mA, select the R1 value with chroma signal in mind.

(2)NTSC standard: The DC voltage level is about 0V and no chroma signal is output. The standard R1 value is 1kΩ.

2-5 Ident Filter (Pin 15)

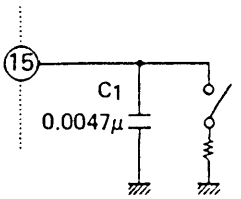


Fig.22

(1) PAL standard:
The phases of the PAL signal R-Y signal component and burst signal change every 1H. The signal detected and then output by ident circuit is input to this pin and smoothed by external capacitor C1. It is finally used for judging the phase of burst signal.
As the value of C1 is increased, noise immunity is improved as much. However, the judgment of burst signal phase takes longer time. The standard value of C1 is 0.0047μF as shown in the above circuit.

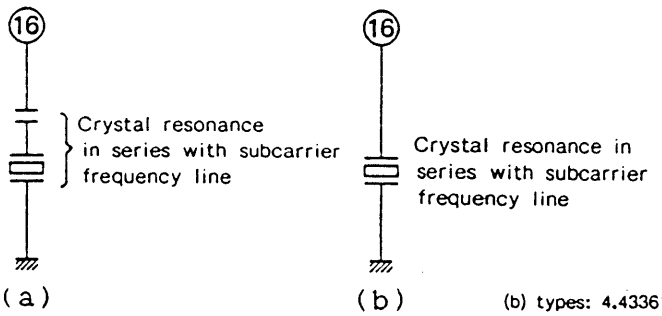
(2) NTSC standard:
NTSC standard requires no ident circuit. Set the pin voltage level to less than 3V for IC switching from PAL to NTSC. Connect this pin to the ground through a 1kΩ of protection resistance.

2-6 X-tal Pin (Pin 16)

Use a crystal (X'tal) oscillator in series with chroma subcarrier frequency line for resonance.

Example:

Fig.23



(b) types: 4.433619MHz - Kinseki EX0004
3.579545MHz - Kinseki EX0017

2-7 APC Filter (Pin 17)

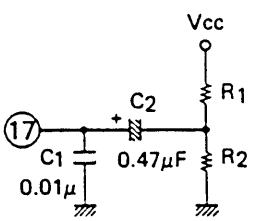


Fig.24

Pin 17 is an APC filter pin.
The internal APC reference voltage is about 6V (Vcc 9V). The DC voltage of this pin is about the same as 6V. Since the ripple rate of the APC reference voltage is is about 57%, the best ratio of R1/R2 is 0.75. If both of the R1 and R2 values are increased, pull-in range is widened. If they are decreased, the pull-in range is narrowed.

2-8 Tint Control (Pin 19)

(1) NTSC standard:
By applying DC voltage to this pin, TINT can be controlled. Since the internal reference voltage is 1/2Vcc, set this pin voltage level to the 1/2Vcc.

(2) PAL standard:
The PAL standard stops the internal TINT circuit operation. Even if voltage is applied to this pin, TINT cannot be controlled. DC voltage apply to this pin would not affect internal function blocks such as the TINT at all.

2-9 B-Y-In/R-Y-In (Pins 18 and 20)

Pins 18 and 20 are pins for receiving chroma signal from the chroma out pin (pin 14). This applies only to the PAL standard.

The output signal from pin 14 is divided into B-Y and R-Y components by the 1H delay line. The B-Y component is input to pin 18 while the R-Y component to pin 20.

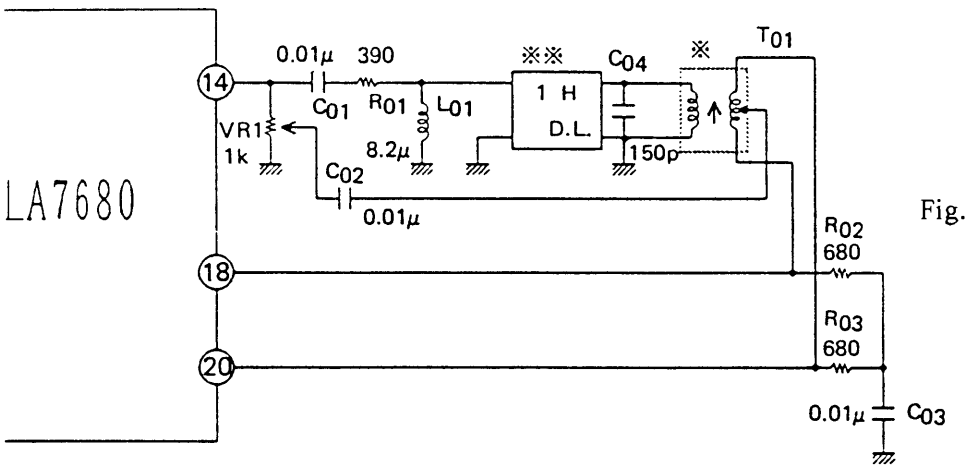


Fig.25

The input impedance of both pins is about 16kΩ. The DC voltage is about 3V DC for PAL and about 2.3V DC for NTSC, with the pins left open. The B-Y and R-Y component should be input to the pins according to this DC voltage.

C01, C02 and C03 are capacitors for DC shutout. The connecting point between R02 and R03 is connected to the ground through capacitor C03 for reducing noise and ripple. If noise or ripple is active, demodulator balance is degraded, causing large carrier leakage.

R01, R02, R03, and L01 are needed for 1H delay line matching. The output signal from pin 14 is divided into two signal components: B-Y and R-Y. VR1 is used for reducing the original signal by the combined loss of the 1H delay line and T01.

The demodulation output ratio can be changed by modifying R-Y or B-Y signal component, as shown below.

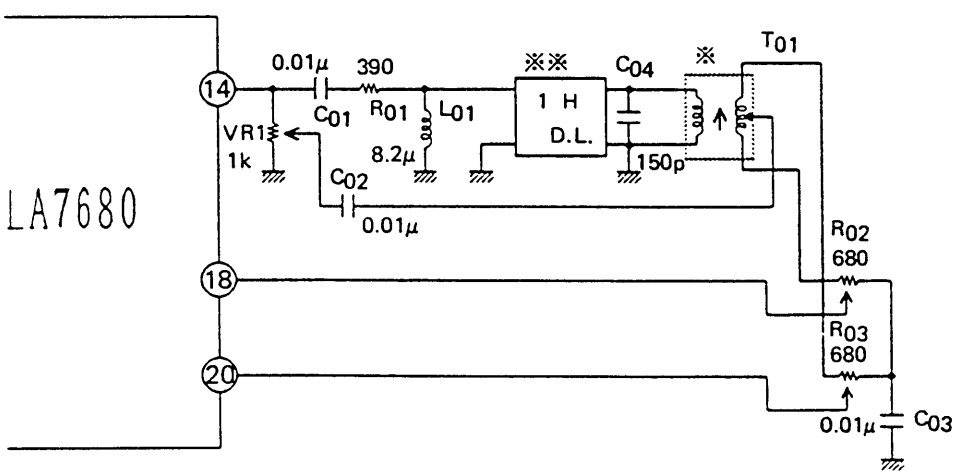


Fig.26

2-10 R-Y/G-Y/B-Y Colour Difference Output (Pin 21,22 and 23)

(1) Pins 21 and 23 are for R-Y and B-Y color difference output, respectively. Pin 22 is for G-Y color difference on the LA7680.

(2) Generally, the low-pass filter (270Ω and 390pF) is connected to the color difference pins for subcarrier filtration. However, it is not always required. Such an external filter has good effect on spark.

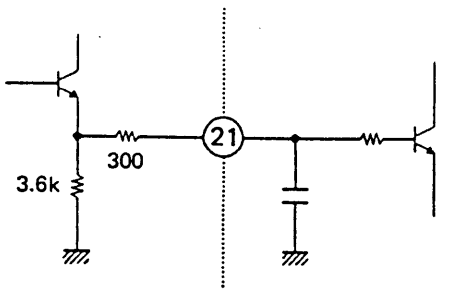


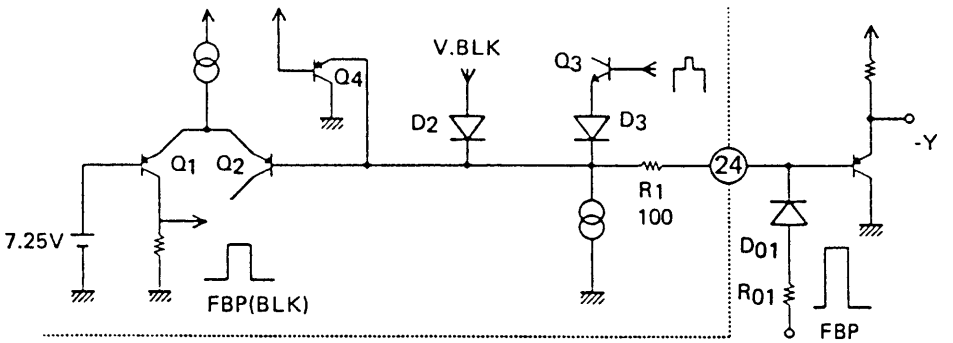
Fig.28
Applicable to pins 22 and 23
The above example circuit includes a low-pass filter for spark.

3. Video Out and Deflection

3-1 Video Output (Pin 24)

Pin 24 is for video output and for FBP input.

Fig.29

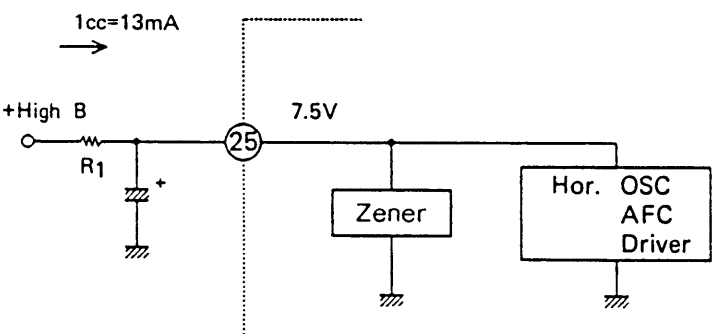


The video signal is output to pin 19 through Q3, and D3. By inputting FBP to pin 24 through D01 and R01, horizontal banking of the video output signal can be controlled. The FBP signal from pin 24 is taken into the IC by Q1 and Q2 (threshold voltage 7.25V) and used as horizontal banking pulse for chroma signal. Resistor R01 is used to restrict to less than 10mA the peak current flowing into pin 24 at the FBP input. Note that FBP is clipped by Q4 at Vcc + VBE point. The FBP ringing may be superimposed on the video signal (-Y) and cause screen output distortion. D01 is a diode used for preventing such a problem.
The horizontal banking is carried out automatically through D2. At this time, the 24-pin output voltage is about 7.2V (17.5H for NTSC and 21.5H for PAL).

3-2 Power Supply (Pin 25)

Pin 25 is power supply pin for horizontal deflection.

Fig.30



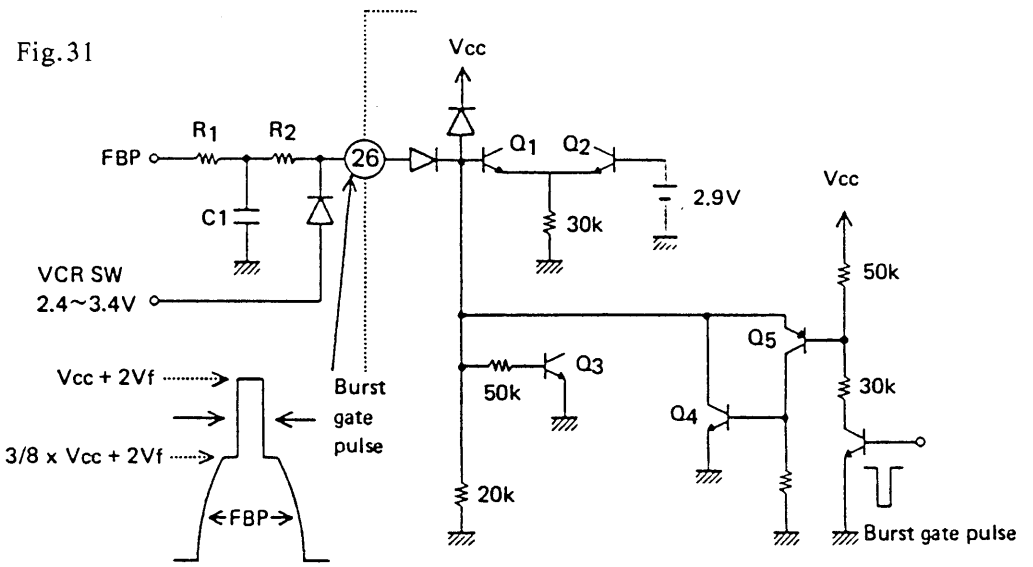
Select the R1 value in order for the current flowing into pin 25 not to reach 13mA.

$$R1=\frac{+B-7.5V}{13mA}$$

3-3 Fly Back Pulse Input,Burst Gate Pulse Output (Pin 26)

Pin 26 serves as a three-functional pin: flyback pulse input, burst gate pulse output and VCR switch.

Fig.31



3-3-1 Flyback pulse input

The flyback pulse at about 100V is input to this pin through resistors R1 and R2. The threshold voltage for flyback pulse input to the IC is 3/8 x Vcc + Vf. Resistors R1 and R2 are used for limitting to less than 5mA the peak current flowing into the internal IC (Q4). Input flyback pulses enter the AFC loop circuit for absorbing horizontal output and storage time. However, since the screen centering was offset in advance, change the R1-C1 integral value to carry out the screen centering.

3-3-2 Burst gate pulse output

Flyback pulses input to the pin through resistors R1 and R2 are limited by Q4 and Q5 at 3/8 x Vcc + 2Vf. The flyback pulse voltage rises up to Vcc + 2Vf only during burst gate pulse output. Because of this, the burst gate pulse is not output if screen phase adjustment is not complete.

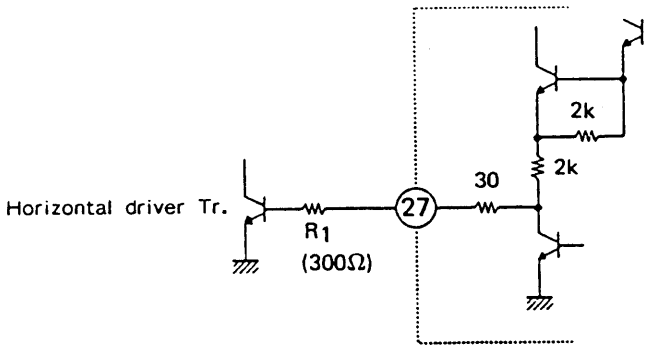
3-3-3 VCR switch

Pin 26 serves as the VCR switch by superimposing 2.4V to 3.4V DC voltage on input signal to this pin. This DC voltage causes Q3 to be always active.
If the VCR switch turns on, the normal AFC 1 (pin 29) control current is doubled. However, the VCR switch cannot function if vertical free-run operation like no channel has been started.

3-4 Horizontal Output (Pin 27)

Pin 27 serves as a horizontal output with push-pull specification.

Fig.32



3-5 Ceramic Resonator (Pin 28)

Pin 28 is used as the pin for connecting a ceramic resonator to the IC.

3-6 AFC Filter (Pin 29)

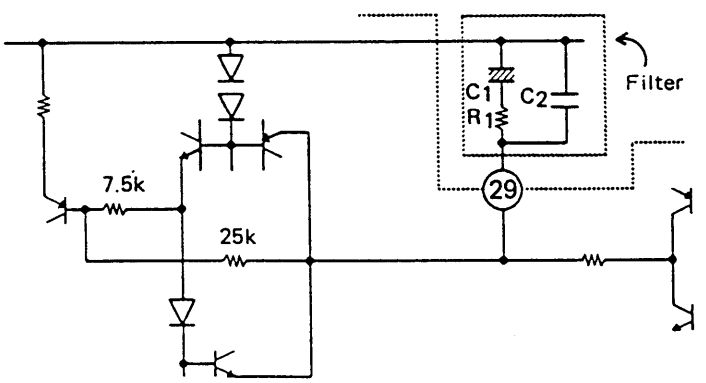
Pin 29 is an AFC1 filter pin.

Since the DC bias for AFC output is determined by 3×Vf from the power supply, the AFC filter should be placed close to the power supply for improving power ripple characteristics.

In the circuit diagram below, C1 is a capacitor for eliminating vertical ripple. Resistor R1 is for producing voltage from control current. And Capacitor C2 is used as a smoothing capacitor.

When the AFC control current is converted to voltage by resistor R1, pin 25 internally limits the voltage at ±1.5V.

Fig.33



3-7 Filter for Horizontal Sync (Pin 30)

Pin 30 is used as a filter pin for detecting horizontal synchronization signal. When horizontal screen image phase adjustment is complete, the voltage at pin 30 gets high. Otherwise, its voltage gets low.

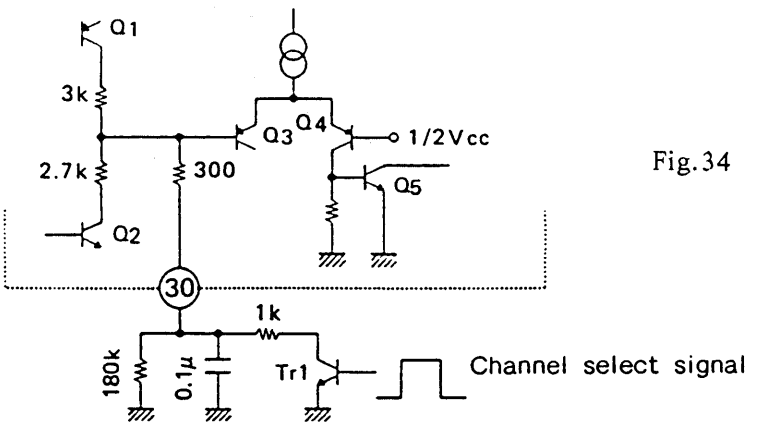


Fig.34

Q3 and Q4 forms a comparator using the 1/2 Vcc voltage as the reference voltage. If the voltage at pin 30 gets below 1/2 Vcc, horizontal synchronization is considered incomplete. In this case, virtual count-down mode is switched to nonstandard mode and at the same time horizontal AFC1 control current is doubled. Therefore, if the external time constant for pin 30 is small, the pull-in time at 4-channel selection is shortened.

However, if the external time constant is too small, the voltage at pin 30 easily gets low due to electric field effect and noise. The standard mode shows better stability than the nonstandard mode in electric field effect and noise. Therefore, the external time constant for pin 30 should be determinated, with electric field effect, noise characteristics, and synchronization pull-in speed in mind. Pin 30 can be used as input pin for channel select signal through transistor TR1 .

3-8 Vertical Output (Pin 31)

Pin 31 is connected with such vertical output ICs as the LA7835/36/37/38(SANYO). The LA7680 has the automatic select circuit for vertical synchronization signal cycle from 50Hz and 60Hz. It outputs the result to pin 31. If the LA7680 selects 60Hz, it outputs high to the pin. Otherwise,it outputs low to the pin.

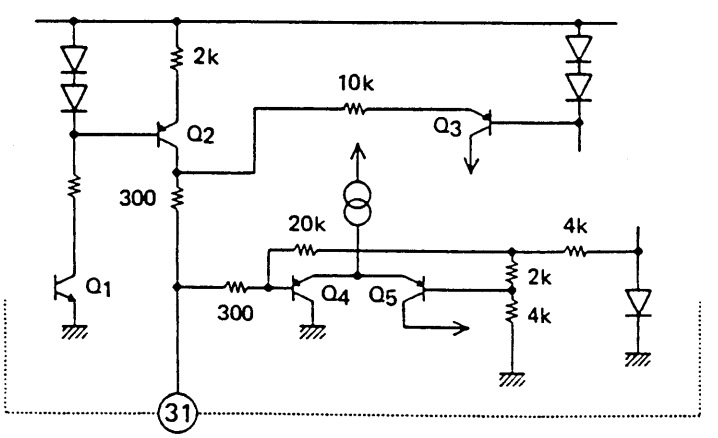
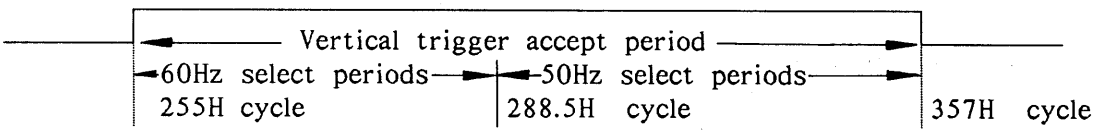


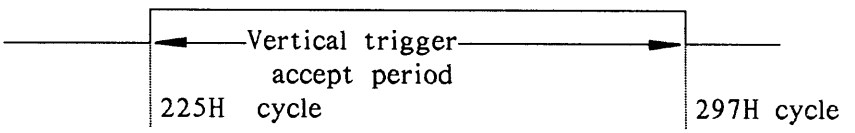
Fig.35

If the cycle of the vertical synchronization signal is fixed to 50Hz or 60 Hz, connect pin 31 to the GND or the Vcc.

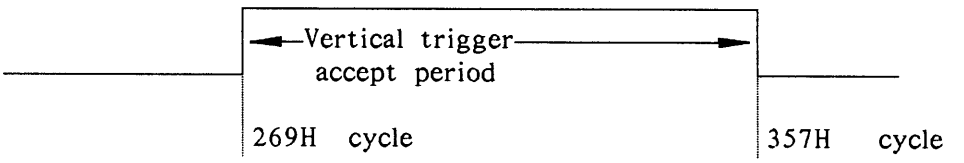
1)To use the internal 50/60HZ cycle select circuit:



2)To set the pin 31 voltage at higher than 8.7V:



3)To set the pin 31 voltage at lower than 0.15V:



3-9 Vertical Output,Sensitivity Setting (Pin 32)

Pin 32 serves as multi-functional pin: Vertical output, sensitivity setting for horizontal synchronization separation, external vertical trigger input,autotrigger mode release switch, and V-HOLD.

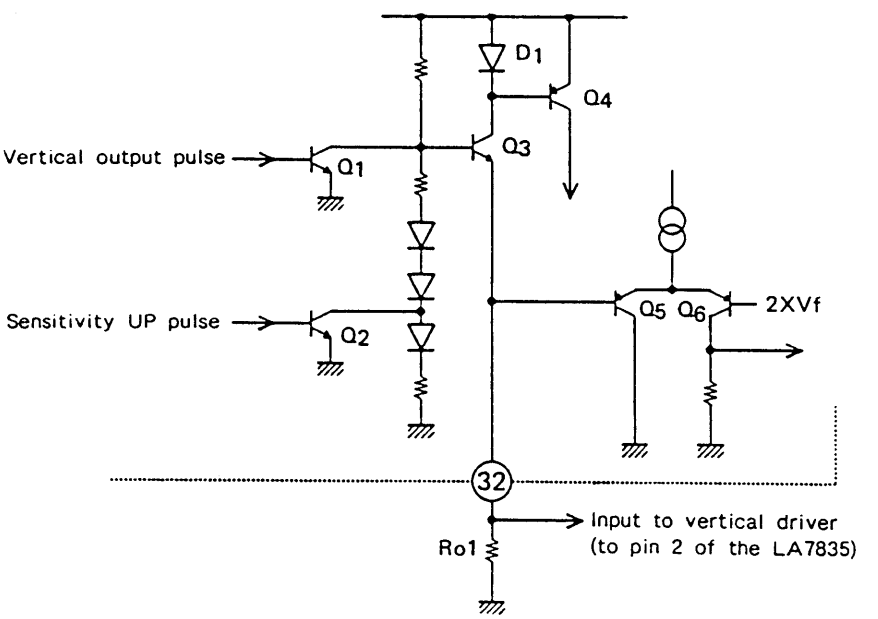


Fig.36

3-10 Vrtical Deflection Circuit

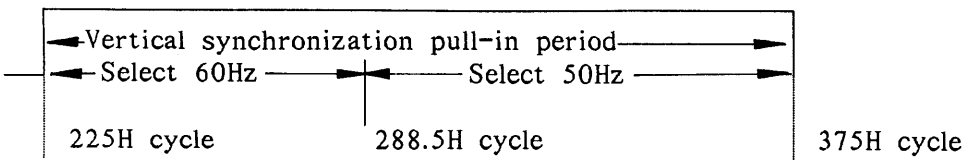
This system has a divider circuit using 2fH as the clock.

3-10-1 50/60Hz Automatic Select

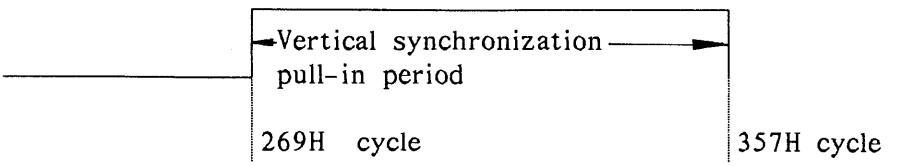
1 Ver ≧ 288.5 : Select50Hz

1 Ver < 288.5 : Select60Hz

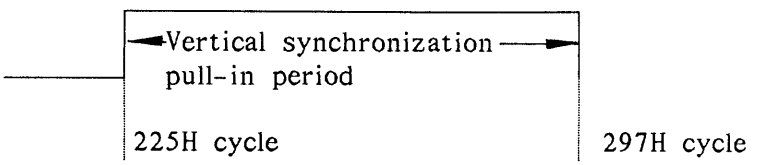
The pull-in period right after synchronization signal input is in the cycle period between 225 and 357, as shown below.



As stated above, if the vertical cycle is 1 Ver ≧ 288.5H, the automatic select circuit selects 50Hz. It then narrows the pull-in period as shown below.

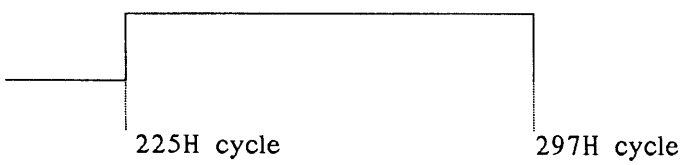


If the automatic select circuit selects 60Hz, it sets the pull-in period as shown below.

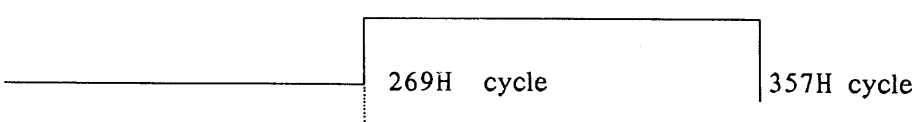


3-10-2 50/60 Fixed Function

To start the 60Hz fixed mode, apply the voltage higher than 8.7V (Vcc=9V) to pin 31. In this mode, the vertical synchronization pull-in period is set as shown below.



To start the 50Hz fixed mode, apply the voltage lower than 0.15V to the pin. In this mode,the vertical synchronization pull-in period is set as shown below.

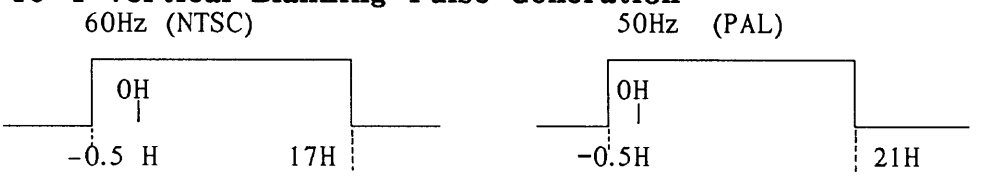


3-10-3 Standard/Nonstandard Judge Circuit

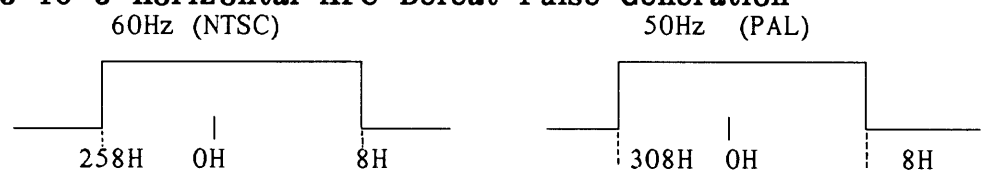
The standard/nonstandard judge circuit is provided for telling standard signals (1 Ver≒262.5H for NTSC or 1 Ver≒312.5H for PAL) from nonstandard signals (1 Ver≒262.5H or 312.5H).
This circuit consists of a base-8 (octal) counter and base-4 (nibble) counter.
It counts up for each Ver cycle.

If the standard signal counter advances to"8", this system resets the system using a pulse signal generated by the system divider. (Standard mode) This counter operate at 1 Ver=262.5H cycle (60Hz NTSC) and at 1 Ver=312.5H (50 Hz PAL). (Auto-trigger mode)
If the nonstandard signal counter advances to"4", the system is reset by the trigger pulse generated within the vertical synchronization pull-in period. (Nonstandard mode) This function works together with the horizontal synchronization signal detect function of pin 30.
The nonstandard mode is started up when the horizontal synchronization is not complete and the voltage at pin 30 gets below 1.2Vcc.

3-10-4 Vertical Blanking Pulse Generation



3-10-5 Horizontal AFC Defeat Pulse Generation



The horizontal AFC defeat period is an period of the above pulse period and the vertical synchronization signal period. Therefore, if the vertical synchronization signal period is longer than 8H, the horizontal AFC defeat period becomes longer as much.

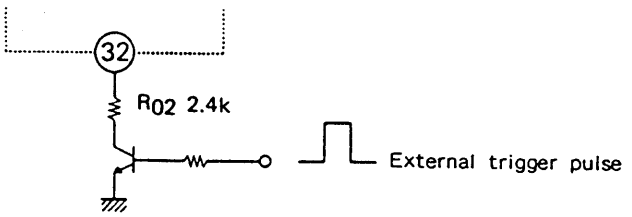
3-10-6 Free-Run Mode

If vertical and horizontal synchronization signals are not input, this system enters into free-run operation mode at 1 Ver 262.5H or 1 Ver 312.5H period. In this case, whether 1 Ver is 262.5H or 312.4H depends on 60Hz or 50Hz at each moment.
That is, when the system receiving 60Hz signals (NTSC) enters a no-signal state, the system is forced into free-run operation mode at 1 Ver 262.5H.
If the system receiving 50Hz signals (PAL) enters a no-signal state, the system is forced into free-run operation mode at 1 Ver 312.5H period.
The system can be operated at 1 Ver 262.5H by applying the voltage higher than 8.7V to pin 31. To start the system operation at 1 Ver 312.5H, apply the voltage lower than 0.15V to the pin.

3-10-7 External Trigger Input

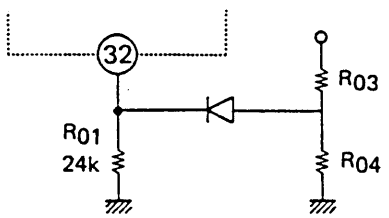
To output an external trigger pulse to an IC, supply the current greater than 1.7mA from pin 32 to the ground.
The synchronizable frequencies by the external trigger pulse is from 1/225H to 1/356.5H.

Fig.37



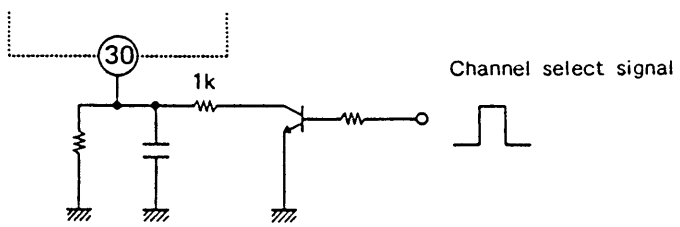
3-10-8 Auto-Trigger Mode Release Switch

Fig.38



To release the auto-trigger mode, add the clamp circuit in order for the 32 pin voltage not to get below 1.7V.
The auto-trigger mode can be released by setting 31 pin voltage level at lower than 1/2Vcc, as shown below.

Fig.39



The channel selection by this system requires 4 Ver periods so that the vertical image adjustment can be completed by the above three functions. To improve the synchronization signal pull-in speed, pin 30 or pin 32 should be used in the above-mentioned manner if the channel selection signal is used for this purpose. That is, both of pin 30 and pin 32 can be used as the release pins for the auto-trigger mode. In this case, there will be no problem if voltage is always applied to pin 32. However, the voltage level at pin 30 should not always be set to lower than 1/2Vcc because the primary function of this pin is to detect a horizontal synchronization signal. For more information on the pin 30 time constants, refer to the item dealing with pin 30.

3-11 Vertical Synchronization Signal Separation Sensitivity Setting

Output signal waveform of pin 32 for standard signal

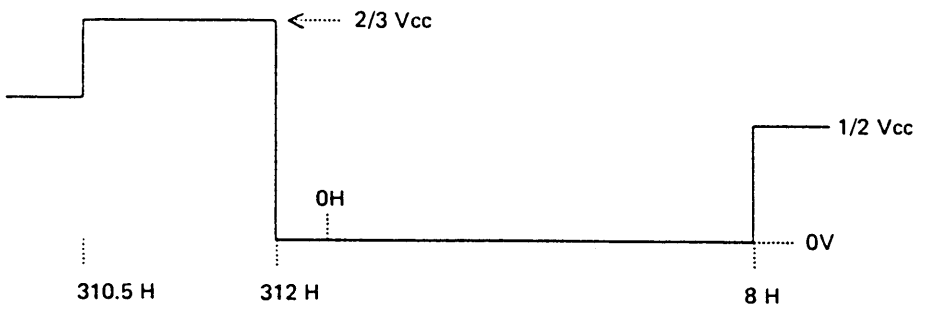


Fig.40

The vertical synchronization signal separation sensitivity can be set by changing the external R01 resistor value of pin 32. The sensitivity of the vertical synchronization separation has a high level period and a low level period. The 32-pin output signal waveform peak voltage during the high level period is 2/3Vcc. If the value of resistor R01 is set to 24kΩ, the minimum synchronization signal pulse width for vertical synchronization is 14μs during the high level sensitivity period and 23.5μs during the low level sensitivity period. This is not affected by change of the R01 value.

In addition, this system is designed to synchronize with the copy guard signal shown below, with R01=22kΩ.

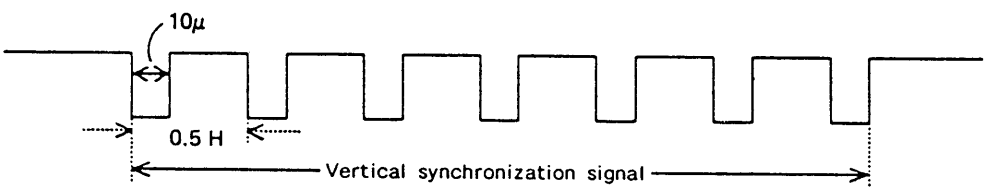


Fig.41

3-12 Sync Separation Input (Pin 33)

Pin 33 is used as a synchronization separation input pin.

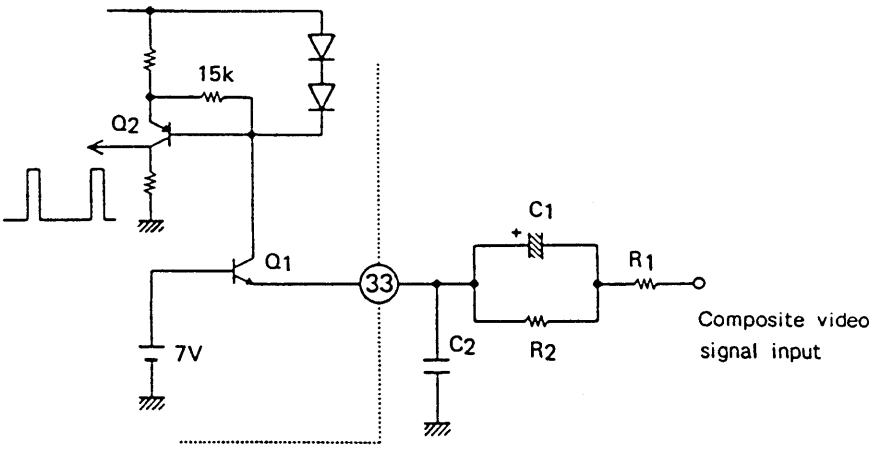


Fig.42

Set the C1 value to 0.22 to 1uF, and adjust R2 to produce the potential difference across R1 so that it becomes equal to about 30% of the synchronization signal. R1 is a resistor to supply the driving current for synchronization signal separation. The value of resistor R1 should be set to supply 300uA when the potential difference across R1 gets to 30% of a synchronization signal. C2 is used as a high-frequency filter for feeble electric field. The filter characteristics are determined by R1 and C2. Pin 33 is used to keep the black screen,for example, if no signal is input to video input pin after the TV set is switched to the video signal input mode .

3-13 AFC Operation

The horizontal defection circuit of the LA7680 is based on double AFC technique. The operational blocks and the waveforms of each block are shown below.

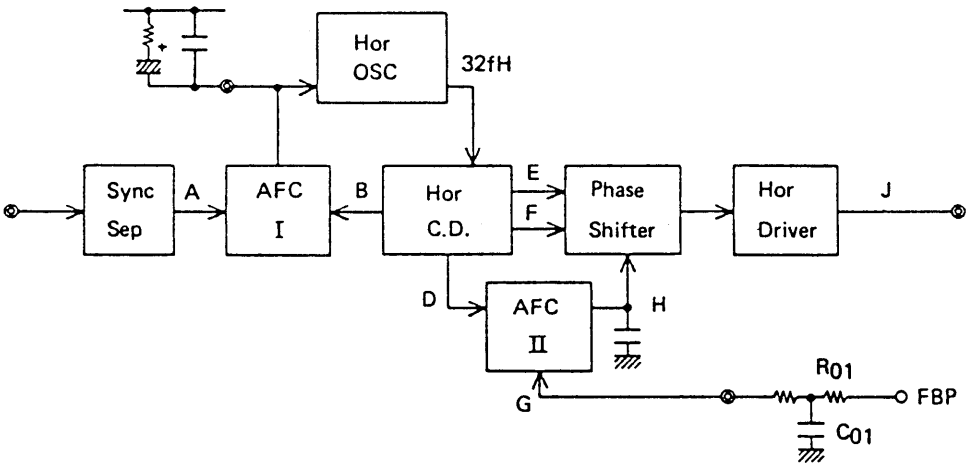


Fig.43

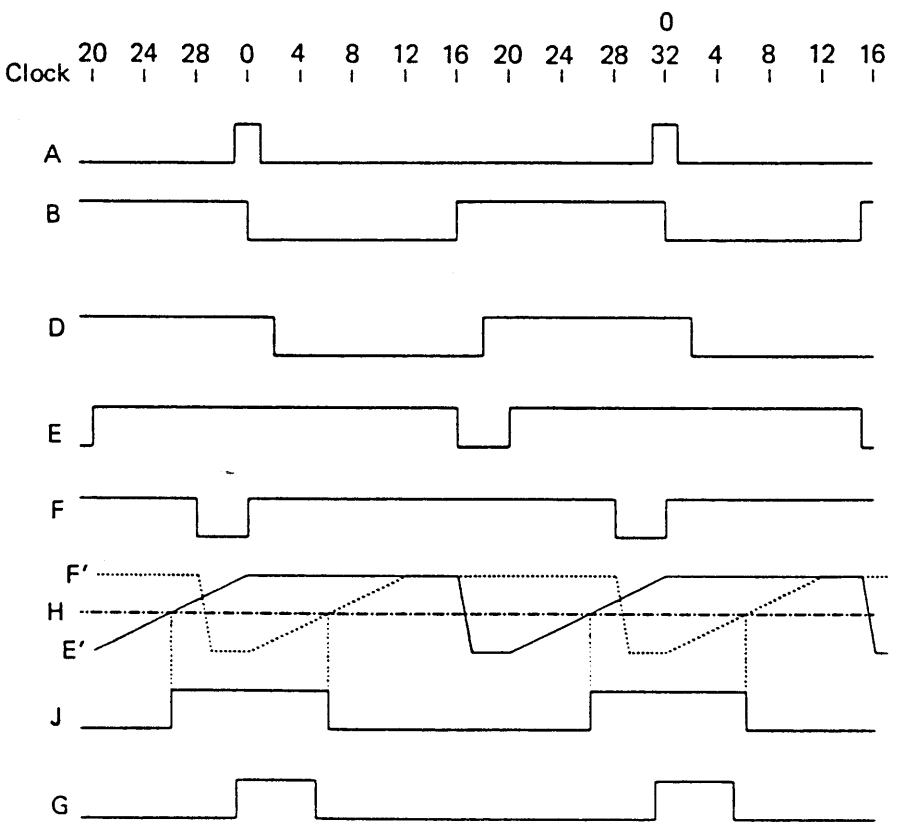


Fig.44

(1) The AFCI controls the horizontal OSC block so that the B pulse falls at the middle of the A pulse signal.
   A: Vertical synchronization signal
   B: fH (Pulse generated by dividing the horizontal OSC output by 32)

(2) The AFCII controls the phase shifter so that the D pulse falls at the middle of the G pulse signal.
   D: Pulse delayed 2 clocks (about 4μs) after B.
   G: FBP pulse delayed by R01 and C01.
   H: AFCII output voltage (As H voltage increases, the phase of signal J is delayed. Otherwise, it is advanced.)
   J: Horizontal driver output pulse

3-14 Brightness Control (Pin 35)

Pin 35 is a brightness control pin. The neutral voltage for brightness control is about 4.5V. At this voltage level, the output voltage of pin 24 (-Y out) is about 3V.
The relationship between the 24-pin output voltage and the brightness control voltage (V-brightness) is show below. Note that the V-brightness can be changed by using VR1.

$$\triangle V_{-y.out} = \frac{-6}{\left(1 + \frac{7R_{01}}{30k}\right)} \cdot \triangle V_{Bright}$$

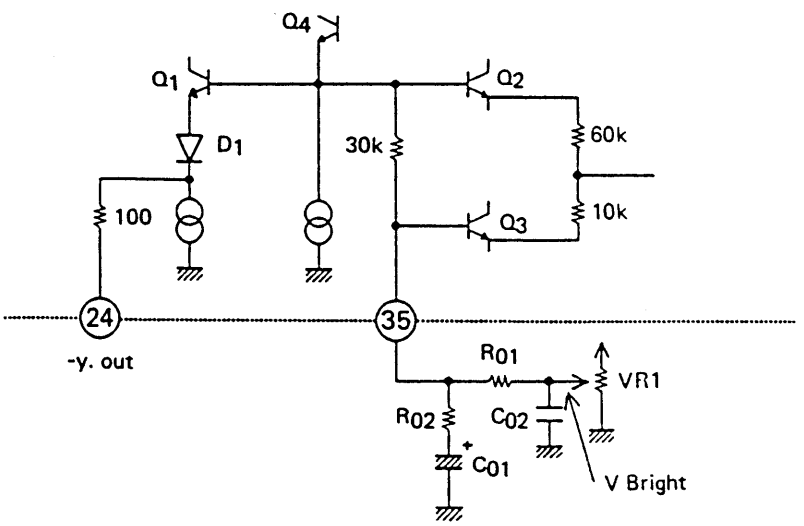


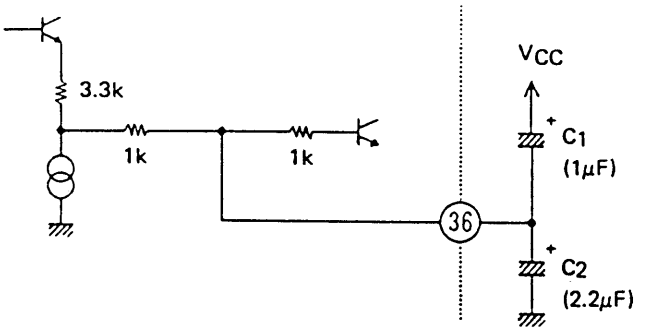
Fig.45

The DC restoration rate can be changed by using R02 and C01. The rate will be the highest if the R02 value is set to "infinite". If the R02 is shorted, the rate will be lowest.

3-15 Pedestal Clamping Filter (Pin 36)

Pin 36 is a filter pin for pedestal clamping.

Fig.46

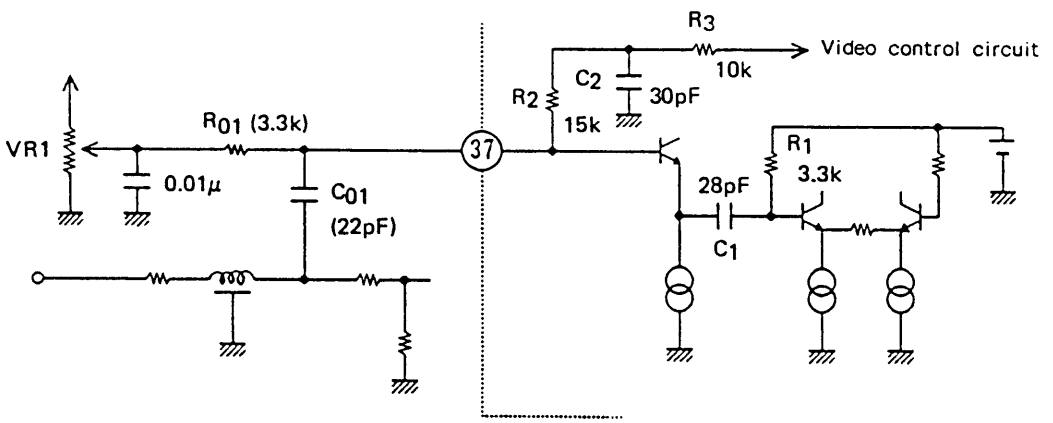


The output voltage of pin 36 is about 3.3V at brightness control neutral level. For transition response during power ON and OFF, two capacitors should be added externally as shown in the above figure. The ratio of C1 (connected with power supply)/C2 (connected with the GND) should be 1/2.

3-16 Video Tone Control (Pin 37)

Pin 37 is used as the second differential input and the video tone control pin.

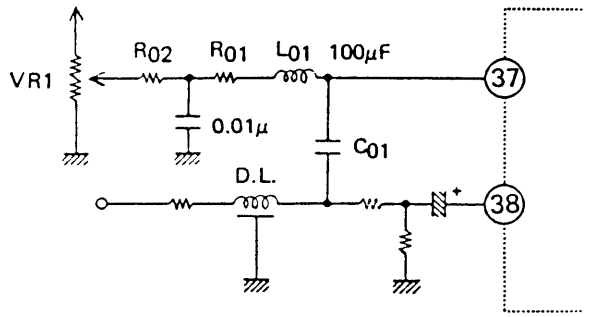
Fig.47



The second differential signal is generated from an input signal to pin 37 which is first differentiated by R01 and C01, and again internally by C1 and R1. The DC voltage from the video tone volume control VR1 is transmitted to the video tone control circuit through R01, pin 37, R2 and R3.

The neutral level of the video control is about 4V. By changing this voltage value, the second differential signal can be controlled.

Fig.48

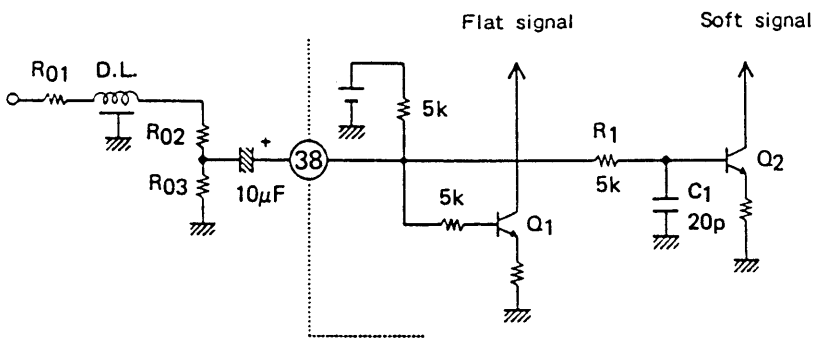


If the video tone is set to "sharp" and the pre-shoot and the undershoot of the -Y output waveform (pin 24) are not equal to each other, connect the coil (L01) to the circuit as shown above. Then, adjust the R01 value so that the pre-shoot and the undershoot can be equal to each other.
If the video tone is set to "soft", connect R02 to the circuit.

3-17 Video Signal Input (Pin 38)

Pin 38 is an input pin for video signal.

Fig.49

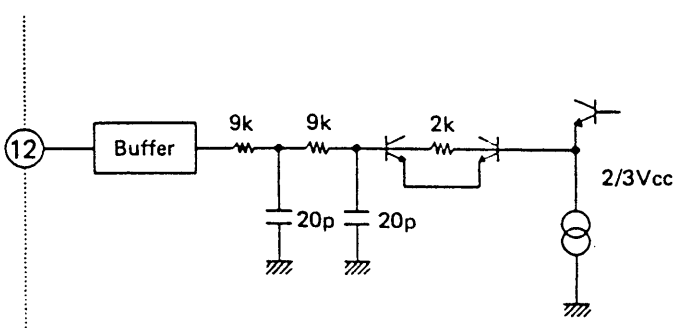


R01, R02 and R03 are matching resistors for delay line.
The standard input level at pin 38 is 0.5Vp-p to 0.8Vp-p. To adjust the input level, use R02 and R03.
The soft video tone signal is generated by removing high frequency component from the video signal of pin 38 with the low pass filter (R1 and C1). The softening can be controlled by changing the composition of the flat signal of Q1 and the soft signal of Q2 with the video tone control voltage from pin 37.

3-18 Contrast Control (Pin 12)

The contrast control is carried out at about 22dB. Its control neutral voltage is 2/3 Vcc.

Fig.50



[Part 3 Power Supply Circuit]

1. Operation Outline

As shown in Fig.1 the power-supply circuit of an A3 chassis is composed of the rectification smoothing circuit, the oscillation circuit, the control circuit and the output rectification circuit.

Fig.2 shows the voltage and current of each point in the normal operation of the power circuit. The AC input voltage is rectified in full-wave in the rectification smoothing circuit, and unstable DC voltage is smoothed by the smoothing capacitor C507. This unstable DC voltage is input to the oscillation circuit. In the oscillation circuit, the blocking oscillation circuit is used for the switching transistor Q513 to generate (in the input coil) the square-wave pulses and the oscillation frequencies corresponding to the operation of the control circuit.

The square-wave pulses obtained in the output coil have a dimension corresponding to the ratio of the input coil to the output coil; these pulses are rectified at the output rectification circuit, thus the desired DC voltage is obtained.

2.Explanation of Circuit Operation

2-1 Starting Operation

When the power is switched ON, a trickle current flows through the starting resistors R520 and R521 toward the switching transistor Q513 base, and a greater amount of collector current flows through the input coil (3)-(7) of the converter transformer. As a result, electromotive force is generated in the input coil (3)-(7), and voltage is also generated in the feedback coil (1)-(2).

This voltage is, through (R519, C514, R524), applied as positive feedback to the transistor Q513 base, thus the transistor is turned ON.

The above operations are performed in an instant, and enough base current is input into Q513 to maintain the ON state.

The collector current of Q513 amplified linearly as time passes according to the $i=V/L*t$ relationship. (Note; that L is the inductance value of the input coil)

2-2 Oscillation Circuit

Each operation of the switching transistor Q513 is explained below.

2-2-1 Switch Off Operation

(A) When the control circuit is not in operation.

The collector current is amplified linearly as time passes. When the collector current becomes hfe times as large as the base current, Q513 can no longer remain ON, and switches OFF immediately.

(B) When the control circuit is in operation .

When Q513 is ON , the positive pulses are generated in the feedback coil(1)-(2), and are integrated to make the sawtooth-wave pulses. The composite voltage is made from these pulses and the fluctuation of the output voltage, and is applied to the base-emitter of Q512. When this base-emitter voltage reaches the a sufficient value (approx. 0.6V-0.7V), the transistor Q512 is turned ON. Then the base current of Q513 is bypassed to the collector-emitter of Q512, and Q513 is immediately switched OFF. The fluctuation of voltage, mentioned previously, is detected on the second side of T511.

When Q513 is switched OFF, the energy stored in the input coil (3)-(7) during the ON period is supplied to the load side from the output coil through the output rectification circuit.

At this time, the current flowing in the output coil attenuates as time passes.
Refer to Fig.2(f).

2-2-2 Switch On Operation

The current flowing in the output coil attenuates as time passes, and when it finally reaches zero,the T1 period ends and the T2 period start.
At this time, resonance is caused by the inductance of the coil (3)-(7) of the converter transformer,T511, and the distribution capacity is inserted equivalently in parallel with T511.

The resonant current flows toward terminal (3) from terminal (7) in the input coil, and as a result, because the generated current flows toward the terminal (2) from the terminal (1) in the feedback coil, Q513 remains OFF.

The resonant current becomes maximum at the end of the T2 period, and the differential coefficient of the current becomes zero.

After that, the polarity of the differential coefficient of the current is inverted. As a result the current directed toward the terminal (1) from terminal (2) is generated in the feedback coil, and applied to the base of Q513.

Thus, Q513 is switched ON momentarily by the positive feedback action in the feedback coil, even if there is only a slight base current.

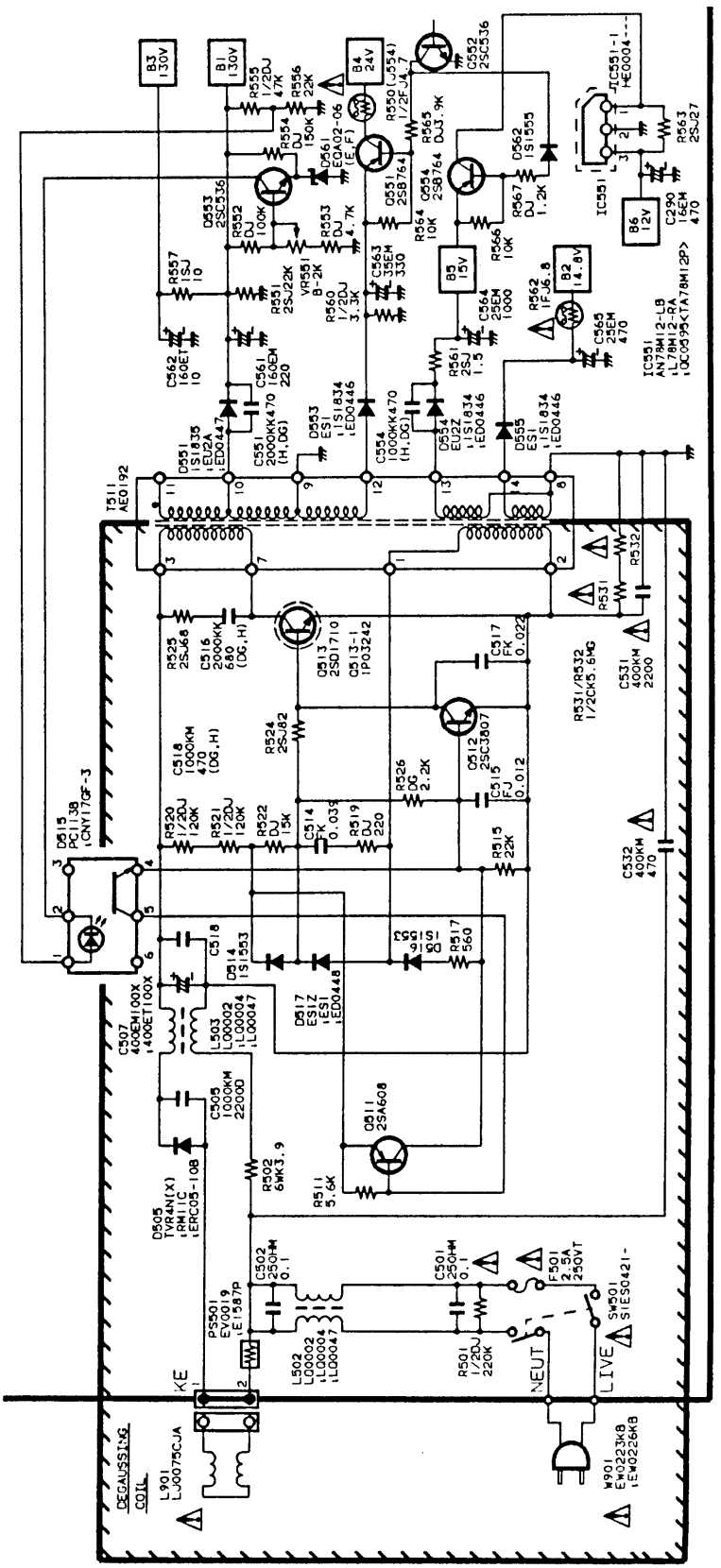


Fig.1 Power supply circuit

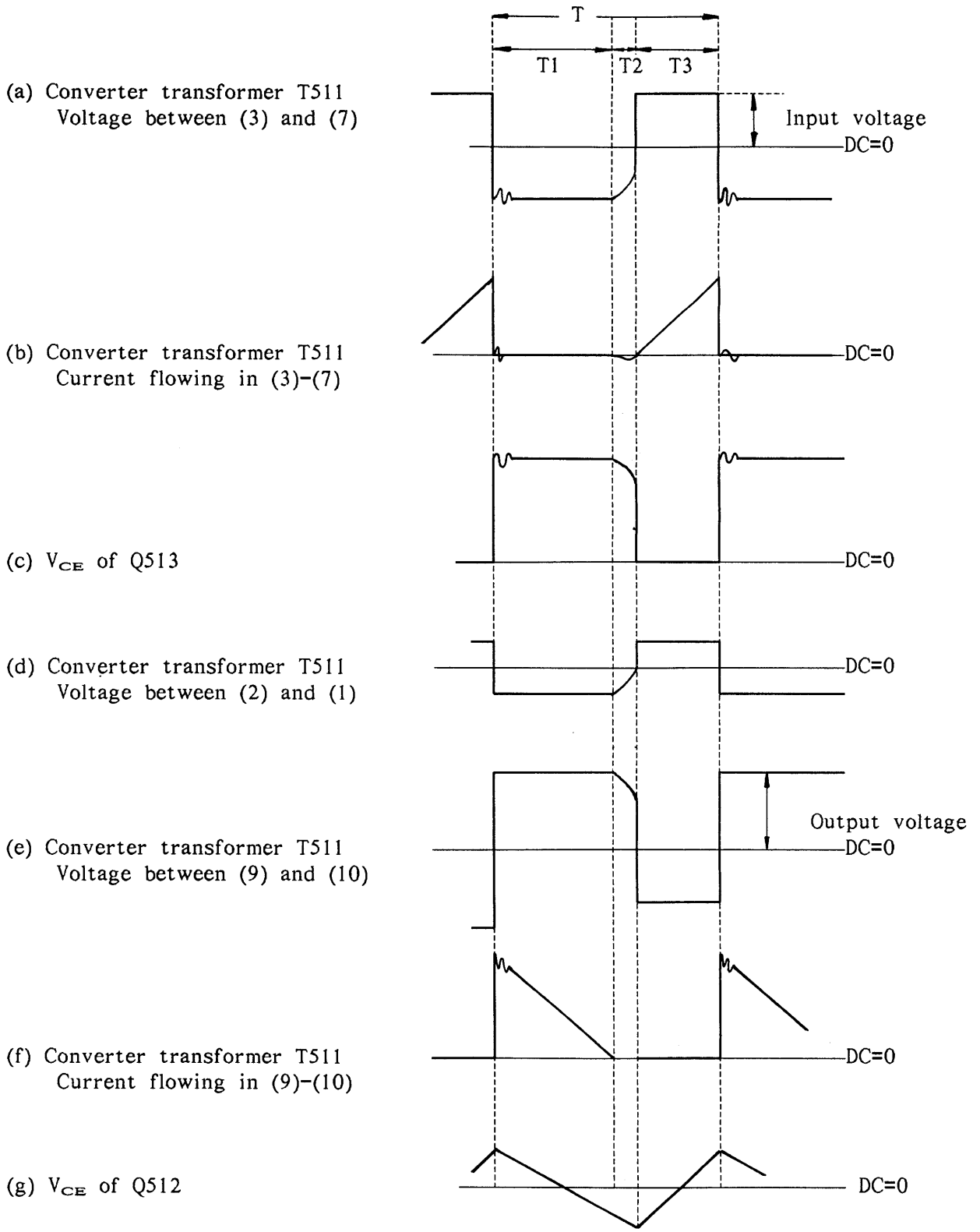


Fig.2 Operation voltage and current waveforms

[Part 4 Vertical Deflection Output IC LA7837]

1. Overview

The LA7837 is the vertical deflection output device designed for use with colour televisions monitors and displays. It incorporate a builtin ramp generator circuit, constant vertical amplitude function for 50/60 Hz operation, thermal protection circuit and pump-up circuit. The LA7837 provides deflection current up to 1.8 Ap-p. This device offer a number of improvements over previous vertical deflection ICs, resulting in simplified circuit and board design with enhanced performance. This include:

* Newly developed driver functions on-chip which allow the AC/DC feedback loop to be implemented with a single IC, thus reducing problems with cross talk from the horizontal signals affecting interlace characteristics. Earlier devices included the previous stage small-signal processing IC in the AC/DC feedback loop. Interlacing and vertical jitter problems occurred frequently since the feedback loop had to physically span two separate devices.
* Improved noise immunity by treating the vertical trigger input as a pulse signal rather than as a linear signal. This limits the effects of noise, and particularly horizontal signal noise, even if the noise is induced onto the connection lines from the previous stage IC.
* Built-in driver amplifier so that the gain of the vertical output amplifier is determined by one device, whereas previously the total gain of the vertical output stage was the product of the previous stage small-signal processing IC gain and the gain of the vertical output section. This improvement results in a major reduction in instability and gain variation problems when different devices are combined.
* Improved cross-over distortion performance, making these devices particularly suitable for high-picture quality, large-screen equipment.
* The LA7837 is available in 13-pin SIPs, which include a built-in heat sink.

2. Features

* Low power consumption
* Minimum external parts count
* Stable interlacing and vertical jitter characteristics
* Constant vertical amplitude for both 50 Hz and 60 Hz operation
* Built-in ramp generator, driver circuit and pump-up circuit
* Vertical output circuit with thermal protection
* Low linearity fluctuation with vertical screen size
* Limited output DC bias fluctuation with vertical frequency

3.Block Diagram and External Connections

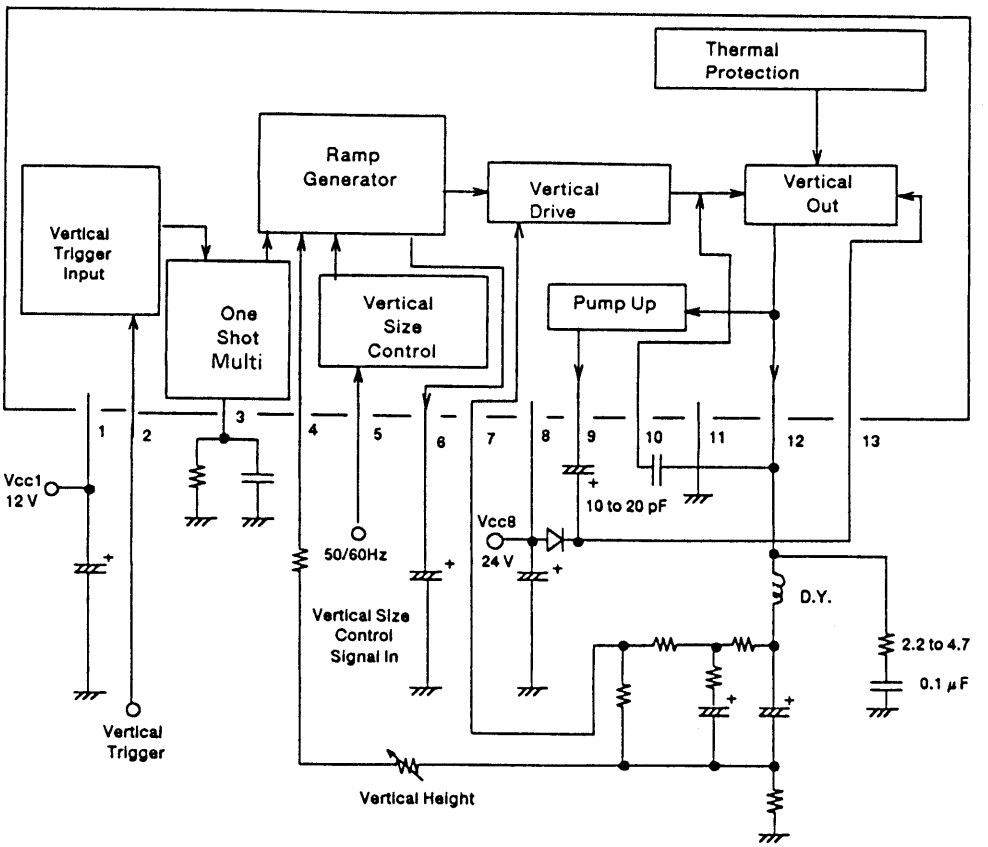


Fig.1

4.Pin Description

Pin		Function
Number	Name	
1	Vcc_1	Input and driver stages positive power supply input
2	IN	Vertical trigger input
3	TC	One-shot time constant
4	I_{RAMP}	Ramp waveform control current
5	50/60	50/60 vertical amplitude control input
6	C_{RAMP}	Ramp waveform integration capacitor
7	FB	Vertical output negative feedback input
8	Vcc_7	Pump-up circuit positive power supply input
9	C_{PUMP}	Pump-up capacitor
10	C_{FILT}	High-frequency stability filter capacitor
11	GND	Power supply ground
12	out	Vertical deflection output
13	V_{CC13}	Output stage positive power supply input

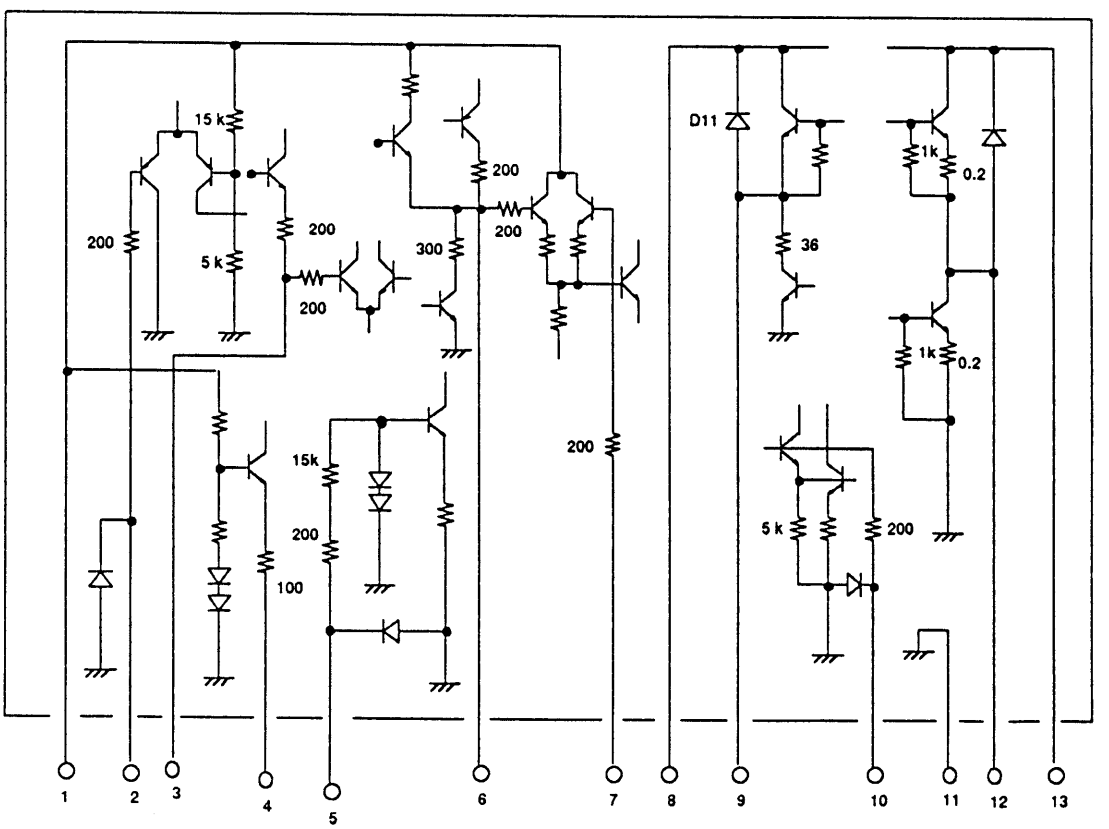


Fig.2 Pin internal circuit

5. Functional Description

5-1 Vertical Trigger Input

The vertical trigger input circuit shown in Fig.3 is driven by the negative polarity vertical sync pulse from the previous stage small-signal processing IC. The falling edge of the input pulse is inverted by the differential amplifier and drives the ramp generator. This pulse is differentiated and only the leading edge used by the ramp generator, ensuring that fluctuations in the input pulse width will not affect circuit operation.

The input threshold level of the trigger circuit is approximately Vcc/4. The input trigger waveform is shown in Fig.4.

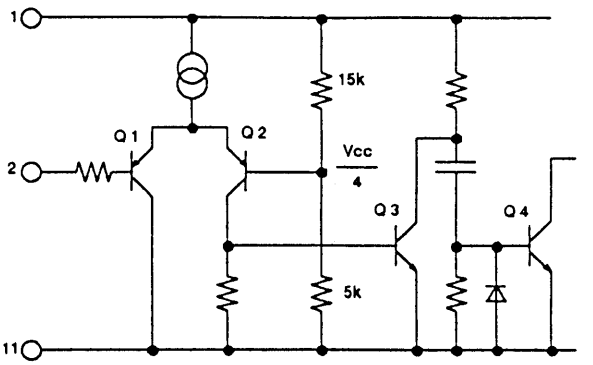


Fig.3 Vertical trigger input circuit

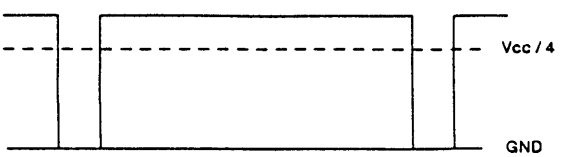


Fig.4. Vertical trigger input pulse

5-2 Ramp Generator

The ramp generator circuit shown in Fig.11 generates the vertical deflection sawtooth waveform. The circuit consists of the one-shot circuit, a current source and a limiter. The sawtooth wave is generated by charging and discharging the 1 μF tantalum capacitor connected to pin 6. The charging current of this capacitor is generated by a Miller circuit constant current source controlled by the current drawn from pin 4. The voltage on pin 4 is held constant at approximately $Vcc_1/2$, hence the peak value of the sawtooth wave can be changed by varying the pin 4 external resistance.

The current at pin 4 with the recommended peak sawtooth voltage of 1.5V, 1μF tantalum capacitor on pin 6, and 60 Hz vertical frequency is given by

$$Q=CV=IT$$

$$\therefore\ I = \frac{CV}{T} = \frac{1\mu F \times 1.5V_{P-P}}{1/60Hz} = 90\mu A$$

For a vertical frequency of 50Hz, the current is:

$$I' = \frac{CV}{T'} = \frac{1\mu F \times 1.5V_{P-P}}{1/50Hz} = 75\mu A$$

5-3 One-Shot

The one-shot circuit clamps the sawtooth voltage following trigger input, to a value of 5/12 Vcc_1. The one-shot period is set by the time constant on pin 3.

By clamping the start of the sawtooth at this voltage, fluctuation of the sawtooth start voltage by the horizontal components is prevented. This measure removes the major source of interlace problems, giving the LA7837 excellent interlace characteristics.

5-3-1 One-shot Time Constant

The one-shot period must be shorter than the vertical retrace period. If it exceeds this period, the sawtooth waveform will still be clamped when the scan line starts. It is suggested that the clamp period, Tc, be set to approximately half the vertical retrace time, TR, ensuring that Tr will be less than Tc even if vertical size is changed.

Interlace characteristics do not change with Tc, provided Tc is less the TR and greater than approximately 200μs.

5-3-2 Time Constant Calculation

The time constant on pin 3 is formed by a capacitor C_O=0.01μF and a resistor R_O, where the clamp time $T \fallingdotseq 0.7C_OR_O$.

For a vertical retrace period of 1 ms, setting R_O to 68kΩ gives $Tr \fallingdotseq 0.7X0.01X10^{-6}X 68X10^3 \fallingdotseq 0.476ms$.

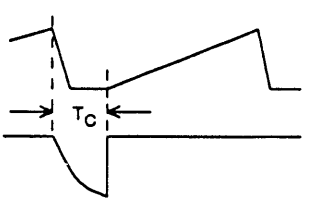


Fig.5 Clamp Waveforms

5-4 Constant Amplitude and Feedback Circuit

The LA7837 IC incorporate circuitry to keep the sawtooth amplitude constant for vertical frequencies of both 50Hz and 60Hz. This ensures a constant screen size for both 50Hz and 60Hz operation when used in dualmode 50Hz/60Hz PAL/NTSC television receivers. This function is controlled by pin 5, the 50Hz/60Hz amplitude control Pin.

* Dual mode
  For 50Hz vertical frequency, pin 5 is grounded. For 60Hz vertical frequency, pin 5 is either connected to pin 1 or to a DC voltage of 3V or more to increase the sawtooth generation current by 20%, thus giving the same screen size as for 50Hz operation.
* 50Hz or 60Hz single mode
  Pin 5 is permanently grounded since it is not needed. Note that it should not be left open, in order to prevent possible damage due to static discharge.

5-5 Driver Circuit

The driver circuit shown in Fig.6 has a differential input stage driven by the sawtooth waveform (waveform (b) in Fig.7). The negative feedback waveform at pin 7 (waveform (a) in Fig.7) derived from the vertical deflection output is applied to the other input of the differential amplifier.

The feedback waveform is created by summing the parabollc waveform generated by the vertical output coupling capacitor C3 and the sawtooth waveform produced by the AC feedback resistor R6 in Fig.11. The feedback operates so that the DC base voltages of the differential amplifier transistors Q7 and Q8 are balanced.

As well as the feedback loop to the differential amplifier, a second loop is formed by feeding the sawtooth amplitude control current from the AC feedback resistor R6 through a fixed resistor and a variable resistor (R1 and Vertical Height in Fig.11). Thus, the sawtooth voltage across resistor R6 modulates the current into pin 4. Since this current is integrated by the capacitor on pin 6, the whole feedback loop effectively cancels the parabolic component of the pin 7 negative feedback waveform due to the waveform component from the vertical output coupling capacitor C3.

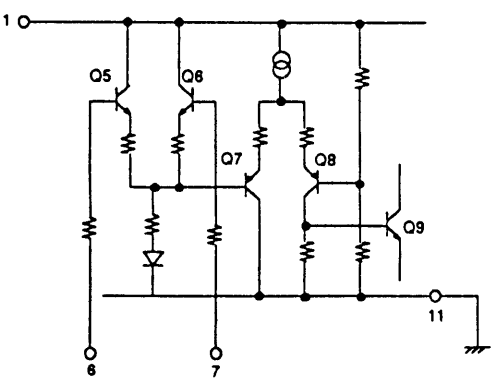


Fig.6 Driver Circuit

5-6 DC Bias Control

DC bias stability depends on correct balance of the pin 6 and 7 waveforms described above.

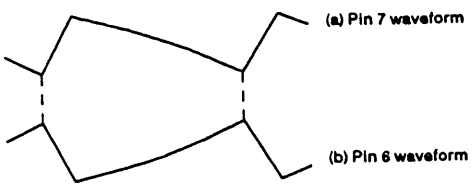


Fig.7 Driver Input Waveforms

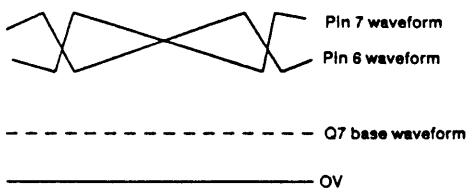


Fig.8 Driver circuit DC waveforms

The minimum DC voltage of the sawtooth waveform at pin 6 is fixed at approximately 5/12 Vcc_1 by the ramp generator circuit. Hence, if the peak value is 1.5Vp-p, the average DC level with a supply voltage on pin 1 of 12V is (5V + 6.5)/2=5.75 V. For a supply voltage of 9 V, the average DC level will be (3.75V + 5.25V)/2-=4.5V. Since the waveforms at pins 6 and 7 are balanced, the average DC level on pin 7 is approximately the same as the average DC level on pin 6. Taking this level to be 5.75 V, and noting that pin 7 is bleeder-connected to resistors R5, R3, R2 and R6, the voltage V_A at the positive side of the vertical output coupling capacitor is given by

$$\frac{V_A(R_2+R_6)}{R_5+R_3+R_2+R_6}=5.75V$$

Then,

$$V_A=\frac{R_5+R_3+R_2+R_6}{R_2+R_6}\times 5.75V$$

Since R6 << R5,R2,R3,

$$V_A \fallingdotseq \frac{R_5+R_3+R_2}{R_2} \times 5.75V$$

Hence the vertical output mid-point voltage is determined by the relative resistances of R2, R3 and R5. To determine the values of R2, R3 and R5, substitute

$V_A \fallingdotseq 12V$

$R_2 = 47k\Omega$

into the expression for V_A above and solve for (R3+R5):

$$R_3+R_5 = \frac{12V \times 47k\Omega}{5.75V} - 47k\Omega = 51k\Omega$$

$$= 51k\Omega$$

For R3=12k, R5=51k-12k=39k, a picture with satisfactory linearity is obtained with R4 $\fallingdotseq$ 1kΩ

However, R4 must be individually trimmed for each circuit to obtain optimum linearity. The value of the AC feedback resistance R6 is set so that the sawtooth amplitude is 1.5 Vp-p when the optimum deflection current flows through R6. For example, if the optimum current is 1 Ap-p,

$$1Ap\text{-}p \times R6 = 1.5Vp\text{-}p$$

$$\therefore R_6 = 1.5\ \Omega$$

5-7 Linearity Correction Circuit (S-Correction)

The linearity correction circuit consisting of resistors R5, R4 and linearity correction capacitor C2 integrates the parabolic waveform generated by the vertical output coupling capacitor C3 shown in Fig.11. This third-order function is bleeder-divided by resistors R4, R3 and R2, and S-correction applied by summing it with the pin 7 AC feedback wave form. The amount of correction is determined by the R4/C2 time constant and the R3/R5 bleeder resistance ratio.

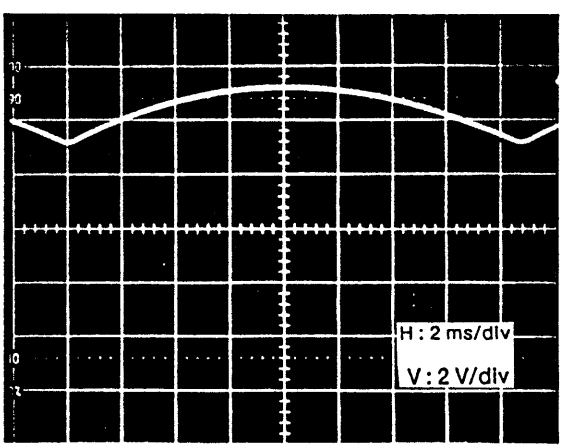


Fig.9 Coupling Capacitor Parabolic Waveform

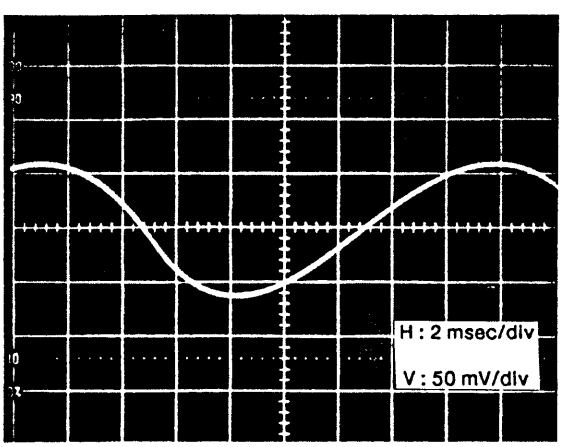


Fig.10 Linearity Correction Capacitor 3-rd Order Waveform

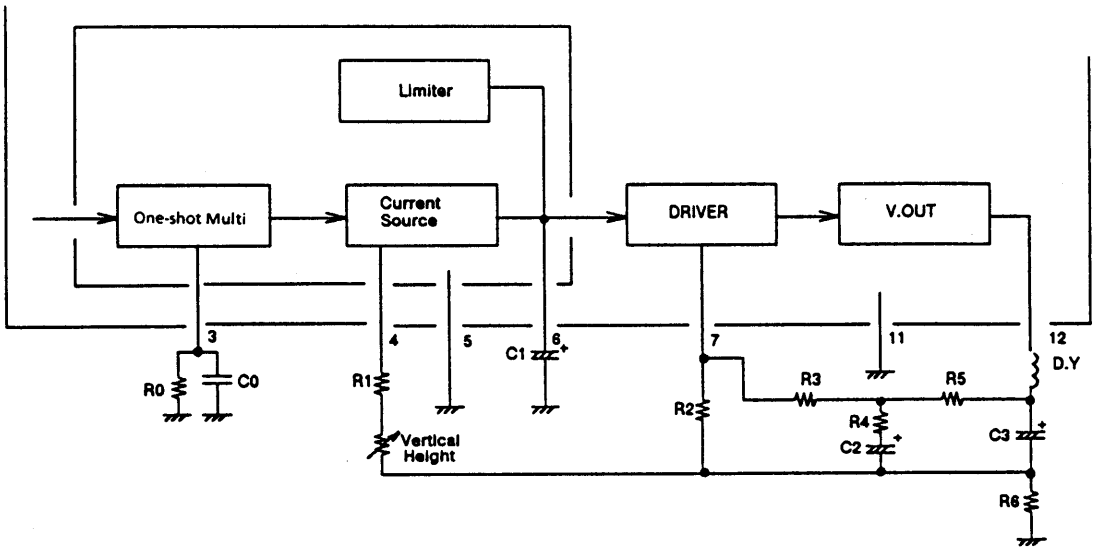


Fig.11 Ramp Generator and Feedback Circuit

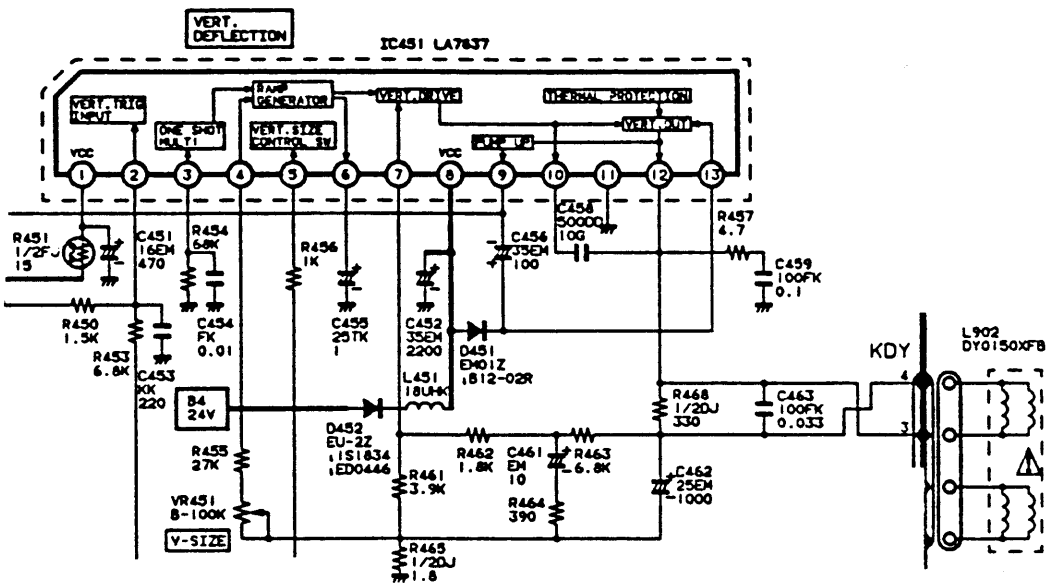


Fig.12 The Schematic Diagram of the Vertical output circuit

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