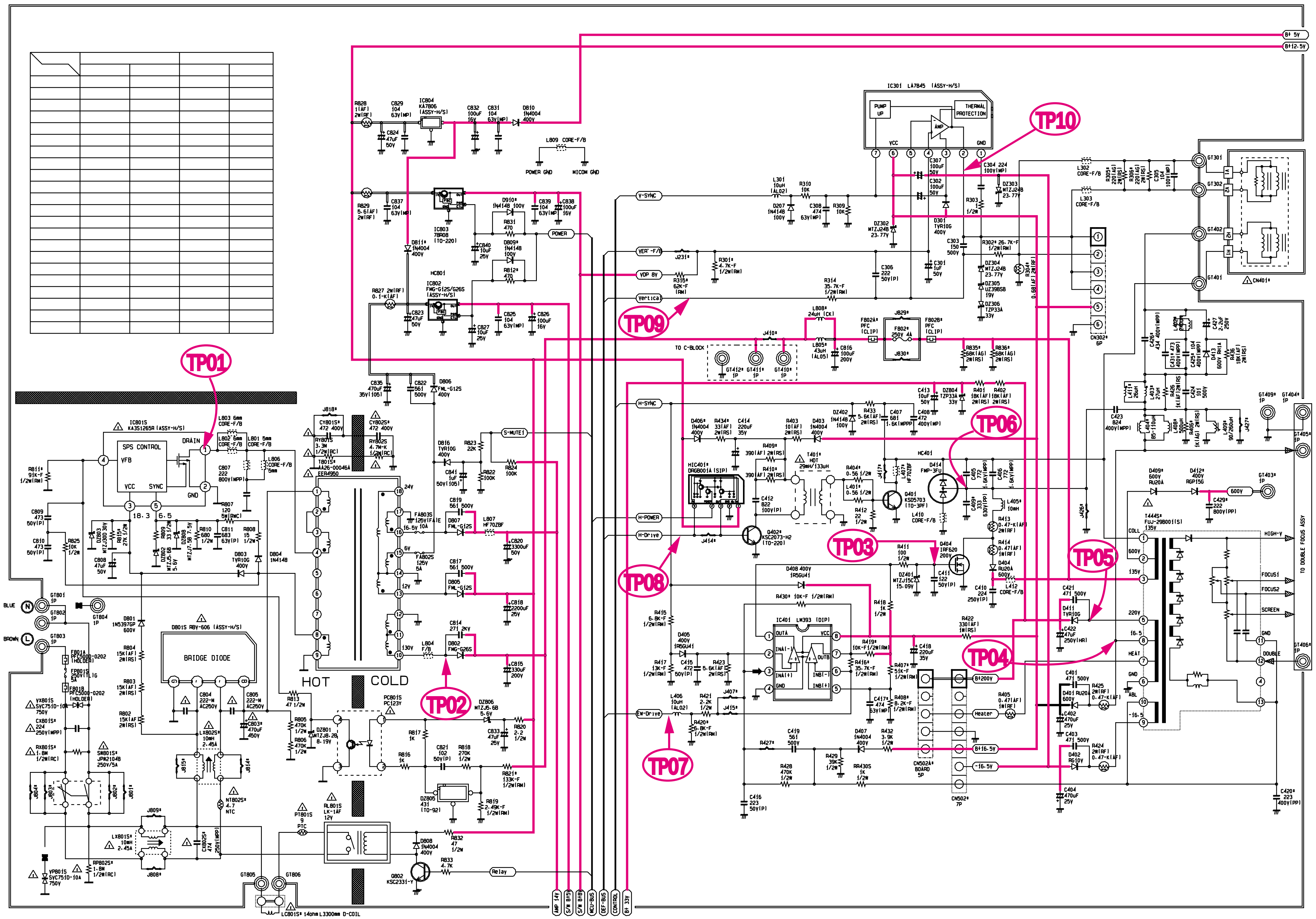
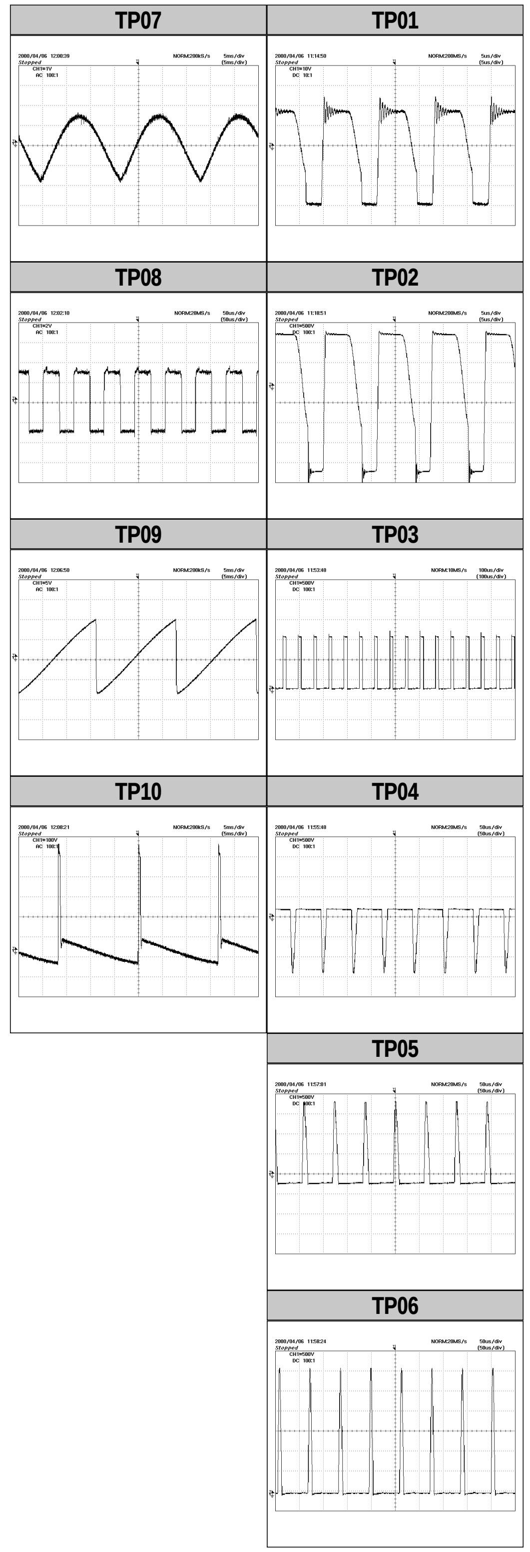
10. Schematic Diagrams

10-1 MAIN 1

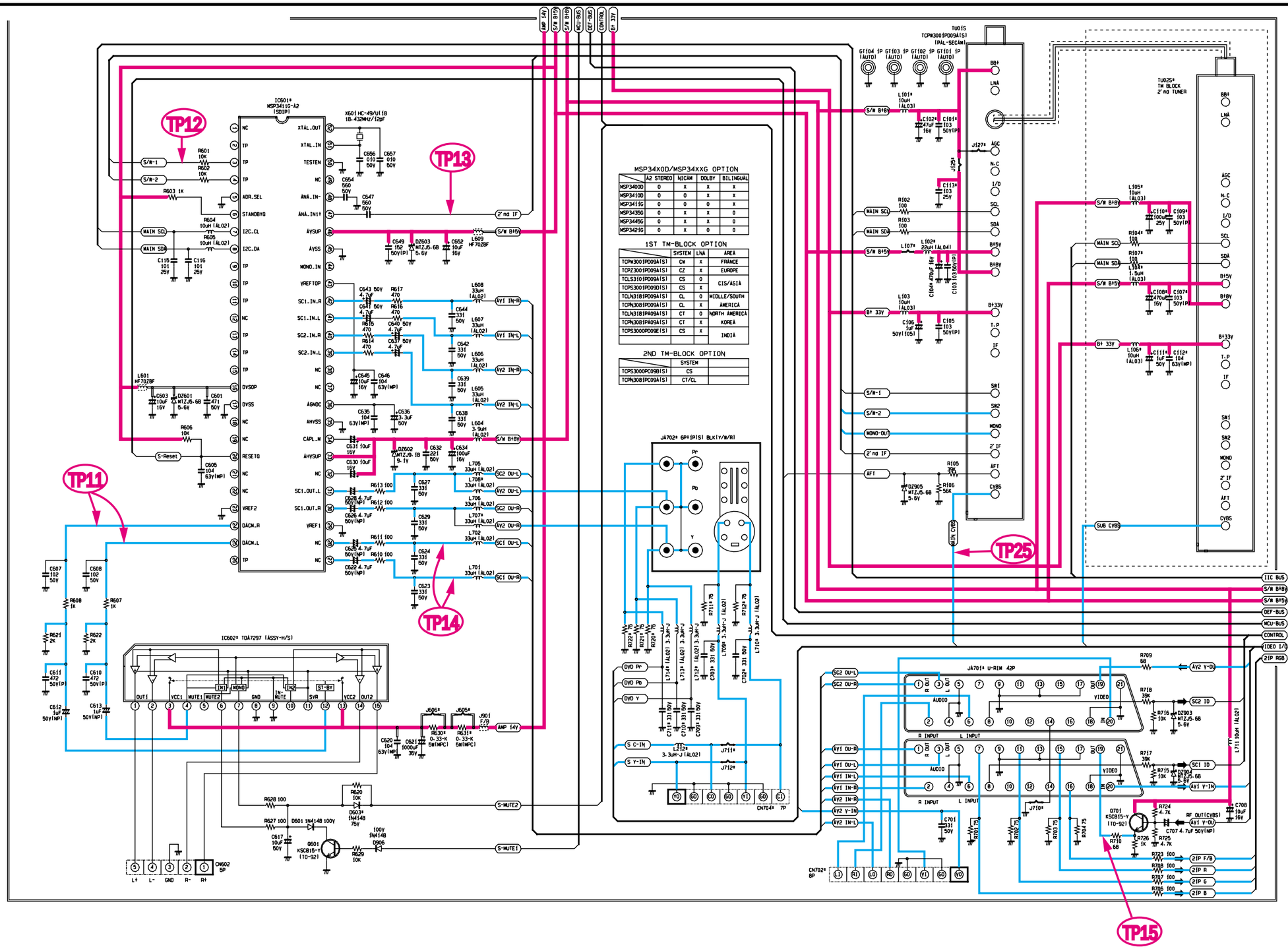




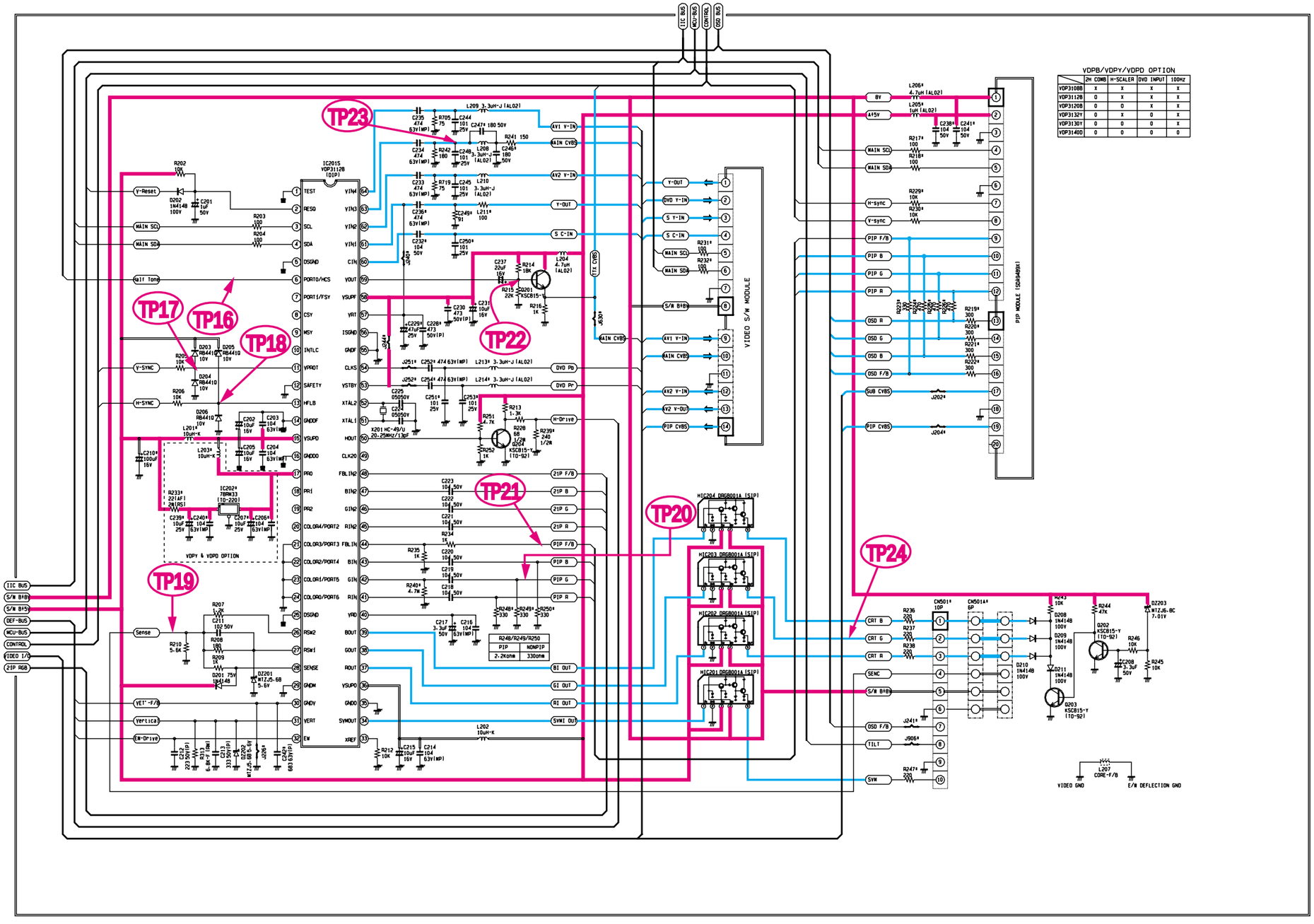
: Power Line

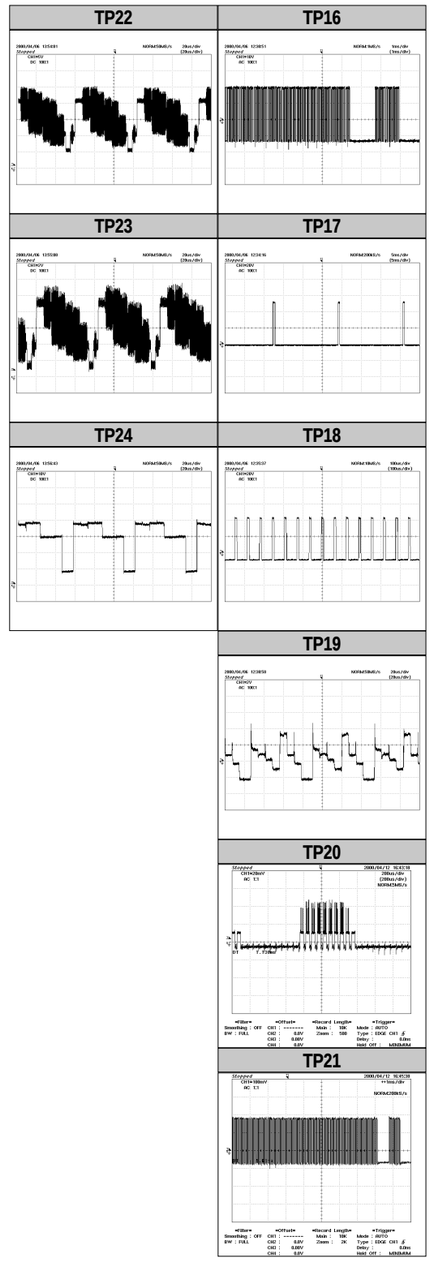
: Signal Line

10-2 MAIN 2

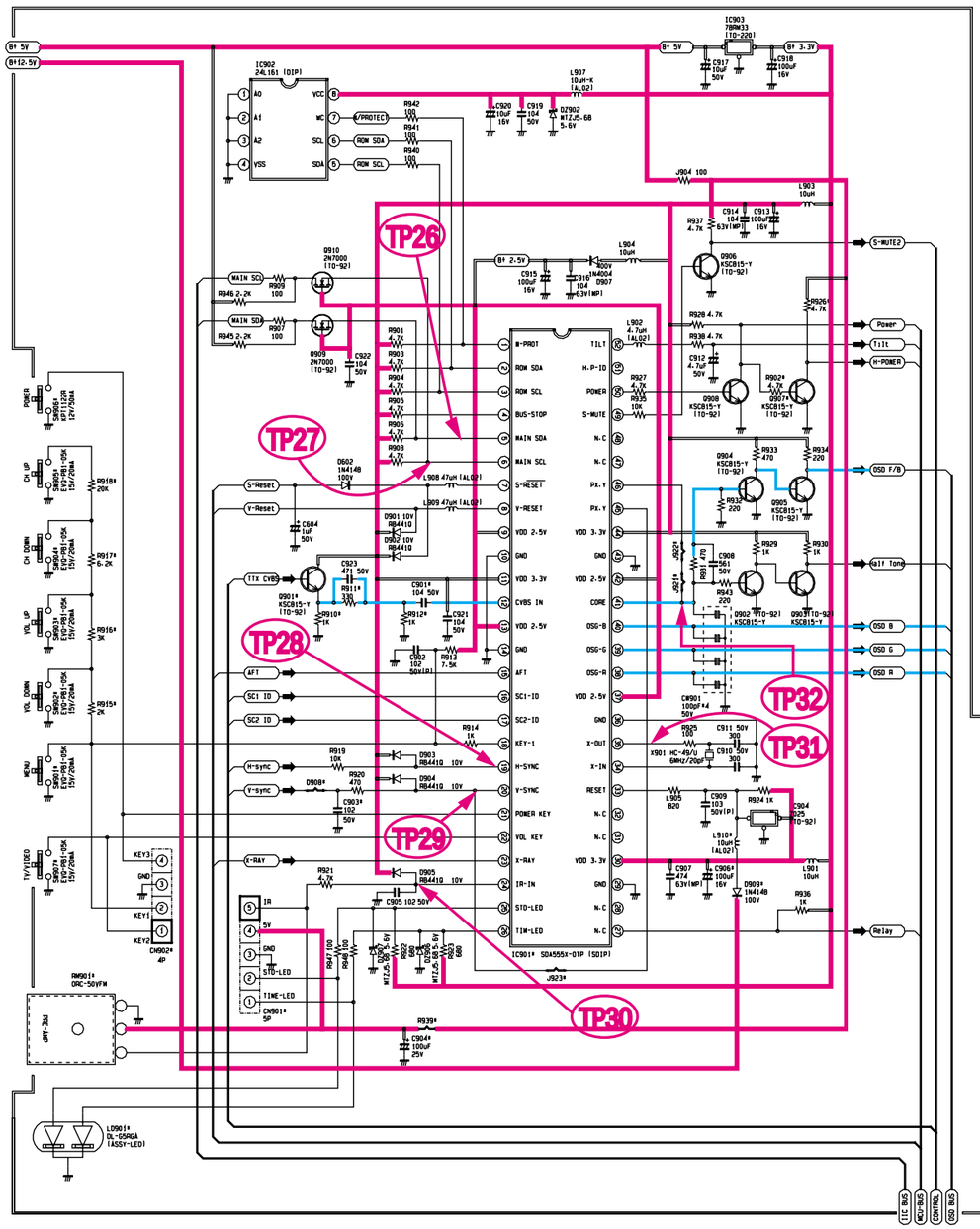

AMP 14V
S/W B+5V
S/W B+8V
MCU-BUS
DEF-BUS
CONTROL
B+ 33V
TP11
TP12
TP13
TP14
TP15
TP25
IC601* MSP3411G-A2 (SDIP)
X601 HC-49/U(18 18.432MHz/18pF
IC602* TDA7297 (ASSY-M/S)
TU01S TCPW300(PD09A1S) (PAL-SECAM)
TU02S* TM BLOCK 2'nd TUNER
MSP34X0D/MSP34XXG OPTION
1ST TM-BLOCK OPTION
2ND TM-BLOCK OPTION
JA702* 6P(PIS) BLK(Y/B/R)
JA701* U-RIM 42P
2'nd IF
S/W B+8V
S/W B+5V
MAIN SCL
MAIN SDA
S-MUTE1
S-MUTE2
AV1 IN-R
AV1 IN-L
AV2 IN-R
AV2 IN-L
SC2 OU-L
AV2 OU-L
SC2 OU-R
AV2 OU-R
SC1 OU-L
SC1 OU-R
DVD Pr
DVD Pb
DVD Y
S C-IN
S Y-IN
IIC BUS
DEF-BUS
MCU-BUS
CONTROL
VIDEO I/O
2IP RGB
SUB CVBS
MAIN CVBS
: Power Line
: Signal Line

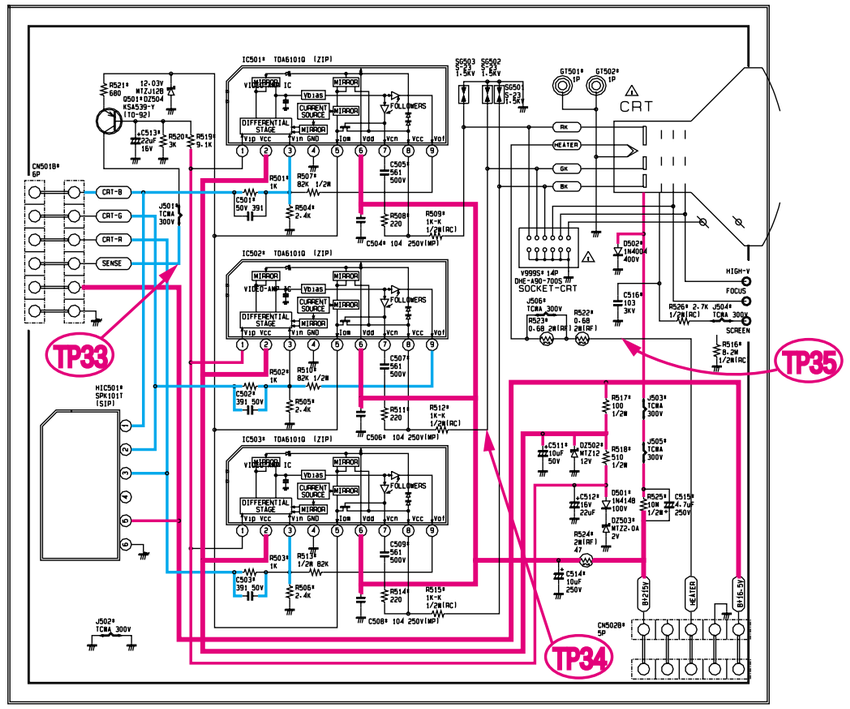
10-3 MAIN3


IIC BUS
MCU-BUS
CONTROL
OSD BUS
IC201S VDP3112B (QIP)
TP23
TP17
TP16
TP18
TP22
TP21
TP20
TP24
TP19
VIDEO S/W MODULE
PIP MODULE (SDA5489A)
VDPY & VDPD OPTION
VDPB/VDPY/VDPD OPTION
2H COMB | H-SCALER | DVD INPUT | 100Hz
VDP3108B x x x x
VDP3112B 0 x x x
VDP3120B 0 0 x x
VDP3132Y 0 x 0 x
VDP3130Y 0 0 0 x
VDP3140D 0 0 0 0
R24B/R24S/R250
PIP | NONPIP
2.2Kohm | 330ohm
: Power Line
: Signal Line


TP22
TP16
TP23
TP17
TP24
TP18
TP19
TP20
TP21

10-4 MAIN 4





KS3A MAIN SCHEMAIC DIAGRAM

CAPACITOR	
Ceramic - SL	No Mark
Ceramic - RH	(RH)
Ceramic - CH	(CH)
Polyester(Induct)	(P)
Polyester(Noninduct)	(PNU)
Polypropylene	(PP)
Metal Polyester	(MP)
M.P.Polypropylene	(MPP)
Tantalium	(T)
Non Polar	(NP)

RESISTOR	
Carbon	No Mark
Composition	(RC)
Metal Oxide	(RS)
Metal Film	(RN)
Fusible	(RF)
Cement-Wire	(RW)
Network	(RN)

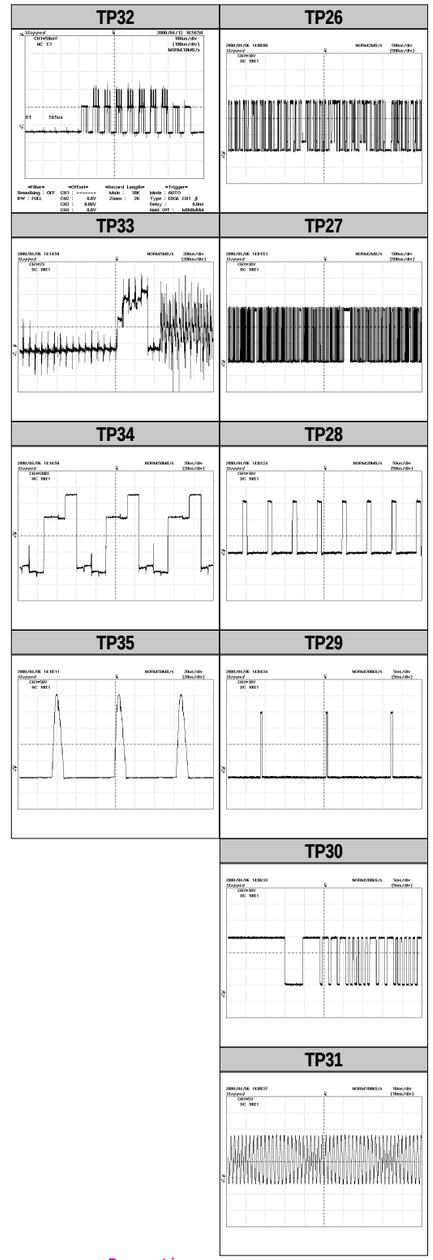
NOTE
1. Resistance is shown in ohm K=1,000 M=1,000,000
2. Unless otherwise noted in schematic all capacitor values less than 1 are expressed in uF. and the values more than 1 in pF.
3. Unless otherwise noted in schematic all inductor values more than 1 are expressed in uH.
4. Voltage read with V.T.V.M (input impedance 2M Ma/all range) from point indicated to chassis ground using a color bar signal with all control at normal line voltage 120 volts.
5. Waveforms in chrominance circuit are taken receiving a color bar signal with enough sensitivity.
6. Waveforms in other circuit are taken using an signal under normal receiving conditions.
7. Voltage readings shown are normal values and may vary 20% except H.V.
8. This is fundamental circuit diagram some production changes may be made without revision of the diagram.
9. The circuits enclose in dotted lines are optional parts. (*)

WARNING : BEFORE SERVICING THIS CHASSIS READ THE 'X-RAY RADIATION PRECAUTION' 'SAFETY PRECAUTION' AND PRODUCT SAFETY NOTICE' IN MANUAL.

CAUTION The shaded Area in the schematic diagram and the parts list designate components which have special character istics important for safety and should be replaced only with types indentical to those in the orignal circuit of specified in the parts list. Before replancing and of these components. Read carefully the PRODUCT SAFETY NOTICE. In this manual. Do not degrade the safety of the receiver through improper servicing.

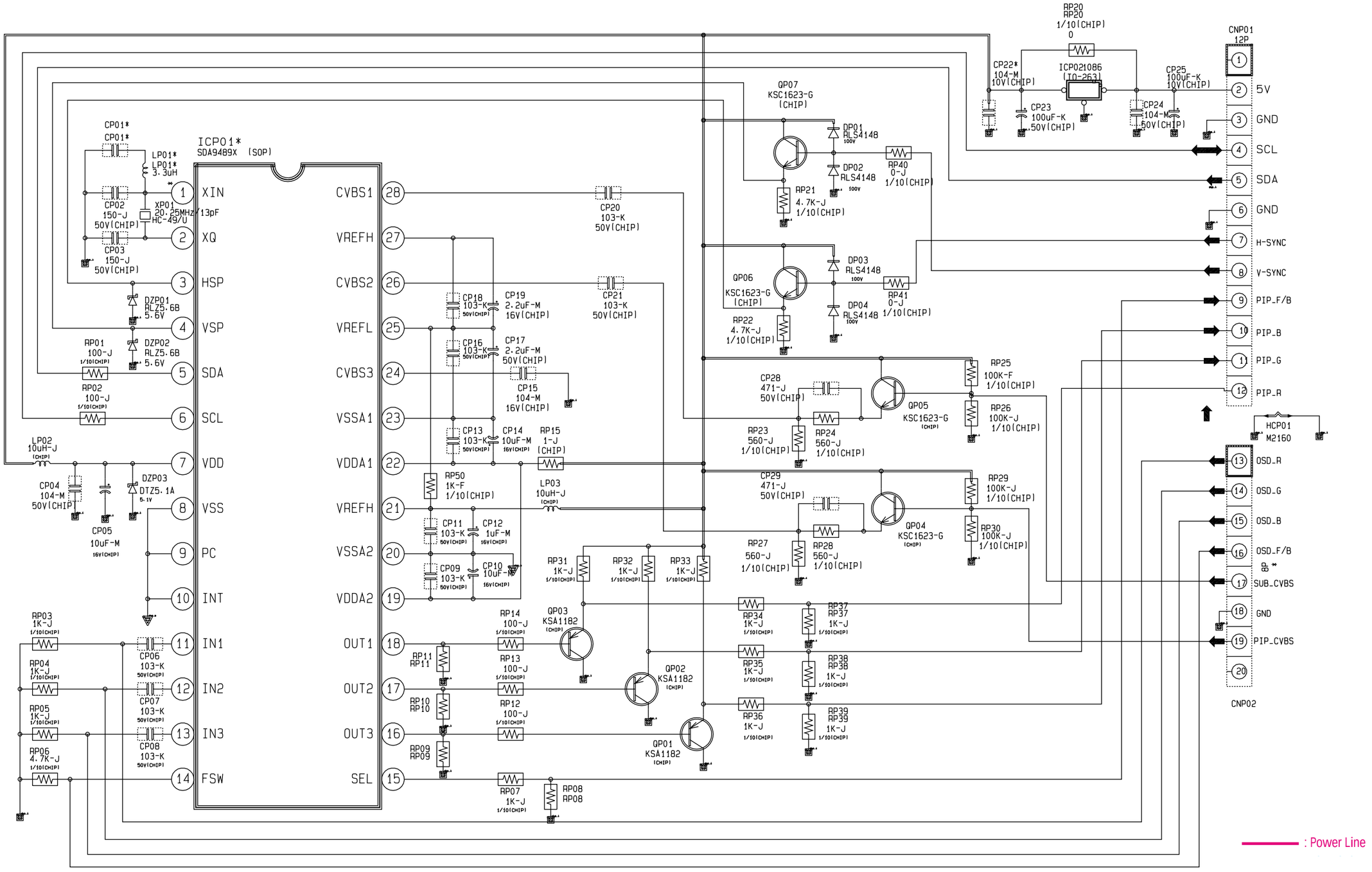
FILE NAME = MAIN

JOB-NO	TEAM	NODE	DESIGN	OPE	EDIT
Dream	KS3A	NC7	Y-K KIM		2000/06/22



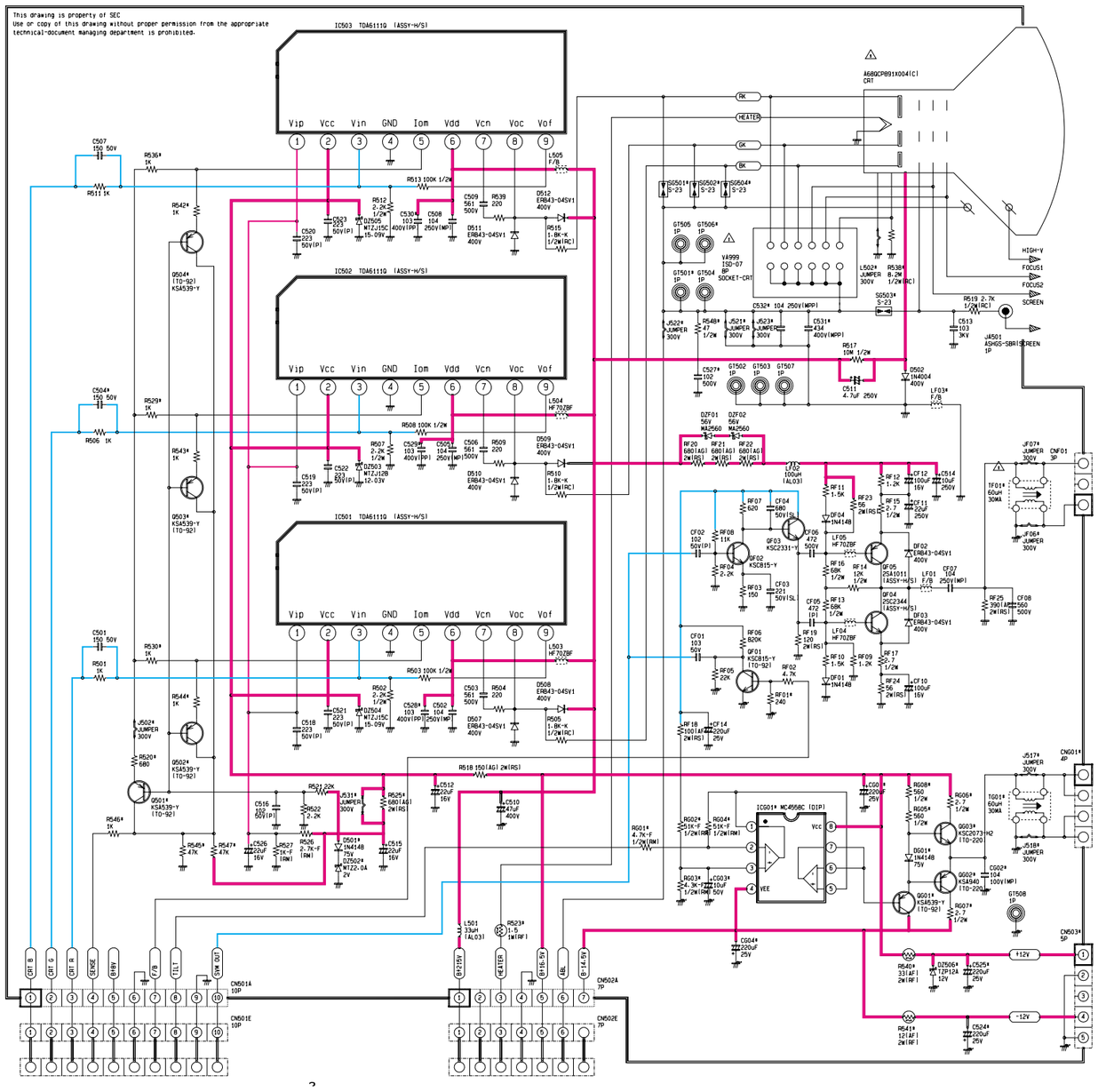
: Power Line
: Signal Line

10-5 PIP

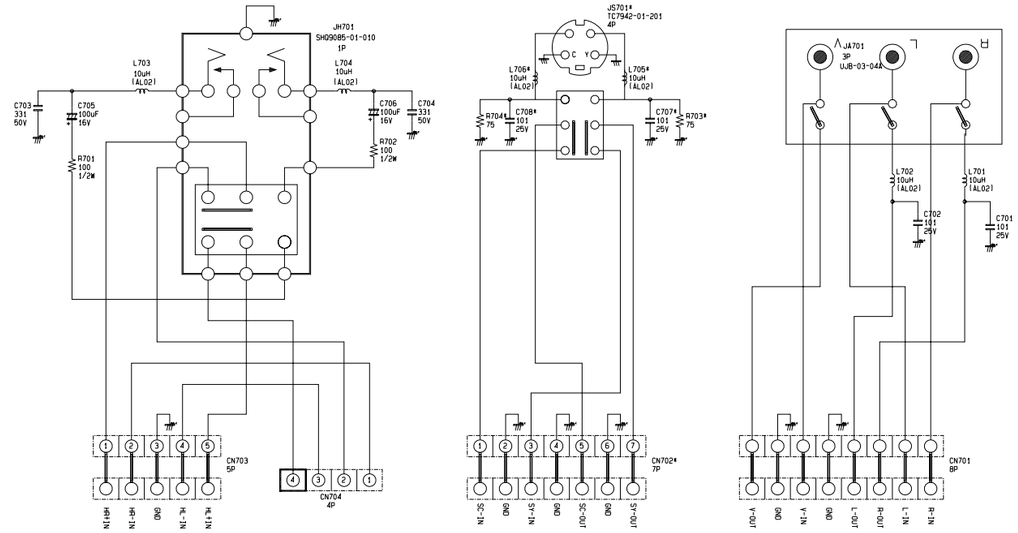

ICP01*
SDA9489X (SOP)
XIN
XQ
HSP
VSP
SDA
SCL
VDD
VSS
PC
INT
IN1
IN2
IN3
FSW
CVBS1
VREFH
CVBS2
VREFL
CVBS3
VSSA1
VDDA1
VREFH
VSSA2
VDDA2
OUT1
OUT2
OUT3
SEL
CNP01
12P
5V
GND
SCL
SDA
GND
H-SYNC
V-SYNC
PIP_F/B
PIP_B
PIP_G
PIP_R
OSD_R
OSD_G
OSD_B
OSD_F/B
SUB_CVBS
GND
PIP_CVBS
CNP02
QP07 KSC1623-G (CHIP)
QP06 KSC1623-G (CHIP)
QP05 KSC1623-G (CHIP)
QP04 KSC1623-G (CHIP)
QP03 KSA1182 (CHIP)
QP02 KSA1182 (CHIP)
QP01 KSA1182 (CHIP)
ICP021086 (TO-263)
HCP01 M2160
: Power Line

10-6 CRT, SIDE AV, VIDEO SWITCH

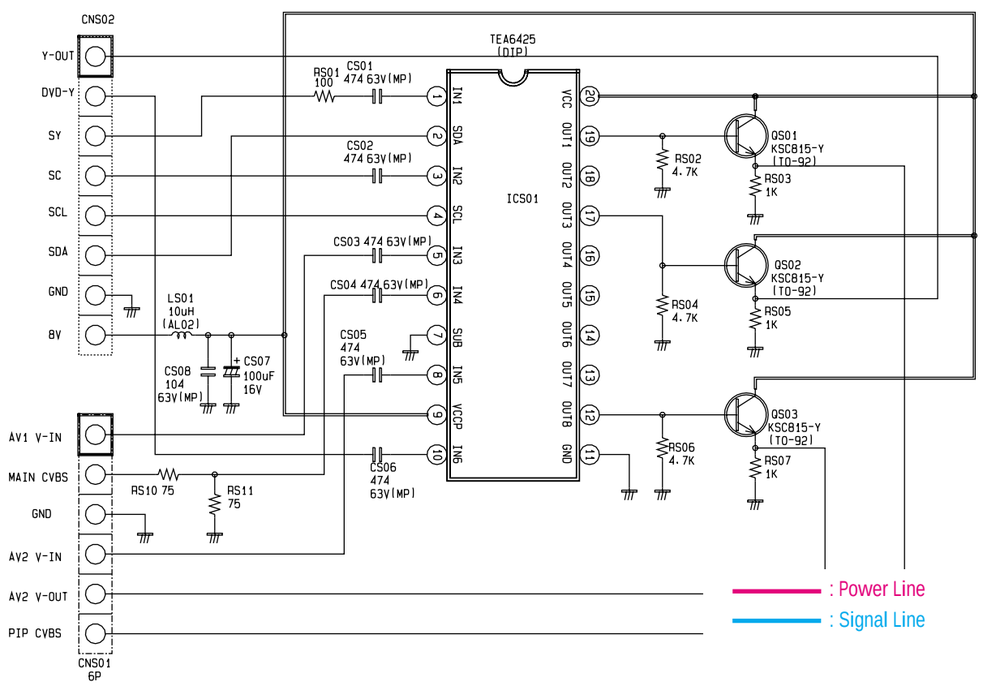
CRT



SIDE AV

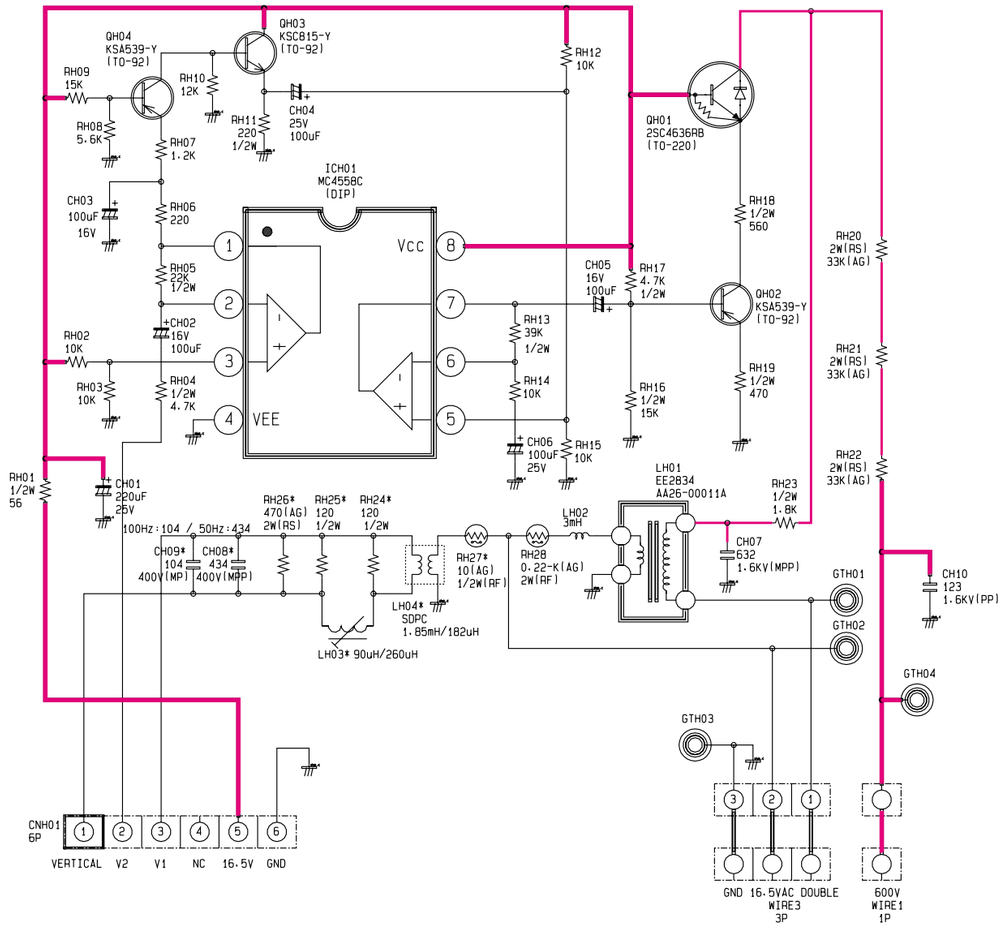


VIDEO SWITCH

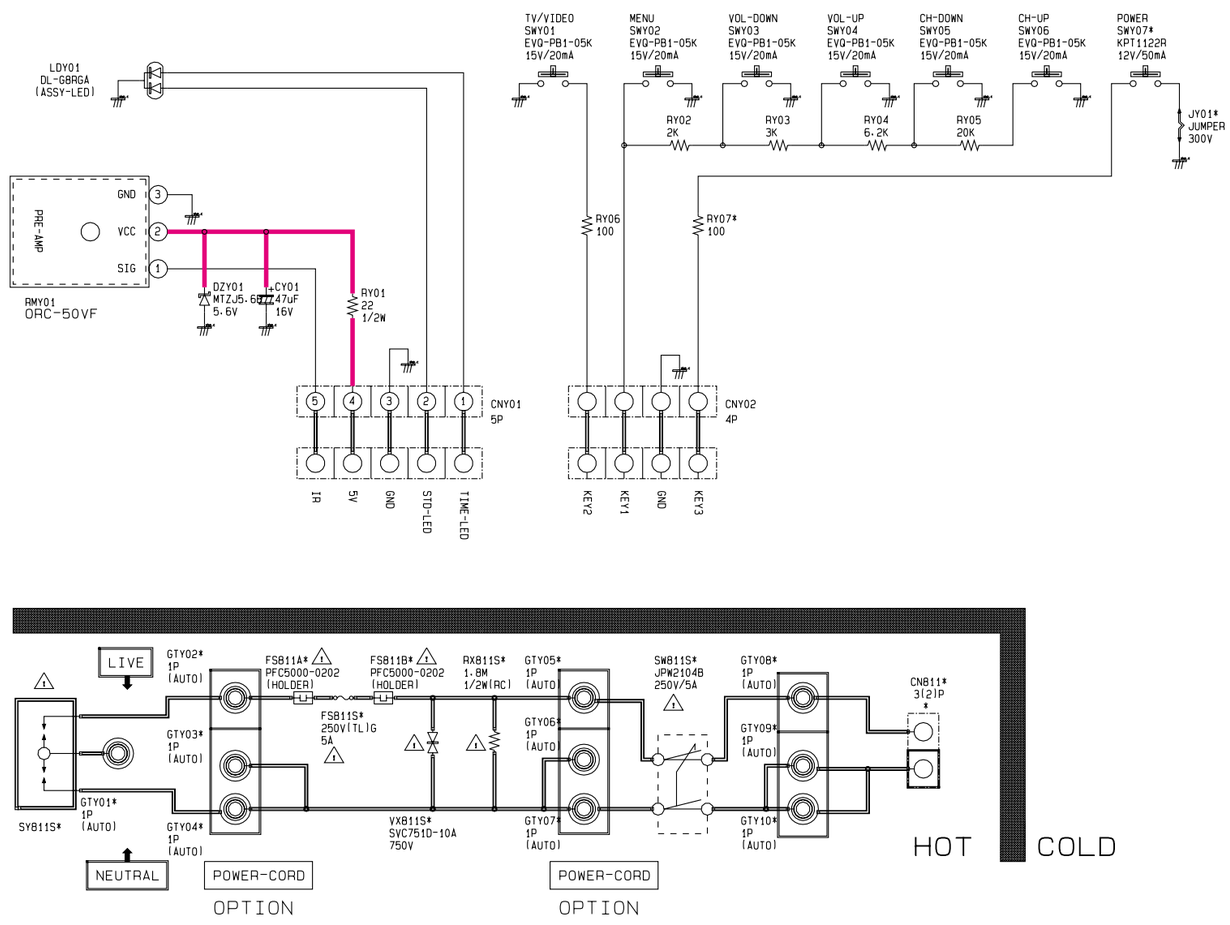


10-7 DOUBLE FOCUS, CONTROL

DOUBLE FOCUS



CONTROL



: Power Line