DP Intel® Xeon™ Processor/Low Voltage Intel® Xeon™ Processor/ Intel® E7500 Chipset Evaluation Kit Board Schematics

Rev A2

THESE SCHEMATICS ARE SUBJECT TO CHANGE.

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intel	EID Chandler, Arizona	DRAWN BY: TCL LAST REVISED: 8/08/02	PROJECT: MC 1 OF 83

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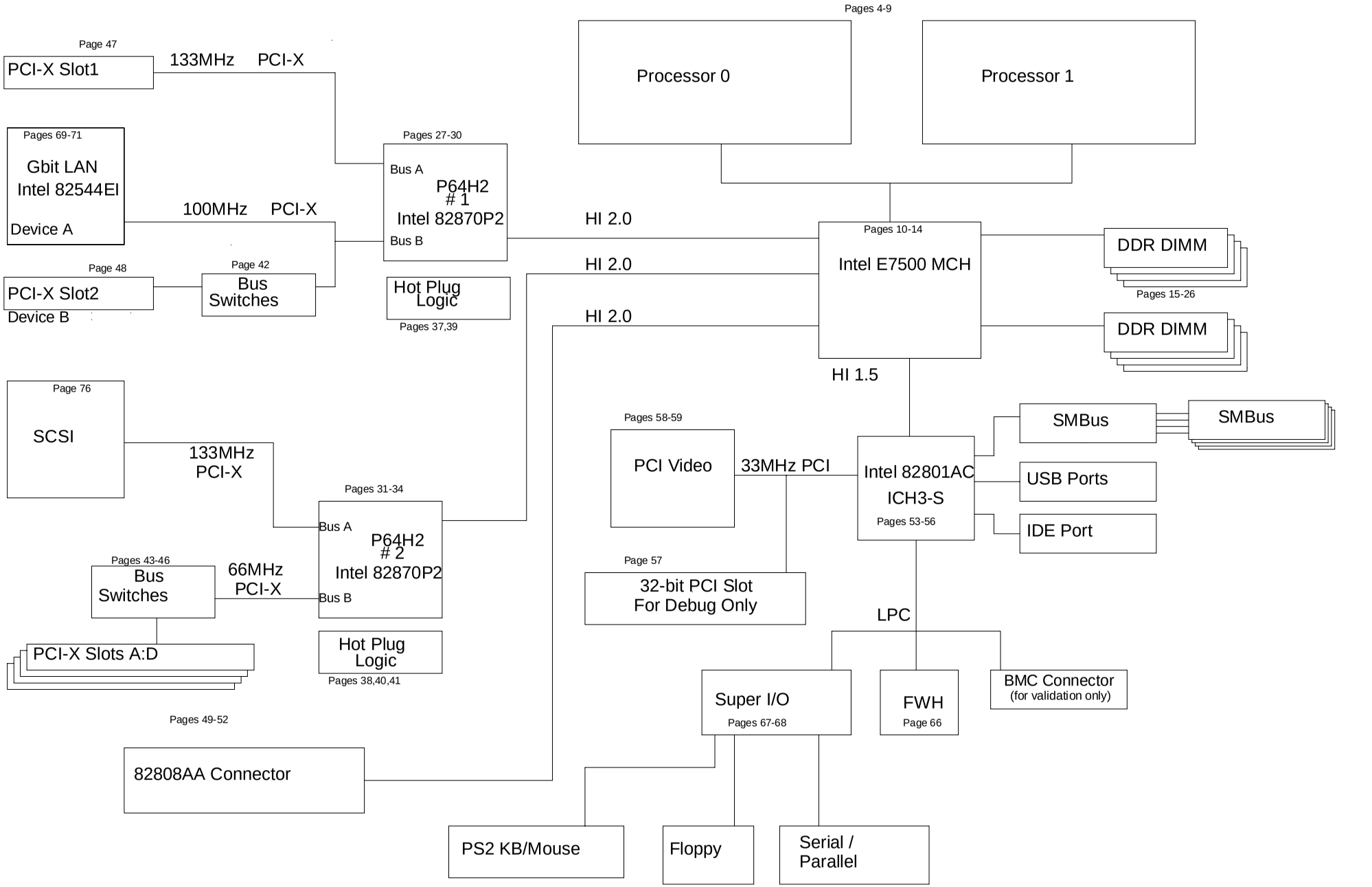

Simplified System Block Diagram

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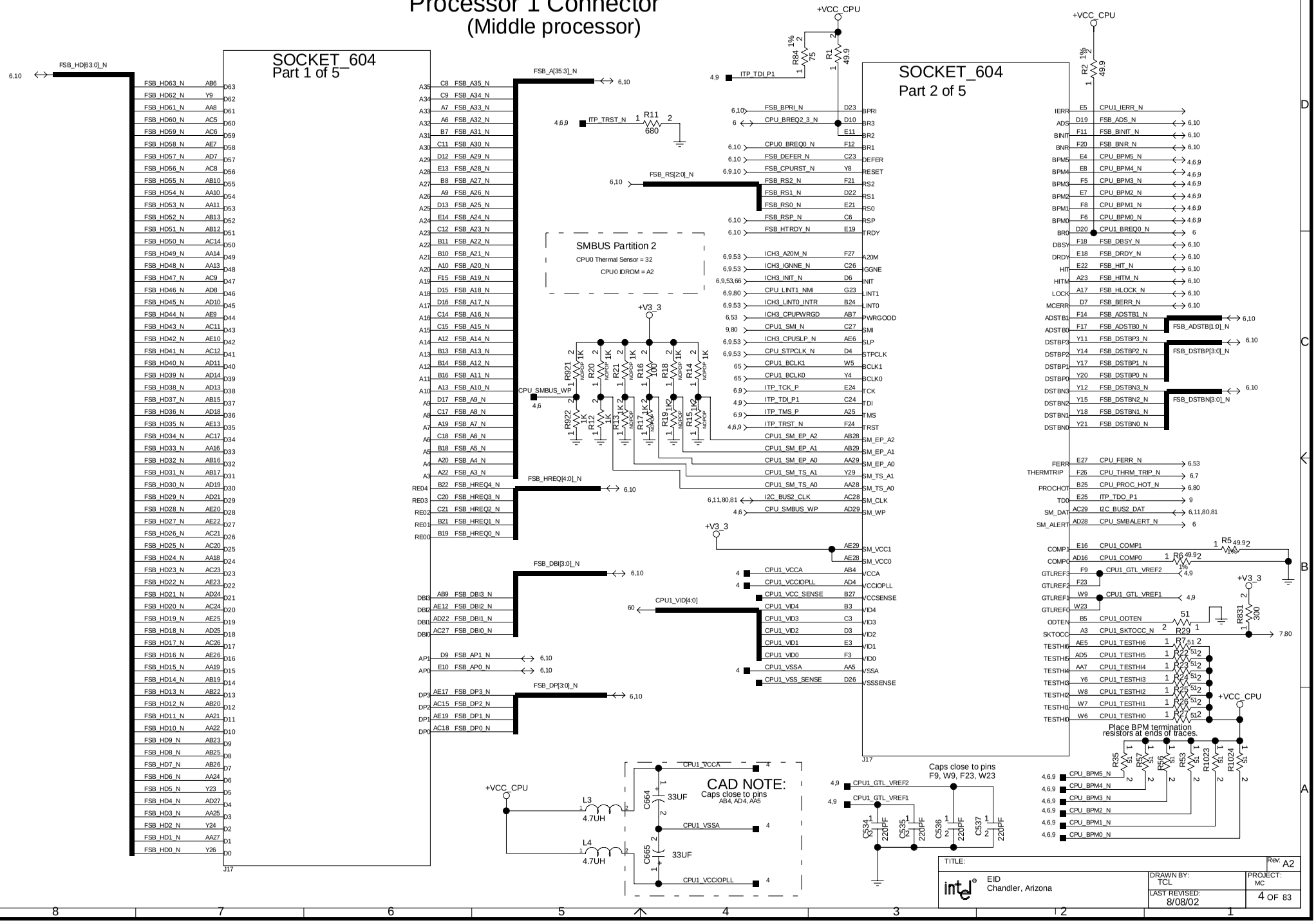
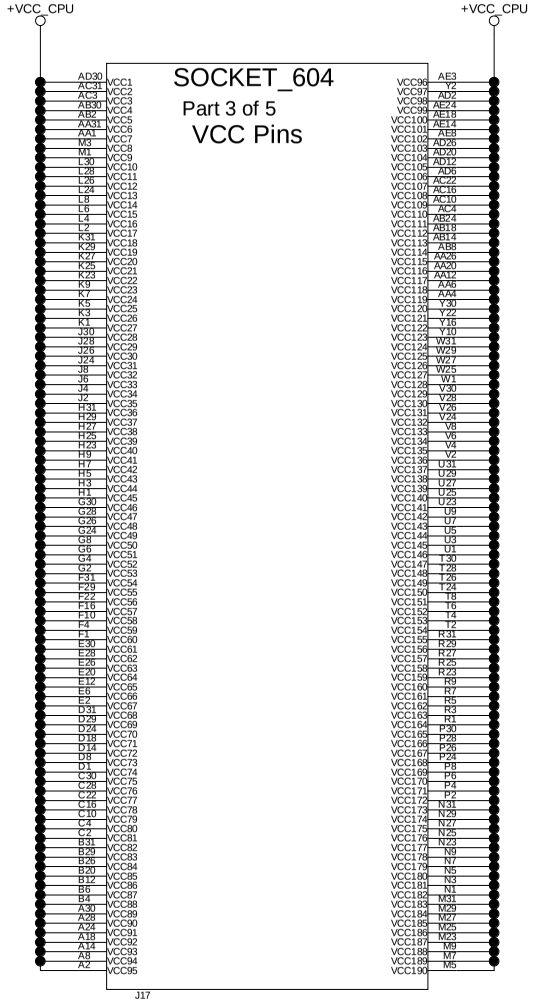
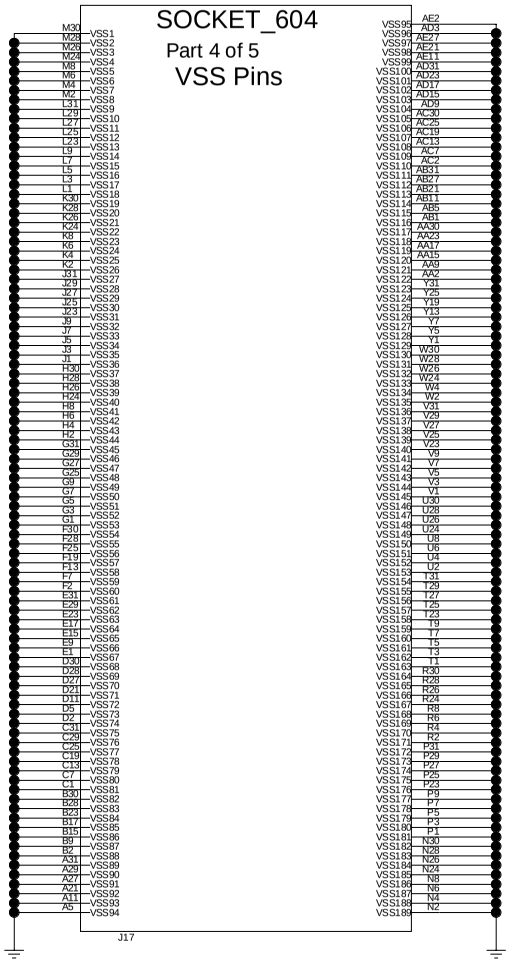
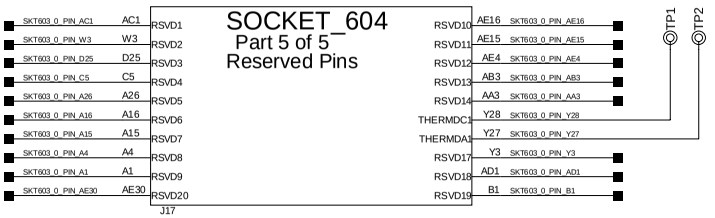
Processor 1 Connector
(Middle processor)



Processor 1 Connector







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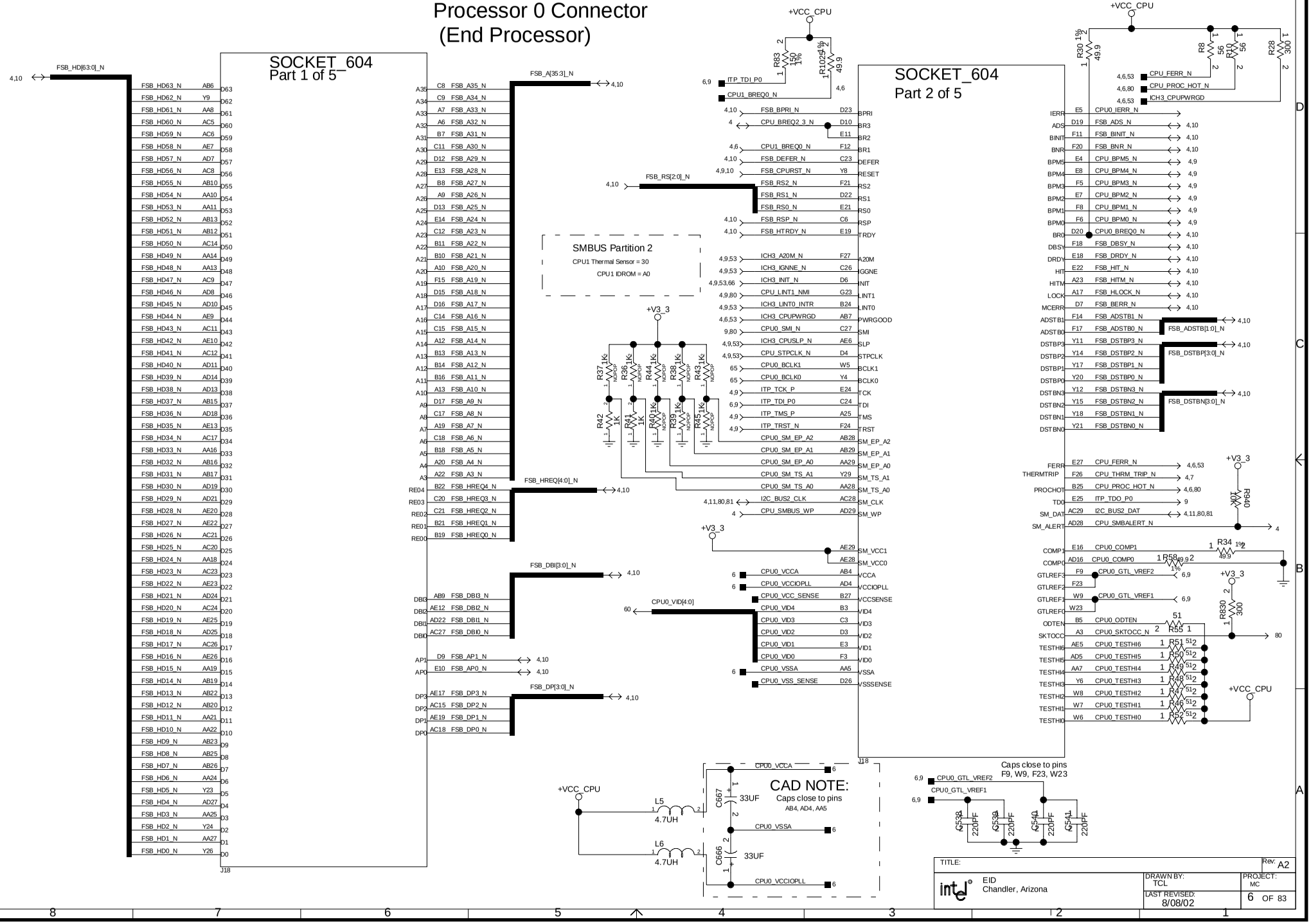
Processor 0 Connector (End Processor)



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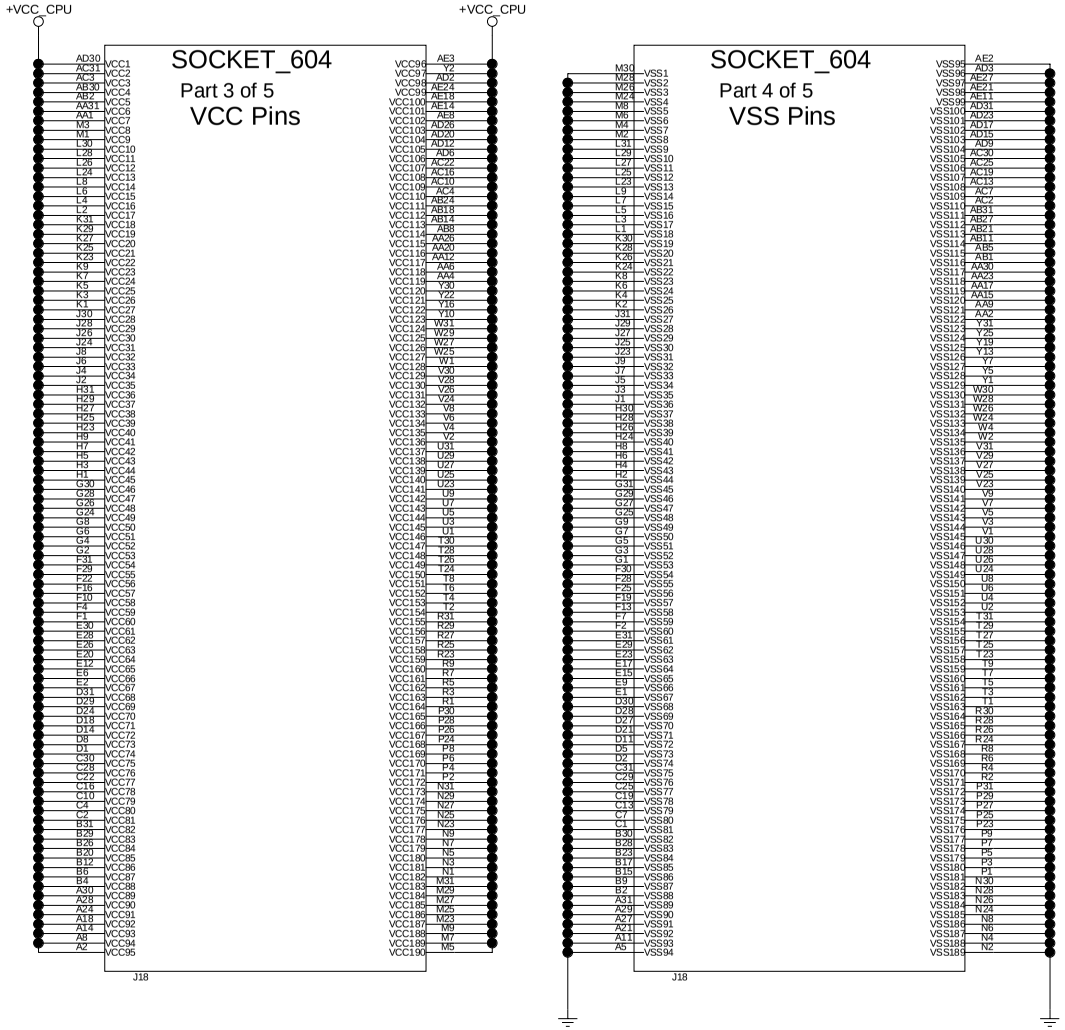
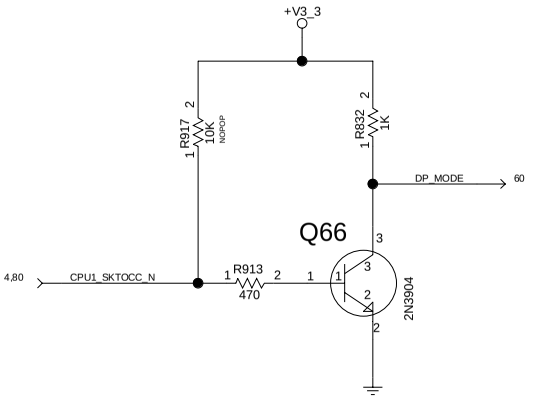
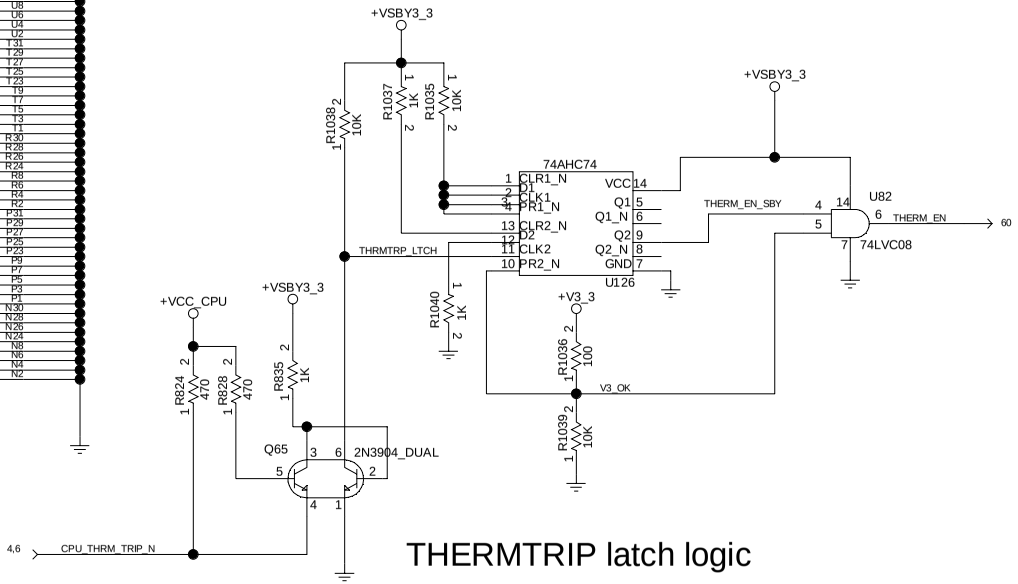
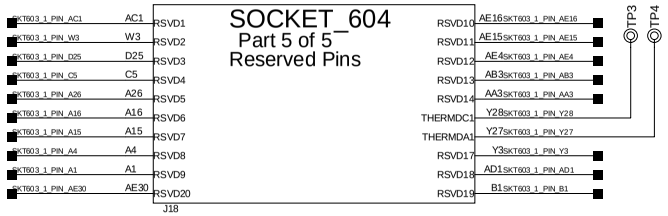
Processor 0 Connector







THERMTRIP latch logic



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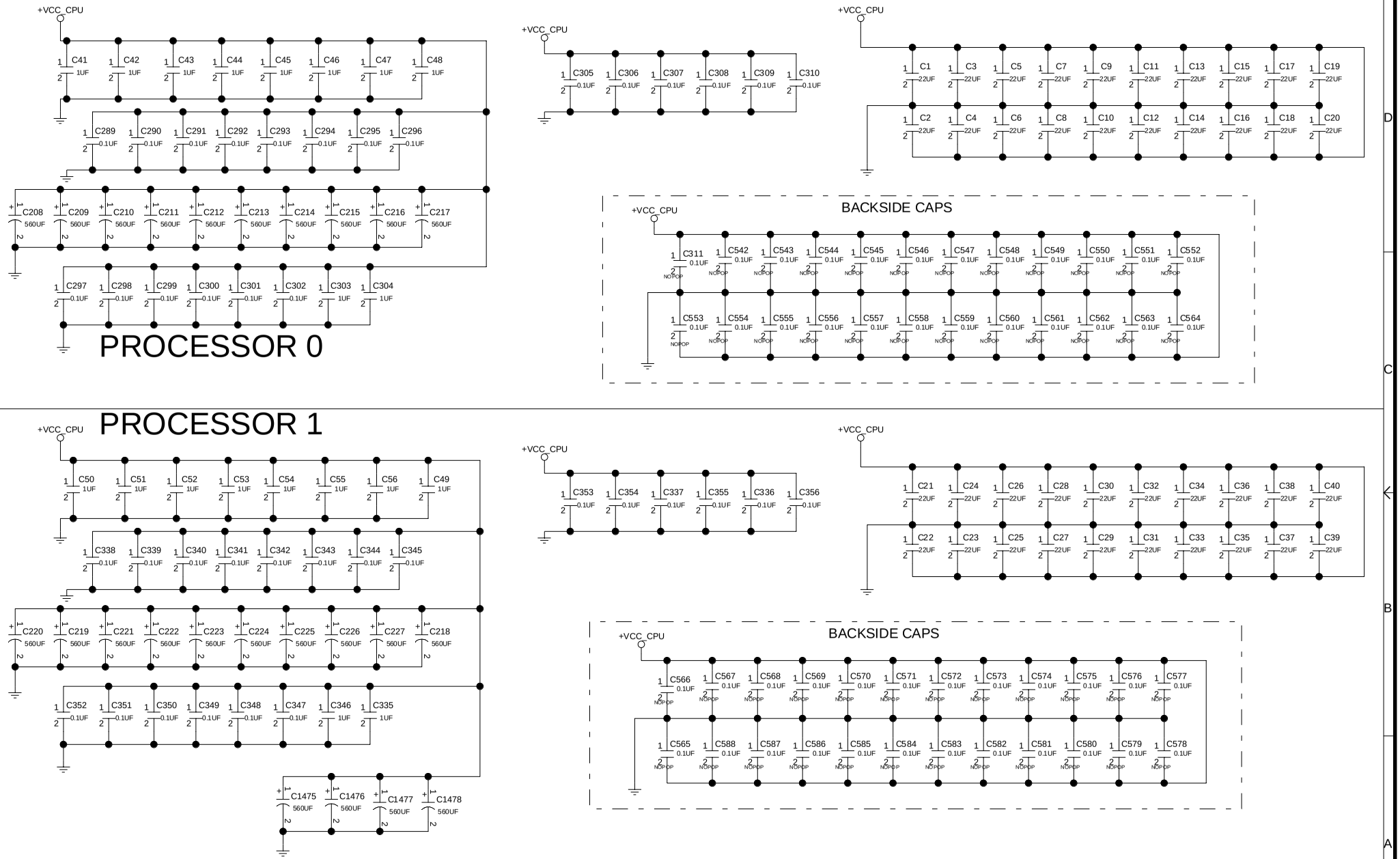

PROCESSOR 0/1 DECOUPLING

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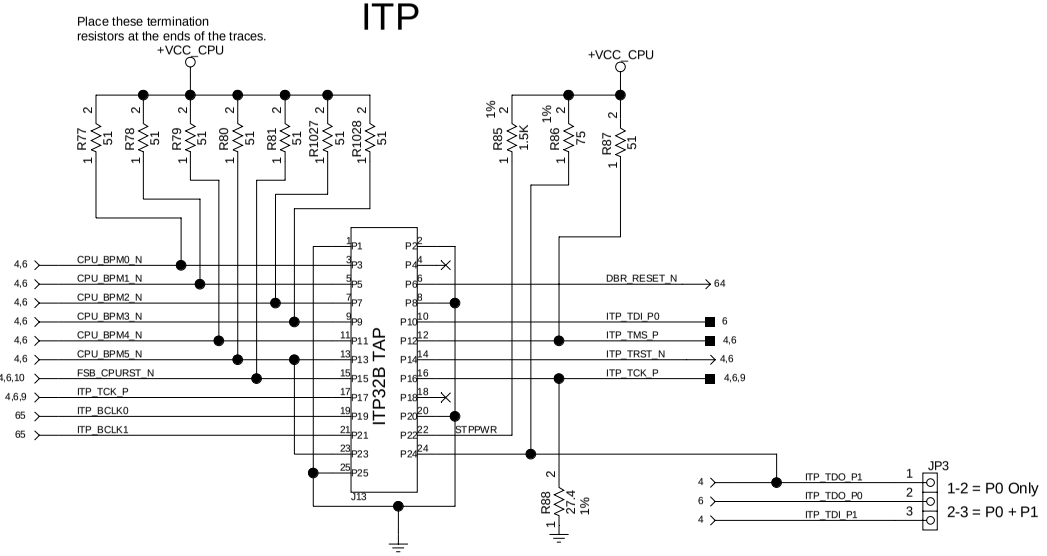
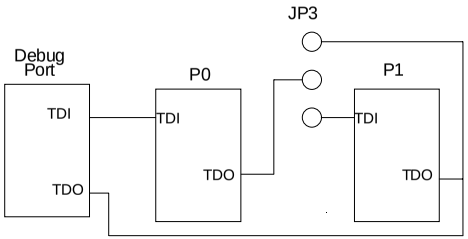
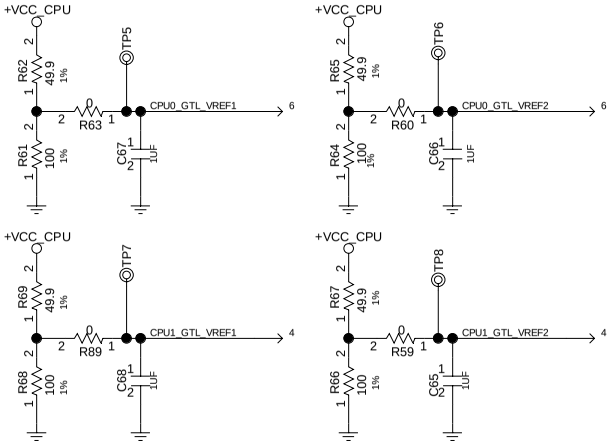
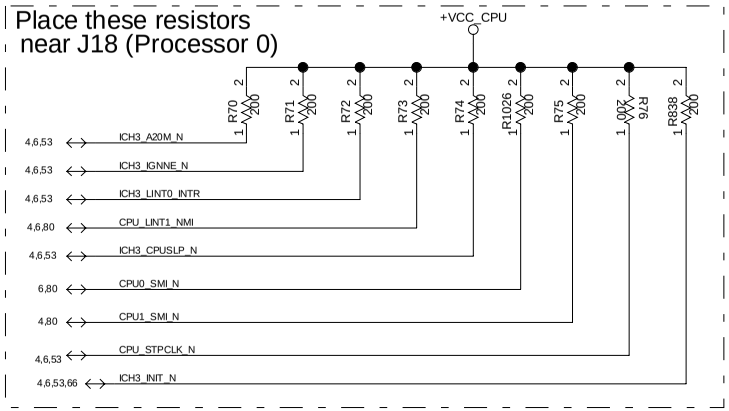
ITP





VREF circuits for GTL+





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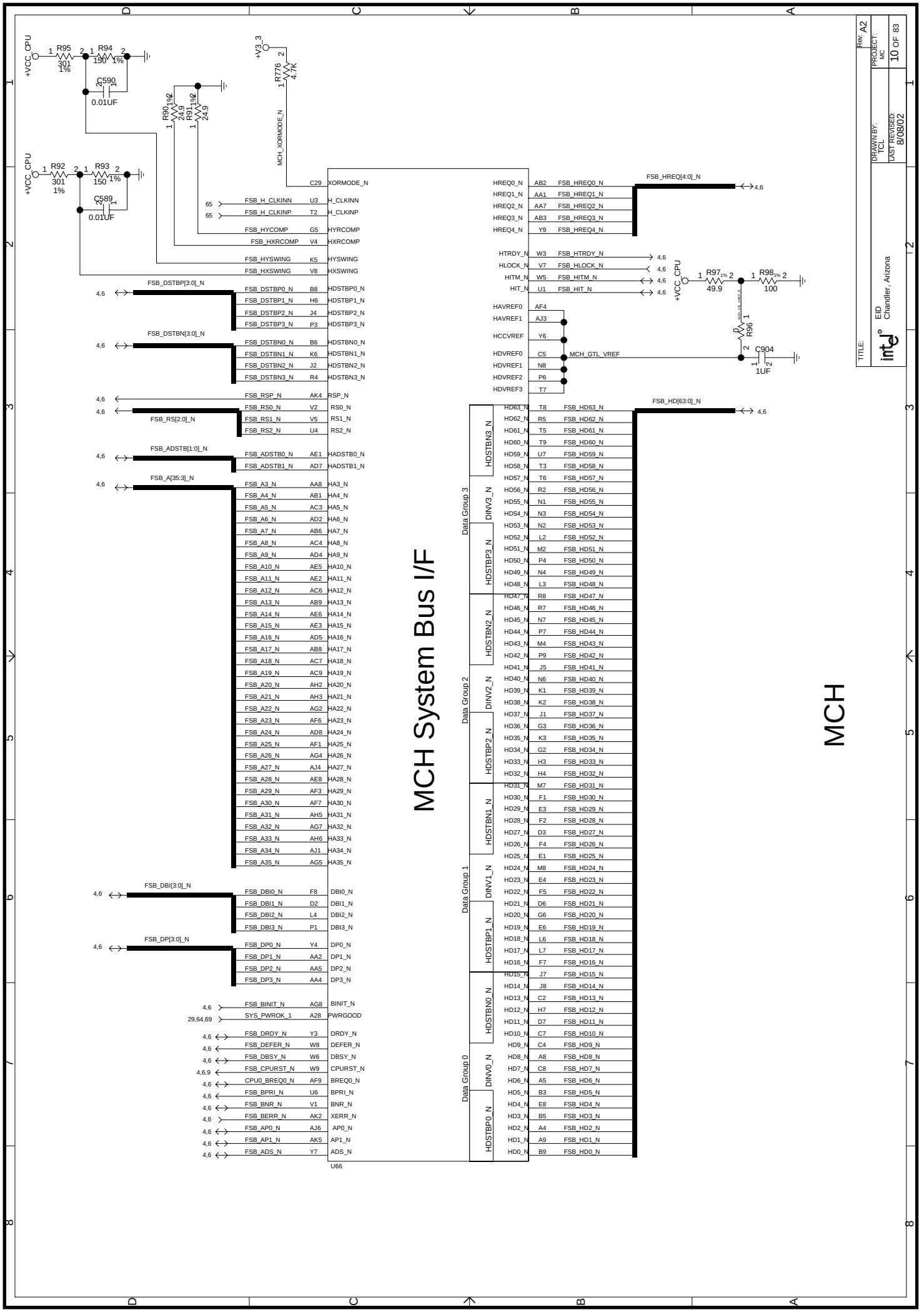
MCH System Bus I/F
MCH
U66
+VCC_CPU
R95 301 1%
R94 150 1%
C590 0.01UF
R92 301 1%
R93 150 1%
C589 0.01UF
+V3_3
R776 4.7K
R90 24.9 1%
R91 24.9 1%
MCH_XORMODE_N
C29 XORMODE_N
FSB_H_CLKINN U3 H_CLKINN
FSB_H_CLKINP T2 H_CLKINP
FSB_HYCOMP G5 HYRCOMP
FSB_HXRCOMP V4 HXRCOMP
FSB_HYSWING K5 HYSWING
FSB_HXSWING V8 HXSWING
FSB_DSTBP[3:0]_N
FSB_DSTBP0_N B8 HDSTBP0_N
FSB_DSTBP1_N H6 HDSTBP1_N
FSB_DSTBP2_N J4 HDSTBP2_N
FSB_DSTBP3_N P3 HDSTBP3_N
FSB_DSTBN[3:0]_N
FSB_DSTBN0_N B6 HDSTBN0_N
FSB_DSTBN1_N K6 HDSTBN1_N
FSB_DSTBN2_N J2 HDSTBN2_N
FSB_DSTBN3_N R4 HDSTBN3_N
FSB_RSP_N AK4 RSP_N
FSB_RS0_N V2 RS0_N
FSB_RS1_N V5 RS1_N
FSB_RS2_N U4 RS2_N
FSB_RS[2:0]_N
FSB_ADSTB[1:0]_N
FSB_ADSTB0_N AE1 HADSTB0_N
FSB_ADSTB1_N AD7 HADSTB1_N
FSB_A[35:3]_N
FSB_A3_N AA8 HA3_N
FSB_A4_N AB1 HA4_N
FSB_A5_N AC3 HA5_N
FSB_A6_N AD2 HA6_N
FSB_A7_N AB6 HA7_N
FSB_A8_N AC4 HA8_N
FSB_A9_N AD4 HA9_N
FSB_A10_N AE5 HA10_N
FSB_A11_N AE2 HA11_N
FSB_A12_N AC6 HA12_N
FSB_A13_N AB9 HA13_N
FSB_A14_N AE6 HA14_N
FSB_A15_N AE3 HA15_N
FSB_A16_N AD5 HA16_N
FSB_A17_N AB8 HA17_N
FSB_A18_N AC7 HA18_N
FSB_A19_N AC9 HA19_N
FSB_A20_N AH2 HA20_N
FSB_A21_N AH3 HA21_N
FSB_A22_N AG2 HA22_N
FSB_A23_N AF6 HA23_N
FSB_A24_N AD8 HA24_N
FSB_A25_N AF1 HA25_N
FSB_A26_N AG4 HA26_N
FSB_A27_N AJ4 HA27_N
FSB_A28_N AE8 HA28_N
FSB_A29_N AF3 HA29_N
FSB_A30_N AF7 HA30_N
FSB_A31_N AH5 HA31_N
FSB_A32_N AG7 HA32_N
FSB_A33_N AH6 HA33_N
FSB_A34_N AJ1 HA34_N
FSB_A35_N AG5 HA35_N
FSB_DBI[3:0]_N
FSB_DBI0_N F8 DBI0_N
FSB_DBI1_N D2 DBI1_N
FSB_DBI2_N L4 DBI2_N
FSB_DBI3_N P1 DBI3_N
FSB_DP[3:0]_N
FSB_DP0_N Y4 DP0_N
FSB_DP1_N AA2 DP1_N
FSB_DP2_N AA5 DP2_N
FSB_DP3_N AA4 DP3_N
FSB_BINIT_N AG8 BINIT_N
SYS_PWROK_1 A28 PWRGOOD
FSB_DRDY_N Y3 DRDY_N
FSB_DEFER_N W8 DEFER_N
FSB_DBSY_N W6 DBSY_N
FSB_CPURST_N W9 CPURST_N
CPU0_BREQ0_N AF9 BREQ0_N
FSB_BPRI_N U6 BPRI_N
FSB_BNR_N V1 BNR_N
FSB_BERR_N AK2 XERR_N
FSB_AP0_N AJ6 AP0_N
FSB_AP1_N AK5 AP1_N
FSB_ADS_N Y7 ADS_N
HREQ0_N AB2 FSB_HREQ0_N
HREQ1_N AA1 FSB_HREQ1_N
HREQ2_N AA7 FSB_HREQ2_N
HREQ3_N AB3 FSB_HREQ3_N
HREQ4_N Y9 FSB_HREQ4_N
FSB_HREQ[4:0]_N
HTRDY_N W3 FSB_HTRDY_N
HLOCK_N V7 FSB_HLOCK_N
HITM_N W5 FSB_HITM_N
HIT_N U1 FSB_HIT_N
HAVREF0 AF4
HAVREF1 AJ3
HCCVREF Y6
HDVREF0 C5
HDVREF1 N8
HDVREF2 P6
HDVREF3 T7
MCH_GTL_VREF
R97 49.9
R98 100
R96 0
C904 1UF
FSB_HD[63:0]_N
Data Group 3
Data Group 2
Data Group 1
Data Group 0
HDSTBN3_N
DINV3_N
HDSTBP3_N
HDSTBN2_N
DINV2_N
HDSTBP2_N
HDSTBN1_N
DINV1_N
HDSTBP1_N
HDSTBN0_N
DINV0_N
HDSTBP0_N
HD63_N T8 FSB_HD63_N
HD62_N R5 FSB_HD62_N
HD61_N T5 FSB_HD61_N
HD60_N T9 FSB_HD60_N
HD59_N U7 FSB_HD59_N
HD58_N T3 FSB_HD58_N
HD57_N T6 FSB_HD57_N
HD56_N R2 FSB_HD56_N
HD55_N N1 FSB_HD55_N
HD54_N N3 FSB_HD54_N
HD53_N N2 FSB_HD53_N
HD52_N L2 FSB_HD52_N
HD51_N M2 FSB_HD51_N
HD50_N P4 FSB_HD50_N
HD49_N N4 FSB_HD49_N
HD48_N L3 FSB_HD48_N
HD47_N R8 FSB_HD47_N
HD46_N R7 FSB_HD46_N
HD45_N N7 FSB_HD45_N
HD44_N P7 FSB_HD44_N
HD43_N M4 FSB_HD43_N
HD42_N P9 FSB_HD42_N
HD41_N J5 FSB_HD41_N
HD40_N N6 FSB_HD40_N
HD39_N K1 FSB_HD39_N
HD38_N K2 FSB_HD38_N
HD37_N J1 FSB_HD37_N
HD36_N G3 FSB_HD36_N
HD35_N K3 FSB_HD35_N
HD34_N G2 FSB_HD34_N
HD33_N H3 FSB_HD33_N
HD32_N H4 FSB_HD32_N
HD31_N M7 FSB_HD31_N
HD30_N F1 FSB_HD30_N
HD29_N E3 FSB_HD29_N
HD28_N F2 FSB_HD28_N
HD27_N D3 FSB_HD27_N
HD26_N F4 FSB_HD26_N
HD25_N E1 FSB_HD25_N
HD24_N M8 FSB_HD24_N
HD23_N E4 FSB_HD23_N
HD22_N F5 FSB_HD22_N
HD21_N D6 FSB_HD21_N
HD20_N G6 FSB_HD20_N
HD19_N E6 FSB_HD19_N
HD18_N L6 FSB_HD18_N
HD17_N L7 FSB_HD17_N
HD16_N F7 FSB_HD16_N
HD15_N J7 FSB_HD15_N
HD14_N J8 FSB_HD14_N
HD13_N C2 FSB_HD13_N
HD12_N H7 FSB_HD12_N
HD11_N D7 FSB_HD11_N
HD10_N C7 FSB_HD10_N
HD9_N C4 FSB_HD9_N
HD8_N A8 FSB_HD8_N
HD7_N C8 FSB_HD7_N
HD6_N A5 FSB_HD6_N
HD5_N B3 FSB_HD5_N
HD4_N E8 FSB_HD4_N
HD3_N B5 FSB_HD3_N
HD2_N A4 FSB_HD2_N
HD1_N A9 FSB_HD1_N
HD0_N B9 FSB_HD0_N
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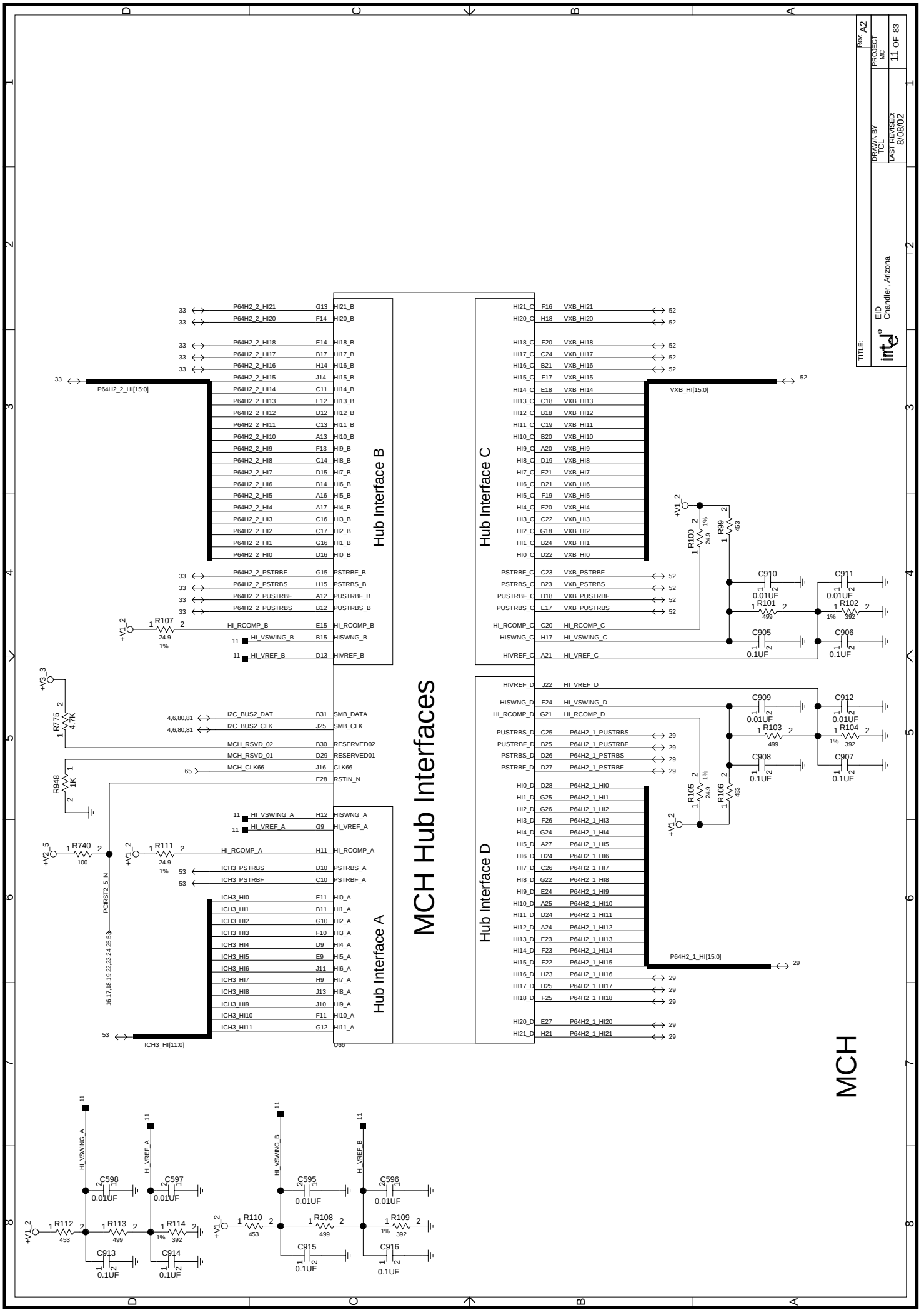
EID
Chandler, Arizona


MCH Hub Interfaces
Hub Interface A
Hub Interface B
Hub Interface C
Hub Interface D
MCH
P64H2_2_HI[15:0]
ICH3_HI[11:0]
VXB_HI[15:0]
P64H2_1_HI[15:0]
HI_VSWING_A
HI_VREF_A
HI_VSWING_B
HI_VREF_B
TITLE:
Intel
EID
Chandler, Arizona
DRAWN BY:
TCL
LAST REVISED:
8/08/02
PROJECT:
MC
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MCH DDR A
MCH DDR Channel A
DDRA_DQ0 AF22 DQ0_A
DDRA_DQ1 AN28 DQ1_A
DDRA_DQ2 AE21 DQ2_A
DDRA_DQ3 AH22 DQ3_A
DDRA_DQS0 AM27 DQS0_A
DDRA_DQS9 AF21 DQS9_A
DDRA_DQ4 AN29 DQ4_A
DDRA_DQ5 AM28 DQ5_A
DDRA_DQ6 AL26 DQ6_A
DDRA_DQ7 AL25 DQ7_A
DDRA_DQ8 AN25 DQ8_A
DDRA_DQ9 AM24 DQ9_A
DDRA_DQ10 AG21 DQ10_A
DDRA_DQ11 AE20 DQ11_A
DDRA_DQS1 AL23 DQS1_A
DDRA_DQS10 AK23 DQS10_A
DDRA_DQ12 AM25 DQ12_A
DDRA_DQ13 AK24 DQ13_A
DDRA_DQ14 AL22 DQ14_A
DDRA_DQ15 AJ22 DQ15_A
DDRA_DQ16 AK19 DQ16_A
DDRA_DQ17 AL19 DQ17_A
DDRA_DQ18 AN17 DQ18_A
DDRA_DQ19 AF18 DQ19_A
DDRA_DQS2 AG18 DQS2_A
DDRA_DQS11 AK18 DQS11A
DDRA_DQ20 AN20 DQ20_A
DDRA_DQ21 AM19 DQ21_A
DDRA_DQ22 AL17 DQ22_A
DDRA_DQ23 AJ18 DQ23_A
DDRA_DQ24 AF19 DQ24_A
DDRA_DQ25 AH19 DQ25_A
DDRA_DQ26 AM21 DQ26_A
DDRA_DQ27 AL20 DQ27_A
DDRA_DQS3 AE18 DQS3_A
DDRA_DQS12 AK20 DQS12_A
DDRA_DQ28 AH20 DQ28_A
DDRA_DQ29 AJ21 DQ29_A
DDRA_DQ30 AN21 DQ30_A
DDRA_DQ31 AJ19 DQ31_A
DDRA_DQ32 AL14 DQ32_A
DDRA_DQ33 AM13 DQ33A
DDRA_DQ34 AJ15 DQ34_A
DDRA_DQ35 AF15 DQ35_A
DDRA_DQS4 AL13 DQS4_A
DDRA_DQS13 AJ13 DQS13_A
DDRA_DQ36 AK14 DQ36_A
DDRA_DQ37 AN13 DQ37_A
DDRA_DQ38 AH14 DQ38_A
DDRA_DQ39 AG14 DQ39_A
DDRA_DQ40 AE14 DQ40_A
DDRA_DQ41 AH13 DQ41_A
DDRA_DQ42 AN12 DQ42_A
DDRA_DQ43 AL11 DQ43_A
DDRA_DQS5 AM12 DQS5_A
DDRA_DQS14 AK12 DQS14_A
DDRA_DQ44 AE15 DQ44_A
DDRA_DQ45 AF13 DQ45_A
DDRA_DQ46 AJ12 DQ46_A
DDRA_DQ47 AM10 DQ47_A
DDRA_DQ48 AE12 DQ48_A
DDRA_DQ49 AH11 DQ49_A
DDRA_DQ50 AG11 DQ50_A
DDRA_DQ51 AN5 DQ51_A
DDRA_DQS6 AL8 DQS6_A
DDRA_DQS15 AM7 DQS15_A
DDRA_DQ52 AG12 DQ52_A
DDRA_DQ53 AF12 DQ53_A
DDRA_DQ54 AM9 DQ54_A
DDRA_DQ55 AM6 DQ55_A
DDRA_DQ56 AG10 DQ56_A
DDRA_DQ57 AJ9 DQ57_A
DDRA_DQ58 AM3 DQ58_A
DDRA_DQ59 AM2 DQ59_A
DDRA_DQS7 AL6 DQS7_A
DDRA_DQS16 AH9 DQS16_A
DDRA_DQ60 AH10 DQ60_A
DDRA_DQ61 AE11 DQ61_A
DDRA_DQ62 AL5 DQ62_A
DDRA_DQ63 AM4 DQ63_A
DDRA_CB0 AE16 CB0_A
DDRA_CB1 AH16 CB1_A
DDRA_CB2 AL16 CB2_A
DDRA_CB3 AK15 CB3_A
DDRA_DQS8 AJ16 DQS8_A
DDRA_DQS17 AF16 DQS17_A
DDRA_CB4 AE17 CB4_A
DDRA_CB5 AG17 CB5_A
DDRA_CB6 AM15 CB6_A
DDRA_CB7 AG15 CB7_A
Low Nibble Data Group 0
High Nibble Data Group 0
Low Nibble Data Group 1
High Nibble Data Group 1
Low Nibble Data Group 2
High Nibble Data Group 2
Low Nibble Data Group 3
High Nibble Data Group 3
Low Nibble Data Group 4
High Nibble Data Group 4
Low Nibble Data Group 5
High Nibble Data Group 5
Low Nibble Data Group 6
High Nibble Data Group 6
Low Nibble Data Group 7
High Nibble Data Group 7
Low Nibble Check Bits
High Nibble Check Bits
U66
Address Bus
WE_N_A AE23 DDRA_WE_N_R 16,17,18,19,20
CAS_N_A AE22 DDRA_CAS_N_R 16,17,18,19,20
RAS_N_A AN24 DDRA_RAS_N_R 16,17,18,19,20
MA0_A AF24 DDRA_MA0_R 16,17,18,19,20
MA1_A AK26 DDRA_MA1_R 16,17,18,19,20
MA2_A AH26 DDRA_MA2_R 16,17,18,19,20
MA3_A AJ27 DDRA_MA3_R 16,17,18,19,20
MA4_A AG27 DDRA_MA4_R 16,17,18,19,20
MA5_A AH28 DDRA_MA5_R 16,17,18,19,20
MA6_A AL28 DDRA_MA6_R 16,17,18,19,20
MA7_A AL29 DDRA_MA7_R 16,17,18,19,20
MA8_A AK29 DDRA_MA8_R 16,17,18,19,20
MA9_A AM30 DDRA_MA9_R 16,17,18,19,20
MA10_A AJ24 DDRA_MA10_R 16,17,18,19,20
MA11_A AK30 DDRA_MA11_R 16,17,18,19,20
MA12_A AM31 DDRA_MA12_R 16,17,18,19,20
BA1_A AH23 DDRA_BA1_R 16,17,18,19,26
BA0_A AL31 DDRA_BA0_R 16,17,18,19,20
Chip Select
CS7_N_A AL2 DDRA_CS7_N_R 19,20
CS6_N_A AL3 DDRA_CS6_N_R 19,20
CS5_N_A AK7 DDRA_CS5_N_R 18,26
CS4_N_A AN8 DDRA_CS4_N_R 18,26
CS3_N_A AH8 DDRA_CS3_N_R 17,20
CS2_N_A AL10 DDRA_CS2_N_R 17,20
CS1_N_A AK11 DDRA_CS1_N_R 16,20
CS0_N_A AE13 DDRA_CS0_N_R 16,20
VTT_DDR
R841 47
RCVEN_IN_A AM22 DDRA_RCV_EN_IN 20
RCVEN_OUT_A AG20 DDRA_RCV_EN_OUT 20
DDRCOMP_A AH17 DDRA_DRCOMP
DDRCVOH_A AK17 DDRCVOH_A
DDRCVOL_A AN16 DDRCVOL_A
R115 6.81
C1669 0.1UF
C1668 0.1UF
C1667 0.1UF
C1666 0.1UF
R524 6.98K 1%
C779 0.01UF
C780 0.1UF
+V2_5
C778 0.01UF
C777 0.1UF
R523 6.98K 1%
R522 13K
R521 13K
CKE_A AE19 R117 0 DDRA_CKE0 16,17,18,19,20
RESERVED AM18 R118 0 DDRA_CKE1 16,17,18,19,20
Command Clock
CMDCLK3_A AE25 DDRA_CMDCLK3 19
CMDCLK3_N_A AE24 DDRA_CMDCLK3_N 19
CMDCLK2_A AG26 DDRA_CMDCLK2 18
CMDCLK2_N_A AF25 DDRA_CMDCLK2_N 18
CMDCLK1_A AJ25 DDRA_CMDCLK1 17
CMDCLK1_N_A AH25 DDRA_CMDCLK1_N 17
CMDCLK0_A AG24 DDRA_CMDCLK0 16
CMDCLK0_N_A AG23 DDRA_CMDCLK0_N 16
Voltage Ref
DDRVREF5_A AJ28
DDRVREF4_A AK27
DDRVREF3_A AK21
DDRVREF2_A AM16
DDRVREF1_A AL9
DDRVREF0_A AJ7
R923 0
R924 0
R925 0
DDRA_VREF_FLT_1
DDRA_VREF_FLT_2
DDRA_VREF_FLT_3
C1143 0.1UF
C1144 0.1UF
C1145 0.1UF
VREF_DDR_MCH
13,62
TITLE:
intel
EID
Chandler, Arizona
DRAWN BY: TCL
LAST REVISED: 8/08/02
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MCH DDR B
MCH DDR Channel B
DDRB_DQ0 F33 DQ0_B
DDRB_DQ1 K30 DQ1_B
DDRB_DQ2 J32 DQ2_B
DDRB_DQ3 N25 DQ3_B
DDRB_DQS0 L30 DQS0_B
DDRB_DQS9 H31 DQS9_B
DDRB_DQ4 N27 DQ4_B
DDRB_DQ5 G32 DQ5_B
DDRB_DQ6 M29 DQ6_B
DDRB_DQ7 N26 DQ7_B
DDRB_DQ8 J33 DQ8_B
DDRB_DQ9 K32 DQ9_B
DDRB_DQ10 P27 DQ10_B
DDRB_DQ11 P25 DQ11_B
DDRB_DQS1 M31 DQS1_B
DDRB_DQS10 N29 DQS10_B
DDRB_DQ12 J31 DQ12_B
DDRB_DQ13 L31 DQ13_B
DDRB_DQ14 P26 DQ14_B
DDRB_DQ15 P28 DQ15_B
DDRB_DQ16 T29 DQ16_B
DDRB_DQ17 T30 DQ17_B
DDRB_DQ18 U30 DQ18_B
DDRB_DQ19 T26 DQ19_B
DDRB_DQS2 U33 DQS2_B
DDRB_DQS11 U31 DQS11_B
DDRB_DQ20 R32 DQ20_B
DDRB_DQ21 T27 DQ21_B
DDRB_DQ22 V33 DQ22_B
DDRB_DQ23 V31 DQ23_B
DDRB_DQ24 P30 DQ24_B
DDRB_DQ25 P33 DQ25_B
DDRB_DQ26 R26 DQ26_B
DDRB_DQ27 T32 DQ27_B
DDRB_DQS3 R29 DQS3_B
DDRB_DQS12 R31 DQS12_B
DDRB_DQ28 N32 DQ28_B
DDRB_DQ29 P31 DQ29_B
DDRB_DQ30 R28 DQ30_B
DDRB_DQ31 T25 DQ31_B
DDRB_DQ32 W27 DQ32_B
DDRB_DQ33 AE33 DQ33_B
DDRB_DQ34 AF31 DQ34_B
DDRB_DQ35 W25 DQ35_B
DDRB_DQS4 AE32 DQS4_B
DDRB_DQS13 AC30 DQS13_B
DDRB_DQ36 AA28 DQ36_B
DDRB_DQ37 AD32 DQ37_B
DDRB_DQ38 AG33 DQ38_B
DDRB_DQ39 W26 DQ39_B
DDRB_DQ40 AA29 DQ40_B
DDRB_DQ41 AB33 DQ41_B
DDRB_DQ42 V26 DQ42_B
DDRB_DQ43 AD31 DQ43_B
DDRB_DQS5 AC31 DQS5_B
DDRB_DQS14 AB30 DQS14_B
DDRB_DQ44 Y28 DQ44_B
DDRB_DQ45 AB32 DQ45_B
DDRB_DQ46 AB29 DQ46_B
DDRB_DQ47 V25 DQ47_B
DDRB_DQ48 Y25 DQ48_B
DDRB_DQ49 AB27 DQ49_B
DDRB_DQ50 AH32 DQ50_B
DDRB_DQ51 AH31 DQ51_B
DDRB_DQS6 AE28 DQS6_B
DDRB_DQS15 AD27 DQS15_B
DDRB_DQ52 AC28 DQ52_B
DDRB_DQ53 AA26 DQ53_B
DDRB_DQ54 AG30 DQ54_B
DDRB_DQ55 AH33 DQ55_B
DDRB_DQ56 AJ30 DQ56_B
DDRB_DQ57 AG29 DQ57_B
DDRB_DQ58 AB25 DQ58_B
DDRB_DQ59 AA25 DQ59_B
DDRB_DQS7 AE27 DQS7_B
DDRB_DQS16 AF28 DQS16_B
DDRB_DQ60 AL32 DQ60_B
DDRB_DQ61 AJ31 DQ61_B
DDRB_DQ62 AC27 DQ62_B
DDRB_DQ63 AB26 DQ63_B
DDRB_CB0 V28 CB0_B
DDRB_CB1 U25 CB1_B
DDRB_CB2 Y31 CB2_B
DDRB_CB3 AA33 CB3_B
DDRB_DQS8 W29 DQS8_B
DDRB_DQS17 Y30 DQS17_B
DDRB_CB4 U28 CB4_B
DDRB_CB5 U27 CB5_B
DDRB_CB6 AA31 CB6_B
DDRB_CB7 AA32 CB7_B
Low Nibble Data Group 0
High Nibble Data Group 0
Low Nibble Data Group 1
High Nibble Data Group 1
Low Nibble Data Group 2
High Nibble Data Group 2
Low Nibble Data Group 3
High Nibble Data Group 3
Low Nibble Data Group 4
High Nibble Data Group 4
Low Nibble Data Group 5
High Nibble Data Group 5
Low Nibble Data Group 6
High Nibble Data Group 6
Low Nibble Data Group 7
High Nibble Data Group 7
Low Nibble Check Bits
High Nibble Check Bits
U66
Address Bus
WE_N_B D32 DDRB_WE_N_R 22,23,24,25,26
CAS_N_B H28 DDRB_CAS_N_R 22,23,24,25,26
RAS_N_B V32 DDRB_RAS_N_R 20,22,23,24,25
MA0_B M26 DDRB_MA0_R 22,23,24,25,26
MA1_B K29 DDRB_MA1_R 22,23,24,25,26
MA2_B H30 DDRB_MA2_R 22,23,24,25,26
MA3_B G30 DDRB_MA3_R 22,23,24,25,26
MA4_B F32 DDRB_MA4_R 22,23,24,25,26
MA5_B G29 DDRB_MA5_R 22,23,24,25,26
MA6_B F31 DDRB_MA6_R 22,23,24,25,26
MA7_B E33 DDRB_MA7_R 22,23,24,25,26
MA8_B E31 DDRB_MA8_R 22,23,24,25,26
MA9_B F29 DDRB_MA9_R 22,23,24,25,26
MA10_B L25 DDRB_MA10_R 20,22,23,24,25
MA11_B C31 DDRB_MA11_R 22,23,24,25,26
MA12_B C32 DDRB_MA12_R 22,23,24,25,26
BA1_B H27 DDRB_BA1_R 22,23,24,25,26
BA0_B K26 DDRB_BA0_R 22,23,24,25,26
Chip Select
CS7_N_B Y27 DDRB_CS7_N_R 20,25
CS6_N_B AD28 DDRB_CS6_N_R 20,25
CS5_N_B AE26 DDRB_CS5_N_R 24,26
CS4_N_B AE31 DDRB_CS4_N_R 24,26
CS3_N_B AF27 DDRB_CS3_N_R 23,26
CS2_N_B AF30 DDRB_CS2_N_R 23,26
CS1_N_B AK32 DDRB_CS1_N_R 22,26
CS0_N_B AH29 DDRB_CS0_N_R 22,26
VTT_DDR
R843 47
RCVEN_IN_B N30 DDRB_RCV_EN_IN 26
RCVEN_OUT_B R25 DDRB_RCV_EN_OUT 26
DDRCOMP_B W30 DDRB_DRCOMP
R120 6.81
DDRCVOH_B W32 DDRCVOH_B
DDRCVOL_B V29 DDRCVOL_B
R527 6.98K 1%
C782 0.01UF
C781 0.1UF
C784 0.01UF
C783 0.1UF
+V2_5
R526 6.98K 1%
R525 13K
R528 13K
RESERVED K33 R123 0 DDRB_CKE1 22,23,24,25,26
CKE_B M32 R124 0 DDRB_CKE0 22,23,24,25,26
Command Clock
CMDCLK3_B K27 DDRB_CMDCLK3 25
CMDCLK3_N_B L27 DDRB_CMDCLK3_N 25
CMDCLK2_B J26 DDRB_CMDCLK2 24
CMDCLK2_N_B K25 DDRB_CMDCLK2_N 24
CMDCLK1_B L28 DDRB_CMDCLK1 23
CMDCLK1_N_B M28 DDRB_CMDCLK1_N 23
CMDCLK0_B J29 DDRB_CMDCLK0 22
CMDCLK0_N_B J28 DDRB_CMDCLK0_N 22
Voltage Ref
DDRVREF5_B E30
DDRVREF4_B M25
DDRVREF3_B N33
DDRVREF2_B U26
DDRVREF1_B AG32
DDRVREF0_B AC25
R928 0
R927 0
R926 0
DDRB_VREF_FLT.1
DDRB_VREF_FLT.2
DDRB_VREF_FLT.3
C1146 0.1UF
C1147 0.1UF
C1148 0.1UF
VREF_DDR_MCH
12,62
TITLE:
intel
EID
Chandler, Arizona
DRAWN BY: TCL
LAST REVISED: 8/08/02
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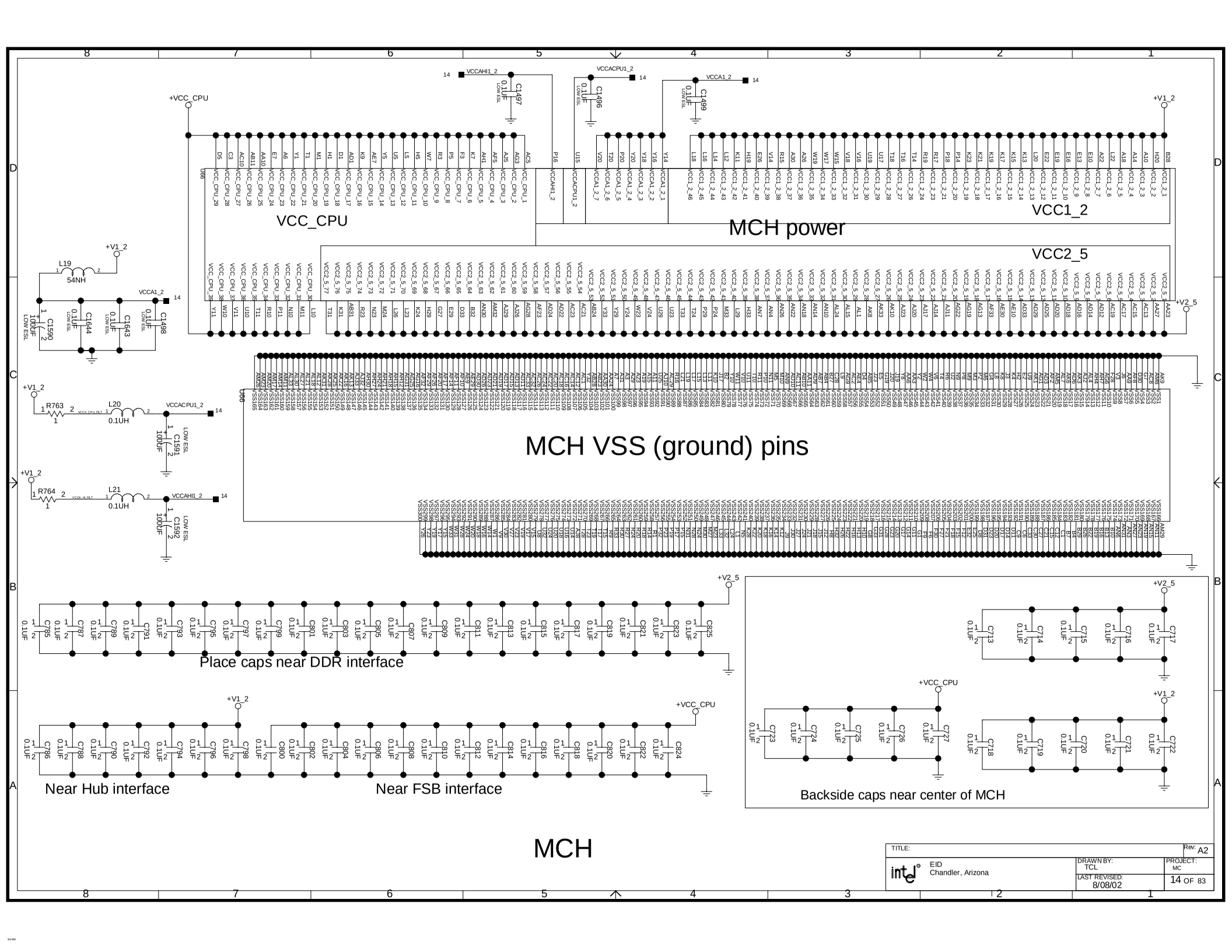
Rev: A2


VCC_CPU
VCC1_2
MCH power
VCC2_5
MCH VSS (ground) pins
Place caps near DDR interface
Near Hub interface
Near FSB interface
Backside caps near center of MCH
MCH
+VCC_CPU
+V1_2
+V2_5
VCCAHI1_2
VCCACPU1_2
VCCA1_2
TITLE:
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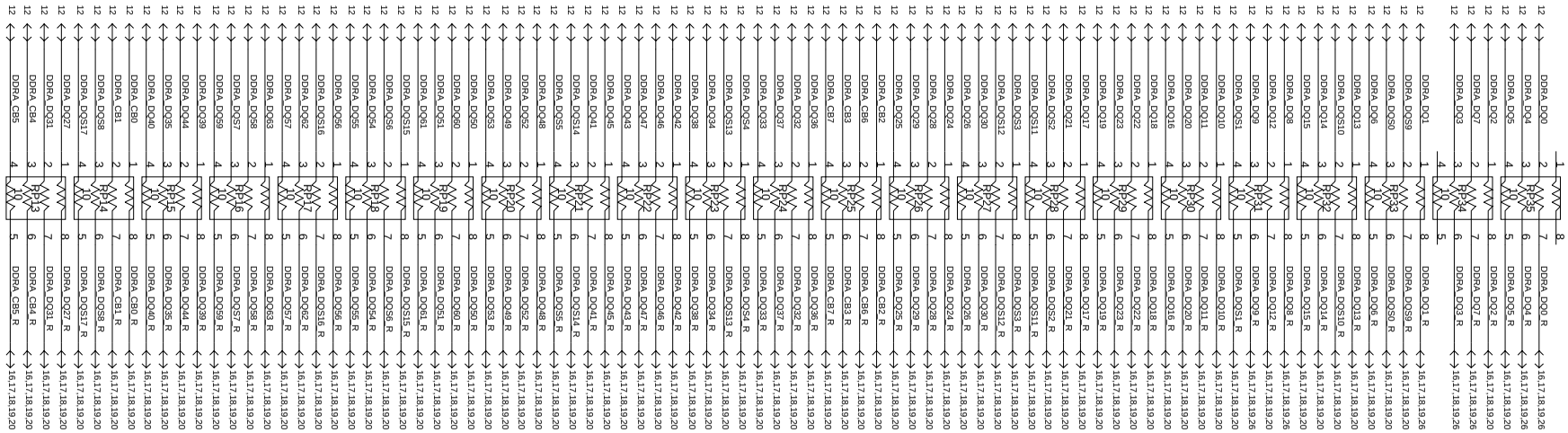
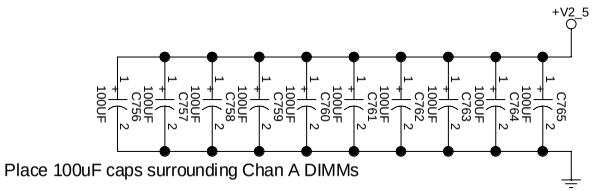
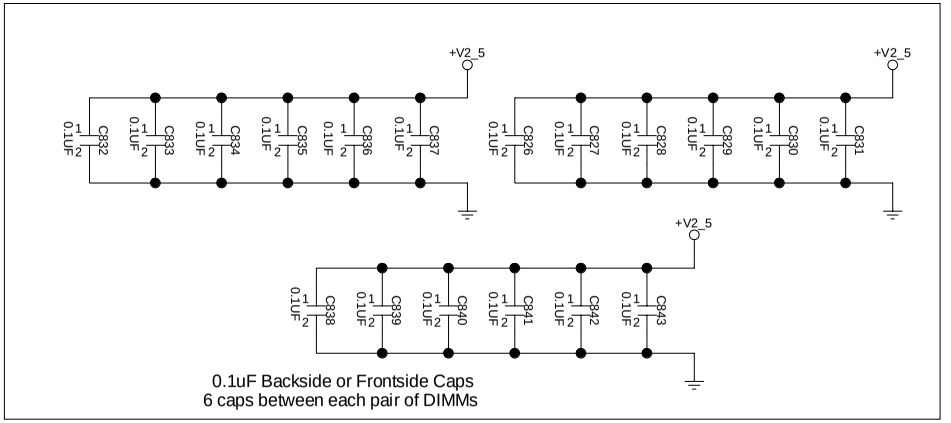
DDR Channel A Series Resistors

Place near DIMM A-1





Place 100uF caps surrounding Chan A DIMMs



0.1uF Backside or Frontside Caps
6 caps between each pair of DIMMs

CAD Note: All Caps should have direct attatchment to 2.5V plane, and 2 vias to GND.

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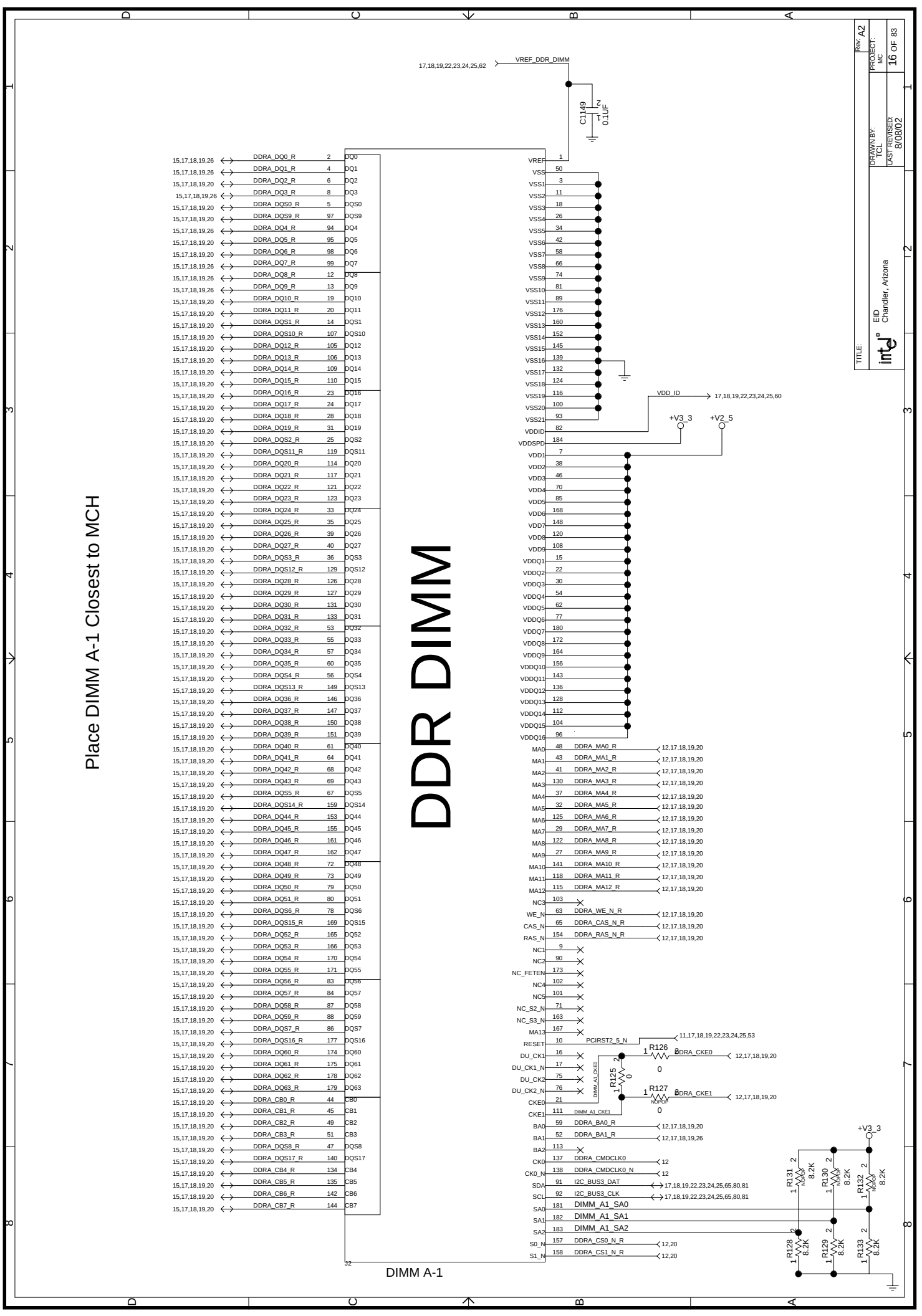
Place DIMM A-1 Closest to MCH
DDR DIMM
DIMM A-1
VREF_DDR_DIMM
17,18,19,22,23,24,25,62
C1149
0.1UF
VDD_ID
17,18,19,22,23,24,25,60
+V3_3
+V2_5
DDRA_CKE0
DDRA_CKE1
PCIRST2_5_N
11,17,18,19,22,23,24,25,53
DIMM_A1_CKE0
DIMM_A1_CKE1
DIMM_A1_SA0
DIMM_A1_SA1
DIMM_A1_SA2
Rev: A2
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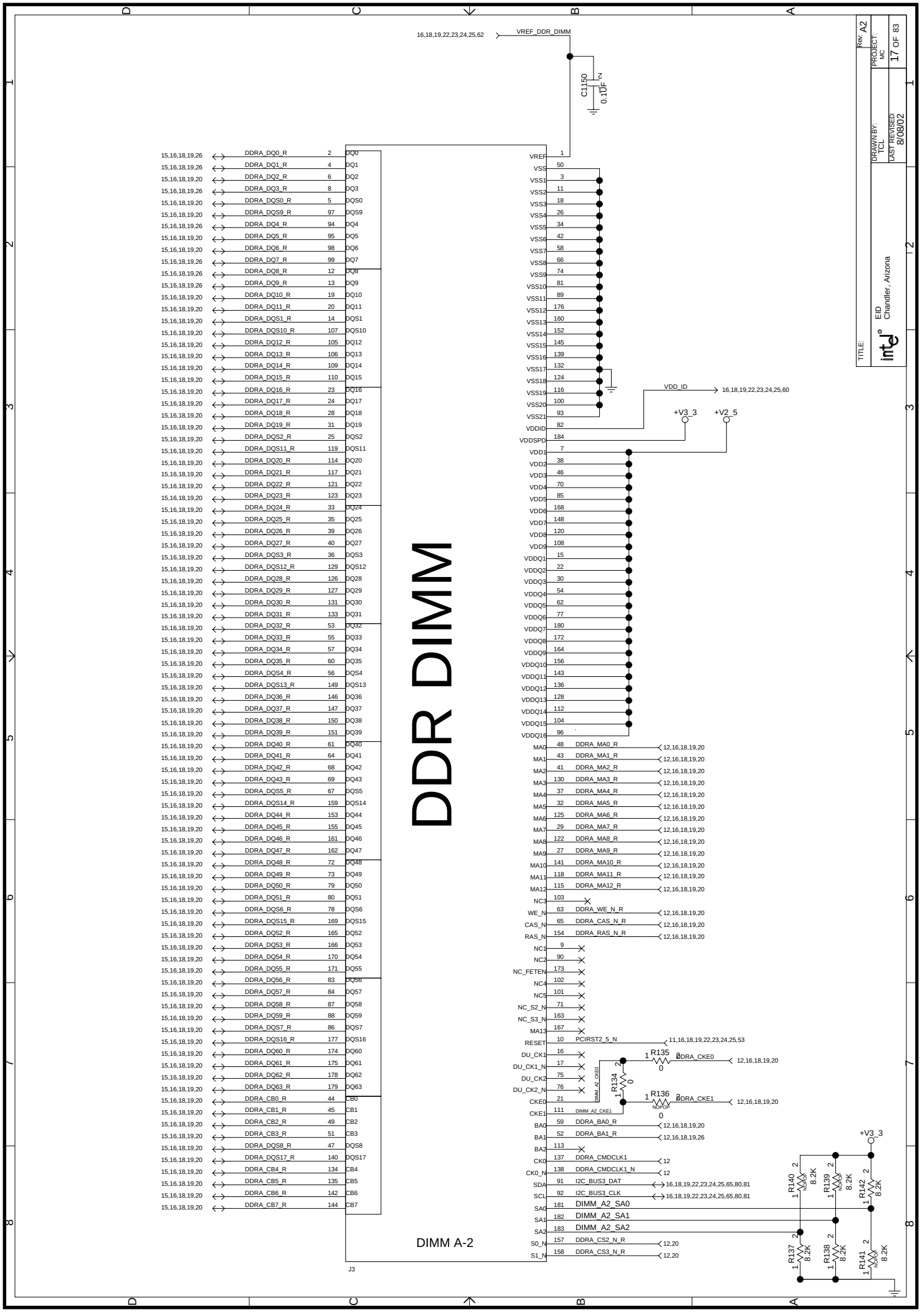
DDR DIMM
DIMM A-2
VREF_DDR_DIMM
16,18,19,22,23,24,25,62
C1150
0.1UF
VDD_ID
16,18,19,22,23,24,25,60
+V3_3
+V2_5
DDRA_DQ0_R
DDRA_DQ1_R
DDRA_DQ2_R
DDRA_DQ3_R
DDRA_DQS0_R
DDRA_DQS9_R
DDRA_DQ4_R
DDRA_DQ5_R
DDRA_DQ6_R
DDRA_DQ7_R
DDRA_DQ8_R
DDRA_DQ9_R
DDRA_DQ10_R
DDRA_DQ11_R
DDRA_DQS1_R
DDRA_DQS10_R
DDRA_DQ12_R
DDRA_DQ13_R
DDRA_DQ14_R
DDRA_DQ15_R
DDRA_DQ16_R
DDRA_DQ17_R
DDRA_DQ18_R
DDRA_DQ19_R
DDRA_DQS2_R
DDRA_DQS11_R
DDRA_DQ20_R
DDRA_DQ21_R
DDRA_DQ22_R
DDRA_DQ23_R
DDRA_DQ24_R
DDRA_DQ25_R
DDRA_DQ26_R
DDRA_DQ27_R
DDRA_DQS3_R
DDRA_DQS12_R
DDRA_DQ28_R
DDRA_DQ29_R
DDRA_DQ30_R
DDRA_DQ31_R
DDRA_DQ32_R
DDRA_DQ33_R
DDRA_DQ34_R
DDRA_DQ35_R
DDRA_DQS4_R
DDRA_DQS13_R
DDRA_DQ36_R
DDRA_DQ37_R
DDRA_DQ38_R
DDRA_DQ39_R
DDRA_DQ40_R
DDRA_DQ41_R
DDRA_DQ42_R
DDRA_DQ43_R
DDRA_DQS5_R
DDRA_DQS14_R
DDRA_DQ44_R
DDRA_DQ45_R
DDRA_DQ46_R
DDRA_DQ47_R
DDRA_DQ48_R
DDRA_DQ49_R
DDRA_DQ50_R
DDRA_DQ51_R
DDRA_DQS6_R
DDRA_DQS15_R
DDRA_DQ52_R
DDRA_DQ53_R
DDRA_DQ54_R
DDRA_DQ55_R
DDRA_DQ56_R
DDRA_DQ57_R
DDRA_DQ58_R
DDRA_DQ59_R
DDRA_DQS7_R
DDRA_DQS16_R
DDRA_DQ60_R
DDRA_DQ61_R
DDRA_DQ62_R
DDRA_DQ63_R
DDRA_CB0_R
DDRA_CB1_R
DDRA_CB2_R
DDRA_CB3_R
DDRA_DQS8_R
DDRA_DQS17_R
DDRA_CB4_R
DDRA_CB5_R
DDRA_CB6_R
DDRA_CB7_R
DDRA_MA0_R
DDRA_MA1_R
DDRA_MA2_R
DDRA_MA3_R
DDRA_MA4_R
DDRA_MA5_R
DDRA_MA6_R
DDRA_MA7_R
DDRA_MA8_R
DDRA_MA9_R
DDRA_MA10_R
DDRA_MA11_R
DDRA_MA12_R
DDRA_WE_N_R
DDRA_CAS_N_R
DDRA_RAS_N_R
PCIRST2_5_N
11,16,18,19,22,23,24,25,53
DDRA_CKE0
DDRA_CKE1
DIMM_A2_CKE0
DIMM_A2_CKE1
DDRA_BA0_R
DDRA_BA1_R
DDRA_CMDCLK1
DDRA_CMDCLK1_N
I2C_BUS3_DAT
I2C_BUS3_CLK
DIMM_A2_SA0
DIMM_A2_SA1
DIMM_A2_SA2
DDRA_CS2_N_R
DDRA_CS3_N_R
R135
R136
R134
R140
R139
R142
R137
R138
R141
8.2K
NOPOP
J3
TITLE:
EID
Chandler, Arizona
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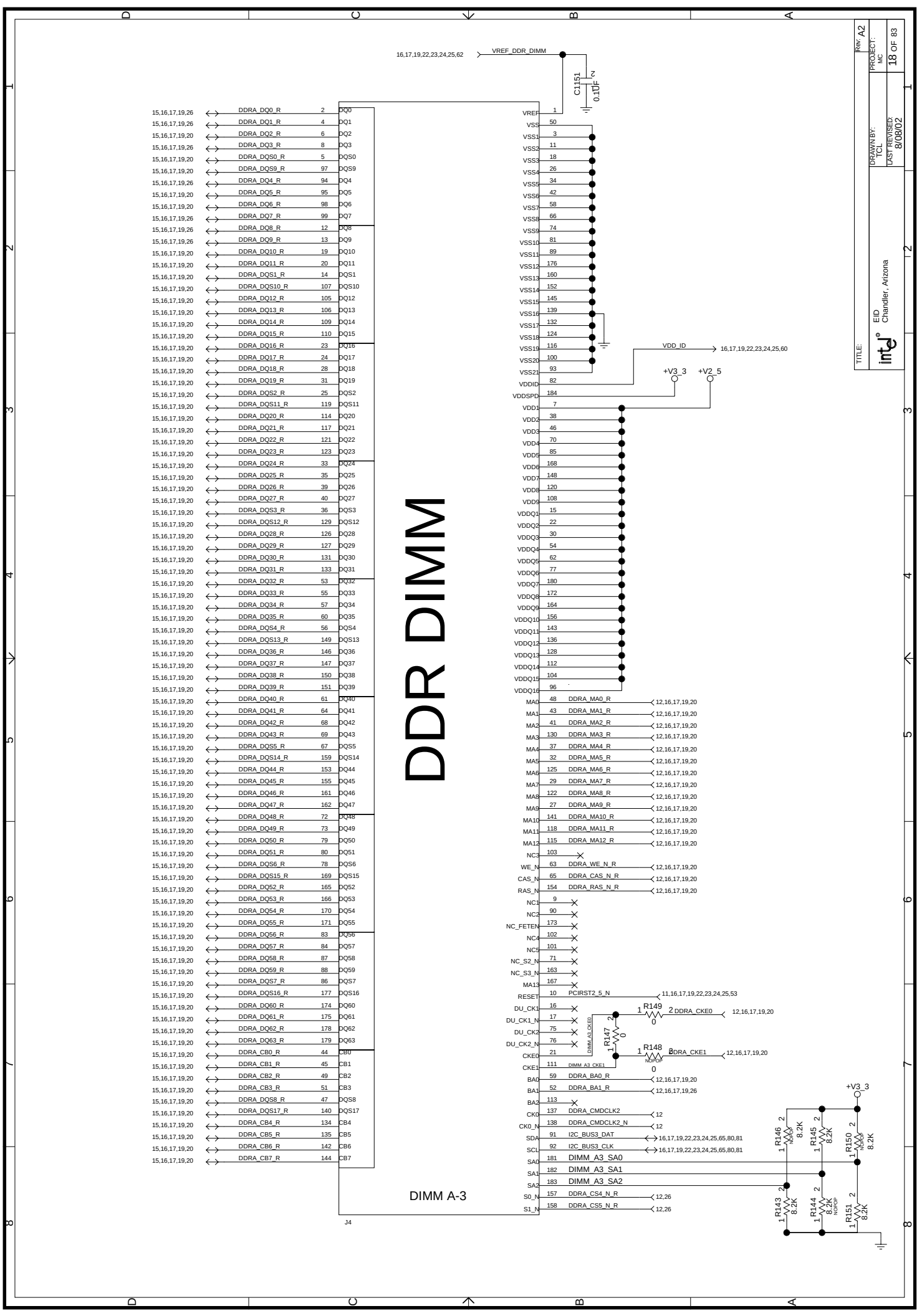
DDR DIMM
DIMM A-3
VREF_DDR_DIMM
C1151
0.1UF
VDD_ID
+V3_3
+V2_5
DDRA_DQ0_R
DDRA_DQ1_R
DDRA_DQ2_R
DDRA_DQ3_R
DDRA_DQS0_R
DDRA_DQS9_R
DDRA_DQ4_R
DDRA_DQ5_R
DDRA_DQ6_R
DDRA_DQ7_R
DDRA_DQ8_R
DDRA_DQ9_R
DDRA_DQ10_R
DDRA_DQ11_R
DDRA_DQS1_R
DDRA_DQS10_R
DDRA_DQ12_R
DDRA_DQ13_R
DDRA_DQ14_R
DDRA_DQ15_R
DDRA_DQ16_R
DDRA_DQ17_R
DDRA_DQ18_R
DDRA_DQ19_R
DDRA_DQS2_R
DDRA_DQS11_R
DDRA_DQ20_R
DDRA_DQ21_R
DDRA_DQ22_R
DDRA_DQ23_R
DDRA_DQ24_R
DDRA_DQ25_R
DDRA_DQ26_R
DDRA_DQ27_R
DDRA_DQS3_R
DDRA_DQS12_R
DDRA_DQ28_R
DDRA_DQ29_R
DDRA_DQ30_R
DDRA_DQ31_R
DDRA_DQ32_R
DDRA_DQ33_R
DDRA_DQ34_R
DDRA_DQ35_R
DDRA_DQS4_R
DDRA_DQS13_R
DDRA_DQ36_R
DDRA_DQ37_R
DDRA_DQ38_R
DDRA_DQ39_R
DDRA_DQ40_R
DDRA_DQ41_R
DDRA_DQ42_R
DDRA_DQ43_R
DDRA_DQS5_R
DDRA_DQS14_R
DDRA_DQ44_R
DDRA_DQ45_R
DDRA_DQ46_R
DDRA_DQ47_R
DDRA_DQ48_R
DDRA_DQ49_R
DDRA_DQ50_R
DDRA_DQ51_R
DDRA_DQS6_R
DDRA_DQS15_R
DDRA_DQ52_R
DDRA_DQ53_R
DDRA_DQ54_R
DDRA_DQ55_R
DDRA_DQ56_R
DDRA_DQ57_R
DDRA_DQ58_R
DDRA_DQ59_R
DDRA_DQS7_R
DDRA_DQS16_R
DDRA_DQ60_R
DDRA_DQ61_R
DDRA_DQ62_R
DDRA_DQ63_R
DDRA_CB0_R
DDRA_CB1_R
DDRA_CB2_R
DDRA_CB3_R
DDRA_DQS8_R
DDRA_DQS17_R
DDRA_CB4_R
DDRA_CB5_R
DDRA_CB6_R
DDRA_CB7_R
DDRA_MA0_R
DDRA_MA1_R
DDRA_MA2_R
DDRA_MA3_R
DDRA_MA4_R
DDRA_MA5_R
DDRA_MA6_R
DDRA_MA7_R
DDRA_MA8_R
DDRA_MA9_R
DDRA_MA10_R
DDRA_MA11_R
DDRA_MA12_R
DDRA_WE_N_R
DDRA_CAS_N_R
DDRA_RAS_N_R
PCIRST2_5_N
DDRA_CKE0
DDRA_CKE1
DDRA_BA0_R
DDRA_BA1_R
DDRA_CMDCLK2
DDRA_CMDCLK2_N
I2C_BUS3_DAT
I2C_BUS3_CLK
DIMM_A3_SA0
DIMM_A3_SA1
DIMM_A3_SA2
DDRA_CS4_N_R
DDRA_CS5_N_R
R149
R147
R148
R146
R145
R150
R143
R144
R151
8.2K
NOPOP
J4
TITLE:
intel
EID
Chandler, Arizona
DRAWN BY:
TCL
LAST REVISED:
8/08/02
PROJECT:
MC
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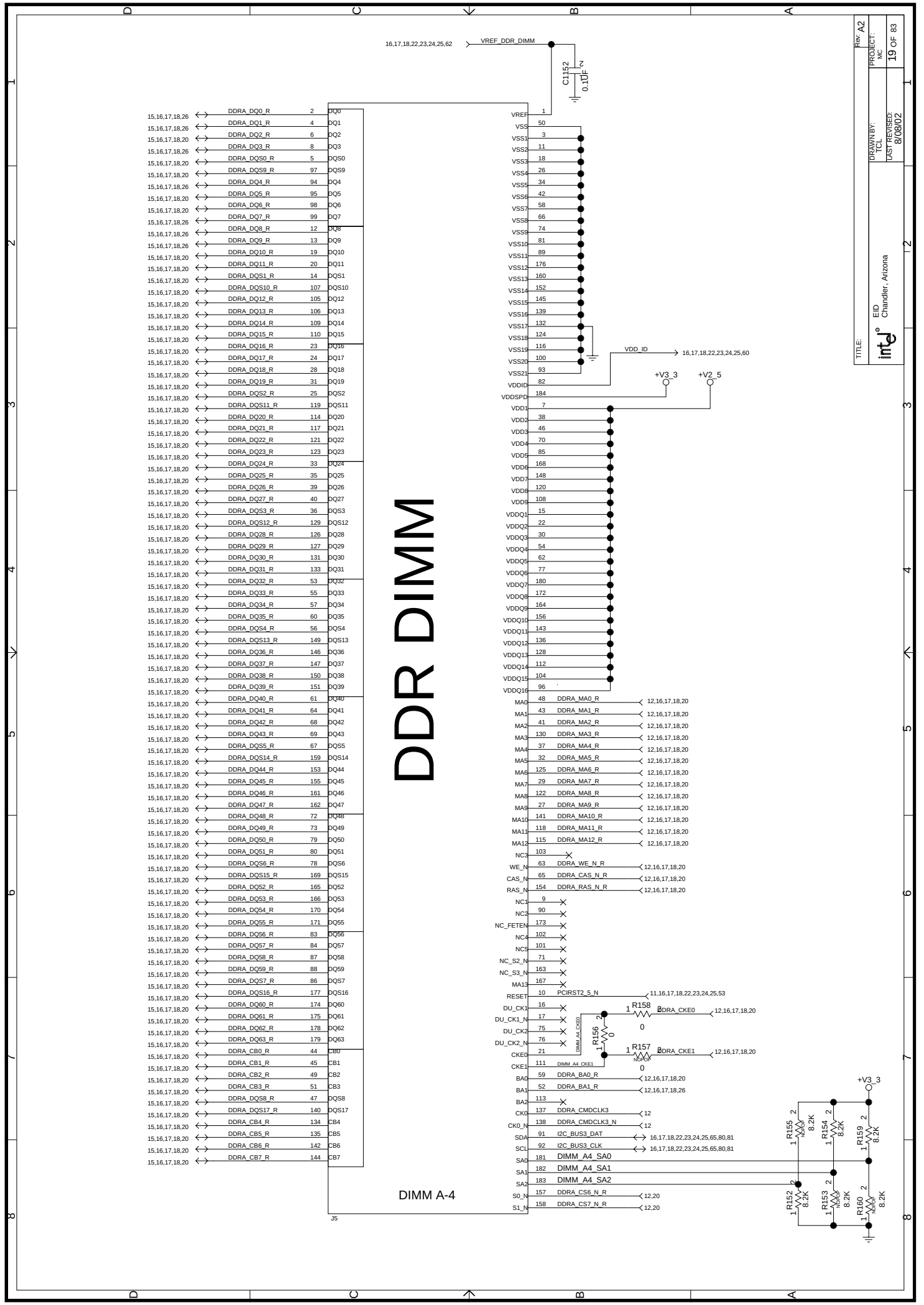
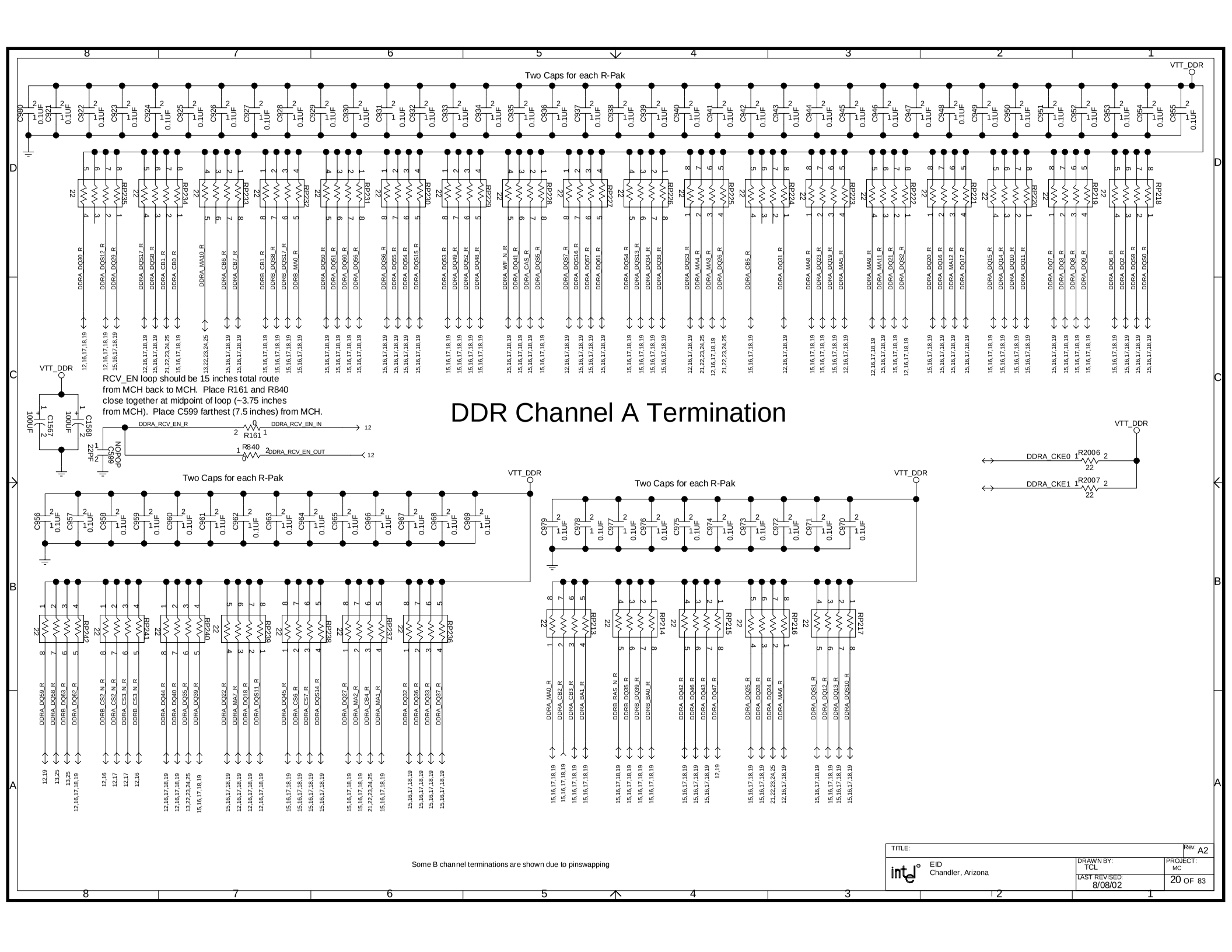

DDR DIMM
DIMM A-4
VREF_DDR_DIMM
C1152
0.1UF
VDD_ID
+V3_3
+V2_5
DDRA_DQ0_R
DDRA_DQ1_R
DDRA_DQ2_R
DDRA_DQ3_R
DDRA_DQS0_R
DDRA_DQS9_R
DDRA_DQ4_R
DDRA_DQ5_R
DDRA_DQ6_R
DDRA_DQ7_R
DDRA_DQ8_R
DDRA_DQ9_R
DDRA_DQ10_R
DDRA_DQ11_R
DDRA_DQS1_R
DDRA_DQS10_R
DDRA_DQ12_R
DDRA_DQ13_R
DDRA_DQ14_R
DDRA_DQ15_R
DDRA_DQ16_R
DDRA_DQ17_R
DDRA_DQ18_R
DDRA_DQ19_R
DDRA_DQS2_R
DDRA_DQS11_R
DDRA_DQ20_R
DDRA_DQ21_R
DDRA_DQ22_R
DDRA_DQ23_R
DDRA_DQ24_R
DDRA_DQ25_R
DDRA_DQ26_R
DDRA_DQ27_R
DDRA_DQS3_R
DDRA_DQS12_R
DDRA_DQ28_R
DDRA_DQ29_R
DDRA_DQ30_R
DDRA_DQ31_R
DDRA_DQ32_R
DDRA_DQ33_R
DDRA_DQ34_R
DDRA_DQ35_R
DDRA_DQS4_R
DDRA_DQS13_R
DDRA_DQ36_R
DDRA_DQ37_R
DDRA_DQ38_R
DDRA_DQ39_R
DDRA_DQ40_R
DDRA_DQ41_R
DDRA_DQ42_R
DDRA_DQ43_R
DDRA_DQS5_R
DDRA_DQS14_R
DDRA_DQ44_R
DDRA_DQ45_R
DDRA_DQ46_R
DDRA_DQ47_R
DDRA_DQ48_R
DDRA_DQ49_R
DDRA_DQ50_R
DDRA_DQ51_R
DDRA_DQS6_R
DDRA_DQS15_R
DDRA_DQ52_R
DDRA_DQ53_R
DDRA_DQ54_R
DDRA_DQ55_R
DDRA_DQ56_R
DDRA_DQ57_R
DDRA_DQ58_R
DDRA_DQ59_R
DDRA_DQS7_R
DDRA_DQS16_R
DDRA_DQ60_R
DDRA_DQ61_R
DDRA_DQ62_R
DDRA_DQ63_R
DDRA_CB0_R
DDRA_CB1_R
DDRA_CB2_R
DDRA_CB3_R
DDRA_DQS8_R
DDRA_DQS17_R
DDRA_CB4_R
DDRA_CB5_R
DDRA_CB6_R
DDRA_CB7_R
DDRA_MA0_R
DDRA_MA1_R
DDRA_MA2_R
DDRA_MA3_R
DDRA_MA4_R
DDRA_MA5_R
DDRA_MA6_R
DDRA_MA7_R
DDRA_MA8_R
DDRA_MA9_R
DDRA_MA10_R
DDRA_MA11_R
DDRA_MA12_R
DDRA_WE_N_R
DDRA_CAS_N_R
DDRA_RAS_N_R
PCIRST2_5_N
R158
R156
R157
DDRA_CKE0
DDRA_CKE1
DIMM_A4_CKE0
DIMM_A4_CKE1
DDRA_BA0_R
DDRA_BA1_R
DDRA_CMDCLK3
DDRA_CMDCLK3_N
I2C_BUS3_DAT
I2C_BUS3_CLK
DIMM_A4_SA0
DIMM_A4_SA1
DIMM_A4_SA2
DDRA_CS6_N_R
DDRA_CS7_N_R
R155
R154
R159
R152
R153
R160
8.2K
J5
TITLE:
intel
EID
Chandler, Arizona
DRAWN BY:
TCL
LAST REVISED:
8/08/02
PROJECT:
MC
19 OF 83
Rev: A2

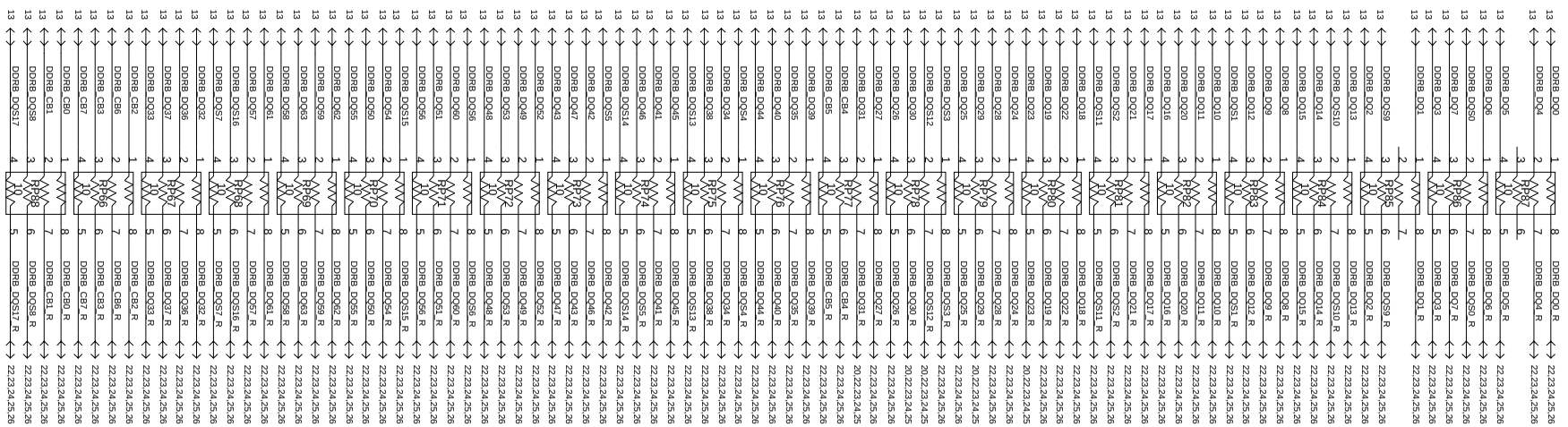
DDR Channel A Termination

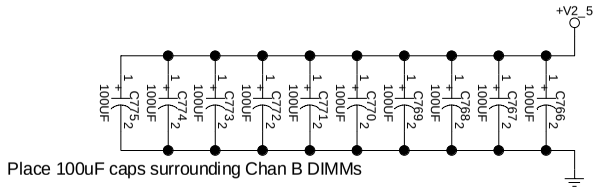


TITLE:		Rev: A2
intel EID Chandler, Arizona	DRAWN BY: TCL	PROJECT: MC
	LAST REVISED: 8/08/02	20 OF 83

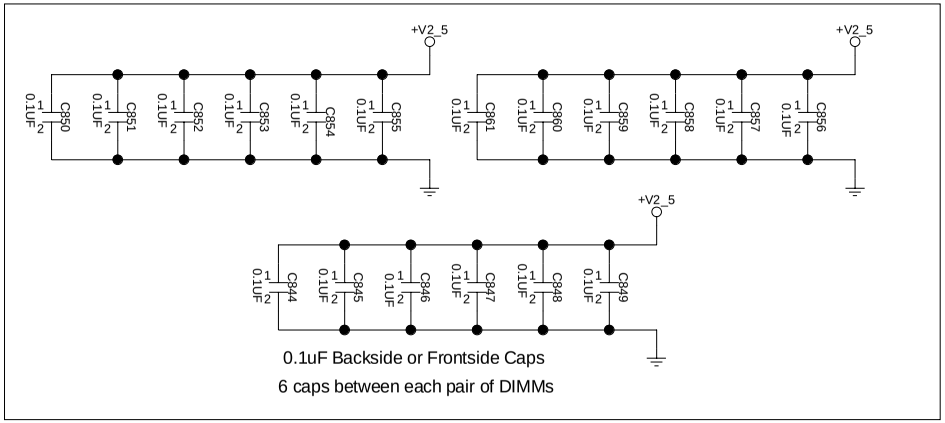
DDR Channel B Series Resistors

Place near DIMM B-1





Place 100uF caps surrounding Chan B DIMMs



0.1uF Backside or Frontside Caps

6 caps between each pair of DIMMs

CAD Note: All Caps should have direct attatchment to 2.5V plane, and 2 vias to GND.

TITLE:		Rev: A2
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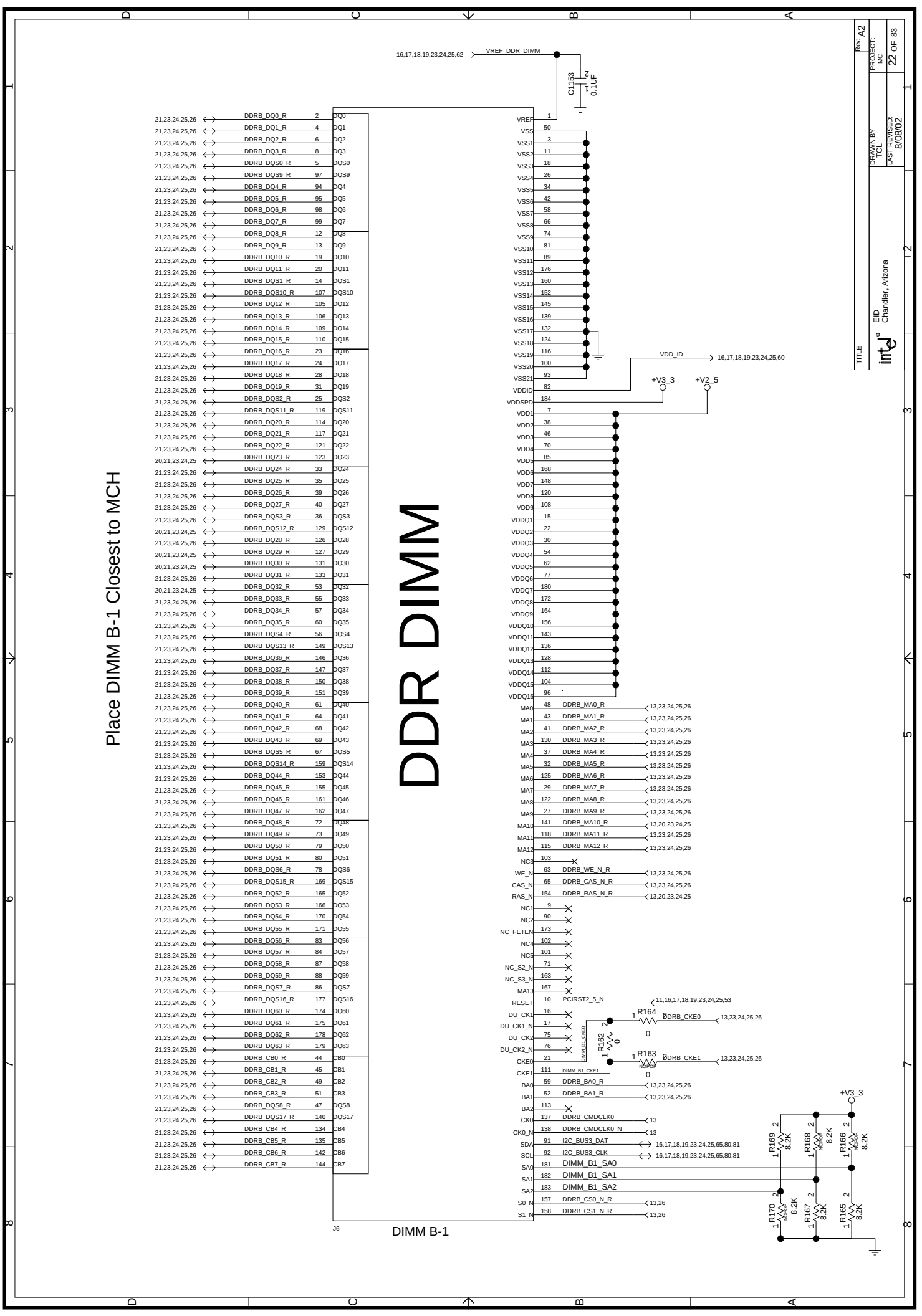
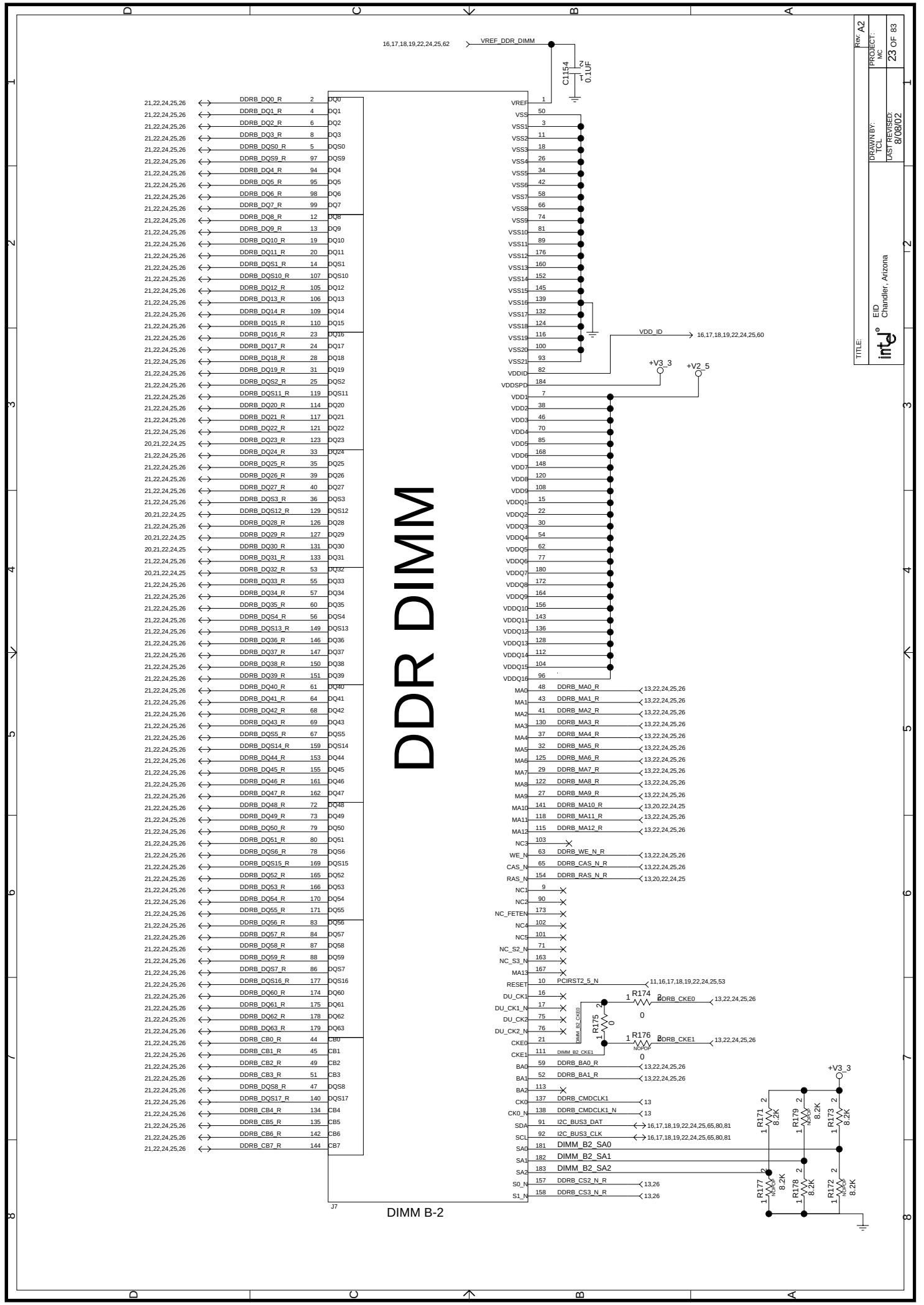
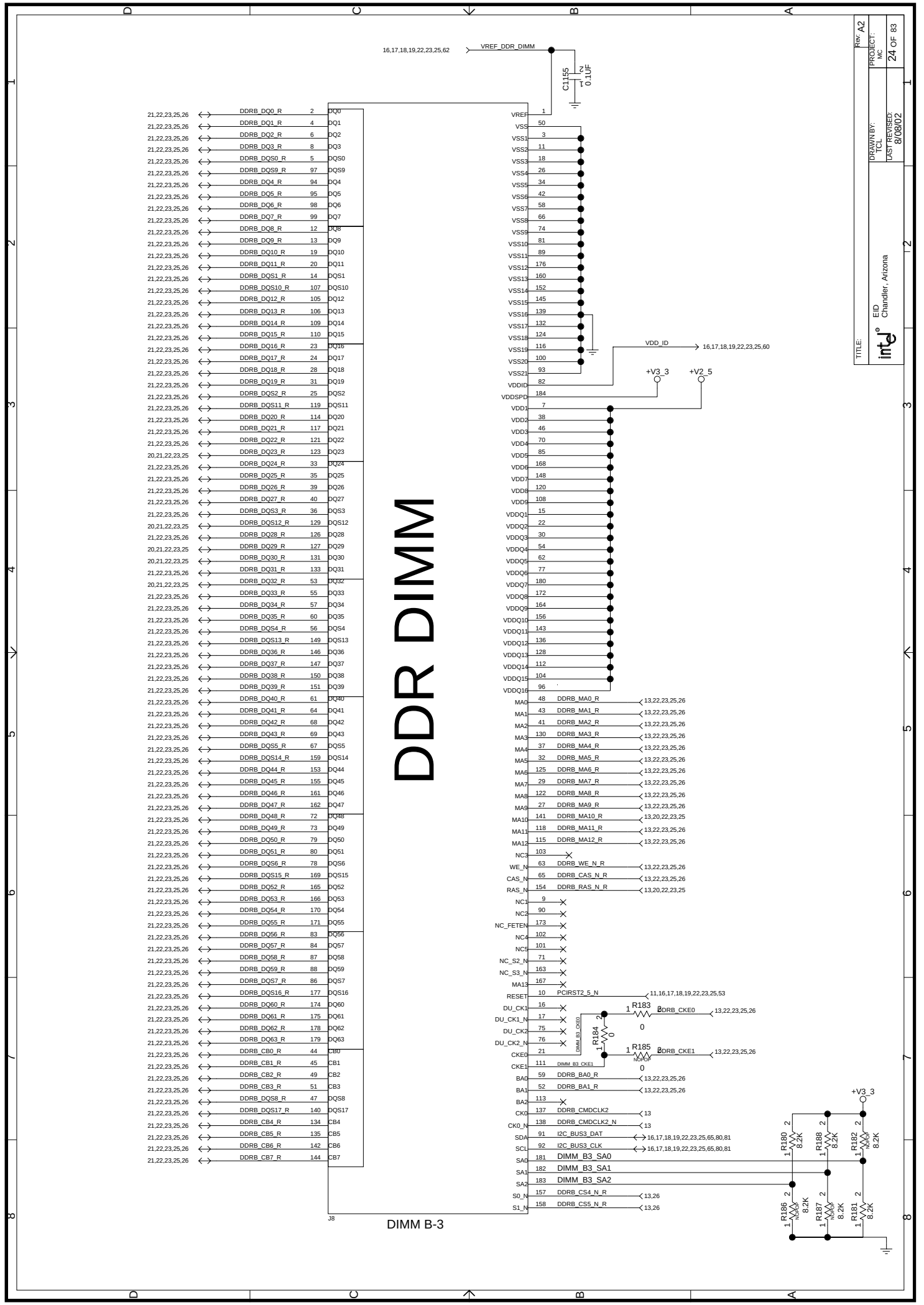

Place DIMM B-1 Closest to MCH
DDR DIMM
DIMM B-1
J6
VREF_DDR_DIMM
C1153
0.1UF
VDD_ID
+V3_3
+V2_5
DDRB_DQ0_R
DDRB_DQ1_R
DDRB_DQ2_R
DDRB_DQ3_R
DDRB_DQS0_R
DDRB_DQS9_R
DDRB_DQ4_R
DDRB_DQ5_R
DDRB_DQ6_R
DDRB_DQ7_R
DDRB_DQ8_R
DDRB_DQ9_R
DDRB_DQ10_R
DDRB_DQ11_R
DDRB_DQS1_R
DDRB_DQS10_R
DDRB_DQ12_R
DDRB_DQ13_R
DDRB_DQ14_R
DDRB_DQ15_R
DDRB_DQ16_R
DDRB_DQ17_R
DDRB_DQ18_R
DDRB_DQ19_R
DDRB_DQS2_R
DDRB_DQS11_R
DDRB_DQ20_R
DDRB_DQ21_R
DDRB_DQ22_R
DDRB_DQ23_R
DDRB_DQ24_R
DDRB_DQ25_R
DDRB_DQ26_R
DDRB_DQ27_R
DDRB_DQS3_R
DDRB_DQS12_R
DDRB_DQ28_R
DDRB_DQ29_R
DDRB_DQ30_R
DDRB_DQ31_R
DDRB_DQ32_R
DDRB_DQ33_R
DDRB_DQ34_R
DDRB_DQ35_R
DDRB_DQS4_R
DDRB_DQS13_R
DDRB_DQ36_R
DDRB_DQ37_R
DDRB_DQ38_R
DDRB_DQ39_R
DDRB_DQ40_R
DDRB_DQ41_R
DDRB_DQ42_R
DDRB_DQ43_R
DDRB_DQS5_R
DDRB_DQS14_R
DDRB_DQ44_R
DDRB_DQ45_R
DDRB_DQ46_R
DDRB_DQ47_R
DDRB_DQ48_R
DDRB_DQ49_R
DDRB_DQ50_R
DDRB_DQ51_R
DDRB_DQS6_R
DDRB_DQS15_R
DDRB_DQ52_R
DDRB_DQ53_R
DDRB_DQ54_R
DDRB_DQ55_R
DDRB_DQ56_R
DDRB_DQ57_R
DDRB_DQ58_R
DDRB_DQ59_R
DDRB_DQS7_R
DDRB_DQS16_R
DDRB_DQ60_R
DDRB_DQ61_R
DDRB_DQ62_R
DDRB_DQ63_R
DDRB_CB0_R
DDRB_CB1_R
DDRB_CB2_R
DDRB_CB3_R
DDRB_DQS8_R
DDRB_DQS17_R
DDRB_CB4_R
DDRB_CB5_R
DDRB_CB6_R
DDRB_CB7_R
DDRB_MA0_R
DDRB_MA1_R
DDRB_MA2_R
DDRB_MA3_R
DDRB_MA4_R
DDRB_MA5_R
DDRB_MA6_R
DDRB_MA7_R
DDRB_MA8_R
DDRB_MA9_R
DDRB_MA10_R
DDRB_MA11_R
DDRB_MA12_R
DDRB_WE_N_R
DDRB_CAS_N_R
DDRB_RAS_N_R
PCIRST2_5_N
DIMM_B1_CKE0
DIMM_B1_CKE1
DDRB_BA0_R
DDRB_BA1_R
DDRB_CMDCLK0
DDRB_CMDCLK0_N
I2C_BUS3_DAT
I2C_BUS3_CLK
DIMM_B1_SA0
DIMM_B1_SA1
DIMM_B1_SA2
DDRB_CS0_N_R
DDRB_CS1_N_R
R164
R163
R162
R169
R168
R166
R170
R167
R165
8.2K
0
NOPOP
DRAWN BY: TCL
LAST REVISED: 8/08/02
PROJECT: MC
Rev: A2
22 OF 83
TITLE:
EID
Chandler, Arizona


DDR DIMM
VREF_DDR_DIMM
16,17,18,19,22,24,25,62
C1154
0.1UF
VDD_ID
16,17,18,19,22,24,25,60
+V3_3
+V2_5
DIMM_B2_SA0
DIMM_B2_SA1
DIMM_B2_SA2
DIMM B-2
J7
Rev: A2
PROJECT: MC
23 OF 83
DRAWN BY: TCL
LAST REVISED: 8/08/02
TITLE:
EID
Chandler, Arizona


DDR DIMM
VREF_DDR_DIMM
16,17,18,19,22,23,25,62
C1155
0.1UF
VDD_ID
16,17,18,19,22,23,25,60
+V3_3
+V2_5
DIMM_B3_SA0
DIMM_B3_SA1
DIMM_B3_SA2
R180
R188
R182
R186
R187
R181
8.2K
R183
R184
R185
0
DIMM_B3_CKE0
DIMM_B3_CKE1
J8
DIMM B-3
TITLE:
EID
Chandler, Arizona
DRAWN BY:
TCL
LAST REVISED:
8/08/02
PROJECT:
MC
Rev: A2
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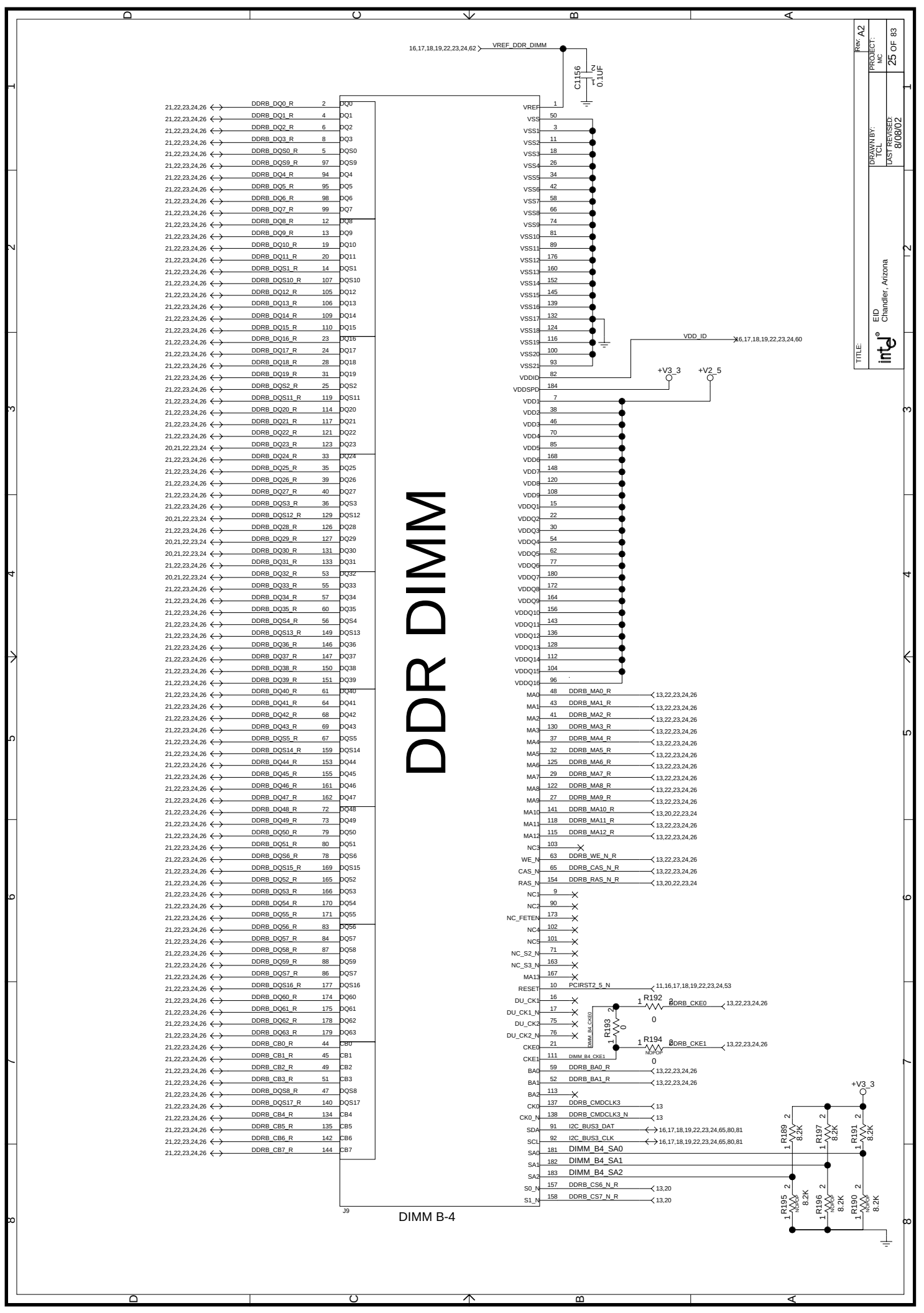
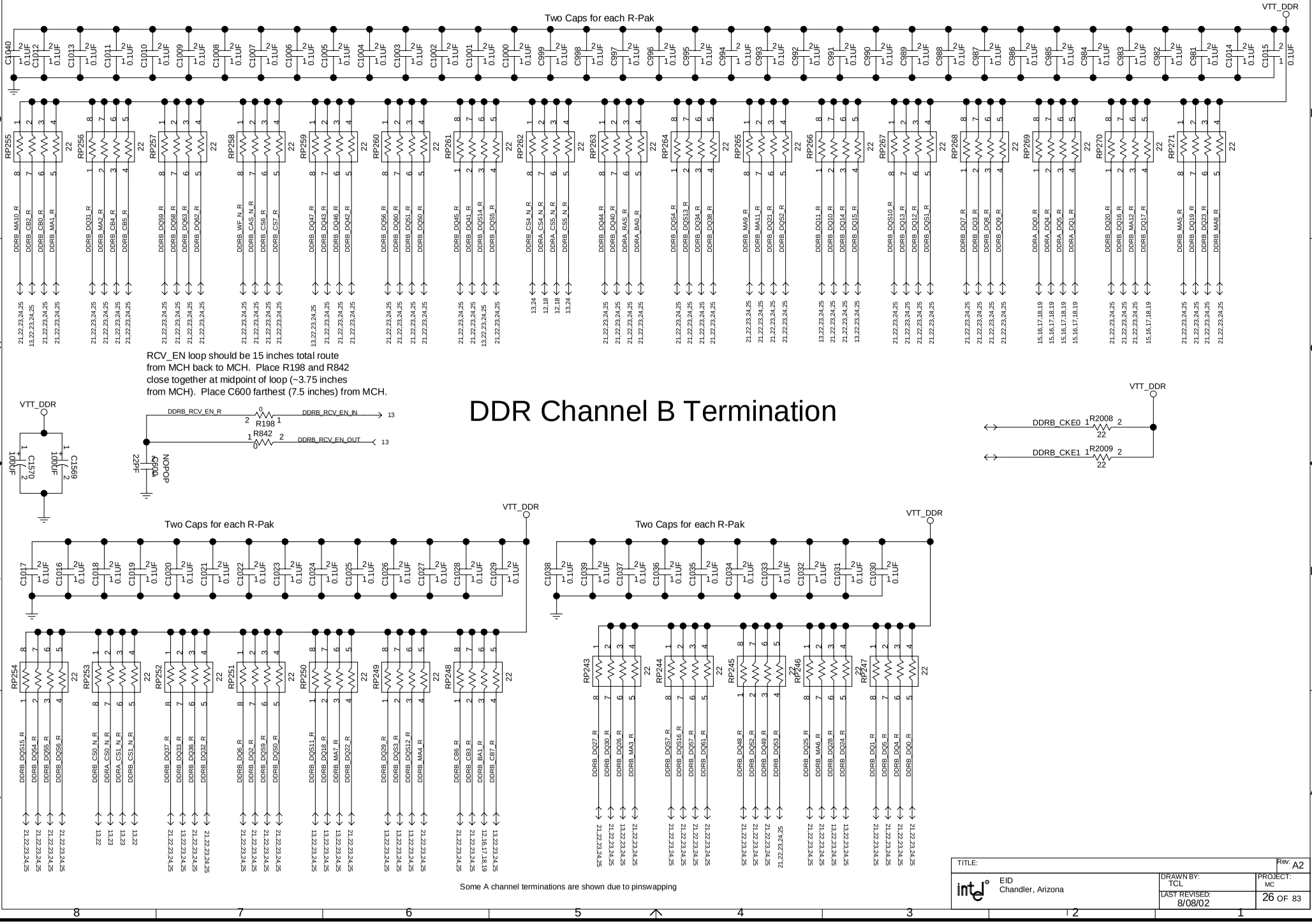

DDR DIMM
VREF_DDR_DIMM
C1156
0.1UF
VDD_ID
+V3_3
+V2_5
J9
DIMM B-4
R192
R193
R194
DIMM_B4_CKE0
DIMM_B4_CKE1
DIMM_B4_SA0
DIMM_B4_SA1
DIMM_B4_SA2
R189
R197
R191
R195
R196
R190
8.2K
NOSTUFF
Rev: A2
PROJECT: MC
25 OF 83
DRAWN BY: TCL
LAST REVISED: 8/08/02
TITLE:
EID
Chandler, Arizona

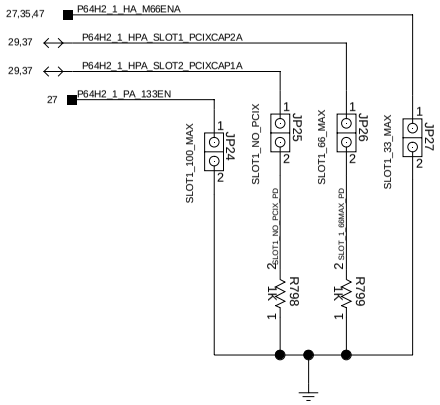
DDR Channel B Termination

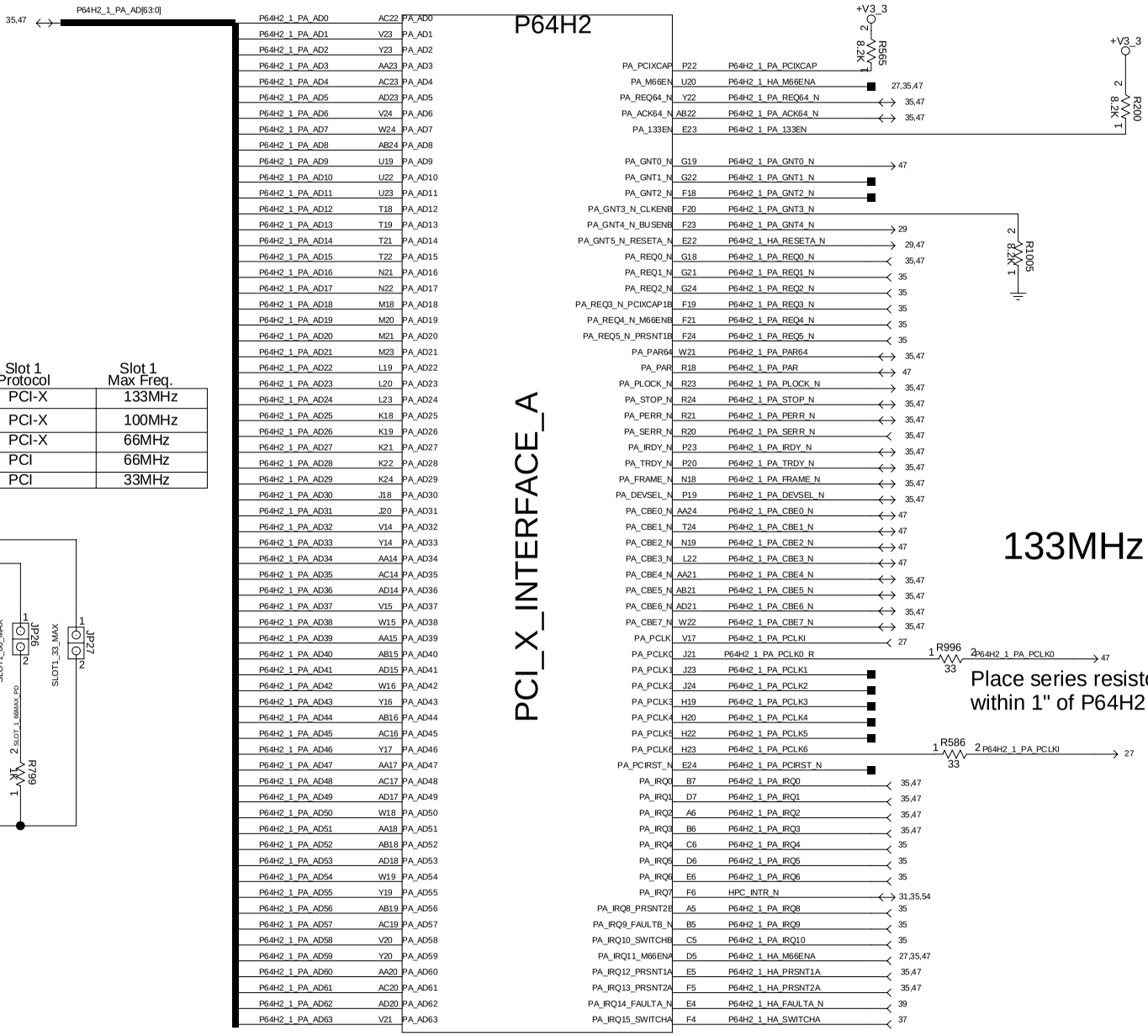


TITLE:			Rev: A2
intel EID Chandler, Arizona	DRAWN BY: TCL	PROJECT: MC	
	LAST REVISED: 8/08/02	26 OF 83	

For Validation Only

JP24	JP25	JP26	JP27	Slot 1 Protocol	Slot 1 Max Freq.
No Jumper	No Jumper	No Jumper	No Jumper	PCI-X	133MHz
Jumper	No Jumper	No Jumper	No Jumper	PCI-X	100MHz
Jumper	No Jumper	Jumper	No Jumper	PCI-X	66MHz
Jumper	Jumper	Jumper	No Jumper	PCI	66MHz
Jumper	Jumper	Jumper	Jumper	PCI	33MHz

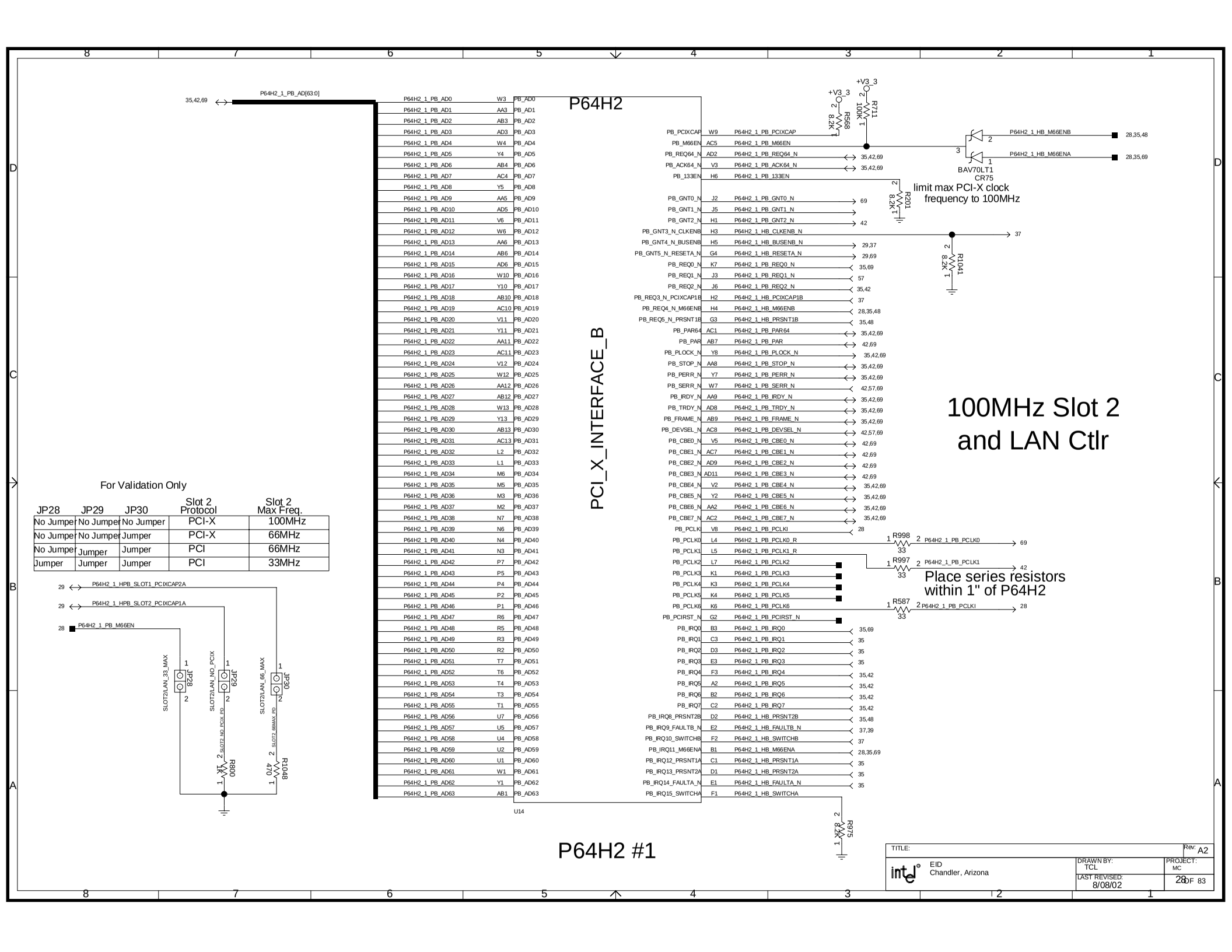




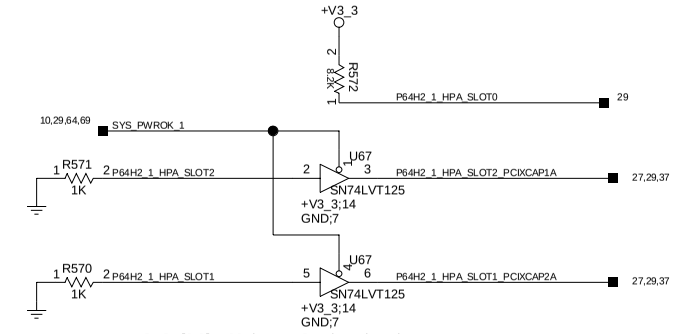
133MHz Slot 1

P64H2 #1

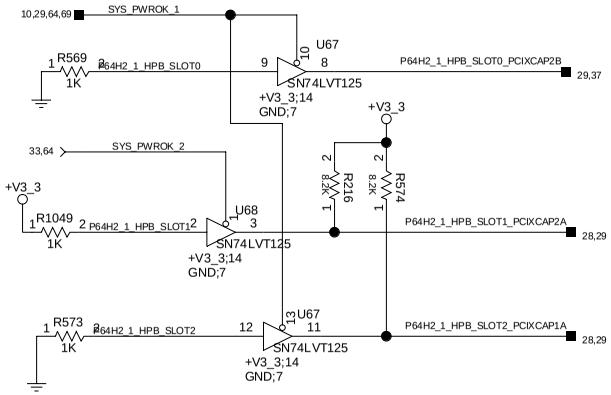
TITLE:	Rev: A2
EID Chandler, Arizona	DRAWN BY: TCL
	PROJECT: MC
	LAST REVISED: 8/08/02
	27 OF 83


P64H2
PCI_X_INTERFACE_B
100MHz Slot 2
and LAN Ctlr
P64H2 #1
For Validation Only
JP28 JP29 JP30 Slot 2 Protocol Slot 2 Max Freq.
No Jumper No Jumper No Jumper PCI-X 100MHz
No Jumper No Jumper Jumper PCI-X 66MHz
No Jumper Jumper Jumper PCI 66MHz
Jumper Jumper Jumper PCI 33MHz
limit max PCI-X clock frequency to 100MHz
Place series resistors within 1" of P64H2
BAV70LT1
CR75
U14
TITLE:
Rev: A2
EID
Chandler, Arizona
DRAWN BY: TCL
LAST REVISED: 8/08/02
PROJECT: MC
28 OF 83

P64H2 #1

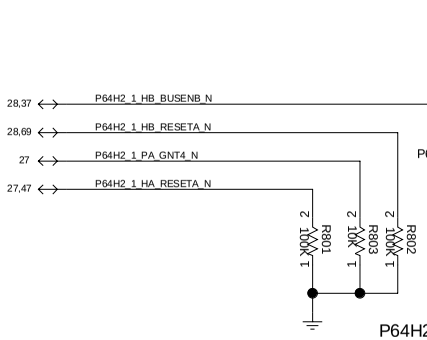


HPA_SLOT[2:0] = 001b ==> One hot-plug slot



HPB_SLOT[2:0] = 010b ==> Two hot-plug slots

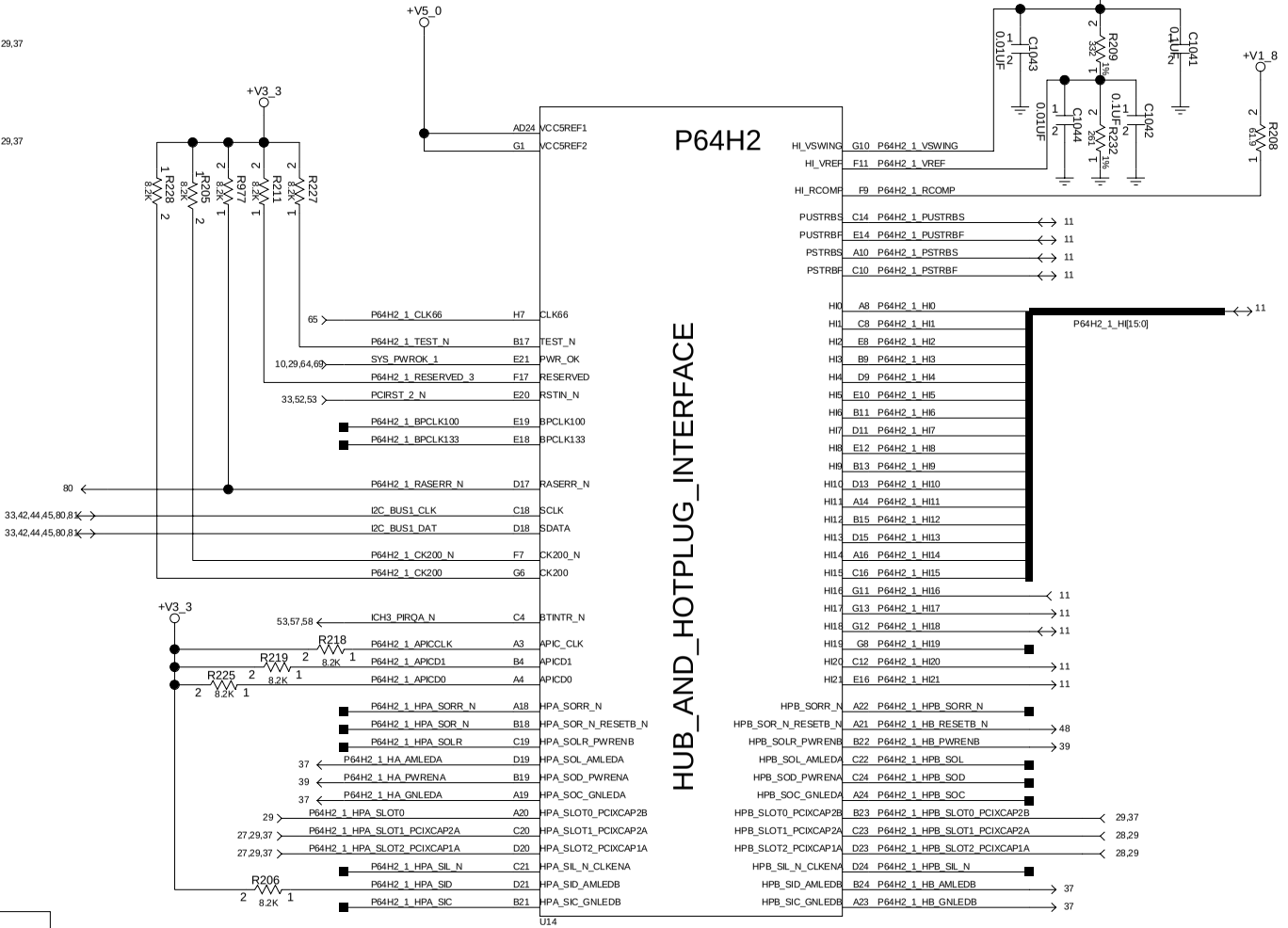
PCIXCAP[2:1]B= 11b ==> 100MHz PCI-X capable



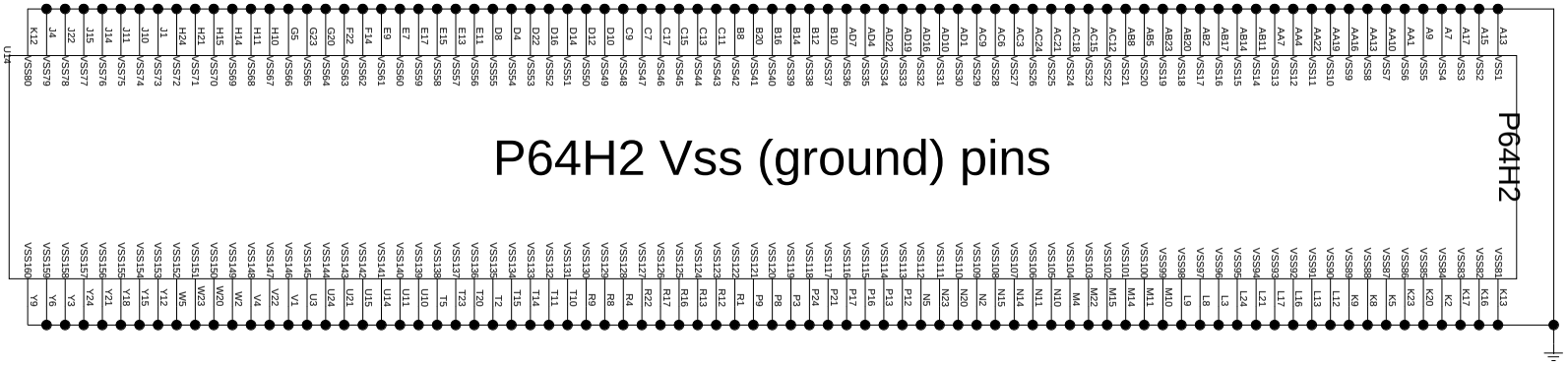
P64H2 SMBus Address Strapping

Bit	Value
7	1
6	1
5	PA_GNT5_RESETA_N
4	0
3	PA_GNT4_BUSENB_N
2	PB_GNT5_RESETA_N
1	PB_GNT4_BUSENB_N

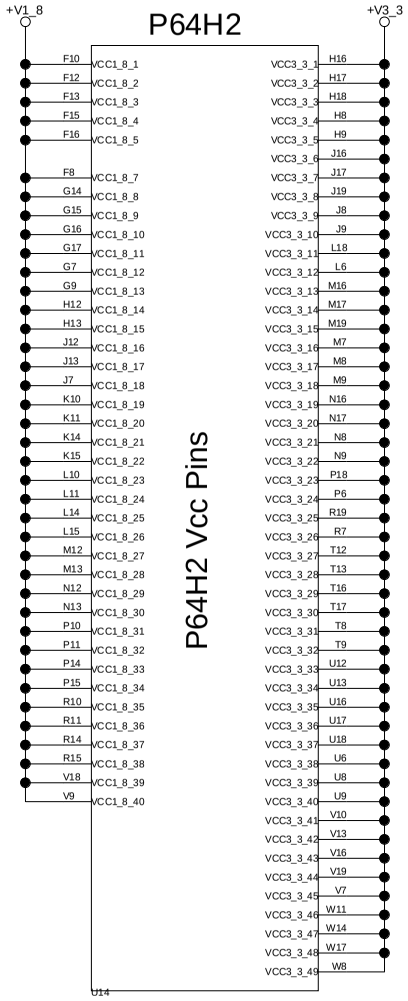
P64H2 #1 SMBus Address = C2h

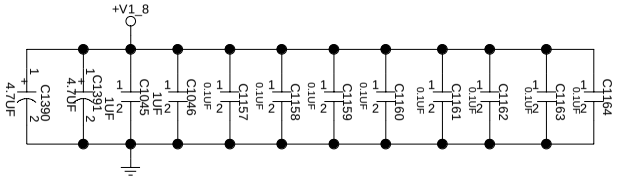


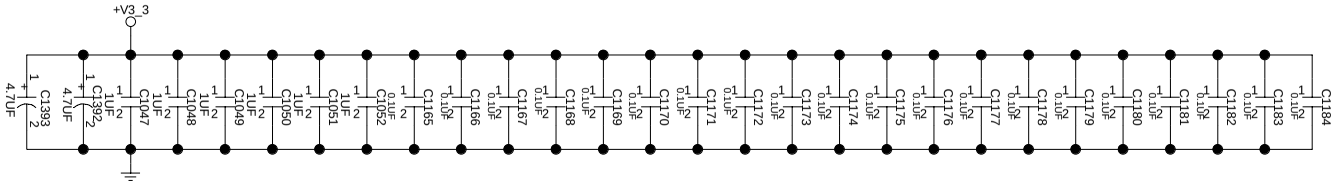
TITLE:			Rev: A2
intel EID Chandler, Arizona	DRAWN BY: TCL	PROJECT: MC	
	LAST REVISED: 8/08/02	29 OF 83	



P64H2 Vss (ground) pins







P64H2 #1 power, ground and decoupling

TITLE:		Rev: A2
intel EID Chandler, Arizona	DRAWN BY: TCL	PROJECT: MC
	LAST REVISED: 8/08/02	30 OF 83

133MHz AIC-7902 SCSI

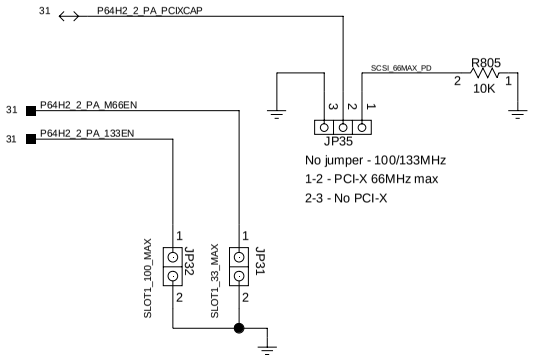
P64H2

PCI_X_INTERFACE_A

P64H2 #2

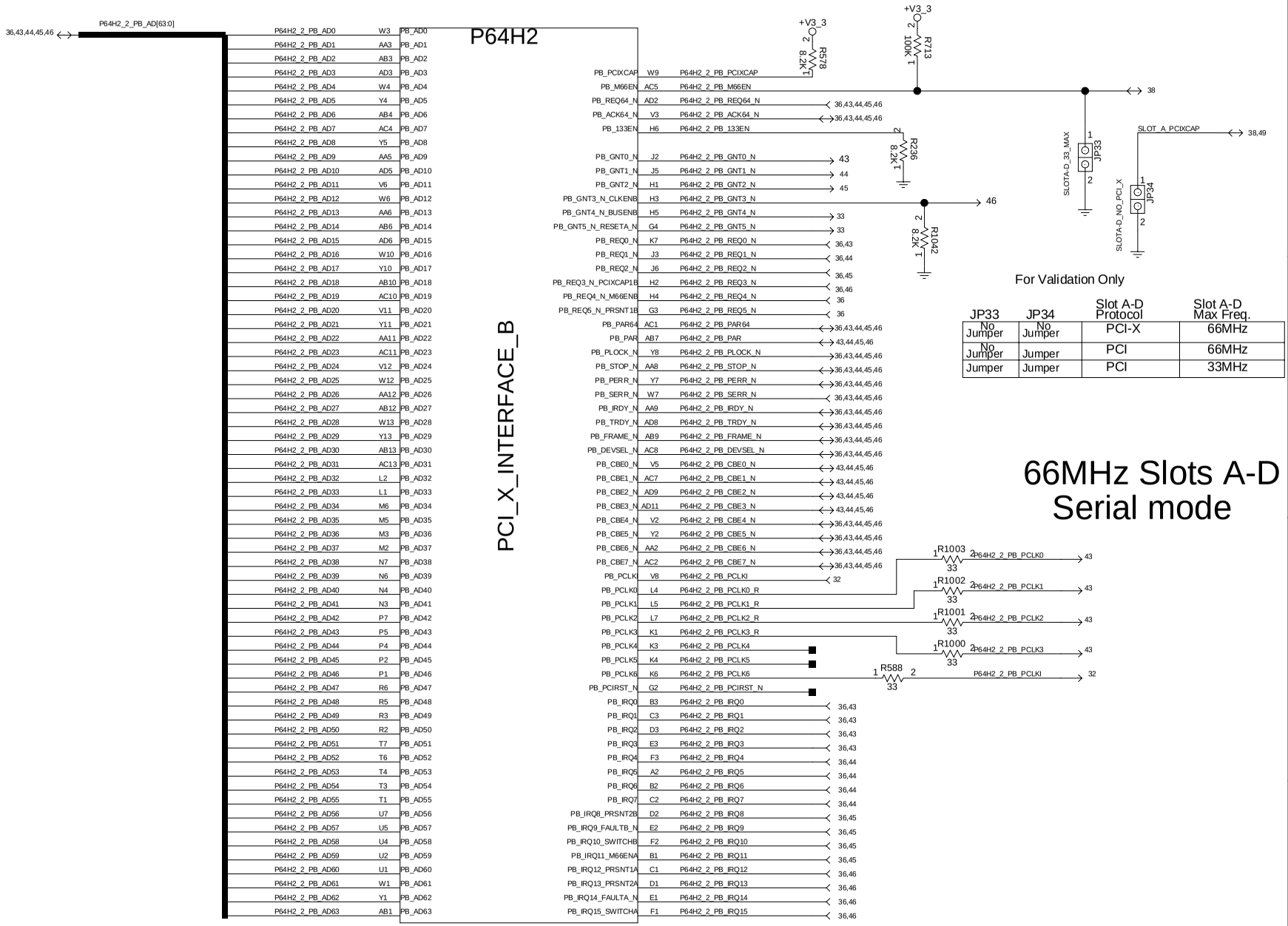
For Validation Only

JP31	JP32	JP35	Protocol	Max Freq.
No Jumper	No Jumper	No Jumper	PCI-X	133MHz
No Jumper	Jumper	No Jumper	PCI-X	100MHz
No Jumper	Jumper	Pin 1-2	PCI-X	66MHz
No Jumper	Jumper	Pin 2-3	PCI	66MHz
Jumper	Jumper	Pin 2-3	PCI	33MHz



Place series resistors within 1" of P64H2

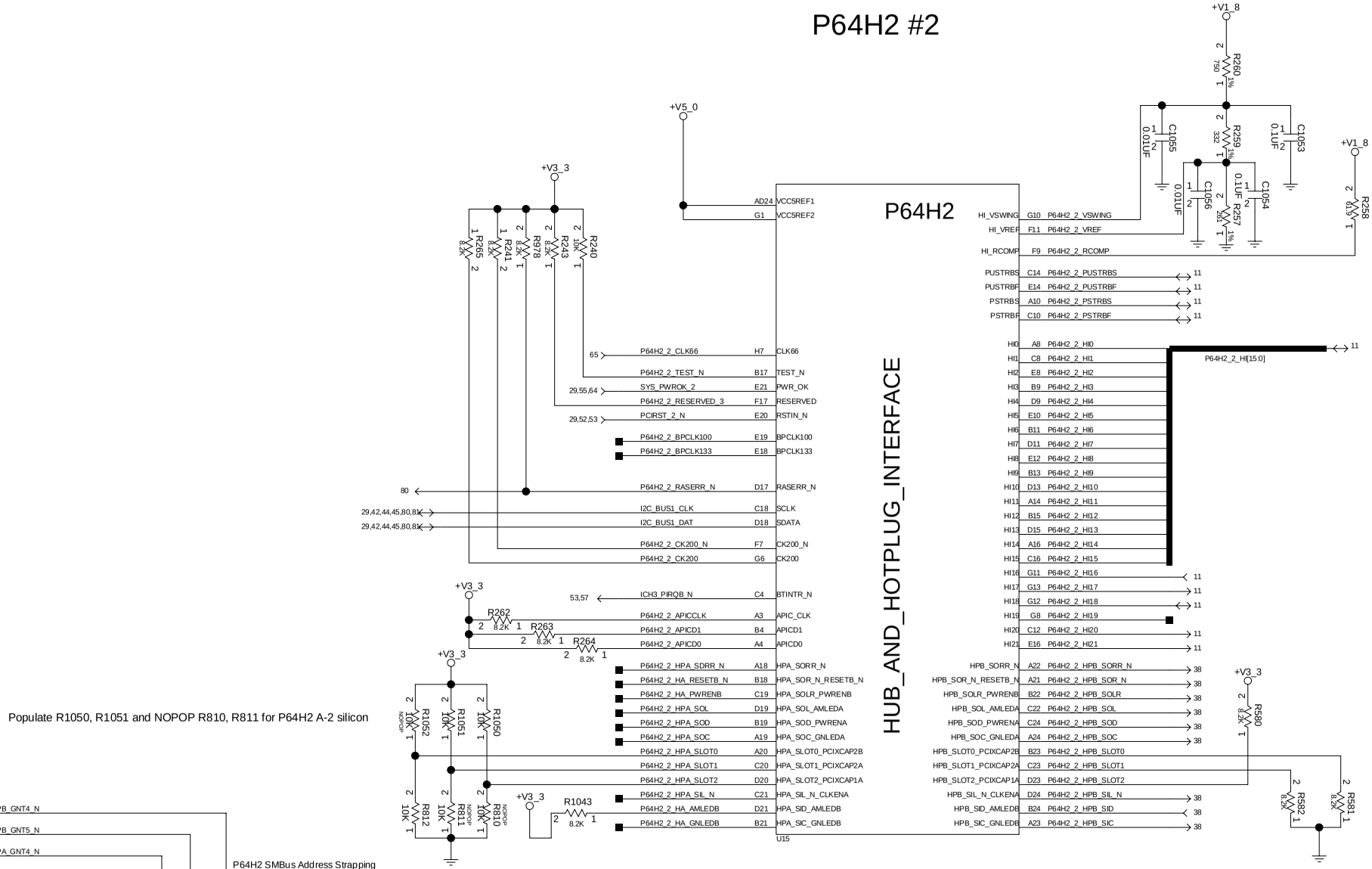
TITLE:		Rev: A2
intel EID Chandler, Arizona	DRAWN BY: TCL	PROJECT: MC
	LAST REVISED: 8/08/02	31 OF 83



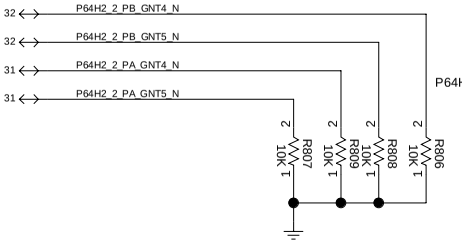
P64H2 #2

TITLE:		Rev: A2
intel EID Chandler, Arizona	DRAWN BY: TCL	PROJECT: MC
	LAST REVISED: 8/08/02	32 OF 83

P64H2 #2



Populate R1050, R1051 and NOPOP R810, R811 for P64H2 A-2 silicon

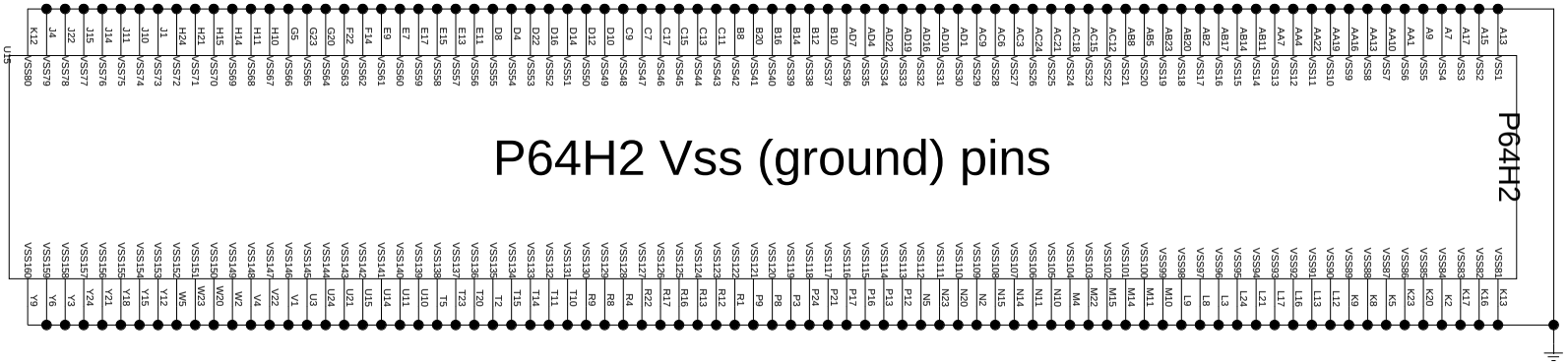


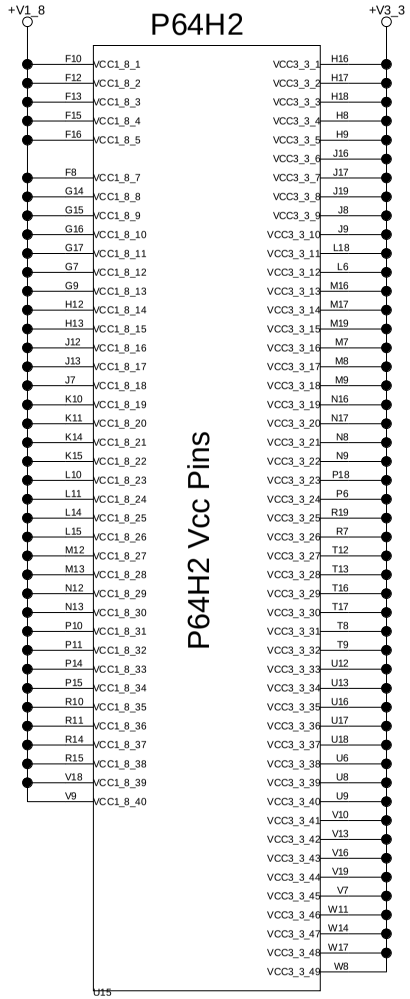
P64H2 SMBus Address Strapping

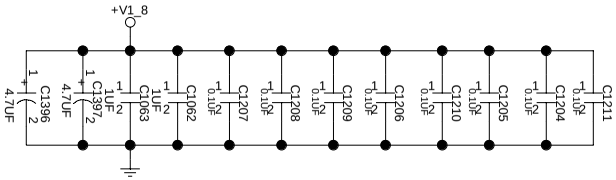
Bit	Value
7	1
6	1
5	PA_GNT5_RESETA_N
4	0
3	PA_GNT4_BUSENB_N
2	PB_GNT5_RESETA_N
1	PB_GNT4_BUSENB_N

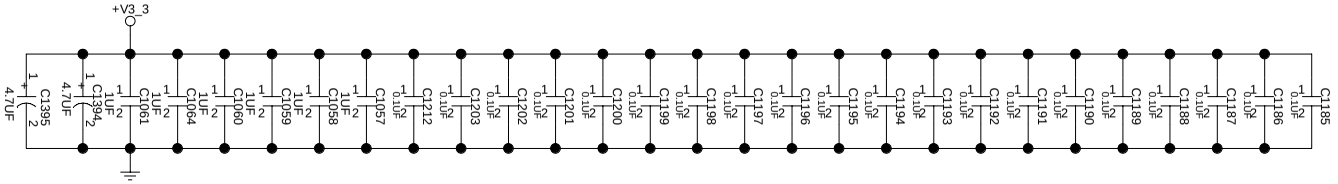
P64H2 #2 SMBus Address = C0h

TITLE:		Rev: A2
intel EID Chandler, Arizona	DRAWN BY: TCL	PROJECT: MC
	LAST REVISED: 8/08/02	33 OF 83



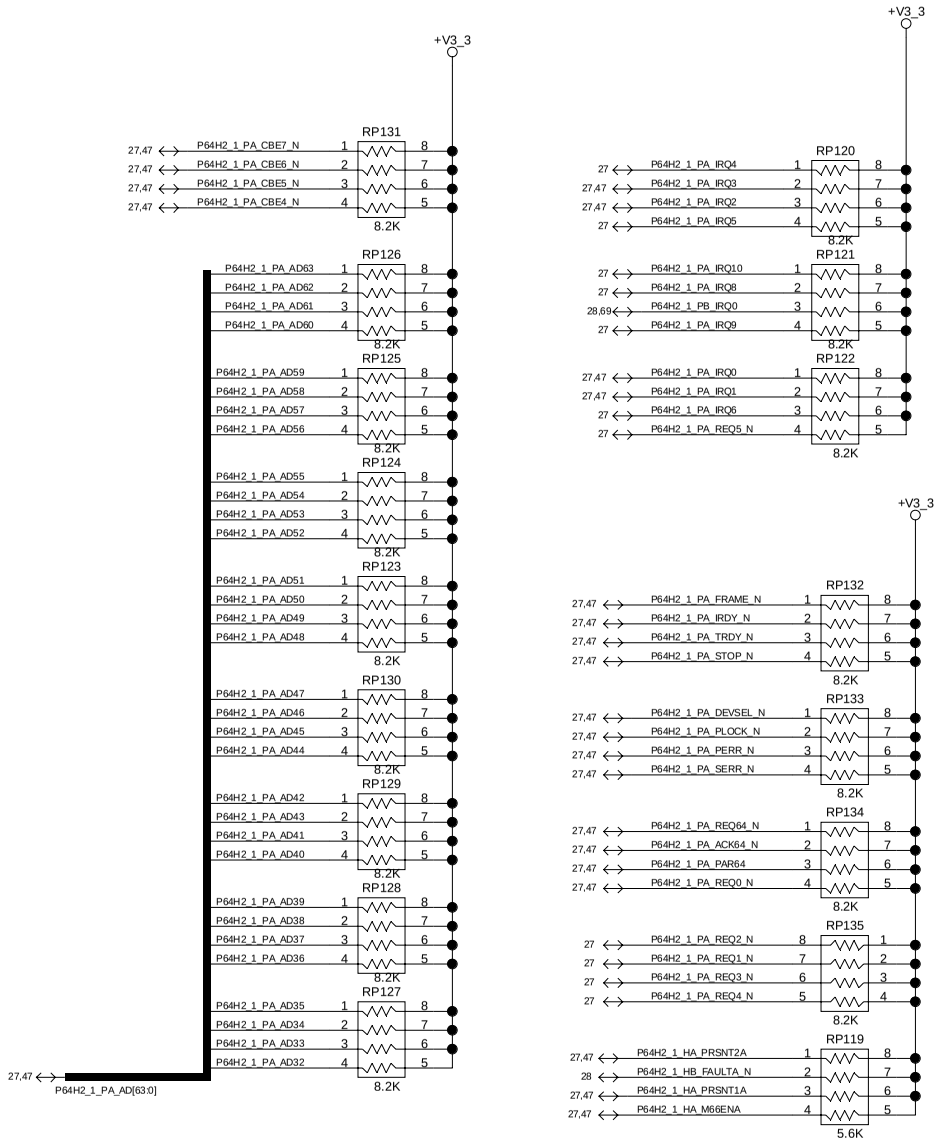




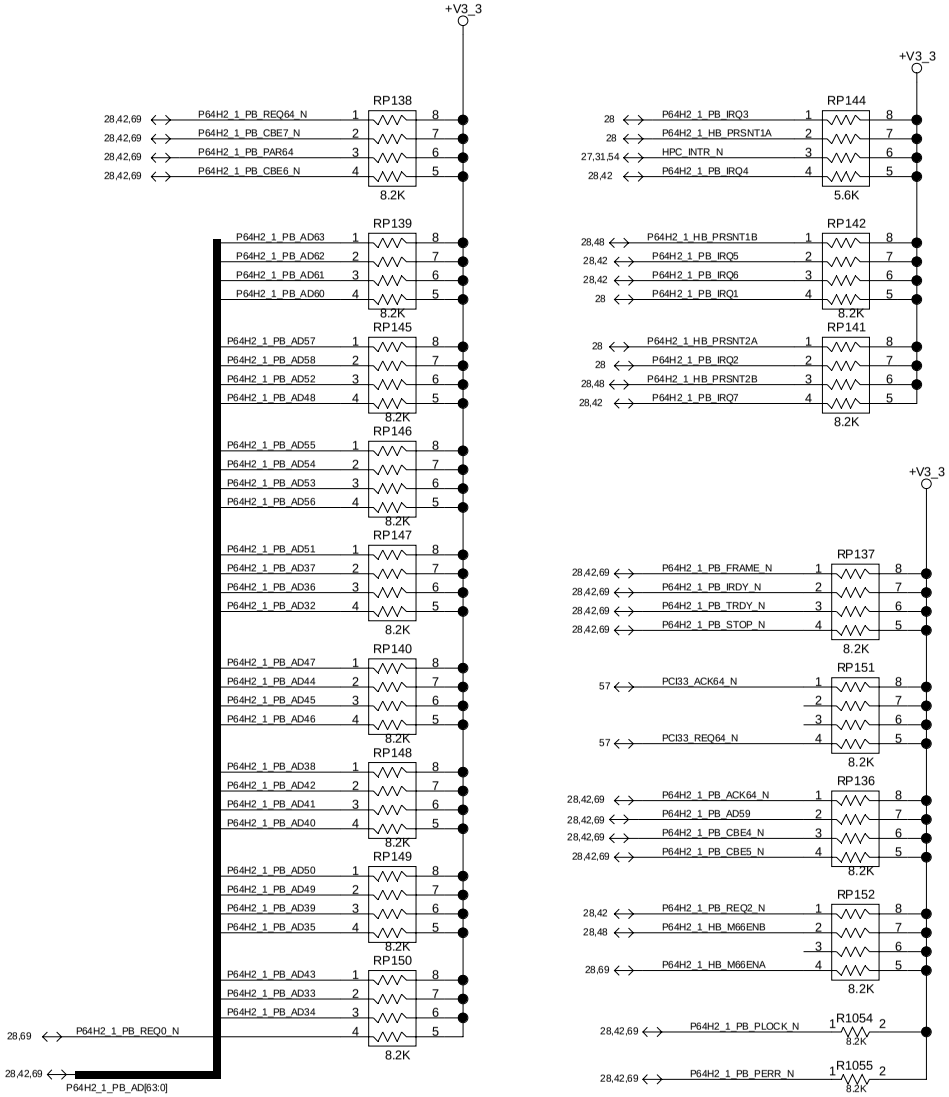


P64H2 #2 power, ground and decoupling

TITLE:		Rev: A2
intel EID Chandler, Arizona	DRAWN BY: TCL	PROJECT: MC
	LAST REVISED: 8/08/02	34 OF 83

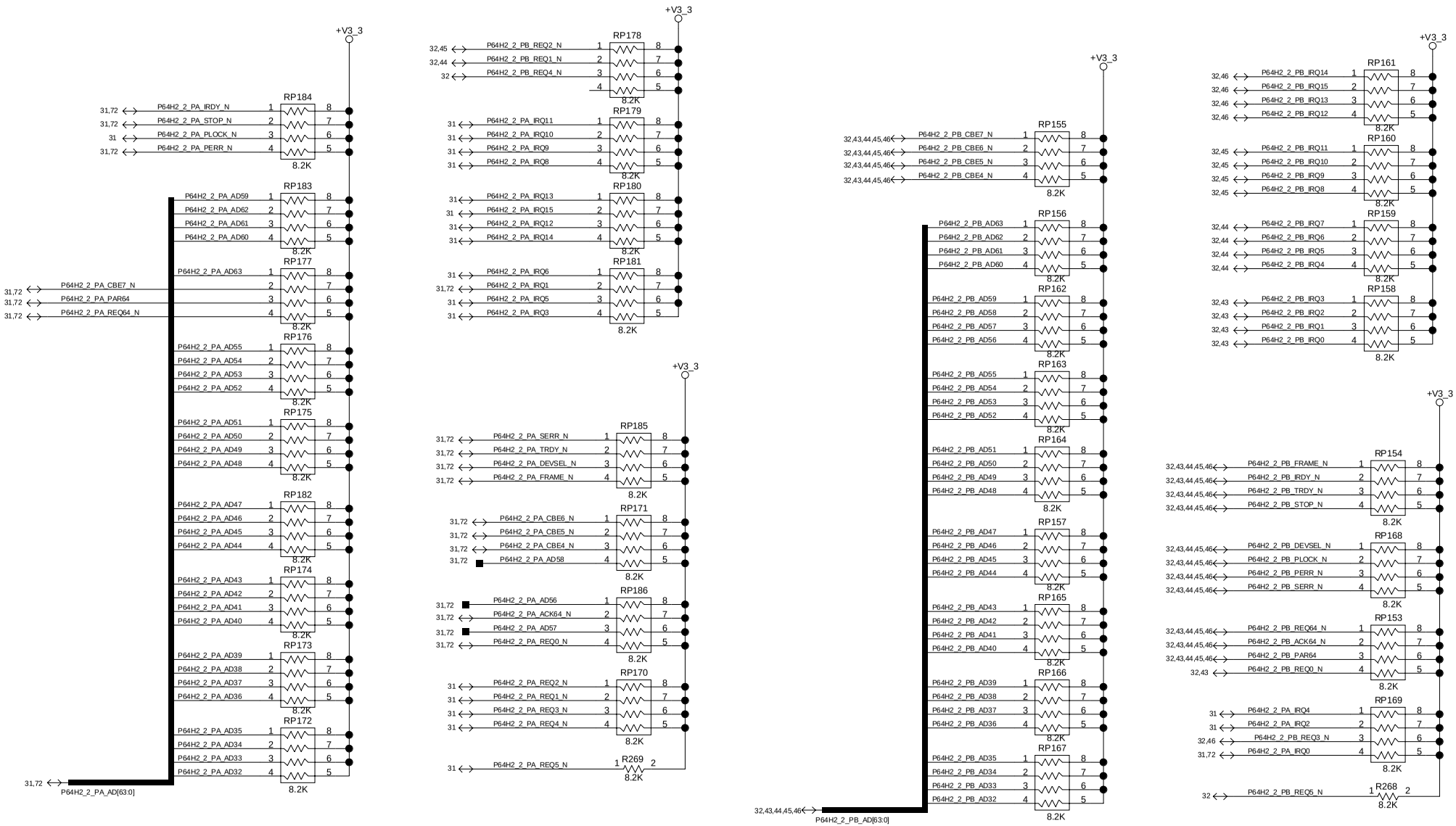


P64H2 #1 PCI Bus A pull-ups



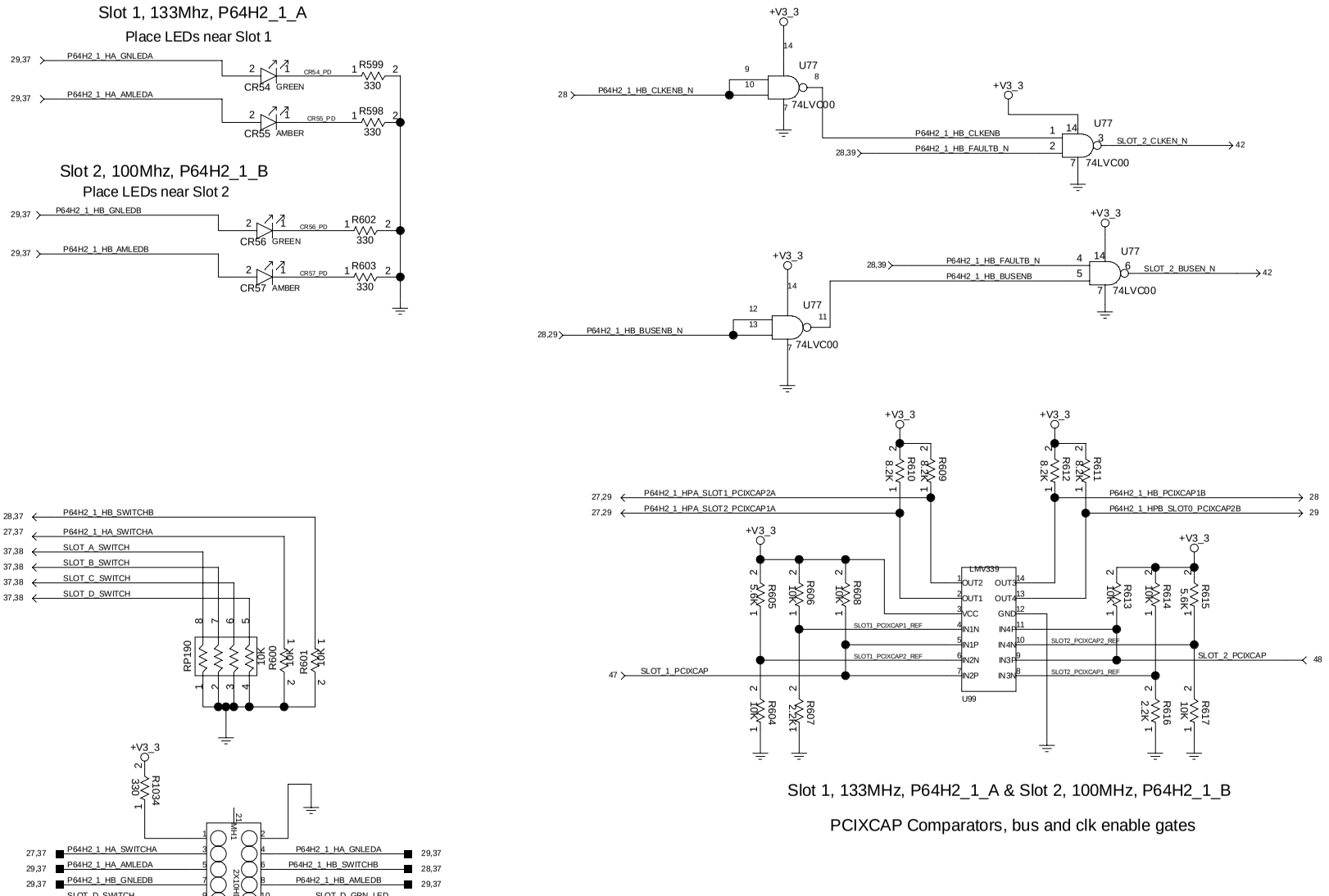
P64H2 #1 PCI Bus B pull-ups

TITLE:		Rev: A2
intel EID Chandler, Arizona	DRAWN BY: TCL	PROJECT: MC
	LAST REVISED: 8/08/02	35 OF 83



P64H2 #2 PCI pull-ups

TITLE:		Rev: A2
intel EID Chandler, Arizona	DRAWN BY: TCL	PROJECT: MC
	LAST REVISED: 8/08/02	36 OF 83



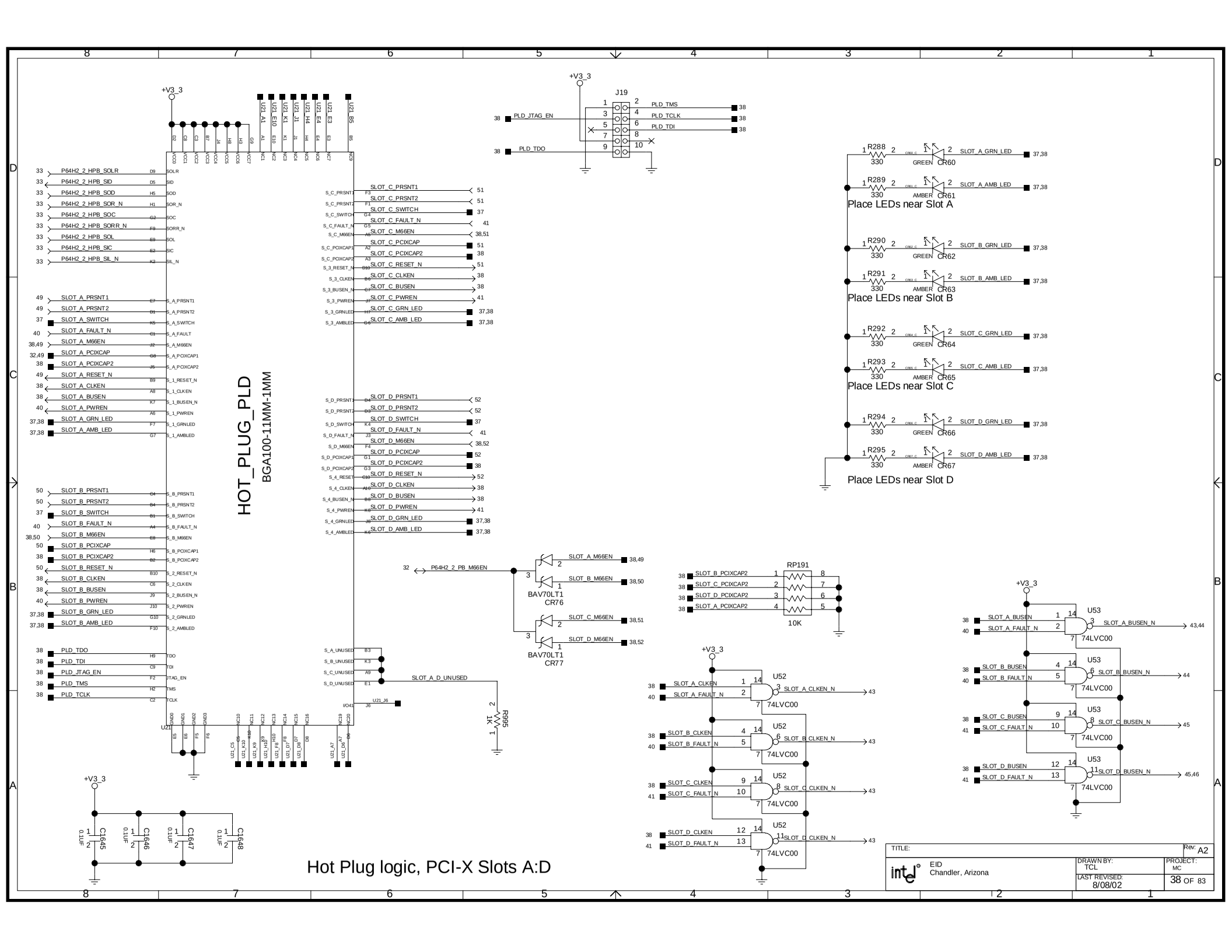
Slot 1, 133MHz, P64H2_1_A & Slot 2, 100MHz, P64H2_1_B

PCIXCAP Comparators, bus and clk enable gates

Chassis hot-plug switch board connector

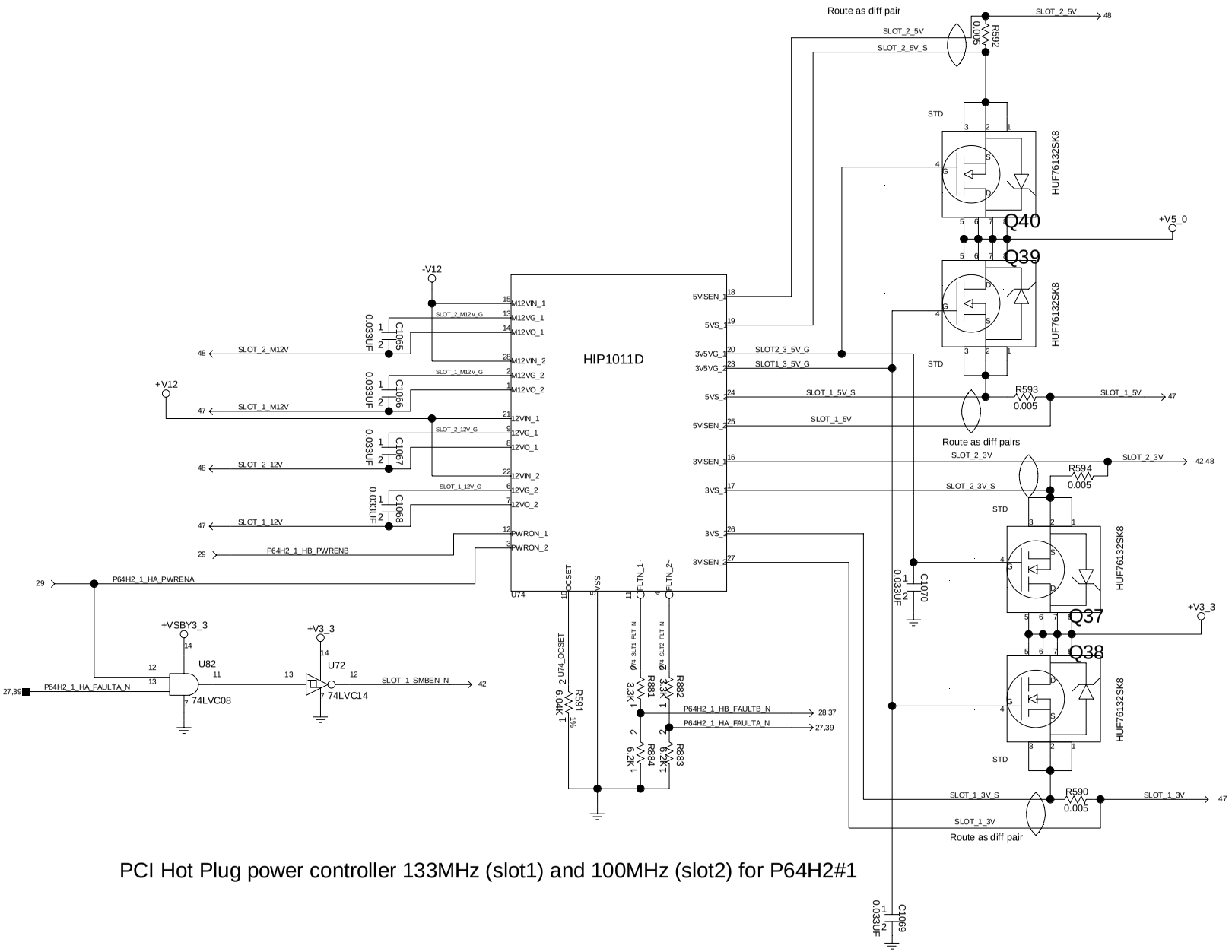
Hot Plug logic, PCI-X Slots 1,2

TITLE:			Rev: A2
intel EID Chandler, Arizona	DRAWN BY: TCL	PROJECT: MC	
	LAST REVISED: 8/08/02	37 OF 83	



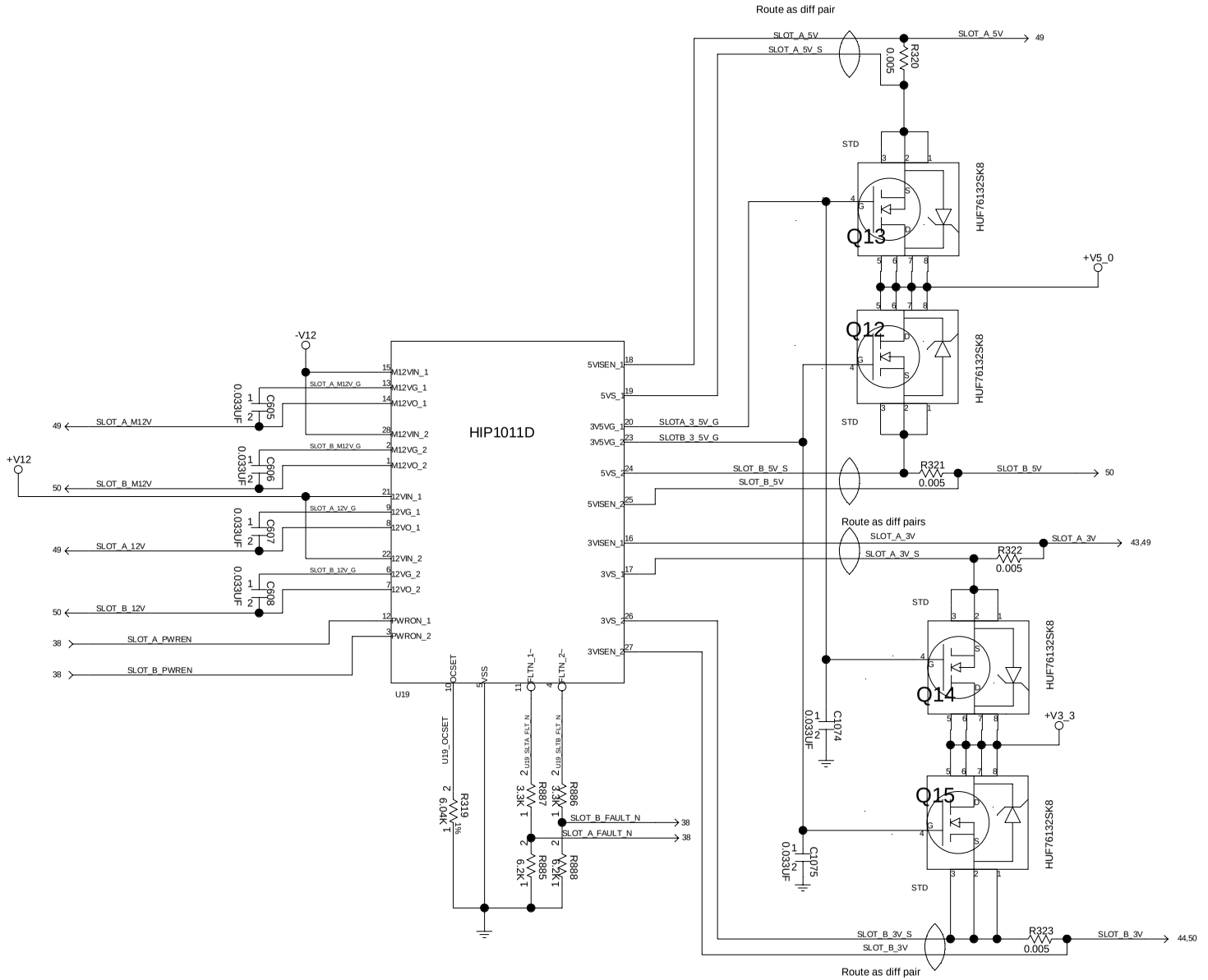
Hot Plug logic, PCI-X Slots A:D

TITLE:	Rev: A2
intel EID Chandler, Arizona	DRAWN BY: TCL
	PROJECT: MC
	LAST REVISED: 8/08/02
	38 OF 83



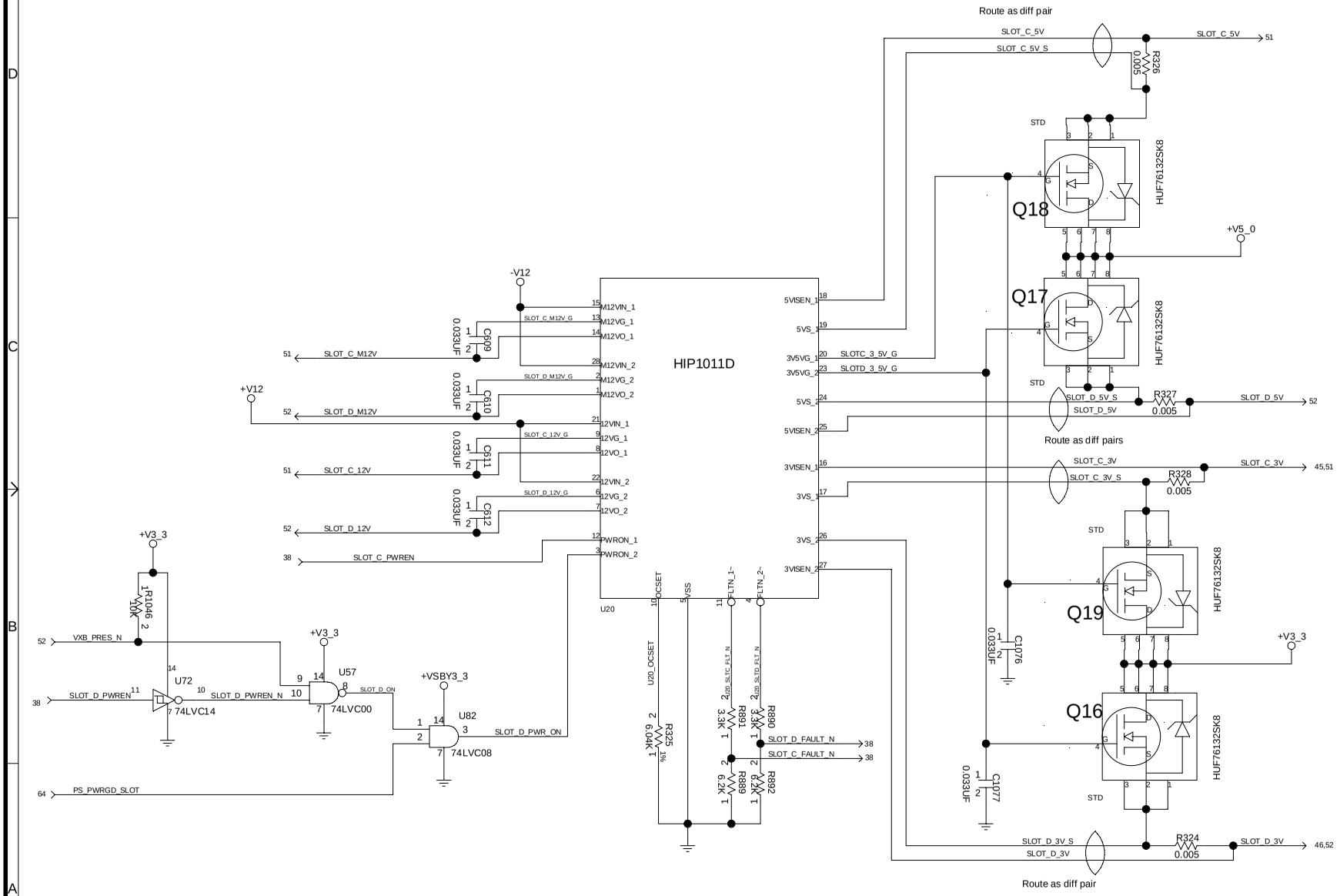
PCI Hot Plug power controller 133MHz (slot1) and 100MHz (slot2) for P64H2#1

TITLE:		Rev: A2
intel EID Chandler, Arizona	DRAWN BY: TCL	PROJECT: MC
	LAST REVISED: 8/08/02	39 OF 83



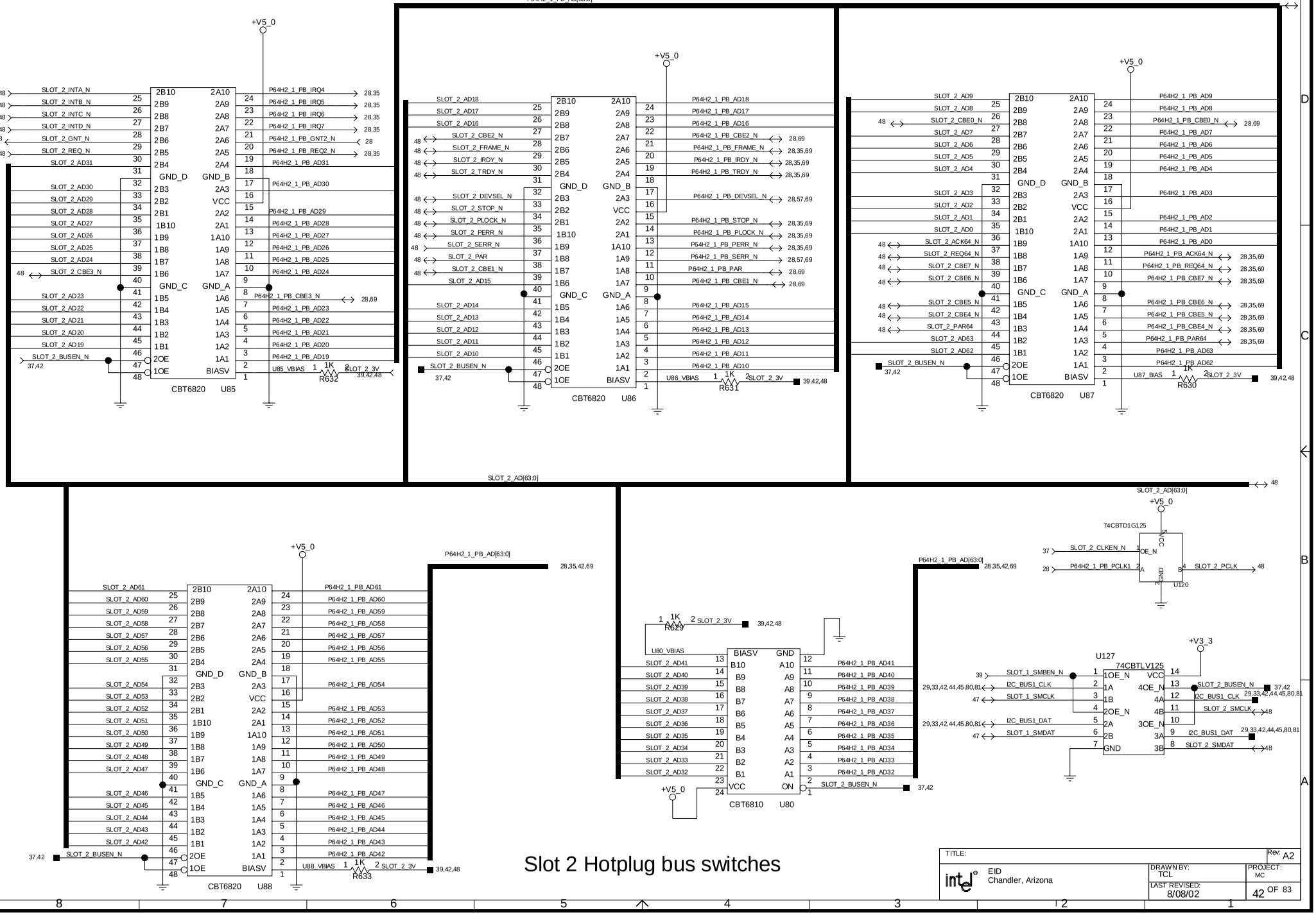
PCI Hot Plug power control. 66MHz Slots A and B

TITLE:			Rev: A2
intel EID Chandler, Arizona	DRAWN BY: TCL	PROJECT: MC	
	LAST REVISED: 8/08/02	40 OF 83	



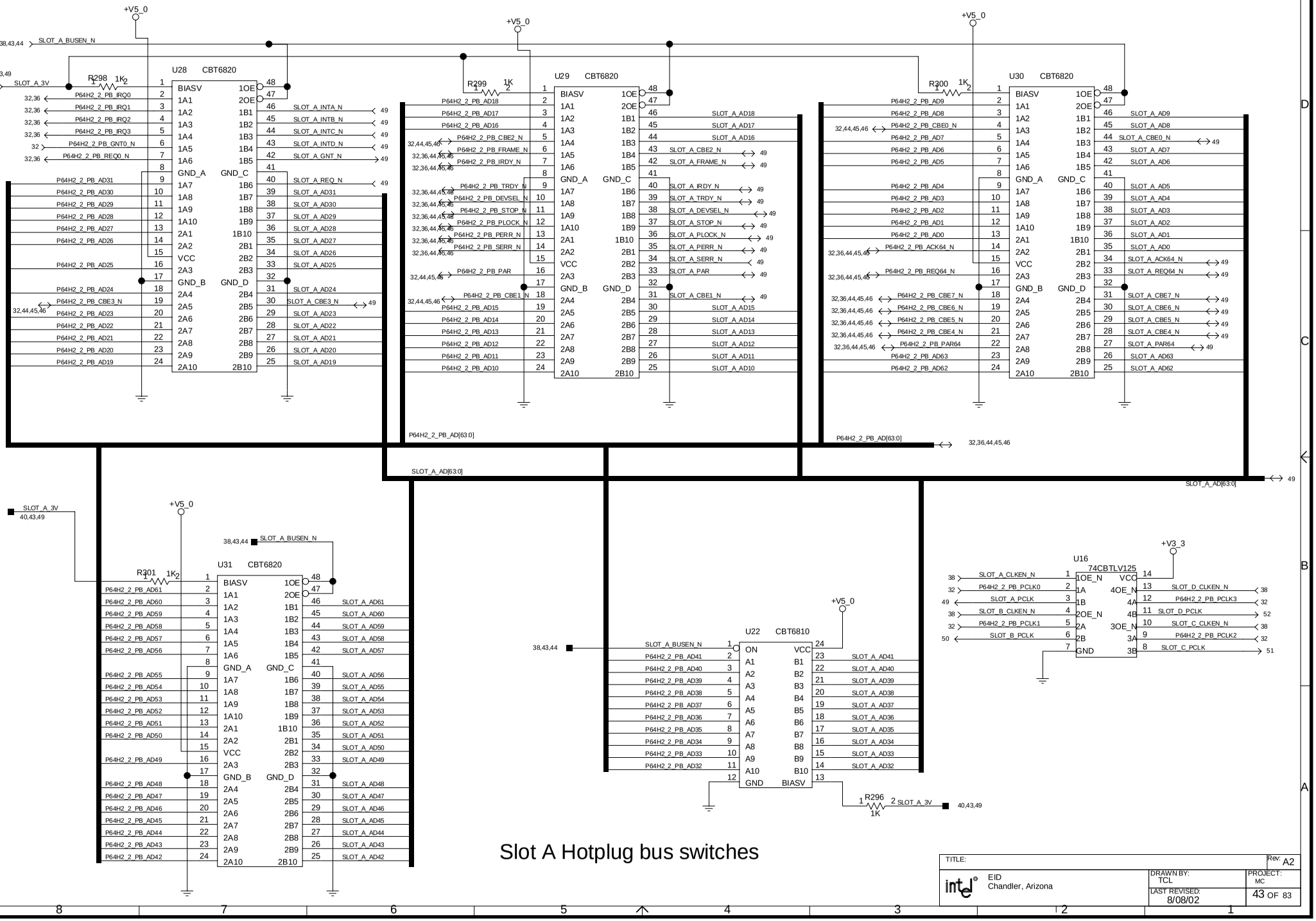
PCI Hot Plug power control. 66MHz Slots C and D

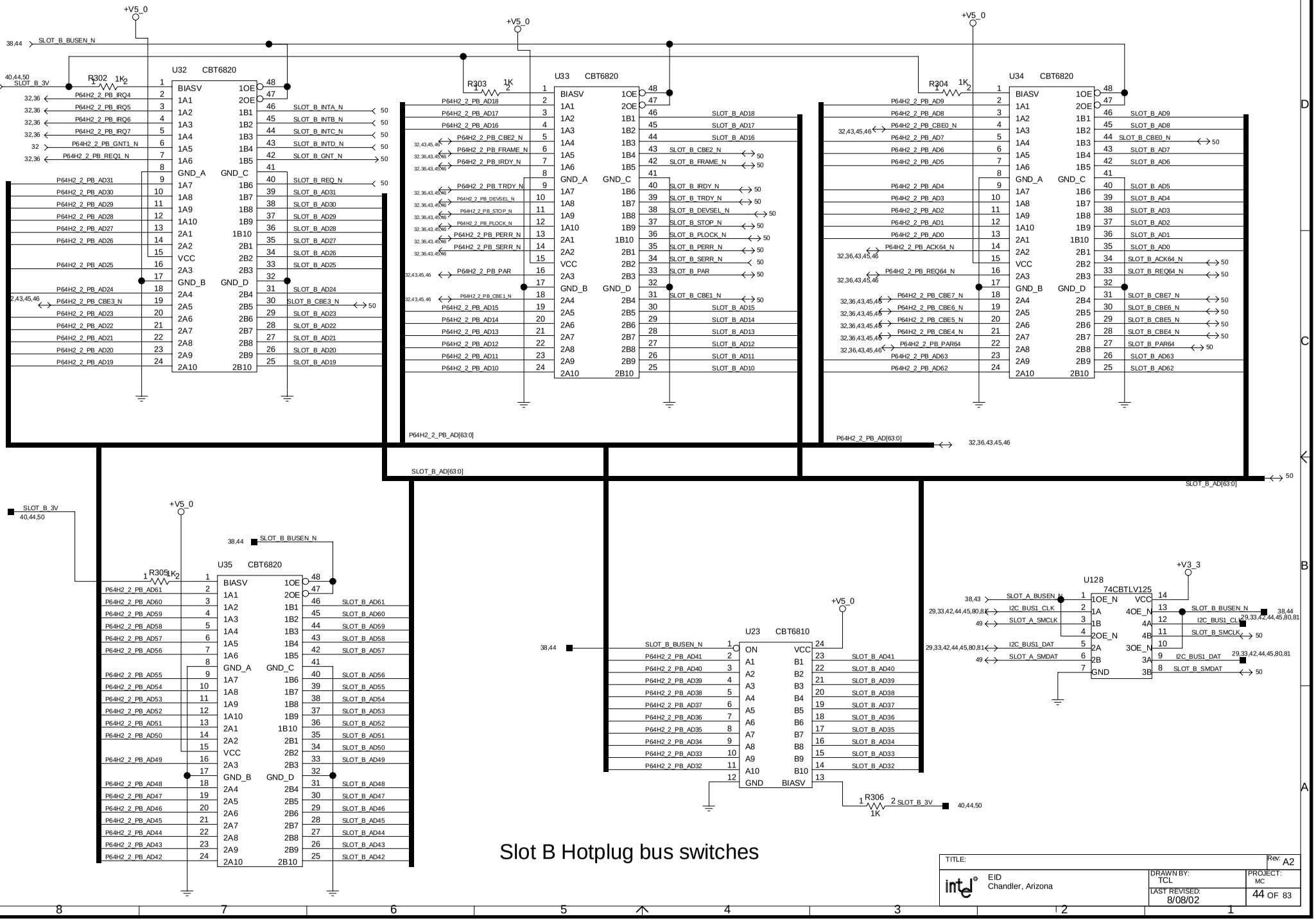
TITLE:		Rev: A2
intel EID Chandler, Arizona	DRAWN BY: TCL	PROJECT: MC
	LAST REVISED: 8/08/02	41 OF 83



Slot 2 Hotplug bus switches

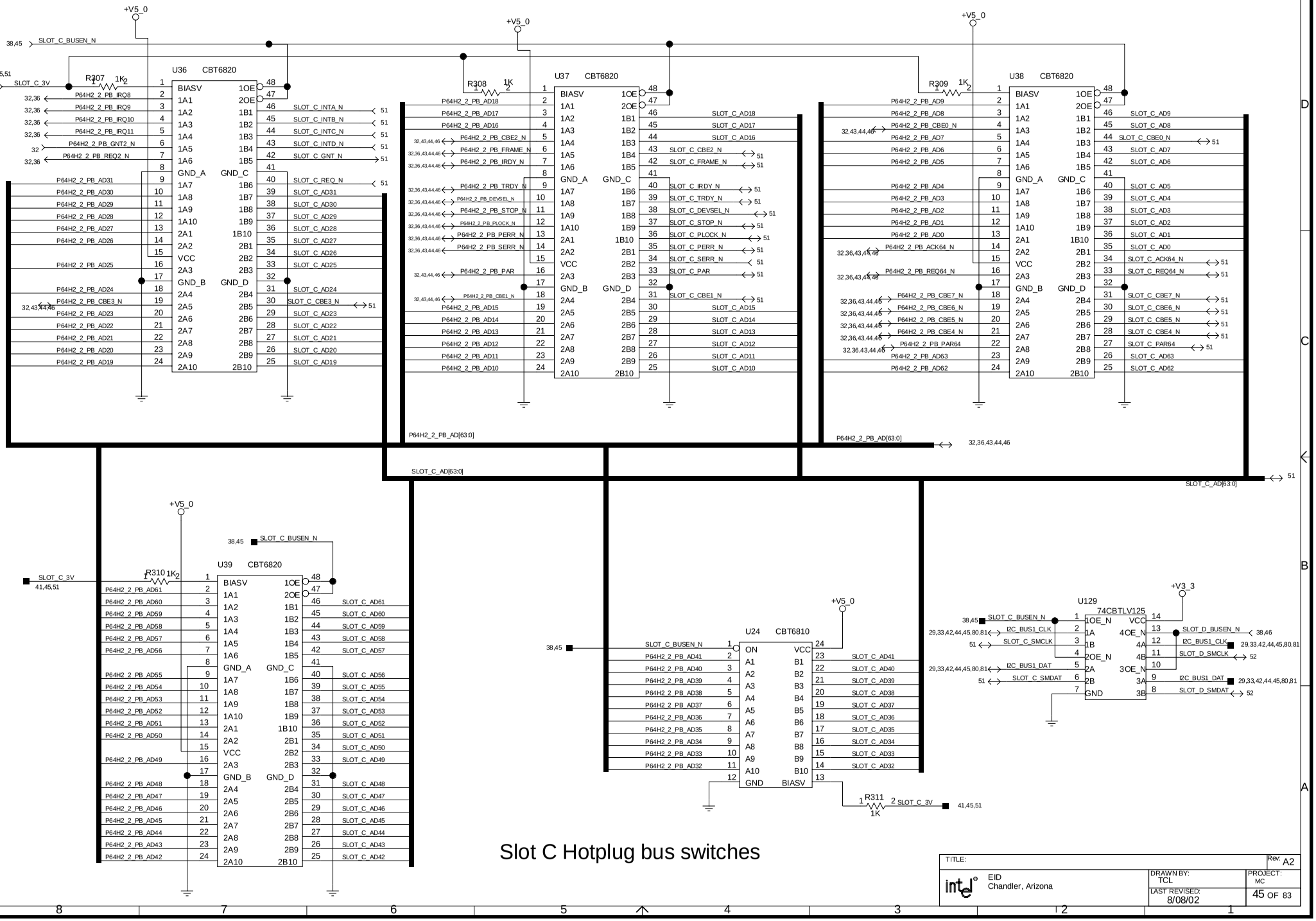
TITLE:		Rev: A2
intel EID Chandler, Arizona	DRAWN BY: TCL	PROJECT: MC
	LAST REVISED: 8/08/02	42 OF 83

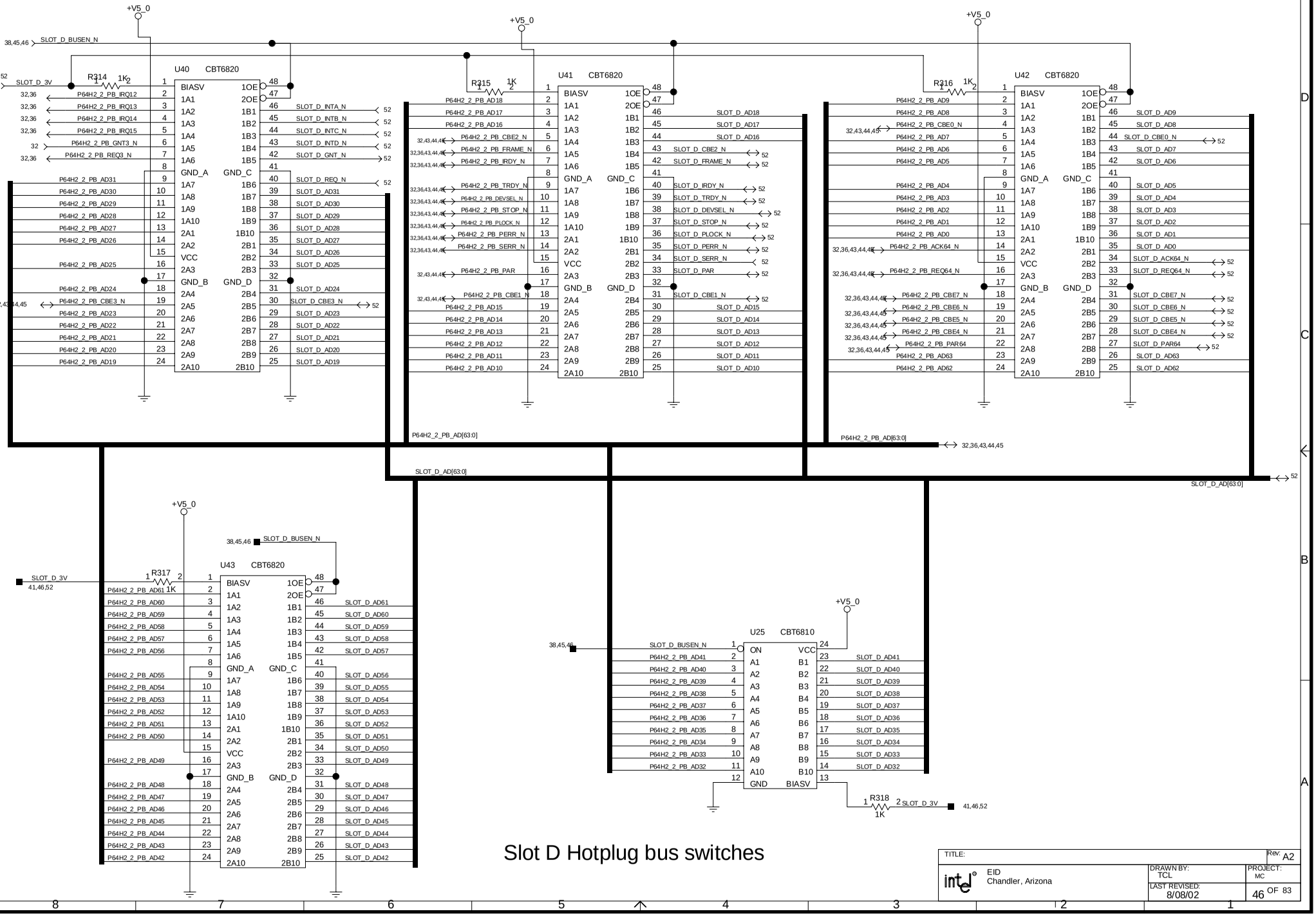

U28 CBT6820
U29 CBT6820
U30 CBT6820
U31 CBT6820
U22 CBT6810
U16 74CBTLV125
R298 1K
R299 1K
R300 1K
R301 1K
R296 1K
+V5_0
+V3_3
SLOT_A_BUSEN_N
SLOT_A_3V
P64H2_2_PB_AD[63:0]
SLOT_A_AD[63:0]
Slot A Hotplug bus switches
TITLE:
Rev: A2
EID
Chandler, Arizona
DRAWN BY: TCL
LAST REVISED: 8/08/02
PROJECT: MC
43 OF 83



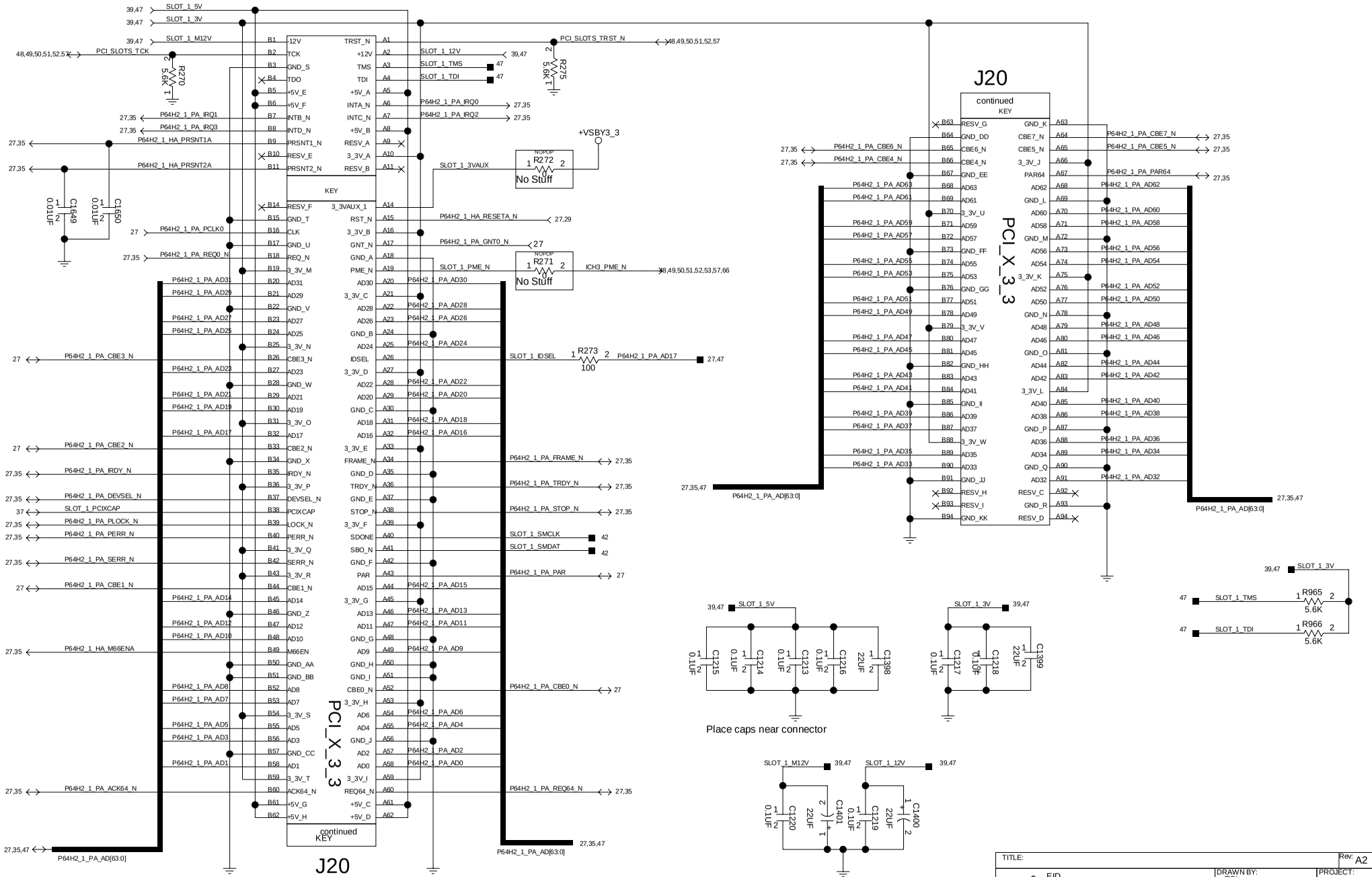
Slot B Hotplug bus switches

TITLE:	Rev: A2
intel EID Chandler, Arizona	DRAWN BY: TCL
	PROJECT: MC
	LAST REVISED: 8/08/02
	44 OF 83


U36 CBT6820
U37 CBT6820
U38 CBT6820
U39 CBT6820
U24 CBT6810
U129 74CBTLV125
R307 1K
R308 1K
R309 1K
R310 1K
R311 1K
+V5_0
+V3_3
SLOT_C_BUSEN_N
SLOT_C_3V
P64H2_2_PB_AD[63:0]
SLOT_C_AD[63:0]
Slot C Hotplug bus switches
TITLE:
Rev: A2
EID
Chandler, Arizona
DRAWN BY: TCL
LAST REVISED: 8/08/02
PROJECT: MC
45 OF 83

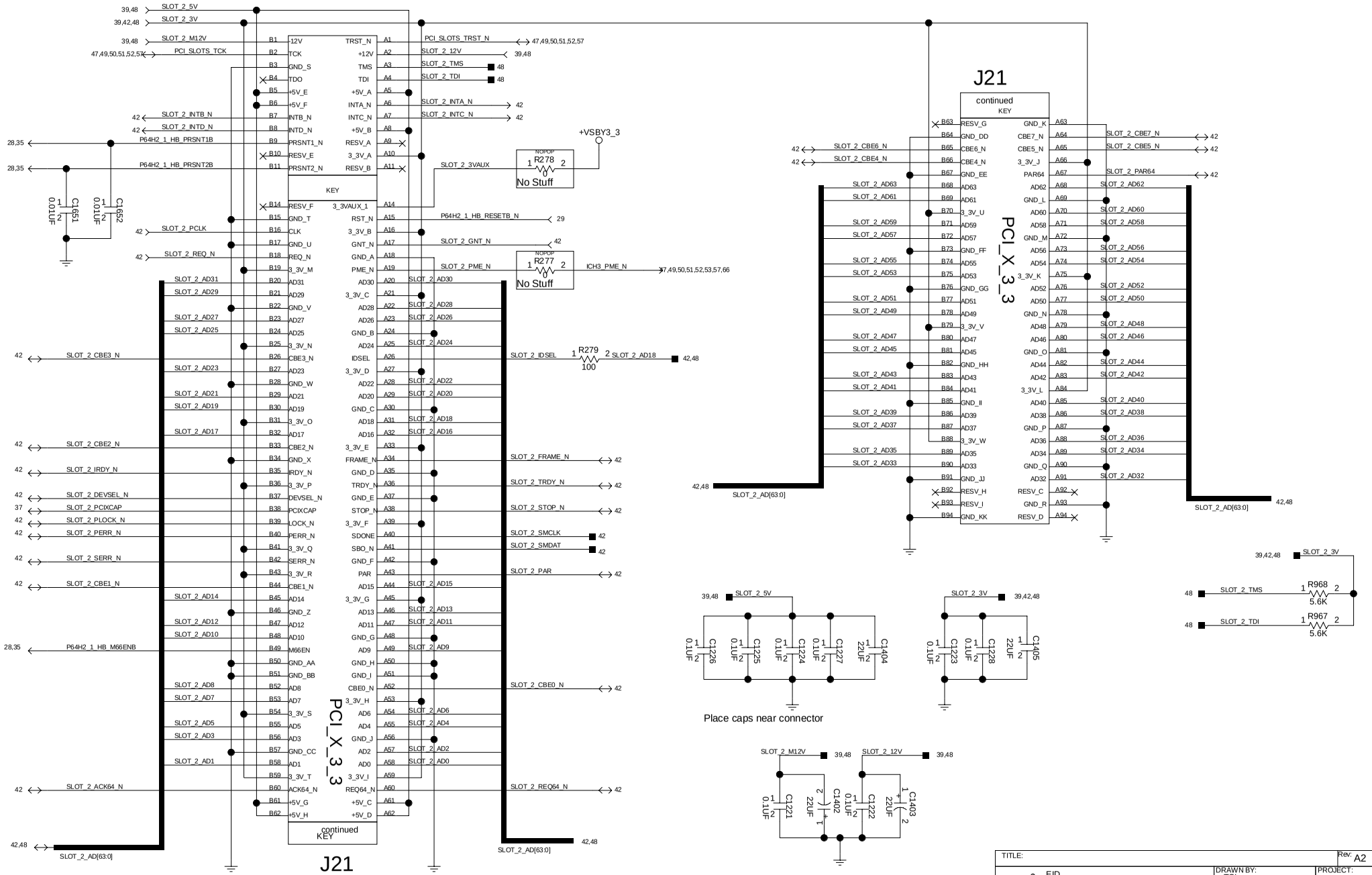

+V5_0
38,45,46 SLOT_D_BUSEN_N
41,46,52 SLOT_D_3V
R314 1K
U40 CBT6820
BIASV 1OE
1A1 2OE
1A2 1B1
1A3 1B2
1A4 1B3
1A5 1B4
1A6 1B5
GND_A GND_C
1A7 1B6
1A8 1B7
1A9 1B8
1A10 1B9
2A1 1B10
2A2 2B1
VCC 2B2
2A3 2B3
GND_B GND_D
2A4 2B4
2A5 2B5
2A6 2B6
2A7 2B7
2A8 2B8
2A9 2B9
2A10 2B10
32,36 P64H2_2_PB_IRQ12
32,36 P64H2_2_PB_IRQ13
32,36 P64H2_2_PB_IRQ14
32,36 P64H2_2_PB_IRQ15
32 P64H2_2_PB_GNT3_N
32,36 P64H2_2_PB_REQ3_N
SLOT_D_INTA_N
SLOT_D_INTB_N
SLOT_D_INTC_N
SLOT_D_INTD_N
SLOT_D_GNT_N
SLOT_D_REQ_N
SLOT_D_AD31
SLOT_D_AD30
SLOT_D_AD29
SLOT_D_AD28
SLOT_D_AD27
SLOT_D_AD26
SLOT_D_AD25
SLOT_D_AD24
SLOT_D_CBE3_N
SLOT_D_AD23
SLOT_D_AD22
SLOT_D_AD21
SLOT_D_AD20
SLOT_D_AD19
P64H2_2_PB_AD31
P64H2_2_PB_AD30
P64H2_2_PB_AD29
P64H2_2_PB_AD28
P64H2_2_PB_AD27
P64H2_2_PB_AD26
P64H2_2_PB_AD25
P64H2_2_PB_AD24
32,43,44,45 P64H2_2_PB_CBE3_N
P64H2_2_PB_AD23
P64H2_2_PB_AD22
P64H2_2_PB_AD21
P64H2_2_PB_AD20
P64H2_2_PB_AD19
R315 1K
U41 CBT6820
P64H2_2_PB_AD18
P64H2_2_PB_AD17
P64H2_2_PB_AD16
32,43,44,45 P64H2_2_PB_CBE2_N
32,36,43,44,45 P64H2_2_PB_FRAME_N
32,36,43,44,45 P64H2_2_PB_IRDY_N
32,36,43,44,45 P64H2_2_PB_TRDY_N
32,36,43,44,45 P64H2_2_PB_DEVSEL_N
32,36,43,44,45 P64H2_2_PB_STOP_N
32,36,43,44,45 P64H2_2_PB_PLOCK_N
32,36,43,44,45 P64H2_2_PB_PERR_N
32,36,43,44,45 P64H2_2_PB_SERR_N
32,43,44,45 P64H2_2_PB_PAR
32,43,44,45 P64H2_2_PB_CBE1_N
P64H2_2_PB_AD15
P64H2_2_PB_AD14
P64H2_2_PB_AD13
P64H2_2_PB_AD12
P64H2_2_PB_AD11
P64H2_2_PB_AD10
SLOT_D_AD18
SLOT_D_AD17
SLOT_D_AD16
SLOT_D_CBE2_N
SLOT_D_FRAME_N
SLOT_D_IRDY_N
SLOT_D_TRDY_N
SLOT_D_DEVSEL_N
SLOT_D_STOP_N
SLOT_D_PLOCK_N
SLOT_D_PERR_N
SLOT_D_SERR_N
SLOT_D_PAR
SLOT_D_CBE1_N
SLOT_D_AD15
SLOT_D_AD14
SLOT_D_AD13
SLOT_D_AD12
SLOT_D_AD11
SLOT_D_AD10
P64H2_2_PB_AD[63:0]
R316 1K
U42 CBT6820
P64H2_2_PB_AD9
P64H2_2_PB_AD8
32,43,44,45 P64H2_2_PB_CBE0_N
P64H2_2_PB_AD7
P64H2_2_PB_AD6
P64H2_2_PB_AD5
P64H2_2_PB_AD4
P64H2_2_PB_AD3
P64H2_2_PB_AD2
P64H2_2_PB_AD1
P64H2_2_PB_AD0
32,36,43,44,45 P64H2_2_PB_ACK64_N
32,36,43,44,45 P64H2_2_PB_REQ64_N
32,36,43,44,45 P64H2_2_PB_CBE7_N
32,36,43,44,45 P64H2_2_PB_CBE6_N
32,36,43,44,45 P64H2_2_PB_CBE5_N
32,36,43,44,45 P64H2_2_PB_CBE4_N
32,36,43,44,45 P64H2_2_PB_PAR64
P64H2_2_PB_AD63
P64H2_2_PB_AD62
SLOT_D_AD9
SLOT_D_AD8
SLOT_D_CBE0_N
SLOT_D_AD7
SLOT_D_AD6
SLOT_D_AD5
SLOT_D_AD4
SLOT_D_AD3
SLOT_D_AD2
SLOT_D_AD1
SLOT_D_AD0
SLOT_D_ACK64_N
SLOT_D_REQ64_N
SLOT_D_CBE7_N
SLOT_D_CBE6_N
SLOT_D_CBE5_N
SLOT_D_CBE4_N
SLOT_D_PAR64
SLOT_D_AD63
SLOT_D_AD62
P64H2_2_PB_AD[63:0]
32,36,43,44,45
SLOT_D_AD[63:0]
52
R317 1K
U43 CBT6820
P64H2_2_PB_AD61
P64H2_2_PB_AD60
P64H2_2_PB_AD59
P64H2_2_PB_AD58
P64H2_2_PB_AD57
P64H2_2_PB_AD56
P64H2_2_PB_AD55
P64H2_2_PB_AD54
P64H2_2_PB_AD53
P64H2_2_PB_AD52
P64H2_2_PB_AD51
P64H2_2_PB_AD50
P64H2_2_PB_AD49
P64H2_2_PB_AD48
P64H2_2_PB_AD47
P64H2_2_PB_AD46
P64H2_2_PB_AD45
P64H2_2_PB_AD44
P64H2_2_PB_AD43
P64H2_2_PB_AD42
SLOT_D_AD61
SLOT_D_AD60
SLOT_D_AD59
SLOT_D_AD58
SLOT_D_AD57
SLOT_D_AD56
SLOT_D_AD55
SLOT_D_AD54
SLOT_D_AD53
SLOT_D_AD52
SLOT_D_AD51
SLOT_D_AD50
SLOT_D_AD49
SLOT_D_AD48
SLOT_D_AD47
SLOT_D_AD46
SLOT_D_AD45
SLOT_D_AD44
SLOT_D_AD43
SLOT_D_AD42
U25 CBT6810
ON VCC
A1 B1
A2 B2
A3 B3
A4 B4
A5 B5
A6 B6
A7 B7
A8 B8
A9 B9
A10 B10
GND BIASV
P64H2_2_PB_AD41
P64H2_2_PB_AD40
P64H2_2_PB_AD39
P64H2_2_PB_AD38
P64H2_2_PB_AD37
P64H2_2_PB_AD36
P64H2_2_PB_AD35
P64H2_2_PB_AD34
P64H2_2_PB_AD33
P64H2_2_PB_AD32
SLOT_D_AD41
SLOT_D_AD40
SLOT_D_AD39
SLOT_D_AD38
SLOT_D_AD37
SLOT_D_AD36
SLOT_D_AD35
SLOT_D_AD34
SLOT_D_AD33
SLOT_D_AD32
R318 1K
SLOT_D_3V
41,46,52
Slot D Hotplug bus switches
TITLE:
Rev: A2
intel
EID
Chandler, Arizona
DRAWN BY: TCL
PROJECT: MC
LAST REVISED: 8/08/02
46 OF 83

PCI-X Slot 1 (P64H2 #1, PCI Bus A)



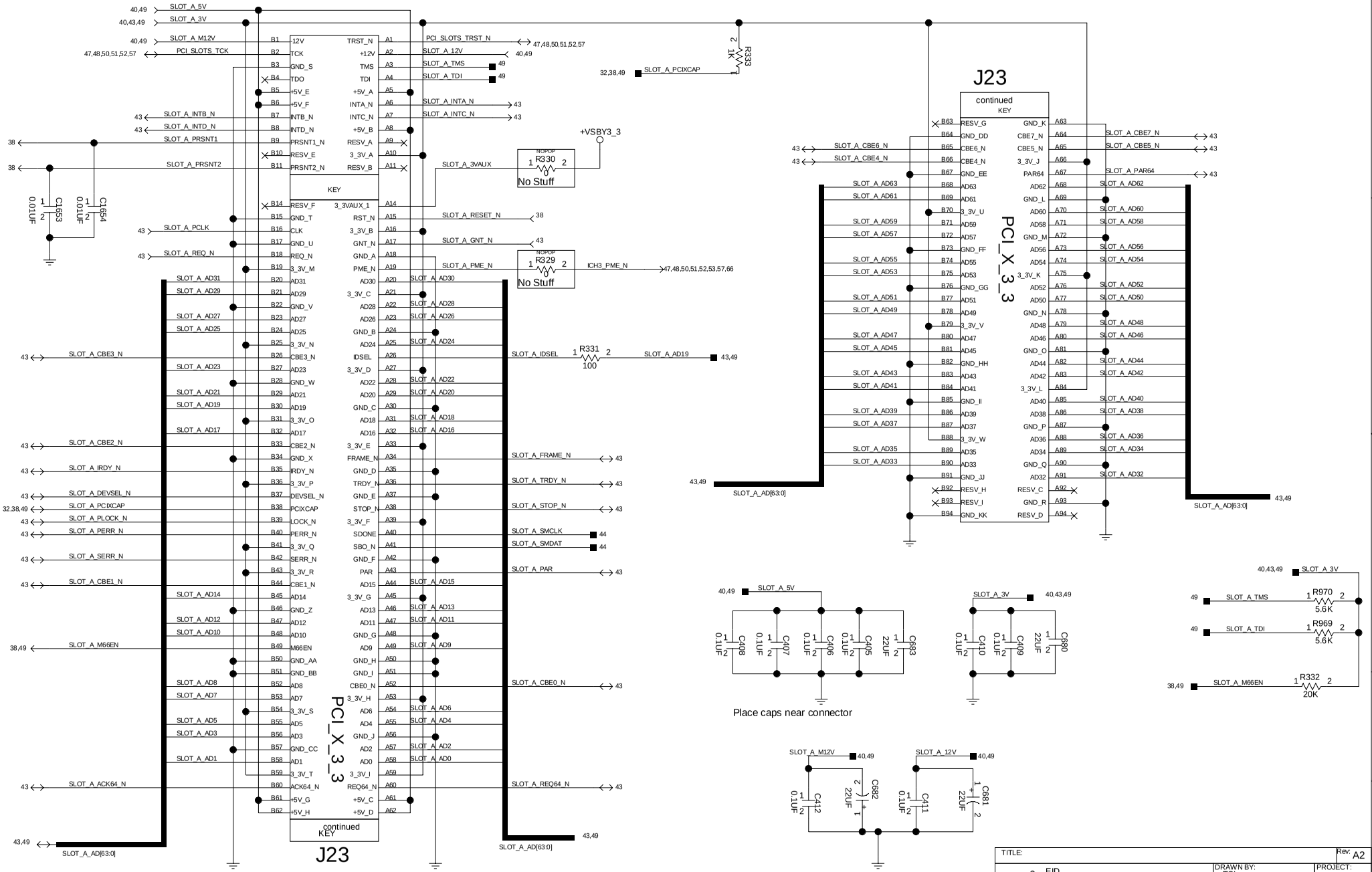
TITLE:	Rev: A2
intel EID Chandler, Arizona	DRAWN BY: TCL
	PROJECT: MC
	LAST REVISED: 8/08/02
	47 OF 83

PCI-X Slot 2 (P64H2 #1, PCI Bus B)



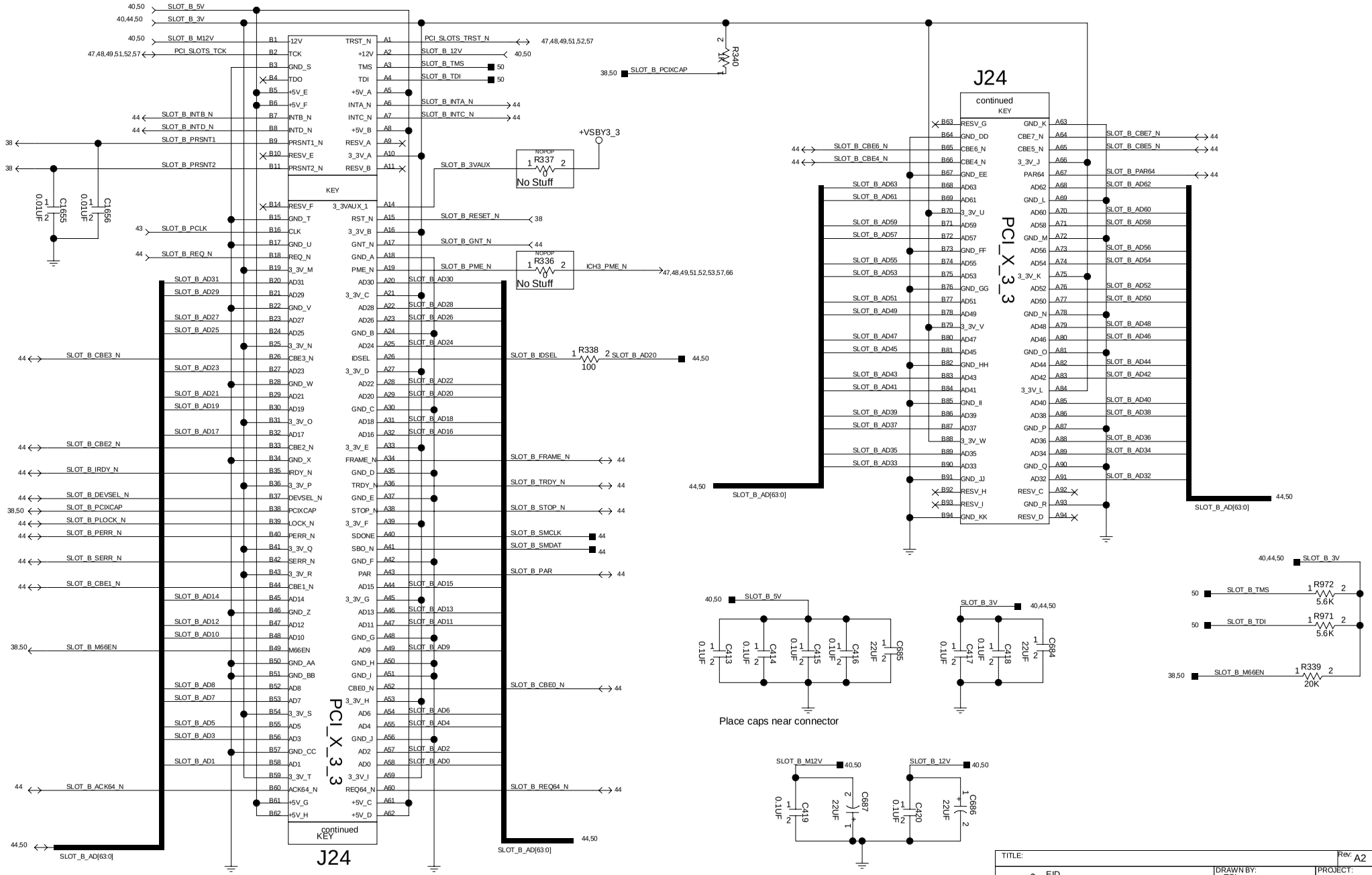
TITLE:	Rev: A2
EID Chandler, Arizona	DRAWN BY: TCL PROJECT: MC LAST REVISED: 8/08/02 48 OF 83

PCI-X 66MHz SLOT A



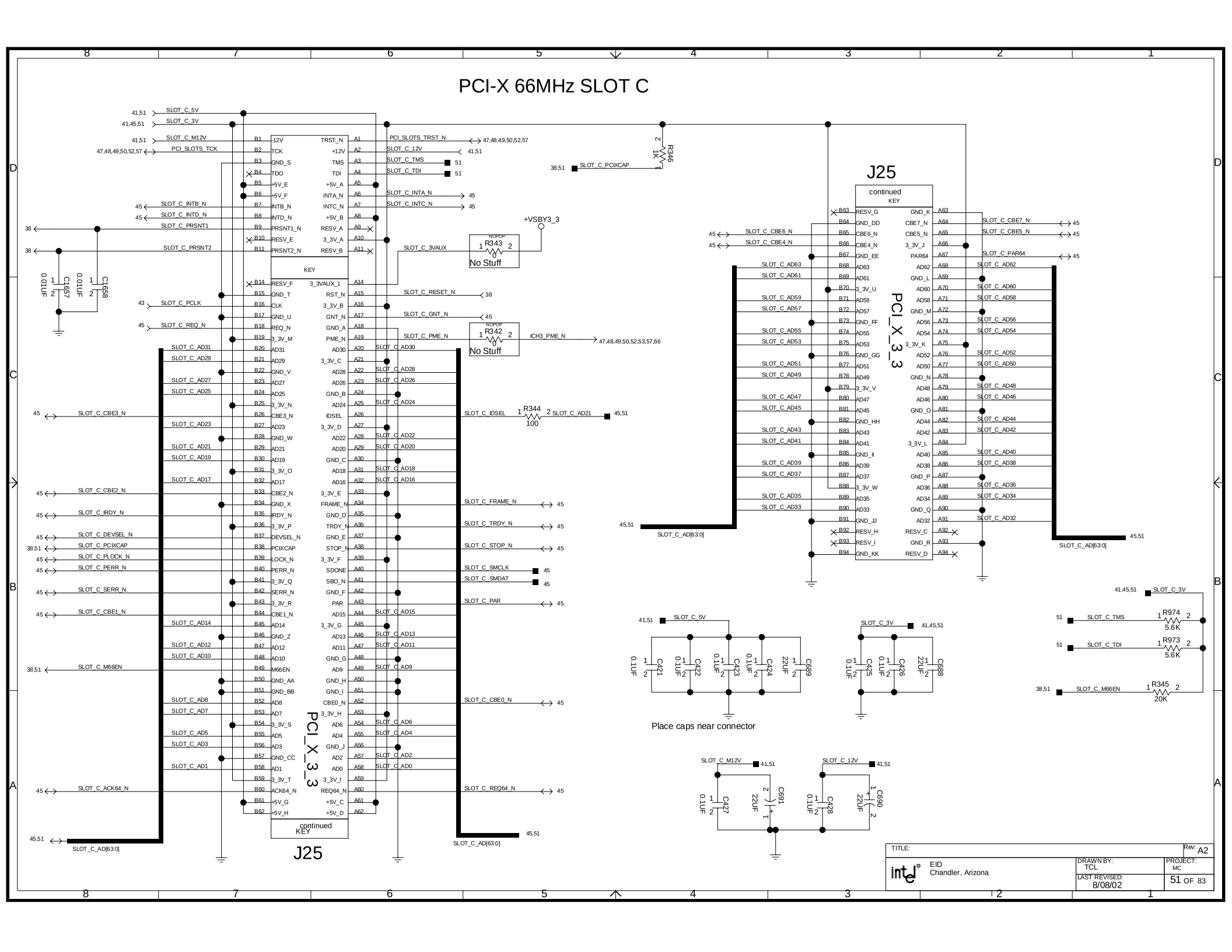
TITLE:		Rev: A2
intel EID Chandler, Arizona	DRAWN BY: TCL	PROJECT: MC
	LAST REVISED: 8/08/02	49 OF 83

PCI-X 66MHz SLOT B



TITLE:	Rev: A2
EID Chandler, Arizona	DRAWN BY: TCL
	PROJECT: MC
	LAST REVISED: 8/08/02
	50 OF 83

PCI-X 66MHz SLOT C



TITLE:

Rev: A2

intel EID Chandler, Arizona

DRAWN BY: TCL

PROJECT: MC

LAST REVISED: 8/08/02

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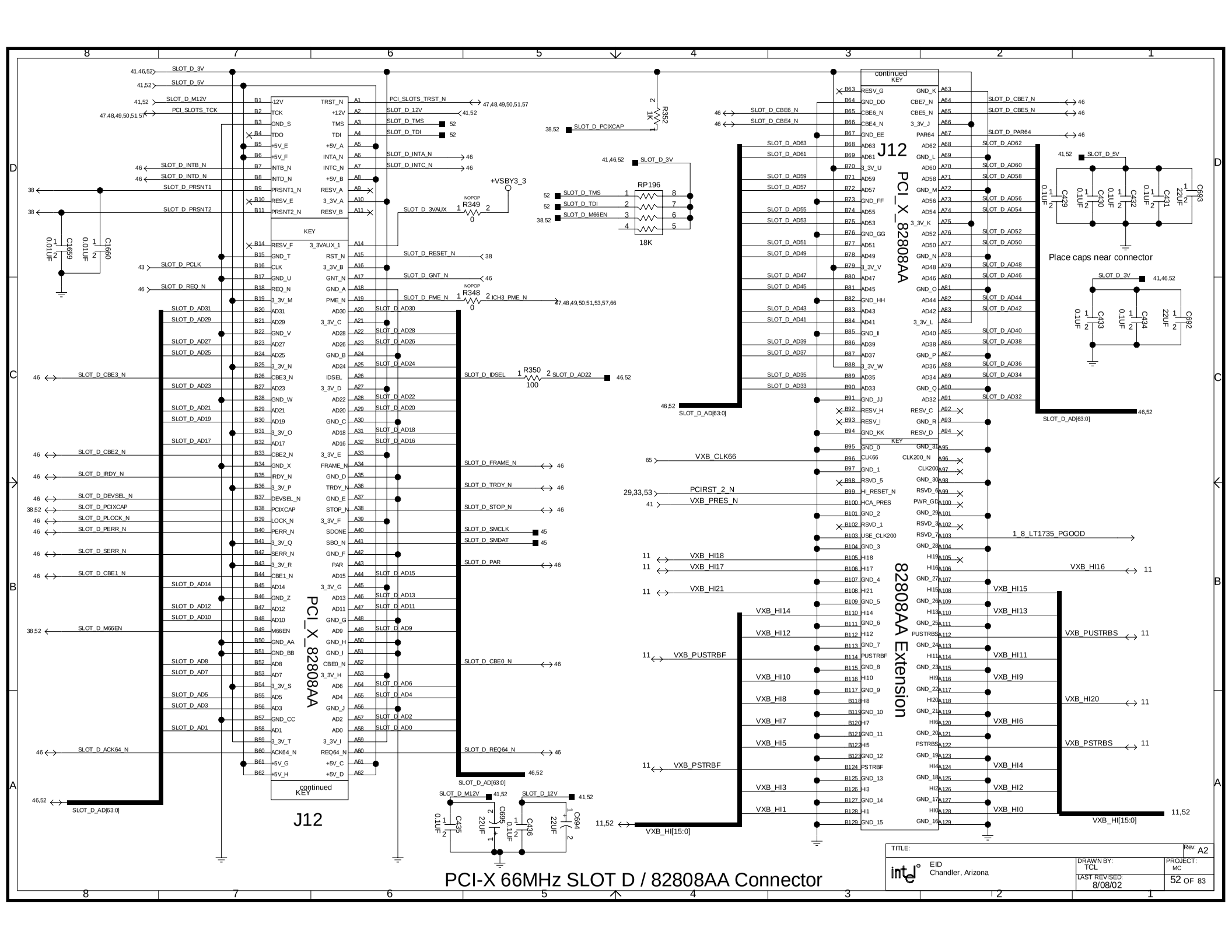
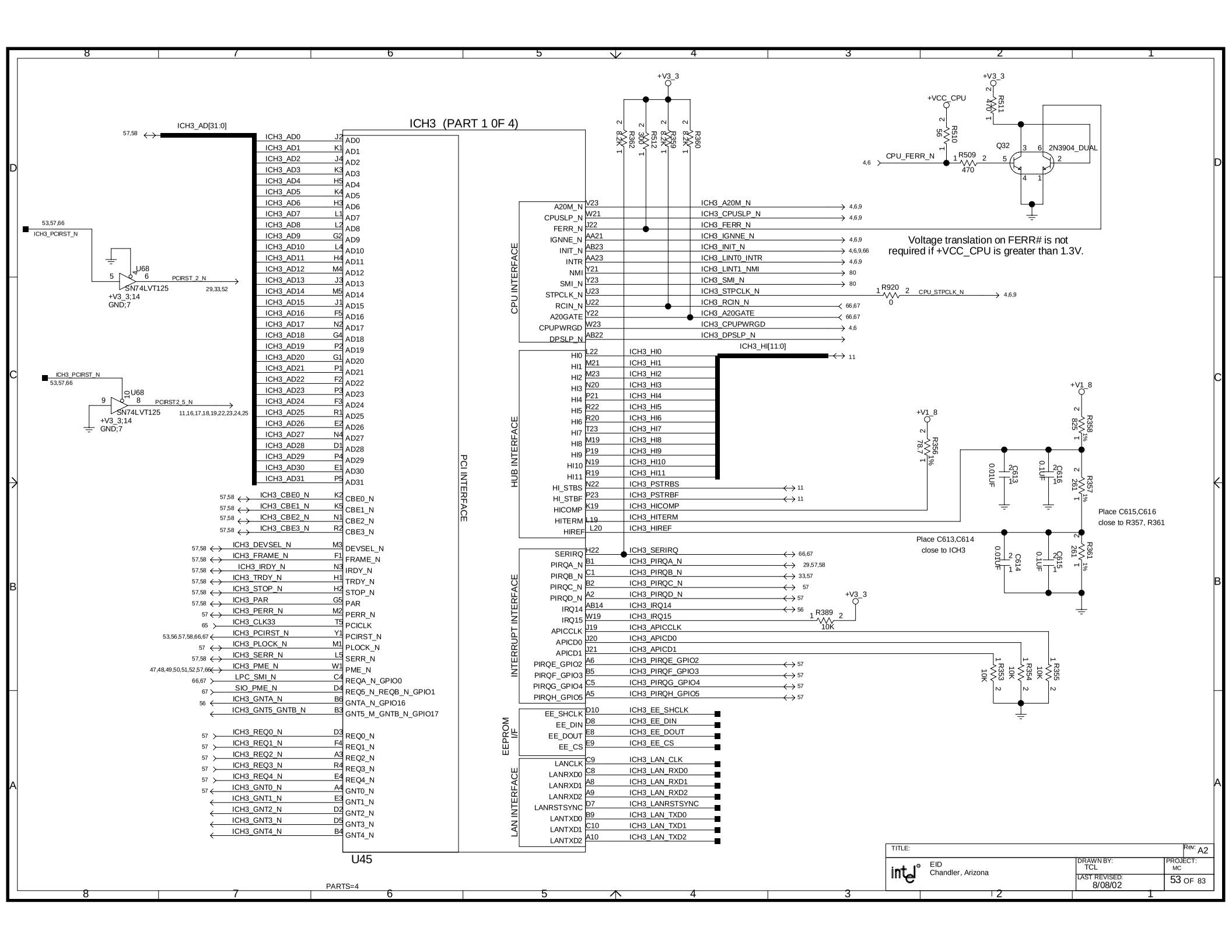
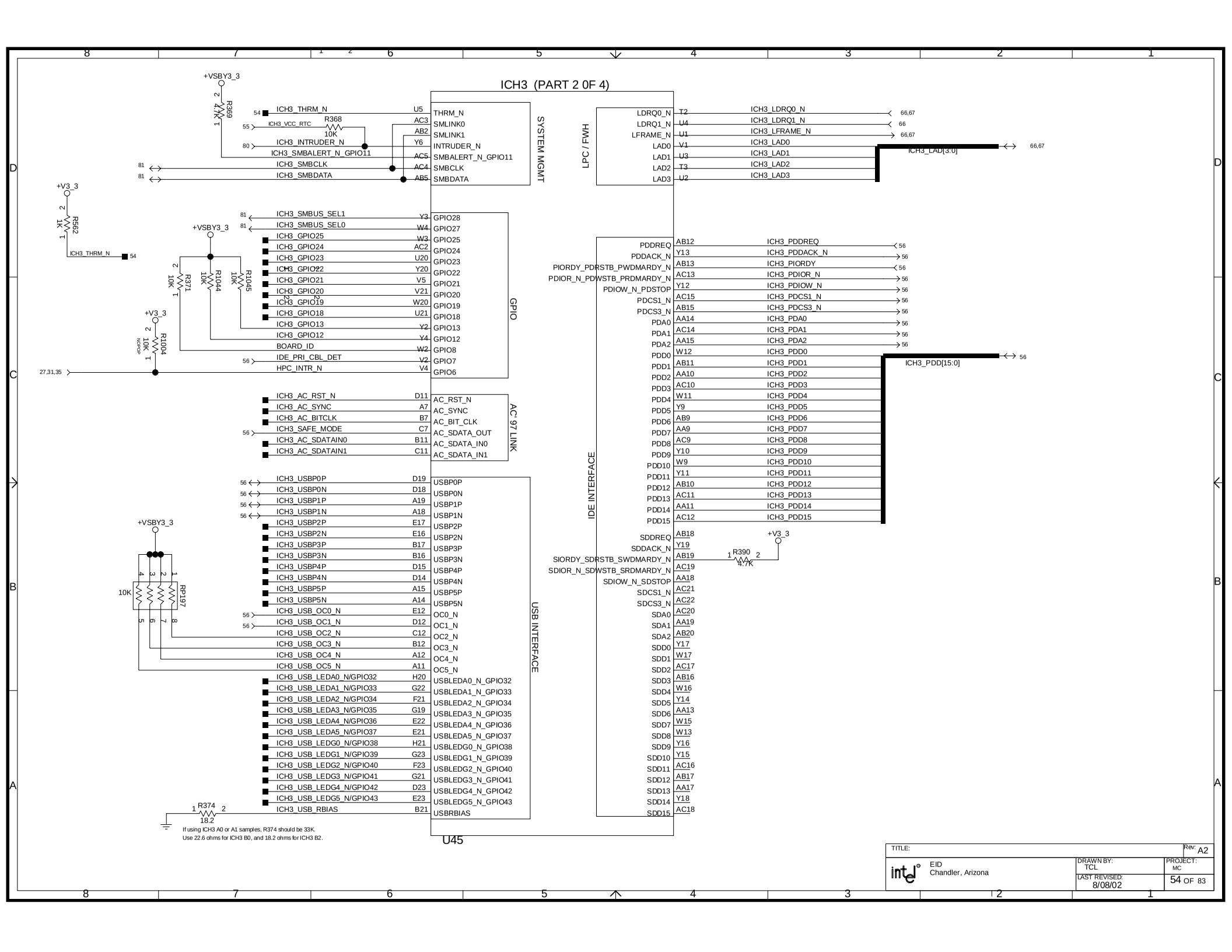

PCI-X 66MHz SLOT D / 82808AA Connector
PCI_X_82808AA
82808AA Extension
J12
KEY
continued
Place caps near connector
SLOT_D_AD[63:0]
VXB_HI[15:0]
TITLE:
Rev: A2
EID
Chandler, Arizona
DRAWN BY: TCL
PROJECT: MC
LAST REVISED: 8/08/02
52 OF 83


ICH3 (PART 1 0F 4)
U45
PCI INTERFACE
CPU INTERFACE
HUB INTERFACE
INTERRUPT INTERFACE
EEPROM I/F
LAN INTERFACE
ICH3_AD[31:0]
ICH3_HI[11:0]
Voltage translation on FERR# is not required if +VCC_CPU is greater than 1.3V.
Place C615,C616 close to R357, R361
Place C613,C614 close to ICH3
SN74LVT125
2N3904_DUAL
PARTS=4
TITLE:
Rev: A2
EID
Chandler, Arizona
DRAWN BY: TCL
PROJECT: MC
LAST REVISED: 8/08/02
53 OF 83


ICH3 (PART 2 0F 4)
SYSTEM MGMT
GPIO
AC' 97 LINK
USB INTERFACE
LPC / FWH
IDE INTERFACE
U45
THRM_N
SMLINK0
SMLINK1
INTRUDER_N
SMBALERT_N_GPIO11
SMBCLK
SMBDATA
GPIO28
GPIO27
GPIO25
GPIO24
GPIO23
GPIO22
GPIO21
GPIO20
GPIO19
GPIO18
GPIO13
GPIO12
GPIO8
GPIO7
GPIO6
AC_RST_N
AC_SYNC
AC_BIT_CLK
AC_SDATA_OUT
AC_SDATA_IN0
AC_SDATA_IN1
USBP0P
USBP0N
USBP1P
USBP1N
USBP2P
USBP2N
USBP3P
USBP3N
USBP4P
USBP4N
USBP5P
USBP5N
OC0_N
OC1_N
OC2_N
OC3_N
OC4_N
OC5_N
USBLEDA0_N_GPIO32
USBLEDA1_N_GPIO33
USBLEDA2_N_GPIO34
USBLEDA3_N_GPIO35
USBLEDA4_N_GPIO36
USBLEDA5_N_GPIO37
USBLEDG0_N_GPIO38
USBLEDG1_N_GPIO39
USBLEDG2_N_GPIO40
USBLEDG3_N_GPIO41
USBLEDG4_N_GPIO42
USBLEDG5_N_GPIO43
USBRBIAS
LDRQ0_N
LDRQ1_N
LFRAME_N
LAD0
LAD1
LAD2
LAD3
PDDREQ
PDDACK_N
PIORDY_PDRSTB_PWDMARDY_N
PDIOR_N_PDWSTB_PRDMARDY_N
PDIOW_N_PDSTOP
PDCS1_N
PDCS3_N
PDA0
PDA1
PDA2
PDD0
PDD1
PDD2
PDD3
PDD4
PDD5
PDD6
PDD7
PDD8
PDD9
PDD10
PDD11
PDD12
PDD13
PDD14
PDD15
SDDREQ
SDDACK_N
SIORDY_SDRSTB_SWDMARDY_N
SDIOR_N_SDWSTB_SRDMARDY_N
SDIOW_N_SDSTOP
SDCS1_N
SDCS3_N
SDA0
SDA1
SDA2
SDD0
SDD1
SDD2
SDD3
SDD4
SDD5
SDD6
SDD7
SDD8
SDD9
SDD10
SDD11
SDD12
SDD13
SDD14
SDD15
ICH3_LAD[3:0]
ICH3_PDD[15:0]
+VSBY3_3
+V3_3
R369 8.2K
R368 10K
R562 1K
R371 10K
R1044 10K
R1045 10K
R1004 10K NOPOP
RP197 10K
R390 4.7K
R374 18.2
If using ICH3 A0 or A1 samples, R374 should be 33K.
Use 22.6 ohms for ICH3 B0, and 18.2 ohms for ICH3 B2.
TITLE:
Rev: A2
EID
Chandler, Arizona
DRAWN BY: TCL
PROJECT: MC
LAST REVISED: 8/08/02
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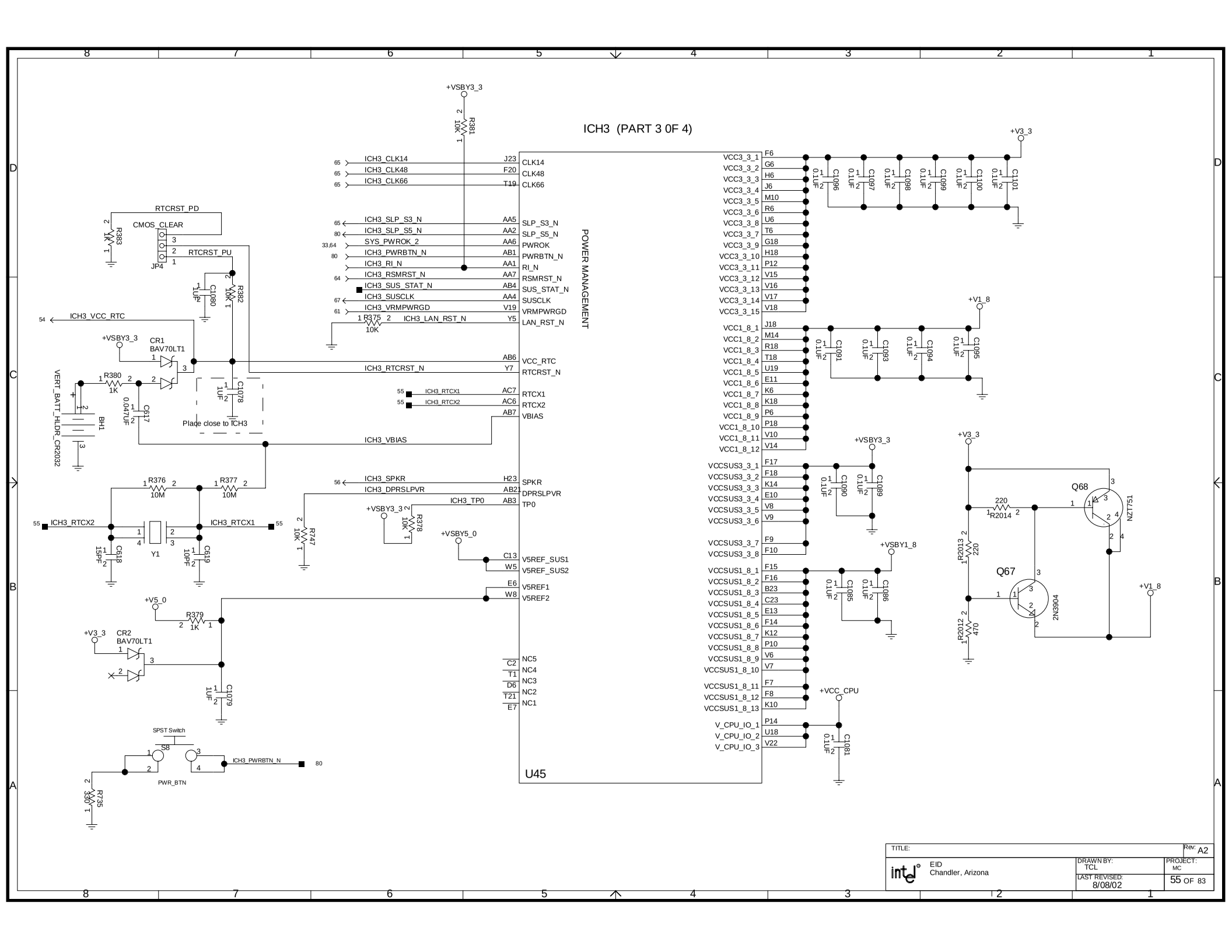
ICH3 (PART 3 0F 4)
U45
POWER MANAGEMENT
+VSBY3_3
+V3_3
+V1_8
+VSBY5_0
+VSBY1_8
+VCC_CPU
+V5_0
RTCRST_PD
CMOS_CLEAR
RTCRST_PU
JP4
ICH3_VCC_RTC
CR1
BAV70LT1
CR2
VERT_BATT_HLDR_CR2032
BH1
Place close to ICH3
ICH3_VBIAS
ICH3_RTCX1
ICH3_RTCX2
Y1
ICH3_SPKR
ICH3_DPRSLPVR
ICH3_TP0
ICH3_CLK14
ICH3_CLK48
ICH3_CLK66
ICH3_SLP_S3_N
ICH3_SLP_S5_N
SYS_PWROK_2
ICH3_PWRBTN_N
ICH3_RI_N
ICH3_RSMRST_N
ICH3_SUS_STAT_N
ICH3_SUSCLK
ICH3_VRMPWRGD
ICH3_LAN_RST_N
ICH3_RTCRST_N
SPST Switch
S8
PWR_BTN
Q68
Q67
NZT751
2N3904
TITLE:
Rev: A2
EID
Chandler, Arizona
DRAWN BY: TCL
PROJECT: MC
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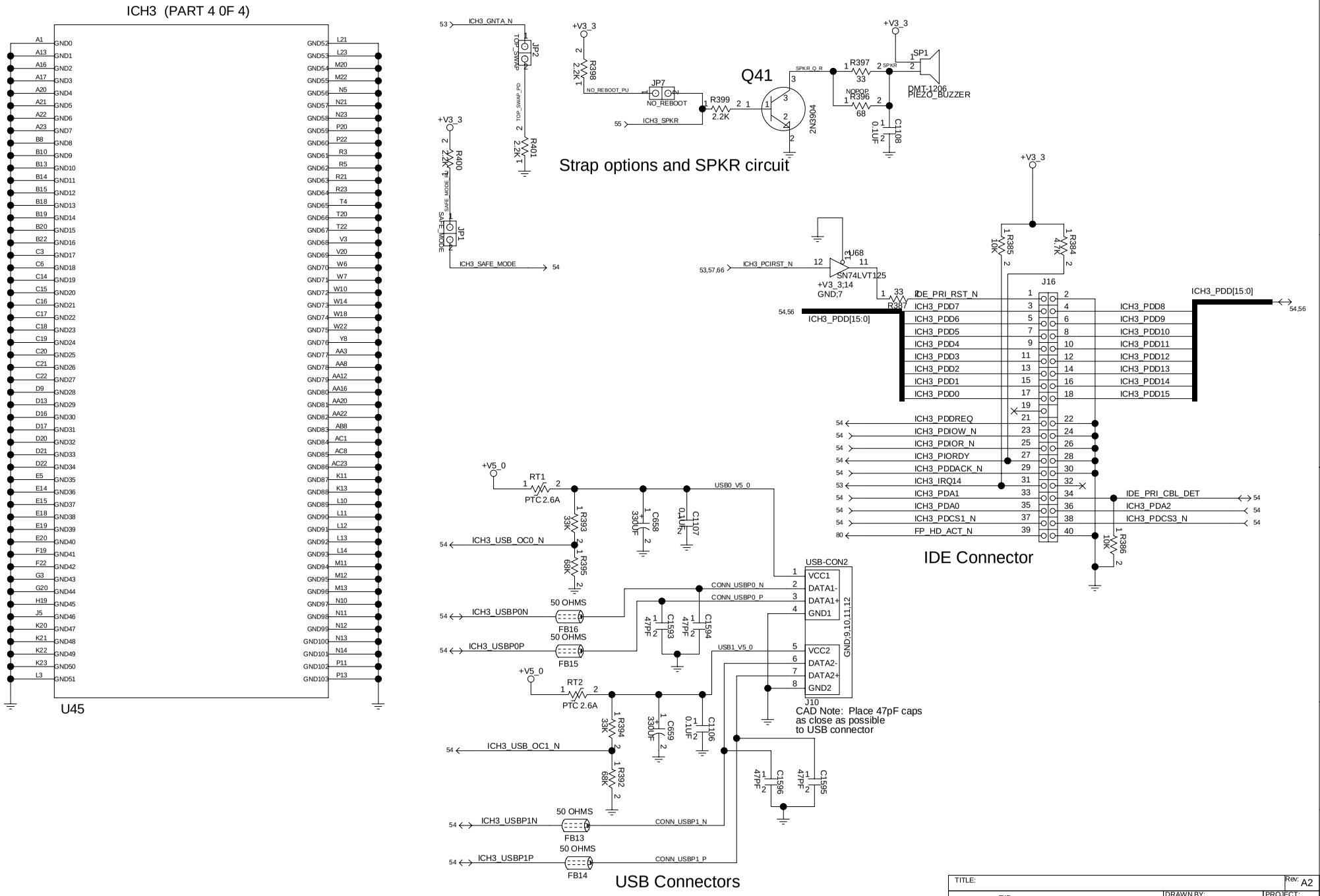
ICH3 (PART 4 0F 4)
U45
Strap options and SPKR circuit
ICH3_GNTA_N
JP2
TOP_SWAP
R398
2.2K
+V3_3
JP7
NO_REBOOT
NO_REBOOT_PU
R399
2.2K
ICH3_SPKR
Q41
2N3904
SPKR_Q_R
R397
33
SP1
SPKR
DMT-1206
PIEZO_BUZZER
R396
68
NOPOP
C1108
0.1UF
R401
2.2K
R400
2.2K
JP1
SAFE_MODE
ICH3_SAFE_MODE
ICH3_PCIRST_N
U68
SN74LVT125
+V3_3;14
GND;7
R385
10K
R384
4.7K
J16
IDE_PRI_RST_N
R387
33
ICH3_PDD[15:0]
ICH3_PDD7
ICH3_PDD6
ICH3_PDD5
ICH3_PDD4
ICH3_PDD3
ICH3_PDD2
ICH3_PDD1
ICH3_PDD0
ICH3_PDD8
ICH3_PDD9
ICH3_PDD10
ICH3_PDD11
ICH3_PDD12
ICH3_PDD13
ICH3_PDD14
ICH3_PDD15
ICH3_PDDREQ
ICH3_PDIOW_N
ICH3_PDIOR_N
ICH3_PIORDY
ICH3_PDDACK_N
ICH3_IRQ14
ICH3_PDA1
ICH3_PDA0
ICH3_PDCS1_N
FP_HD_ACT_N
IDE_PRI_CBL_DET
ICH3_PDA2
ICH3_PDCS3_N
R386
10K
IDE Connector
RT1
PTC 2.6A
USB0_V5_0
C658
330UF
C1107
0.1UF
R393
33K
R395
68K
ICH3_USB_OC0_N
ICH3_USBP0N
ICH3_USBP0P
50 OHMS
FB16
FB15
CONN_USBP0_N
CONN_USBP0_P
C1593
47PF
C1594
47PF
USB-CON2
VCC1
DATA1-
DATA1+
GND1
VCC2
DATA2-
DATA2+
GND2
GND;9,10,11,12
J10
USB1_V5_0
RT2
PTC 2.6A
R394
33K
C659
330UF
C1106
0.1UF
R392
68K
ICH3_USB_OC1_N
ICH3_USBP1N
ICH3_USBP1P
FB13
FB14
CONN_USBP1_N
CONN_USBP1_P
C1596
47PF
C1595
47PF
CAD Note: Place 47pF caps as close as possible to USB connector
USB Connectors
TITLE:
Rev: A2
EID
Chandler, Arizona
DRAWN BY: TCL
PROJECT: MC
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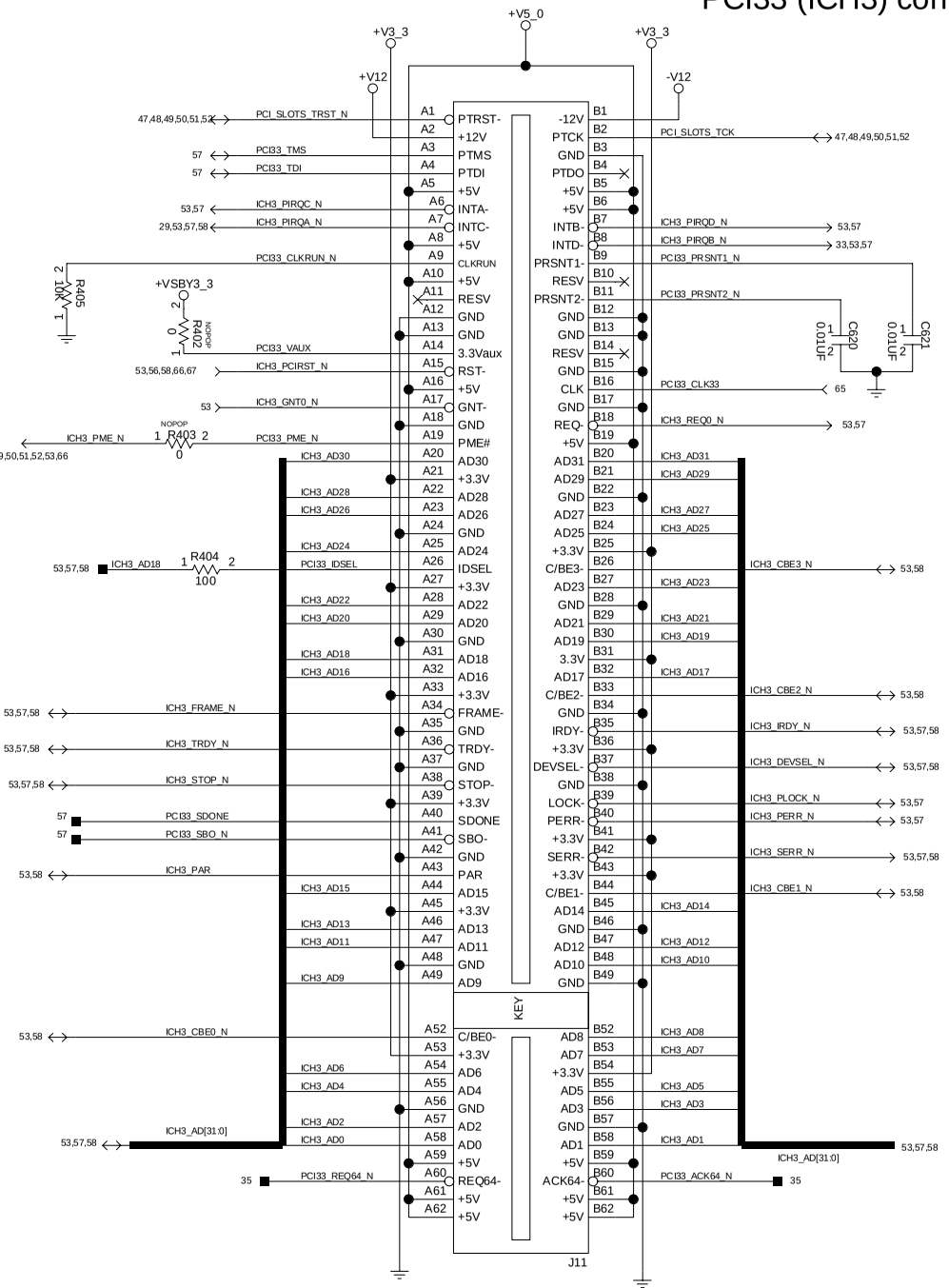
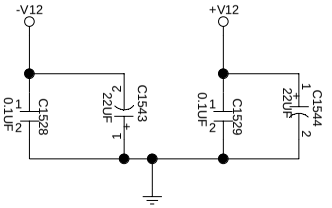
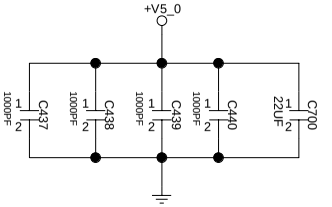
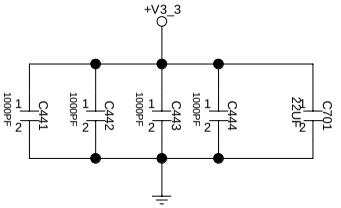
PCI33 (ICH3) connector, termination and decoupling

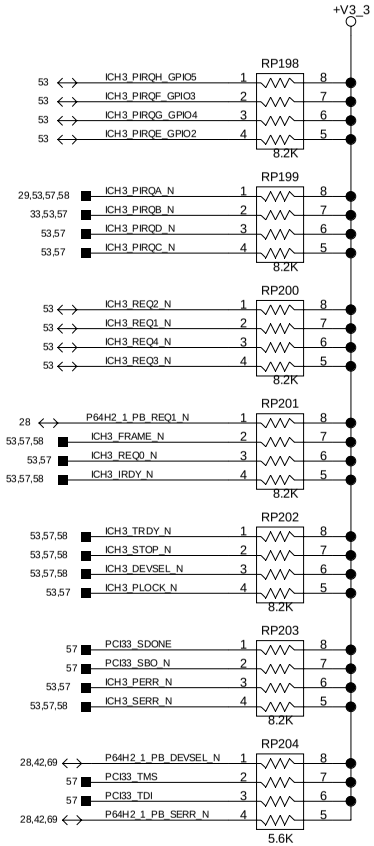




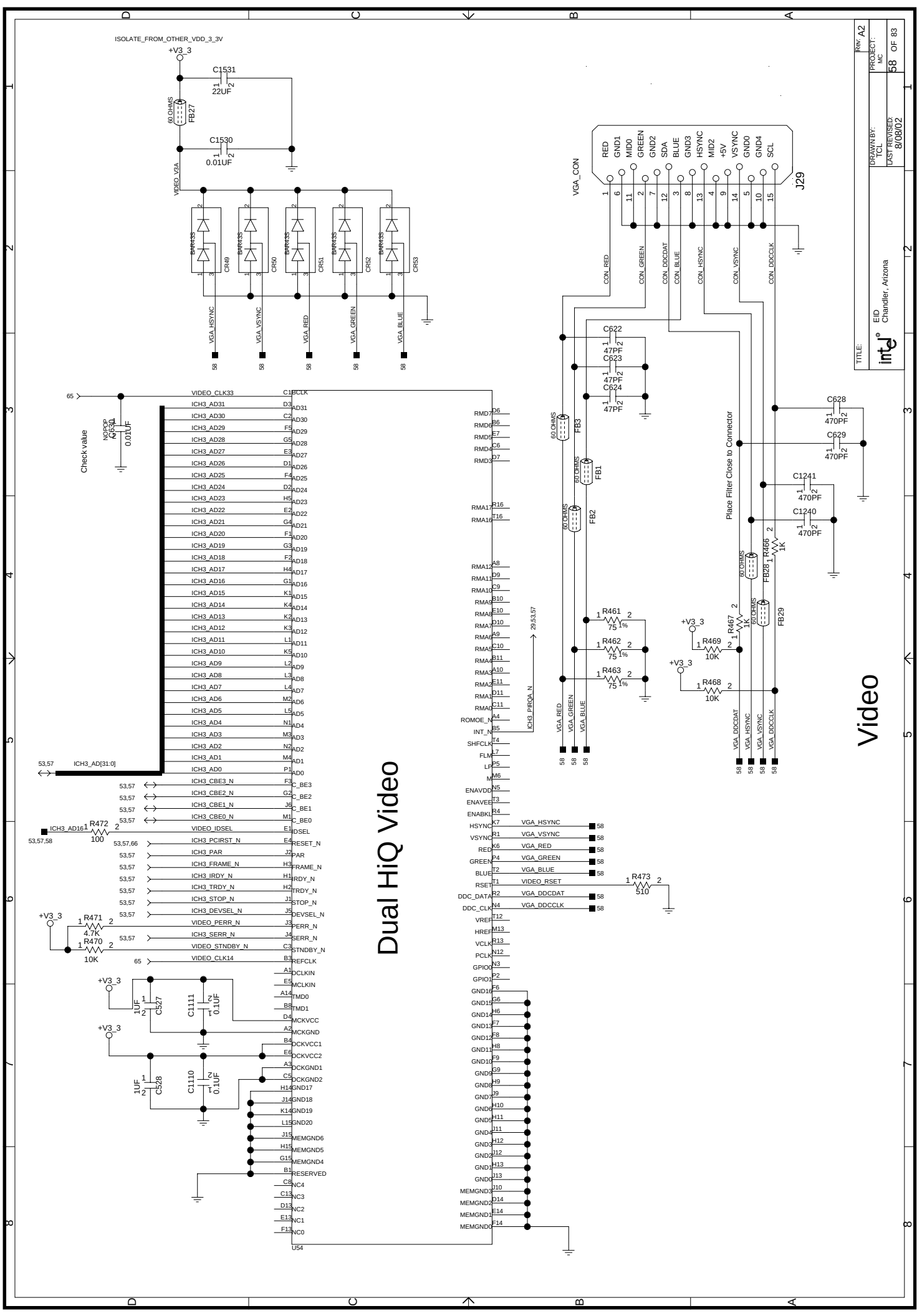


Place caps near connector





TITLE:		Rev: A2
intel EID Chandler, Arizona	DRAWN BY: TCL	PROJECT: MC
	LAST REVISED: 8/08/02	57 OF 83


Video
Dual HiQ Video
ISOLATE_FROM_OTHER_VDD_3_3V
+V3_3
C1531
22UF
C1530
0.01UF
FB27
60 OHMS
VIDEO_V3A
BAR43S
CR49
CR50
CR51
CR52
CR53
VGA_HSYNC
VGA_VSYNC
VGA_RED
VGA_GREEN
VGA_BLUE
VGA_CON
J29
RED
GND1
MID0
GREEN
GND2
SDA
BLUE
GND3
HSYNC
MID2
+5V
VSYNC
GND0
GND4
SCL
CON_RED
CON_GREEN
CON_DDCDAT
CON_BLUE
CON_HSYNC
CON_VSYNC
CON_DDCCLK
C622
C623
C624
47PF
FB3
FB1
FB2
C628
C629
C1241
C1240
470PF
Place Filter Close to Connector
R466
1K
FB28
FB29
R461
R462
R463
75 1%
R467
R469
R468
10K
VGA_RED
VGA_GREEN
VGA_BLUE
VGA_DDCDAT
VGA_HSYNC
VGA_VSYNC
VGA_DDCCLK
Check value
NOPOP
C531
0.01UF
VIDEO_CLK33
ICH3_AD31
ICH3_AD30
ICH3_AD29
ICH3_AD28
ICH3_AD27
ICH3_AD26
ICH3_AD25
ICH3_AD24
ICH3_AD23
ICH3_AD22
ICH3_AD21
ICH3_AD20
ICH3_AD19
ICH3_AD18
ICH3_AD17
ICH3_AD16
ICH3_AD15
ICH3_AD14
ICH3_AD13
ICH3_AD12
ICH3_AD11
ICH3_AD10
ICH3_AD9
ICH3_AD8
ICH3_AD7
ICH3_AD6
ICH3_AD5
ICH3_AD4
ICH3_AD3
ICH3_AD2
ICH3_AD1
ICH3_AD0
ICH3_AD[31:0]
ICH3_CBE3_N
ICH3_CBE2_N
ICH3_CBE1_N
ICH3_CBE0_N
ICH3_AD16
R472
100
VIDEO_IDSEL
ICH3_PCIRST_N
ICH3_PAR
ICH3_FRAME_N
ICH3_IRDY_N
ICH3_TRDY_N
ICH3_STOP_N
ICH3_DEVSEL_N
VIDEO_PERR_N
ICH3_SERR_N
VIDEO_STNDBY_N
VIDEO_CLK14
R471
4.7K
R470
10K
C527
C528
C1111
C1110
0.1UF
U54
RMD7
RMD6
RMD5
RMD4
RMD3
RMA17
RMA16
RMA12
RMA11
RMA10
RMA9
RMA8
RMA7
RMA6
RMA5
RMA4
RMA3
RMA2
RMA1
RMA0
ROMOE_N
INT_N
SHFCLK
FLM
LP
M
ENAVDD
ENAVEE
ENABKL
HSYNC
VSYNC
RED
GREEN
BLUE
RSET
DDC_DATA
DDC_CLK
VREF
HREF
VCLK
PCLK
GPIO0
GPIO1
ICH3_PIRQA_N
VIDEO_RSET
VGA_DDCDAT
VGA_DDCCLK
R473
510
MEMGND3
MEMGND2
MEMGND1
MEMGND0
GND16
GND15
GND14
GND13
GND12
GND11
GND10
GND9
GND8
GND7
GND6
GND5
GND4
GND3
GND2
GND1
GND0
MCKVCC
MCKGND
DCKVCC1
DCKVCC2
DCKGND1
DCKGND2
GND17
GND18
GND19
GND20
MEMGND6
MEMGND5
MEMGND4
RESERVED
NC4
NC3
NC2
NC1
NC0
TITLE:
intel
EID
Chandler, Arizona
DRAWN BY:
TCL
LAST REVISED:
8/08/02
PROJECT:
MC
Rev: A2
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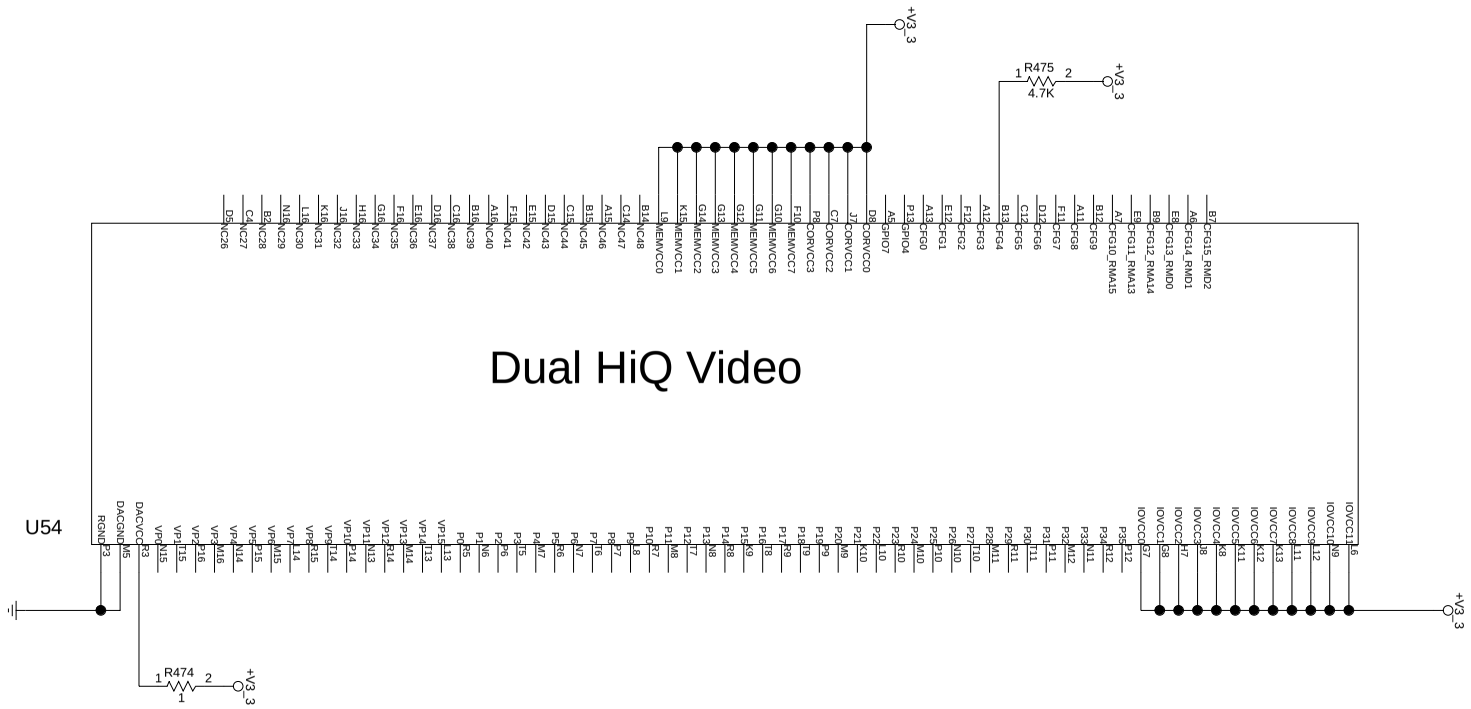
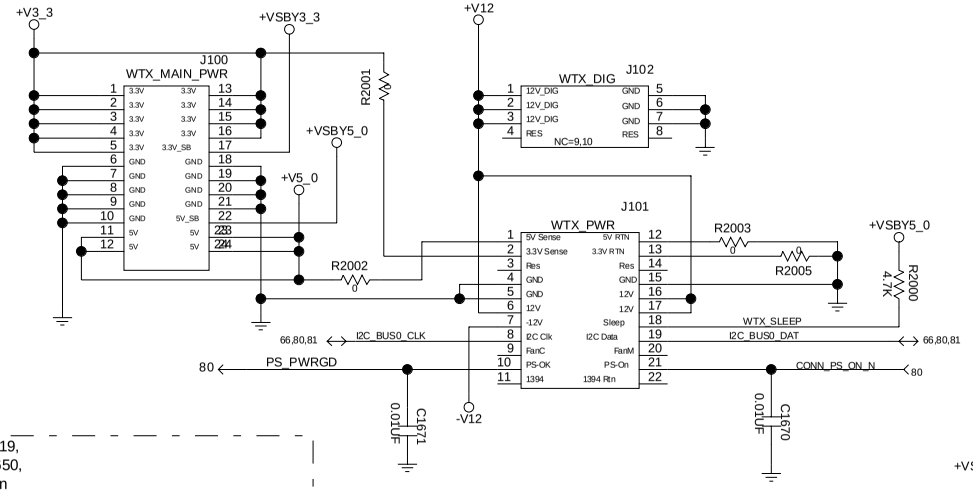
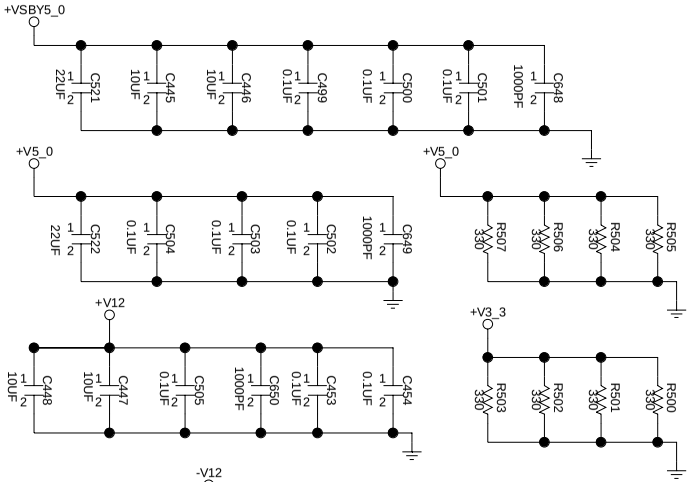


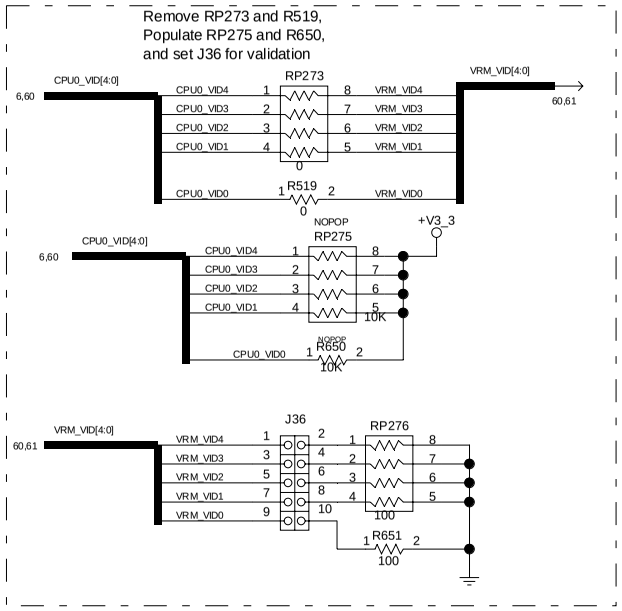
Video

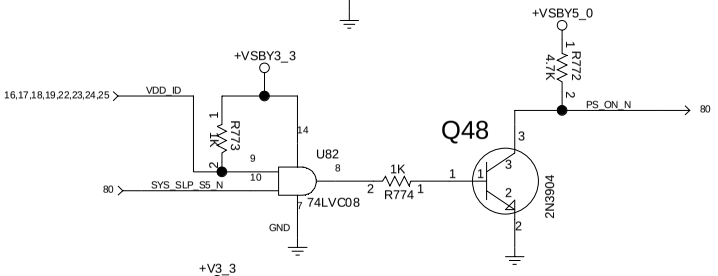
TITLE:		Rev: A2
intel EID Chandler, Arizona	DRAWN BY: TCL	PROJECT: MC
	LAST REVISED: 8/08/02	59 OF 83

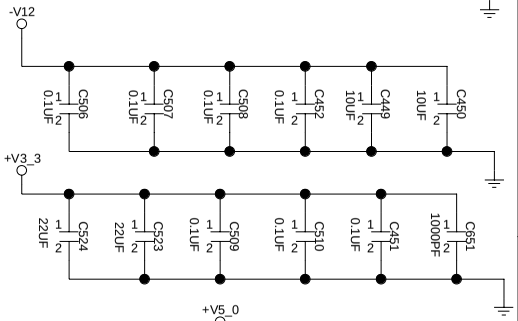
Power Connectors

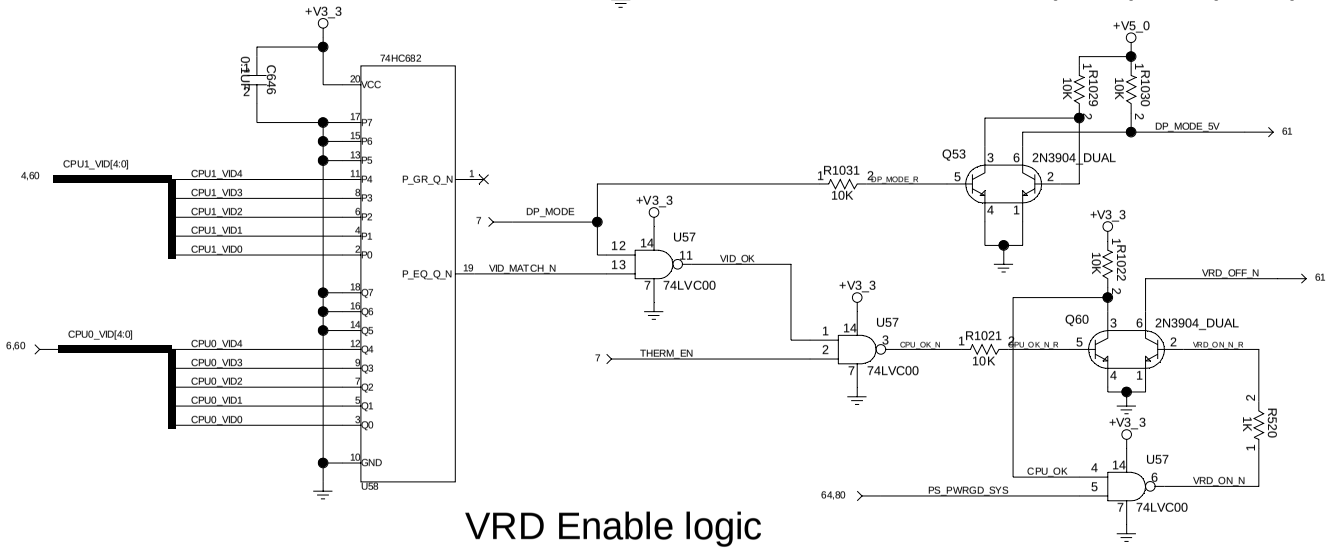












VRD Enable logic

TITLE:			Rev: A2
intel EID Chandler, Arizona	DRAWN BY: TCL	PROJECT: MC	
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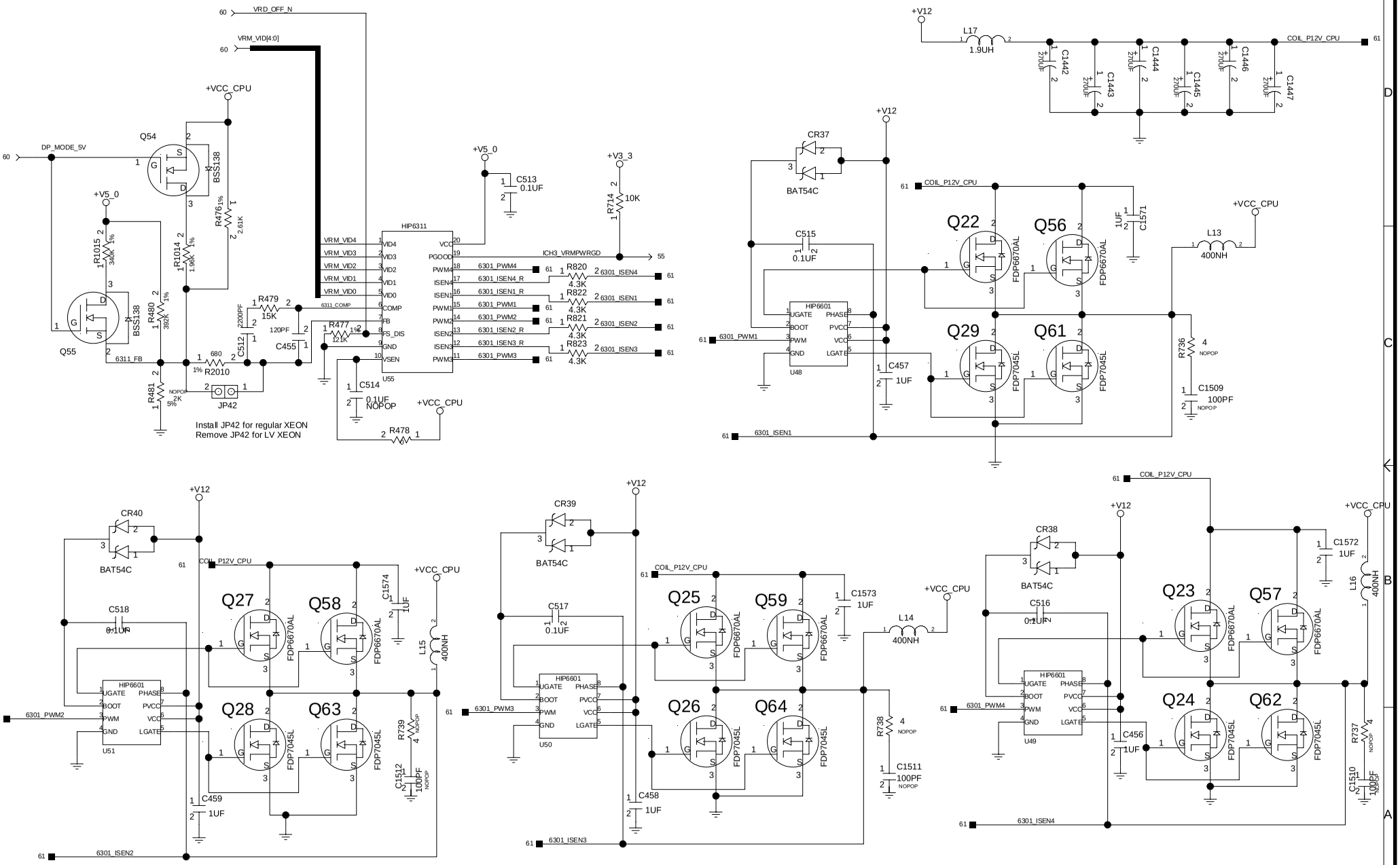

Processor Voltage Regulator circuitry

TITLE:		Rev: A2
intel EID Chandler, Arizona	DRAWN BY: TCL	PROJECT: MC
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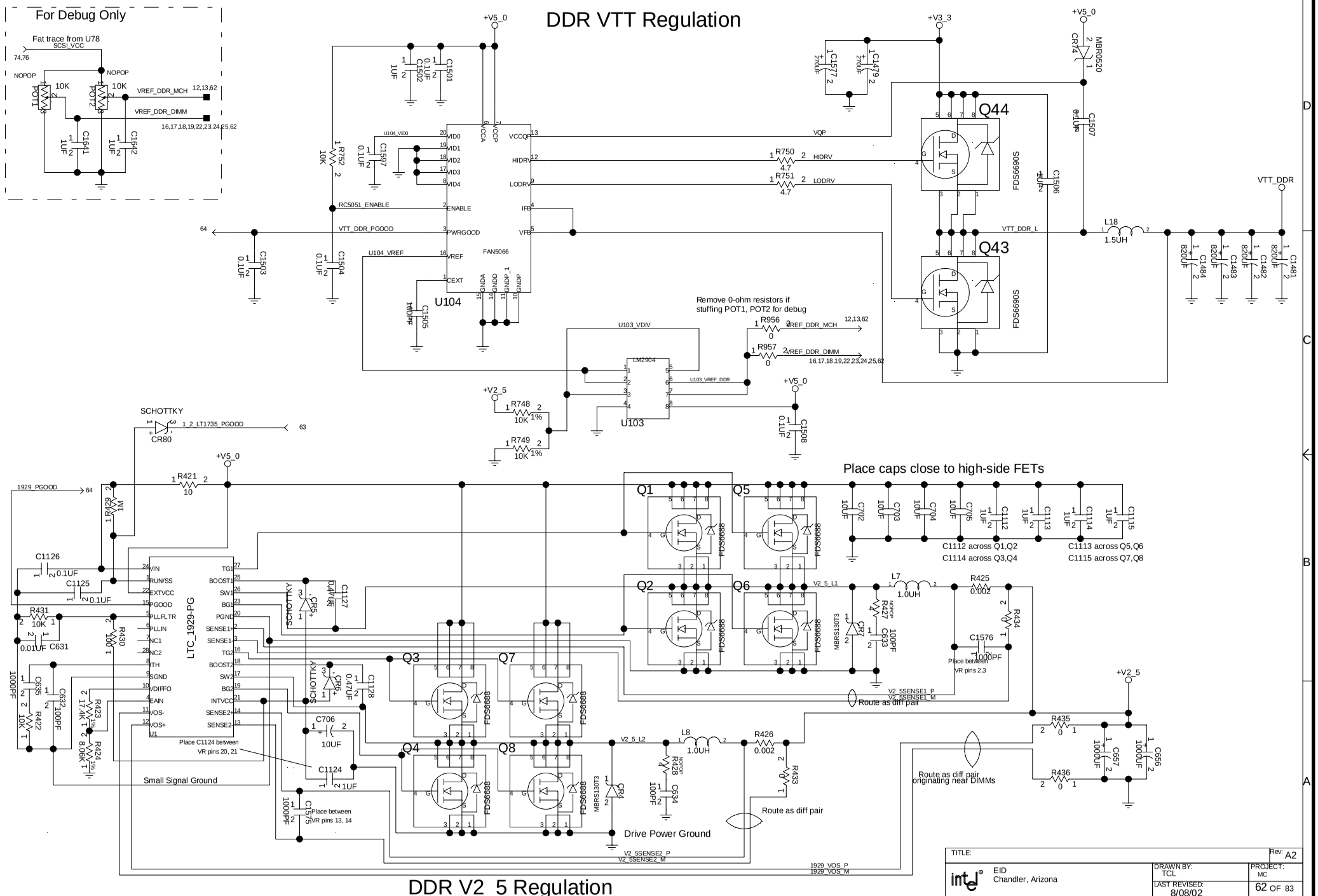
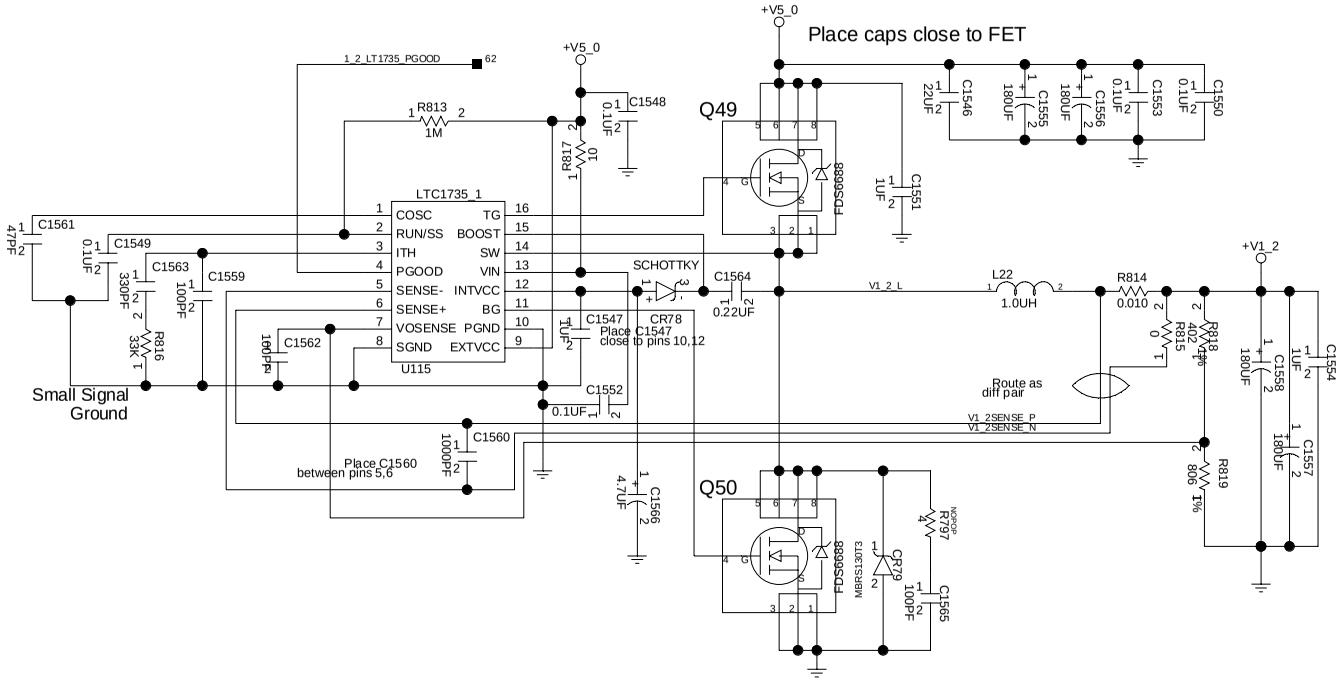
DDR VTT Regulation



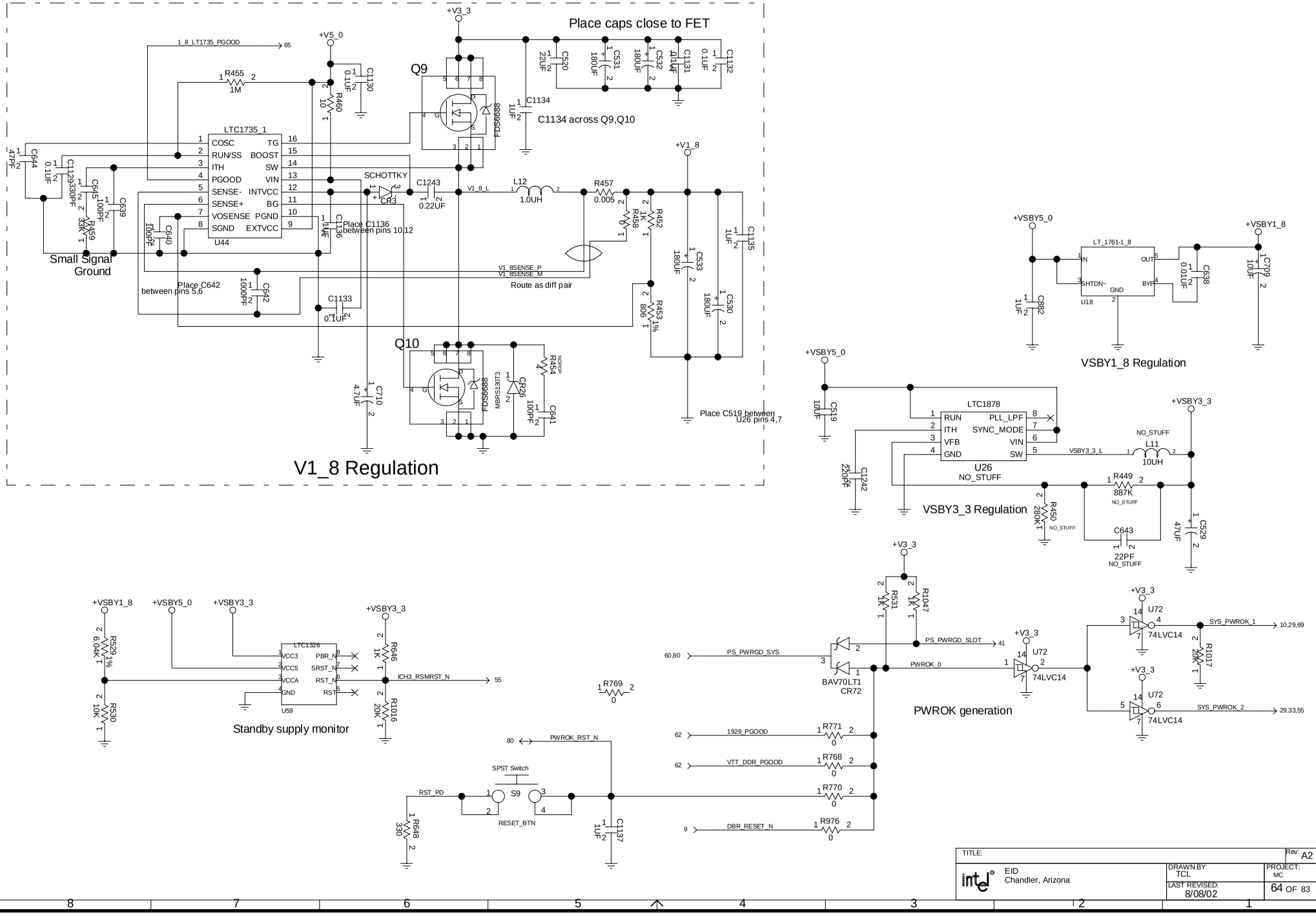
DDR V2_5 Regulation

TITLE:		Rev: A2
intel EID Chandler, Arizona	DRAWN BY: TCL	PROJECT: MC
	LAST REVISED: 8/08/02	62 OF 83

V1.2 Regulation



TITLE:			Rev: A2
intel EID Chandler, Arizona		DRAWN BY: TCL	PROJECT: MC
		LAST REVISED: 8/08/02	63 OF 83



TITLE:	Rev: A2
intel EID Chandler, Arizona	DRAWN BY: TCL
	PROJECT: MC
	LAST REVISED: 8/08/02
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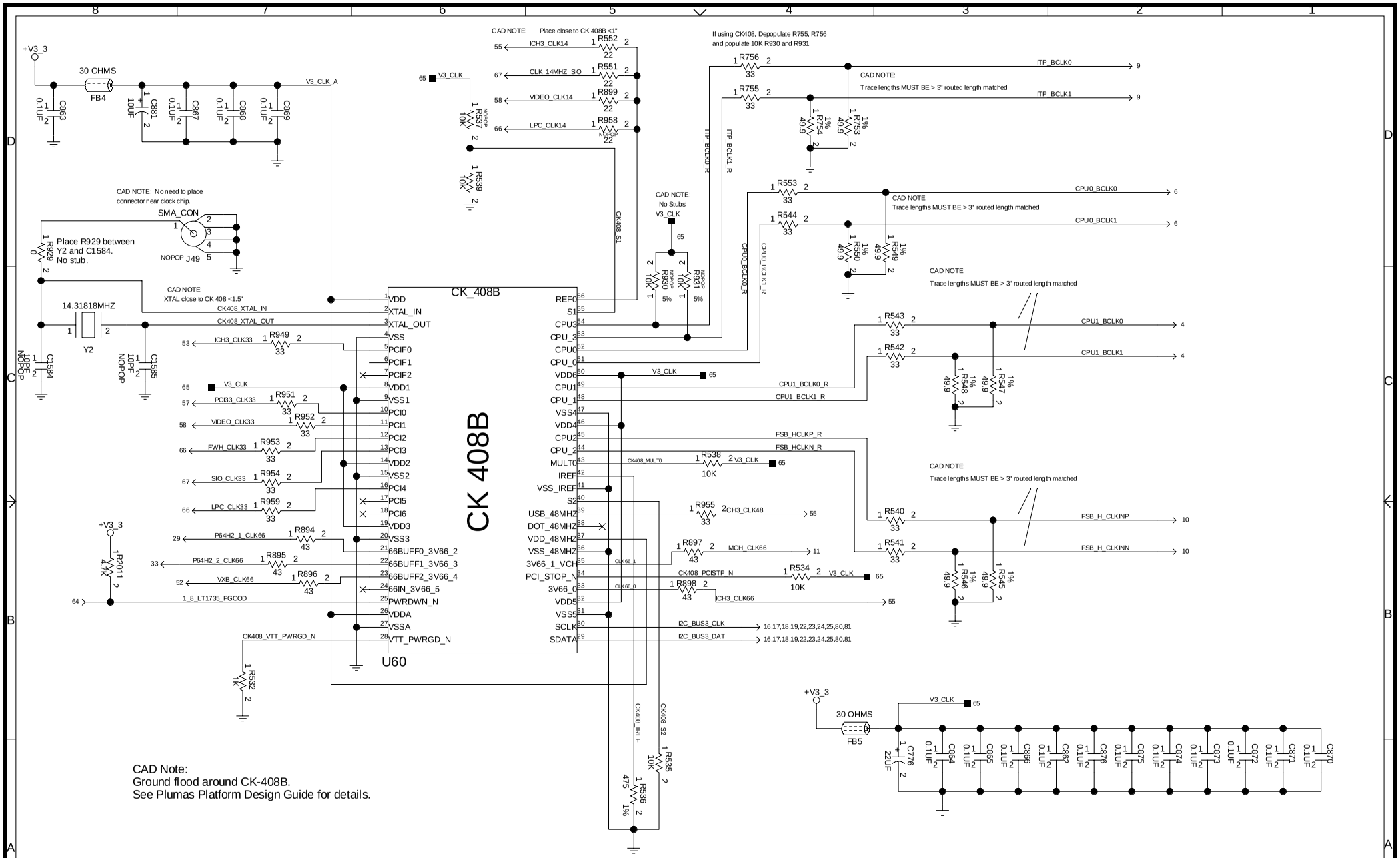
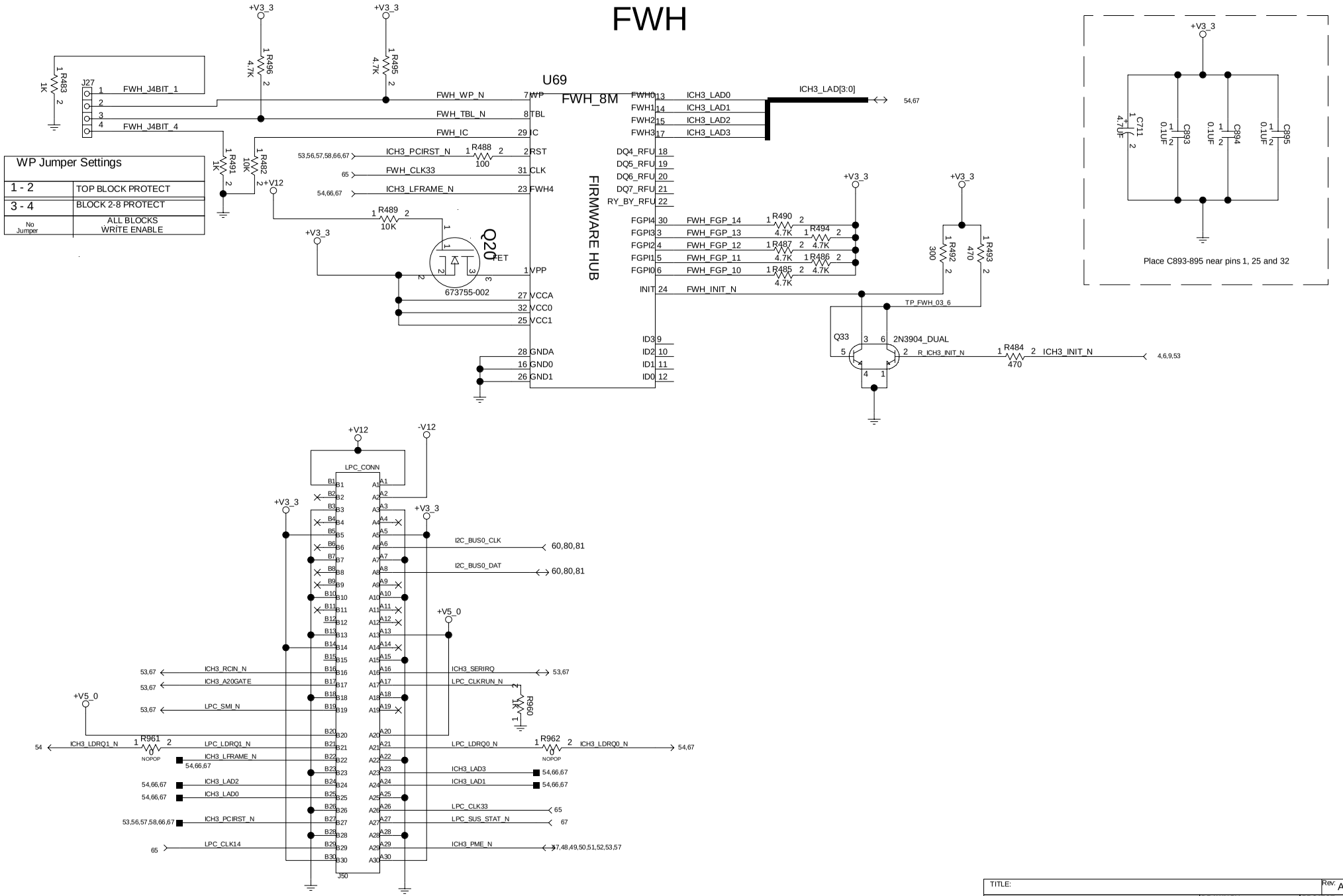


CK408-B
Clock Synthesizer

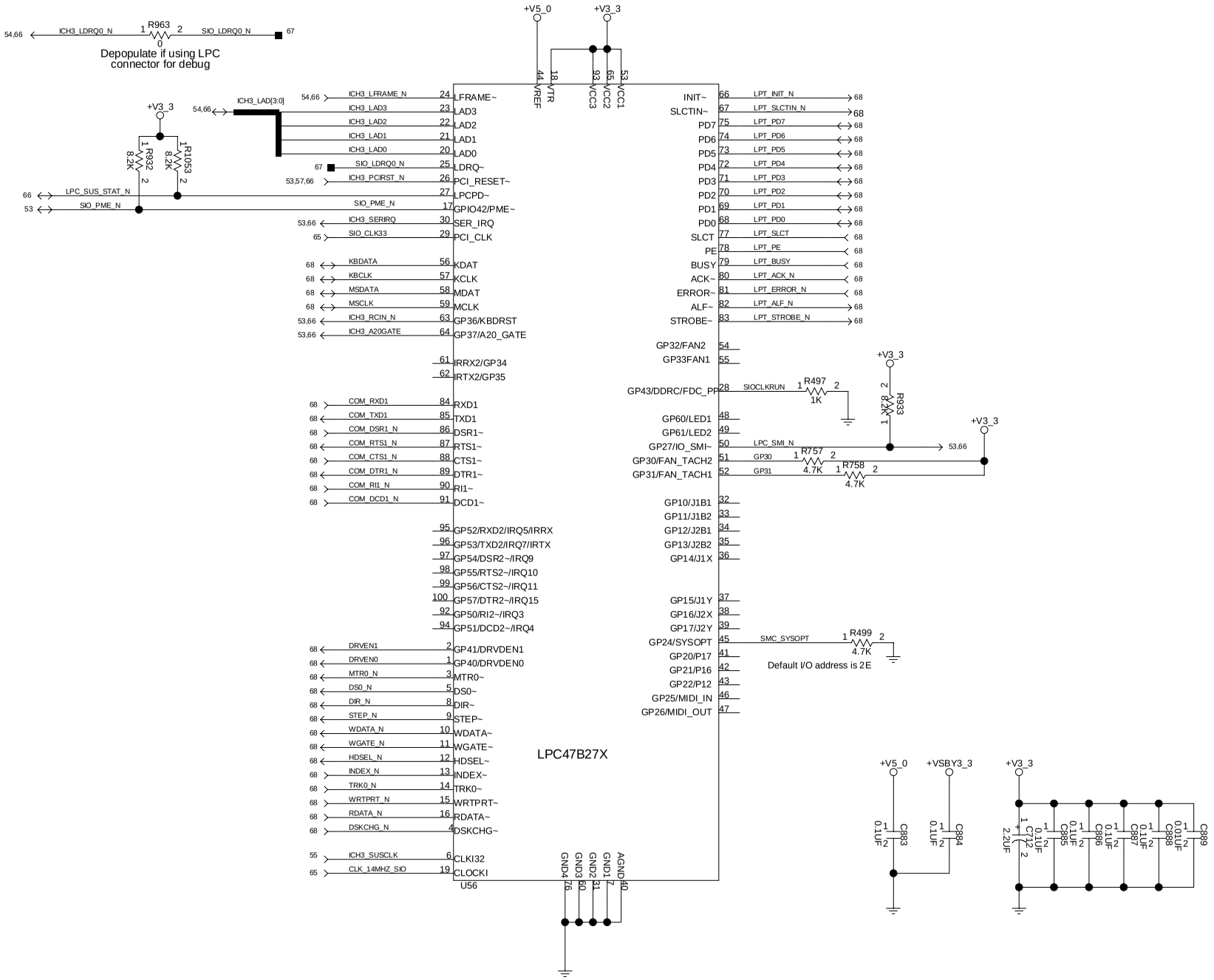
TITLE:		Rev: A2
intel EID Chandler, Arizona	DRAWN BY: TCL	PROJECT: MC
	LAST REVISED: 8/08/02	65 OF 83

FWH



LPC connector (for debug only)

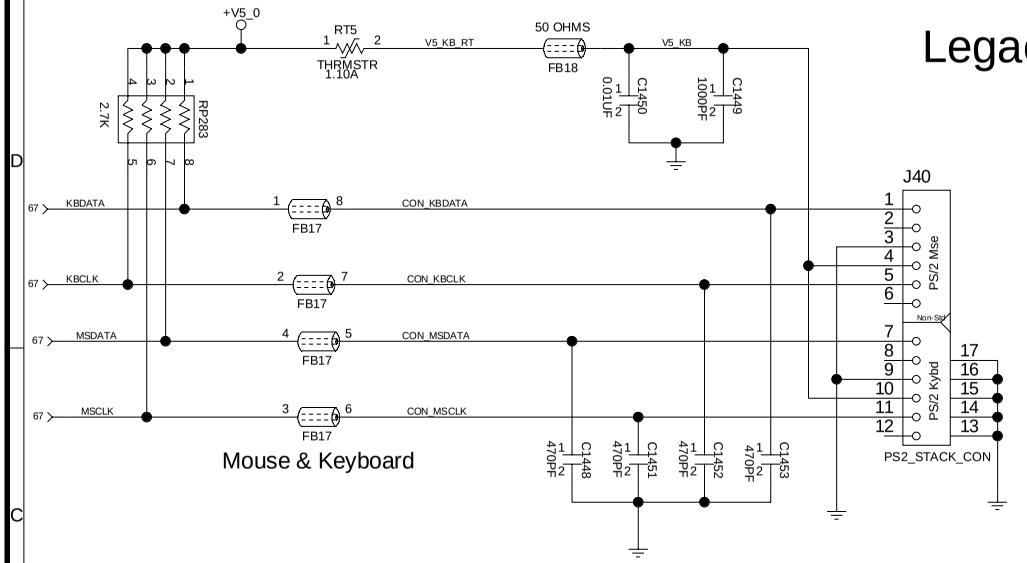
TITLE:			Rev: A2
intel EID Chandler, Arizona	DRAWN BY: TCL	PROJECT: MC	
	LAST REVISED: 8/08/02	66 OF 83	



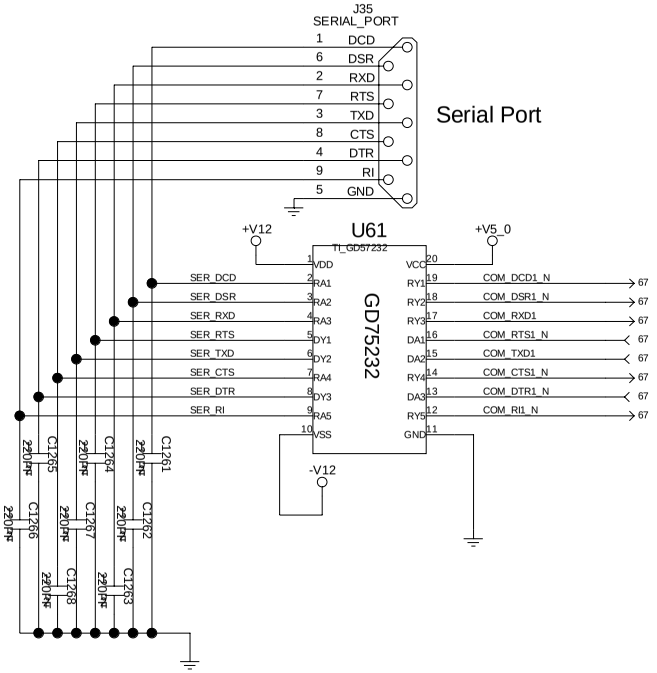
SIO

TITLE:			Rev: A2
intel EID Chandler, Arizona		DRAWN BY: TCL	PROJECT: MC
		LAST REVISED: 8/08/02	67 OF 83

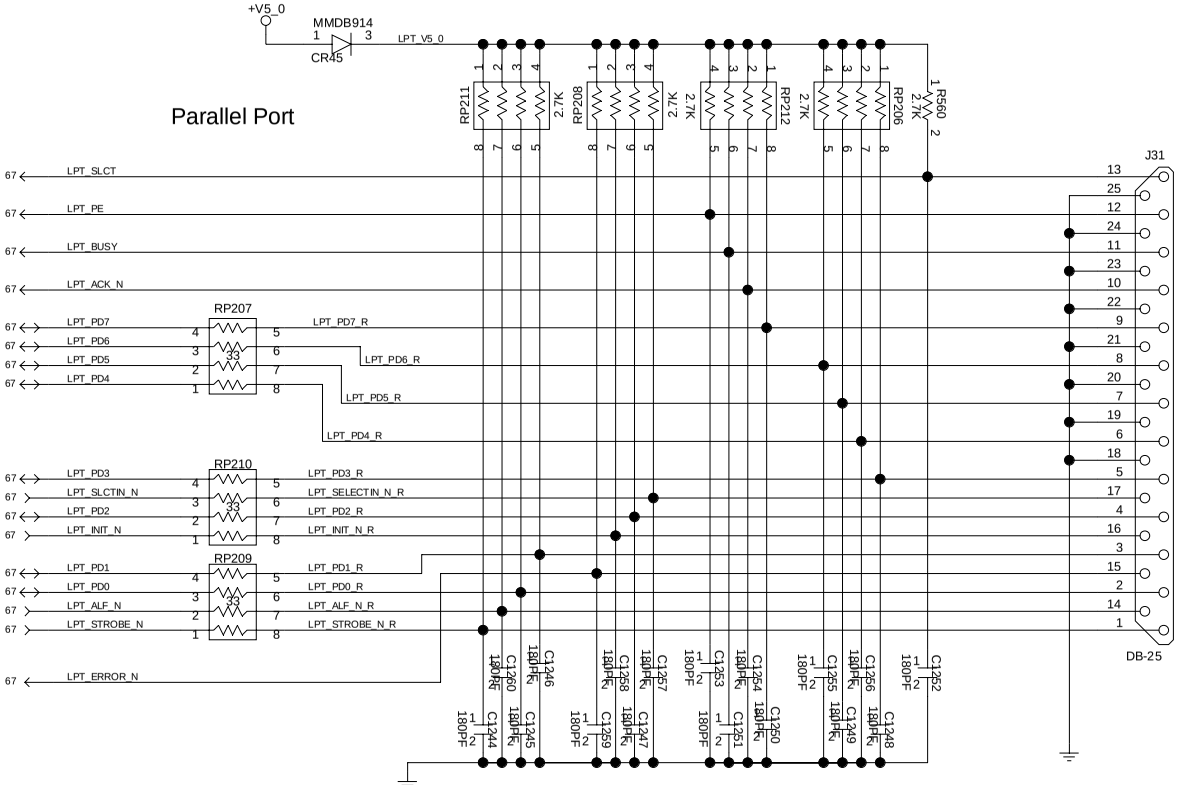
Legacy I/O



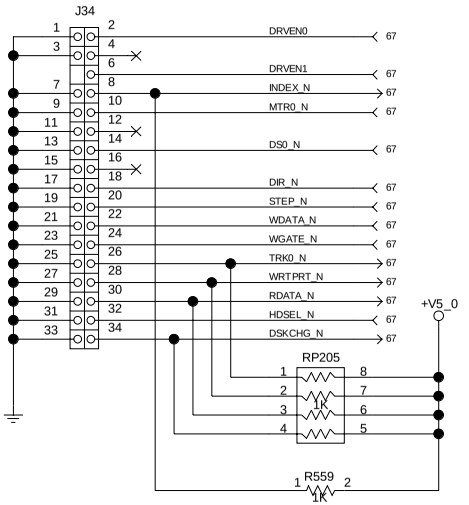
Mouse & Keyboard



Serial Port



Parallel Port



Floppy Connector

TITLE:		Rev: A2	
intel EID Chandler, Arizona	DRAWN BY: TCL	PROJECT: MC	
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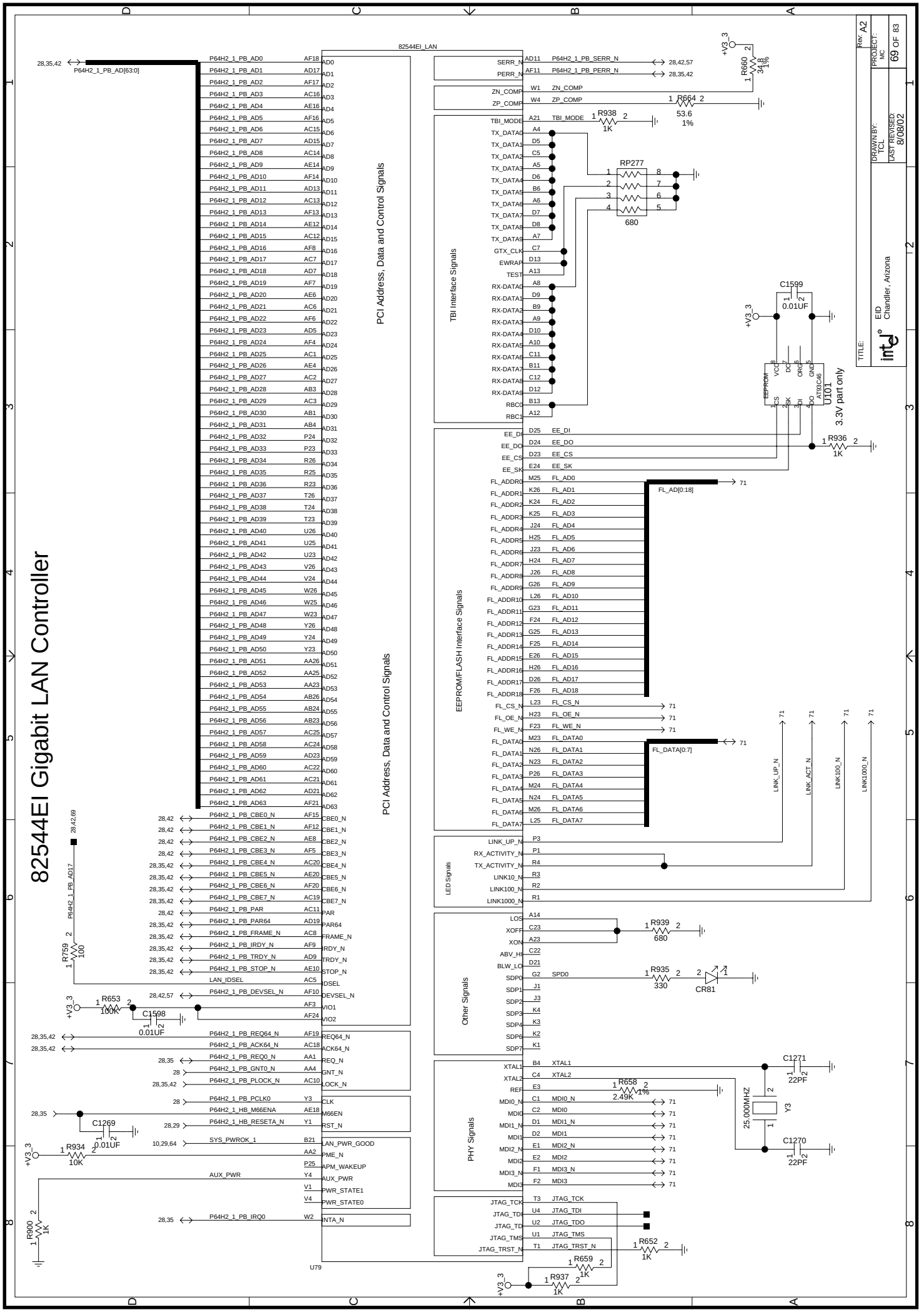
82544EI Gigabit LAN Controller
82544EI_LAN
PCI Address, Data and Control Signals
TBI Interface Signals
EEPROM/FLASH Interface Signals
LED Signals
Other Signals
PHY Signals
U79
U101
3.3V part only
P64H2_1_PB_AD[63:0]
FL_AD[0:18]
FL_DATA[0:7]
LINK_UP_N
LINK_ACT_N
LINK100_N
LINK1000_N
Rev: A2
PROJECT: MC
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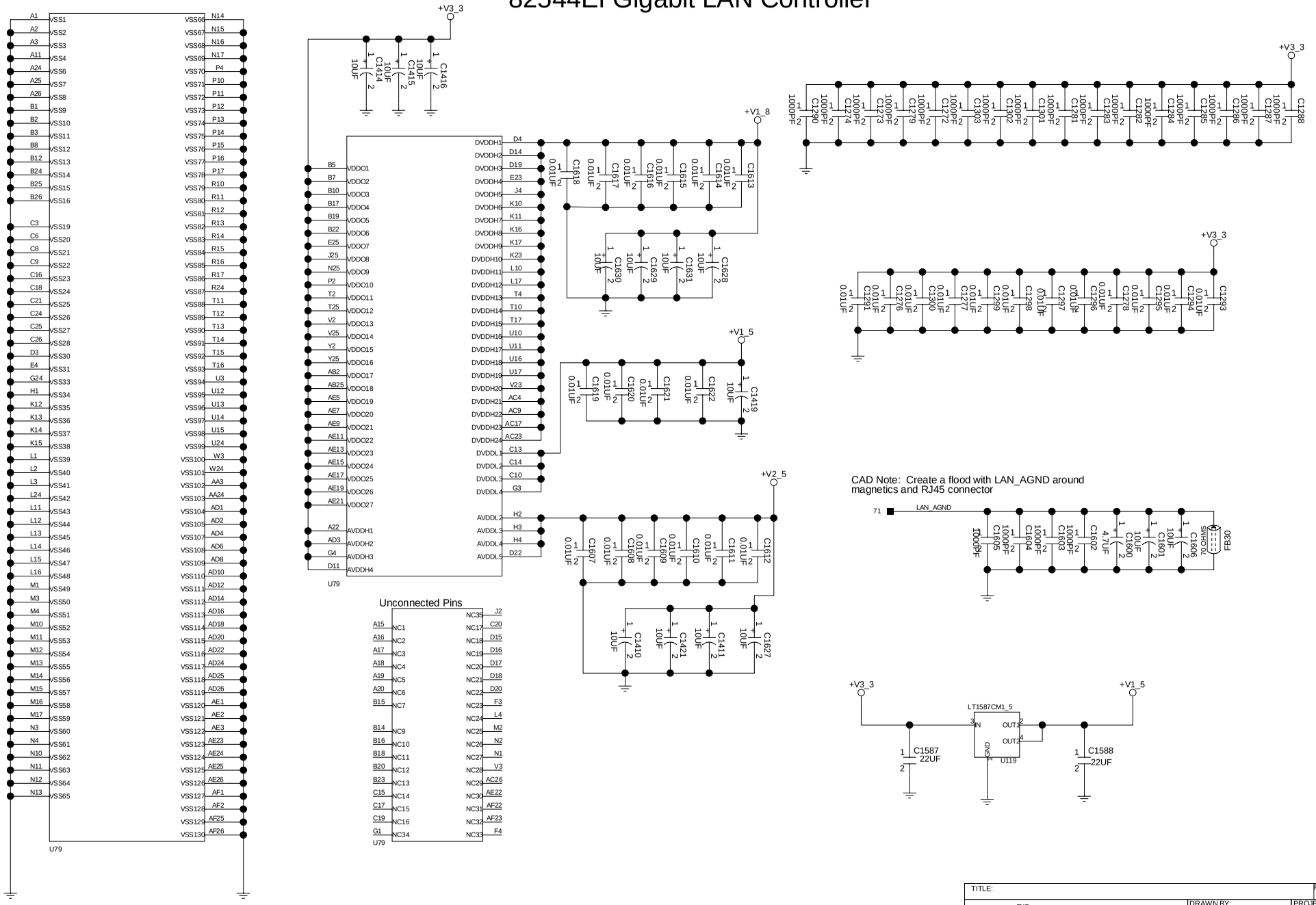
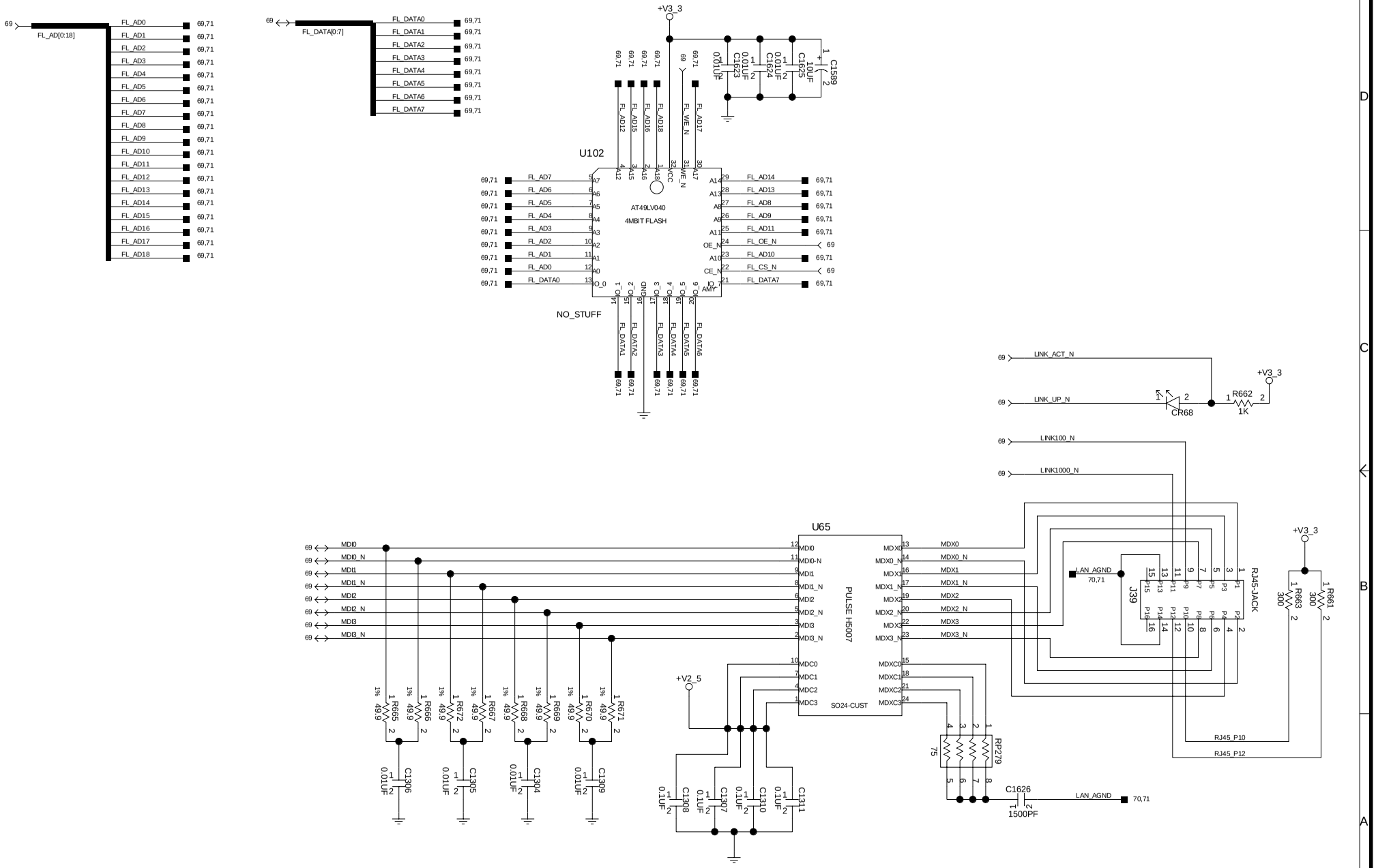
DRAWN BY: TCL
LAST REVISED: 8/08/02
TITLE:
EID
Chandler, Arizona

82544EI Gigabit LAN Controller

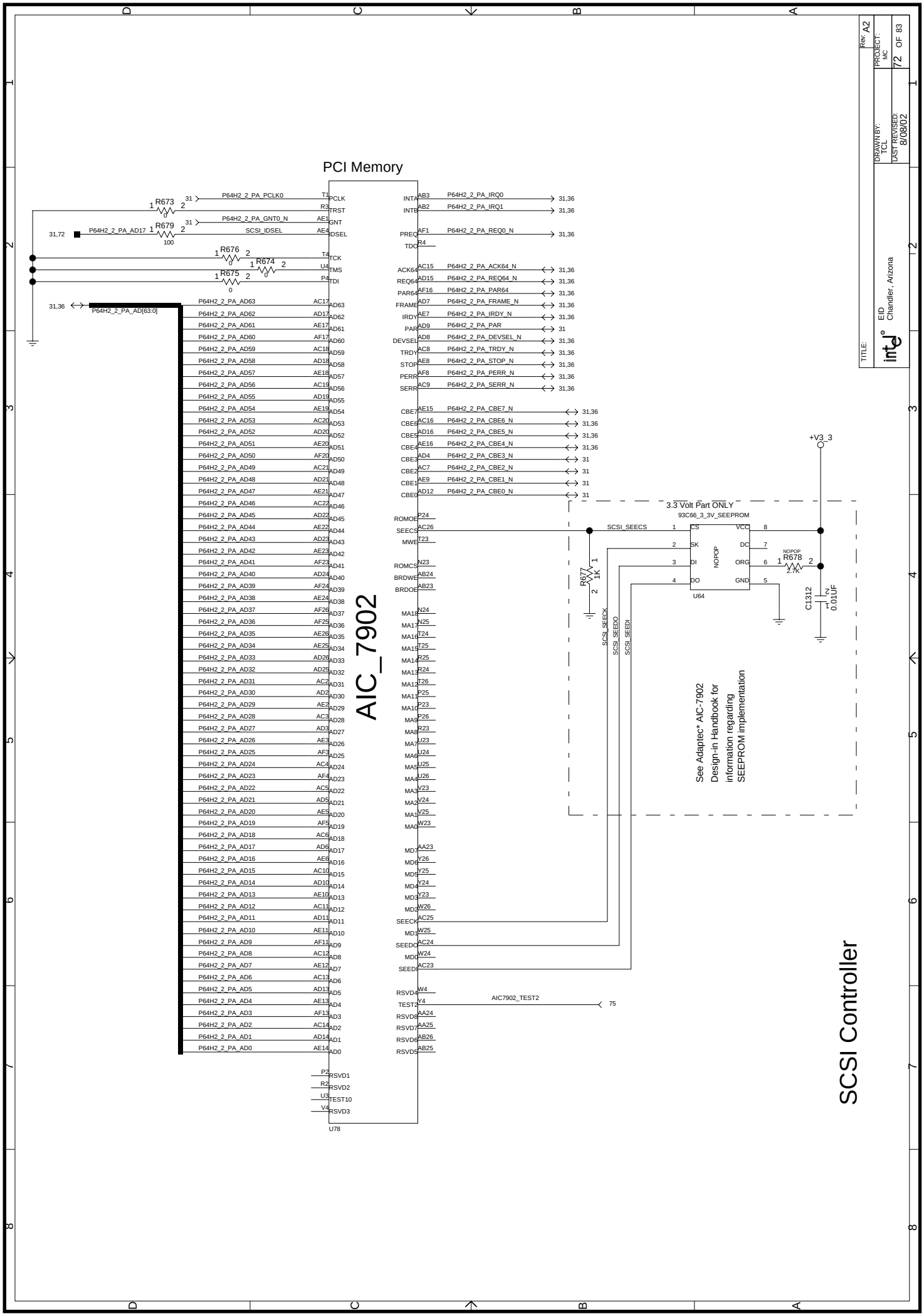


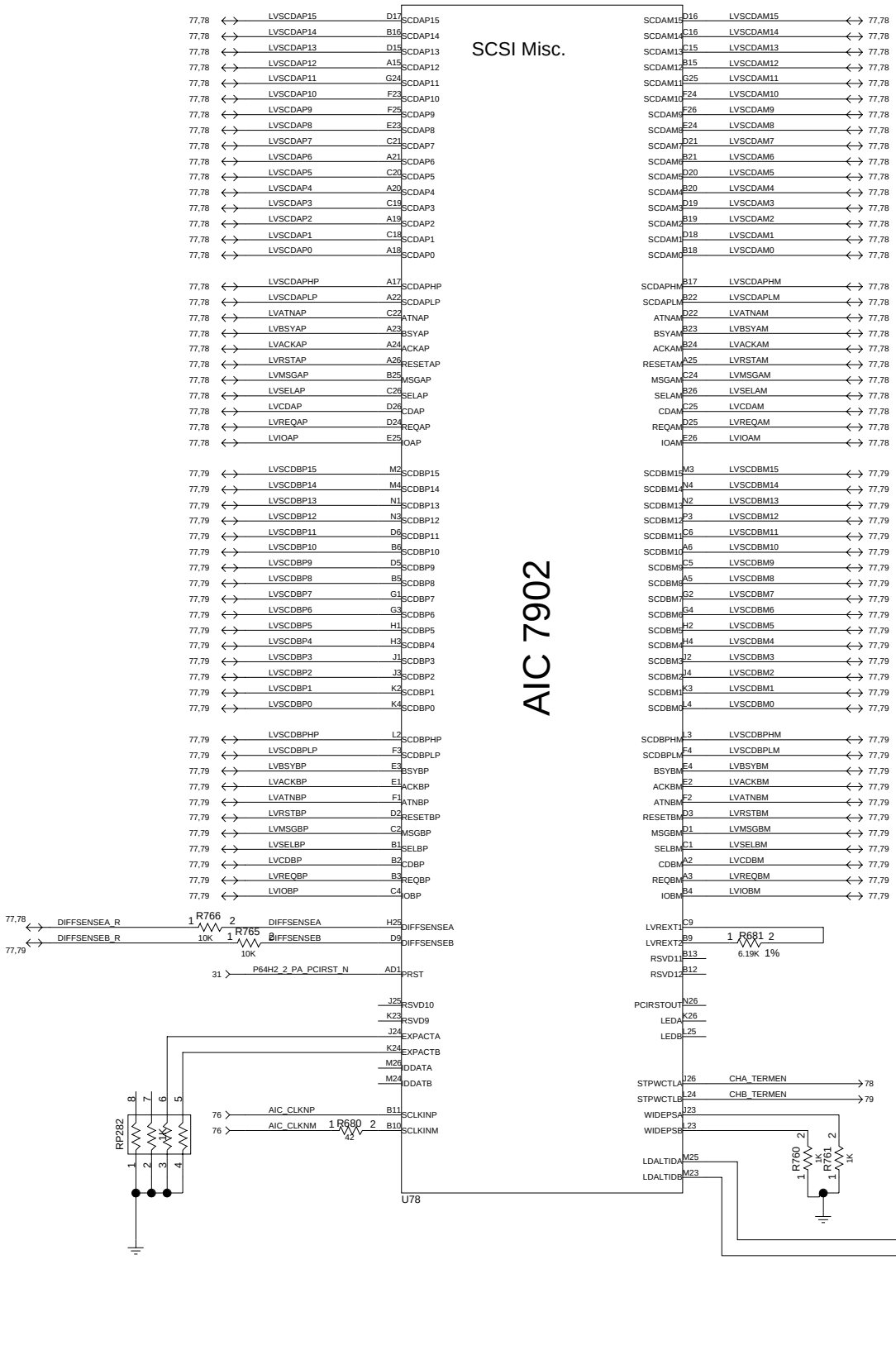
TITLE:			Rev: A2
intel EID Chandler, Arizona	DRAWN BY: TCL	PROJECT: MC	
	LAST REVISED: 8/08/02	70 OF 83	



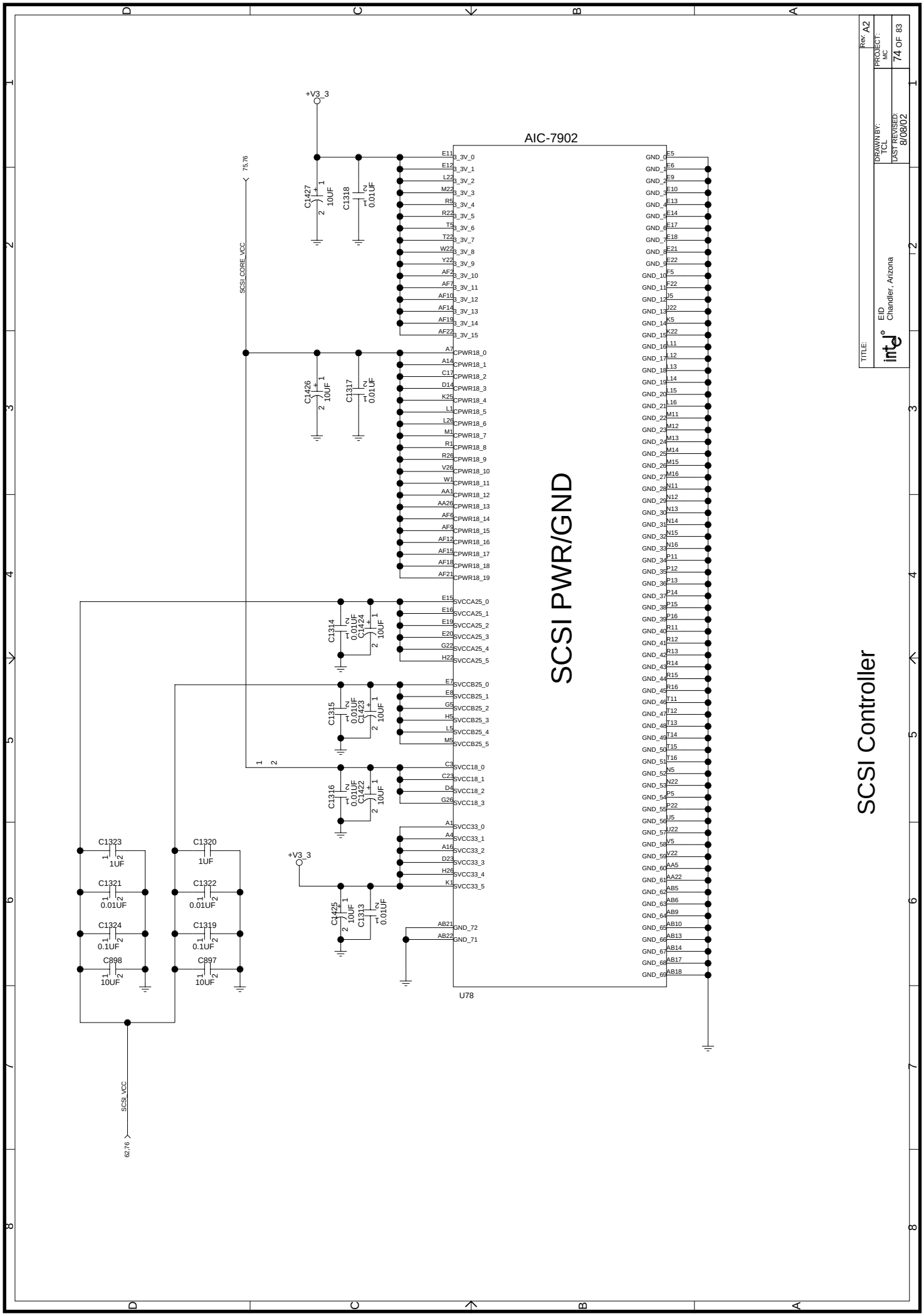
LAN EEPROM, Magnetics and Connector

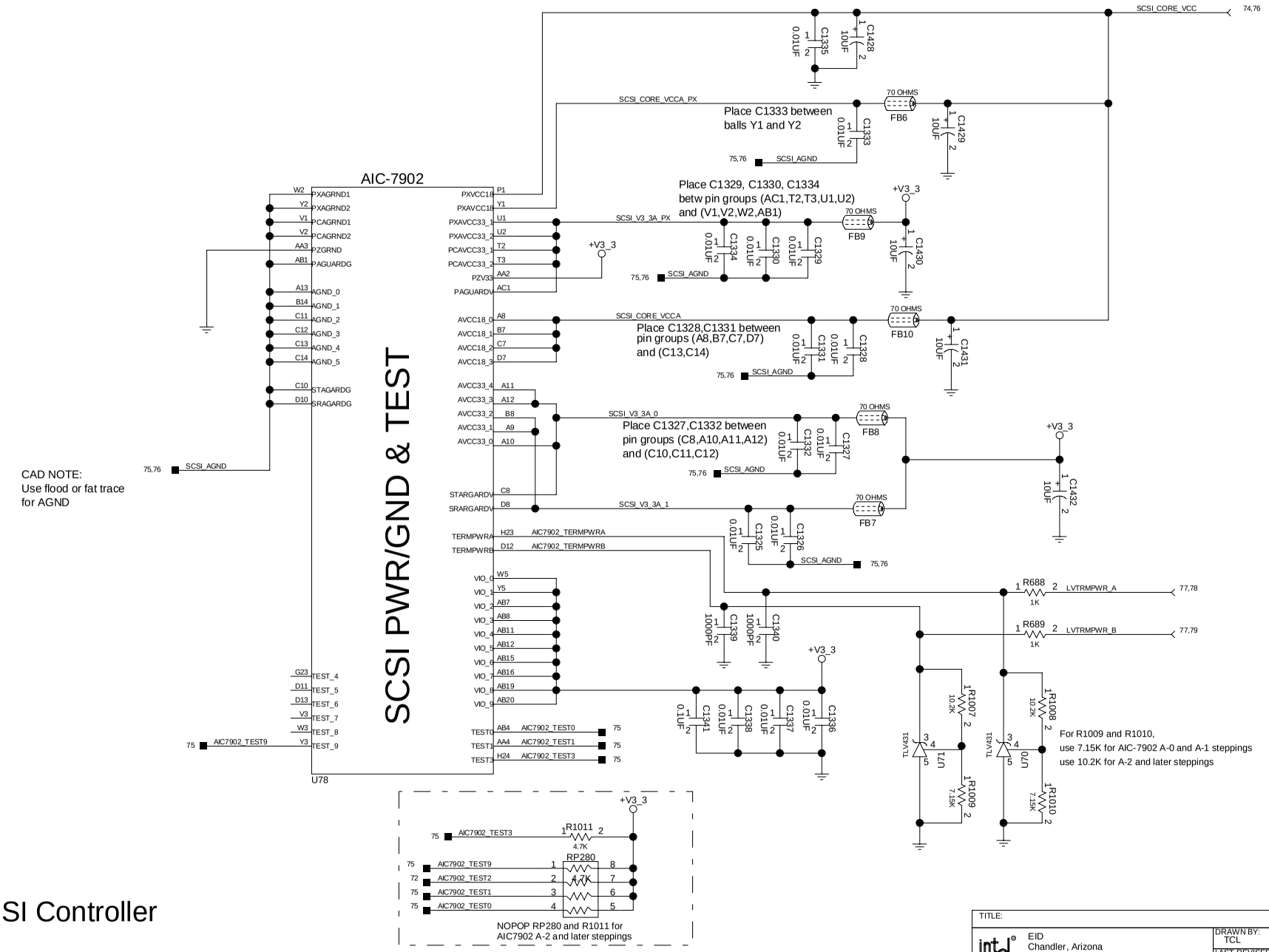
TITLE:	Rev: A2
EID Chandler, Arizona	DRAWN BY: TCL PROJECT: MC LAST REVISED: 8/08/02 71 OF 83


PCI Memory
AIC_7902
SCSI Controller
U78
P64H2_2_PA_PCLK0
P64H2_2_PA_GNT0_N
P64H2_2_PA_AD17
SCSI_IDSEL
P64H2_2_PA_AD[63:0]
R673
R679
R676
R674
R675
100
P64H2_2_PA_IRQ0
P64H2_2_PA_IRQ1
P64H2_2_PA_REQ0_N
P64H2_2_PA_ACK64_N
P64H2_2_PA_REQ64_N
P64H2_2_PA_PAR64
P64H2_2_PA_FRAME_N
P64H2_2_PA_IRDY_N
P64H2_2_PA_PAR
P64H2_2_PA_DEVSEL_N
P64H2_2_PA_TRDY_N
P64H2_2_PA_STOP_N
P64H2_2_PA_PERR_N
P64H2_2_PA_SERR_N
P64H2_2_PA_CBE7_N
P64H2_2_PA_CBE6_N
P64H2_2_PA_CBE5_N
P64H2_2_PA_CBE4_N
P64H2_2_PA_CBE3_N
P64H2_2_PA_CBE2_N
P64H2_2_PA_CBE1_N
P64H2_2_PA_CBE0_N
3.3 Volt Part ONLY
93C66_3_3V_SEEPROM
SCSI_SEECS
SCSI_SEECK
SCSI_SEEDO
SCSI_SEEDI
R677
1K
R678
2.7K
NOPOP
C1312
0.01UF
U64
+V3_3
See Adaptec* AIC-7902 Design-in Handbook for information regarding SEEPROM implementation
AIC7902_TEST2
Rev: A2
PROJECT: MC
SHEET 72 OF 83
DRAWN BY: TCL
LAST REVISED: 8/08/02
TITLE:
EID
Chandler, Arizona



TITLE:	Rev: A2
intel EID Chandler, Arizona	PROJECT: MC
DRAWN BY: TCL	73 OF 83
LAST REVISED: 8/08/02	

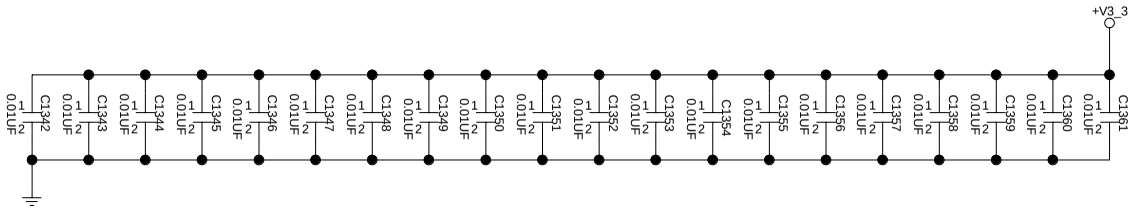

AIC-7902
SCSI PWR/GND
SCSI Controller
U78
+V3_3
SCSI_CORE_VCC
SCSI_VCC
75,76
62,76
C1427 10UF
C1318 0.01UF
C1426 10UF
C1317 0.01UF
C1314 0.01UF
C1424 10UF
C1315 0.01UF
C1423 10UF
C1316 0.01UF
C1422 10UF
C1425 10UF
C1313 0.01UF
C1323 1UF
C1320 1UF
C1321 0.01UF
C1322 0.01UF
C1324 0.1UF
C1319 0.1UF
C898 10UF
C897 10UF
3_3V_0
3_3V_1
3_3V_2
3_3V_3
3_3V_4
3_3V_5
3_3V_6
3_3V_7
3_3V_8
3_3V_9
3_3V_10
3_3V_11
3_3V_12
3_3V_13
3_3V_14
3_3V_15
CPWR18_0
CPWR18_1
CPWR18_2
CPWR18_3
CPWR18_4
CPWR18_5
CPWR18_6
CPWR18_7
CPWR18_8
CPWR18_9
CPWR18_10
CPWR18_11
CPWR18_12
CPWR18_13
CPWR18_14
CPWR18_15
CPWR18_16
CPWR18_17
CPWR18_18
CPWR18_19
SVCCA25_0
SVCCA25_1
SVCCA25_2
SVCCA25_3
SVCCA25_4
SVCCA25_5
SVCCB25_0
SVCCB25_1
SVCCB25_2
SVCCB25_3
SVCCB25_4
SVCCB25_5
SVCC18_0
SVCC18_1
SVCC18_2
SVCC18_3
SVCC33_0
SVCC33_1
SVCC33_2
SVCC33_3
SVCC33_4
SVCC33_5
GND_72
GND_71
GND_0
GND_1
GND_2
GND_3
GND_4
GND_5
GND_6
GND_7
GND_8
GND_9
GND_10
GND_11
GND_12
GND_13
GND_14
GND_15
GND_16
GND_17
GND_18
GND_19
GND_20
GND_21
GND_22
GND_23
GND_24
GND_25
GND_26
GND_27
GND_28
GND_29
GND_30
GND_31
GND_32
GND_33
GND_34
GND_35
GND_36
GND_37
GND_38
GND_39
GND_40
GND_41
GND_42
GND_43
GND_44
GND_45
GND_46
GND_47
GND_48
GND_49
GND_50
GND_51
GND_52
GND_53
GND_54
GND_55
GND_56
GND_57
GND_58
GND_59
GND_60
GND_61
GND_62
GND_63
GND_64
GND_65
GND_66
GND_67
GND_68
GND_69
TITLE:
Rev: A2
PROJECT: MC
74 OF 83
DRAWN BY: TCL
LAST REVISED: 8/08/02
EID Chandler, Arizona

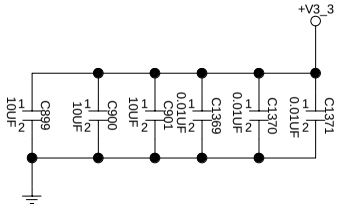


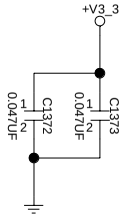
SCSI Controller

TITLE:		Rev: A2
intel EID Chandler, Arizona	DRAWN BY: TCL	PROJECT: MC
	LAST REVISED: 8/08/02	75 OF 83

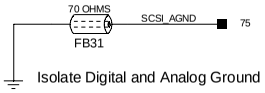
AIC-7902 SCSI Decoupling

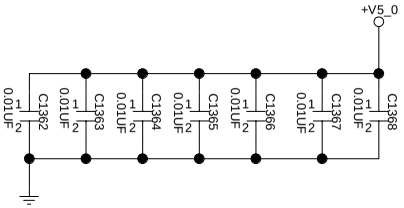




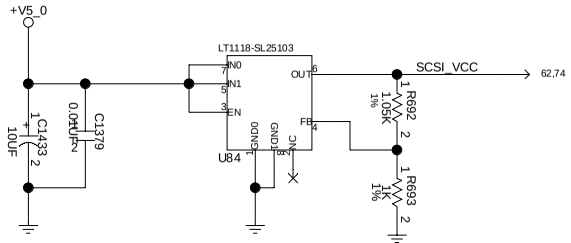


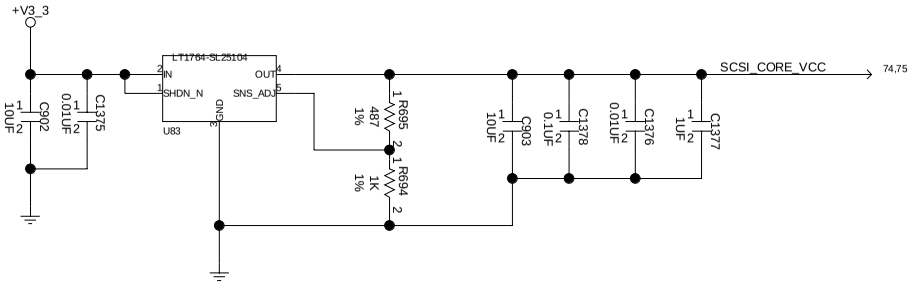
CAD NOTE:
Use flood or fat trace
for SCSI_AGND

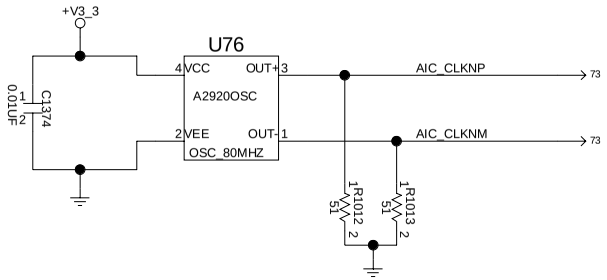




Voltage Regulators and SCSI Clock

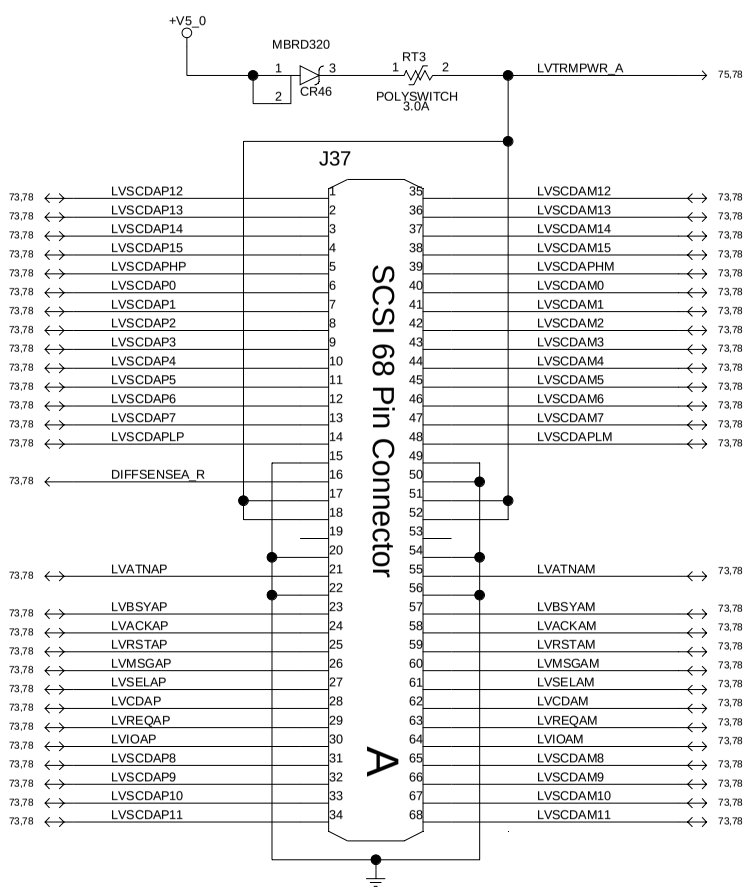


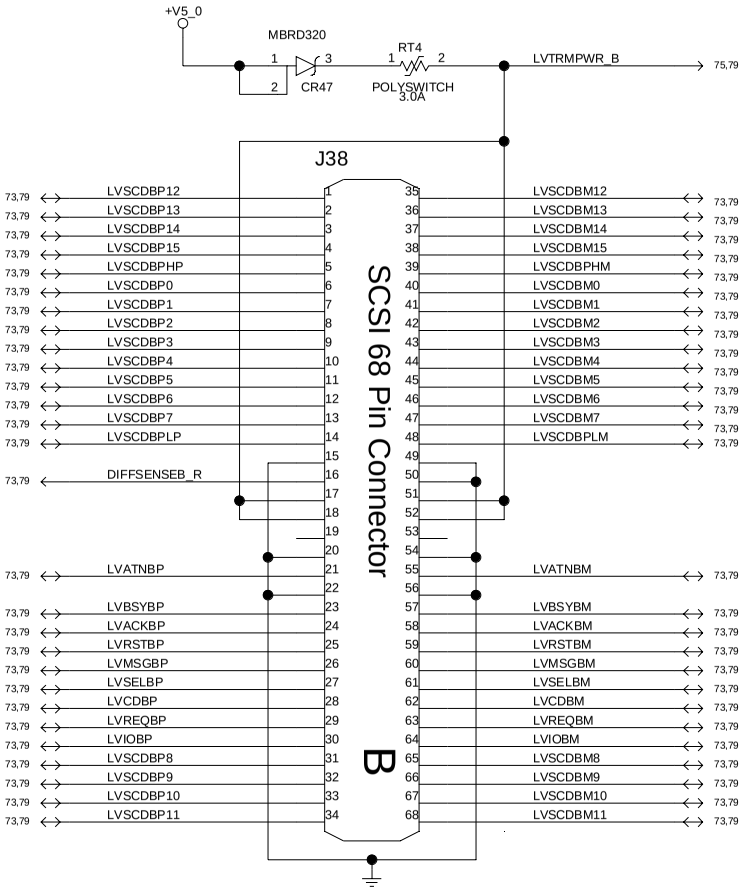




TITLE:			Rev: A2
intel EID Chandler, Arizona	DRAWN BY: TCL	PROJECT: MC	
	LAST REVISED: 8/08/02	76 OF 83	

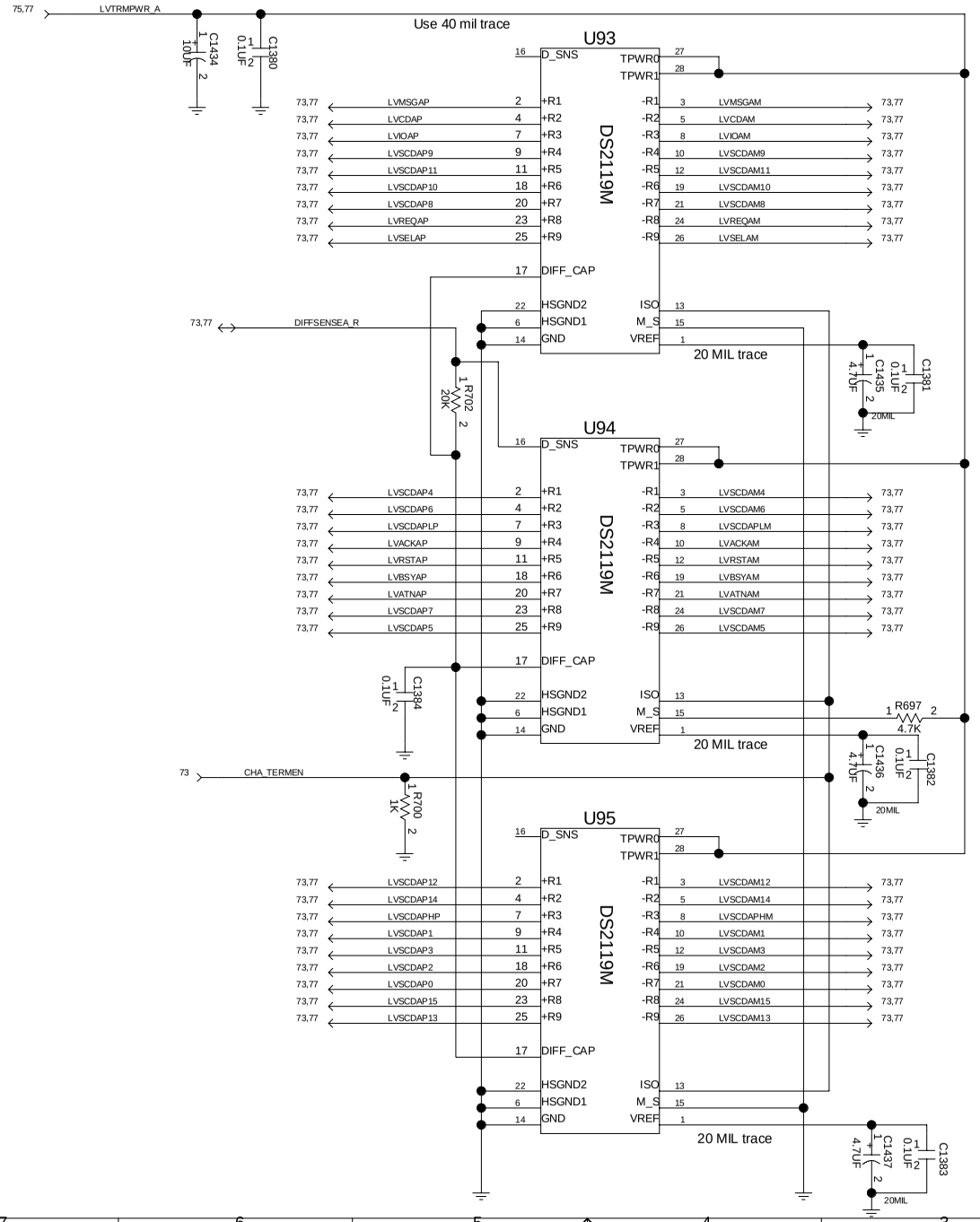
SCSI Connectors A and B





TITLE:			Rev: A2
intel EID Chandler, Arizona	DRAWN BY: TCL	PROJECT: MC	
	LAST REVISED: 8/08/02	77 OF 83	

LVD/SE Termination for SCSI Channel A



TITLE:		Rev: A2
intel EID Chandler, Arizona	DRAWN BY: TCL	PROJECT: MC
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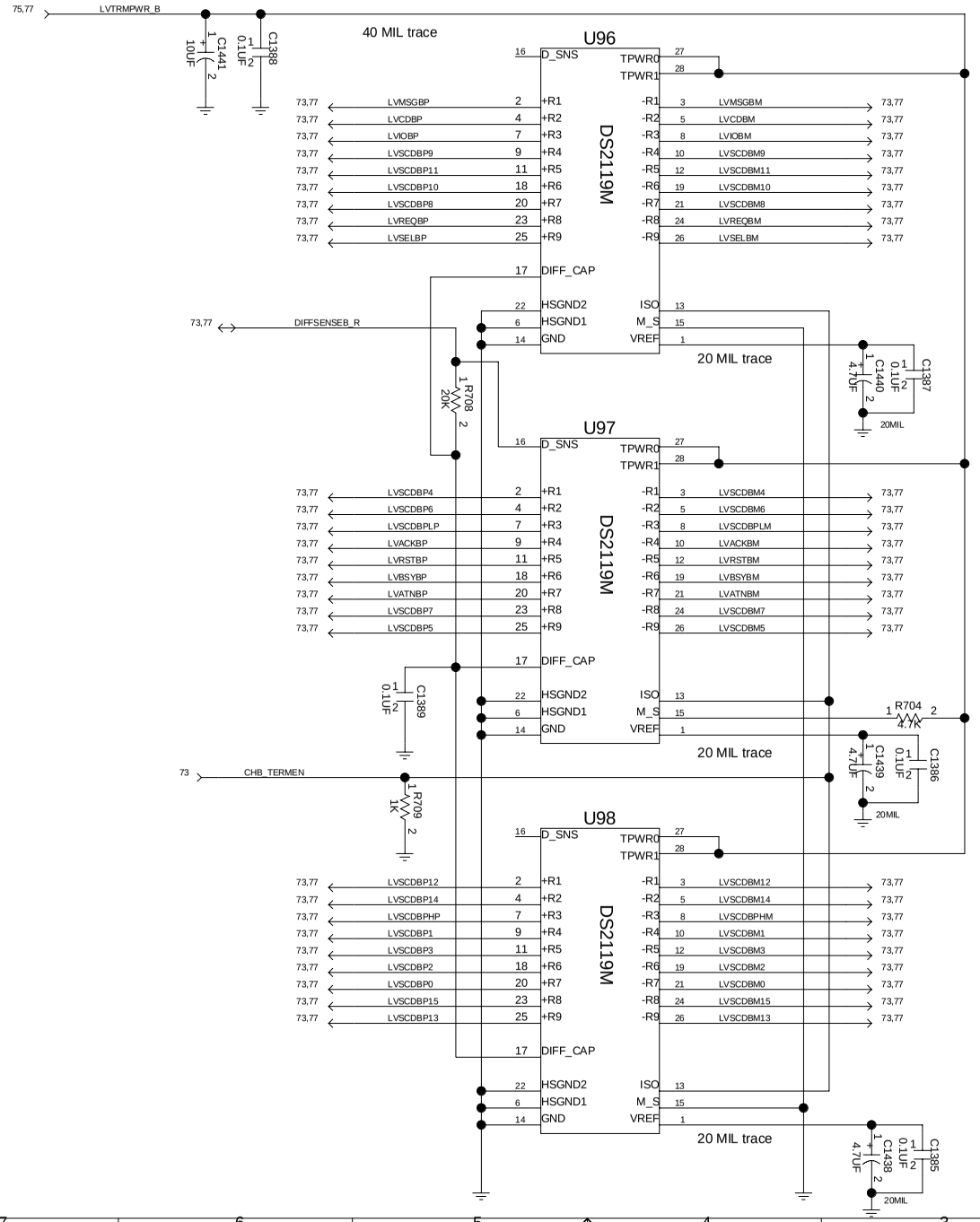
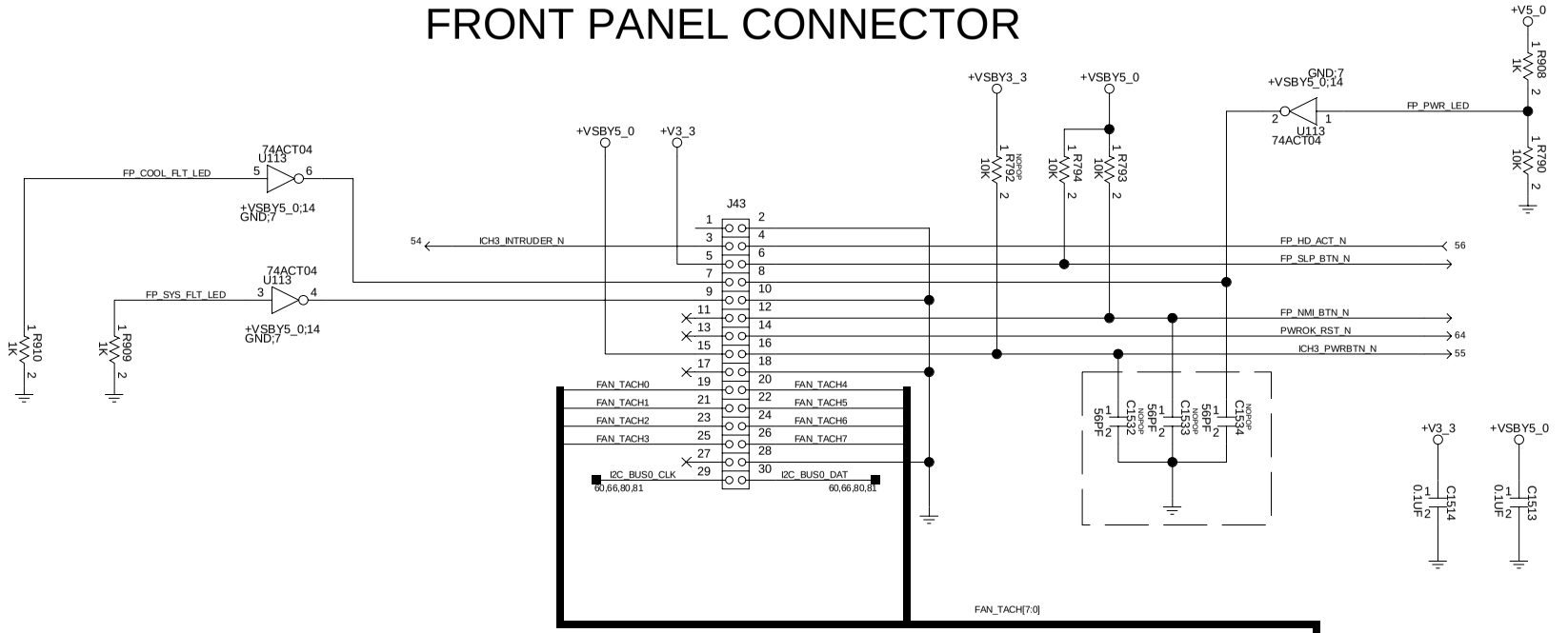
LVD/SE Termination for SCSI Channel B

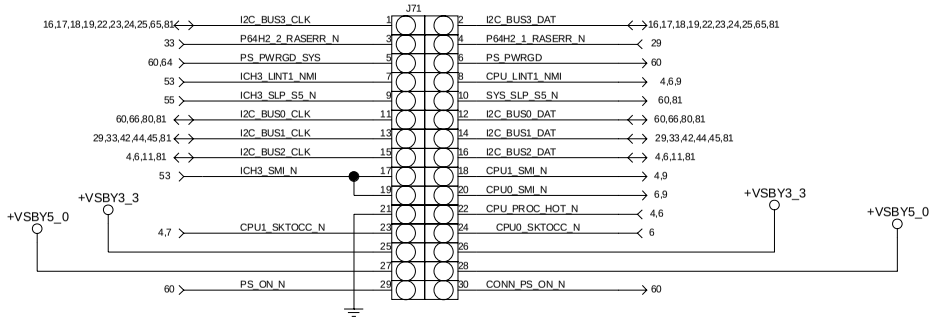


TITLE:		Rev: A2
EID Chandler, Arizona	DRAWN BY: TCL	PROJECT: MC
	LAST REVISED: 8/08/02	79 OF 83

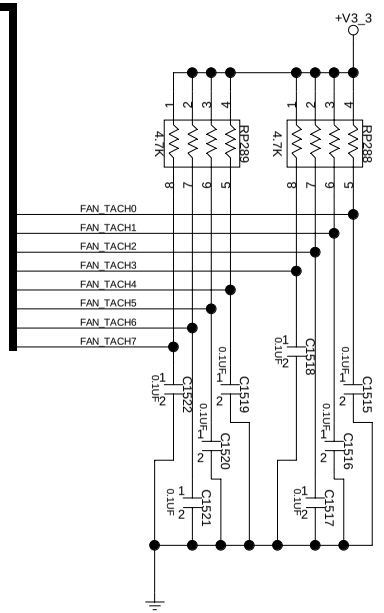
FRONT PANEL CONNECTOR



Install jumpers to short pin pairs
5 and 6, 7 and 8, 9 and 10, 17 and 18,
19 and 20, 29 and 30



BMC Connector
for validation



Pull-ups for fan tach on fan cntl board

TITLE:		Rev: A2
intel EID Chandler, Arizona	DRAWN BY: TCL	PROJECT: MC
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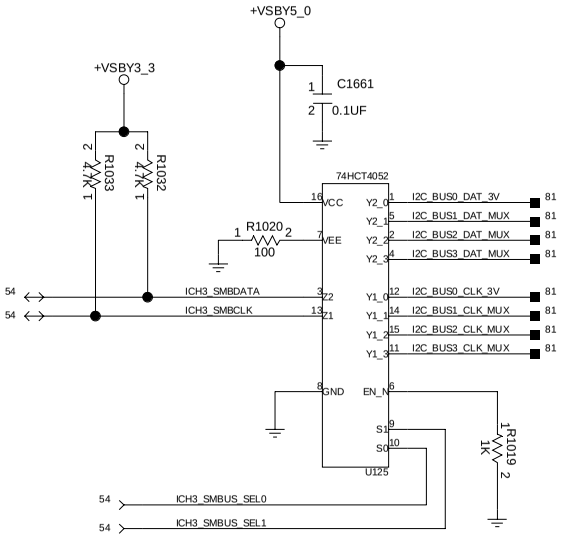
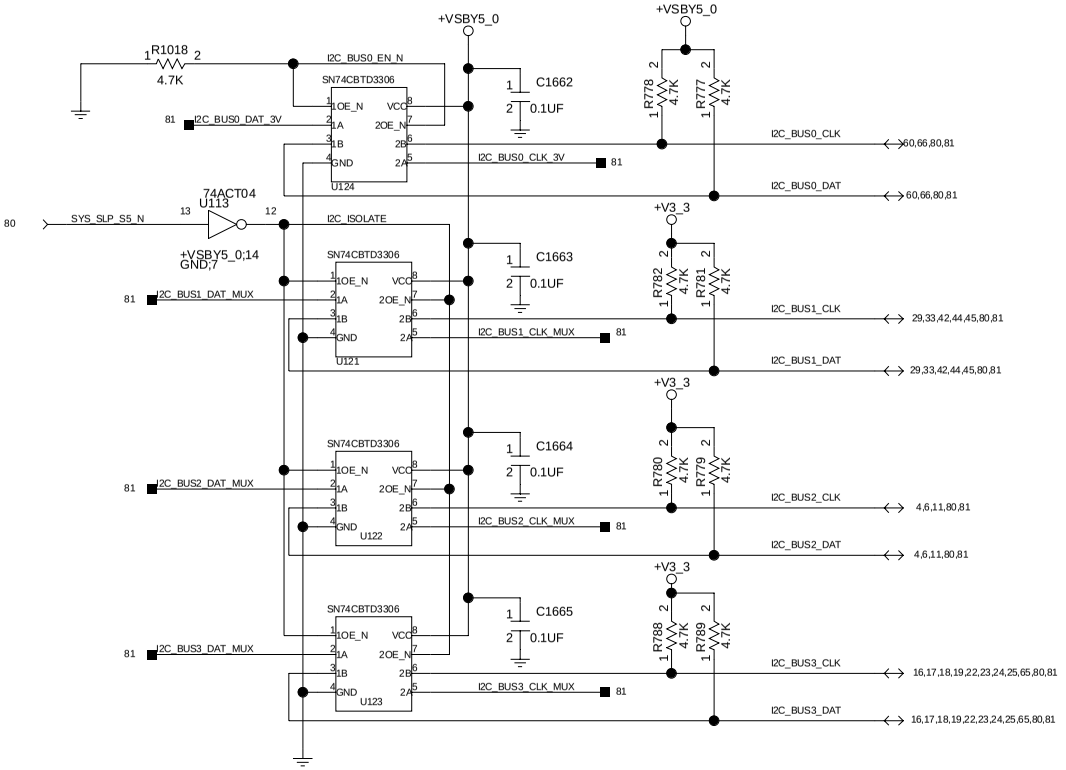
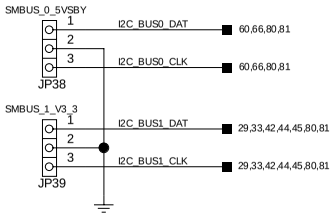
SMBus Mux

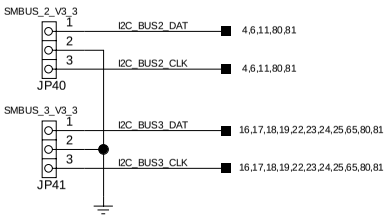


SEL1	SEL0	SMBus Partition
0	0	Bus 0
0	1	Bus 1
1	0	Bus 2
1	1	Bus 3 (default)

SMBus Isolation and Voltage Translation







TITLE:			Rev: A2
intel EID Chandler, Arizona	DRAWN BY: TCL		PROJECT: MC
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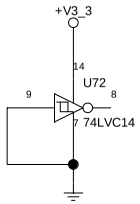
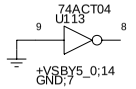
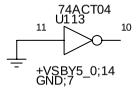
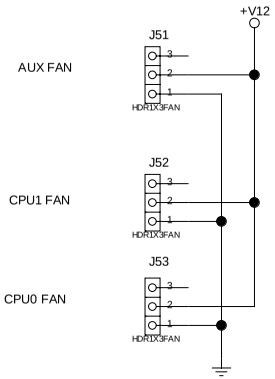
SPARE GATES

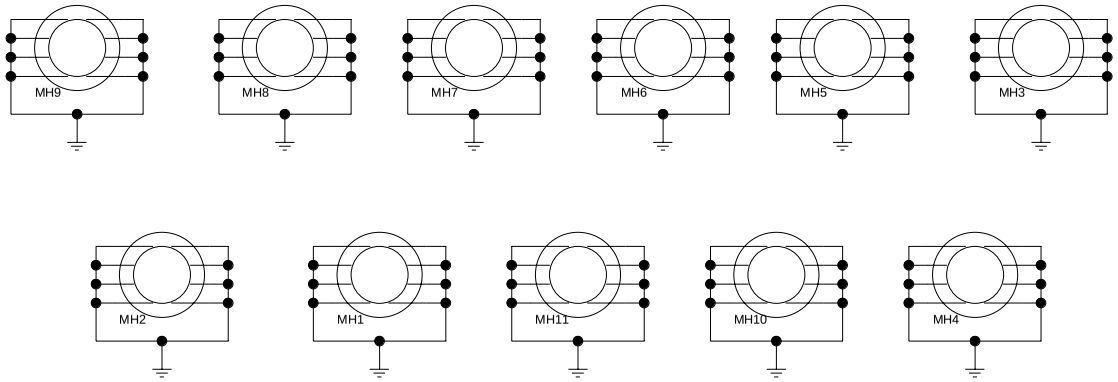




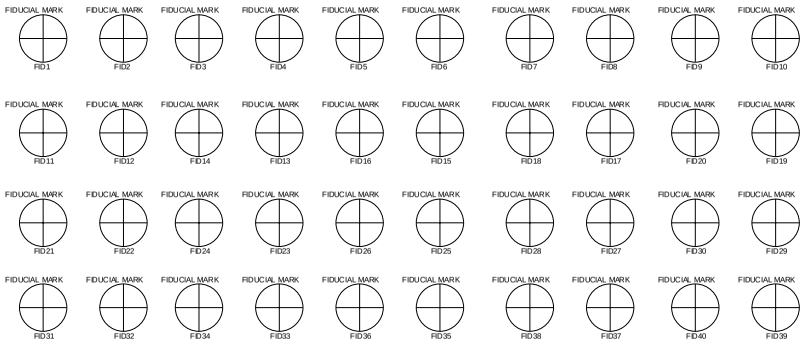




Mounting Holes



Fiducial marks



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I2C BUS 0

Partition Select 00

- Chassis Fan Board EEPROM SMB Address = AAh
- Chassis Fan Board Thermal Sensor SMB Address = 9Ah
- Chassis Fan Board 8-bit I/O (FAN_FAIL) SMB Address = 4Eh
- Chassis Fan Board 8-bit I/O (FAN_PRES) SMB Address = 46h
- Power Supply SMB Address = A6h
- Test Header JP38

+VSBY5_0

I2C BUS 1

Partition Select 01

- P64H2 #1 SMB Address = C2h
- P64H2 #2 SMB Address = C0h
- PCI-X Slot 1 SMB Address Resolution Protocol
- PCI-X Slot 2 SMB Address Resolution Protocol
- PCI-X Slot A SMB Address Resolution Protocol
- PCI-X Slot B SMB Address Resolution Protocol
- PCI-X Slot C SMB Address Resolution Protocol
- PCI-X Slot D SMB Address Resolution Protocol
- Test Header JP39
- BMC Connector J71

+V3_3

I2C BUS 2

Partition Select 10

- Processor 0 IDROM SMB Address = A0h
- Processor 1 IDROM SMB Address = A2h
- Processor 0 Thermal Sensor SMB Address = 30h
- Processor 1 Thermal Sensor SMB Address = 32h
- Plumas MCH SMB Address = 60h
- Test Header JP40
- BMC Connector J71

+V3_3

I2C BUS 3

Partition Select 11 (Default)

- DIMM A-0 SMB Address = A0h
- DIMM A-1 SMB Address = A2h
- DIMM A-2 SMB Address = A4h
- DIMM A-3 SMB Address = A6h
- DIMM B-0 SMB Address = A8h
- DIMM B-1 SMB Address = AAh
- DIMM B-2 SMB Address = ACh
- DIMM B-3 SMB Address = AEh
- CK-408B SMB Address = D2h
- Test Header JP41
- BMC Connector J71

+V3_3

MUX

ICH3-S

SMB Slave Address = 88h

SMBDATA — ICH3_SMBDATA

SMBCLK — ICH3_SMBCLK

GPIO27 — ICH3_SMBUS_SEL0

GPIO28 — ICH3_SMBUS_SEL1

NOTE:
SMBus Addresses expressed as 8-bit hex numbers assume "0" as LSB.
This is actually the Read/Write bit, and may take on either value,
depending on the nature of the transaction.

SMBUS PARTITION MAP

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