

Evaluation Platform System Electronics Board

Revision D

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History

Changes made to Revision D.

1. Added Signals PWROK(A24) +12V(A33) MB12#_R(B33) to J19A.
2. Moved J20
3. Added C229 to -PC IRST

Changes made to Revision C.

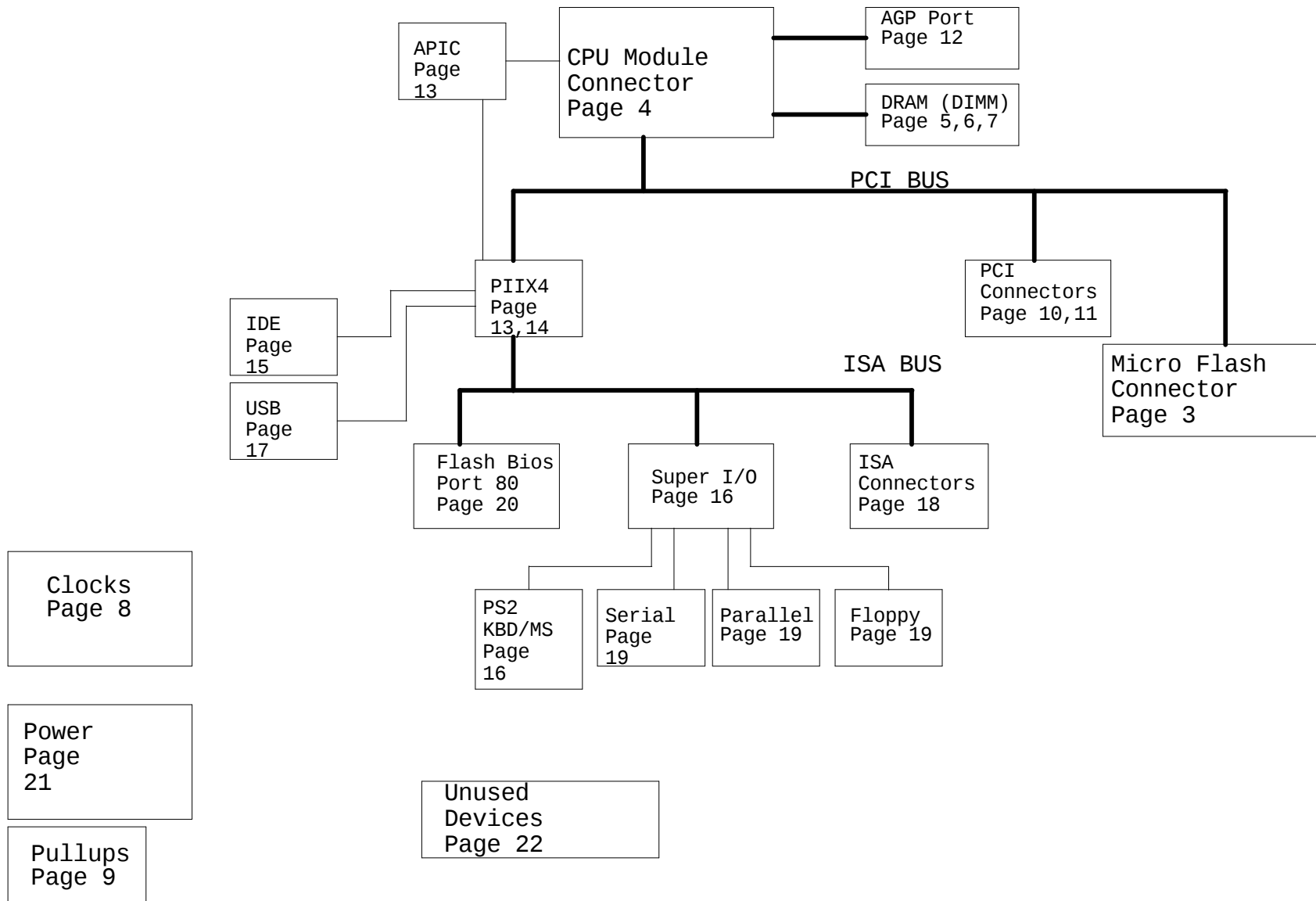
1. Tied VBAT (pin 65) to 3.3V on Super I/O.

Changes made to Revision B.

1. Swapped AD23 and AD19 on 400 pin connector.
2. Separated CSEL on IDE0 and IDE1
3. Swapped pins 1 and 3 (V5 with TP) on CPU-Fan connector.
4. Tied VBAT (pin 65) to 5.0V on Super I/O.
5. Changed RP48 to 4.7K. (Pullups for mouse and keyboard.)
6. Inverted POWERON# signal (SUSC#) from PIIX4 to control soft- on feature.
7. Changed Bulk decoupling on +12 and -12 to 2x220uF from 2x400uF.
8. Changed Bulk decoupling cap C154 from 10uF to 47uF to reduce BOM line items.

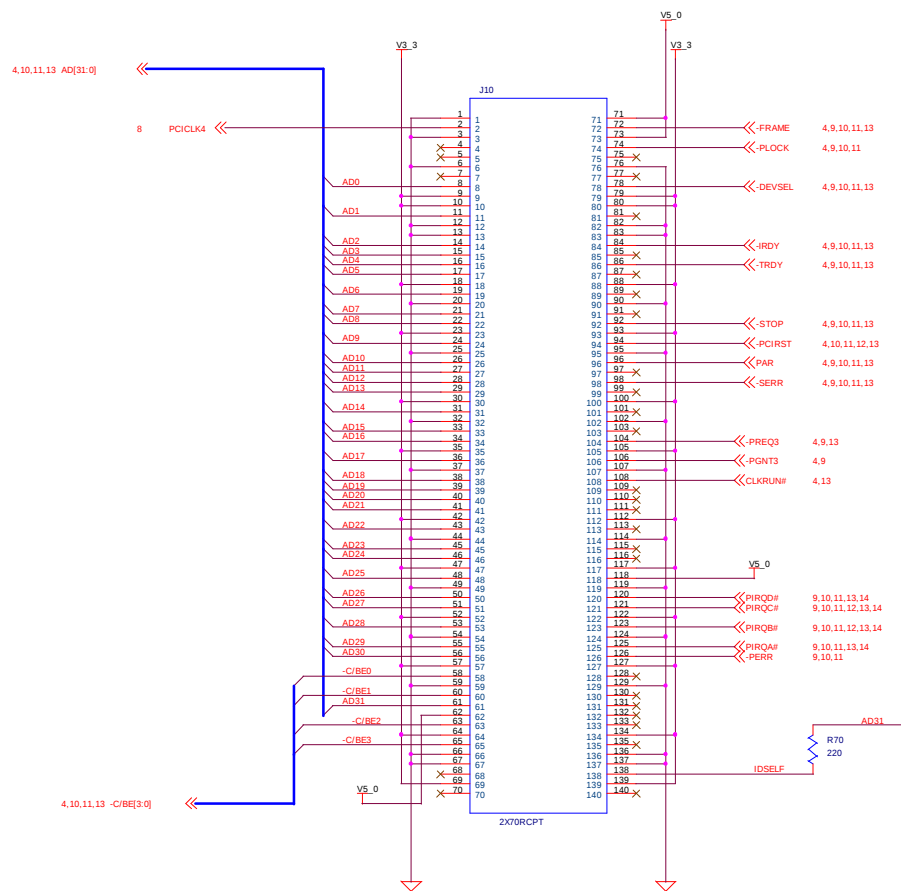
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Title		
Changes		
Size	Document Number	Rev
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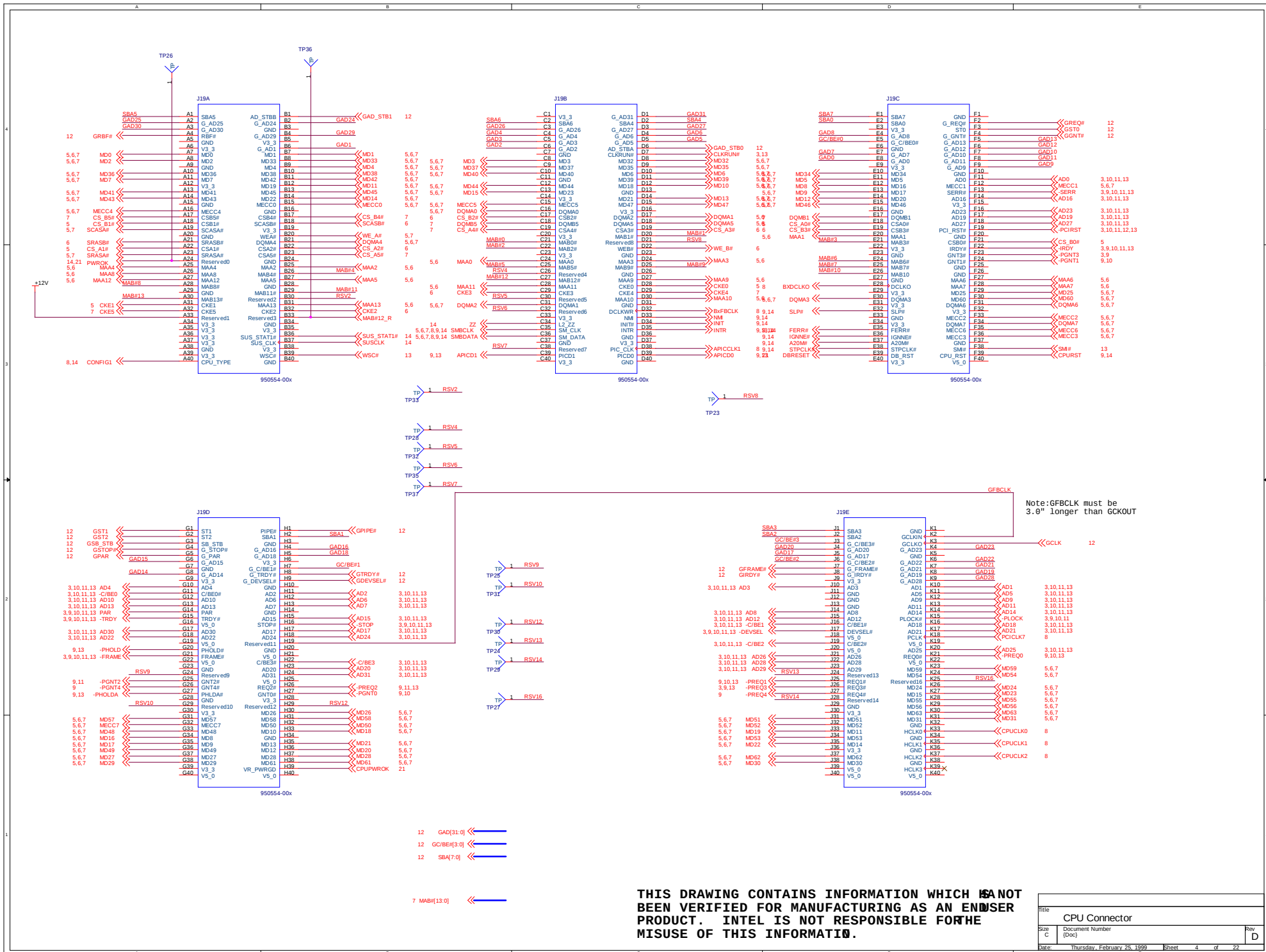
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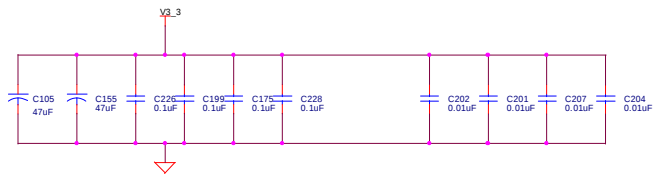
Title			
Size C	Document Number (Doc)		Rev D
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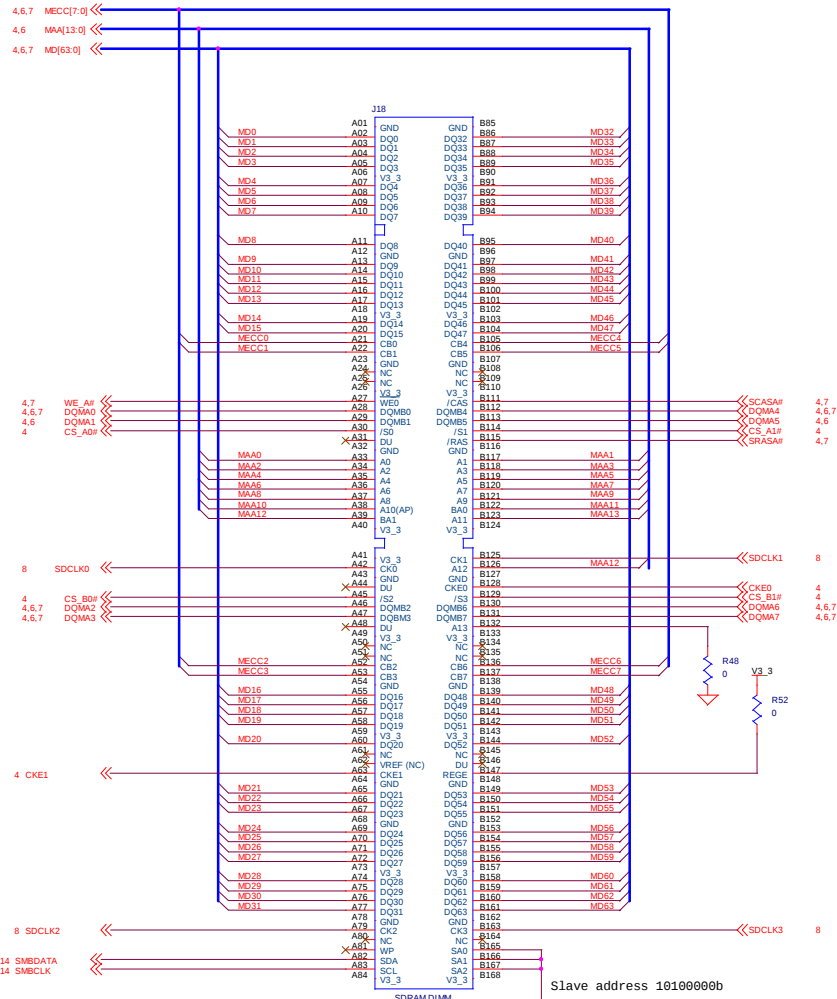
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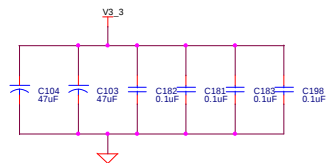
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Size	C	Document Number	
		(Doc)	
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		Rev	D



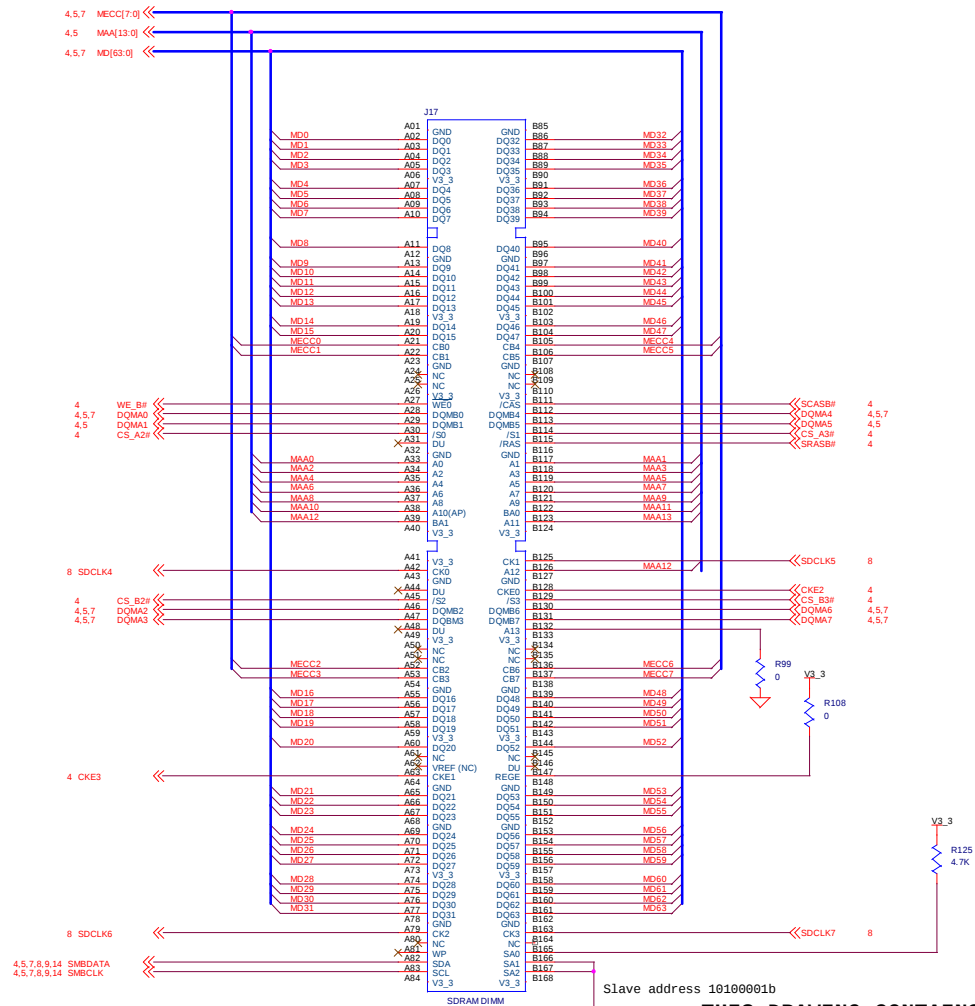


Socket 0



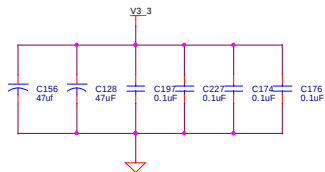


Socket 1

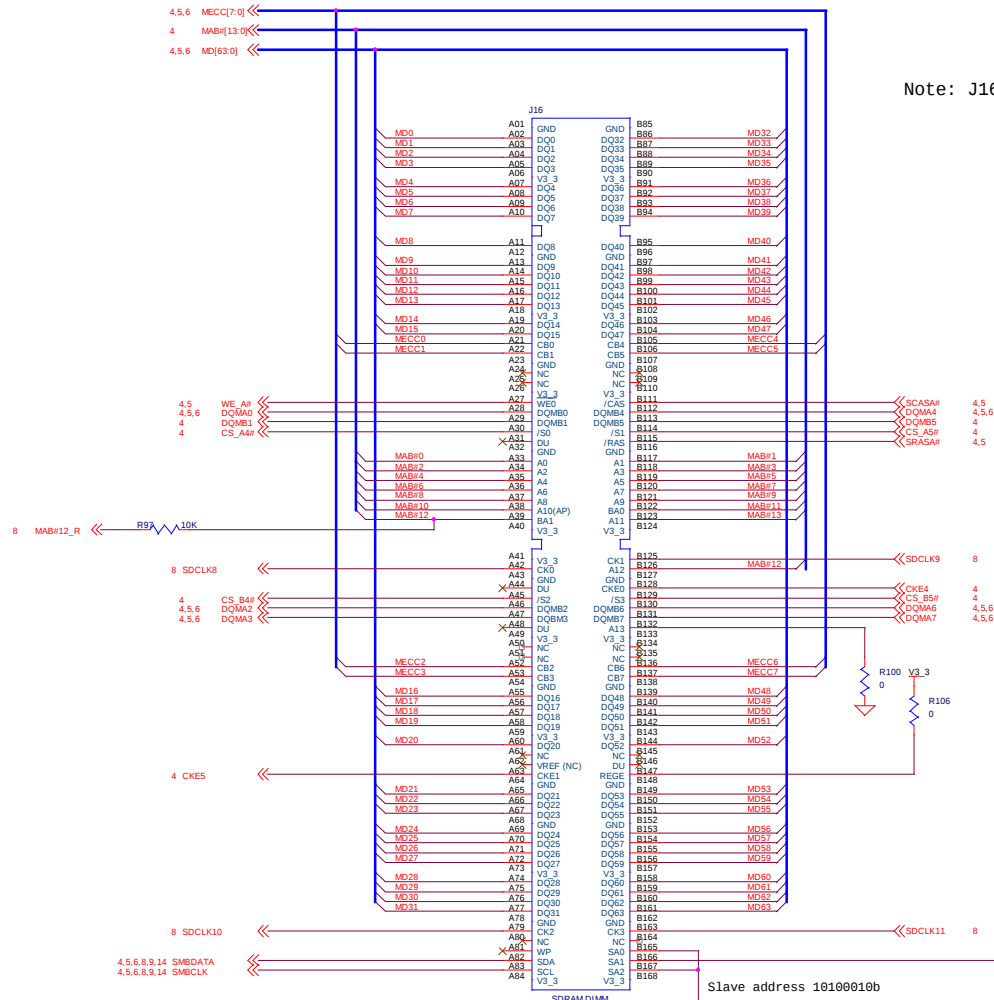


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Title		DIMM1	
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Socket 2



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Title		DIMM2	
Size	C	Document Number	(Doc)
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Rev
D

13,14,16 IRQ1
13,14,16,18 IRQ3
13,14,16,18 IRQ4
13,14,16,18 IRQ5

13,14,16,18 IRQ6
13,14,16,18 IRQ7
13,14,18 IRQ9
13,14,16,18 IRQ10

13,14,18 IRQ11
13,14,16,18 IRQ12
13,14,15,16,18 IRQ14
13,14,15,16,18 IRQ15

13,14,18 IRQ11
13,14,16,18 IRQ12
13,14,15,16,18 IRQ14
13,14,15,16,18 IRQ15

14,18 DRQ5
14,18 DRQ6
14,18 DRQ7

Title			
ISA/PCI Pullups			
Size	Document Number		Rev
C	(Doc)		D
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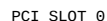
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A5, A8, A10, A16, A59, A61, A62 | A1, A3, A4
B5, B6, B19, B22, B59, B61, B62
```

A21, A27, A33, A39 A45, A53
B25, B31, B36, B41, B43, B54

A9, A11, A14, A19
B10, B14

A12, A13, A18, A24, A30, A35, A37, A42, A48, A56
B3, B12, B13, B15, B17, B28, B34, B38, B46, B49,

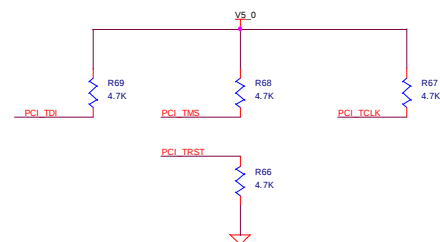
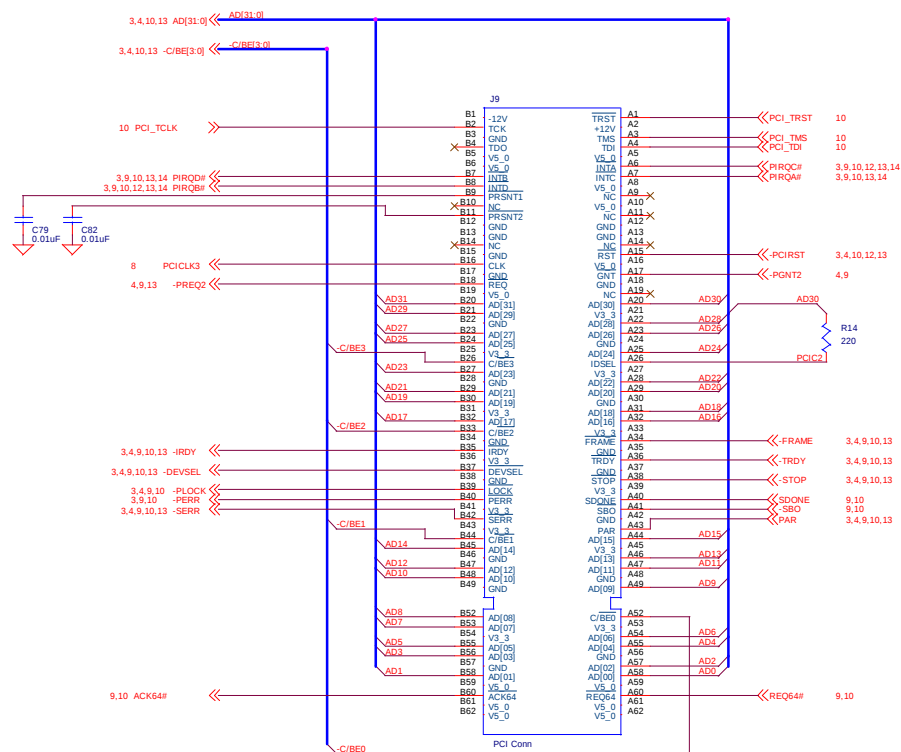
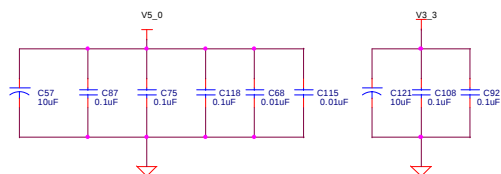
J7/J8 +12V: A2
-12V: B1



PCI SLOT 1

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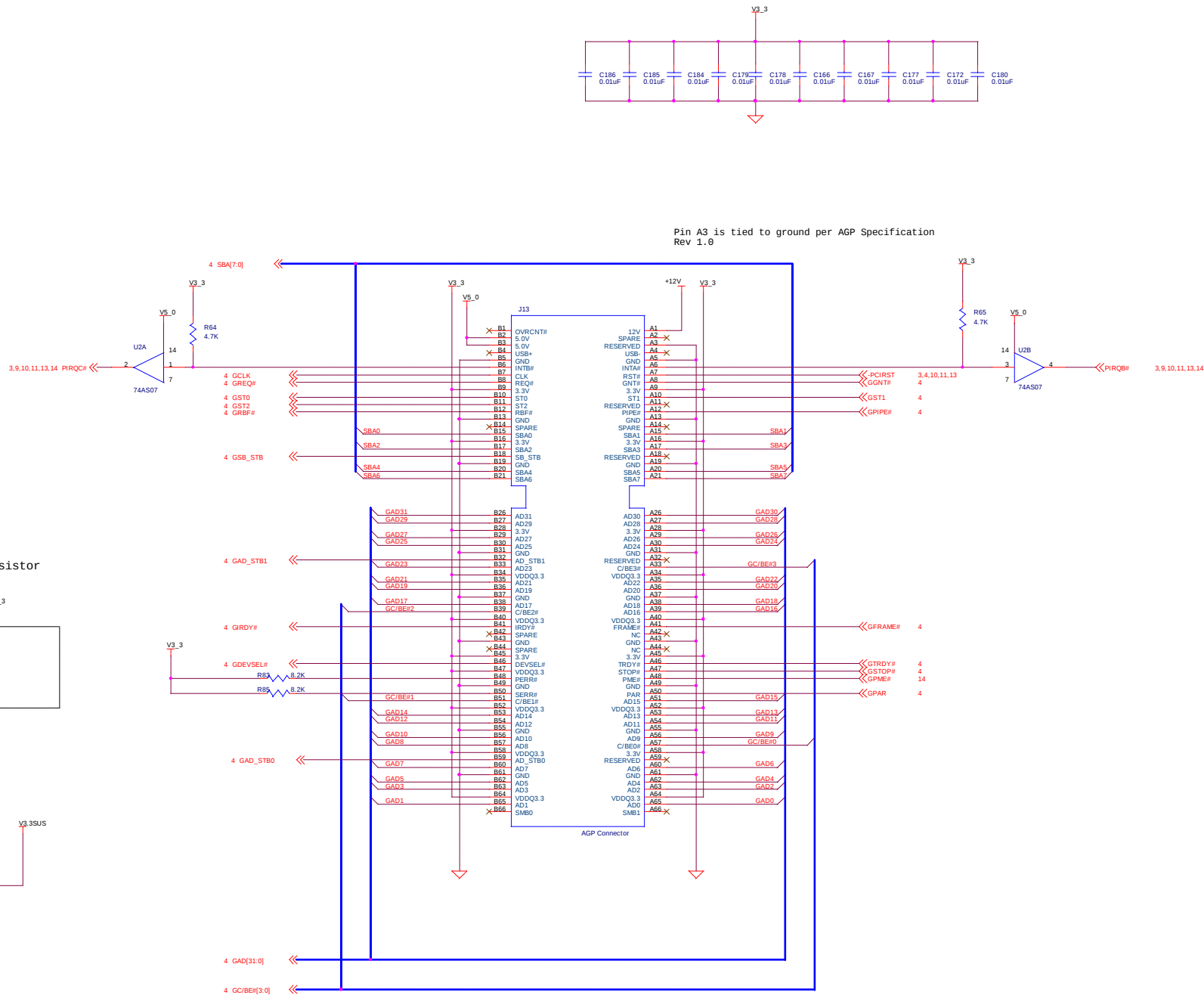
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PCI Slots 0 & 1			
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PCI SLOT 2

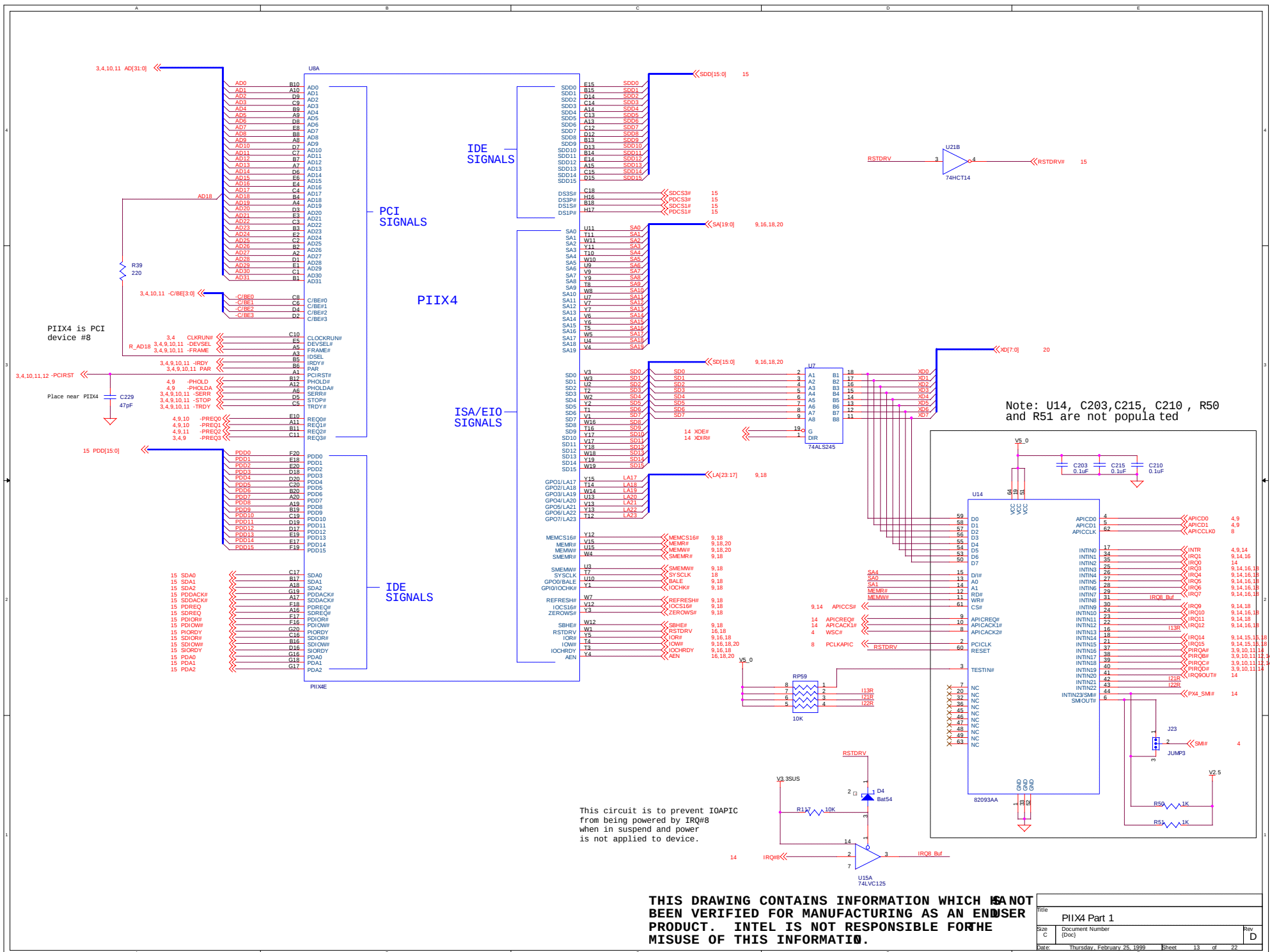
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PCI Slot 2		
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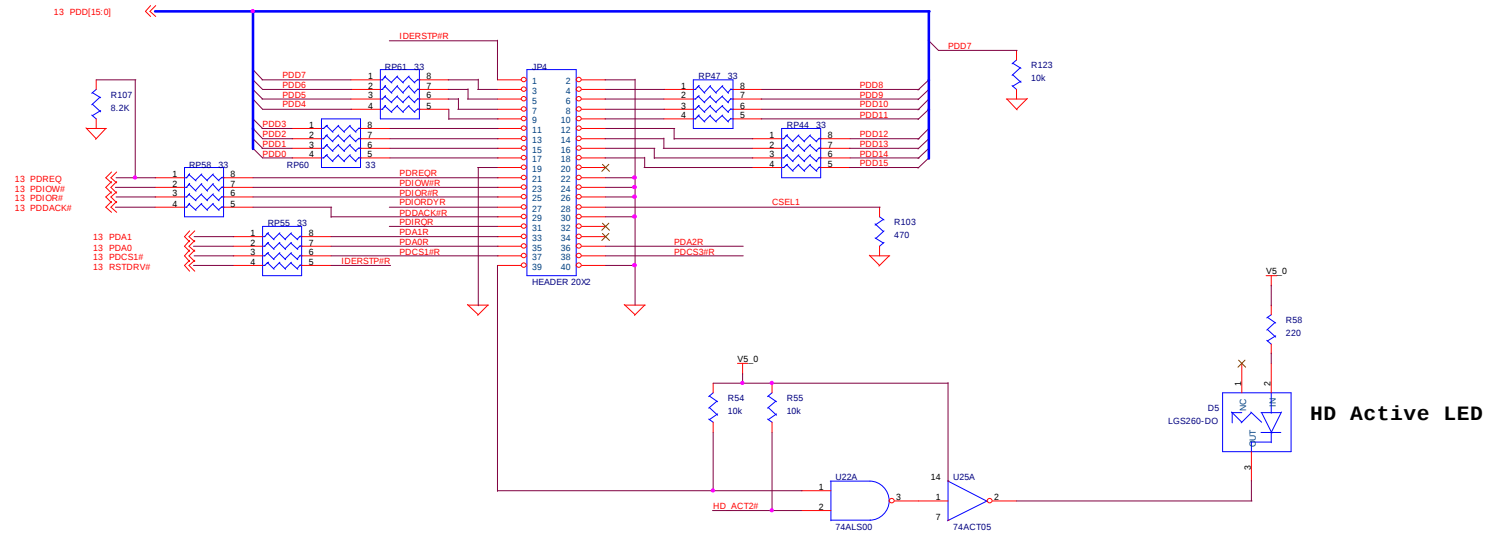
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AGP Connector		
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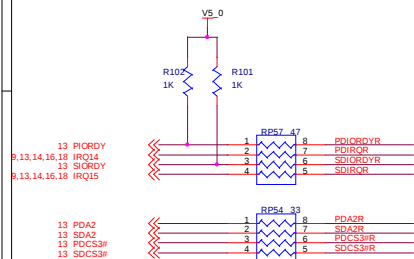
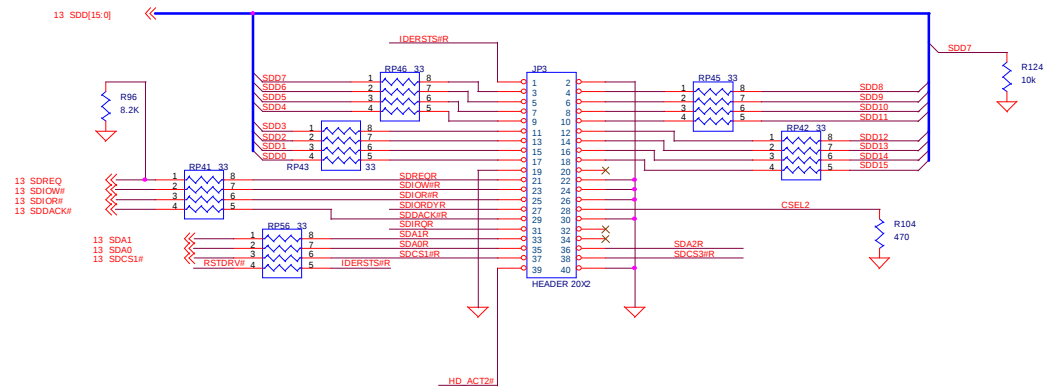


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Size	Document Number	
C	(Doc)	
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Primary IDE Connector

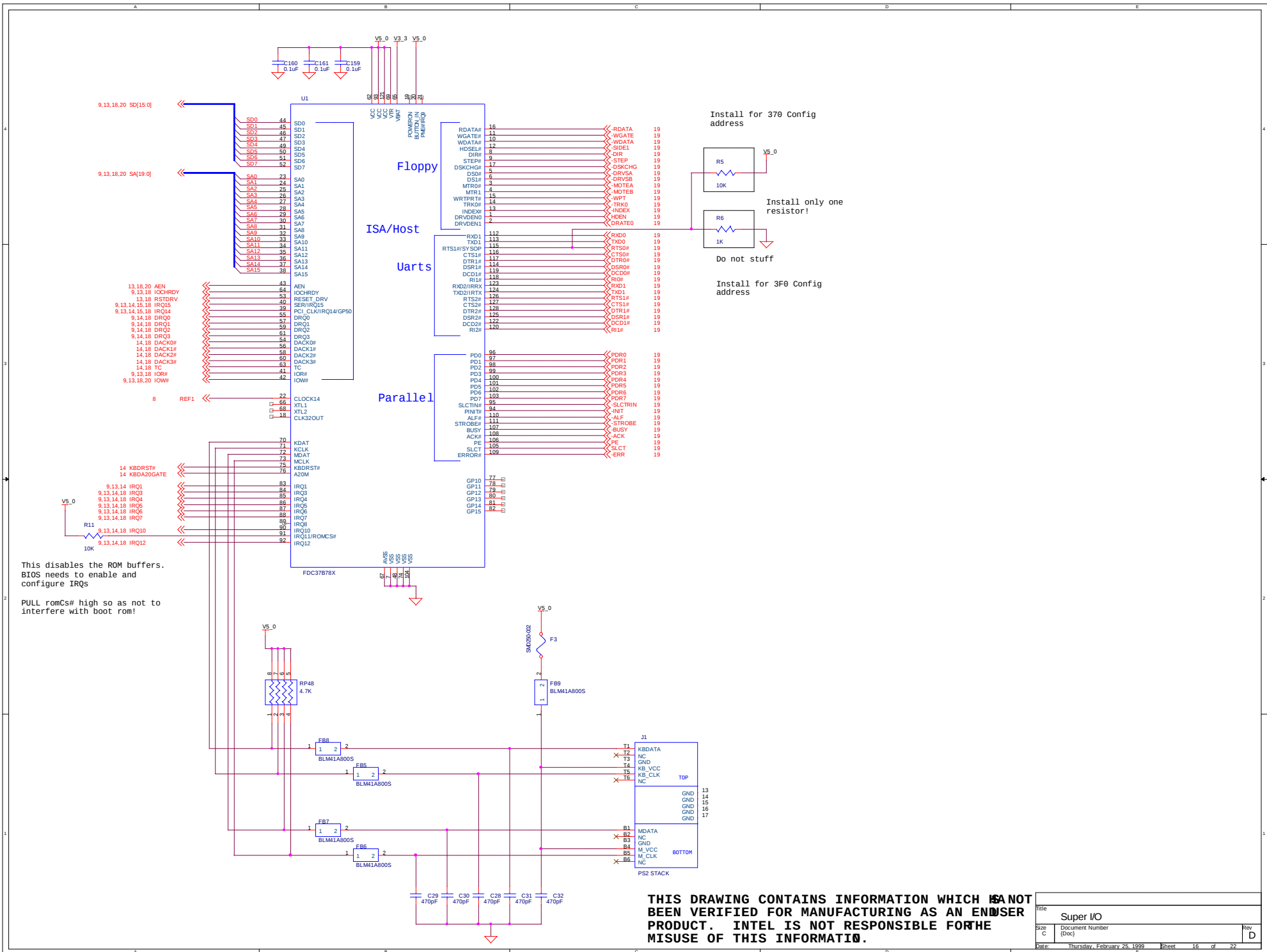


Secondary IDE Connector

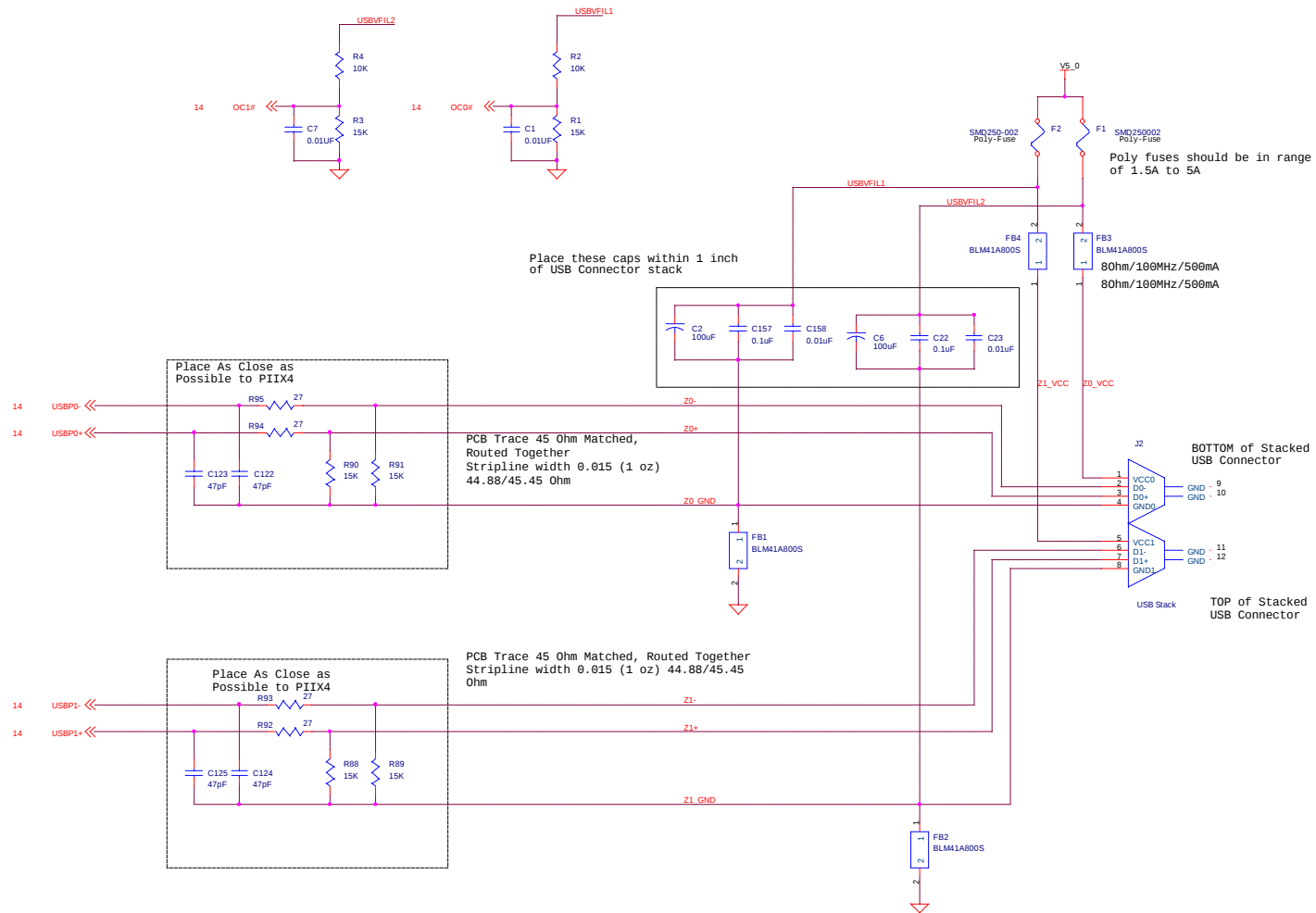


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Title			
IDE Connectors			
Size C	Document Number (Doc)		Rev D
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Title		Super I/O
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Rev	D	



NOTE 1: USB differential traces route together (Z0- & Z0+) and (Z1- & Z1+).
Must be 45 Ohm Matched
Stripline width 0.015 (for 1 oz)->44.88/45.45 Ohm.

NOTE 2: Protect differential traces w/ guard traces or
double space to any other signal.

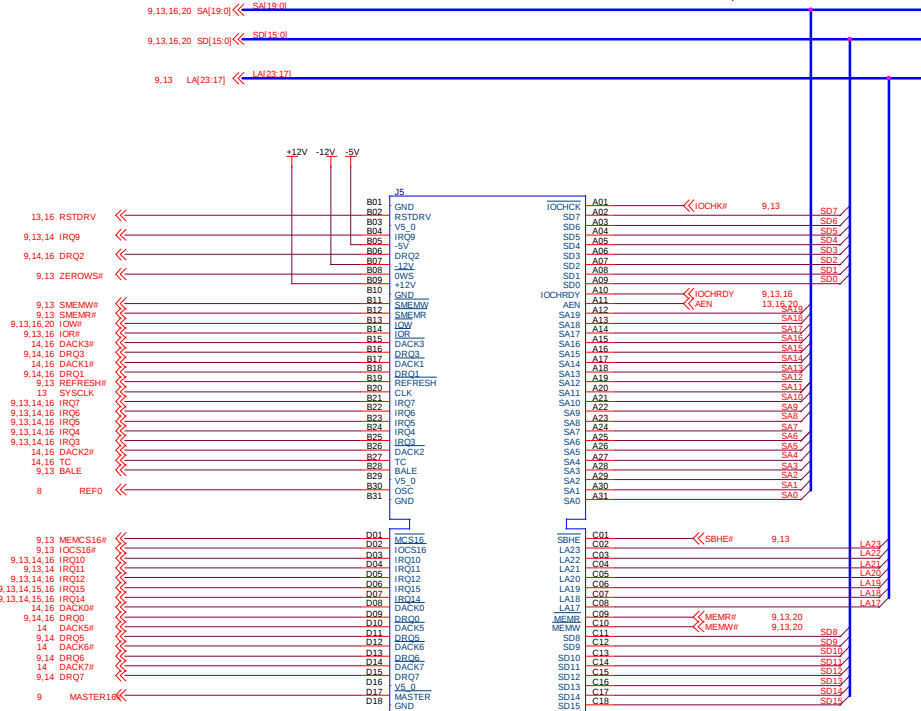
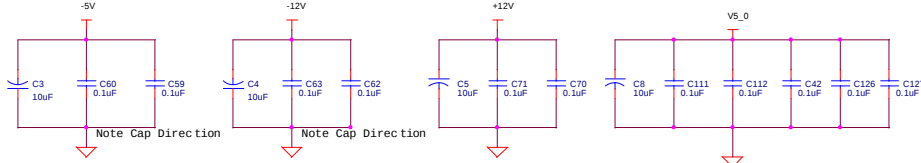
NOTE 3: Place ferrites at connector.

NOTE 4: Poly-fuse min 1.5A
max 5A.

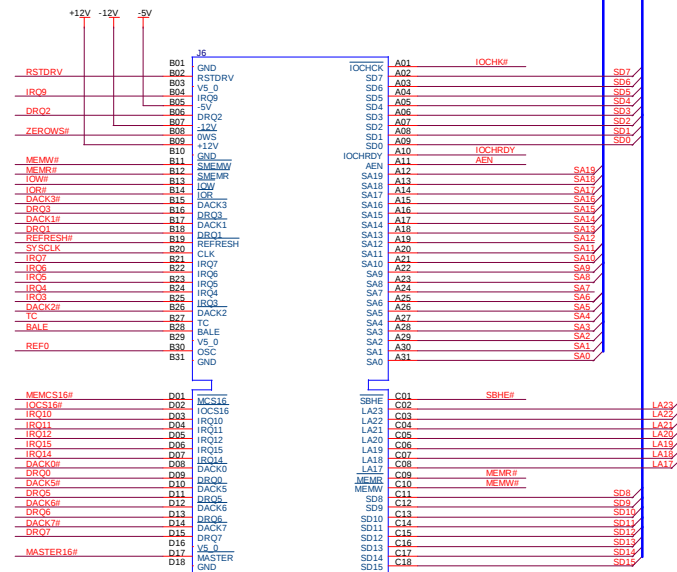
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			D

ISA Slots



ISA Conn A



ISA Conn B

J5/J6 V5_0:
B03, B29, B31, D16

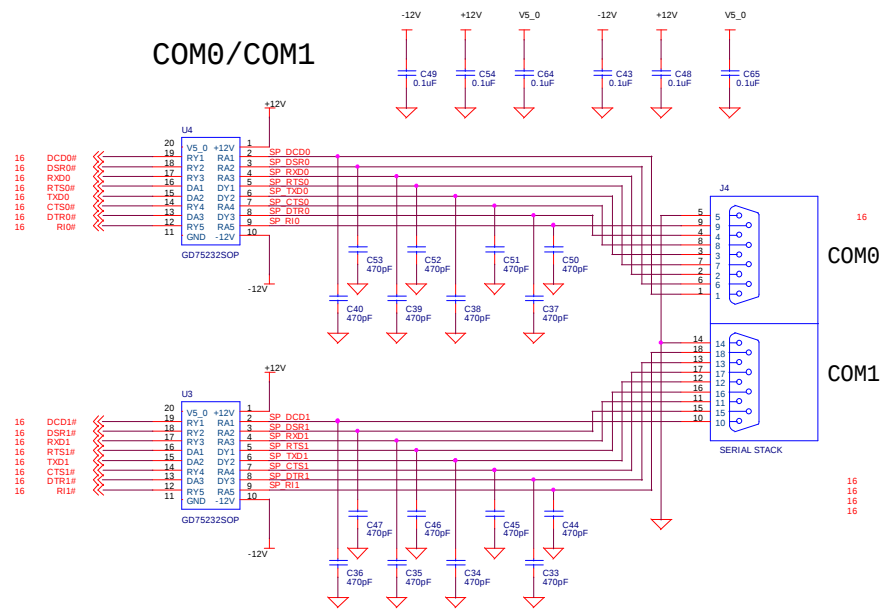
J5/J6 GND:
B01, B10, D18

J5/J6: +12V B09
-12V B07
-5V B05

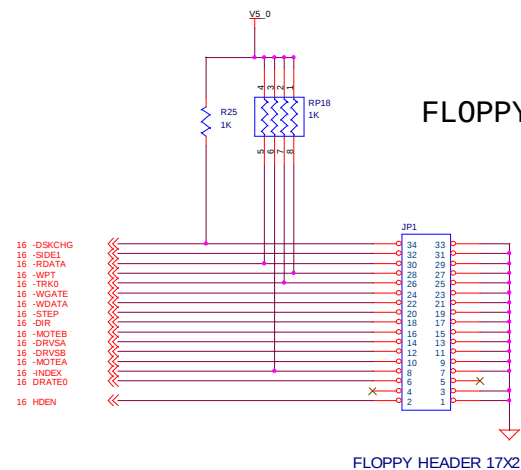
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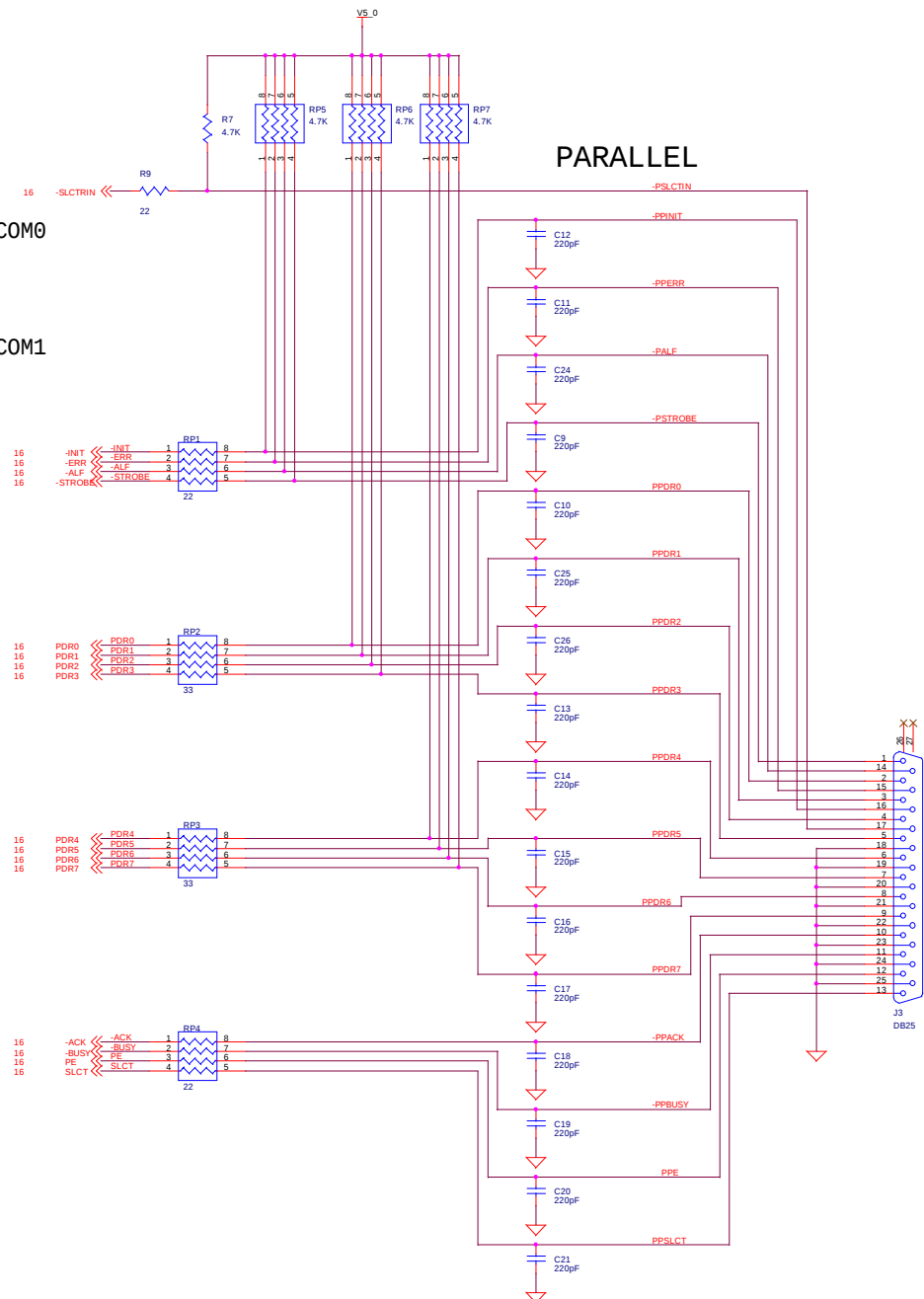
COM0/COM1



FLOPPY

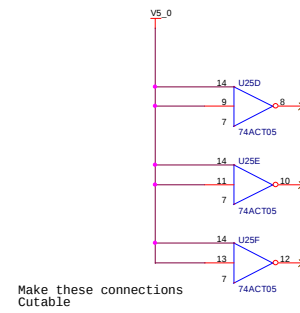
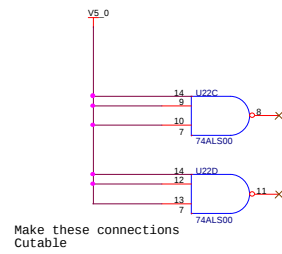
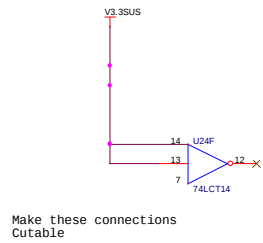
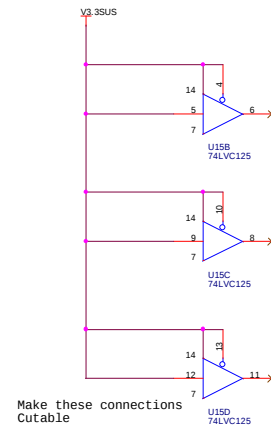
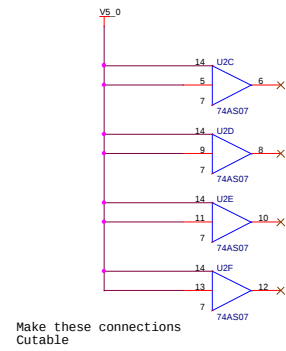
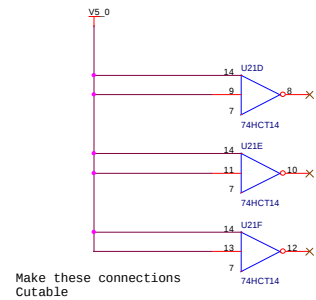


PARALLEL



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Title		
Unused Gates		
Size	Document Number	Rev
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Celeron(TM) Processor in PPGA Daughter Board

Revision
A1

History

REV A0 to REV A1 Changes

1. Removed Translator logic for PREQ0#
2. Removed Termination Resistors on BX side for GTL+
3. Added 20pF load on HCLK for BX clock compensating

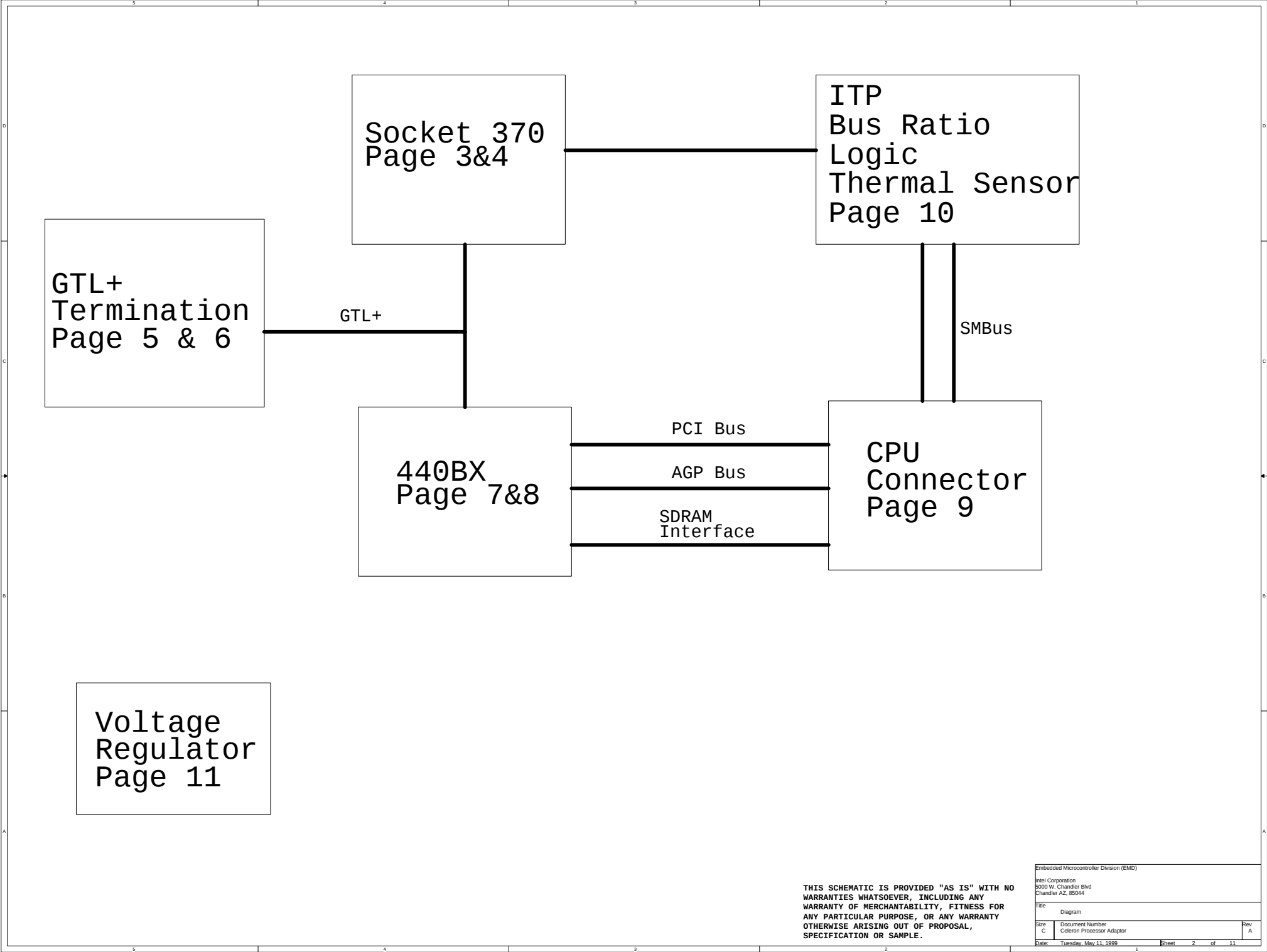
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Embedded Microcontroller Division (EMD)		
Intel Corporation 5000 W. Chandler Blvd Chandler AZ, 85044		
Title		
Title Page / Revision		
Size	Document Number	Rev
C	Celeron Processor Adaptor	A
Date: Tuesday, May 11, 1999		
Sheet 1 of 11		



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Embedded Microcontroller Division (EMD)		
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Title Diagram		
Size C	Document Number Celeron Processor Adapter	Rev A
Date: Tuesday, May 11, 1999 Sheet 2 of 11		

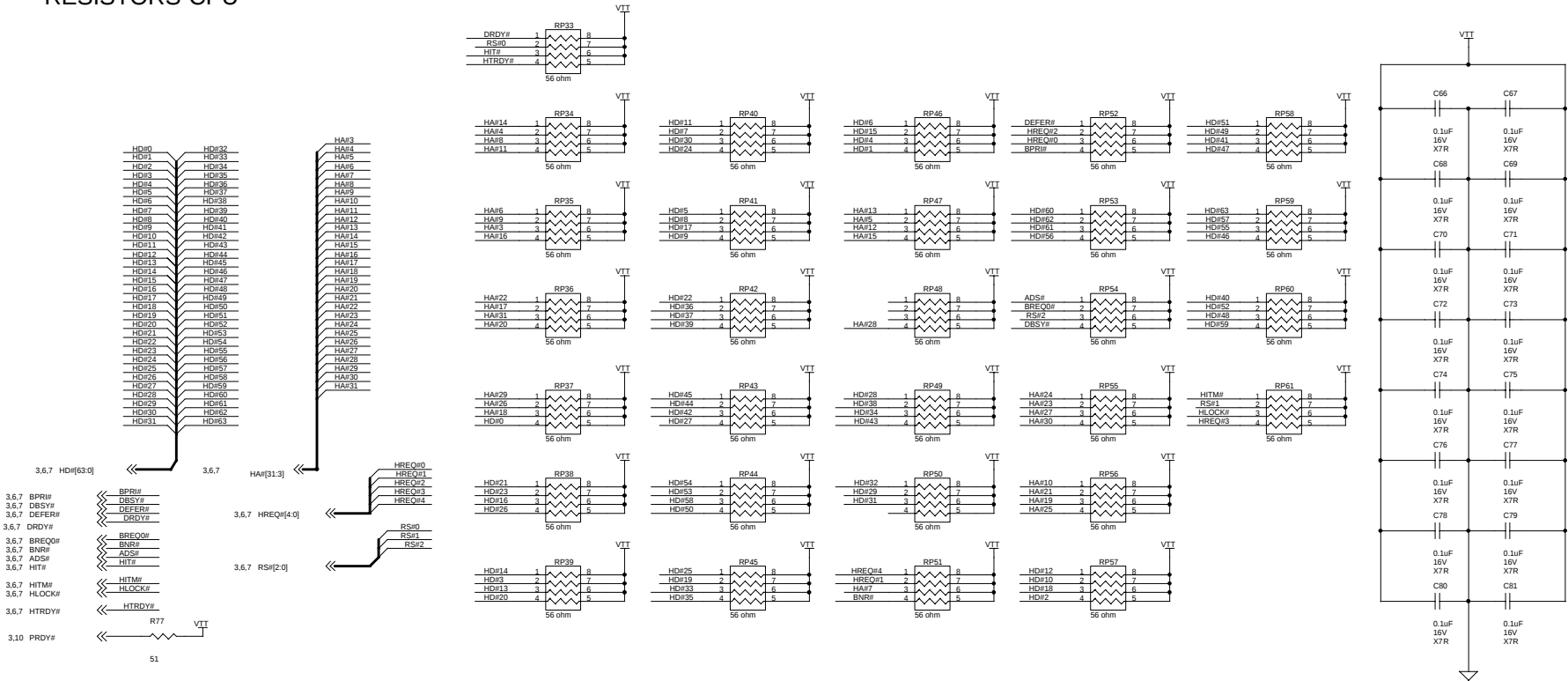
GTL+ TERMINATION
RESISTORS-BX

Resistor Packs placed for Dual End Termination.
Not used on Celeron Processor in PPGA package with
Single End Termination.

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Embedded Microcontroller Division (EMD)		
Intel Corporation 5000 W. Chandler Blvd Chandler AZ, 85044		
Title GTL Termination		
Size C	Document Number Celeron Processor Adaptor	Rev A
Date: Tuesday, May 11, 1999 Sheet 5 of 11		

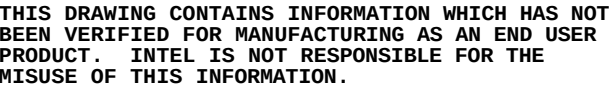
GTL+ TERMINATION RESISTORS-CPU



NOTE : VTT = TERMINATION
VOLTAGE

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Title GTL Termination		
Size C	Document Number Celeron Processor Adaptor	Rev A
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9 MD[63:0]

U4-3

MD0 AE4 MD0
MD1 AE4 MD1
MD2 AE5 MD2
MD3 AD6 MD3
MD4 AE5 MD4
MD5 AB7 MD5
MD6 AC7 MD6
MD7 AB8 MD7
MD8 AB8 MD8
MD9 AB9 MD9
MD10 AC9 MD10
MD11 AE9 MD11
MD12 AB10 MD12
MD13 AC10 MD13
MD14 AE10 MD14
MD15 AD11 MD15
MD16 Y24 MD16
MD17 V25 MD17
MD18 W23 MD18
MD19 W24 MD19
MD20 W25 MD20
MD21 W26 MD21
MD22 V26 MD22
MD23 U24 MD23
MD24 U23 MD24
MD25 T22 MD25
MD26 T23 MD26
MD27 T26 MD27
MD28 R24 MD28
MD29 R25 MD29
MD30 P23 MD30
MD31 V25 MD31
MD32 AC5 MD32
MD33 AE5 MD33
MD34 AB6 MD34
MD35 AC6 MD35
MD36 AB7 MD36
MD37 AE7 MD37
MD38 AE7 MD38
MD39 AC8 MD39
MD40 AD8 MD40
MD41 AE8 MD41
MD42 AB8 MD42
MD43 AE9 MD43
MD44 AD10 MD44
MD45 AE10 MD45
MD46 AB11 MD46
MD47 AC11 MD47
MD48 Y24 MD48
MD49 V26 MD49
MD50 W22 MD50
MD51 V22 MD51
MD52 V24 MD52
MD53 V25 MD53
MD54 U22 MD54
MD55 U26 MD55
MD56 U26 MD56
MD57 T24 MD57
MD58 T25 MD58
MD59 U21 MD59
MD60 R24 MD60
MD61 R26 MD61
MD62 P24 MD62
MD63 P25 MD63

82443BX
492 BGA

MEMORY INTERFACE

CSA0#RASA0#
CSA1#RASA1#
CSA2#RASA2#
CSA3#RASA3#
CSA4#RASA4#
CSA5#RASA5#
CSB0#RASB0#
CSB1#RASB1#
CSB2#RASB2#
CSB3#RASB3#
CSB4#RASB4#
CSB5#RASB5#
DQMA0/CASA0#
DQMA1/CASA1#
DQMA2/CASA2#
DQMA3/CASA3#
DQMA4/CASA4#
DQMA5/CASA5#
DQMA6/CASA6#
DQMA7/CASA7#
DQMB1/CASB1#
DQMB5/CASB5#
CKE0#FENA
CKE1#GCKE
CKE2#CSA6
CKE3#SAT
CKE4#CSB6
CKE5#CSB7
SCASAF
SCASBF
SRASAF
SRASBF
WEAF
WEBF
DCLKWR
DCLK0

AD16 MAB#0
AD16 MAB#1
AD17 MAB#2
AD17 MAB#3
AD18 MAB#4
AD18 MAB#5
AD18 MAB#6
AD18 MAB#7
AD20 MAB#8
AD20 MAB#9
AD20 MAB#10
AD21 MAB#11
AD21 MAB#12
AD22 MAB#13
AB14 CSA#
AE15 CSA1#
AE15 CSA2#
AD15 CSA3#
AE16 CSA4#
AE16 CSA5#
AD25 CSB0#
AD24 CSB1#
AD26 CSB2#
AE17 CSB3#
AE16 CSB4#
AE23 CSB5#
AD13 DQMA0
AC13 DQMA1
AC25 DQMA2
AD26 DQMA3
AE14 DQMA4
AC14 DQMA5
AD22 DQMA6
AA24 DQMA7
AE13 DQMB1
AD14 DQMB5
AC22 CKE0
AE23 CKE1
AE24 CKE2
AD23 CKE3
AC23 CKE4
AE24 CKE5
AE12 SCASAF
AB13 SCASBF
AE16 SRASAF
AA17 SRASBF
AE12 WEAF
AC12 WEBF
AD25 DCLKWR
AB21 DCLK0

MAA[13:0]

MAA0
MAA1
MAA2
MAA3
MAA4
MAA5
MAA6
MAA7
MAA8
MAA9
MAA10
MAA11
MAA12
MAA13

MAB#10
MAB#11
MAB#12
MAB#13

DQMA[7:0]

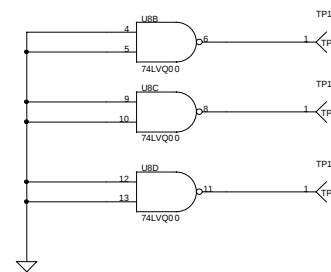
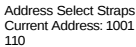
9 BXDCLK0

V3_3

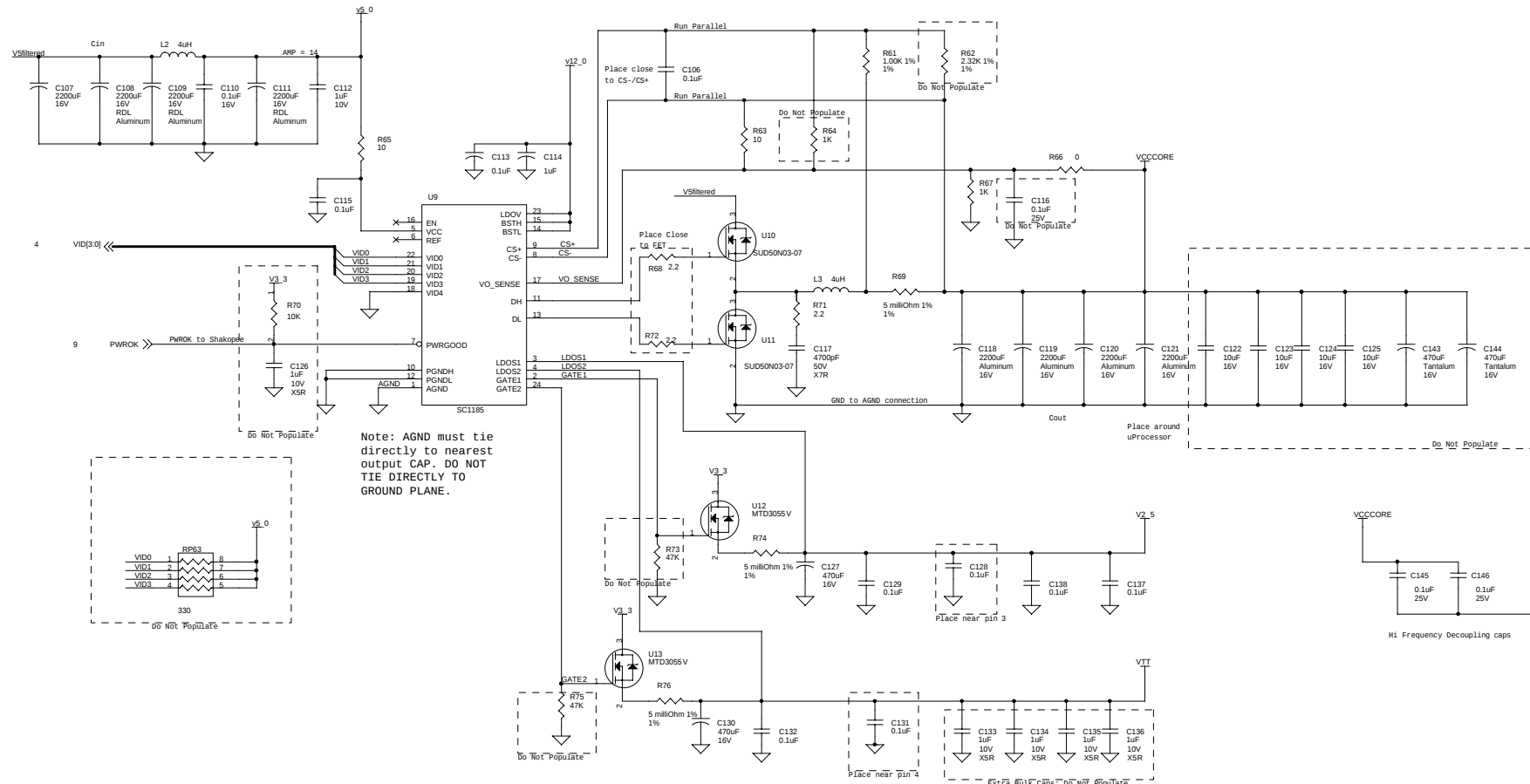
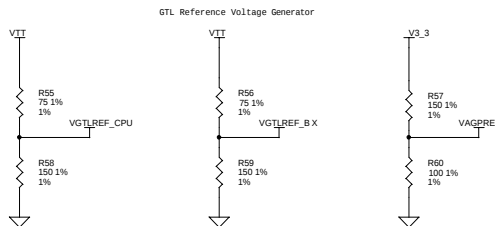
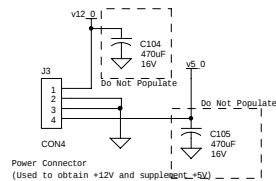
U4-4

82443BX
492 BGA

A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
A12
A13
A14
A15
A16
A17
A18
A19
A20
A21
A22
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Intel Corporation 5000 W. Chandler Blvd Chandler AZ, 85044			
Title ITP/Bus Ratio/Thermal Sensor			
Size C	Document Number Celeron Processor Adaptor	Rev A	
Date: Tuesday, May 11, 1999	Sheet 10 of 11		



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Title	Voltage Regulator	
Size	Document Number	Rev
C	Celeron Processor Adaptor	A
Date:	Tuesday, May 11, 1999	Sheet 11 of 11