13. Circuit Operating Descriptions

13-1 Power

13-1-1 Comparsion between Linear Power Supply and S.M.P.S.

13-1-1 (a) Linear

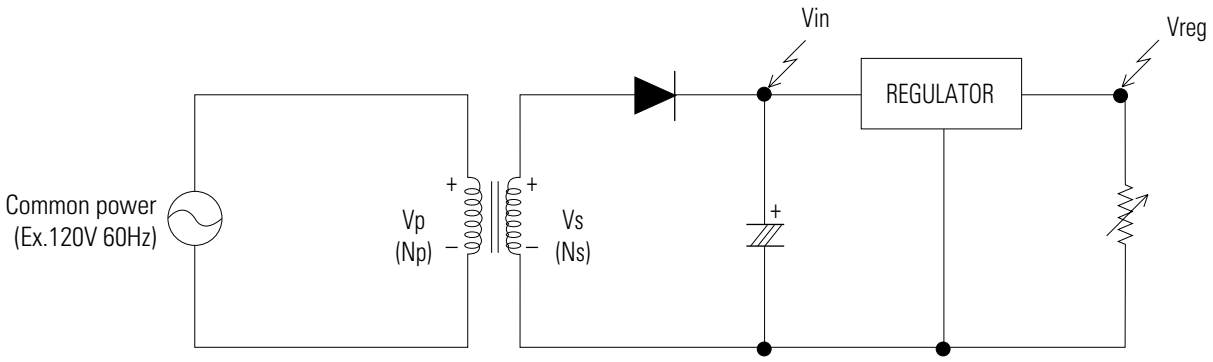

Fig.13-1 Linear Power Supply

◆ Waveform/Description

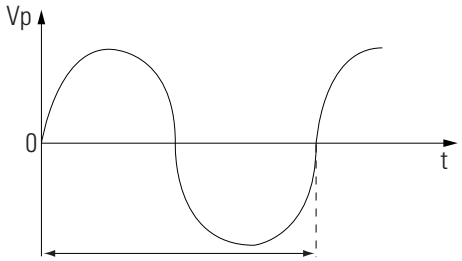

Fig. 13-2

Input : Common power to transformer (Vp).

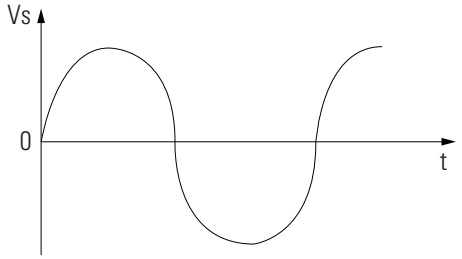

Fig. 13-3

The output Vs of transformer is determined by the ratio of 1st Np and 2nd Ns.
Vs = (Ns/Np) x Vp

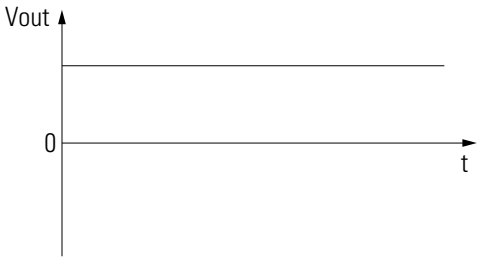

Fig. 13-4

Vout is output (DC) by diode and condensor.

◆ Advantages and disadvantages of linear power supply

1) Advantages : Little noise because the output waveform of transformer is sine wave.

2) Disadvantages :
   ❶ Additional margin is required because Vs is changed (depending on power source). (The regulator loss is caused by margin design).
   ❷ Greater core size and condensor capacity are needed, because the transformer works on a single power frequency.

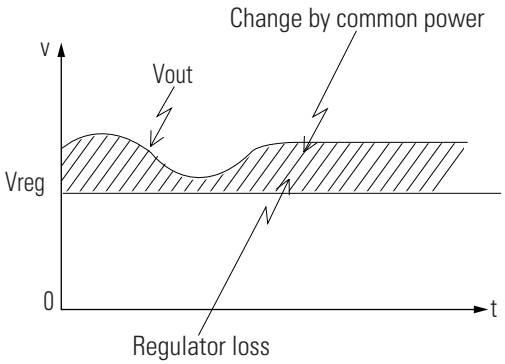

Fig. 13-5

13-1-1 (b) S.M.P.S. (Ringing Choke Converter methol)

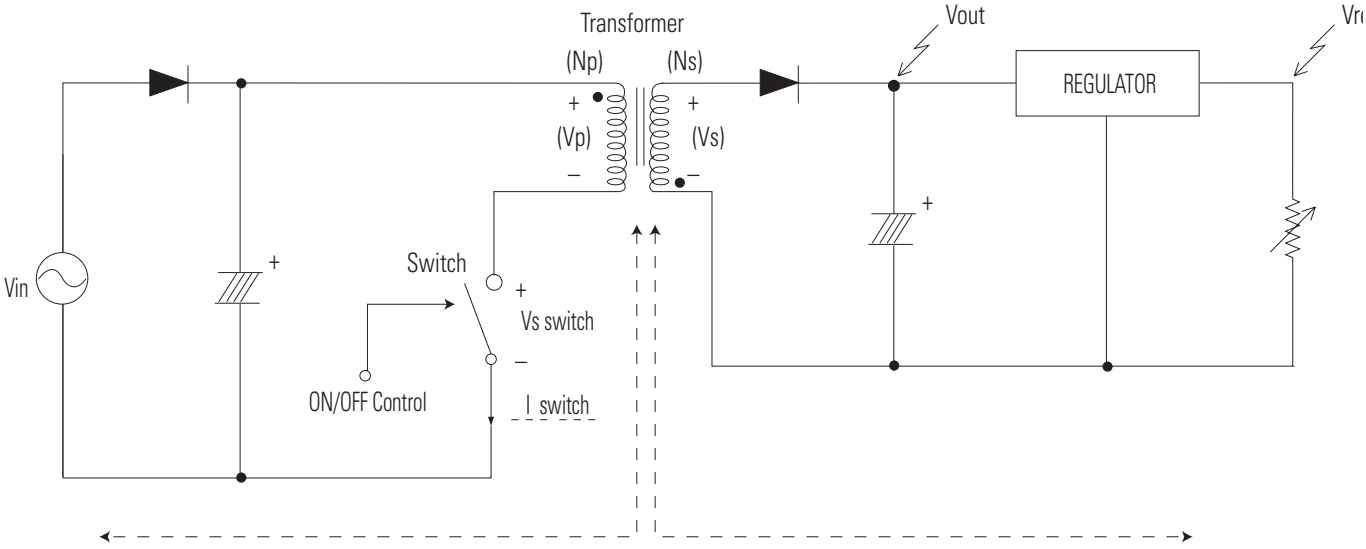

Fig. 13-6

◆ Terms

1) 1st : Common power input to 1st winding.
2) 2nd : Circuit followings output winding of transformer.
3) f (Frequency) : Switching frequency (T : Switching cycle)
4) Duty : (Ton/T) x 100

13-1-2 Circuit description [FLY-Back RCC(Ringing Choke Converter)] Control

13-1-2 (a) AC Power Rectification/Smoothing Terminal

1) PDS01, PDS02, PDS03, PDS04 : Convert AC power to DC(Full wave rectification).
2) PEF10 : Smooth the voltage converted to DC.
3) PLS01, PBS01 : Noise removal at power input/output.
4) PVA1 : SMPS protection at power surge input.

13-1-2 (b) SNUBBER Circuit : PDS11, PCD12, PER13, PRS11, PRS12

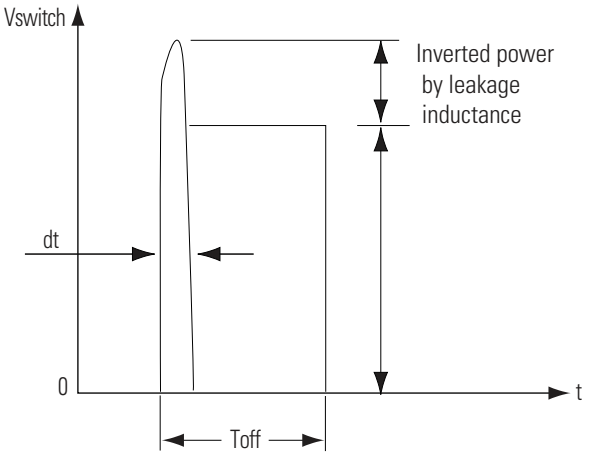

Fig. 13-7

1) Prevent residual high voltage at the terminals of switch during switch off/Suppress noise.
High inverted power occurs at switch (PQR11) off, because of the 1st winding of transformer :
(V=-L1 xdi/dt. L1 : Leakage Induction)
A very high residual voltage exist on both terminals of PQR11 because dt is a very short.

2) SNUBBER circuit protects PQR11 from damage through leakage voltage suppression by RC, (Charges the leakage voltage to PDS11, PER13, PCD12 and discharges to PRS13).

13-1-2 (c) Driving circuit

When Vin supplied, driving current Ig occurs through the PQR11. By this IC (=Hfe x Ig) occurs throug the PQR11 and the Vb is inducted to base winding coil NB of PQR11. By inducted Vb, Ib start flow and the PQR11 is sustained (S/W ON). Ib is constant and Ic increases in Proportion to time. After constant time passed Ib become to shortage and PQR11 is cut OFF (S/W OFF).

Circuit Operating Description

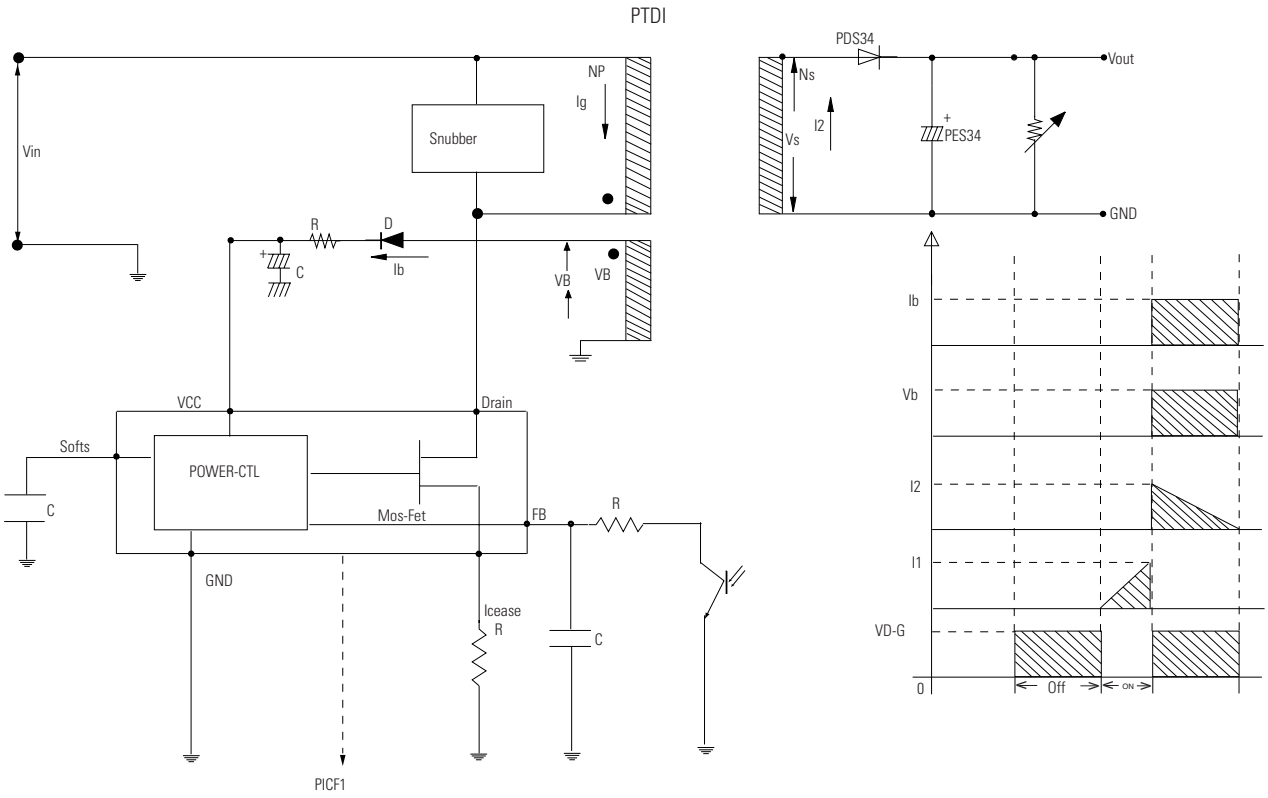

Fig. 13-8 Driving Circuit

13-1-2 (d) Feedback Control Circuit

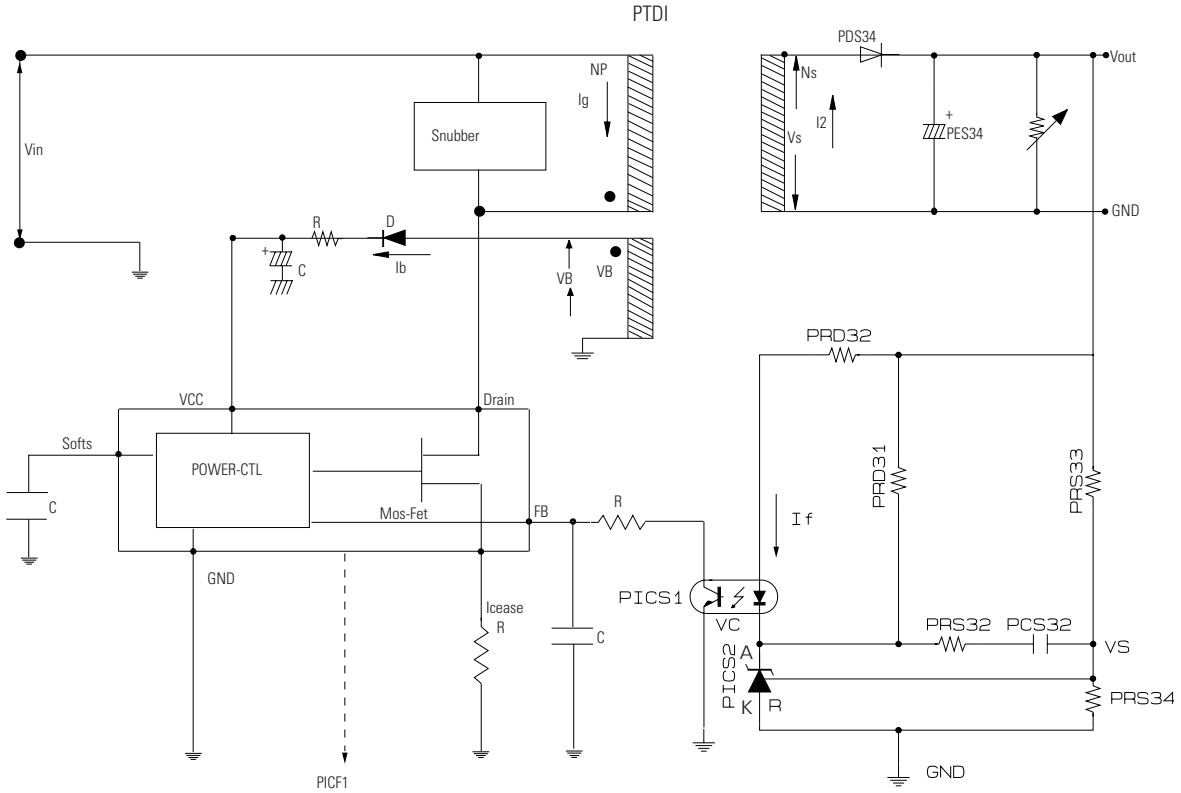

Fig.13-9

◆ Operation descriptions

1) Internal OP-Amp '+' base potential of PICS2 is 2.5V and external "-" input potential is connected with PRS33 and PRS34 to maintain Vout of 5.8V.
2) If load of 5.8V terminal increase (or AC inout voltage decrease) and Vout decrease over 5.8V,
   Then : PICS2 "R" potential decrease over 2.5V --> PICS2 A-K BASE Current decrease --> PICS2 A-K Current decrease --> PICS1 DIODE Current decrease --> PICS1 C-E Current decrease --> PICS1 C-E Voltage increase --> PICS1 F-B Voltage increase --> OUT DUTY increase TRANS Primary Cuttent Increase --> TRANS Primary Power increase --> Vout increase --> Vout maintain 5.8V

   - PRD31, PRD32 : Reduce 5.8V overshoot.
   - PRS32, PCS32 : Prevent PICS2 oscillation (for phase correction).

13-1-3 Internal Block Diagram

◆ Internal Block Diagram

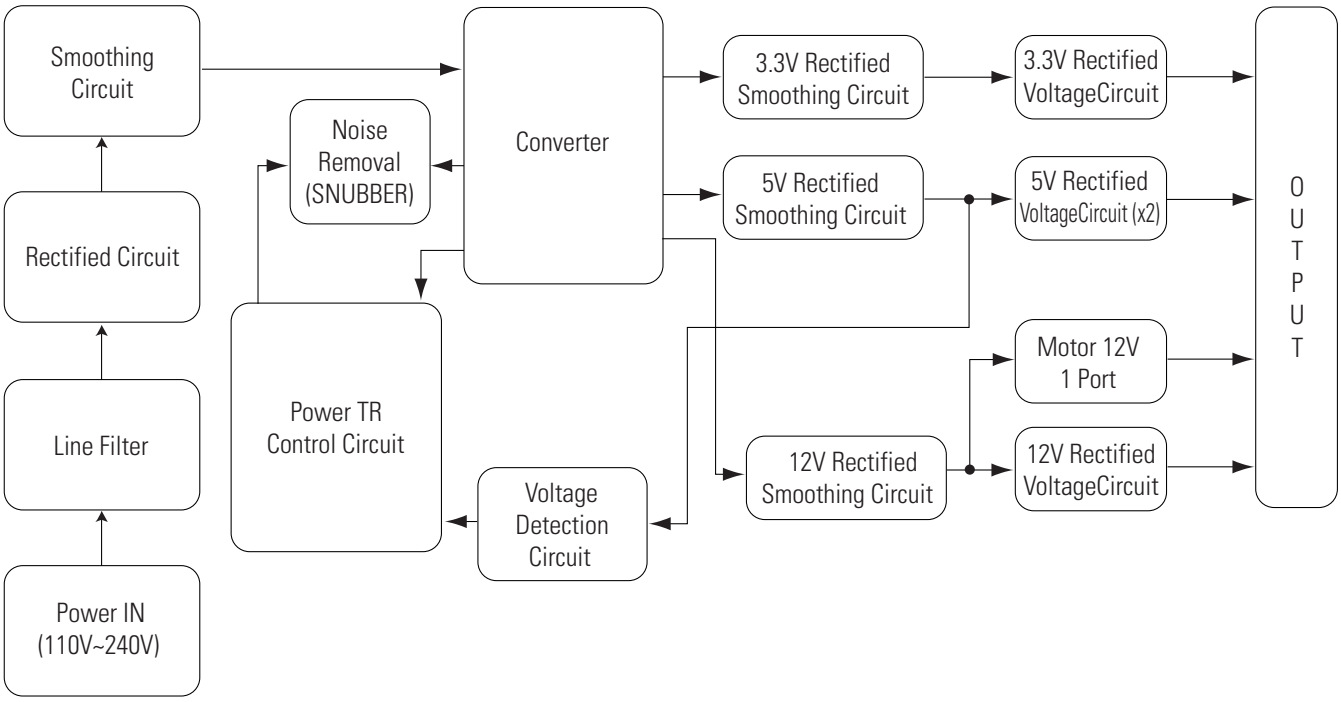

Fig.13-10

13-2 System Control

13-2-1 Outline

The main micom peripheral circuit is composed of 8M Flash Memory (ZIC3) for Microcode and data save, 16Mbit SDRAM (ZIC2) for temporary data read and write.
The Micom (ZIC1 ; Vaddis 962) mounted in main board analizes the key commands of front panel or instructions of remote control and controls the devices on board to execute the corresponding commands after initializing the devices connected with micom on board at power on.

13-2-2 Block Diagram

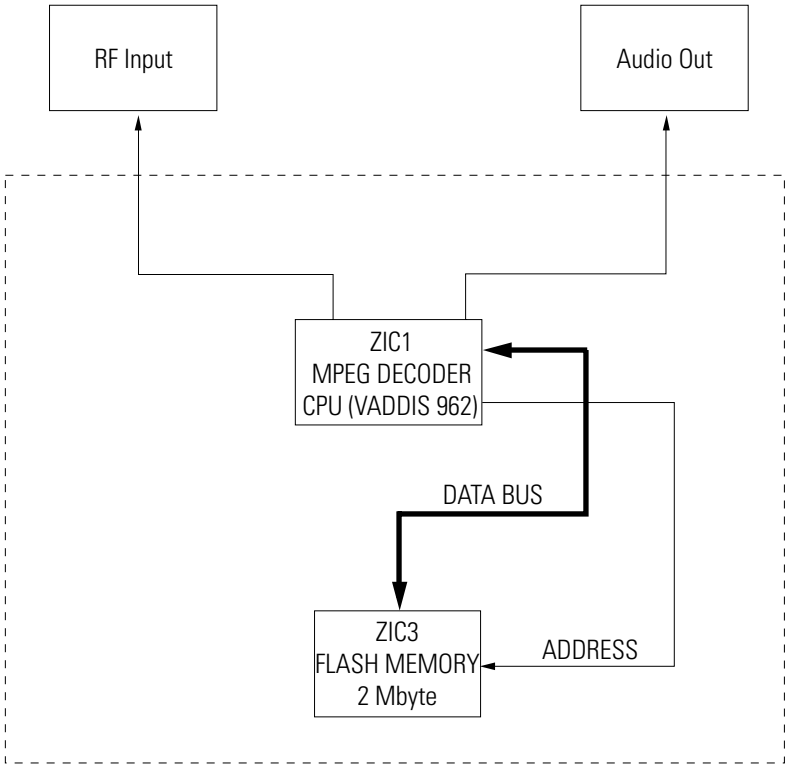

Fig. 13-11

13-3 DVD Data Processor

13-3-1 Outline

The Vaddis 962 (highly-integrated device) includes the full front-end disc controller, back-end decoder functions as well as the host control CPU.
The principal off-chip components include the disc drive with its optical pickup, tray, sled and spindle drivers and motors, 2Mbits of flash EPROM, 64Mbits of SDRAM, and the audio Digital-to-Analog converters some applications.

In case of general disc refresh, the memory is almost filled up periodically. It is because Write rate to memory after disc playback and signal process is faster than Read of A/V decoder. When the memory is filled, this status is reported by interrupt to main micom, which controls the servo to kick back the pick-up to the previous track after memorizing the last data read from disc until now. It takes some times to jump to the previous track and return to the original(jump location) again. The memory will have an empty space because A/V decoder reads out data of memory.
When the memory has an empty space, where data can be processed and written and the pick-up correctly gets to the original location(before kick back location) again, it reads data again avoids the interrupt of data read previously. The basic operation repeats to perform as described above.

13-3-2 Block Diagram

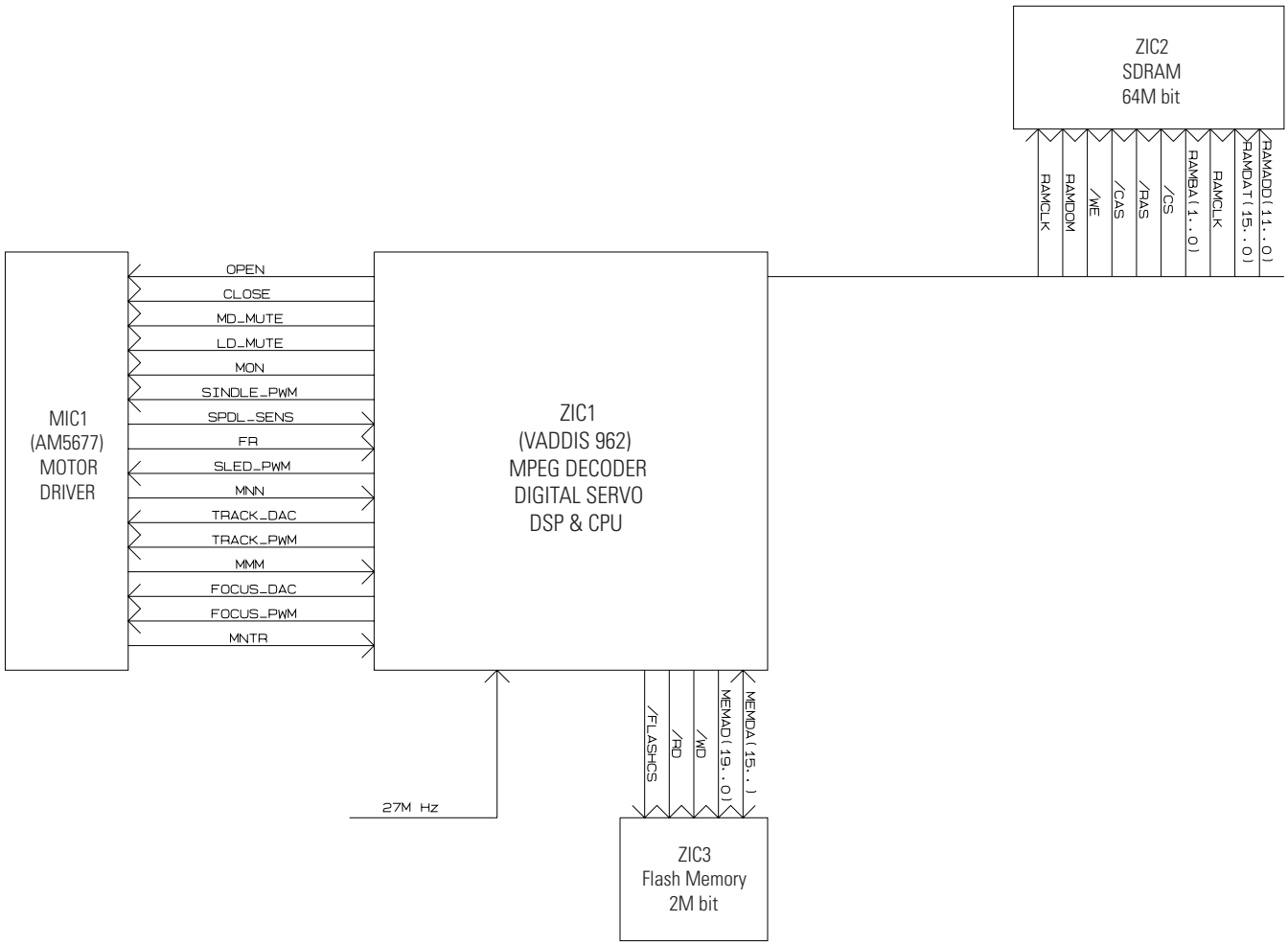

Fig.13-12

13-4 Video

13-4-1 Outline

ZIC1(A/V decoder with video encoder) diverges from the 27MHz crystal, then generates VSYNC and HSYNC.
ZIC1(A/V decoder with video encoder) does RGB encoding, copy guard processing and D/A conversion of 8bit video data internally inputted from video decoder block by ZIC1.
Video signal converted into analog signal is outputted via amplifier of analog part.

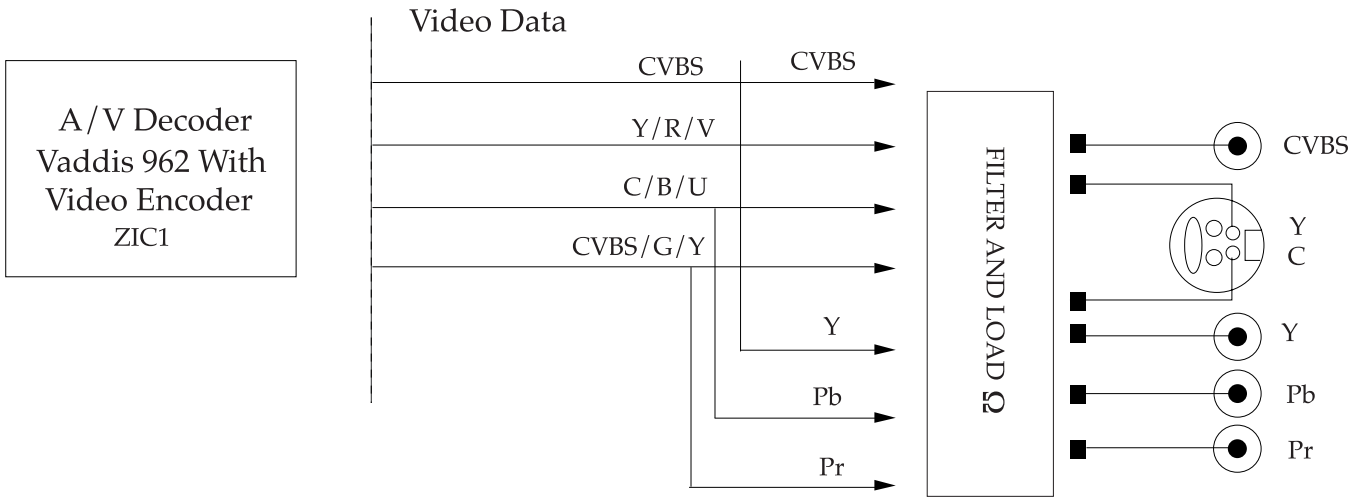

Fig. 13-13 Video Output Block Diagram

13-4-2 NTSC/PAL Digital Encoder (VADDIS 962 ; Built in video encode)

ZIC1 inputted from pin 161 with 27MHz generates HSYNC and VSYNC which are based on video signal.
ZIC1 is synchronous signals with decoded video signal and control the output timing of 8bit video signal of ITUR601 format.
The separate signal is encoded to NTSC/PAL by control of ZIC1.
The above signals, which are CVBS (Composite Video Burst Synchronized)/G (GREEN)/Y [PIN148] , Y (S_VIDEO)/R (RED)/Pr [PIN151] and C (S_VIDEO)/B (BLUE)/Pb, are selectively outputted CVBS +S_VIDEO, RGB/Component menu setup. In Course of encoding, 8bit data can extend to 10bit or more.
To convert the extended data to quantization noise as possible, ZIC1 adopts 14bit D/A converter.
ZIC1 perform video en-coding as well as copy protection.

13-5 Audio

13-5-1 Outline

A/V decoder (ZIC1 ; Vaddis 962) is supply to DATA 0 for 2-channel mixed audio output.
The audio data transmitted from A/V decoder (ZIC1 ; Vaddis 962) are converted into analog signal via audio D/A converter and outputted via post filter and amplifier.
CD and VCD are outputted with only 2 channels audio data and transmit them to Data 0.
If DVD of multichannel Source disc, if is downmixed and transmit them to Data0.

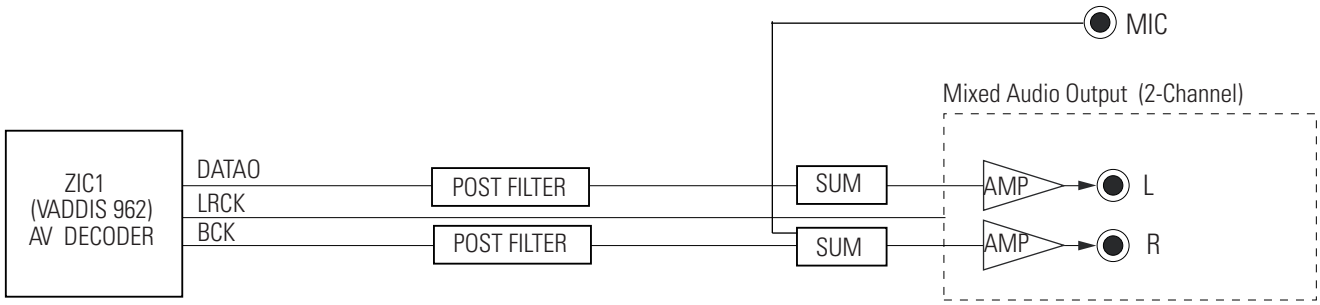

Fig. 13-14 Audio Output Block Diagram

13-5-2 DVD Audio Outline

1) Compressed Data
The audio data inputted to ZICI (Vaddis 9) A/V decoder is divided into compressed data and uncompressed data. It is compressed data that is compressed with multi-channel audio data such as Dolby digital, MPEG, DTS. WMA. etc.
The compressed data inputted to ZICI (Vaddis 9) is converted into the uncompressed data of 2,4, and 6 channel throught ZICI built-in audio decoder and is outputted to data 0 throught digital audio interface.
The compressed data is transmitted to external AC-3 amplifier or MPEG/DTS amplifier as IEC-958/1937 transmission data format compressed by ZIC1 built-in IEC-958 output process

2) Uncompressed Data
The uncompressed data is that data isn't compressed. so it is called CD-DA. LPCM data.
The 2 channels data converted through audio decoder 2-chennel data and data 0 and are outputted in digital audio interface. Via IEC-958 output proses, they is transmitted to digital amplifier or AC-3/MPEG/DTS amplifier built in the external digital input source with IEC-958/1937 transmission format.

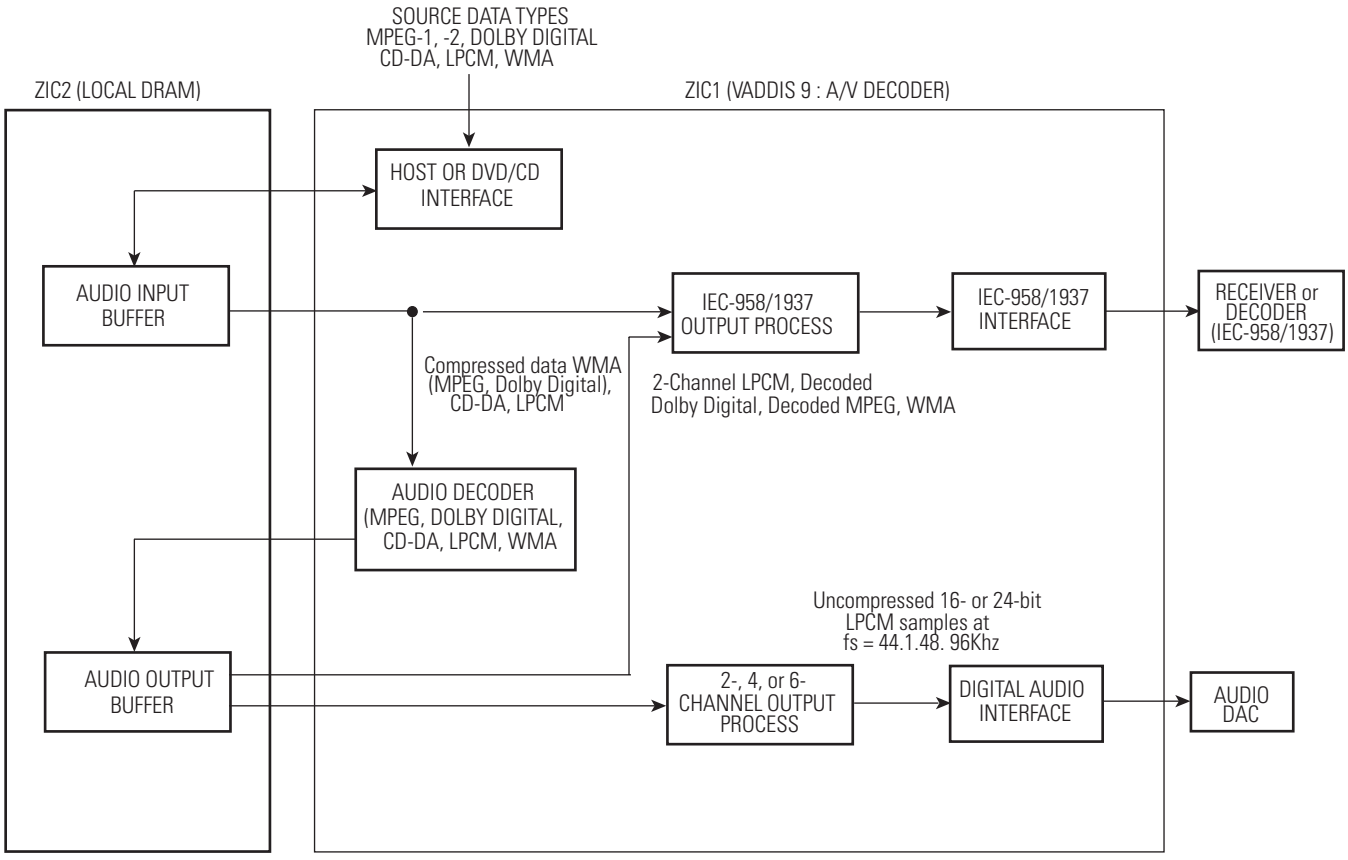

Fig. 13-15 Audio Decoder and Output Interface Datapath

13-6 Servo

13-6-1 Outline

SERVO system of DVD is Compoced of Focusing SERVO, Tracking SERVO, SLED Linked SERVO and CLV SERVO (DISC Motor Control SERVO).

1) Focusing SERVO : Focuses the optical spot output from object lens onto the disc surface. Maintains a uniform distance between object lens of Pick-up and disc (for surface vibration of disc).
2) Tracking SERVO : Make the object lens follow the disc track in use of tracking error signal (created from Pick-up).
3) SLED Linked SERVO : When the tracking actuator inclines outwardly as the object lens follows the track dur ing play, the SLED motor moves slightly (and counteracts the incline).
4) CLV SERVO (DISC Motor Control SERVO) : Controls the disc motor to maintain a constant linear velocity (necessary for RF signal).

13-6-2 Block Diagram

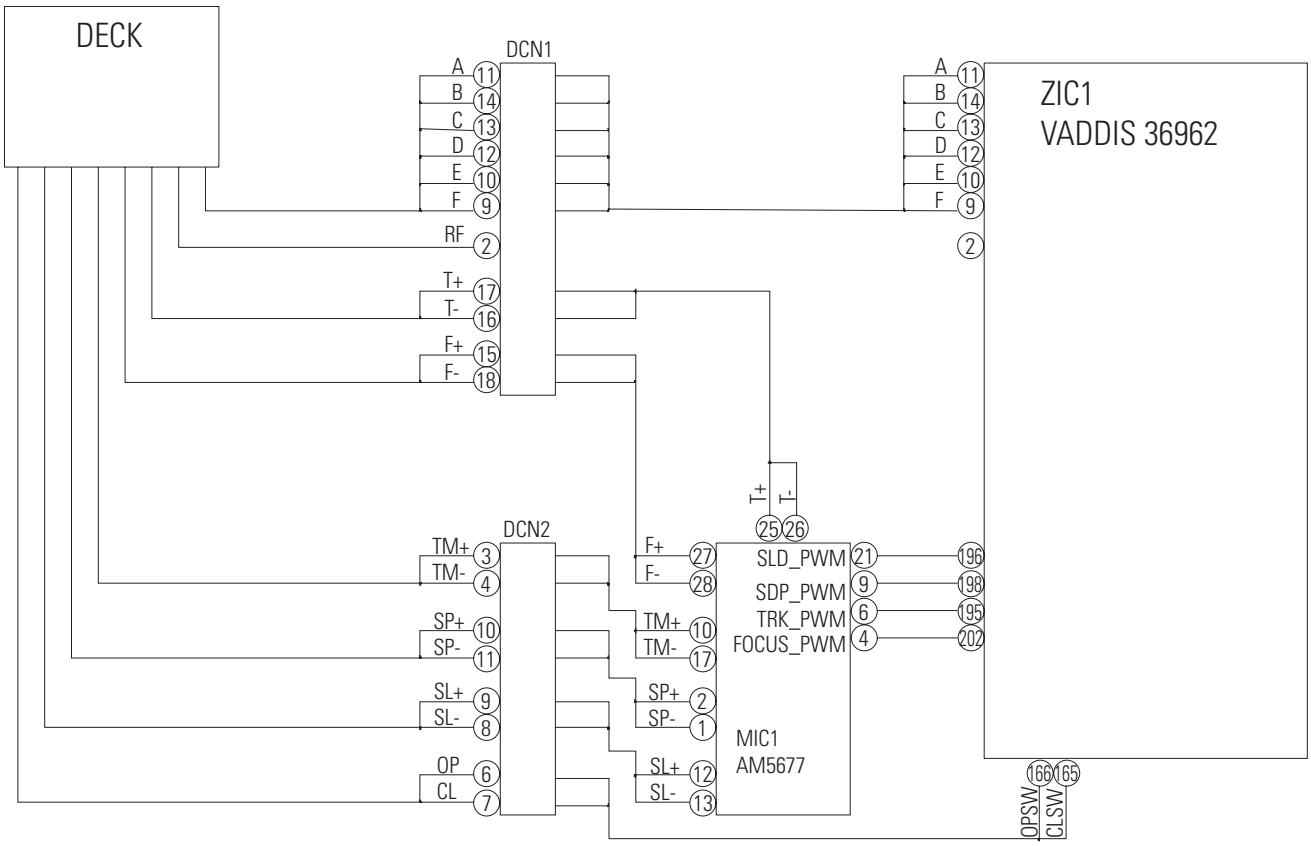

Fig.13-16

13-6-3 Operation

1) FOCUSING SERVO

(1) FOCUS INPUT

The focus loop is changed from open loop to closed loop, and the triangular waveform moves the object lens up and down (at pin 202 of ZIC1 during Focus SERVO ON.) At that time, S curve is generated in ZIC1.

Summing signal of PD A, B, C, D, is generated, and zero cross(1.65V) point occurs when S curve is focused and ABCD signal exceeds a preset,constant value. The focus loop is changed to
closed loop, and the object lens follows the disc movement, maintaining a constant distance from the disc.
(these operations are same in CD and DVD).

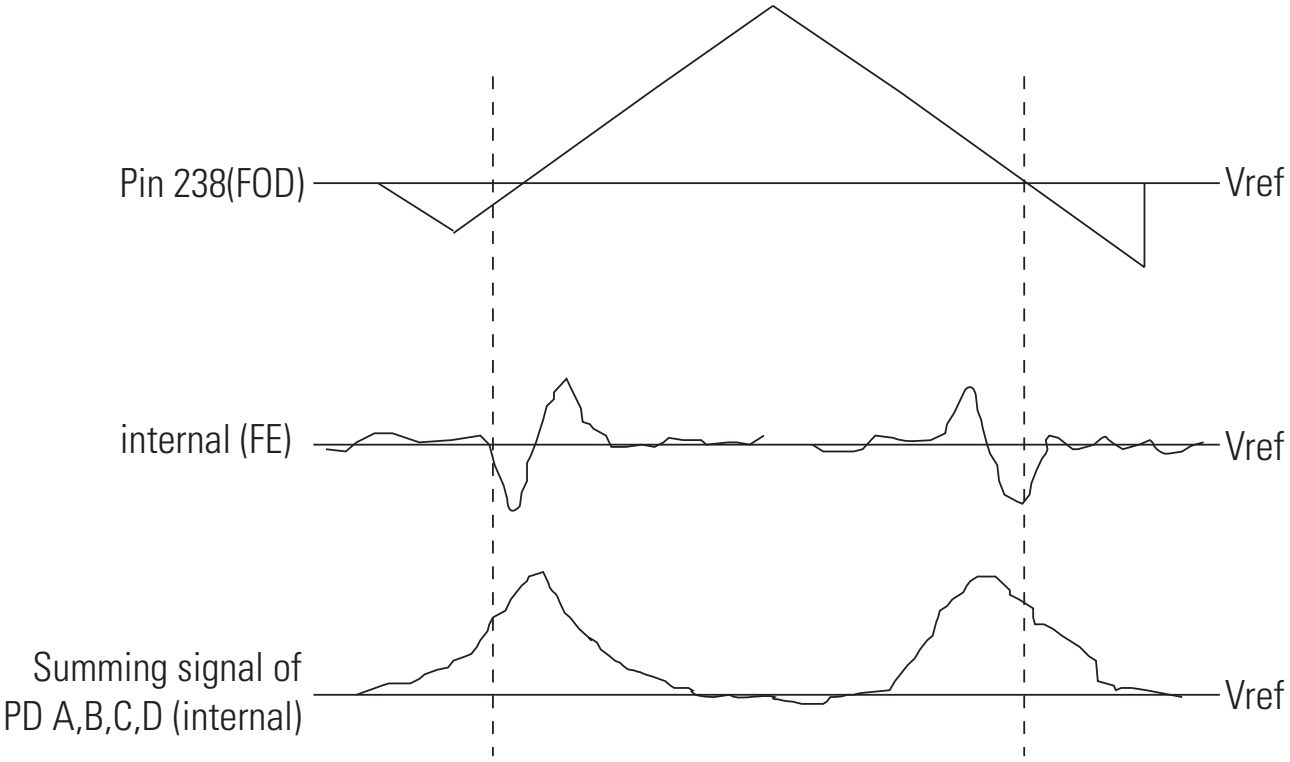

Fig. 13-17

(2) PLAY

When focus loop closes the loop during focus servo on, both pin 27 and pin 28 of MIC1 are controlled by ZIC1.

2) TRACKING SERVO

(1) NORMAL PLAY MODE

❶ For DVD
Composite : The signal output from PD A, B, C, D of Pick-up, the tracking error
phase difference of A+C and B+D in RIC1, and inputs to ZIC1. Then, it is output to ZIC1 pin 169 via digital equalizer, and applied to the tracking actuator through FIC3.

Pin 69 of ZIC1 is controlled by VREF(approx. 1.65V) during normal play.
Meanwhile, DVD repeats the track jump from 1 to 4 in inner direction at normal play (because data- read speed from disc is faster than data output speed on screen).

❷ For CD, VCD
Receive the signal output through E, F of Pick-up. The tracking error signal is similar to DVD.

(2) SEARCH Mode :

Search mode : Fine seek,(Moving the tracking actuator slightly little below 255 track) and coarse search, moving much in use of sled motor. The coarse search will be described in sled linked servo and now, the fine seek is explained shortly.
If the object lens is located near target, cut off the tracking loop and give the control signal as many as desired count to move the tracking actuator via ZIC1 pin 184 terminal(TRACK_PWM).

3) SLED LINKED SERVO

- Normal play mode
  Move SLED motor slightly by means of PWM signal in ZIC1 pin 196, as the tracking actuator moves along with track during play. Control to move the entire Pick-up as the tracking actuator moves.

- Coarse search mode
  In case of long-distance search (such as chapter serach), ZIC1 uses open-loop jump method.
  Then, read ID and compute the existing track count after input of next track.
  If the existing track count is within fine seek range, tracking begins using fine seek.

4) CLV SERVO(DISC MOTOR CONTROL SERVO)

Detect SYNC signal from R/U in ZIC1, and output PWM signal to ZIC1 pin 236 for constant linear velocity.