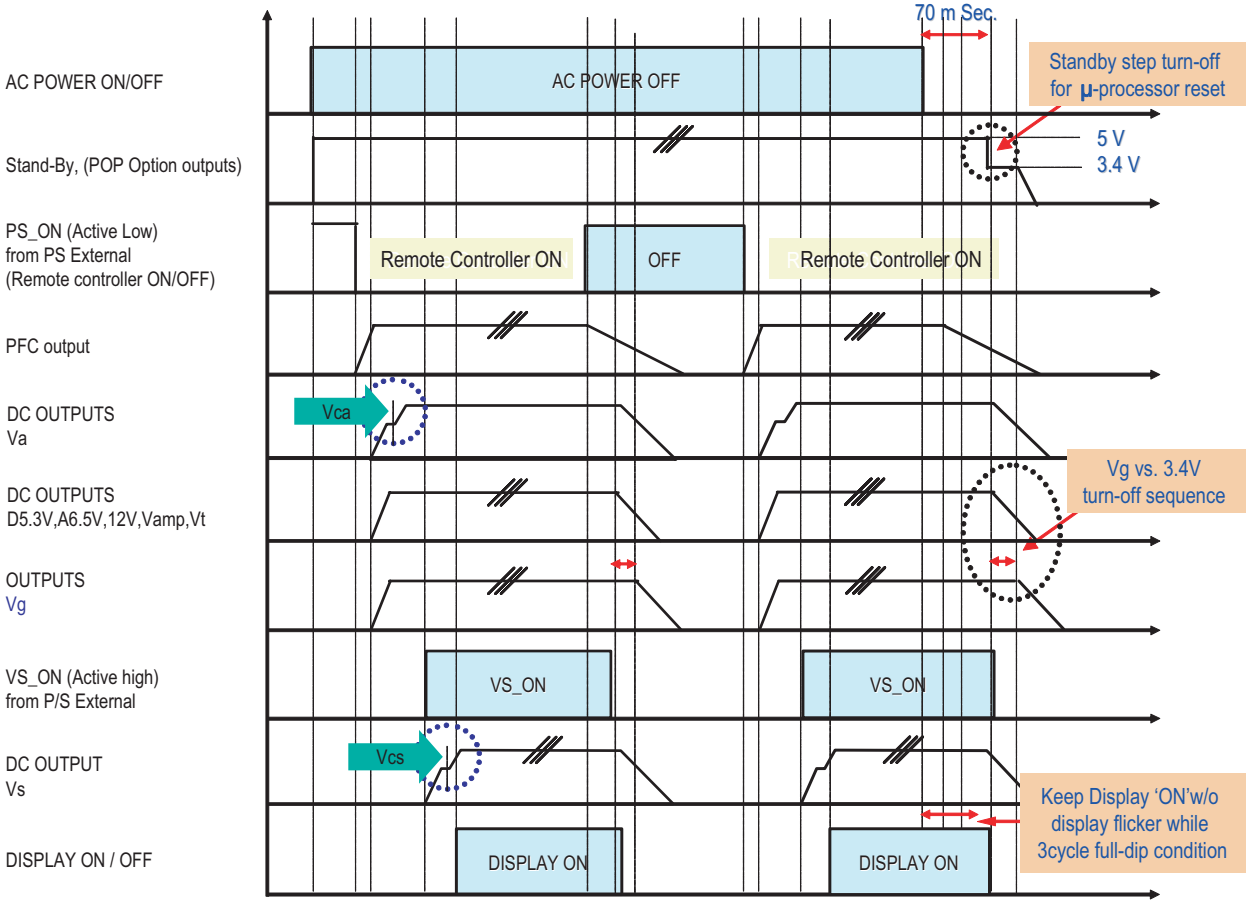
13. Circuit Description

13-1 Power ON/OFF Signal Timing Sequence



1. When connecting the AC power cord, Stand-By 5V from the Main SMPS is supplied to the Main Board (Pin 3 of CN1002 of Main Board).

2. When pressing the Power button on the remote control or on the main body, PS_ON (Pin 5 of CN1002 of Main Board) changes from High to Low.

3. If the PS_ON signal changes to Low, the Main SMPS supplies power to the Main Board and Logic Board, and Va and Vg power is supplied to the DC-DC SMPS.

4. If the VS_ON signal from the Logic Board changes from Low to High, the Main SMPS supplies VS power to the X and Y Main Board through the DC-DC SMPS, and the screen displays a picture on it.

13-2 Partial Block Description

13-2-1 Main SMPS

1. Summary
This is a service manual about the explanation of basic operation in power circuit (1H309W) for 50" PDP.

2. Input Part
This switching mode power supply (SMPS) has the input voltage range of 90 ~ 264[Vac].
Thus, at 90[Vac] input condition or any voltage level in a spec, the power board must operate even if the ac source is cut off and re-input ON.

3. Output Part
This power circuit has the 10 outputs. In steady state, the specification about the output's voltage and current is the same as following Table 1.

Table 1. PDP SMPS's output specifications (for 50")

Output Circuit	Nominal Voltage [V]	Voltage Adjustment [V]	Total Regulation	Nominal Load [A]	Load Variation [A]	Peak Current [A]	Ripple Noise [mV p-p]
Vs	210	190 - 220	± 2%	1.7	0.1 - 2.5	10.0	800
Va	70	60 - 80	± 2%	0.7	0.1 - 3.0	4.5	500
D5.3V	5.3	----------	± 5%	3.5	0.1 - 5.0	6.0	50
A6.5V	6.5	----------	± 5%	1.5	0.01 - 3.0	4.0	50
FAN_8V	8	----------	± 5%	-	0.01 - 0.2	0.5	120
Vg	15	----------	± 5%	0.5	0.01 - 1.0	1.5	120
12V	12	----------	± 5%	1.3	0.01 - 1.5	3.0	120
Vamp	18	----------	± 10%	0.1	0.01 - 2.5	3.0	180
Vt	33	----------	± 5%	5m	1m - 6m	7m	300
STBY	5.0	----------	± 5%	0.5	0.01 - 1.0	1.5	50

① Over Voltage Protectionl
This power circuit has the function of over voltage protection (O.V.P) in all outputs.
In condition of any over voltage in each output ports, the power supply is shut-down by O.V.P function for the protection of part's damage.

② Short / Over Current Protection
Because any output ports have small impedance (smaller than 300m ohm) at the output short condition, power circuit was designed to have the function of short / over current protection (O.C.P) in all outputs. Thus, in condition of any over current in each output ports, the power supply is shut-down by O.C.P function for the protection of part's damage. The specification about the O.C.P in each port is the same as following Table 2.

Table 2. OCP specification

Protection	Output Circuit	Trip point	Notes
Over Current	Vs	3.0 - 6.0A	Shut down by Under Voltage
	Va	3.5A or more	Short Circuit Protection Shut down by Under Voltage
	Output except Vs&Va	----------	

4. Basic Function

① Remote Control
This power circuit has the function of remote control by using the relay (250V, 10A)

② Free Voltage
This power circuit has the free voltage input range.

③ Power Factor Correction
This power circuit has the PFC for high power factor (higher than 0.9)

④ Protection
This power circuit has the function of short / O.V.P / O.C.P for the protection of part's damage.

5. Explanation of Circuit Blocks

① Filter Circuit
Line filter consists of Common Mode Reactor L8102¡¤ L8103, Normal Mode Reactor L8101, X-condenser C8101 · C8106, Line by-pass condenser(Y-con) C8104 · C8105 and surge protection parts ; NR8101 · NR8102 · NR8103 · NR8104 · SQ8104 · SQ8105.
This block reduces the high frequency ground noise from the original ac power source.

② Rectifier / DC link Circuit
This rectifier circuit creates the dc regulated voltage from AC input line.
【Power Source】
· **Sub-power Source**
The half-wave AC voltage through the D8151 creates the sub-dc source in C8121.

· **Main-power Source**
The full-wave AC voltage through the RC8101 creates the main-dc source for PFC input.

③ Inrush Current Protection Circuit
In a transient response interval of the AC source injection, the high inrush current flows from ac source to this power board because of an input capacitor having the low impedance. At that interval, the part¡¯s damage is quite within the realms of possibility. The inrush current protection circuit removes this possibility in a transient interval by adding thermistor (TH8101, TH8102). After PFC input capacitor is fully charged, (in steady state), the relays (RL8101, RL8102) are ON and input normal current flows through them without any overheat.

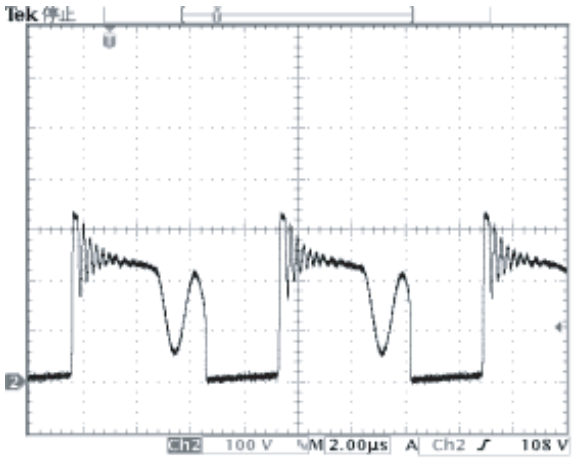
④ Sub-Power Circuit
【Basic Operation】
This Stand-by block is controlled by SMPS operation ; On/off switching FET inside of PRC [pulse ratio controlled] IC (STR-V152).
Using the switching operation, we can get the energy in an input capacitor [C8121] to transmit to output-port for STD 5V, dc source for Micom and PFC controller. The PRC controller STR-V152 can be operated by injection of the Start-up current to 8 pin of it. Output voltage is also controlled by following method ;
Controlled op-amp [Z8171] keeps the output voltage to be constant in steady state by compensating an error voltage between the dividing-resistors (R8174, RX8172 and R8175) and its reference 2.5V. And then output small signal voltage of op-amp induces a Photocoupler current level on the feedback line. Dc source voltage for PFC controller comes from secondary side link in a main transformer (3~5 pin).

【Protection Function】
· **Over Voltage Protection**
When the Vcc voltage is higher than O.V.P level [Vcc(OVP)=31.2V(TYP)], Latch is on and power board is shut down. After Latch is on, this power board can not operate before the voltage of an electric capacitor C8123 is fully discharged for about 5 minutes.

- **Over Current Protection**
  O.C.P function in STR-V152 can be obtained by sensing the MOS-FET's drain peak current per 1 pulse (Pulse by Pulse method). This sensing value comes from the voltage across sensing-resistor(R8122) between OCP(FET source,3Pin) and GND(5Pin). Thus, this power board can protect any part's damage caused by over current flowing.

- **Over Load Protection**
  If there is an overload state in output ports due to some reason, this power board operates in UVLO mode for protection of IC's damage.

- **Over Heat Protection**
  If the temperature on the chip parts is higher than about 135℃, this power board operates in thermal protection mode and makes Latch on, finally this power board is shut down.



< Vds Voltage Waveform on Sub-power Circuit FET >

⑤ PFC Circuit

【Basic Operation】

After the sub-dc voltage source is on, Vcc of PFC controller IC(UCC2818A) induces the PSON port to be "L" level and this makes the oscillation with a frequency $\frac{0.6}{RT \times CT}$ (RT:R8239, CT:C8235) in it. The PFC block consists of two inside feedback loop to control FET duty ratio. The first is the voltage loop that keeps the output voltage to be constant by sensing the output voltage in 11 pin. And the second loop controls the power factor by comparing the input line voltage (6pin) and reference in it. By this current loop, the input current waveform can be sinusoidal and now we can get the higher power factor (almost 1.0) in this power board.

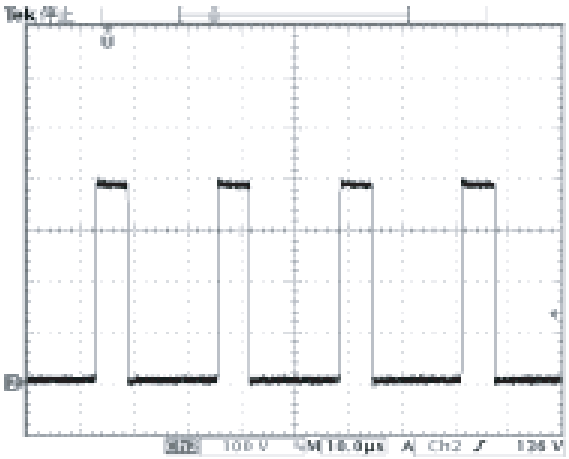
【Protection Function】

· **Over Voltage Protection**

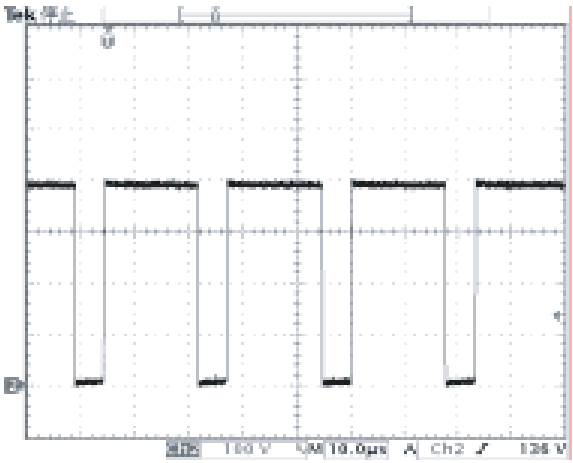
Because the PFC controller IC(UCC2818A) has the function of over voltage protection about the high output voltage limit, even if the overshoot and not-controlled state occur with the deep condition in ac input source or output step load, this controller protects the abnormal output voltage state by decreasing the FET ON ratio. The high output limit level is set to 110% value of voltage across the dividing resistors ; R8247, R8248, R8249, R8250, R8251
(this power board has also the high limit O.V.P level about 440V)

· **Over Current Protection**

PFC controller has the function of over current protection by sensing the voltage (2 pin) coming from the current-sensing resistor R8201. If the over current flows across the sensingresistor, controller decreases the FET duty ratio for protection of part's damage.



< FET Vds Waveform (100Vac input) >



< FET Vds Waveform (230Vac input) >

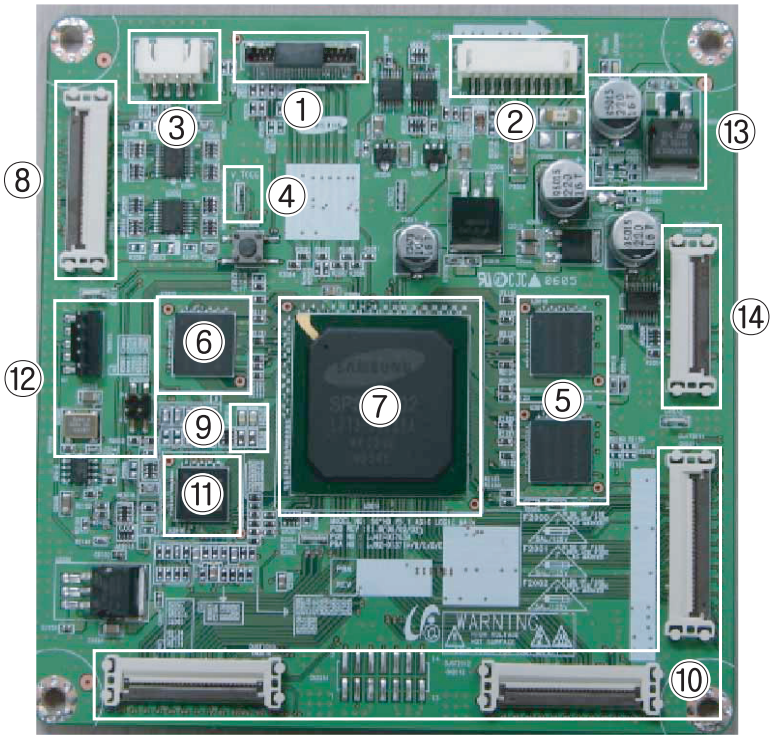
6. Component Spec

Z8231	UCC2818A	18V, 20mA	TEXAS	PFC IC
Q8201, Q8202, Q8205	2SK3911	600V, 20A	TOSHIBA	PFC Switching FET
D8203	FMC-26UA	1200V, 3A	SANKEN	PFC Diode
D8205	FMX-G16S	600V, 5A	SANKEN	PFC Diode
Z8121	STR-V152	17.5V, 4A	SANKEN	ST-BY Switching IC
D8171	FMB-G14L	40V, 5A	SANKEN	ST-BY Diode
Q8301, Q8302	2SK2698	500V, 15A	TOSHIBA	Half SMZ FET
Q8502, Q8503	2SK2698	500V, 15A	TOSHIBA	SMZ FET
Z8333	SI-3150C	35V, 1.5A	SANKEN	Regulator
Z8334	SI-3050J	25V, 2.0A	SANKEN	Regulator
RC8336	FMX-22S	200V, 10A	SANKEN	Vamp Output Diode
D8332	1SS244	250V, 625mA	ROHM	Vt Output Diode
RC8331	FMX-22S	200V, 10A	SANKEN	Vg Output Diode
RC8332	FMB-26L	60V, 10A	SANKEN	12V Output Diode
Q8332	2SK2232	60V, 25A	TOSHIBA	6.5V Switching IC
RC8333, RC8334	FMB-26L	60V, 10A	SANKEN	6.5V Output Diode
Q8331	2SK3659	20V, 65A	NEC	5.3V Switching IC
RC8335	FME-24H	40V, 15A	SANKEN	5.3V Output Diode
Q8401	2SK2698	500V, 15A	TOSHIBA	Va FET
RC8401	FMX-G26S	600V, 10A	SANKEN	Va Output Diode
RC8551	FMG-26S	600V, 6A	SANKEN	Vs Output Diode
RC8101	RBV-1506J	600V, 15A	SANKEN	Bridge Diode
RL8101, RL8102	G5PA-1-M-E	250V, 10A	OMRON	Relay

13-2-2 PDP Module

1. Logic Board

■ A name of main part of Logic Board and vocabulary.



Item	Name	Explanation
①	LVDS Connector	The connector to receive LVDS-encoded RGB, H, V, DATAEN and DCLK signals from the Video Board.
②	Power Connector	The connector to receive power (5V) and the control signal for the Logic Board.
③	Communications Connector	The connector to connect the keyscan, which adjusts the pattern and registry values, the window manager and the 512K loading board.
④	V-TOGG	V-SYNC Out pin.
⑤	DDR MEMORY (MENCON)	Memory for saving address output data.
⑥	DDR MEMORY (SFP)	Memory for saving DRIVE output and FRAME DELAY data.
⑦	ASIC CHIP	The Main Processor that generates and outputs the logic drive signal and address data.
⑧	Y Connector	The connector to output the Y Drive Board control signal.
⑨	Operating Status LED	The LED that shows if the Sync and Clock signals are normally applied to the Logic Board. (Normal Condition: Blinks at a 0.5 second interval) For an initial drive, LED2001 is on for 2 seconds and LCD2002 blinks at a 0.5 second interval.
⑩	CN2010, CN2011, CN2012	The connector to output address data and the control signal to the lower E, F and G-buffer board.
⑪	ARM-PROCESSOR	The IC circuit that controls the control signal to drive the Logic Main.
⑫	Micom Loading 5Pin Connector Initial image option PIN (CN2009)	: The connector for loading the Micom Drive program (CN2015). Loads the program in connection with the GA-WRITER. : Initial image select F/W or BLACK : Jumper Yes : 4 3 / 2 1 (■ ■ / □ □) or 4 3 / 2 1 (□ □ / ■ ■) Full White, Jumper No : 4 3 / 2 1 (□ □ / □ □) Black
⑬	Main Power Input	The Power Block that receives 5V input from SMPS and outputs 3.3V (L4957AD3.3V regulator adopted)
⑭	X Connector	The connector to output the X Drive Board control signal.

■ About Logic Board

The Logic Board consists of a Logic Main board, which processes the video signal input through LVDS and creates the address driver output and XY drive signals, and a Buffer board, which buffers the output signal and outputs the signal to the Address Driver IC (TCP IC).

Logic Board		Function	Remark
Logic Main		- Video Signal Processing (W/L, error diffusion, APC, FCR) Built-in LVDS Application and 1 ASIC Chip - Outputs the Address Driver Control and Data Signals to the Buffer board - Outputs the XY Drive Board Control Signal - Major Drive Voltage Monitoring (MICOM Circuit Block) : Detects abnormal voltage applications and protects drive circuits - Temperature Induced Operating Mode (Low Temperature/Room Temperature/High Temperature) : Optimization of discharge by temperature	
Buffer Board	E Buffer Board	Outputs data and control signals to the bottom left TCP IC.	Single Scan and RSDS applied
	F Buffer Board	Outputs data and control signals to the center up TCP IC.	
	G Buffer Board	Outputs data and control signals to the bottom right TCP IC.	

■ Normal Waveform

If the PDP set and the Logic Board are operating properly, the Operating LED of Figure 1 blinks normally (at a 0.5 second interval) and the V-SYNC and data are properly output. If the screen is displayed abnormally, check if the Vref voltage supplied to the DDR is 1.25V.

If the set is out of order, follow the troubleshooting procedures below.

1. Visual Inspection: Check if the Operating LED of the Logic Main blinks at a 0.5 second interval.
   ▶ The Operating LED blinks too fast or too slow when Micom is processing data abnormally. In this case, reload the data to the Micom. To load the data, load the data using the GA-WRITER, connecting power to the module.

2. If no problem has been found by a visual inspection, check if the drive waveform and address data are normal using an oscilloscope.
   (Checkpoint : For drive waveform output, measure the power of the damping resistance.
   For address data output, because the address output is RSDS data, measure the output using a Differential Prove for a more accurate result.

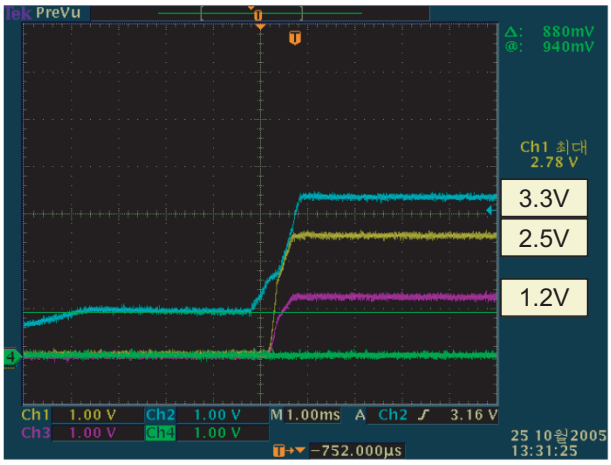
   ▶ If the drive waveform or address output is not measured, check if the output of R2104, which is to the left of U2010, is 3.3V using a multimeter. No output is measured when the program is corrupted. In this case, reload the program. If the output is measured, check if the ASIC_nRESET TP output is 3.3V. If the set does not work or no picture is displayed when the output is normal, load the program using the GA-WRITER or measure the output again using another oscillator as this happens when the clock generator is out of order through an oscillator (X2000) short, or an error occurred during the program's initial run.

   ▶ For an abnormally displayed screen, check the data output. If the data output is normal, the reason may be a hardware short or a resistance crack. First check if there is short or crack on the Logic Board (Logic Main and Buffer) through a visual inspection and measure the resistance of the resistor in the area in question. For address data, check if the U2003 regulator output is 2.5V as an abnormal screen may be caused by an abnormal operation of the DDR memory through the wrong Vref voltage. Then, measure the R2018 and R2020 resistors and check if the output voltage is 1.25V. If not, the reason may be because BGA is open or short. In this case, since this defect is not repairable, replace the board, reload the latest program and retest it.

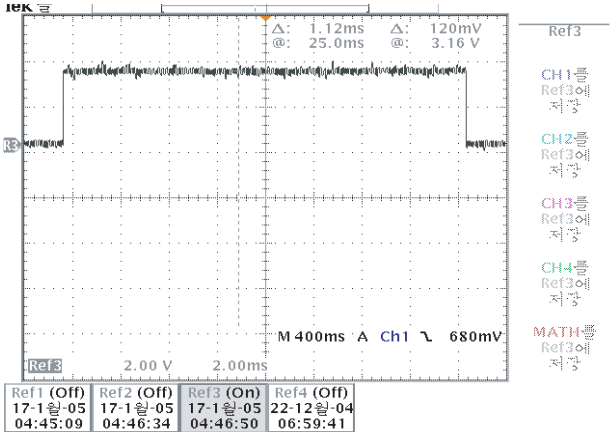
   ▶ If the screen is displayed abnormally when the Vref voltage is normal, conduct a short test to find any abnormal points and repair the points, if found. If the found short is internal, replace the board.

   ▶ The following waveform shows a waveform when the V-sinc and address data are output properly.

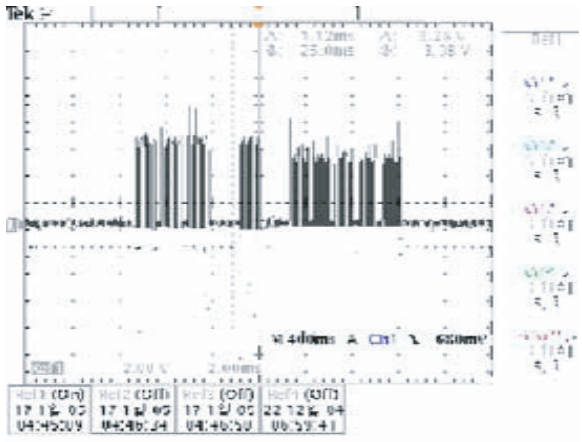
▶ In addition, you must first conduct a preliminary appearance inspection to locate damages to a device, a blank screen due to a missing jumper and any abnormal operations because of a missing jumper.



Normal Power Input Waveform
1. ARM3.3V or D3.3V
   * ASIC_nRESET and ARM-RESET must also be output as 3.3V.
2. D2.5V(DDR I/O)
3. D1.2V (for ASIC Core)



< Normal V-SYNC Output Waveform >



Since it is RSDS, process the signal using a differential signal. The above waveform is a positive signal. The waveform of the negative signal output is the reverse of the positive signal.

2. X, Y Control Block

■ Drive Circuit Definition

The Drive Circuit is a circuit that generates a waveform (high-voltage pulse) for the X and Y electrode group of the panel's external port so as to control the panel. The high-voltage switching pulse is generated through the combination of the IC HYBRID (Drive block + IGBT) and FET.

■ Drive Circuit Mechanism

A picture is displayed on the PDP by applying voltage to the X, Y and ADDRESS electrodes of each pixel according to the appropriate condition. The drive waveform applied to 42HD V4 is of the ISSS (ISSS: Interweaving Scan and Selective Sustain with Scan IC) type and has IDS (InDependent Sustain) in the Scan section unlike the existing ADS. Discharges within a PDP pixel can be classified into 3 types:

① Address Discharge: To form a wall voltage within the pixel by giving information (applying DATA voltage) to the pixel to be lit.

② Sustain Discharge: Sustain Discharge is a display section that voluntarily maintains the discharge of the pixels whose wall voltage has been formed by the Address Discharge. (Optical output for displaying a picture is generated).

③ Erase Discharge: To selectively perform Address Discharge for each pixel, all pixels on the panel should be in the same status (the wall electric charge status and space electric charge status must be the same). Therefore, the Erase Discharge section is an important component for guaranteeing the drive margin, and is implemented by various methods such as applying a log waveform. However, the current 42HD V4 has adopted a wall voltage control through an RA (Repeated Auto-quenching) reset that separates the discharge area and performs switching to perform an efficient erase operation, while the gradient was the same in the RAMP section in the existing approach.

1) Address Discharge

A discharge that is caused by the difference between the plus electric potential (Va apply voltage of 65~70V + Positive Wall Charge) of the electrode and the negative electric potential (Applied GND Level + Negative Wall Charge) of the Y electrode. The Address discharge forms a wall voltage within the pixel to display color (to be discharged) before the Sustain Discharge period. That is, the pixel whose wall charge has been formed by the Address Discharge forms a Sustain Discharge vis the following Sustain pulse.

2) Sustain Discharge

A Sustain Discharge is a Self-Sustaining Discharge formed by the accumulation of the electric potential of the Sustain pulse (generally 200 ~ 210 Volt) alternating over the X and Y electrodes during the sustain period, and the wall charge depending on whether the pixel has previously been discharged or not. That is, it is controlled by the memory characteristics, one of the basic characteristics of the AC PDP (in that the past operating conditions determine the current status). That is, if a wall voltage exists on the pixel (if the pixel is on), a discharge is formed again because the applied voltage, which is the sum of the following applied Sustain voltage and the wall voltage, is higher than the discharge threshold voltage. If no wall voltage exists on the pixel (if the pixel is off), a discharge will not occur because the Sustain voltage is not higher than the discharge threshold voltage. The Sustain Discharge period is the period for generating actual optical output so as to display a picture on the PDP screen.

3) Erase Discharge

The purpose of a Reset (Erase) Discharge is to create uniformity of the wall voltage within all panel pixels. It evens the wall voltages regardless of the Sustain Discharge in the previous stage. The Erase Discharge has to remove the wall voltage introduced by the Sustain Discharge by supplying ions or electrons by a discharge. When the wall voltage is removed through a discharge, the time when the reverse polarity is applied to the wall voltage (fine width erasing) is to be limited or ions or electrons are to be supplied by a weak discharge (low voltage erasing) so as to prevent a wall charge in reverse polarity.

There are 2 known weak discharge (low-voltage) erase methods. 1) A log waveform adopted by F company and 2) a weak erase discharge via a ramp waveform adopted by Matsushita and other companies. Both methods control the externally applied voltage by the difference of the wall voltage of the pixel by applying the rising gradient of the erasing waveform slowly, because the discharge begins when the sum of the existing remaining wall voltage and the rising waveform voltage exceeds the drive threshold voltage. In addition, a weak discharge is introduced, because the applied voltage is low.

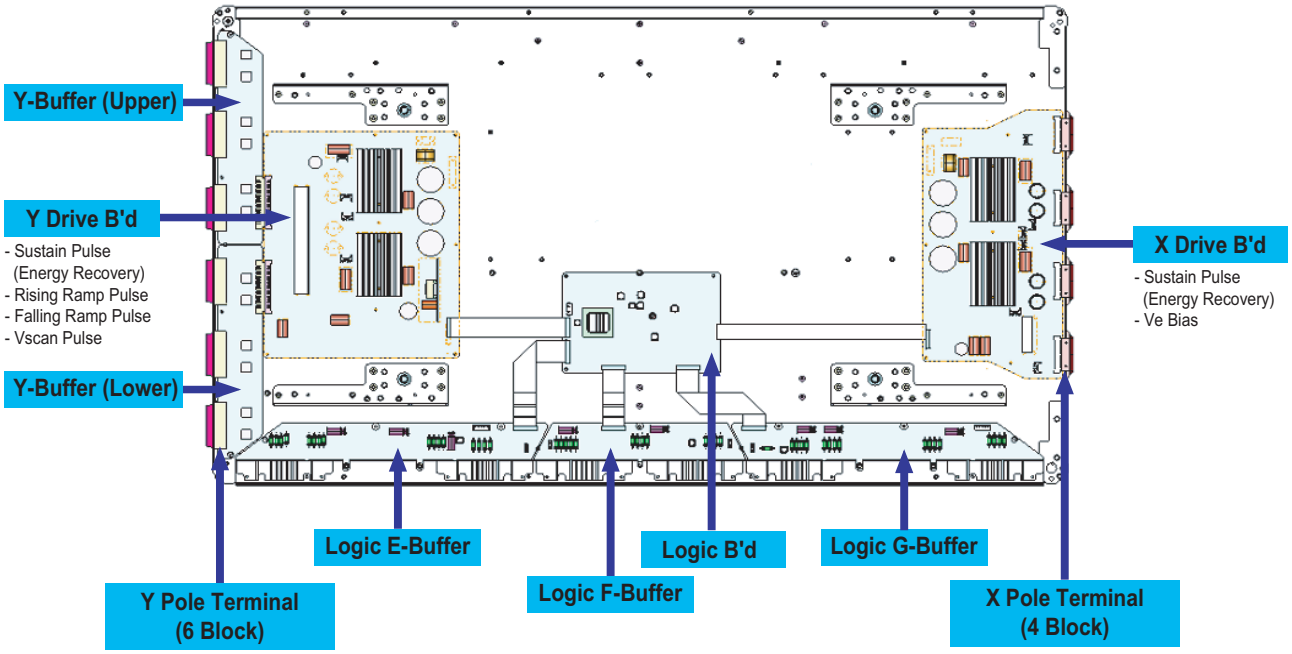
■ Requisite Components Necessary for Drive Board Operation

1) Power
- Supplied from the power board. The optimal value may differ from the following:
  a) Vs : 200V - Sustain
  b) Vset : 190V - Y Rising Ramp
  c) Ve : 110V - Ve bias
  d) Vscan : -190V - Scan low bias
  e) Vsc_h : -70V - Scan high bias (Created by the DC-DC power block of the Y Drive board)
  f) Vdd : 5V - Logic signal buffer IC
  g) Vcc : 15V - Gate drive IC

2) Logic Signal
- Supplied by the Logic board
- Gate signal of each switch

■ Drive Circuit Architecture and Function Description

- Description of the function of each board



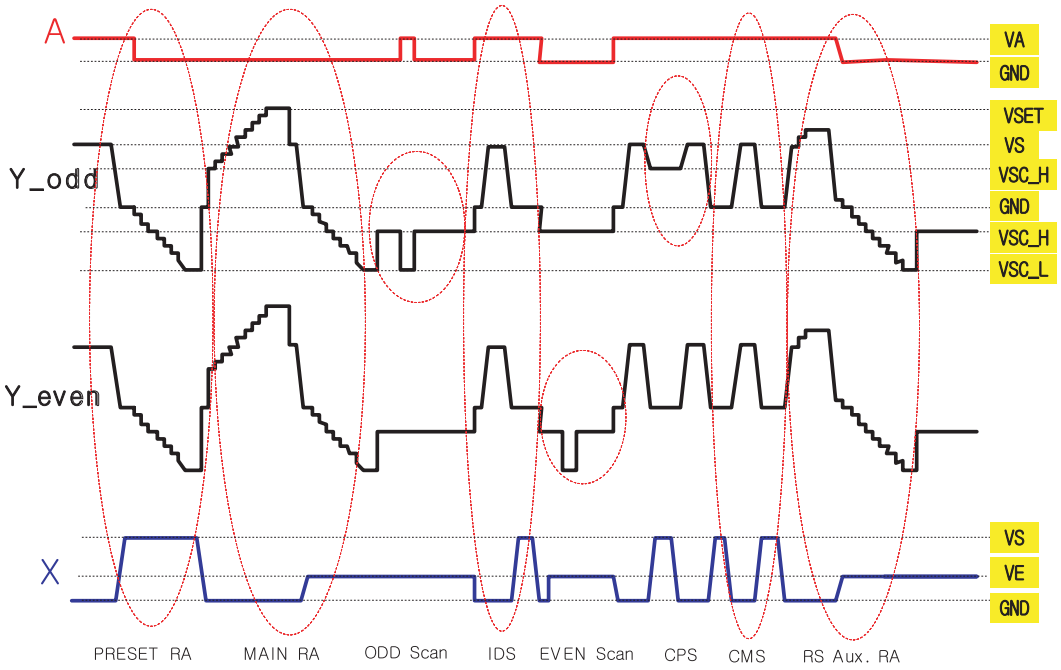
1) X Drive Board
This is connected to the X port part of the panel. 1) Sustain voltage waveform (including ERC) is output, and 2) Ve bias in the Scan section is maintained.

2) Y Drive Board
This is connected to the Y port part of the panel. It outputs 1) Sustain voltage wave form (including ERC), and 2) Y Rising, Falling Ramp waveform, and maintains 3) Vscan bias.

3) Y Buffer Board
A board, which applies the Scan waveform to the Y terminal block, consists of 12 Scan Driver ICs (TI SN755870: 64 Outputs).

■ Drive Waveform Specifications

- Drive Waveform



- Description of the function of each pulse

1) Y Preset RA Pulse
This is supplied to the first sub-field and erases the discharge status of the previous subfield.

2) Y Main RA Pulse
During the Y Rising Ramp section, approximately 300V~350V (Vscan-h + Vset) of external voltage is supplied to the Y electrode, and a weak discharge is started when each gap voltage is equal to the discharge start voltage. While maintaining the weak discharge, as a whole, negative wall charges are accumulated on the Y electrode and positive wall charges on the X electrode and the address electrode.
During the Y Falling Ramp section, the negative wall charges accumulated on the Y electrode by the approximately 105V of X bias are used to erase the positive wall charges on the X electrode, and the address electrode maintains most of the positive wall charges accumulated during the (0V) Rising Ramp section preparing for the next address discharge.

3) Y Scan Pulse (Odd/Even)
A scan pulse classifies the Y electrode into Odd and Even lines and selects FPC output electrodes sequentially (one line-at-a-time). At this time, Vscan is called the Scan Bias Voltage.
A Vscan voltage of approximately -175 Volt (Vsc_1) is supplied to the electrode lines. For the other lines, -56 volt (Vsc_h is higher than Vscan-l by 120V) is supplied. However, negative wall charges are accumulated on the Y electrode by the Ramp pulse, and positive wall charges are accumulated on the address electrode, and the voltage applied to the cells, to which the Address pulse (70V~75V) has been applied, becomes higher than the discharge voltage. An address Discharge occurs as a result. Since the Scan and Data pulse is applied one line at a time as above, the address time of PDP is very long.

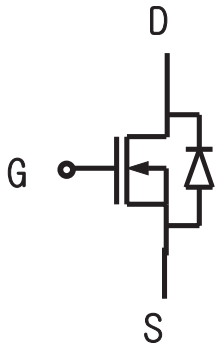
4) IDS Pulse (InDependent Sustain Pulse)
Since an Odd Scan is performed first, the Odd line output sustains optical twice during the IDS section. At this time, a Sustain Discharge does not occur for the Even line because the Even line is not scanned.

5) CPS Pulse (ComPare Sustain Pulse)
By floating the Odd line that caused the Sustain Discharge in the IDS section to the Vscan-h level, and introducing the Sustain Discharge only for Even lines, it compensates for the optical output difference between the Even and Odd lines.

6) CMS Pulse (ComMon Sustain Pulse)
Actual optical is output during the common Sustain Discharge section.

■ Mechanism of the FET Operation and High-Voltage Switching

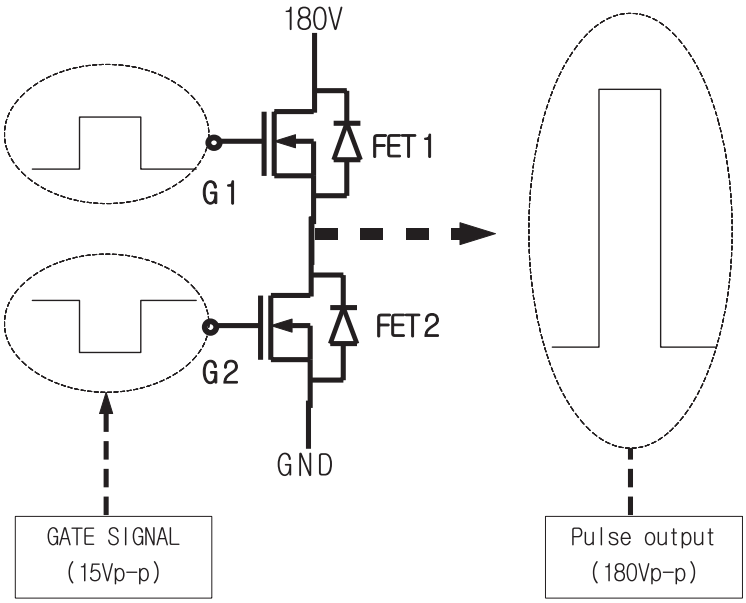
Mechanism of the FET Operation



G : Gate
S : Source
D : Drain

1) When the signal is output to the gate, (positive electric potential) FET short circuits
(i.e. Conductor of resistance 0)
2) When no signal is output to the gate (GND), FET changes to an open circuit (i.e. an insulator of resistance ∞).

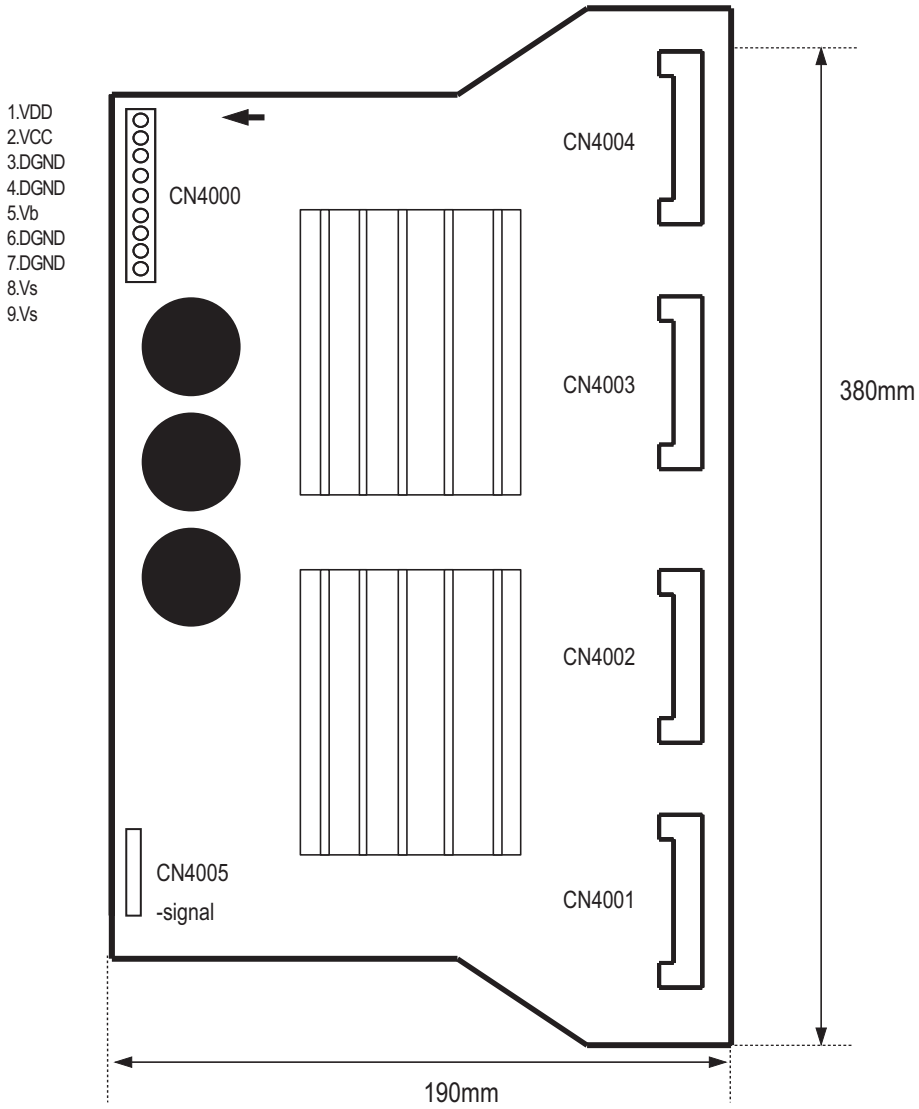
High-Voltage Switching of the FET Operation



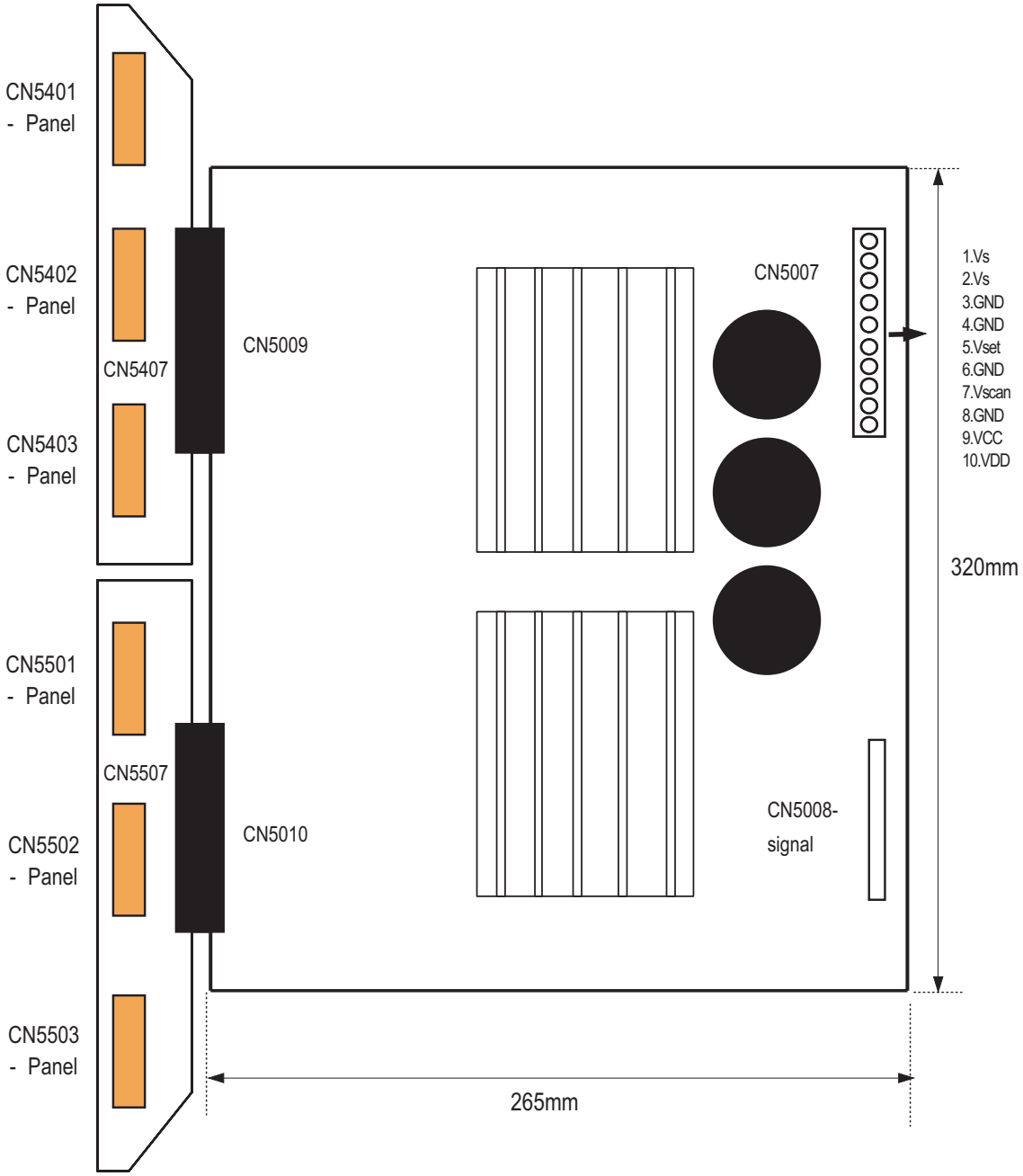
1) When no signal is applied to G1, FET1 is opened and when the signal is applied to G2, FET2 short circuits, GND is output via the output terminal.
2) When a signal is applied to G1, FET1 short cir cuits and when no signal is applied to G2, FET2 is opened, and 180V is output via the output terminal.

■ Drive Board Connector Layout

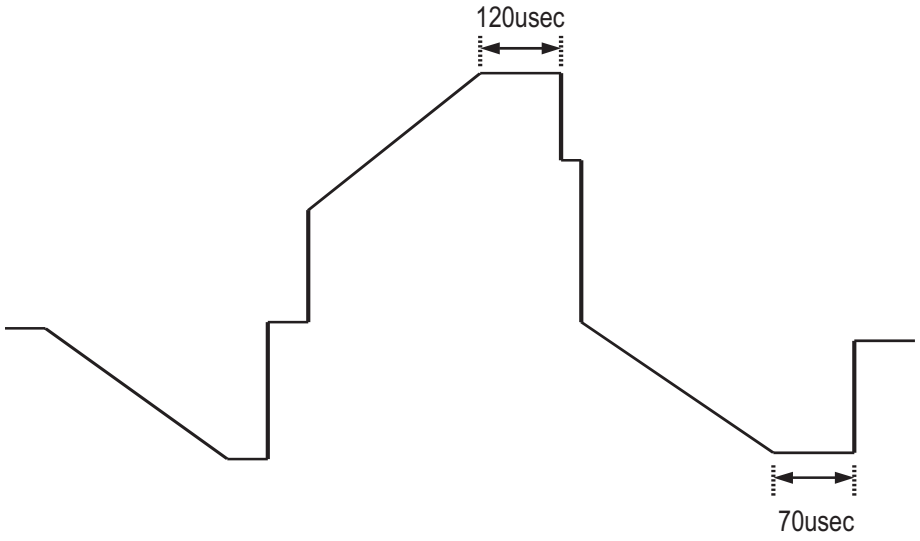
1) X-Main Board

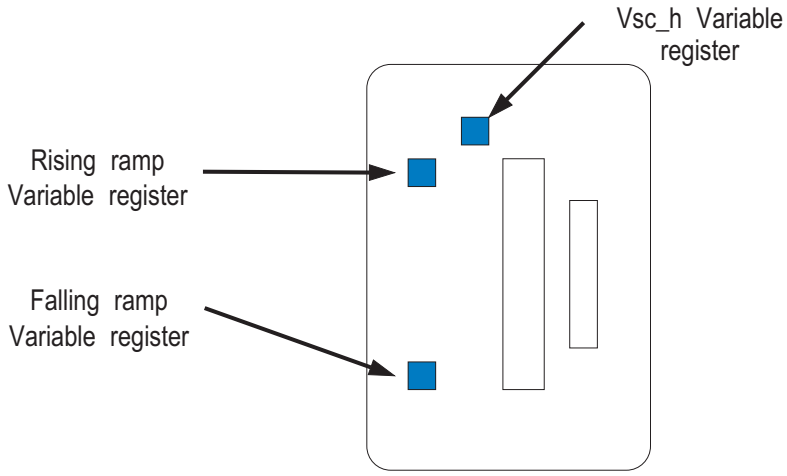


2) Y-Main Board



▶ Adjust the drive waveform so that the main reset (rising, falling:40usec) is the same as those in the F/W pattern.
(※ Attachment 1 reference)



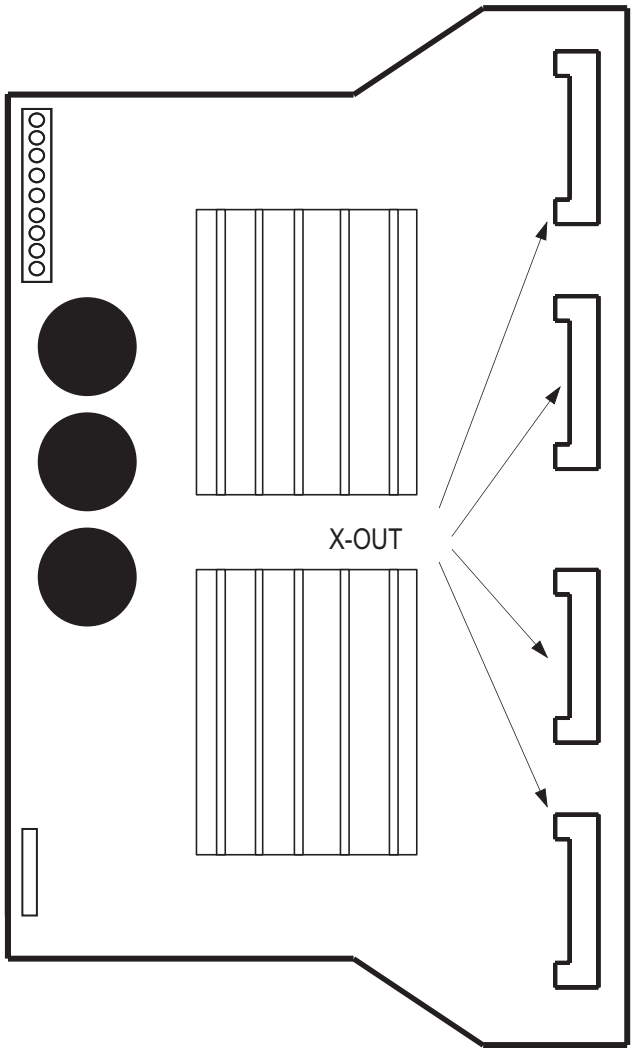


< Y-Main >

<Voltage Adjustment Specifications>

Vset	Vs	Vsc_l	Vsc_h	Ve	Va
190V	200V	-190V	-70V	115V	65V

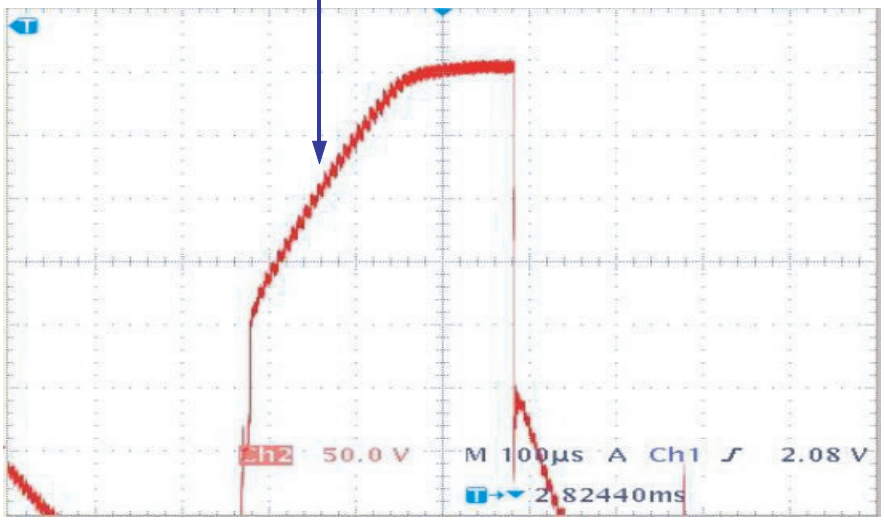
▶ Check that the output of X-Out of the X board follows the waveform of ※Attachment 2 when the power is supplied.



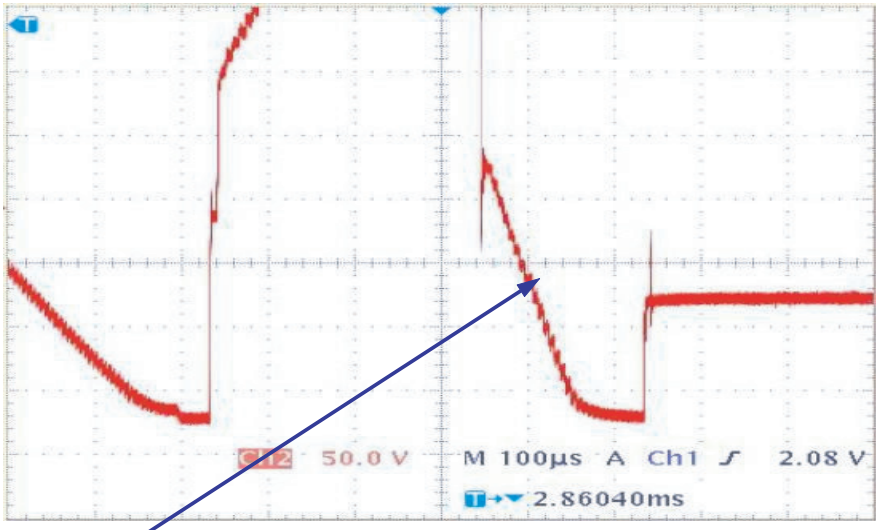
※ Attachment 1

■ Y Output Waveform

Rising Ramp

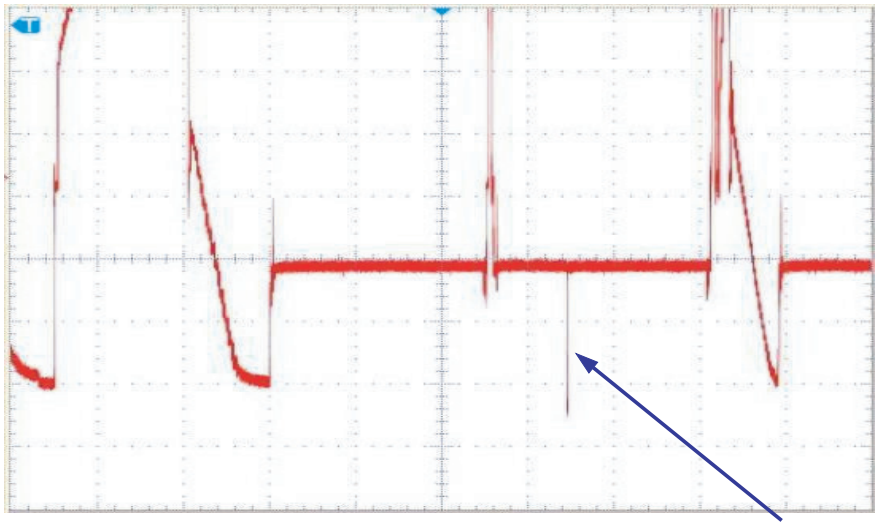


< Rising Ramp >

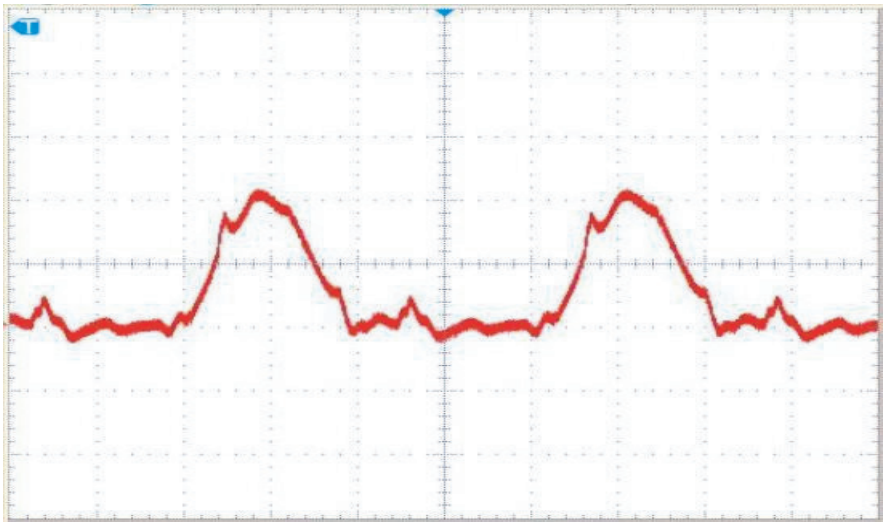


Falling Ramp

< Falling Ramp >



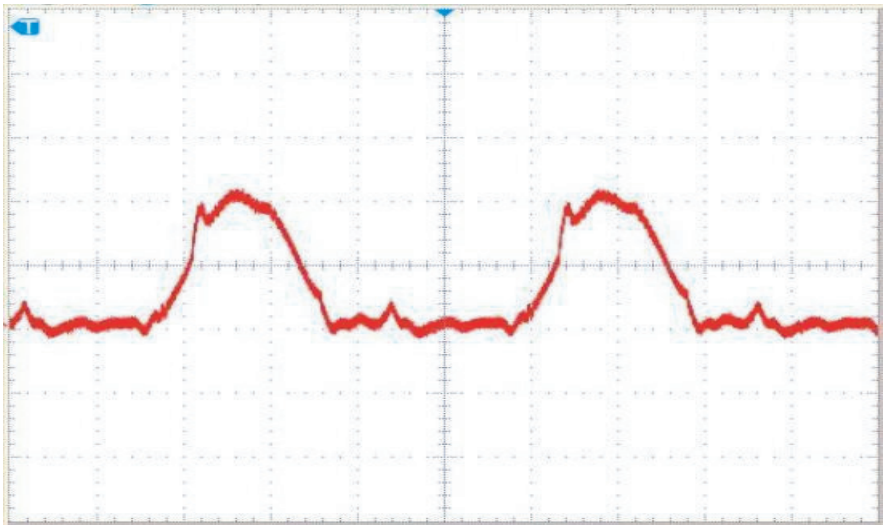
< Even_Scan >



< Y Sustain >

※ Attachment 2

■ X Output Waveform



< X Sustain >

MEMO