4. Circuit Description (VE710s-2/VE710b-2/VA721)

A. Scaling controller

The ADC is to convert RGB analog signal to digital signal that scaling chip can acknowledge.
The HSYNC input receives a logic signal and provides the frequency reference for pixel clock generation.
The scaling IC is to converts the input signal ranging from VGA to SXGA into SXGA resolution that panel can acknowledge.

GENERAL DESCRIPTION

The MST8116A is a high performance, and fully integrated graphics processing IC solution for LCD monitors with resolutions up to SXGA. It is configured with an integrated triple-ADC/PLL, a high quality scaling engine, an on-screen display controller, a built-in output clock generator, a panel timing controller (TCON), and RSDS display interface. To further reduce system costs, the MST8116A also integrates intelligent power management control capability for green-mode requirements and spread-spectrum support for EMI management.

PIN DESCRIPTION

CPU Interface

Pin Name Pin Type Function Pin

HWRESET Schmitt Trigger Input
w/ 5V-tolerant Hardware reset; active high 32
CS Input w/ 5V-tolerant 3 Wire Serial Bus Chip Select; active high 69
SDA I/O w/ 5V-tolerant 3 Wire Serial Bus Data; 4mA driving strength 70
SCL Input w/ 5V-tolerant 3 Wire Serial Bus Clock 71
INT Output CPU interrupt; 4mA driving strength 72

Analog Interface

Pin Name Pin Type Function Pin

HSYNC0 Schmitt Trigger Input
w/ 5V-tolerant Analog HSYNC input 37
VSYNC0 Schmitt Trigger Input
w/ 5V-tolerant Analog VSYNC input 38
REFP Internal ADC top de-coupling pin 66
REFM Internal ADC bottom de-coupling pin 67
RIN0 Analog Input Analog red input 63
RIN0M Analog Input Reference ground for analog red input 62
SOGIN0 Analog Input Sync-on-green input 61
GIN0 Analog Input Analog green input 60
GIN0M Analog Input Reference ground for analog green input 59
BIN0 Analog Input Analog blue input 58
BIN0M Analog Input Reference ground for analog blue input 57
REXT External resistor 390 ohm to AVDD 52

RSDS Interface

Pin Name Pin Type Function Pin

CLKAP Output A-Link Positive RSDS Differential Clock Output from "Odd" Channel 118
CLKAN Output A-Link Negative RSDS Differential Clock Output from "Odd" Channel 119
CLKBP Output B-Link Positive RSDS Differential Clock Output from "Even" Channel 120
CLKBN Output B-Link Negative RSDS Differential Clock Output from "Even" Channel 121
BA[3:1]P Output A-Link Positive RSDS Differential Data Output from "Odd" Channel 92, 90, 88
BA[3:1]N Output A-Link Negative RSDS Differential Data Output from "Odd" Channel 93, 91, 89
GA[3:1]P Output A-Link Positive RSDS Differential Data Output from "Odd" Channel 102, 100, 98
GA[3:1]N Output A-Link Negative RSDS Differential Data Output from "Odd" Channel103, 101,99
RA[3:1]P Output A-Link Positive RSDS Differential Data Output from "Odd" Channel 112, 110, 108
RA[3:1]N Output A-Link Negative RSDS Differential Data Output from "Odd" Channel 113, 111, 109
BB[3:1]P Output B-Link Positive RSDS Differential Data Output from "Even" Channel 4, 128, 124
BB[3:1]N Output B-Link Negative RSDS Differential Data Output from "Even" Channel 5, 1, 125
GB[3:1]P Output B-Link Positive RSDS Differential Data Output from "Even" Channel 14, 12, 8
GB[3:1]N Output B-Link Negative RSDS Differential Data Output from "Even" Channel 15, 13, 9
RB[3:1]P Output B-Link Positive RSDS Differential Data Output from "Even" Channel 24, 22, 16
RB[3:1]N Output B-Link Negative RSDS Differential Data Output from "Even" Channel 25, 23, 17
GPO[8:5] Output TCON GPO[8:5]; 4mA driving strength 29, 28, 30,31
GPO[4:0] Output w/ Pull-down TCON GPO[4:0]; 4~12mA driving strength programmable 79-83
OINV Output w/ Pull-down Resistor TCON "Odd" Channel Inversion; 4~12mA driving strength programmable 78
EINV Output w/ Pull-down Resistor TCON "Even" Channel Inversion; 4~12mA driving strength programmable 77
OSP Output w/ Pull-down Resistor TCON "Odd" Channel Start Pulse; 4~12mA driving strength programmable 76
ESP Output w/ Pull-down Resistor TCON "Even" Channel Start Pulse; 4~12mA driving strength programmable 75

GPIO Interface

Pin Name Pin Type Function Pin

GOUT1/PWM1 Output GOUT1/PWM1; 4mA driving strength 74
GOUT0/PWM0 Output GOUT0/PWM0; 4mA driving strength 73
Misc. Interface
Pin Name Pin Type Function Pin
BYPASS For External Bypass Capacitor 3
XIN Crystal Oscillator Input Xin 33
XOUT Crystal Oscillator Output Xout 34
Power Pins
Pin Name Pin Type Function Pin
AVDD 3.3V Power ADC Power 45, 51, 55, 65
AVSS Ground ADC Ground 39, 42, 48, 56,
64, 68
AVDD_PLL 3.3V Power PLL Power 53
AVSS_PLL Ground PLL Ground 54
AVDD_MPLL 3.3V Power MPLL Power 35
AVSS_MPLL Ground MPLL Ground 2, 36
VDDP 3.3V Power Digital Output Power 11, 21, 84, 94,
104, 114, 126
GNDP Ground Digital Output Ground 10, 20, 85, 95,
105, 115, 127
VDDC 2.5V Power Digital Core Power 18, 87, 97, 117
GNDC Ground Digital Core Ground 19, 86, 96, 116
No Connects
Pin Name Pin Type Function Pin
NC No Connect. Leave These Pins Floating.
6, 7, 26, 27, 40,
41, 43, 44, 46,
47, 49, 50, 106,
107, 122, 123
Resolution 8 Bits
DC ACCURACY
Differential Nonlinearity ±0.5 +1.50/-1.0 LSB
Integral Nonlinearity ±1 LSB
No Missing Codes Guaranteed
ANALOG INPUT
Input Voltage Range
Minimum 0.5 V p-p
Maximum 1.0 V p-p
Input Bias Current 1 uA
Input Full-Scale Matching 1.5 %FS
Brightness Level Adjustment 62 %FS
SWITCHING PERFORMANCE
Maximum Conversion Rate 165 MSPS
Minimum Conversion Rate 20 MSPS
HSYNC Input Frequency 15 200 kHz
PLL Clock Rate 20 162.5 MHz
PLL Jitter 500 ps p-p
Sampling Phase Tempco TBD ps/°C
DIGITAL INPUTS
Input Voltage, High (VIH) 2.5 V
Input Voltage, Low (VIL) 0.8 V
Input Current, High (IIH) -1.0 uA
Input Current, Low (IIL) 1.0 uA
Input Capacitance 5 pF
DIGITAL OUTPUTS
Output Voltage, High (VOH) VDDP-0.1 V
Output Voltage, Low (VOL) 0.1 V
DYNAMIC PERFORMANCE
Analog Bandwidth, Full Power 250 MHz
Channel to Channel Matching 0.5% Full-Scale
3.3V Supply Voltages VVDD_33 -0.3 3.6 V
2.5V Supply Voltages VVDD_25 -0.3 2.75 V
Input Voltage (5V tolerant inputs) VIN5Vtol -0.3 5.0 V
Input Voltage (non 5V tolerant inputs) VIN -0.3 VVDD_33 V

B. MTV312M64

The MTV312M micro-controller is an 8051 CPU core embedded device especially tailored for CRT/LCD
Monitor applications. It includes an 8051 CPU core, 1024-byte SRAM, 14 built-in PWM DACs, VESA DDC interface, 4-channel A/D converter, and a 64K-byte internal program Flash-ROM.
A “CMOS output pin” means it can sink and drive at least 4mA current. It is not recommended to use such
pin as input function.
A “open drain pin” means it can sink at least 4mA current but only drive 10~20uA to VDD. It can be used as input or output function and

needs an external pull up resistor.
A “8051 standard pin” is a pseudo open drain pin. It can sink at least 4mA current when output is at low level, and drives at least 4mA current for 160nS when output transits from low to high, then keeps driving at 100uA to maintain the pin at high level. It can be used as input or output function. It needs an external pull up resistor when driving heavy load device.

POWER CONFIGURATION
The MTV312M can work on 5V or 3.3V power supply system.
In 5V power system, the VDD pin is connected to 5V power and the VDD3 needs an external capacitor, all output pins can swing from 0~5V, input pins can accept 0~5V input range.
And ADC conversion range is 5V. However, X1 and X2 pins must be kept below 3.3V.
In 3.3V power system, the VDD and VDD3 are connected to 3.3V power, all output pins swing from 0~3.3V, HSYNC, VSYNC and open drain pin can accept 0~5V input range, other pins must be kept below 3.3V. And the ADC conversion range is 3.3V.

C. *INVERTER*

In order to drive the CCFLs embedded in the panel module, there is a half bridge inverter to convert by the controller.
The input 12V up to hundreds of AC voltage output.
The inverter is formed by symmetric in order to drive the separate lamp modules.
The input stage consists of a PWM controller, half bridge inverter, and switching MOSFET to convert DC input into AC output.
The output stage consists of a tuning capacitor, coupling capacitor, transformer, push-pull MOSFET pair to boost AC output up to hundreds of voltage.
And one resister is serial to lamp for output voltage feedback.
There are two signal to control the inverter which come from system.
Logic “high” level which send to I901 is turn on the inverter.
BRI signal control brightness by DC level which was integral from PWM signal.