COLOR TFT-LCD TV
SERVICE MANUAL

MODEL : LT-32HTFH

CAUTION !!
BEFORE SERVICING THE TFT-LCD TV,
READ THE SAFETY PRECAUTIONS IN THIS MANUAL.

SERVICE MANUAL	

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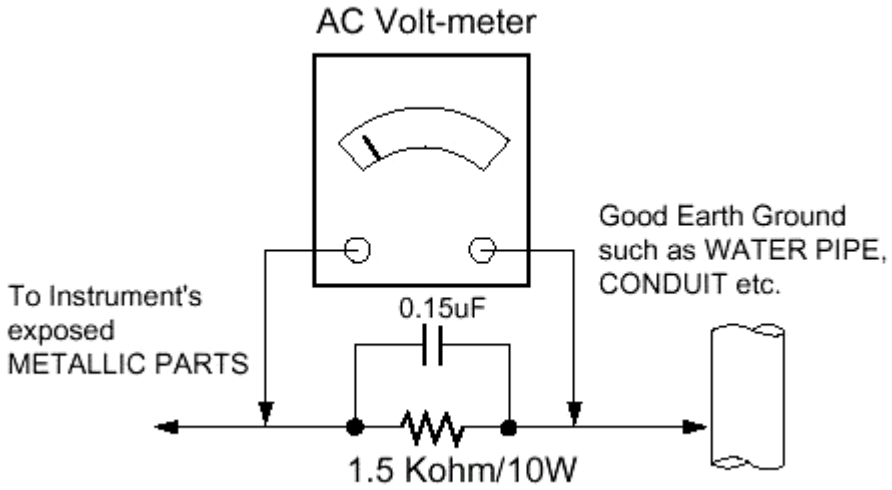
SAFETY PRECAUTIONS

!! Important Safety Notice !!

Many electrical and mechanical parts in this chassis have special safety-related characteristics.
These parts are identified by in the Schematic Diagram and Replacement Parts List.
It is essential that these special safety parts should be replaced with the same components as recommended in this manual to prevent Shock, Fire, or other Hazards.
Do not modify the original design without permission of manufacturer.

Leakage Current Hot Check (See below Figure)
Plug the AC cord directly into the AC outlet.
Do not use a line Isolation Transformer during this check.
Connect 1.5K/10watt resistor in parallel with a 0.15uF capacitor between a known good earth ground (Water Pipe, Conduit, etc.) and the exposed metallic parts.
Measure the AC voltage across the resistor using AC voltmeter with 1000 ohms/volt or more sensitivity.
Reverse plug of the AC cord into the AC outlet and repeat AC voltage measurements for each exposed metallic part. Any voltage measured must not exceed 0.75 volt RMS, which is, corresponds to 0.5mA.
In case any measurement is out of the limits specified, there is possibility of shock hazard and the set must be checked and repaired before it is returned to the customer.

Leakage Current Hot Check circuit



SERVICING PRECAUTIONS

CAUTION!!
Before servicing receivers covered by this service manual, read and follow the SAFETY PRECAUTIONS on page 2 of this publication.

General Servicing Precautions
1.Always unplug the receiver AC power cord from AC power source before;
ⓐRemoving or reinstalling any component, circuit board module or any other receiver assembly.
ⓑDisconnecting or reconnecting any receiver electrical plug or other electrical connection.
ⓒConnecting a test substitute in parallel with an electrolytic capacitor in the receiver.
CAUTION!! A wrong part substitution or incorrect polarity installation of electrolytic capacitors may result in an explosion harzard.
2.Do not spray chemicals on or near this receiver or any of its assemblies.
3.Do not defect any plug/socket voltage interlocks with which receivers covered by this service manual might be equipped.
4.Always connect the test receiver ground lead to the receiver chassis ground before connecting the test receiver positive lead. Always remove the test receiver ground lead last.
5.Do not connect the test fixture ground strap to power supply heatsink in this receiver

Electrostatically Sensitive(ES) Devices
Some semiconductor(solid state) devices can be damaged easily by static electricity. Such components commonly are called Electrostatically Sensitive(ES) Device.Examples

Circuit Board Foil Repair
Excessive heat applied to the copper foil of any printed circuit board will weaken the adhesive that bonds the foil to the circuit board causing the foil th separate from or “lift-off” the board.
The following guidelines and procedures should be flollowed whenever this condition is encountered.

At IC Connections
To repair a defective copper pattern at IC connections use the following procedure to install a jumper wire on the copper pattern side of the circuit board.(Use this technique only on IC connections.)

1.Carefully remove the damaged copper pattern with a sharp knife.
(Remove only as much copper as absolutely necessary.)
2.Carefully scratch away the solder resist and acrylic coating(if used) from the end of the remaining coopper pattern.
3.Bend a small “U” in one end of a small guage jumper wire and carefully crimp it around the IC pin.
4.Route the jumper wire along the path of the out-away copper pattern and let it overlap the previously scraped end of the good copper pattern. Solder the overlapped area and clip off any excess jumper wire.

SPECIFICATIONS

Note: Specifications and others are subject to change without notice for improvement.

1.Scope.
This document is the specification of 32" TFT-LCD Color TV.

2.Power
1) Power requirement
150W

2) AC / DC SMPS.
Input Frequency : 50 / 60㎐
Input Voltage: AC 100V- 240V 2.5A ~1.5A
Output Voltage: DC 12V, 24V

3) Power cord
Use UL listed and CSA certified detachable power cord type; SVT, 3-conductors, 18AWG For AC 120V area. Use VDE listed detachable power cord type; HO5VV-F, 3-conductors, 18AWG for AC 220 240V area.

3.Tuning system
FVS 100 Program

4.Sound output
10W+10Wrms Stereo (Max)

5.Antenna input impedance
VHF / UHF at 75ohm

6.OSD Type (On Screen Display)
Windows type (Center)

7.External in/output
HDMI INPUT, PC ANALOG INPUT, PC AUDIO INPUT, HEADPHONE OUTPUT, SVC port
S-VIDEO AUDIO INPUT, S-VIDEO INPUT, COMPONEN INPUT, COAXIAL OUT,
SCART 1(FULL), SCART 2(HALF), TUNER

8. Function
CATV/Hyper band
Auto Program
Manual Program
Auto Sleep
Quick view
ACMS(Auto channel Memory System)
PSM(Picture Status memory)
SSM(Sound Status memory)
PIP **:** COMPONET, PC-ANALOG, HDMI(Main) – Tuner, SCART 1, SCART 2, S-Video(Sub)
TUNER, SCART1, SCART2, S-Video(Main) – PC ANALOG, HDMI, COMPONET(Sub)
ARC(ASPECT RATIO CONTROL)

SPECIFICATIONS

9.Receiving RF TV system

NO	Model System	LT-32HTFH	/	/
1	PAL-B	○	/	/
2	PAL-G	○	/	/
3	PAL-I, I /I	○	/	/
4	PAL-D	○	/	/
5	PAL-K	○	/	/
6	SECAM-B	○	/	/
7	SECAM-G	○	/	/
8	SECAM-D	○	/	/
9	SECAM-K	○	/	/
10	SECAM-K1	○	/	/
11	SECAM-I (6.0)	○	/	/
12	NTSC-3.58 / 4.5	X	/	/
13	NTSC-3.58 / 5.5	X	/	/
14	NTSC-3.58 / 6.0	X	/	/
15	NTSC-3.58 / 6.5	X	/	/
16	NTSC-3.58 / 4.5(5.0)	X	/	/
17	NTSC-4.43 / 5.5	X	/	/
18	NTSC-4.43 / 6.0	X	/	/
19	NTSC-4.43 / 6.5	X	/	/
20	PAL 5.5 / 60Hz	○	/	/
21	PAL 6.0 / 60Hz	○	/	/
22	PAL 6.5 / 60Hz	○	/	/
23	SECAM 5.5 / 60Hz	○	/	/
24	SECAM 6.0 / 60Hz	○	/	/
25	SECAM 6.5 / 60Hz	○	/	/
26	SECAM L / L'	○	/	/
	TOTAL SYSTEM	18	/	/

SPECIFICATIONS

10. PC Mode Scan Frequency & Timing

1) Scan Freq: H: 31 56 kHz / V: 56 75Hz

2) Preset Timing Chart

Mode	Best resolution	Horizontal frequency(KHz)	Vertical frequency(Hz)
XGA	1024 x 768	48.4 KHz	60 Hz
	1024 x 768	56.5 KHz	70 Hz
	1024 x 768	60.0 KHz	75 Hz

Note!! :

ⓐ If the set is cold, there may be a small “flicker” when the set is switched on. This is Normal, there is nothing wrong with the set.

ⓑ If possible, use the XGA 1024 x 768@60HZ video mode to obtain the best image quality for your LCD monitor. If used under the other resolutions, some scaled or processed pictures may appear on the screen.

ⓒ Some dot defects may appear on the screen, like Red, Green or Blue spot. However, this will have no impact or effect on the monitor performance.

SPECIFICATIONS

11. TFT – LCD Panel Character

Description

LTA320W2-L03 is a color active matrix TFT(Thin Film Transistor) liquid crystal display(LCD) that uses amorphous silicon TFTs as a switching devices. This model is composed of a TFT LCD panel, a driver circuit and a back-light system. The resolution of a 32.0" contains 1366 X 768 pixels and can display up to 16.7 million colors with wide viewing anale of 85 ° or higher in all directions.

Features

- High contrast ratio, high aperture structure
- APVA(Advanced Patterned Vertical Align) mode
- Wide verwing anale(±170°)
- High speed response
- WXGA(1366 X 768 pixels) resolution(16:9)
- Low Power consumption
- Dyrect Type 16 CCFL(Cold Cathode Fluorescent Lamp)
- DE only mode
- LVDS(Low-Voltage Differential Signal) interface.(1pixel/clock)

Applications

- Home-alone Multimedia TFT-LCD TV
- Display terminals for AV applications products
- High Definition TV(HD TV)

● Feature

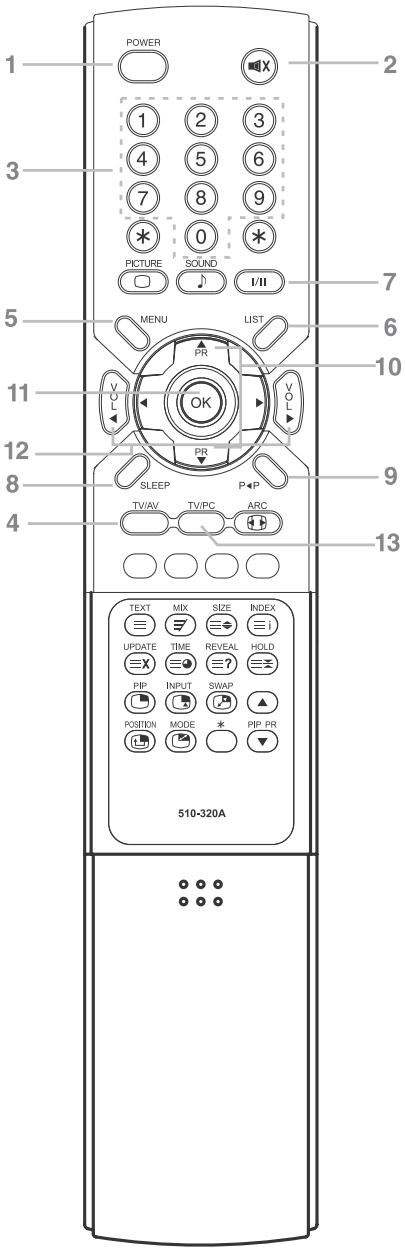
Size	32.0 inches
Driver element	a-si TFT Active Matrix
Display area	697.6845mm(H) X 392.256mm(V)
Display colors	16.7M(true)
Number of Pixels	1366 X 768 Pixel(16:9)
Pixel arrangement	RGB Vertical Stripe
Pixel Pitch	0.51075mm (H) x 0.51075mm(W)
Display mode	Normally Black
Surface treatment	Haze 44%, Hard-Coating(3H)

LOCATION OF CONTROL

All the functions can be controlled with the remote controller. Some functions can also be adjusted with the buttons on the side panel of the set.

Remote controller

Before you use the remote controller, please install the batteries.



1. POWER

Turns the TV on from standby or off to standby mode.

2. MUTE

Turns the sound on and off.

3. NUMBER buttons

Selects programme numbers.

4. TV/AV

Selects TV, VIDEO, S-VIDEO,
RADIO(Only when the set is Radio On.),
COMPONENT1/2, PC ANALOG, HDMI mode.
Clears the menu from the screen.

5. MENU

Displays a main menu.

6. LIST

Displays the programme list menu.

7. I/II

Selects the language during dual language broadcast.
Selects the sound output.

8. SLEEP

Sets the sleep timer.

9. P◀P

Returns to the previously viewed programme.

10. PR▲/PR▼ (Programme Up/Down)

Selects next programme or a menu item.

11. OK

Accepts your selection or displays the current mode.

12. VOL◀/VOL▶ (Volume Up/Down)

Adjusts the sound level.

13. TV/PC

Selects TV or PC mode directly.

LOCATION OF CONTROL

14. PICTURE( )
Recalls your preferred picture setting

15. SOUND(♪)
Recalls your preferred sound setting

16. ARC( )
You can watch TV in various picture formats; **Auto, 16:9, 14:9, 4:3, 16:9 Zoom, 14:9 Zoom, 4:3 Zoom.** Repeatedly press the **ARC** button to select your desired picture format.
Note. 16:9 and 4:3 in PC mode are available.

17. TELETEXT buttons
These buttons are used for Teletext.
For further details, see the 'Teletext' section.

18. INPUT( )
Selects the AV source of sub picture in PIP mode.

19. PIP( )
Displays a PIP(Picture In Picture) screen.

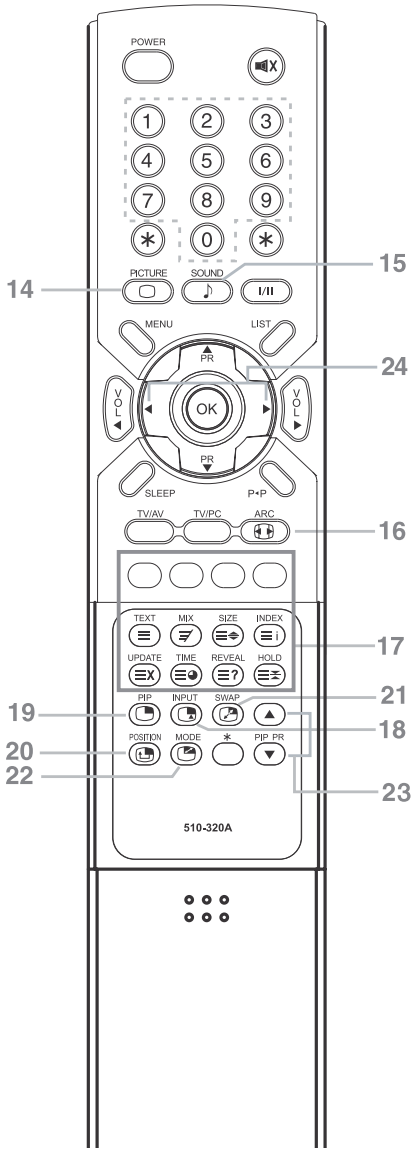
20. POSITION( )
Selects a position of PIP screen.

21. SWAP( )
Switches a main picture to sub picture in PIP mode.

22. MODE( )
Selects a PIP screen mode. – 16:1, 9:1 and 3:1 mode.

23. PIP PR▲/PIP PR▼
Selects a programme when RF signal is displayed in PIP mode.

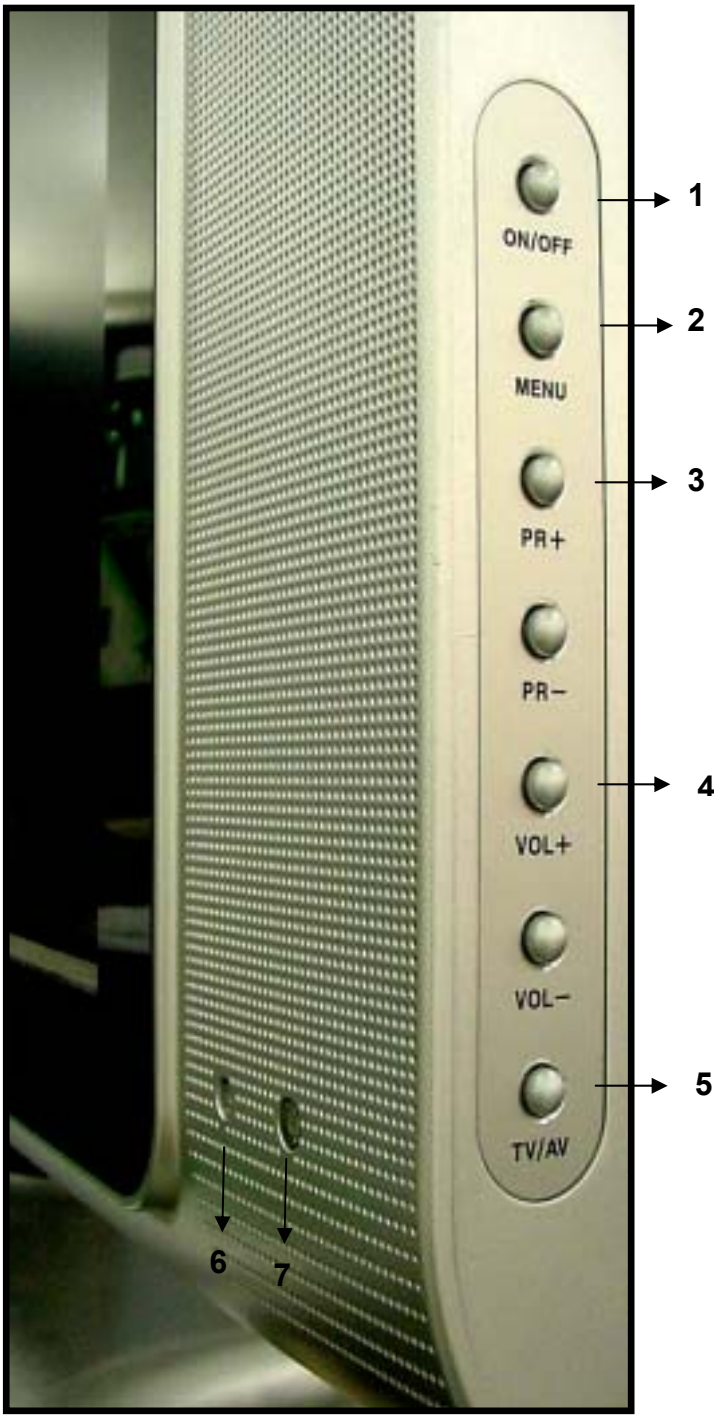
24. ◀▶
Adjusts menu settings.



LOCATION OF CONTROL

1-3. Controller of Panel

< SIDE VIEW>



1.ON/OFF:
Switches TV set on or off.

2.MENU:
Display a menu.

3.+ PR - (Programme Up/Down):
Selects a programme or a menu item.

4.+ VOL -(Volume Up/Down):
Adjusts the volume.
Adjusts menu settings.

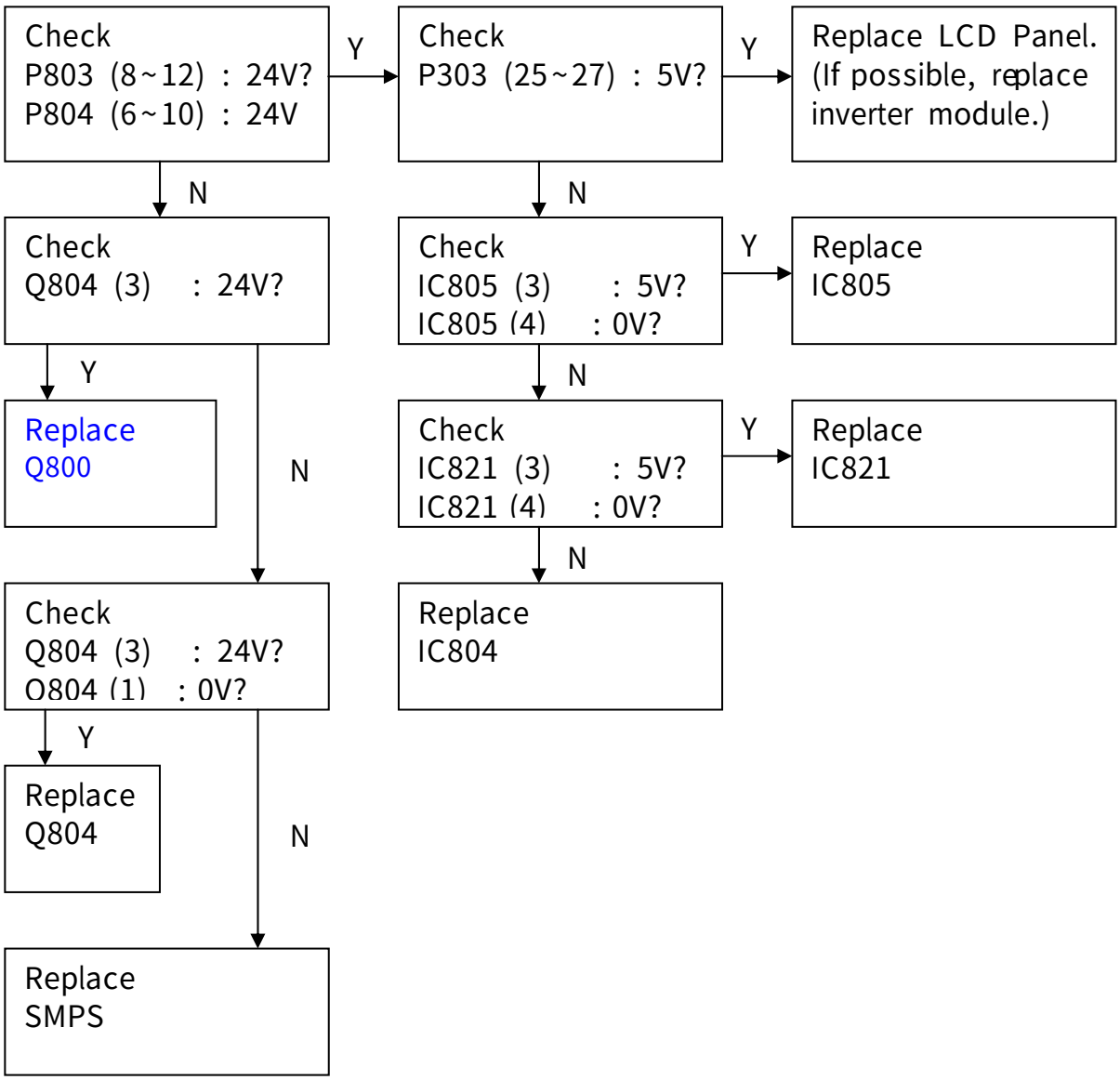
5.TV/AV:
Selects input signal source.
Clears the menu from the screen.

6:POWER INDICATOR:
Illuminates red when the TV is in-power standby mode.
Illuminates green when the TV is-switched power on mode.
Illuminates amber when the TV is-switched power saving mode.

7.REMOTE CONTROL SENSOR:
Accepts the IR signal of remote controller.

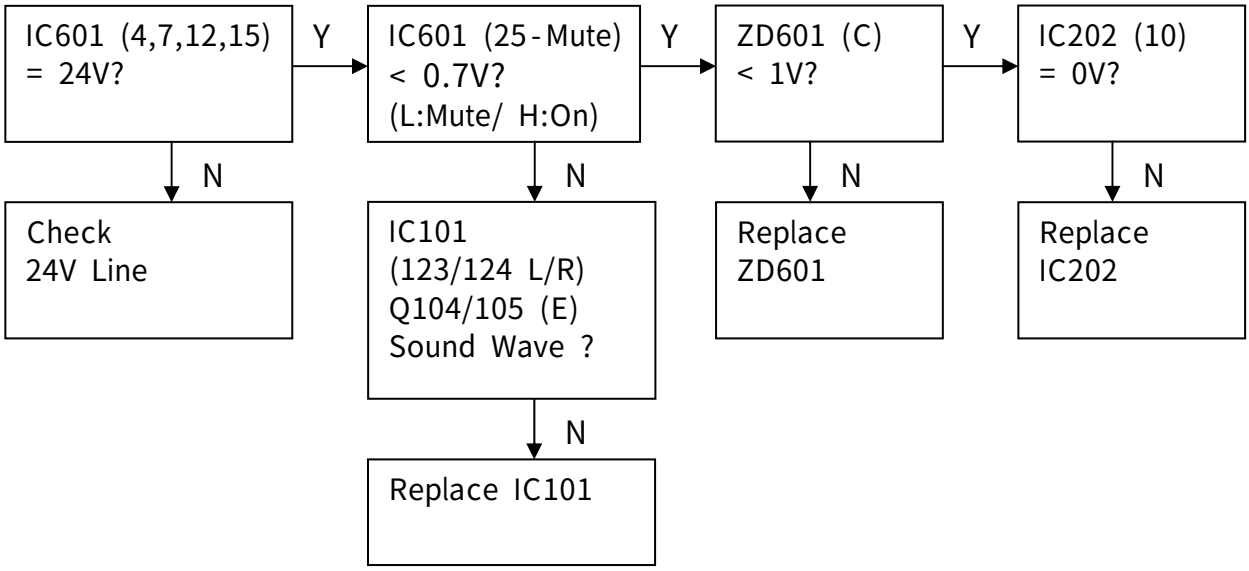
TROUBLE SHOOTING

No Raster

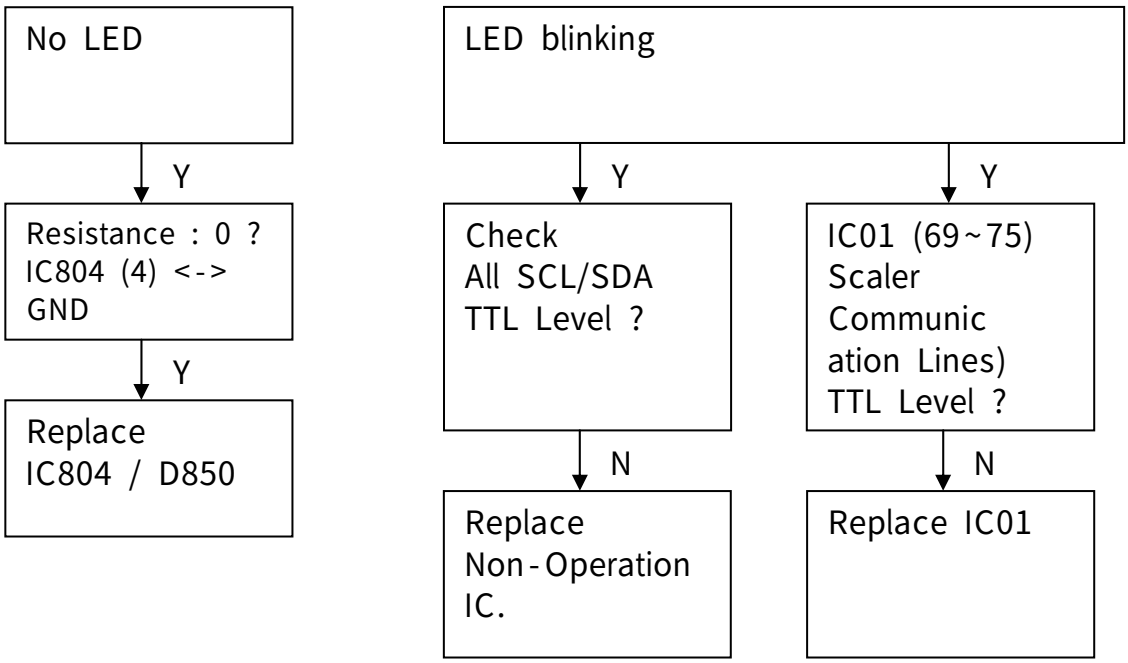


TROUBLE SHOOTING

No Sound & Picture OK



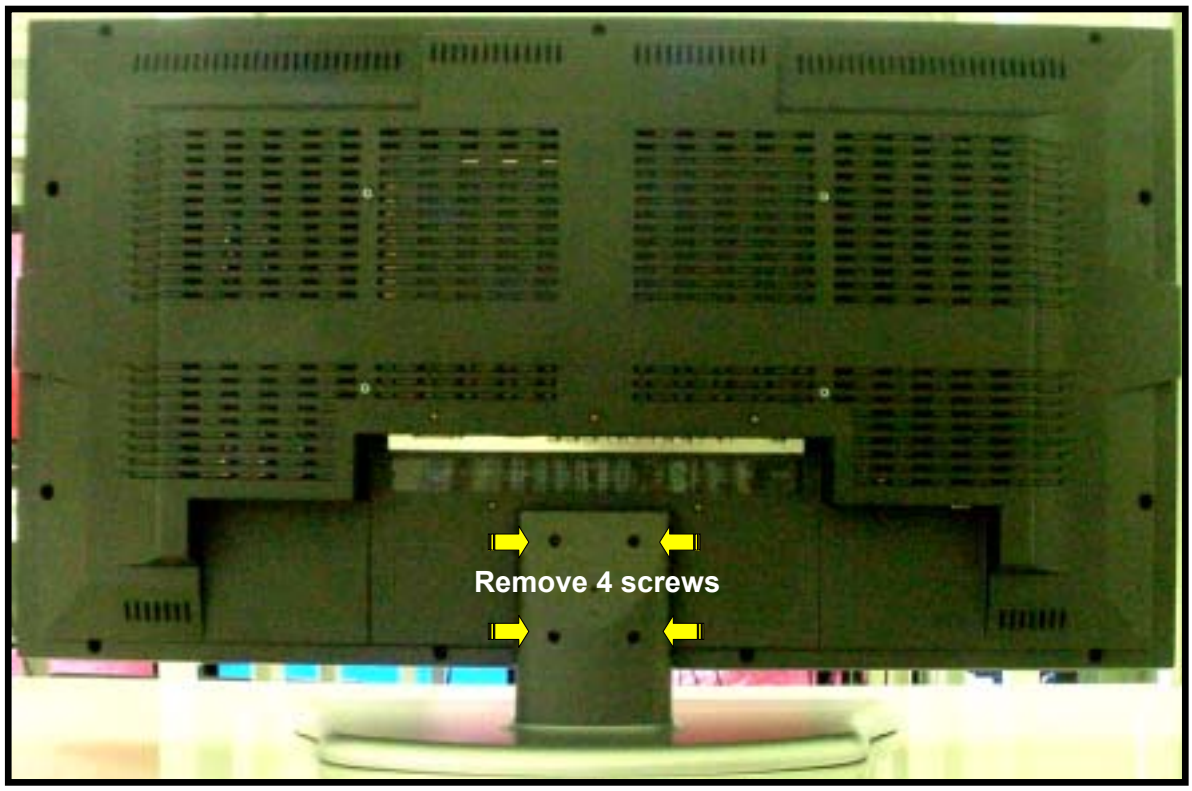
No Operation

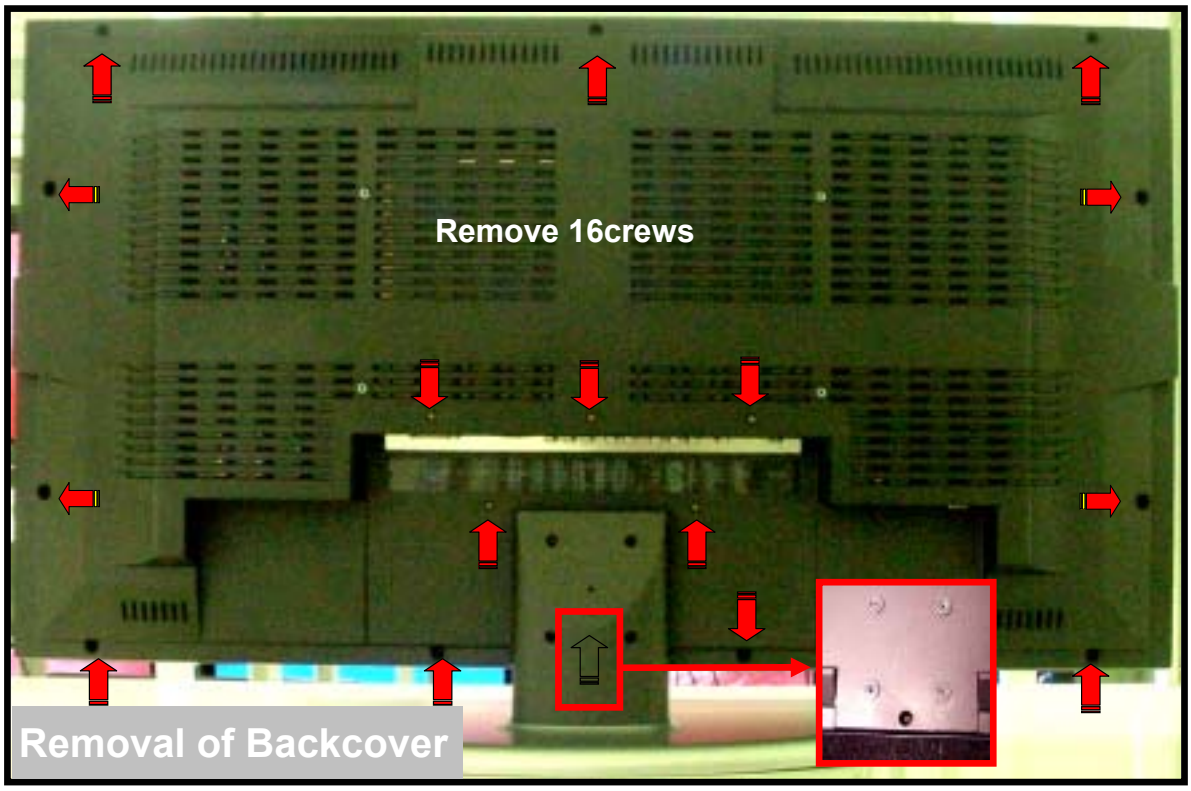


DEASSEMBLY PROCEDURE

1. Disassembly procedure

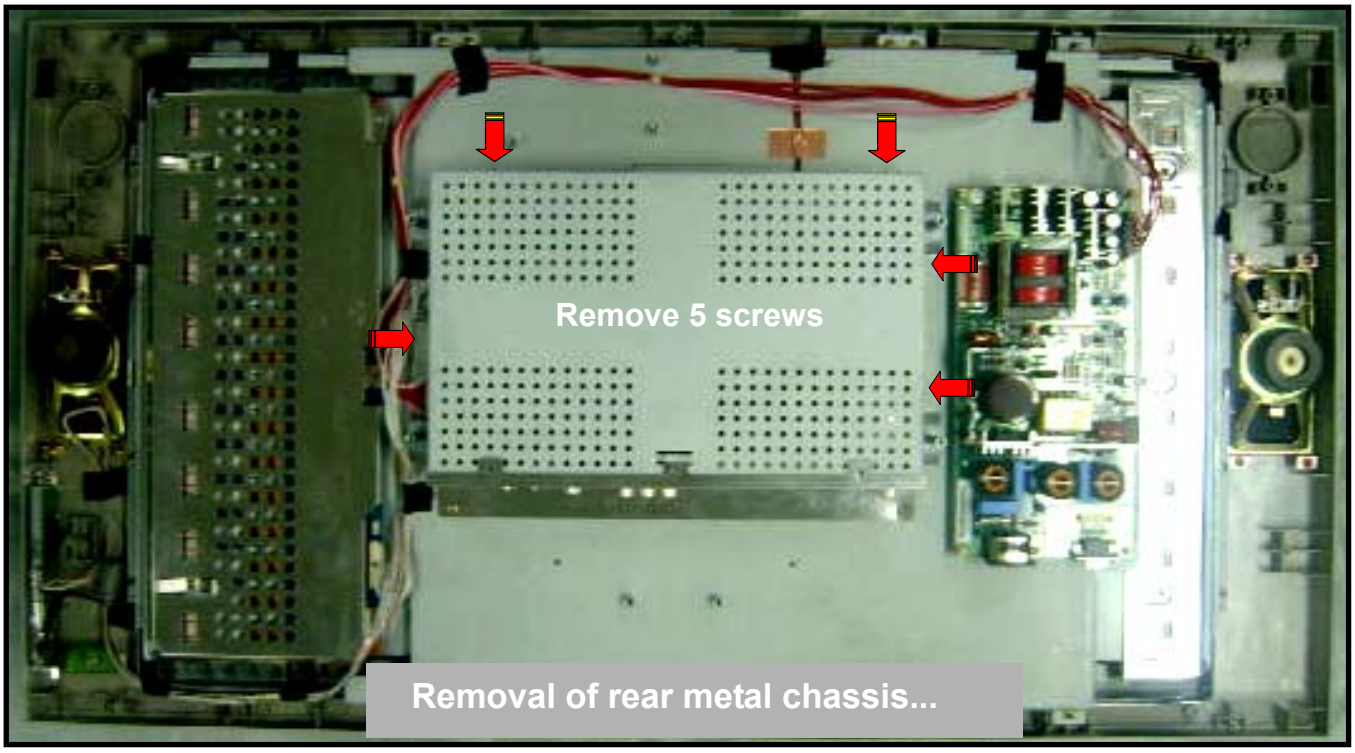
1).Back cover

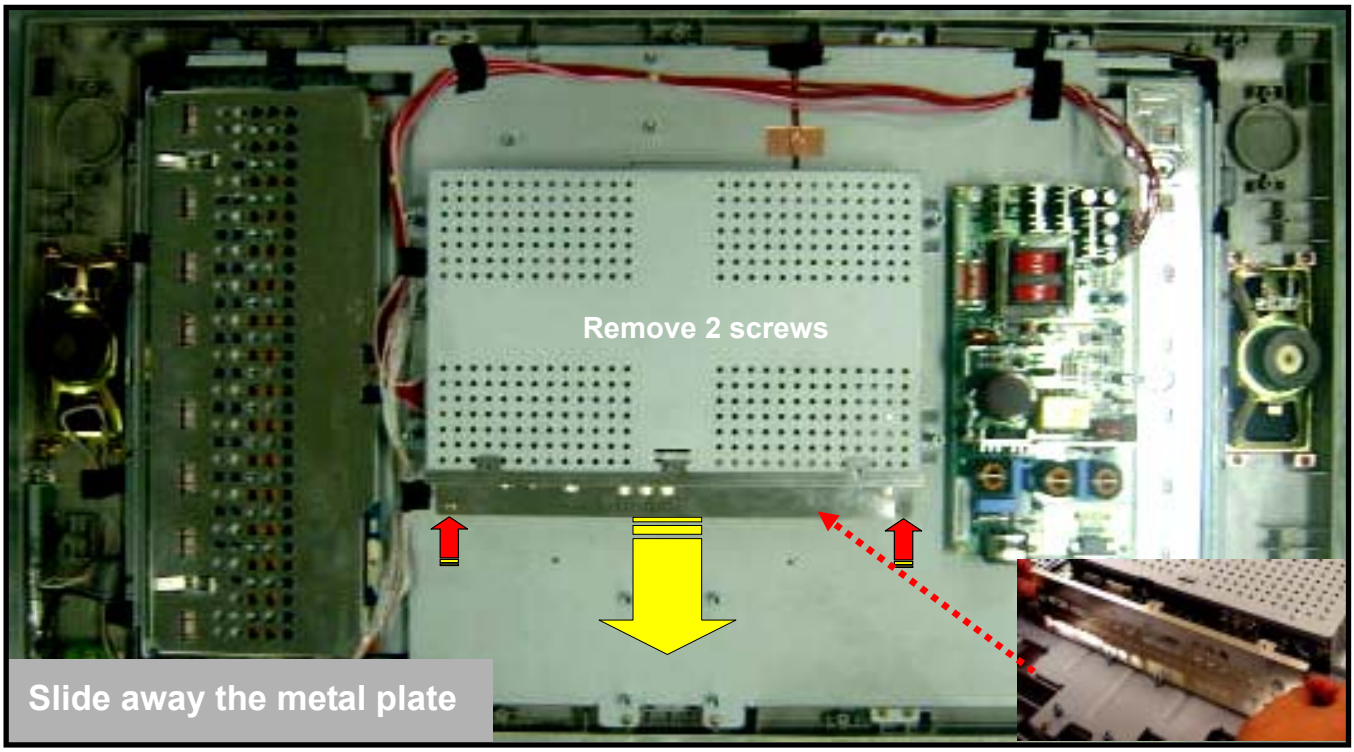




DEASSEMBLY PROCEDURE

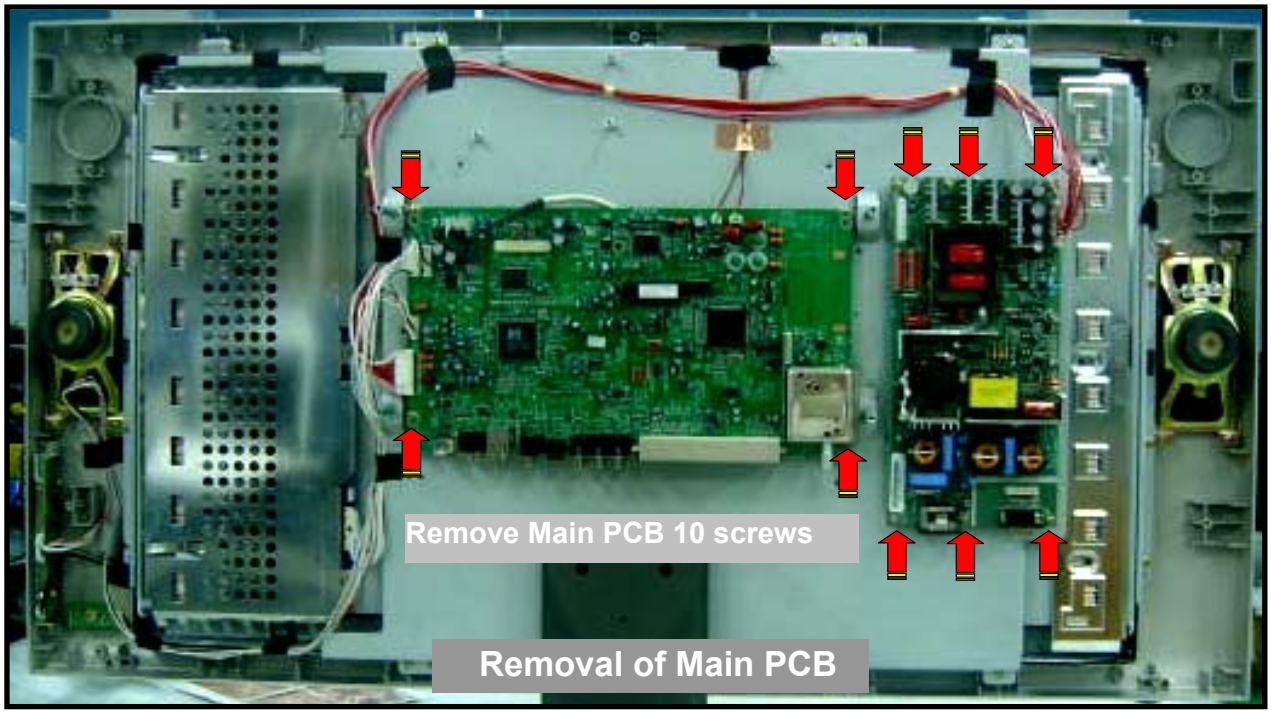
2).Metal plate & Rear chassis

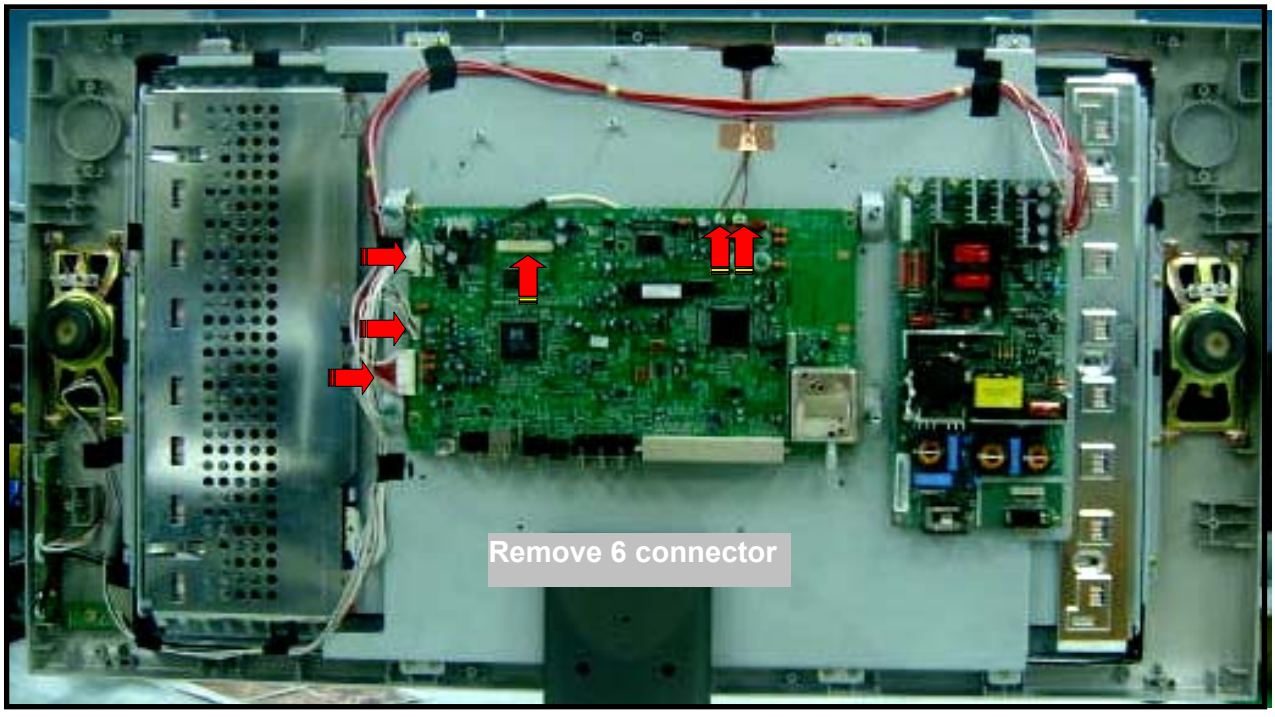




DEASSEMBLY PROCEDURE

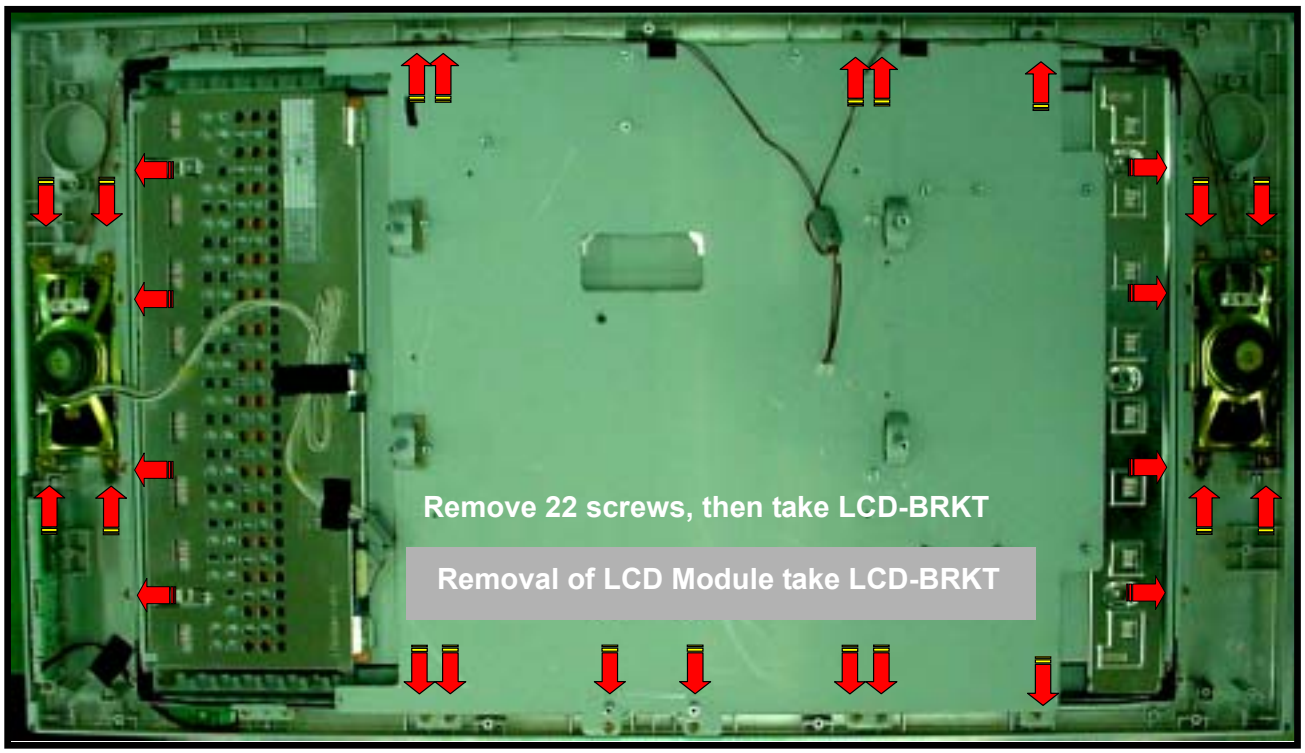
3).Metal plate & Rear chassis





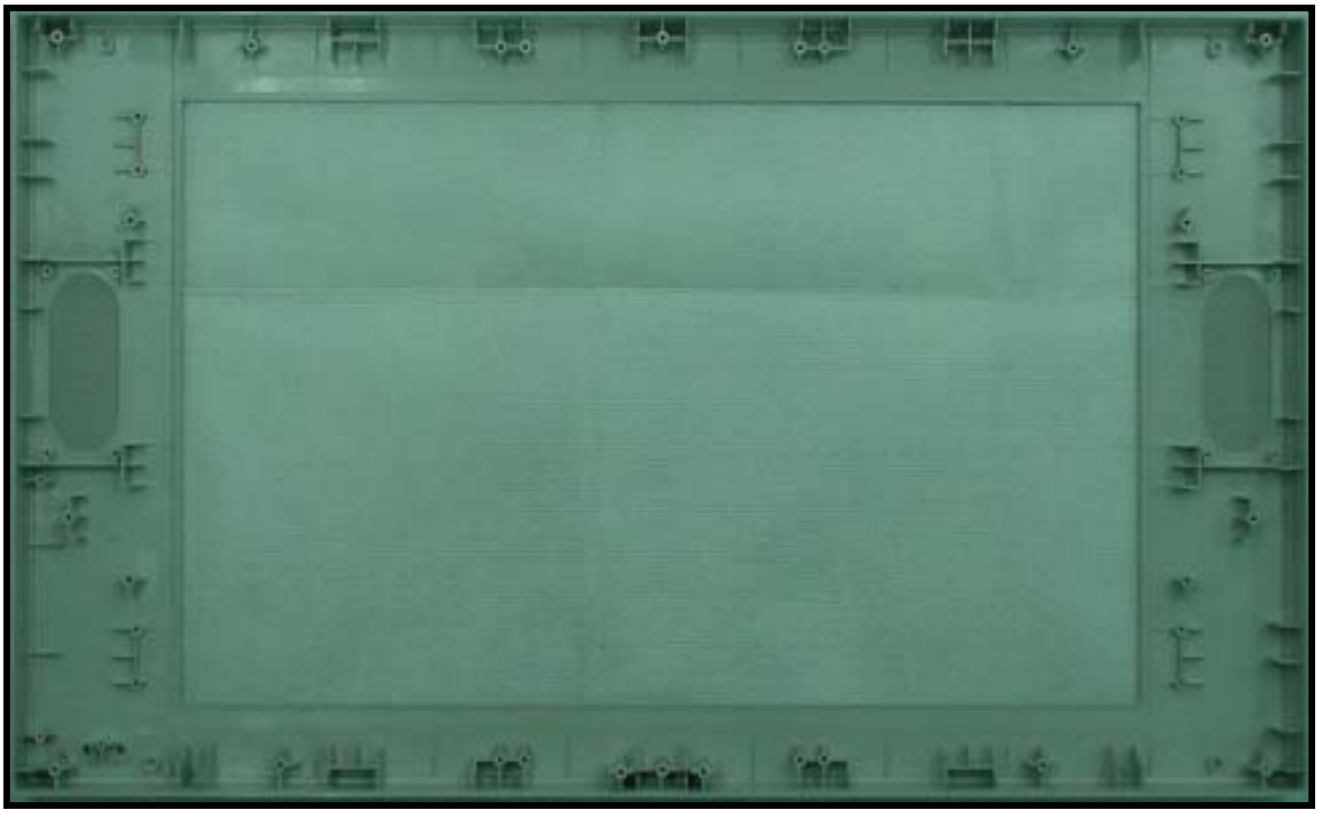
DEASSEMBLY PROCEDURE

4).LCD Panel chassis



DEASSEMBLY PROCEDURE

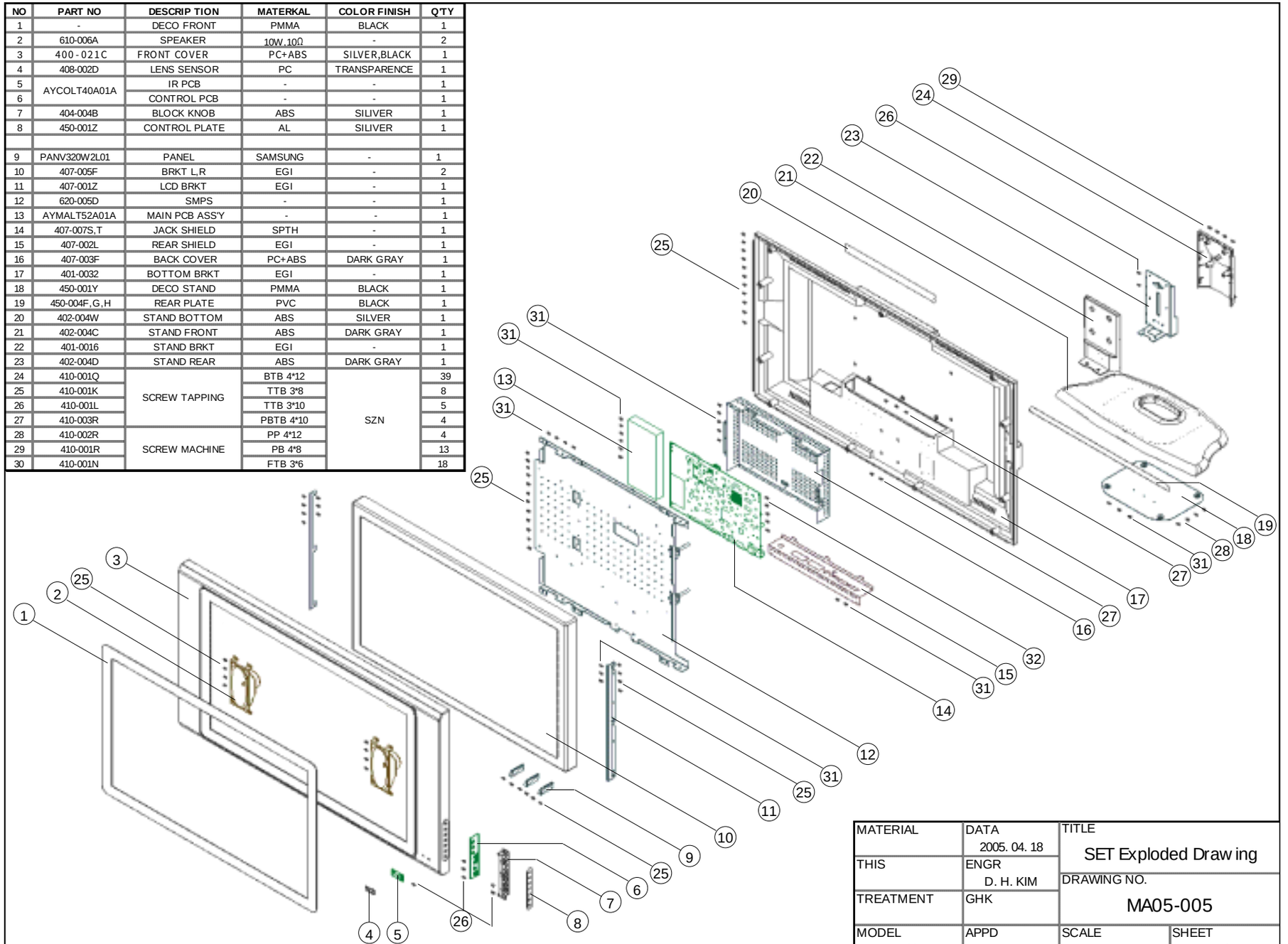
5).LCD Module



Front mask remains after removing LCD Module

MECHANICAL EXPLODED VIEW

NO	PART NO	DESCRIP TION	MATERKAL	COLOR FINISH	Q'TY
1	-	DECO FRONT	PMMA	BLACK	1
2	610-006A	SPEAKER	10W,10Ω	-	2
3	400-021C	FRONT COVER	PC+ABS	SILVER,BLACK	1
4	408-002D	LENS SENSOR	PC	TRANSPARENCE	1
5	AYCOLT40A01A	IR PCB	-	-	1
6		CONTROL PCB	-	-	1
7	404-004B	BLOCK KNOB	ABS	SILIVER	1
8	450-001Z	CONTROL PLATE	AL	SILIVER	1
9	PANV320W2L01	PANEL	SAMSUNG	-	1
10	407-005F	BRKT L,R	EGI	-	2
11	407-001Z	LCD BRKT	EGI	-	1
12	620-005D	SMPS	-	-	1
13	AYMALT52A01A	MAIN PCB ASS'Y	-	-	1
14	407-007S,T	JACK SHIELD	SPTH	-	1
15	407-002L	REAR SHIELD	EGI	-	1
16	407-003F	BACK COVER	PC+ABS	DARK GRAY	1
17	401-0032	BOTTOM BRKT	EGI	-	1
18	450-001Y	DECO STAND	PMMA	BLACK	1
19	450-004F,G,H	REAR PLATE	PVC	BLACK	1
20	402-004W	STAND BOTTOM	ABS	SILVER	1
21	402-004C	STAND FRONT	ABS	DARK GRAY	1
22	401-0016	STAND BRKT	EGI	-	1
23	402-004D	STAND REAR	ABS	DARK GRAY	1
24	410-001Q	SCREW TAPPING	BTB 4*12	SZN	39
25	410-001K		TTB 3*8		8
26	410-001L		TTB 3*10		5
27	410-003R		PBTB 4*10		4
28	410-002R	SCREW MACHINE	PP 4*12		4
29	410-001R		PB 4*8		13
30	410-001N		FTB 3*6		18



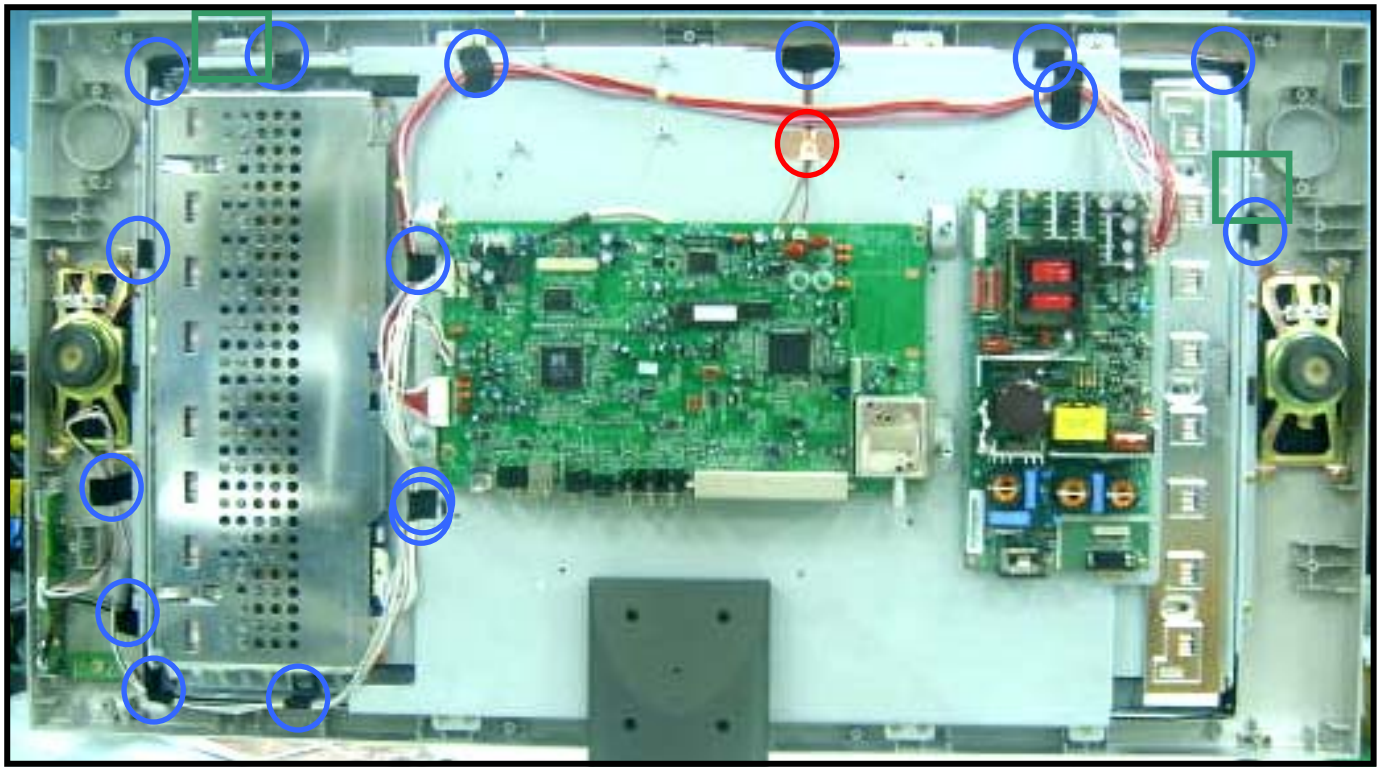
MATERIAL	DATA 2005. 04. 18	TITLE SET Exploded Drawing	
THIS	ENGR D. H. KIM		
TREATMENT	GHK	DRAWING NO. MA05-005	
MODEL LT32H	APPD	SCALE -	SHEET 1 / 1

WIRE DRESSING

1. Wire Dressing

Note: Using acetate
Using Copper (Conducted tape)
Using Ferrite Cpre

	Using Copper Tape
	Using Conducted tape
	Using Ferrite Cpre



ADJUSTMENT INSTRUCTION
WITH DEFAULT FACTORY DATA

1.SVC mode data Adjustment

NOTE!! When the EEPROM has been replaced, the SVC data should be restored as the function of individual system and specification.
When the EEPROM has been replaced White Blance Checking.

[Enter and exit SVC mode]
Note: into the SVC mode, Initialize with default data.

1) Press 5 Seconds MENU buttons on both TV set and Remote Controller at the same time to get into SVC mode.
2) Press the PR ▲▼ button several times to find SVC Data.
3) Input the corresponding SVC data referring to Table below with the VOL ◀▶, key.
4) Press TV/AV button to exit SVC mode

1-1. Factory outgoing setting & Initialize with default data (into the SVC mode)]

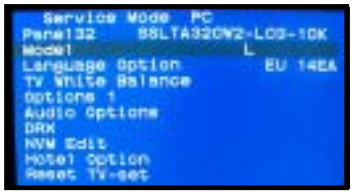
Main menu	Change value	Sub menu	Change value
(Model)	(L)		
Language Option	EU 14EA		
(TV White Balance)	TV White Balance Sub-menu	Settings	ALL
		Start	
		PC	Yes
Option 1	Option 1 Sub-menu	System	BG/I/DK/L
		China/Australia	No
		AV1	RGB
		Text	WEST_EU
		Top	YES
		VPS/PDC	YES
		Data Service	Text
		ATS Delay Time	60
		Game	No
		DVI	Yes
		DTV	No
		QURAN	No
Audio Options	Audio Options Sub-menu	M	+ 42
		BG/I/DK	+ 21
		NICAM	+ 26
		FM Radio	+ 10
		Scart Volume	+ 118
		Surround	0
		Mute if no carrier	Yes
		High Deviation	No
		DUAL	No
		MONO	No
		STEREO	Yes
(DRX)	(Sub-menu)		
(NVM Edit)	(Sub-menu)		
(Hotel Option)	(Sub-menu)		
(Reset TV-set)	(Sub-menu)		

Waring: Do not change the "( )" item…

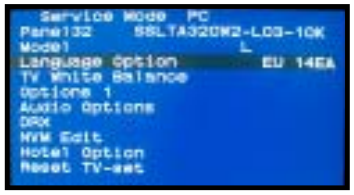
ADJUSTMENT INSTRUCTION WITH DEFAULT FACTORY DATA

2. White Blance Checking

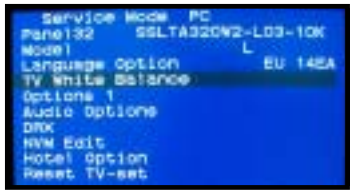
1. Panel : SSLTA320W2-L03-10K



2. MODEL : L



3. Language Option : EU 14EA

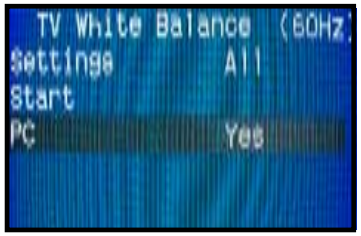


4. PC Pattern Generator
1024 x 768, 60Hz
(Pattern Generator : MSPG-3420)

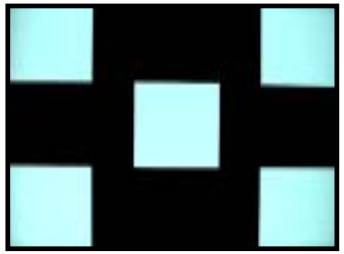
5. Setting : All

6. Setting : All Start Click

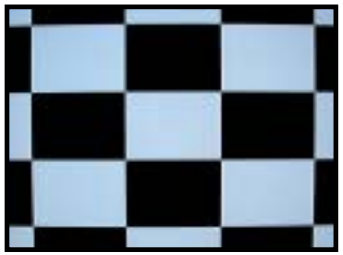
7. PC White Balance Setting中



8. White Balance Setting Verify



9. Pattern Generator : MSPG-3420
PATTEN : Patten No. : 33
MODE : 1024*768(13)



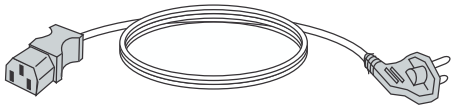
10. Equipment : MSPG-925FS
MODE : 1024*768

INSPECTION INSTRUCTION

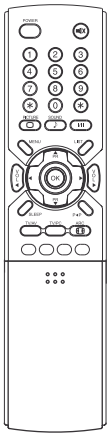
1. Supplied Accessories

■ **Make Sure the following accessories are provided with Product.**

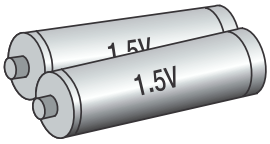
1. AC Cord



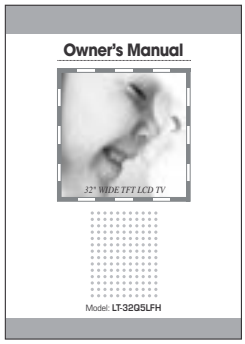
2. Remote controller



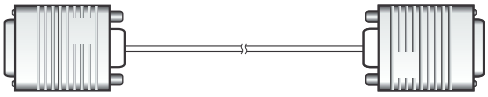
3. Batteries (type AAA)



4. Instruction manual

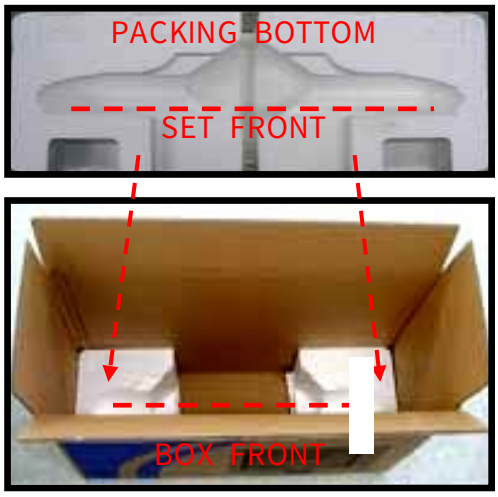


5. VGA cable



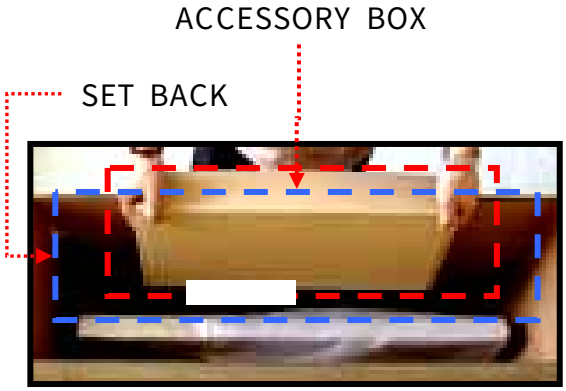
6. PC Audio IN cable

2. Packing condition



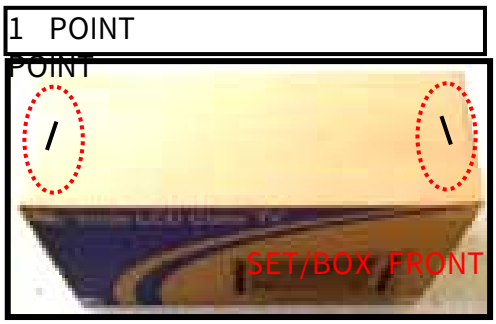
<picture 1> PACKING insert in BOX

<picture2> SET insert in BOX

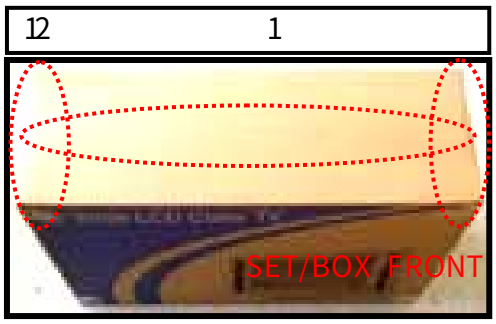


<picture3> Accessory Box insert

<picture4> TOP PACKING insert in BOX

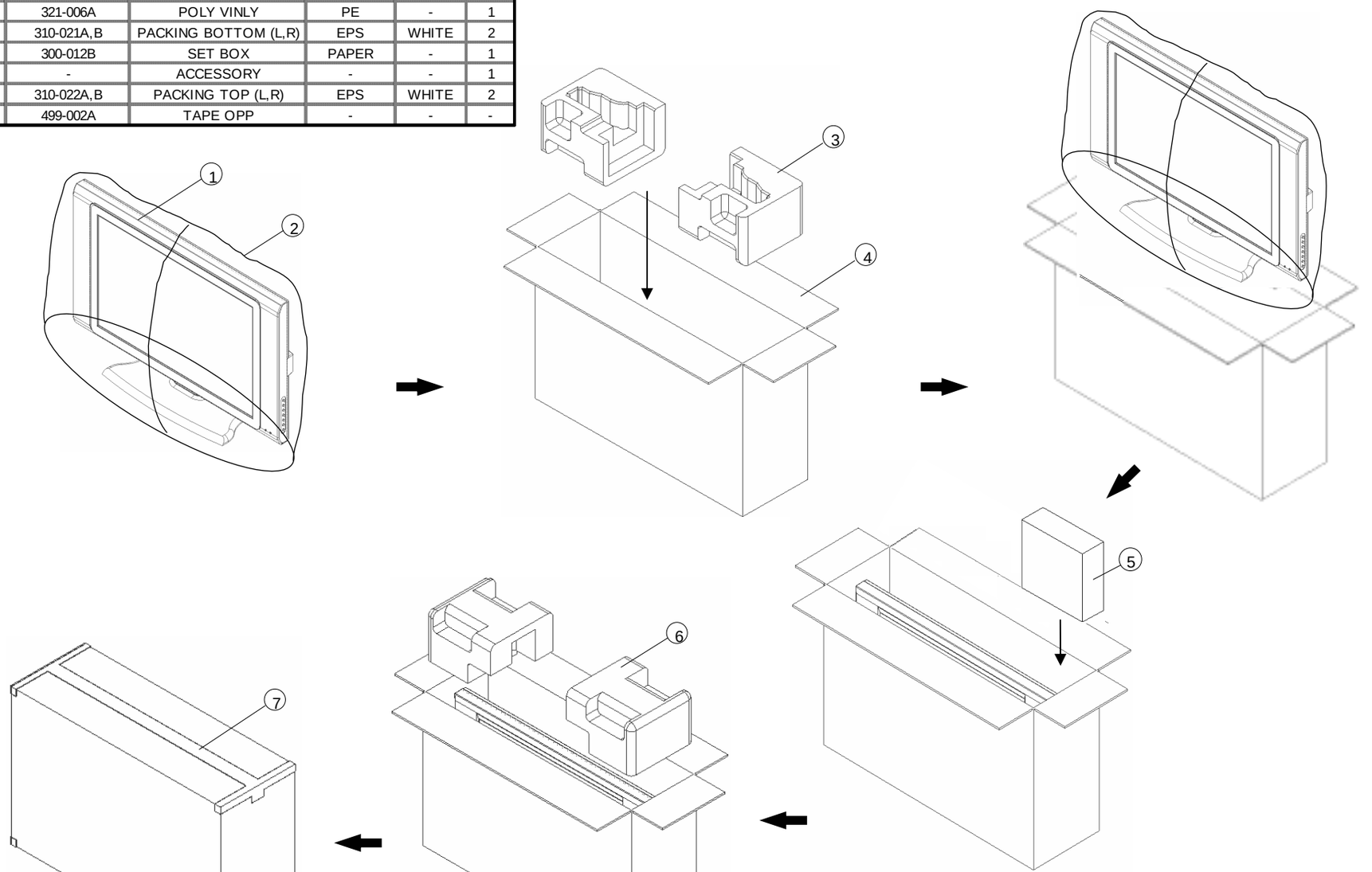


<Picture 1>Staping



<Picture 2>Taping TOP of SET box with OPP TAPE

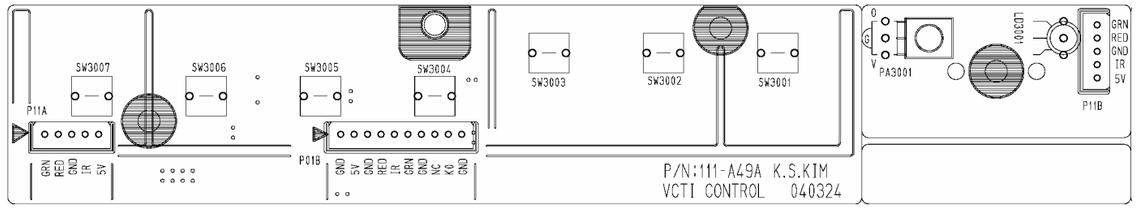
NO	PART NO	DESCRIP TION	MATERKAL	COLOR	Q'TY
1	-	LCD COLOR TV	-	-	1
2	321-006A	POLY VINLY	PE	-	1
3	310-021A,B	PACKING BOTTOM (L,R)	EPS	WHITE	2
4	300-012B	SET BOX	PAPER	-	1
5	-	ACCESSORY	-	-	1
6	310-022A,B	PACKING TOP (L,R)	EPS	WHITE	2
7	499-002A	TAPE OPP	-	-	-

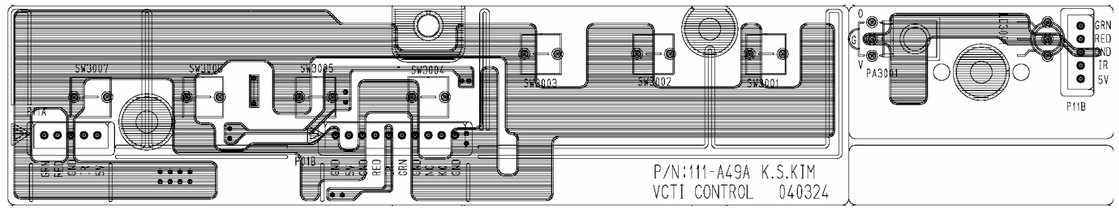


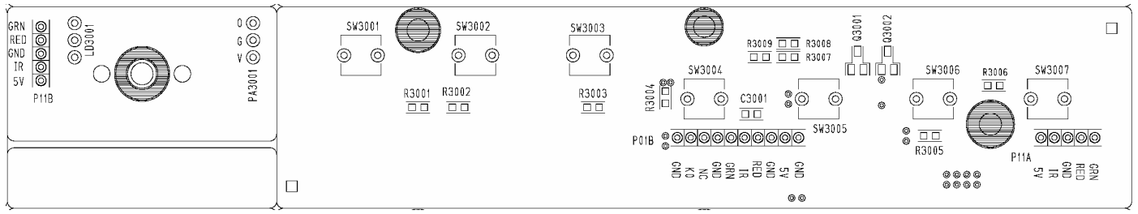
MATERIAL	DATA 2005. 10. 26	TITLE SET Packing Exploded Drawg	
THIS	ENGR D. H. KIM	DRAWING NO. MA05-006	
TREATMENT	GHK		
MODEL LT32H	APPD	SCALE -	SHEET 1 / 1

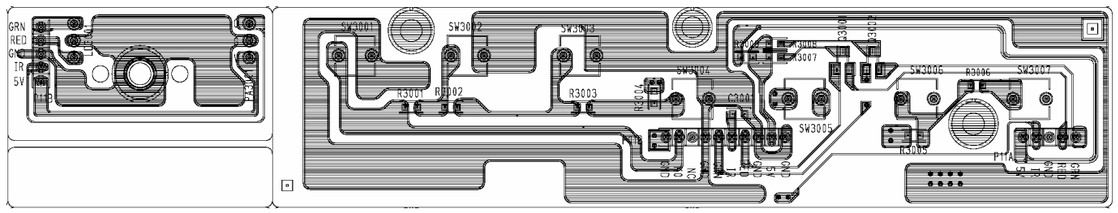
PCB LAYOUT

1. CONTROL PCB

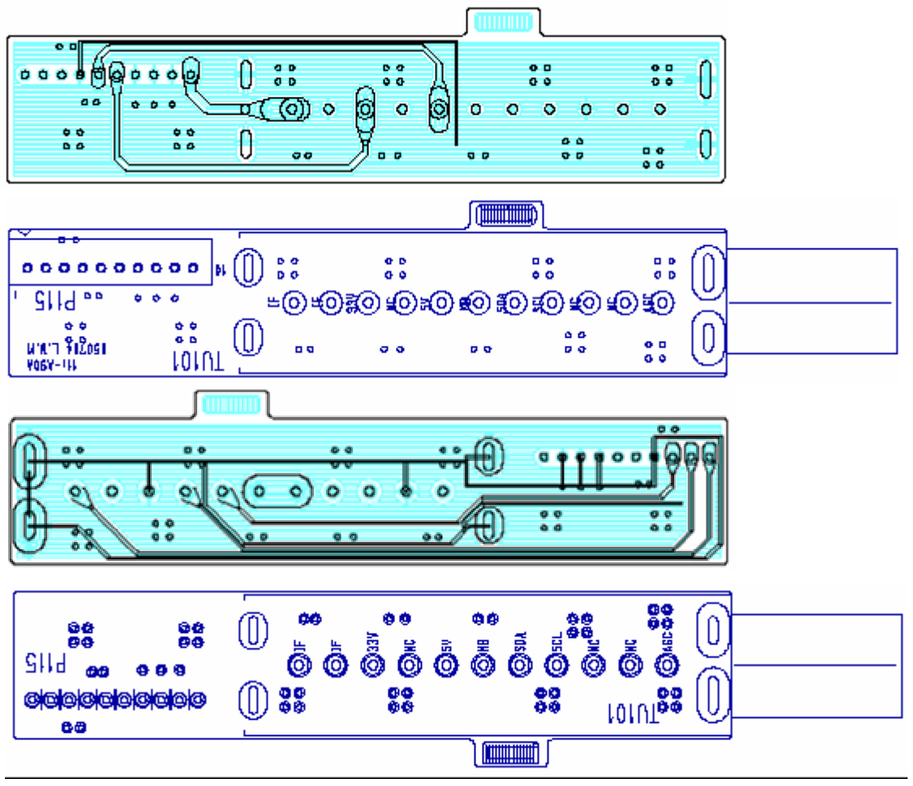




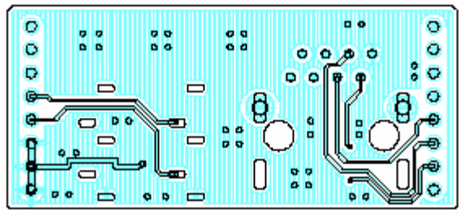


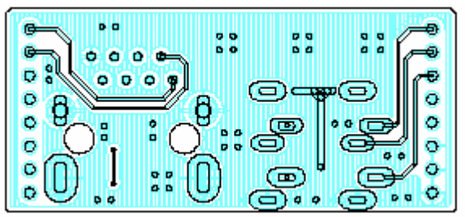


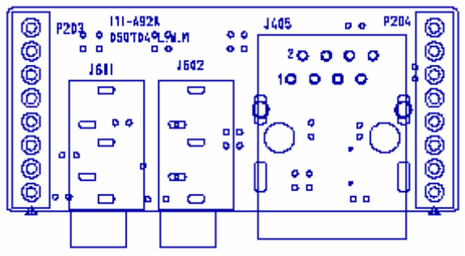
2. Tuner PCB

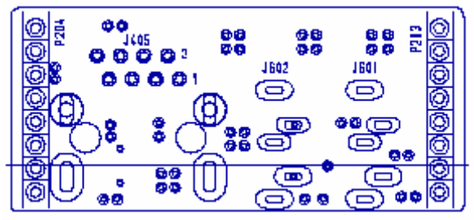


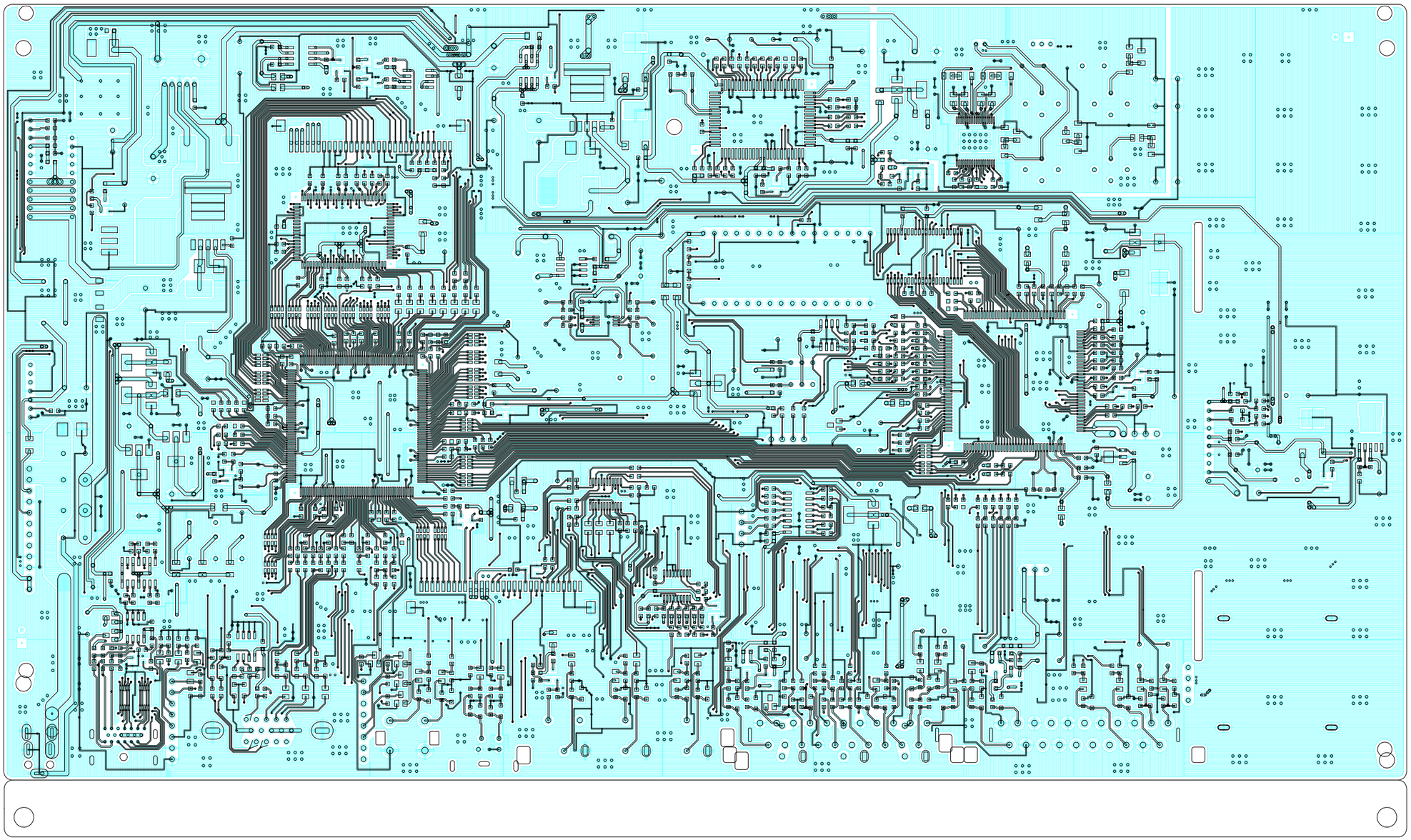
3. SUB PCB

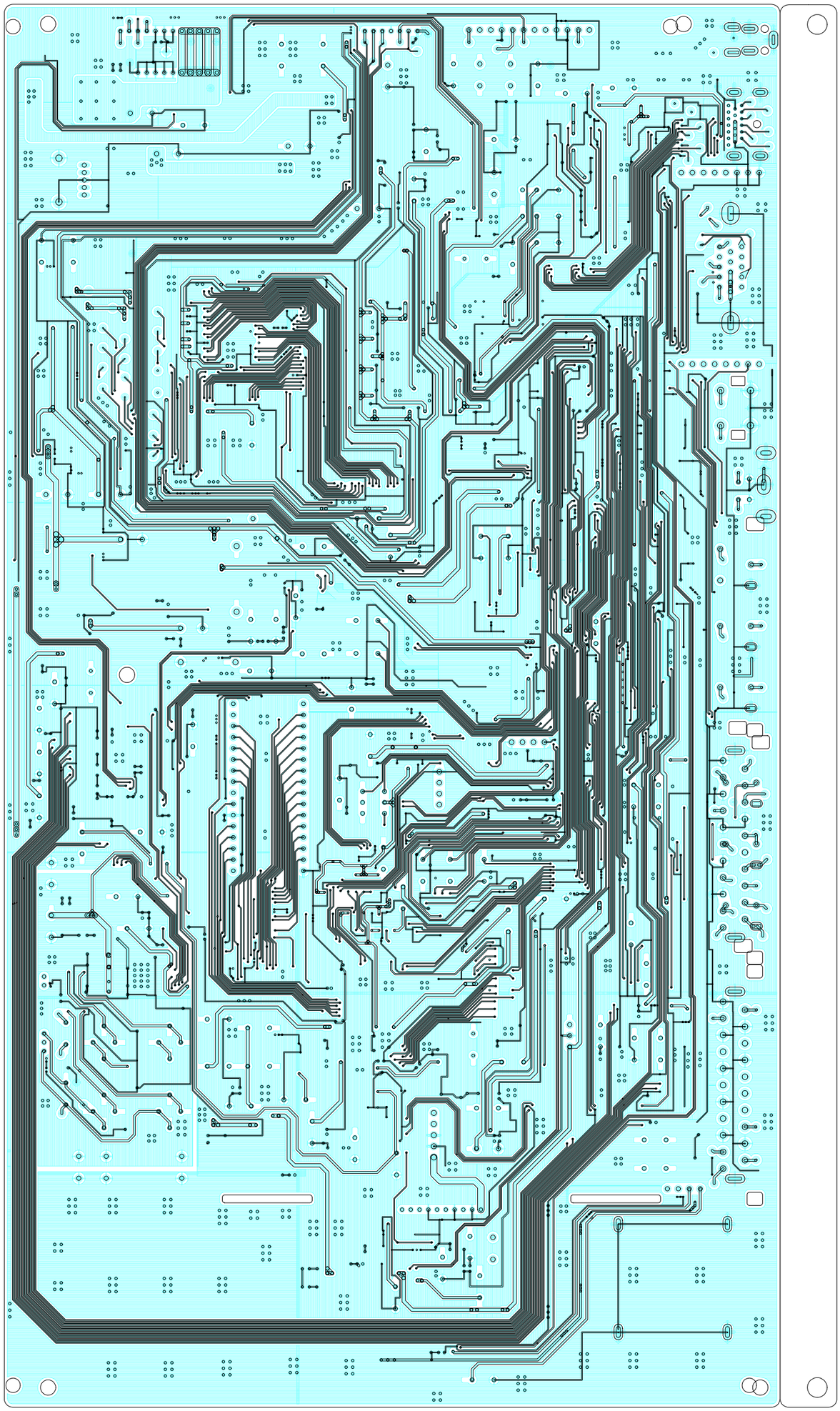




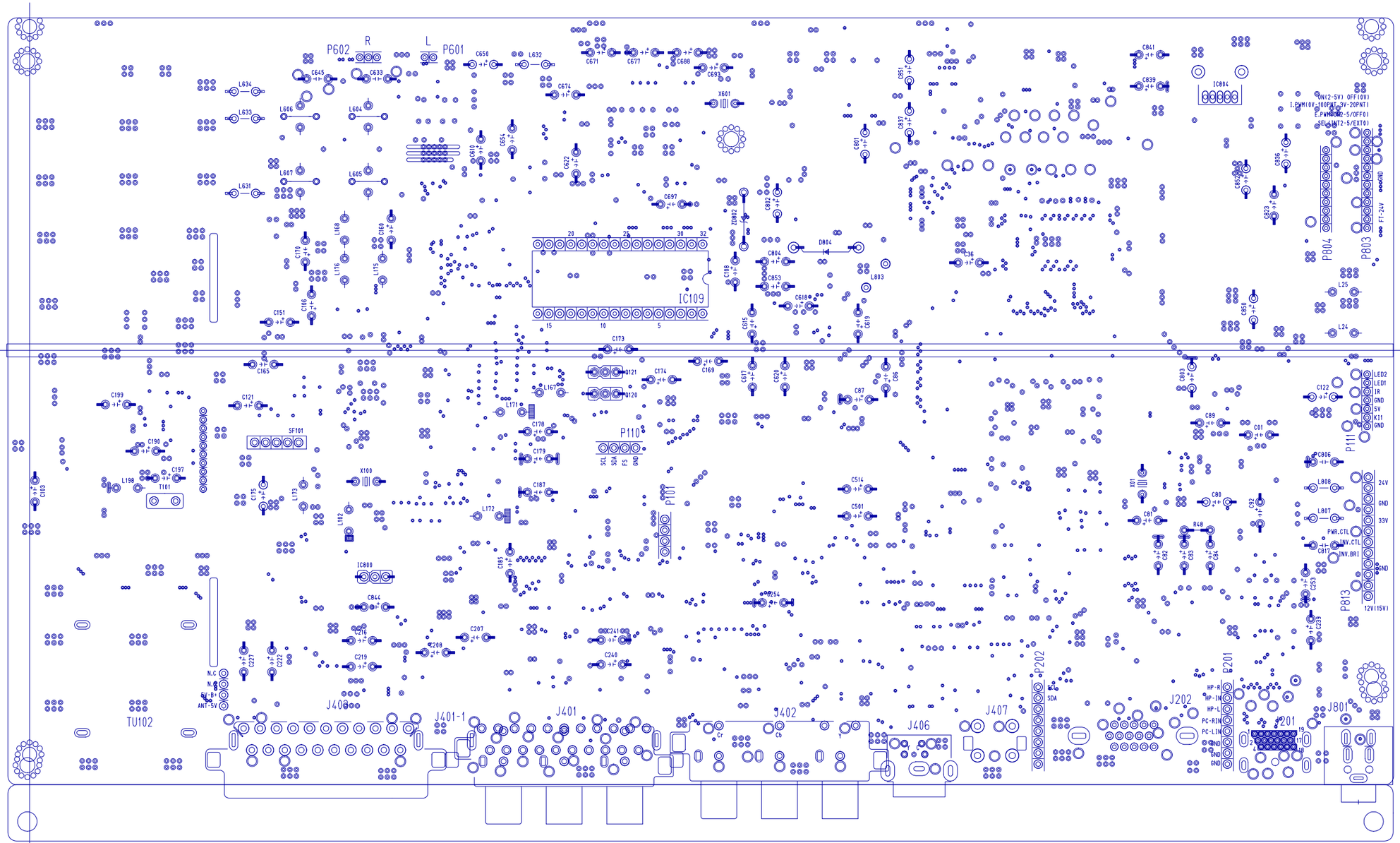




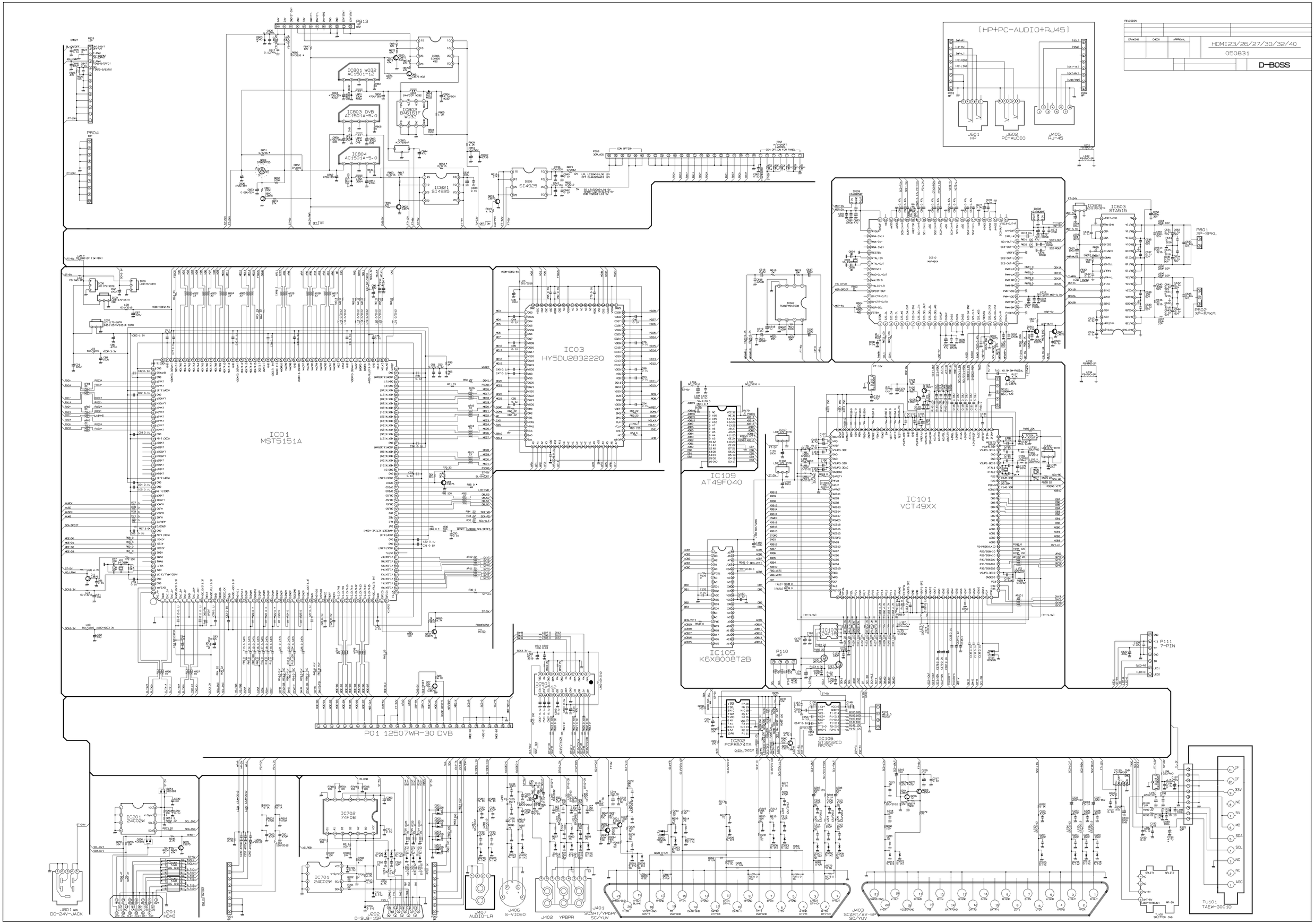




111-A84B
HD23/26/27/30/32
050926



P602
R
L
P601
IC109
IC804
P804
P803
P110
P101
P111
P813
P202
P201
J202
J201
J801
J406
J407
J402
J401
J401-1
J403
TU102
SF101
T101
X100
X601
X01
IC800



REVISION
DRAWING
CHECK
APPROVAL
HDMI23/26/27/30/32/40
050831
D-BOSS
[HP+PC-AUDIO+RJ45]
J601 HP
J602 PC-AUDIO
J405 RJ-45
IC801 W032 AC1501-12
IC803 DVB AC1501A-5.0
IC804 AC1501A-5.0
IC802 BA6161F W032
IC821 SI4925
IC805 SI4925
IC01 MST5151A
IC03 HY5DU283222Q
IC109 AT49F040
IC101 VCT49XX
IC105 K6X8008T2B
IC103 24C16
IC606 IC603 STA515
P601 2P-SPKL
P602 3P-SPKR
P110 4P
P111 7-PIN
IC501 PI3V512
IC202 PCF8574TS
IC106 SI3232CD RS232
P01 12507WR-30 DVB
IC201 24C02W
IC702 74F08
IC701 24C02W
J801 DC-24V-JACK
J201 HDMI
J202 D-SUB-15P
J407 AUDIO-LR
J406 S-VIDEO
J402 YPBPR
J401 SCART/YPbPr SC/YUV
J403 SCART/AV-6P SC/YUV
TU101 TAEW-G001D

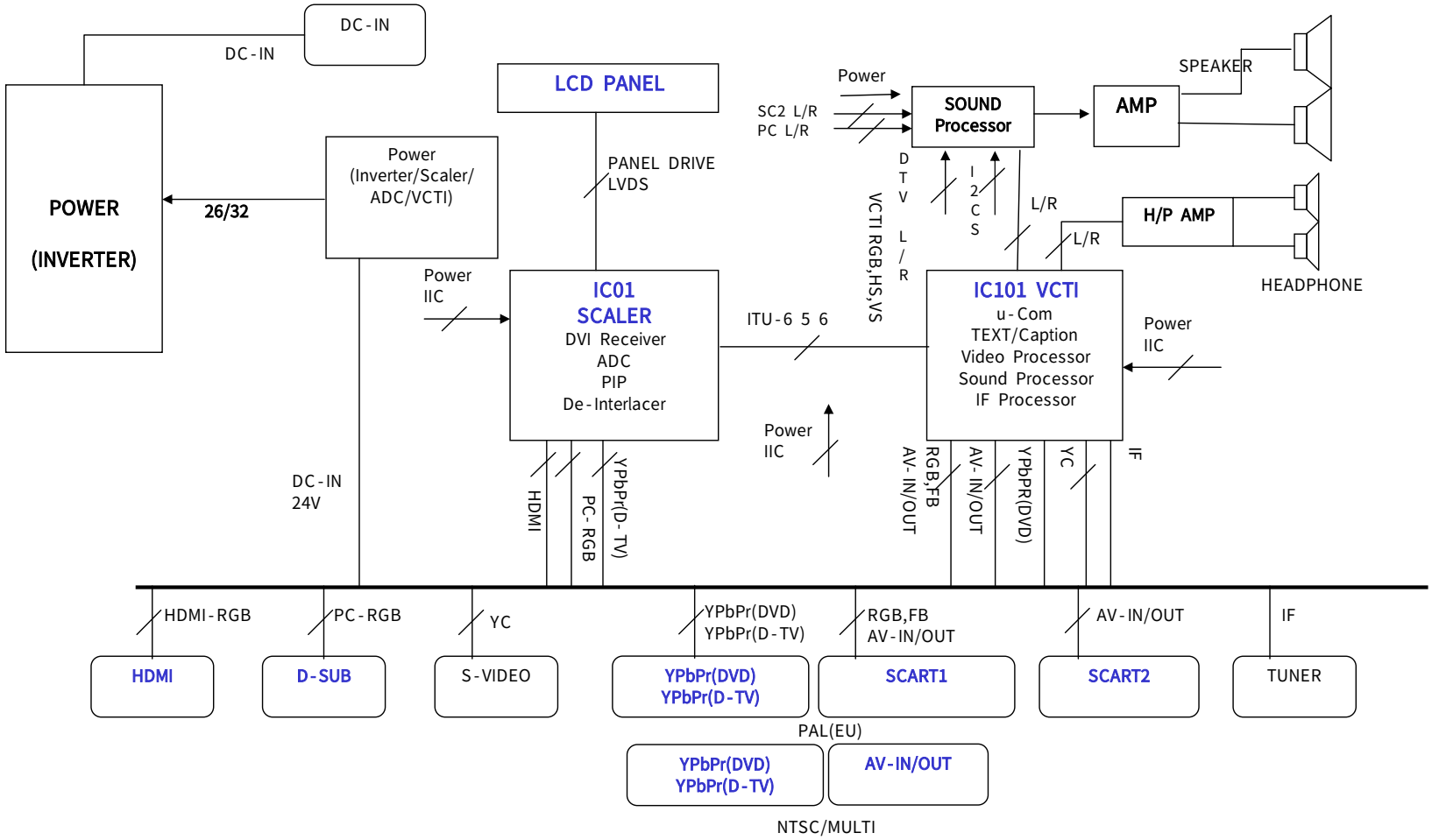
REPLACEMENT PART LIST

NO_LEVEL	CD_CHILD	DC_ITEM_SPEC	NM_ITEM	QT_REAL	DC_ITEM_UNIT
.1	300-003R	40 ACCESSORY BOX	BOX, ACCESSORY	1	EA
.2	300-012B	32" BOX NO BRAND	BOX, CARTON	1	EA
.3	310-021A	32"H-MODEL	PACKING, BOTTOM "L"	1	EA
.4	310-021B	32"H-MODEL	PACKING, BOTTOM "R"	1	EA
.5	310-022A	32"H-MODEL	PACKING, TOP "L"	1	EA
.6	310-022B	32"H-MODEL	PACKING, TOP "R"	1	EA
.7	320-001A	ACCESSORY PACKING	BAG, VINYL	1	EA
.8	321-006A	30 SET PACKING	BAG, PACKING	1	EA
.9	404-004J	H, C/KEY,SILVER	BLOCK KNOB	1	EA
.10	407-001Z	32",LCD BRKT,SS	SHIELD, FRONT	1	EA
.11	407-002L	32" SHIELD PCB,SS	SHIELD, REAR	1	EA
.12	407-005F	32"SS FIX BRKT L/R	SHIELD,SUPPORT(SS)	2	EA
.13	407-007W	VCTI-32"(HD/DVB-T)	SHIELD, JACK (YUV)	1	EA
.14	410-001K	TTB 3*8	SCREW	6	EA
.15	410-001L	TTB 3*10	SCREW	5	EA
.16	410-001N	FTB 3*6	SCREW	18	EA
.17	410-001Q	BTB 4*12	SCREW	49	EA
.18	410-001R	PB 4*8	SCREW	10	EA
.19	410-002R	PP 4*12	SCREW	4	EA
.20	490-001M	7ITS FK10-2-104-13	FORM, SHIELD	1	EA
.21	490-001R	7ITS FK 6-4-35-13	FORM, SHIELD	2	EA
.22	490-011L	MSF15-20-30-00K	FORM, SHIELD	1	EA
.23	490-011W	MK-7-03-325-11	FORM, SHIELD	1	EA
.24	490-011X	MK-15-15-310-00K	FORM, SHIELD	2	EA
.25	491-001A	W40mm,L20mm, COPPER	TAPE, CONDUCTIVE	2	EA
.26	492-001A	CLIP, ZCAT1325-0530	FERRITE CORE	2	EA
.27	492-001B	CLIP, ZCHT1730-0730	FERRITE CORE	1	EA
.28	499-002A	W:70mm	TAPE, OPP	4000	mm
.29	499-004A	W:20mm, L:30m	TAPE, ACETATE	400	mm
.30	500-037V	DIBOSS,32HTFH,EN/TUR	OWNERS MANUAL	1	EA
.31	501-001B	ENGLISH	LABEL, WARNING	1	EA
.32	501-0030	SILVER/BLACK	LABEL,SERIAL	1	EA
.33	501-018G	DIBOSS(N),58mm	STICKER, LOGO	1	EA
.34	501-113E	32" DIBOSS(N)	LABEL, ID	1	EA
.35	502-001O	ENGLISH	LABEL, BOX ID	1	EA
.36	509-009W	DIBOSS(N),COMMON	LABEL, BRAND	2	EA
.37	509-012S	HD+HDMI LABEL	LABEL, SPEC	2	EA
.38	510-320A	NO BRAND,(PR),symbol	REMOCON (WEE),L-GRAY	1	EA
.39	520-001A	1.5V, AAA SIZE	BATTERY	2	EA
.40	610-006A	10W,8Ohm(CT156B03K)	SPEAKER	2	EA
.41	620-005D	32",SMPS,HNE,150W	AD/DC ADAPTER	1	EA
.42	621-001B	VDE KKP-4819R (EU)	POWER CORD	1	EA
.43	626-002C	IVORY,1.8M,15P,SHORT	CABLE, PC RGB	1	EA
.44	627-001A	1.8M, BK	CABLE, PC-SOUND	1	EA
.45	AYBCLT32A01L	32H, HDMI YUV ENG	BACK COVER ASSY	1	EA
.46	AYCALT43A02A	32H, HDMI,PR+,- NO/B	Front body,32inch	1	EA
.47	AYCOLT40A01A	VCTI N/F CONTROL	CONTROL PCB ASSY	1	EA
.48	AYMALT52A01B	HD READ_MULT_32(5V)	MAIN PCB ASSY	1	EA
.49	AYSTLT32A01F	30", H-MODEL,REV.01	STAND ASSY	1	EA
.50	CON02P200AOU	30.1 SPK,2P 700MMH/-	LEAD ASSY	1	EA
.51	CON03P200AOY	301 SPK,3P 900MM H/-	LEAD ASSY	1	EA
.52	CON05P200ABH	301 LED,5P 200MM H/H	LEAD ASSY	1	EA
.53	CON07P200AD3	VCTI-232627,7P-10P	LEAD ASSY, 1000CTRL	1	EA
.54	CON12P200ACL	32,W2,IVT,12P,300MM	LEAD ASSY	1	EA
.55	CON12P250ACX	32" SMPS 12P 850MM	LEAD ASSY	1	EA
.56	CON30P125AHJ	2632 +CORE SS,LVDS	LEAD ASSY-HDMI32 SS	1	EA
.57	PANLTA320W03	32",SS,LTA320W2-L14	PANEL, LCD COLOR	1	EA

BLOCK DIAGRAM

1. Block Diagram

32 Block Diagram



CIRCUIT DESCRIPTIONS

General Description for 32.0” color TFT LCD TV.

The TFT LCD TV described in the followings is based on a Multi TV system, digital Control display, 32.0" diagonal. The TFT LCD TV is intended to be a finished product, Basically a display device mounted inside an enclosure which will provide the safety Requirements. With the exception of LCD Panel, the display device shall be composed entirely of solid state components.
These components shall have a history of reliable service in identity applications and shall be applied in the circuits.

1. SCALER SECTION.
2. VCT 49xxi SECTION.
3. Video A/D Converter

CIRCUIT DESCRIPTIONS

1.SCALER SECTION.

Device : MST5151A

Features: LCD TV controller with PC & multimedia display functions
Input supports up to UXGA & 1080P
Supports up to SXGA panels
Integrated two-port triple-ADC/PLL
Integrated DVI/HDCP/HDMI compliant receiver
YUV422 digital video input ports
Dual high-quality scaling engines
Dual 3-D video de-interlacers
Full function PIP/POP
MStarACE picture/color processing engine
Embedded On-screen display controller (OSD) engine
Digital audio I/O & sync processor
Built-in dual-link LVDS transmitter
5 Volt tolerant inputs
Low EMI and power saving features
Supports PWM & GPO controls
208-pin PQFP package

- Analog RGB/YPbPr Input Ports

Dual analog ports support up to 165Mhz
Supports PC RGB input up to UXGA@60Hz
Supports HDTV RGB/YPbPr/YCbCr up to 1080P
On-chip high-performance PLLs
Supports Composite Sync and SOG (Sync-on-Green) separator
Automatic color calibration

- DVI/HDCP/HDMI Compliant Input Port

Operates up to 165 MHz (up to UXGA @60Hz)
Single link on-chip DVI 1.0 compliant receiver
High-bandwidth Digital Content Protection
(HDCP) 1.1 compliant receiver
High Definition Multimedia Interface (HDMI)
1.0 compliant receiver with I2S and S/PDIF digital audio outputs
Long-cable tolerant robust receiving

- Video Input Port

Two 4:2:2 ITU656 8-bit digital video input ports
One 4:2:2 ITU601 16-bit digital video input port
Supports 16-bit YUV 4:2:2 interlaced/ progressive video input up to 1080i/720P

- Auto-Configuration/Auto-Detection

Auto input signal format (SOG, Composite,Separated HSYNC, VSYNC, and DE),
and input mode (all PC & TV modes) detection
Auto-tuning function including phasing, positioning, offset, gain, and jitter detection
Sync Detection for H/V Sync

- Dual High-Performance Scaling Engines

Fully programmable shrink/zoom capabilities
Nonlinear video scaling supports various modes including Panorama

- Video Processing & Conversion

Dual 3-D motion adaptive video de-interlacers with upgraded edge-oriented adaptive
algorithm for smooth low-angle edges
Automatic 3:2 pull-down & 2:2 pull-down detection and recovery
PIP/POP with programmable size and location, supports multi-video applications
Video-over-graphic overlay
MStar 2nd Generation Advanced Color Engine

- On-Screen OSD Controller

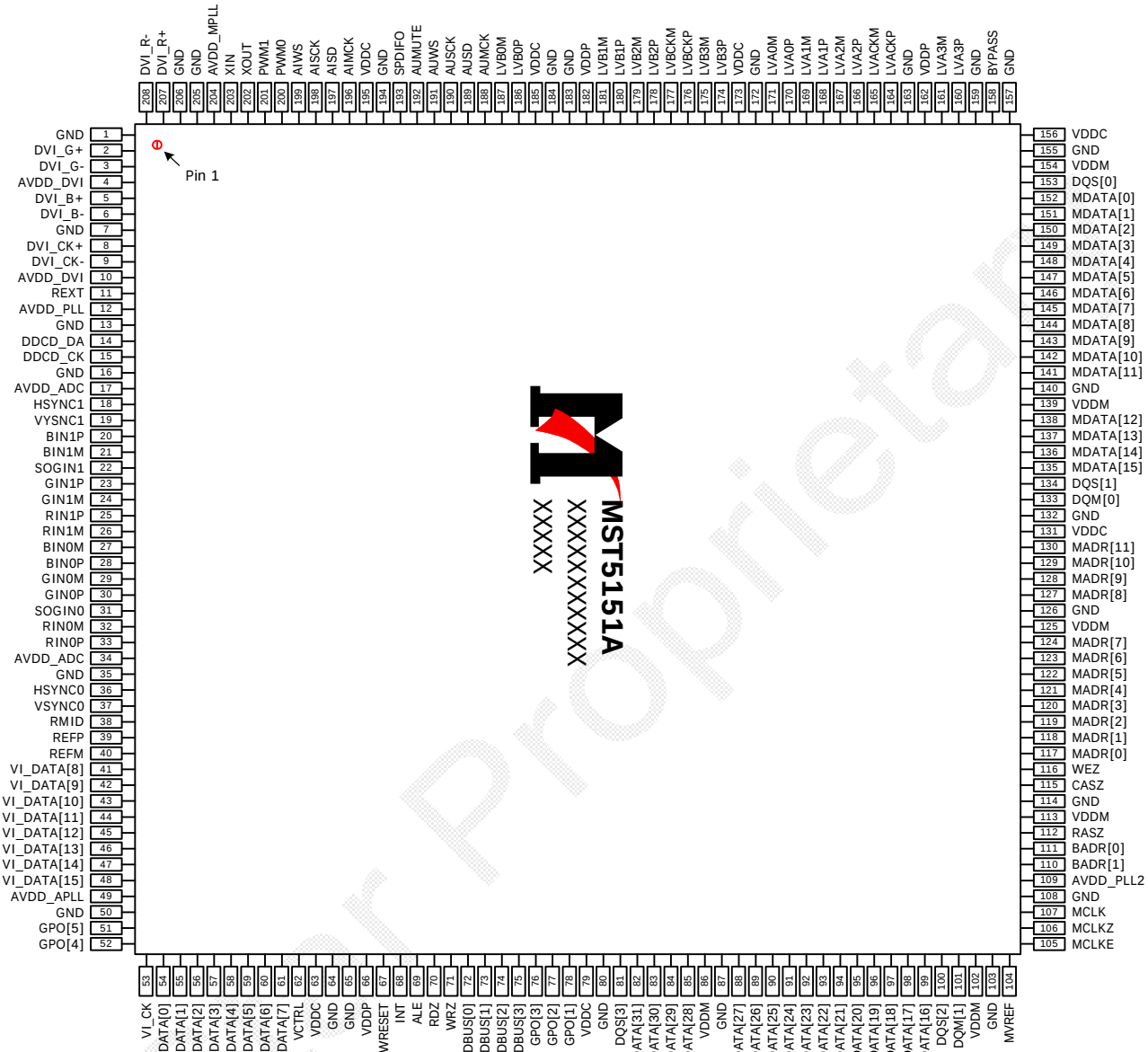
1) Description

The MST5151A is a high performance and fully integrated graphics processing IC solution for multi-function LCD monitor/TV with resolutions up to SXGA. It is configured with an integrated triple-ADC/PLL, an integrated DVI/HDCP/HDMI receiver, two video de-interlacers, two high quality scaling engines, an on-screen display controller, and a built-in output clock generator. By use of external frame buffer, PIP/POP is provided for multimedia applications. It supports de-interlaced full-screen video, video-on-graphic overlay, split screen, frame rate conversion, and aspect ratio conversion for various video sources. To further reduce system costs, the MST5151A also integrates intelligent power management control capability for green-mode requirements and spread-spectrum support for EMI management.

.

CIRCUIT DESCRIPTIONS

PIN DIAGRAM (MST5151A)



MSTar Proprietary

CIRCUIT DESCRIPTIONS

PIN DESCRIPTION

MCU Interface

Pin Name	Pin Type	Function	Pin
HWRESET	Schmitt Trigger Input w/ 5V-tolerant	Hardware Reset, active high	67
DBUS[3:0]	I/O w/ 5V-tolerant	MCU 4-bit DDR Direct bus; 4mA driving strength	75-72
ALE	I w/ 5V-tolerant	MCU Bus ALE, active high	69
RDZ	I w/ 5V-tolerant	MCU Bus RDZ, active high	70
WRZ	I w/ 5V-tolerant	MCU Bus WDZ, active high	71
INT	Output	MCU Bus Interrupt; 4mA driving strength	68

Analog Interface

Pin Name	Pin Type	Function	Pin
RMID		Mid-Scale Voltage Bypass	38
REFP		Internal ADC Top De-coupling Pin	39
REFM		Internal ADC Bottom De-coupling Pin	40
REXT	Analog Input	External Resister 390 ohm to AVDD_DVI	11
HSYNC0	Schmitt Trigger Input w/ 5V-tolerant	Analog HSYNC Input from Channel 0	36
VSYNC0	Schmitt Trigger Input w/ 5V-tolerant	Analog VSYNC Input from Channel 0	37
BIN0M	Analog Input	Reference Ground for Analog Blue Input from Channel 0	27
BIN0P	Analog Input	Analog Blue Input from Channel 0	28
GIN0M	Analog Input	Reference Ground for Analog Green Input from Channel 0	29
GIN0P	Analog Input	Analog Green Input from Channel 0	30
SOGIN0	Analog Input	Sync On Green Input from Channel 0	31
RIN0M	Analog Input	Reference Ground for Analog Red Input from Channel 0	32
RIN0P	Analog Input	Analog Red Input from Channel 0	33
HSYNC1	Schmitt Trigger Input w/ 5V-tolerant	Analog HSYNC Input from Channel 1	18
VSYNC1	Schmitt Trigger Input w/ 5V-tolerant	Analog VSYNC Input from Channel 1	19
BIN1P	Analog Input	Analog Blue Input from Channel 1	20
BIN1M	Analog Input	Reference Ground for Analog Blue Input from Channel 1	21
SOGIN1	Analog Input	Sync On Green Input from Channel 1	22
GIN1P	Analog Input	Analog Green Input from Channel 1	23

CIRCUIT DESCRIPTIONS

Pin Name	Pin Type	Function	Pin
GIN1M	Analog Input	Reference Ground for Analog Green Input from Channel 1	24
RIN1P	Analog Input	Analog Red Input from Channel 1	25
RIN1M	Analog Input	Reference Ground for Analog Red Input from Channel 1	26

DVI Interface

Pin Name	Pin Type	Function	Pin
DVI_R+	Input	DVI Input Channel Red +	207
DVI_R-	Input	DVI Input Channel Red -	208
DVI_G+	Input	DVI Input Channel Green +	2
DVI_G-	Input	DVI Input Channel Green -	3
DVI_B+	Input	DVI Input Channel Blue +	5
DVI_B-	Input	DVI Input Channel Blue -	60
DVI_CK+	Input	DVI Input Clock +	8
DVI_CK-	Input	DVI Input Clock -	9

Video Interface

Pin Name	Pin Type	Function	Pin
VI_CK	Input w/ 5V-tolerant	Digital Video Input Clock	66
VI_DATA[15:0]	Input w/ 5V-tolerant	Digital Video Input Data[15:0]	48-41, 61-54

Digital Audio Interface

Pin Name	Pin Type	Function	Pin
AUMCK	Output	Audio Master Clock Output	188
AUSD	Output	Audio Serial Data Output; 4mA driving strength	189
AUSCK	Output	Audio Serial Clock Output; 4mA driving strength	190
AUWS	Output	Word Select Output; 4mA driving strength	191
AUMUTE	Output	Audio Output Mute Control	192
SPDIFO	Output	S/PDIF Audio Output; 4mA driving strength	193
AIMCK	Input	Audio Master Clock Input	196
AISD	Input	Audio Serial Data Input	197
AISCK	Input	Audio Serial Clock Input	198
AIWS	Input	Word Select Input	199

Not for Proprietary

CIRCUIT DESCRIPTIONS

LVDS Interface

Pin Name	Pin Type	Function	Pin
LVA0M	Output	A-Link Negative LVDS Differential Data Output	171
LVA0P	Output	A-Link Positive LVDS Differential Data Output	170
LVA1M	Output	A-Link Negative LVDS Differential Data Output	169
LVA1P	Output	A-Link Positive LVDS Differential Data Output	168
LVA2M	Output	A-Link Negative LVDS Differential Data Output	167
LVA2P	Output	A-Link Positive LVDS Differential Data Output	166
LVA3M	Output	A-Link Negative LVDS Differential Data Output	161
LVA3P	Output	A-Link Positive LVDS Differential Data Output	160
LVACKM	Output	A-Link Negative LVDS Differential Data Output	165
LVACKP	Output	A-Link Positive LVDS Differential Data Output	164
LVB0M	Output	B-Link Negative LVDS Differential Data Output	187
LVB0P	Output	B-Link Positive LVDS Differential Data Output	186
LVB1M	Output	B-Link Negative LVDS Differential Data Output	181
LVB1P	Output	B-Link Positive LVDS Differential Data Output	180
LVB2M	Output	B-Link Negative LVDS Differential Data Output	179
LVB2P	Output	B-Link Positive LVDS Differential Data Output	178
LVB3M	Output	B-Link Negative LVDS Differential Data Output	175
LVB3P	Output	B-Link Positive LVDS Differential Data Output	174
LVBCKM	Output	B-Link Negative LVDS Differential Data Output	177
LVBCKP	Output	B-Link Positive LVDS Differential Data Output	176

GPO Interface

Pin Name	Pin Type	Function	Pin
PWM0	Output	GPO with PWM Function; 4mA driving strength	200
PWM1	Output	GPO with PWM Function; 4mA driving strength	201
GPO[1]	I/O	GPO / FIELD input; 4mA driving strength	78
GPO[2]	I/O	GPO / Digital VSYNC Input; 4mA driving strength	77
GPO[3]	I/O	GPO / DE Input; 4mA driving strength	76
GPO[4]	I/O	GPO / Secondary Video Clock Input; 4mA driving strength	52
GPO[5]	I/O	GPO / Digital HSYNC Input; 4mA driving strength	51

CIRCUIT DESCRIPTIONS

DRAM Interface

Pin Name	Pin Type	Function	Pin
MVREF	Input	Reference Voltage for DDR SDRAM Interface	104
MCLKE	Output	DRAM Memory Clock Enable	105
MCLKZ	Output	DRAM Memory clock Complementary /Input (for differential clocks)	106
MCLK	Output	DRAM Memory Clock	107
RASZ	Output	Row Address Strobe, active low	112
CASZ	Output	Column Address Strobe, active low	115
WEZ	Output	Write Enable, active low	116
DQM[1:0]	Output	Data Mask Byte Enable	101, 133
DQS[3:0]	Output	Data Strobe	81, 100, 134, 153
BADR[1:0]	Output	Memory Bank Address	110, 111
MADR[11:0]	Output	Memory Address	130-127, 124-117
MDATA[31:0]	I/O	Memory Data	82-85, 88-99, 135-138, 141-152

Misc. Interface

Pin Name	Pin Type	Function	Pin
XIN	Crystal Oscillator Input	Crystal Oscillator Input	203
XOUT	Crystal Oscillator Output	Crystal Oscillator Output	202
DDCD_DA	I/O w/ 5V-tolerant	HDCP Serial Bus Data / DDC data of DVI port; 4mA driving strength	14
DDCD_CK	Input w/ 5V-Tolerant	HDCP Serial Bus Clock / DDC Clock of DVI Port	15
BYPASS		For External Bypass Capacitor	158
VCTRL	Output	Regulator Control	62

Power Pins

Pin Name	Pin Type	Function	Pin
AVDD_DVI	3.3V Power	DVI Power	4, 10
AVDD_ADC	3.3V Power	ADC Power	17, 34
AVDD_PLL	3.3V Power	PLL Power	12
AVDD_PLL2	3.3V Power	PLL Power	109
AVDD_APLL	1.8V Power	Audio PLL Power	49
AVDD_MPLL	3.3V Power	PLL Power	204

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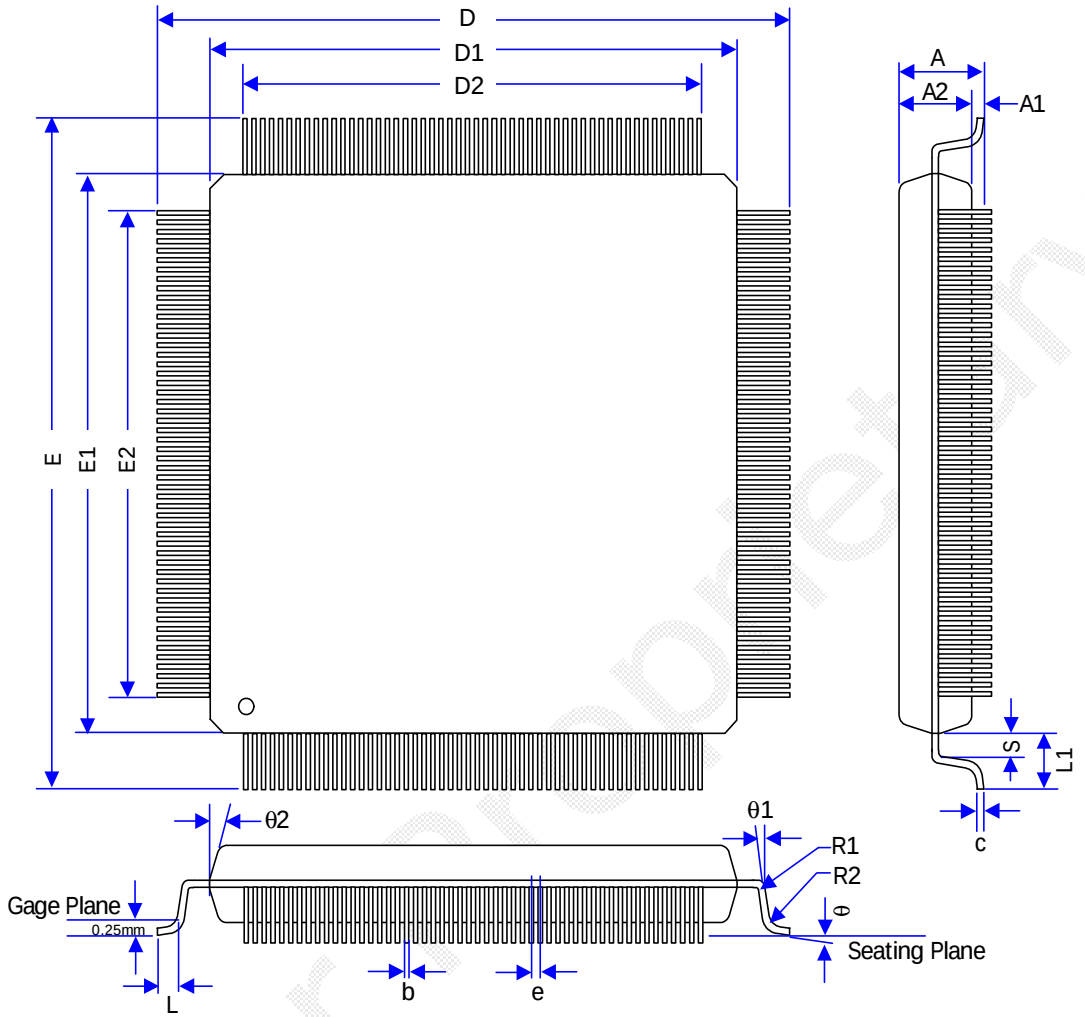
CIRCUIT DESCRIPTIONS

Pin Name	Pin Type	Function	Pin
VDDM	3.3V Power (SDR SDRAM) / 2.5V Power (DDR SDRAM)	DRAM Interface Power	86, 102, 113, 125, 139, 154
VDDP	3.3V Power	Digital Output Power	66, 162, 182
VDDC	1.8V Power	Digital Core Power	63, 79, 131, 156, 173, 185, 195
GND	Ground	Ground	1, 7, 13, 16, 35, 50, 64, 65, 80, 87, 103, 108, 114, 126, 132, 140, 155, 157, 159, 163, 172, 183, 184, 194, 205, 206

MStar Proprietary

MECHANICAL DIMENSIONS



Symbol	Millimeter			Inch		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	-	-	4.10	-	-	0.161
A1	0.25	-	-	0.010	-	-
A2	3.20	3.32	3.60	0.126	0.131	0.142
D	31.20			1.228		
D1	28.00			1.102		
D2	25.50			1.004		
E	31.20			1.228		
E1	28.00			1.102		
E2	25.50			1.004		
R1	0.13	-	-	0.005	-	-
R2	0.13	-	0.30	0.005	-	0.012

Symbol	Millimeter			Inch		
	Min.	Nom.	Max.	Min.	Nom.	Max.
θ	0°	-	7°	0°	-	7°
θ1	0°	-	-	0°	-	-
θ2	8° Ref			8° Ref		
b	0.17	0.20	0.27	0.007	0.008	0.011
c	0.11	0.15	0.23	0.004	0.006	0.009
e	0.50 BSC.			0.020 BSC.		
L	0.73	0.88	1.03	0.029	0.035	0.041
L1	1.60 Ref			0.063 Ref		
S	0.20	-	-	0.008	-	-

CIRCUIT DESCRIPTIONS

General Description

Introduction

The VCT 49xxI is an IC family of high-quality single-chip TV processors. Modular design and deep-submicron technology allow the economic integration of features in all classes of single-scan TV sets. The VCT 49xxI family is based on functional blocks contained and approved in existing products like DRX 396xA, MSP 34x5G, VSP 94x7B, DDP 3315C, and SDA 55xx.

Each member of the family contains the entire IF, audio, video, display, and deflection processing for 4:3 and 16:9 50/60-Hz mono and stereo TV sets. The integrated microcontroller is supported by a powerful OSD generator with integrated Teletext & CC acquisition including on-chip page memory.

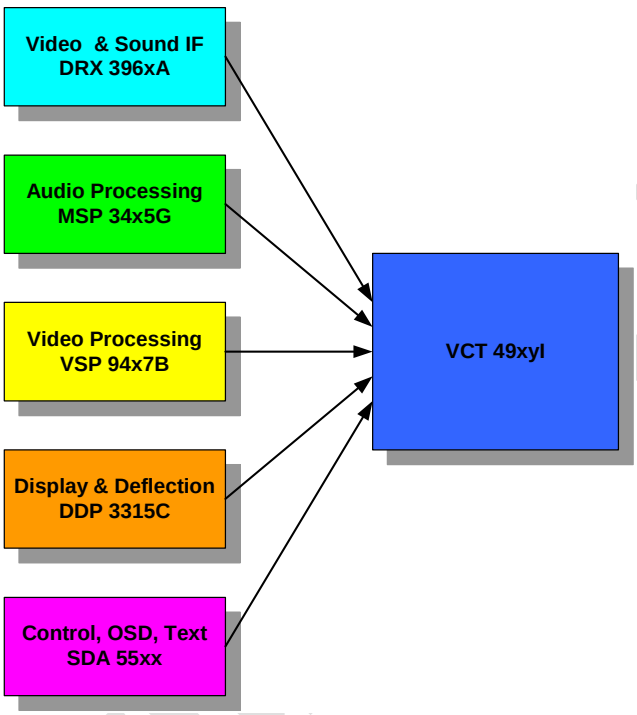


Fig. : Single-chip VCT 49xxI

Features

The VCT 49xxI family offers a rich feature set, covering the whole range of state-of-the-art 50/60-Hz TV applications.

- PSSDIP88-1/-2 package
- PMQFP144-2 package
- Submicron CMOS technology
- Low-power standby mode
- Single 20.25-MHz reference crystal
- 8-bit 8051 instruction set compatible CPU
- Up to 256 kB on-chip program ROM
- WST, PDC, VPS, and WSS acquisition
- Closed Caption and V-chip acquisition
- Up to 10 pages on-chip teletext memory
- Multi-standard QSS IF processing with single SAW
- FM Radio and RDS with standard TV tuner
- TV-sound demodulation:
  - all A2 standards
  - all NICAM standards
  - BTSC/SAP with MNR (DBX optional)
  - EIA-J
- Baseband sound processing for loudspeaker channel:
  - volume
  - bass and treble
  - loudness
  - balance
  - spatial effect (e.g. pseudo stereo)
  - Micronas AROUND (virtual Dolby optional)
  - Micronas BASS
- CVBS, S-VHS, YC_rC_b and RGB inputs
- 4H adaptive comb filter (PAL/NTSC)
- multi-standard color decoder (PAL/NTSC/SECAM)
- Nonlinear horizontal scaling “panorama vision”
- Luma and chroma transient improvement (LTI, CTI)
- Non-linear color space enhancement (NCE)
- Dynamic black level expander (BLE)
- Scan velocity modulation output
- Soft start/stop of H-drive
- Vertical angle and bow correction
- Average and peak beam current limiter
- Nonlinear and dynamic EHT compensation
- Black switch off procedure (BSO)

CIRCUIT DESCRIPTIONS

Chip Architecture

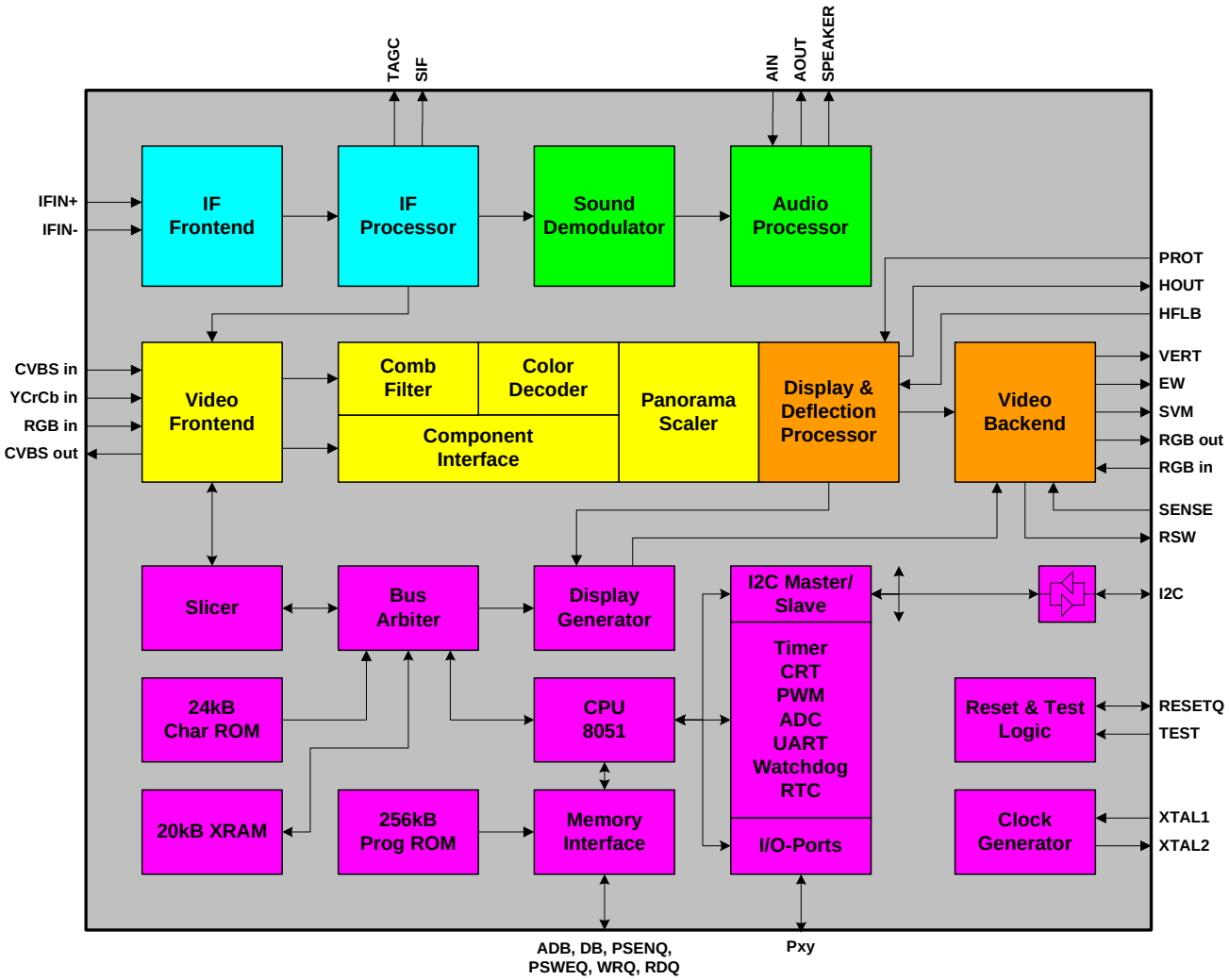


Fig. : Block diagram of the VCT 49xxI

WORK

CIRCUIT DESCRIPTIONS

Pin Connections and Short Descriptions

NC = not connected
LV = if not used, leave vacant
OBL = obligatory; connect as described in circuit diagram
IN = Input Pin
OUT = Output Pin
SUPPLY = Supply Pin

Pin No.		Pin Name	Type	Connection (If not used)	Short Description
PSSDIP 88-pin	PMQFP-2 144-pin				
1	128	GND	SUPPLY	OBL	Ground Platform
2	129	VSUP5.0BE	SUPPLY	OBL	Supply Voltage Analog Video Back-end, 5.0 V
3	130	TEST	IN	GND	Test Input, reserved for Test
4	131	VERT+	OUT	LV	Differential Vertical Sawtooth Output
5	132	VERT-	OUT	LV	Differential Vertical Sawtooth Output
6	133	EW	OUT	LV	Vertical Parabola Output
7	134	RSW2	OUT	LV	Range Switch 2 Output
8	135	RSW1	OUT	LV	Range Switch 1 Output
9	136	SENSE	IN	GND	Sense ADC Input
10	137	GNDM	IN	GND	Reference Ground for Sense ADC
11	138	FBIN	IN	GND	Fast Blank Input, Back-end
12	139	RIN	IN	GND	Analog Red Input, Back-end
13	140	GIN	IN	GND	Analog Green Input, Back-end
14	141	BIN	IN	GND	Analog Blue Input, Back-end
15	142	SVMOUT	OUT	VSUP5.0BE	Scan Velocity Modulation Output
16	143	ROUT	OUT	VSUP5.0BE	Analog Red Output
17	144	GOUT	OUT	VSUP5.0BE	Analog Green Output
18	1	BOUT	OUT	VSUP5.0BE	Analog Blue Output
19	2	VRD		OBL	Reference Voltage for RGB DACs
20	3	XREF		OBL	Reference Current for RGB DACs
21	4	VSUP3.3BE	SUPPLY	OBL	Supply Voltage Analog Video Back-end, 3.3 V
22	5	GND	SUPPLY	OBL	Ground Platform
23	6	GND	SUPPLY	OBL	Ground Platform
24	7	VSUP3.3IO	SUPPLY	OBL	Supply Voltage I/O Ports, 3.3 V
25	8	VSUP3.3DAC	SUPPLY	OBL	Supply Voltage Video DACs, 3.3 V
26	9	GNDDAC	SUPPLY	OBL	Ground Video DACs
27	10	SAFETY	IN	GND	Safety Input

WORK IN PROGRESS

CIRCUIT DESCRIPTIONS

Pin No.		Pin Name	Type	Connection (If not used)	Short Description
PSSDIP 88-pin	PMQFP-2 144-pin				
28	11	HFLB	IN	HOUT	Horizontal Flyback Input
29	12	HOUT	OUT	LV	Horizontal Drive Output
30	13	VPROT	IN	GND	Vertical Protection Input
	37	PWMV	OUT	LV	PWM Vertical Output
	38	DFVBL	OUT	LV	Dynamic Focus Vertical Blanking Output
31	39	SDA	IN/OUT	OBL	I^2C Bus Data Input/Output
32	40	SCL	IN/OUT	OBL	I^2C Bus Clock Input/Output
33	41	P21	IN/OUT	LV	Port 2, Bit 1 Input/Output
34	42	P20	IN/OUT	LV	Port 2, Bit 0 Input/Output
35	43	P17	IN/OUT	LV	Port 1, Bit 7 Input/Output
36	44	P16	IN/OUT	LV	Port 1, Bit 6 Input/Output
37	45	P15	IN/OUT	LV	Port 1, Bit 5 Input/Output
38	46	P14	IN/OUT	LV	Port 1, Bit 4 Input/Output
39	47	P13	IN/OUT	LV	Port 1, Bit 3 Input/Output
40	48	P12	IN/OUT	LV	Port 1, Bit 2 Input/Output
41	49	P11	IN/OUT	LV	Port 1, Bit 1 Input/Output
42	50	P10	IN/OUT	LV	Port 1, Bit 0 Input/Output
43	53	VSUP3.3FE	SUPPLY	OBL	Supply Voltage Analog Video Front-end, 3.3 V
44	54	GND	SUPPLY	OBL	Ground Platform
45	55	GND	SUPPLY	OBL	Ground Platform
46	56	VSUP1.8FE	SUPPLY	OBL	Supply Voltage Analog Video Front-end, 1.8 V
47	57	VOUT3	OUT	LV	Analog Video 3 Output
48	58	VOUT2	OUT	LV	Analog Video 2 Output
49	59	VOUT1	OUT	LV	Analog Video 1 Output
50	60	VIN1	IN	GND	Analog Video 1 Input
51	61	VIN2	IN	GND	Analog Video 2 Input
52	62	VIN3	IN	GND	Analog Video 3 Input
53	63	VIN4	IN	GND	Analog Video 4 Input
54	64	VIN5	IN	GND	Analog Video 5 Input
55	65	VIN6	IN	GND	Analog Video 6 Input
56	66	VIN7	IN	GND	Analog Video 7 Input
57	67	VIN8	IN	GND	Analog Video 8 Input
58	68	VIN9	IN	GND	Analog Video 9 Input

WORK IN PROGRESS

CIRCUIT DESCRIPTIONS

Pin No.		Pin Name	Type	Connection (If not used)	Short Description
PSSDIP 88-pin	PMQFP-2 144-pin				
59	69	VIN10	IN	GND	Analog Video 10 Input
60	70	VIN11	IN	GND	Analog Video 11 Input
61	98	P23	IN/OUT	LV	Port 2, Bit 3 Input/Output
62	99	P22	IN/OUT	LV	Port 2, Bit 2 Input/Output
63	100	XTAL2	OUT	OBL	Analog Crystal Output
64	101	XTAL1	IN	OBL	Analog Crystal Input
65	102	VSUP1.8DIG	SUPPLY	OBL	Supply Voltage Digital Core, 1.8 V (main and standby supply)
66	103	GND	SUPPLY	OBL	Ground Platform
67	104	GND	SUPPLY	OBL	Ground Platform
68	105	VSUP3.3DIG	SUPPLY	OBL	Supply Voltage Digital Core, 3.3 V (main and standby supply)
69	106	VSUP5.0IF	SUPPLY	OBL	Supply Voltage Analog IF Front-end, 5.0 V
70	107	GNDIF	SUPPLY	OBL	Ground Analog IF Front-end
71	108	RESETQ	IN/OUT	OBL	$\overline{\text{Reset}}$ Input/Output
72	109	IFIN+	IN	$VREF_{IF}$	Differential IF Input
73	110	IFIN-	IN	$VREF_{IF}$	Differential IF Input
74	111	VREFIF		OBL	Reference Voltage, IF ADC
75	112	TAGC	OUT	LV	Tuner AGC Output
76	113	AIN1R / SIF	IN/OUT	GND	Analog Audio 1 Input, Right Analog 2nd Sound IF Output
77	114	AIN1L	IN	GND	Analog Audio 1 Input, Left
78	115	AIN2R	IN	GND	Analog Audio 2 Input, Right
79	116	AIN2L	IN	GND	Analog Audio 2 Input, Left
	117	AIN3R	IN	GND	Analog Audio 3 Input, Right
	118	AIN3L	IN	GND	Analog Audio 3 Input, Left
	119	AOUT2R	OUT	LV	Analog Audio 2 Output, Right
	120	AOUT2L	OUT	LV	Analog Audio 2 Output, Left
80		AIN3R / AOUT2R	IN / OUT	LV	Analog Audio 3 Input, Right Analog Audio 2 Output, Right
81		AIN3L / AOUT2L	IN / OUT	LV	Analog Audio 3 Input, Left Analog Audio 2 Output, Left
82	121	AOUT1R	OUT	LV	Analog Audio 1 Output, Right
83	122	AOUT1L	OUT	LV	Analog Audio 1 Output, Left
84	123	SPEAKERR	OUT	LV	Analog Loudspeaker Output, Right

WORK IN PROGRESS

CIRCUIT DESCRIPTIONS

Pin No. PSSDIP 88-pin	Pin No. PMQFP-2 144-pin	Pin Name	Type	Connection (If not used)	Short Description
85	124	SPEAKERL	OUT	LV	Analog Loudspeaker Output, Left
86	125	VREFAU		OBL	Reference Voltage, Audio
87	126	VSUP8.0AU	SUPPLY	OBL	Supply Voltage Analog Audio, 8.0 V
88	127	GND	SUPPLY	OBL	Ground Platform
	71	P37 / 656IO7	IN/OUT	LV	Port 3, Bit 7 Input/Output Digital 656 Bus 7 Input/Output
	72	P36 / 656IO6	IN/OUT	LV	Port 3, Bit 6 Input/Output Digital 656 Bus 6 Input/Output
	73	P35 / 656IO5	IN/OUT	LV	Port 3, Bit 5 Input/Output Digital 656 Bus 5 Input/Output
	74	P34 / 656IO4	IN/OUT	LV	Port 3, Bit 4 Input/Output Digital 656 Bus 4 Input/Output
	75	P33 / 656IO3	IN/OUT	LV	Port 3, Bit 3 Input/Output Digital 656 Bus 3 Input/Output
	76	GNDEIO	SUPPLY	OBL	Ground Extended I/O Ports
	77	VSUP3.3EIO	SUPPLY	OBL	Supply Voltage Extended I/O Ports, 3.3 V
	78	P32 / 656IO2	IN/OUT	LV	Port 3, Bit 2 Input/Output Digital 656 Bus 2 Input/Output
	79	P31 / 656IO1	IN/OUT	LV	Port 3, Bit 1 Input/Output Digital 656 Bus 1 Input/Output
	80	P30 / 656IO0	IN/OUT	LV	Port 3, Bit 0 Input/Output Digital 656 Bus 0 Input/Output
	81	P26 / 656VIO	IN/OUT	LV	Port 2, Bit 6 Input/Output Digital 656 Vsync Input/Output
	82	P25 / 656HIO	IN/OUT	LV	Port 2, Bit 5 Input/Output Digital 656 Hsync Input/Output
	83	P24 / 656CLKIO	IN/OUT	LV	Port 2, Bit 4 Input/Output Digital 656 Clock Input/Output
	31	ADB19	OUT	LV	Address Bus 19 Output
	21	ADB18	OUT	LV	Address Bus 18 Output
	19	ADB17	OUT	LV	Address Bus 17 Output
	22	ADB16	OUT	LV	Address Bus 16 Output
	23	ADB15	OUT	LV	Address Bus 15 Output
	18	ADB14	OUT	LV	Address Bus 14 Output
	17	ADB13	OUT	LV	Address Bus 13 Output
	26	ADB12	OUT	LV	Address Bus 12 Output
	14	ADB11	OUT	LV	Address Bus 11 Output

WORK IN PROGRESS

CIRCUIT DESCRIPTIONS

Pin No.		Pin Name	Type	Connection (If not used)	Short Description
PSSDIP 88-pin	PMQFP-2 144-pin				
	96	ADB10	OUT	LV	Address Bus 10 Output
	15	ADB9	OUT	LV	Address Bus 9 Output
	16	ADB8	OUT	LV	Address Bus 8 Output
	27	ADB7	OUT	LV	Address Bus 7 Output
	28	ADB6	OUT	LV	Address Bus 6 Output
	29	ADB5	OUT	LV	Address Bus 5 Output
	30	ADB4	OUT	LV	Address Bus 4 Output
	84	ADB3	OUT	LV	Address Bus 3 Output
	85	ADB2	OUT	LV	Address Bus 2 Output
	86	ADB1	OUT	LV	Address Bus 1 Output
	87	ADB0	OUT	LV	Address Bus 0 Output
	88	DB0	IN/OUT	LV	Data Bus 0 Input/Output
	89	DB1	IN/OUT	LV	Data Bus 1 Input/Output
	90	DB2	IN/OUT	LV	Data Bus 2 Input/Output
	91	DB3	IN/OUT	LV	Data Bus 3 Input/Output
	92	DB4	IN/OUT	LV	Data Bus 4 Input/Output
	93	DB5	IN/OUT	LV	Data Bus 5 Input/Output
	94	DB6	IN/OUT	LV	Data Bus 6 Input/Output
	95	DB7	IN/OUT	LV	Data Bus 7 Input/Output
	32	RDQ	OUT	LV	$\overline{\text{Data Read Enable}}$ Output
	33	WRQ	OUT	LV	$\overline{\text{Data Write Enable}}$ Output
	34	OCF	OUT	LV	Opcode Fetch Output
	35	ALE	OUT	LV	Address Latch Enable Output
	36	RSTQ	OUT	LV	$\overline{\text{Internal CPU Reset}}$ Output
	97	PSENQ	OUT	LV	$\overline{\text{Program Store Enable}}$ Output
	20	PSWEQ	OUT	LV	$\overline{\text{Program Store Write Enable}}$ Output
	51	XROMQ	IN	OBL	$\overline{\text{External ROM Enable}}$ Input
	52	EXTIFQ	IN	LV	$\overline{\text{Enable External Interface}}$ Input
	24	STOPQ	IN	LV	$\overline{\text{Stop CPU}}$ Input
	25	ENEQ	IN	LV	$\overline{\text{Enable Emulation}}$ Input

WORK IN PROGRESS

CIRCUIT DESCRIPTIONS

Pin Descriptions

Supply Pins

VSUP1.8DIG – Supply Voltage 1.8 V
This pin is main and standby supply for the digital core logic of controller, video, display and deflection processing.

VSUP1.8FE – Supply Voltage 1.8 V
This pin is main supply for the analog video front-end.

VSUP3.3FE – Supply Voltage 3.3 V
This pin is main supply for the analog video front-end.

VSUP3.3IO – Supply Voltage 3.3 V
This pin is main and standby supply for the digital I/O-ports.

VSUP3.3DIG – Supply Voltage 3.3 V
This pin is main supply for the digital core logic of IF and audio processing and digital video back-end.

VSUP3.3BE – Supply Voltage 3.3 V
This pin is main supply for the analog video back-end.

VSUP5.0BE – Supply Voltage 5.0 V
This pin is main supply for the analog video back-end.

VSUP8.0AU – Supply Voltage 8.0 V
This pin is main supply for the analog audio processing.

GND – Ground Platform
This pin is main ground for all above supplies.

VSUP3.3DAC – Supply Voltage 3.3 V
This pin is main supply for the video DACs.

GNDDAC – Ground for 3.3 V Video DAC Supply

VSUP5.0IF – Supply Voltage 5.0 V
This pin is main supply for the analog IF front-end.

GNDIF – Ground for 5.0 V IF Supply

VSUP3.3EIO – Supply Voltage 3.3 V
This pin is main and standby supply for the extended digital I/O-ports available in QFP package only. It is internally connected to **VSUP3.3IO.**

GNDEIO – Ground for 3.3 V Extended I/O Supply
It is internally connected to GND.

Application Note:
All **GND** pins must be connected to a low-resistive ground plane underneath the IC. All supply pins must be connected separately with short and low-resistive lines to the power supply. Decoupling capacitors from **VSUPxx** to **GND** have to be placed as closely as possible to these pins. It is recommended to use more than one capacitor. By choosing different values, the frequency range of active decoupling can be extended.

IF Pins

VREFIF – Reference Voltage for Analog IF (Fig. 4–9)
This pin must be connected to **GNDIF** via a circuitry according to the application circuit. Low inductance caps are necessary.

IFIN+, IFIN- – Balanced IF Input (Fig. 4–6)
These pins must be connected to the SAW filter output. The SAW filter has to be placed as close as possible. The layout of the IF input should be symmetrical with respect to **GNDIF**.

SIF – 2nd Sound IF Output (Fig. 4–8)
Output level is set via I^2C-Bus. An appropriate sound processor (e.g. MSP) can be connected to this pin. This pin is also configurable as audio input (see Fig. 4–10).

TAGC – Tuner AGC Output (Fig. 4–7)
This pin controls the delayed tuner AGC. As it is a noise-shaped-I-DAC output, it has to be connected according to the application circuit.

Audio Pins

VREFAU – Reference Voltage for Analog Audio (Fig. 4–14)
This pin serves as the internal ground connection for the analog audio circuitry. It must be connected to the **GND** pin with a 3.3 µF and a 100 nF capacitor in parallel. This pins shows a DC level of typically 3.77 V.

AIN1 L – Audio 1 Inputs (Fig. 4–10)
The analog input signal for audio 1 is fed to this pin. Analog input connection must be AC coupled.

AIN1 R – Audio 1 Inputs (Fig. 4–10)
The analog input signal for audio 1 is fed to this pin. Analog input connection must be AC coupled. This pin is also configurable as sound IF output (see Fig. 4–8).

AIN2 R/L – Audio 2 Inputs (Fig. 4–10)
The analog input signal for audio 2 is fed to this pin. Analog input connection must be AC coupled.

AIN3 R/L – Audio 3 Inputs (Fig. 4–10)
The analog input signal for audio 3 is fed to this pin. Analog input connection must be AC coupled.

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CIRCUIT DESCRIPTIONS

General Description

AOUT1 R/L – Audio 1 Outputs (Fig. 4–11)
Output of the analog audio 1 signal. Connections to these pins are intended to be AC coupled.

AOUT2 R/L – Audio 2 Outputs (Fig. 4–11)
Output of the analog audio 2 signal. Connections to these pins are intended to be AC coupled.

SPEAKER R/L – Loudspeaker Outputs (Fig. 4–13)
Output of the loudspeaker signal. A 1 nF capacitor to **GND** must be connected to these pins. Connections to these pins are intended to be AC-coupled.

Video Pins

VIN 1–11 – Analog Video Input (Fig. 4–15)
These are the analog video inputs. A CVBS, S-VHS, YCrCb or RGB/FB signal is converted using the luma, chroma and component AD converters. The input signals must be AC-coupled by 100nF. In case of an analog fast blank signal carrying alpha blending information the input signal must be DC-coupled.

VOUT 1-3 – Analog Video Output (Fig. 4–16)
The analog video inputs that are selected by the video source select matrix are output at these pins.

RIN, GIN, BIN – Analog RGB Input (Fig. 4–17)
These pins are used to insert an external analog RGB signal, e.g. from a SCART connector which can be switched to the analog RGB outputs with the fast blank signal. Separate brightness and contrast settings for the external analog signals are provided.

FBIN – Fast Blank Input (Fig. 4–18)
This pin is used to switch the RGB outputs to the external analog RGB inputs. The active level (low or high) can be selected by software.

ROUT, GOUT, BOUT – Analog RGB Output (Fig. 4–19)
These pins are the analog Red/Green/Blue outputs of the back-end. The outputs are current sinks.

SVMOUT – Scan Velocity Modulation Output (Fig. 4–19)
This output delivers the analog SVM signal. The D/A converter is a current sink like the RGB D/A converters. At zero signal the output current is 50% of the maximum output current.

VRD – DAC Reference Decoupling (Fig. 4–20)
Via this pin the RGB-DAC reference voltage is decoupled by an external capacitor. The DAC output currents depend on this voltage, therefore a pulldown transistor can be used to shut off all beam currents. A decoupling capacitor of 4.7 µF in parallel to 100 nF (low inductance) is required.

XREF – DAC Current Reference (Fig. 4–20)
External reference resistor for DAC output currents, typical 10 kΩ to adjust the output current of the D/A converters. (see recommended operating conditions). This resistor has to be connected to ground as closely as possible to the pin.

CRT Pins

VPROT – Vertical Protection Input (Fig. 4–22)
The vertical protection circuitry prevents the picture tube from burn-in in the event of a malfunction of the vertical deflection stage. If the peak-to-peak value of the sawtooth signal from the vertical deflection stage is too small, the RGB output signals are blanked.

SAFETY – Safety Input (Fig. 4–22)
This input has two thresholds. A signal between the lower and upper threshold means normal function. A signal below the lower threshold or above the upper threshold is detected as malfunction and the RGB signals will be blanked.

HOUT – Horizontal Drive Output (Fig. 4–21)
This open source output supplies the drive pulse for the horizontal output stage. An external pulldown resistor has to be used. The polarity and gating with the flyback pulse are selectable by software.

HFLB – Horizontal Flyback Input (Fig. 4–22)
Via this pin the horizontal flyback pulse is supplied to the VCT 49xxI.

VERT+, VERT– – Vertical Sawtooth Output (Fig. 4–23)
These pins supply the symmetrical drive signal for the vertical output stage. The drive signal is generated with 15-bit precision. The analog voltage is generated by a 4 bit current-DAC with an external resistor of 6.8 kΩ and uses digital noise shaping.

EW – East-West Parabola Output (Fig. 4–24)
This pin supplies the parabola signal for the East-West correction. The drive signal is generated with 15 bit precision. The analog voltage is generated by a 4 bit current-DAC with an external resistor of 6.8 kΩ and uses digital noise shaping.

PWMV – PWM Vertical Output (Fig. 4–35)
This pin provides an adjustable vertical parabola with 7 bit resolution and appr. 79.4 kHz PWM frequency.

DFVBL – Dynamic Focus Vertical Blanking (Fig. 4–35)
This pin supplies the blank pulse for dynamic focus during vertival blanking period or a free programmable horizontal pulse for horizontal dynamic focus generation.

WORK IN PROGRESS

General Description

SENSE – Measurement ADC Input (Fig. 4–27)
This is the input of the analog to digital converter for the picture and tube measurement. Three measurement ranges are selectable with RSW1 and RSW2.

GNDM – Measurement ADC Reference Input
This is the reference ground for the measurement A/D converter. Connect this pin to GND.

RSW1 – Range Switch1 for Measuring ADC (Fig. 4–25)
These pin is an open drain pulldown output. During cutoff and white drive measurement the switch is off. During the rest of time it is on. The RSW1 pin can be used as second measurement ADC input for picture beam current measurement.

RSW2 – Range Switch2 for Measuring ADC (Fig. 4–26)
These pin is an open drain pulldown output. During cutoff measurement the switch is off. During white drive measurement the switch is on. Also during the rest of time it is on. It is used to set the range for white drive current measurement.

Controller Pins

XTAL1 – Crystal Input and **XTAL2** Crystal Output (Fig. 4–28)
These pins connect a 20.25 MHz crystal to the internal oscillator. An external clock can be fed into XTAL1.

RESETQ – Reset Input/Output (Fig. 4–29)
A low level on this pin resets the VCT 49xxI. The internal CPU can pull down this pin to reset external devices connected to this pin.

TEST – Test Input (Fig. 4–30)
This pin enables factory test modes. For normal operation, it must be connected to ground.

SCL – I^2C Bus Clock (Fig. 4–31)
This pin delivers the I^2C bus clock line. The signal can be pulled down by external slave ICs to slow down data transfer.

SDA – I^2C Bus Data (Fig. 4–31)
This pin delivers the I^2C bus data line.

P10–**P13, P20**–**P23** – I/O Port (Fig. 4–32)
These pins provide CPU controlled I/O ports.

P14–**P17** – I/O Port (Fig. 4–33)
These pins provide CPU controlled I/O ports. Additionally they can be used as analog inputs for the controller ADC.

P24–**P26, P30**–**P37** – I/O Port (Fig. 4–34)
These pins provide CPU controlled I/O ports.

ADB0–**ADB19** – Address Bus Output (Fig. 4–35)
These 20 lines provide the CPU address bus output to access external memory.

DB0–**DB7** – Data Bus Input/Output (Fig. 4–36)
These 8 lines provide the bidirectional CPU data bus to access external memory.

WRQ – $\overline{\text{Data Write Enable}}$ Output (Fig. 4–35)
This pin controls the direction of data exchange between the CPU and the external data memory device (SRAM).

RDQ – $\overline{\text{Data Read Enable}}$ Output (Fig. 4–35)
This pin is used to enable the output driver of the external data memory device (SRAM) for read access.

PSENQ – $\overline{\text{Program Store Enable}}$ Output (Fig. 4–35)
This pin is used to enable the output driver of the external program memory device (ROM/FLASH) for read access.

PSWEQ – $\overline{\text{Program Store Write Enable}}$ Output (Fig. 4–35)
This pin is used to write into the external program flash memory device.

XROMQ – $\overline{\text{External ROM Enable}}$ Input (Fig. 4–37)
This pin must be pulled low to access the external program memory. **XROMQ** has an internal pull-up resistor.

EXTIFQ – $\overline{\text{Enable External Memory Interface}}$ Input (Fig. 4–37)
This pin must be pulled low to enable the external memory interface. **EXTIFQ** has an internal pull-up resistor.

STOPQ – $\overline{\text{Stop}}$ CPU Input (Fig. 4–37)
Applying a low level during the input phase freezes the realtime relevant internal peripherals such as timers and interrupt controller. **STOPQ** has an internal pull-up resistor.

ENEQ – $\overline{\text{Enable Emulation}}$ Input (Fig. 4–37)
Only if this pin is set to low level, STOPQ and OCF are operational. **ENEQ** has an internal pull-up resistor.

ALE – Address Latch Enable Output (Fig. 4–35)
This signal indicates changes on the address bus.

OCF – Opcode Fetch Output (Fig. 4–35)
A high level driven by the CPU during output phase indicates the beginning of a new instruction.

RSTQ – $\overline{\text{Internal CPU Reset}}$ Input/Output (Fig. 4–38)
This pin is used for emulation purpose only. A low level on this pin resets the CPU. It also indicates an internal reset of the CPU.

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CIRCUIT DESCRIPTIONS

General Description

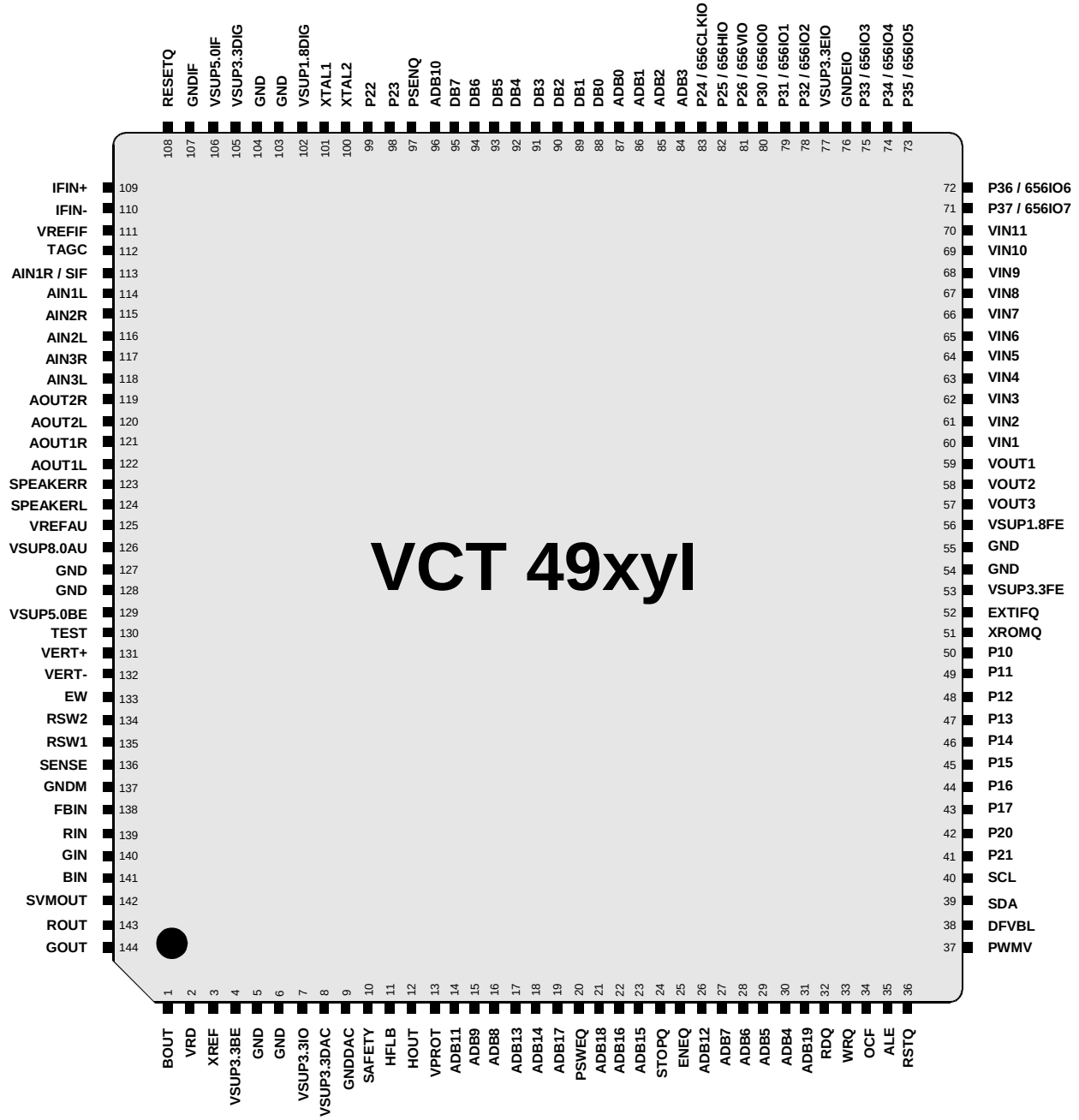

Fig. PMQFP144-2 package

CIRCUIT DESCRIPTIONS

Advance Information Supplement

Subject:	Additional Info for VCT 49xyI
Data Sheet Concerned:	VCT 49xyI 6251-573-1AI, Edition Feb. 18, 2004
Supplement:	Version History
Edition:	Dec. 16, 2004

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Changes to the previous revision are indicated by change bars. Please note section 2.1.1.2., which is of importance for the use of the VCT-I F1 in combination with NICAM-audio modes.

1. VCT 49xyI Version History

1.1. Field Problems

Field test results are available for the VCT 49xyI versions C7 to D5. The versions F1 and F2 are intended to solve all listed field problems.

Table 1–1: History of field problems

No.	Field Problem	C7	D2	D4	D5	F1	F2	Comment
FP01	Streaky Noise	x	x	x	x			Problem solved in F1
FP02	Modulator Imbalance	x	x	x	x			Problem solved in F1
FP03	FM Modulation	x	x	x	x			Problem solved in F1
FP04	Color Clipping	x	x	x	x	x		Problem to be solved in F2
FP05	Closed Caption Performance	x	x	x	x			Problem to be solved in F1
FP06	VSP-AGC performance	x	x	x	x	x		Problem to be solved in F2
FP07	Sync/H-PLL performance	x	x	x	x	x		Problem to be solved in F2

1.2. Functional Problems

For a more detailed description and workarounds of the functional problems please refer to the list of the particular VCT 49xyI version in the next sections. The problem numbers are consistent throughout the whole document. The versions F1 and F2 are intended to solve the remaining problems.

Table 1–2: History of functional problems

No.	Functional Problem	C6	C7	D2	D4	D5	F1	F2	Comment
18	Vertical Synchronisation	x	x						Problem solved in D2
26	Picture Frame Blanked	x	x						Problem solved in D2
34	Reset after Read	x	x						Problem solved in D2

Table 1–2: History of functional problems, continued

No.	Functional Problem	C6	C7	D2	D4	D5	F1	F2	Comment
39	Peaking Filter	x	x						Problem solved in D2
40	Bandwidth of Antialias Filter	x	x						Problem solved in D2
41	SVM Overflow	x	x						Problem solved in D2
42	ADC Initialisation	x	x						Problem solved in D2
43	a) Clock Noise	!	!	!	!	!	!	!	! = Applicative methods solve the problem to a large extent
	b) IF-Nonlinearity	x	x	x*)	x	x	x		*) slight degradation in comparison to C6/7, D4/5. Problem to be solved in F2
45	DRX Video-DAC Headroom	x							Problem solved in C7
46	HORPOS changes color multi-plex	x	x						Problem solved in D2
47	Preframe Generator	x	x						Problem solved in D2
48	DRX AGC Hangup	x	x						Problem solved in D2
50	Fastblank Monitor	x	x	x	x	x			Problem solved in F1
51	East/West Glitch			!	!	!			Problem appeared in D2, Problem solved in F1 ! = workaround available
52	OSD Jitter			x	x				Problem appeared in D2, Problem solved in D5
53	MSP Automatic Standard Detection for EIA-J	x	x	x					Problem solved in D4
54	MSP Standard Toggle in HDEV-Mode fails	x	x	x					Problem solved in D4
55	OSD Offset Compensation	x	x	x	x	x			Problem solved in F1
56	ESD Induced Reset			!	!	!			Problem appeared in D2, Problem solved in F1 ! = workaround available
57	White Blanking Line in OSD	!	!	!	!	!			Problem solved in F1 ! = workaround available
58	EHT			!	!	!			Problem appeared in D2, Problem solved in F1 ! = workaround available
60	VCR detection “TVMODE”	x	x	!	!	!	!	!	! = Workaround available no redesign planned
61	Vertical flywheel mode (VFLYWHLMD)	!	!	!	!	!	!	!	! = Workaround available no redesign planned
62	BLE	!	!	!	!	!			Problem solved in F1 ! = workaround available

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Table 1–2: History of functional problems, continued

No.	Functional Problem	C6	C7	D2	D4	D5	F1	F2	Comment
63	ODC-Modes: FHPULLIN/ SHPULLIN	!	!	!	!	!	!	!	! = Workaround available no redesign planned
64	Safety Pin	x	x	x	x	x			Problem solved in F1
65	13.5MHz Backend Mode	-	-	x	x	x			- = new feature in D2, Problem solved in F1
66	ITU656 Interference	-	-	x	x	x			- = new feature in D2, Problem solved in F1
67	Audio EIA-J: Plop from stereo to mono	x	x	x	x	x	x		under investigation Problem to be solved in F2
68	BSO	x	x	x	x	x			Problem solved in F1
69	H-Out Jitter	!	!	x	x	x			Problem solved in F1 ! = workaround available
70	SCE Luma Input	-	-	x	x	x			- = new feature in D2, Problem solved in F1
71	YUV ECO Mode	x	x	x	x	x			Problem solved in F1
72	Scaler Bondoption	x	x	x	x	x			Problem solved in F1
73	FM radio not working						!		Problem appeared in F1, Problem to be solved in F2 ! = workaround available
74	ITU656 Biterror						x		Problem appeared in F1, Problem to be solved in F2

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7. VCT 49xyI-C7

The VCT 49xyI-C7 is pin-compatible to VCT 49xyI-C6 and VCT 49xyI-C4.

Problem 45 has been solved. Problem 43 is partly solved: Improved internal clock suppression leads to reduced noise floor and better video snr. Problems 53 and 54 have not been detected before D2.

VCT 49xyI-C7 includes functionality of DRX396xA-H8.

Table 7–1: Functional problems of VCT 49xyI-C7:

No.	Problem	Description	Comment	OK
18	Vertical Synchronisation	Vertical pull-in after channel change takes too long	hardware redesign D1 workaround: increase LPFOPOFF	D1
26	Picture Frame Blanked	Left side of picture frame is blanked if HORPOSG<180.	hardware redesign D1	D1
34	Reset after Read	All I2C register with "reset by read" are not functional (NMSTATUS, LBDSTATUS, FBLACTIVE, FBFALL, FBRISE, PFBL/G/R/B).	hardware redesign D1	D1
39	Peaking Filter	In case of PKCF=2,3, the dynamic peaking adaption doesn't work. Thus the peaking signal is limited only.	hardware redesign D1	D1
40	Bandwidth of Antialias Filter	The bandwidth adjustment of the antialias filter 1-6 is disturbed. This causes wrong filter settings after reset and/or after a modification of TRIM_FILTER1-6	hardware redesign D1 workaround: <0xb0 0x2f 0x00 0x01>	D1
41	SVM Overflow	The SVM output signal is not limited correctly over the full range of SVLIM.	hardware redesign D1 workaround: SVLIM = 31	D1
42	ADC Initialisation	Wrong initialisation of RGB ADCs after power-on causes color mismatch.	hardware redesign D1 workaround: <0xb0 0x37 0x00 0xe4>	D1
43	Clock Noise	Induced harmonics of the system clock generate visible interference on weak IF input signals.	hardware redesign D1	
46	HORPOS changes color multiplex	When picture is shifted to the right via HORPOS the color multiplex is inverted.	hardware redesign D1 workaround: HORPOS+HORWIDTH < 1287	D1
47	Preframe Generator	The preframe generator cannot produce full screen background color.	hardware redesign D1	D1

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No.	Problem	Description	Comment	OK
48	DRX AGC Hangup	If VAGC_REDUC>0 and positive signal jumps above top level, AGC hangup may occur and CVBS output level is reduced.	firmware redesign D1 workaround: KI_CHANGE_TH = 19 after standard change	D2
53	MSP Automatic Standard Detection	Automatic standard detection fails, if EIA-J is selected as preferred 4.5MHz-sound carrier.	firmware redesign D4 workaround: avoid Mod_4_5MHz[1:0]=[1,0]. If Mod_ASS and Mod_Dis_Std_Chg = 1, EIA-J is detected anyhow	D4
54	MSP Standard Toggle in HDEV-Mode fails	Toggling between Standard 3 and 8 while Mod_HDEV_A = 1 leads to occasional sound impairments	firmware redesign D4 workaround: not available	D4

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2. VCT 49xyI-F1

The VCT 49xyI-F1 is targeted to solve field and functional problems of the earlier VCT-I versions. For that purpose some new registers were implemented. In addition workarounds used for VCT-I versions prior to F1 may not be compatible.

The VCT 49xyI-F1 is pin-compatible to VCT 49xyI-D5.

Functional problems 50, 56, 57 and 58, 62, 64, 65, 66, 68, 69, 70, 71 have been solved. Problem 55 has been solved but requires software initialisation. Field problems FP01, FP02 and FP03 have been solved, FP06 and FP07 are still under inverstigation. New features F19 and F20 have been successfully implemented.

Table 2–1: New features of VCT 49xyI-F1:.

No.	Feature	Description	Ok
F19	Vertical Peaking	Additional mode for vertical peaking in 4H-combfilter allows switching between 2H and 1H peaking filter. See new register VPM in section 2.1.2.	F1
F20	Fastblank Output	The fastblank signal of the TVT display generator is availbale as output signal for LCD-Scaler applications. It can be programmed to the pin PWMV, P11 and P21.	F1

Table 2–2: Field problems of VCT 49xyI-F1:

No.	Problem	Description	Comment	Ok
FP06	VSP-AGC performance	Poor performance with some non standard signals	hardware redesign in F2	
FP07	Sync/H-PLL performance	Poor performance with some VCR tapes	hardware redesign in F2	

Table 2–3: Functional problems of VCT 49xyI-F1:

No.	Problem	Description	Comment	Ok
73	FM Radio not working	root causes: a) fast carrier recovery is automatically always ON, but should be OFF for FM-Radio mode b) When switching to FM-Radio mode the output frequency sometimes will not be set correctly	firmware redesign F2 workaround: s. 2.1.1.4. W3 & W4	F2
74	ITU656 Biterror	Bit errors on ITU656 output data produce noisy and unstable picture.	metal fix F1 no workaround available	

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2.1. Register Changes on VCT 49xyI-F1

2.1.1. DRX Part

The major improvement of the VCT 49xyI-F1 DRX-performance is based on the speed up of the Tuner-AGC, the Video AGC and the Carrier Recovery. While the faster Tuner and Video AGC help to improve significantly the Streaky Noise and Airplane Flutter issues, the extended Carrier Recovery removes all remaining field test matters. Although the fast modes are activated by default, some new registers are introduced to enable the configuration of the modified functions if necessary.

Table 2–4: New DRX Registers

Name	Sub	Addr	Dir	Reset	Range	Function
Advanced Settings						
MOD_ACCU_BS[9:0]	h10	h100E[10:1]	RW	0	-512..511	**Modulator imbalance value** Write:set manual imbalance value (with MOD_IF=0, MOD_IR=0, for take-over set MOD_UPDATE=1) Read:compensated imbalance value
MOD_UPDATE	h10	h100E[0]	W	0	0,1	**Update modulator imbalance** 1: write Modulator imbalance value into hardware
MOD_TH[3:0]	h10	h100F[11:8]	W	5	0..15	**Imbalance control threshold** Selects the edge sensitivity
MOD_MODE	h10	h100F[7]	W	1	0,1	**Imbalance Control estimation mode** 0: trigger estimation on rising edges 1: trigger estimation on rising and falling edges
MOD_If[3:0]	h10	h100F[6:3]	W	6	0..15	**Imbalance control integral part (falling)** The control uses this value for decreasing imbalance
MOD_Ir[2:0]	h10	h100F[2:0]	W	1	0..7	**Imbalance control integral part (rising)** The control uses this value for increasing imbalance
NOISE_BS[3:0]	h10	h1013[3:0]	W	15	0..15	**Maximum deviation for noise reduction**
PHAC_BP	h10	h1015[9]	W	0	0,1	**Phase correction bypass** 0: active phase correction 1: bypass phase correction
FAST_VAGC_EN	h10	h1023[8]	W	1	0,1	**Enable Fast VAGC** 0: Fast VAGC disabled 1: Fast VAGC enabled
COMP_DC_MUX[2:0]	h10	h10B3[11:9]	W	7	0..7	**Multiplexer for DC estimation during compensation** The reference signal is attenuated with the following filter H(z) = 0.5*(1+z^-(4+COMP_DC_MUX)) @fs=40.5MHz
COMP_FREQ_BS[8:0]	h10	h10B3[8:0]	W	93	0..511	**Increment for reference signal generation** 19.7kHz<fref<10.1MHz COMP_FREQ_BS = (fref*2048/40.5MHz)
Firmware						
BP_KI_MIN_BS[5:0]	h10	h10A5[5:0]	W	21	0..63	**Minimum KI setting** TAGC_KI and VAGC_KI will not be set below this values

2.1.1.1. Comments to the Tuner and Video-AGCs

The fast mode of the Video AGC is enabled by default and can be switched off by FAST_VAGC_EN = 0. Nevertheless, switching off this new AGC is not recommended.

In earlier versions the VAGC_KI and TAGC_KI values had to be continuously updated to prevent the adaptive KI control from setting them too low. In the new version a minimum limit register is implemented: BP_KI_MIN_BS allows to determine the minimum allowed KIs.

For example : BP_KI_MIN_BS = 0x15 means: TAGC_KI must not be lower than 2 and VAGC_KI must not be lower than 5.

BP_KI_MIN_BS is set to 0x15 by default. Should there be a need for further improving Streaky Noise, 0x16 or 0x17 can be user selected. With the new algorithm VAGC_KI = 6 or 7 are also stable settings and do not produce any stripes.

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All controller software workarounds used at former versions which write the KIs will no longer be needed and should be removed (see also next section).

2.1.1.2. Comments to the Carrier Recovery in Connection with NICAM Audio Performance

The speed up of the carrier recovery to optimize the performance at non standard RF signals (caused by FM modulation and modulator imbalance) is mainly based on a significant extension of the PLL-bandwith. However as a matter of principle any extension of the PLL bandwith increases the system noise sensitivity.

Since the NICAM audio system is basically highly sensitive to phase noise, the fast carrier recovery may reduce the NICAM sensitivity, depending on the RF-signal condition. To avoid any reduction of the NICAM sound quality it is recommended to switch off the carrier recovery speed up in case of NICAM reception setting the register PHAC_BP to 1 (see also section 2.1.1.4., WP5).

2.1.1.3. Status of VCT 49xyl-F1 and how to deal with currently used workarounds

The following table gives recommendations how to deal with workarounds used at C7/Dx:

No.	Problem	Countries	Workaround for C7 / Dx	Side-Effect	Status in F1	Recommendation for F1
FP1	Streaky Noise	Korea	T1-Coefficients for M/N Speed up DRX video AGC: - write VAGC_KI=5 every 20ms - write TAGC_KI=2 every 20ms	Could not solve problem completely	significantly improved	remove WA
FP2	Modulator Imbalance	Korea, China, Thailand, Brazil Vietnam	Adaptively (AFC_LOCK_QUAL): - CR_AMP_TH 16 -> 64	Reduced FM sound S/N	significantly improved	remove WA
FP3	FM Modulation	India, Pakistan, Korea	Adaptively (NLPFLD): - CLMPST1 28 -> 45 - CLMPD1 11-> 3 - CR_P 3-> 4	Could not solve problem completely	significantly improved	remove WA
	Flicker, Airplane Flutter RC: default AGC setting too slow	Asia, France, Czech	Speed up DRX video AGC: - write VAGC_KI=5 every 20ms - write TAGC_KI=2 every 20ms	SW code overhead adaptive functionality not usablex	significantly improved, previously forced values now default	remove WA

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No.	Problem	Countries	Workaround for C7 / Dx	Side-Effect	Status in F1	Recommen-dation for F1
	Hsync Distortion	Malaysia	Speed up DRX video AGC: - KI_CHANGE_TH=1 - VAGC_REDUC=1	none	previously forced val-ues now default	remove WA
	Color Sensitivity, bar edge distortion RC: default NOISE_BS=15 too high	India, Malaysia	Reduce NOISE_BS to 8 (partly adaptively when chroma level is small)	Measured Video S/N 1-2dB smaller	unchanged (0xF still default)	keep WA

2.1.1.4. Recommended Workarounds for VCT 49xyI-F1

Although the field problems have been fixed successfully, there are recommendations for specific input-signals.

Please consider the following table.

No.	Issue	Workaround for F1	Side-Effect	Plan for F2
W1	Imbalance control can cause prob-lems when changing from high to low RF signal levels	If TAGC_I = 0: - set MOD_Ir = 0 - set MOD_If = 0 - write MOD_ACCU_BS = 0 (consider also W2)	none	under inves-tigation
W2	MOD_ACCU_BS must be written several times until value is accepted	Write MOD_ACCU_BS until readback value matches written value (remember that MOD_UPDATE has to be 1 for writ-ing MOD_ACCU_BS)	none	firmware redesign
W3	FM radio not working; root cause: fast carrier recovery is automatically ON in FM radio mode, should be OFF	Set PHAC_PB to 1 in FM radio mode only, to 0 in TV modes	none	firmware redesign
W4	When switching to FM-Radio mode the output frequency sometimes will not be set correctly	Repeat switching to FM-Radio mode and subsequently read out AFC_DEV until the value is 0	none	firmware redesign
W5	Reduction of NICAM sensitivity at weak RF signal conditions	Set PHAC_PB to 1 in NICAM audio mode	none	under inves-tigation

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2.1.2. VSP Part

Table 2–5: New VSP Registers

Name	Sub	Dir	Sync	Reset	Range	Function
CD						
LPCDEL[2:0]	h07[2:0]	RW	VS_CD	0	-8..7	**Window Shift For Fine Error Calculation** 100: -4 clock cycles 000: no offset 011: +3 clock cycles
THRSEL[1:0]	h07[13:12]	RW	VS_CD	0	0,1,2,3	**H Slicing Level Threshold** 00: 50% 01: 31% 10: 37% 11: 25%
CVBSLPBW[1:0]	hB4[5:4]	RW	VS_CD	0	0..3	**CVBSLP Bandwidth** 00: very small 01: small 10: wide 11: very wide
CVBSFEBW[1:0]	hB4[3:2]	RW	VS_CD	0	0..3	**CVBSFE Bandwidth** 00: very small 01: small 10: wide 11: very wide
PDTHD[1:0]	hB4[1:0]	RW	VS_CD	0	0,1,2,3	**AGC Peak Dark Threshold** 00: 140 01: 124 10: 104 11: 70
MINVWIN	hB5[15]	RW	VS_CD	0	0,1	**Calculate MINV** 0: every line 1: over 4 lines Note: set to '0' for standard CVBS and '1' for component input
THRELIM	hB5[14]	RW	VS_CD	0	0,1	**Limit Threshold to MINV** 0: no limitation 1: limit
CETHD[1:0]	hB5[13:12]	RW	VS_CD	0	0,1,2,3	**Coarse Error Threshold** 00: +-255 01: +-192 10: +-160 11: +-128
THRELP[1:0]	hB5[11:10]	RW	VS_CD	0	0..3	**Lowpass Coeff for Threshold Value** 00: very strong 01: strong 10: weak 11: filter off
FECA[1:0]	hB5[4:3]	RW	VS_CD	0	0..3	**Fine Error Calculation** 00: normal syncs 01: short syncs 10: new algorithm 11: fine error disabled
PWREDLIM[2:0]	hB5[2:0]	RW	VS_CD	0	0..7	**Peak White Reduction Limit** 000: 63 001: 48 010: 32 011: 24 100: 16 101: 12 110: 8 111: 4
NSREDTHD[1:0]	hB6[1:0]	RW	VS_CD	0	0,1,2,3	**Noise Reduction Threshold** 00: 256 01: 384 10: 512 11: 640

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Table 2–5: New VSP Registers, continued

Name	Sub	Dir	Sync	Reset	Range	Function
COMB						
VPM	h1F[4]	RW	VS_COMB	0	0,1	**Vertical Peaking Mode** 0: 2H PAL, 1H NTSC (old mode) 1: 1H PAL, 2H NTSC (new mode)
MACROVISION						
MVRESULT[1:0]	h26[1:0]	R	VS_CD		0,1, 2, 3	**Macrovision Detection** 00: nothing present 01: AGC process present and colorstripe process not present 10: AGC process present and colorstripe process type 2 present 11: AGC process present and colorstripe process type 3 present
ITU						
ITUOUTSTR	h55[10]	RW	VS_ITU	0	0,1	**ITU656 Output Pad Strength** 0: normal 1: weak

Table 2–6: Extended VSP Registers

Name	Sub	Dir	Sync	Reset	Range	Function
CD						
AGCMD[1:0]	h0B[7:6]	RW	VS_CD	0	0,1,2,3	**AGC Method (ADC1)** 00: sync amplitude and peak white 01: sync amplitude only 10: **sync amplitude, peak white and peak dark** 11: fixed to value AGCADJ1
I2C						
REV[4:0]	hFC[4:0]	R			1,2,3,4,5, 6	**VCTH Revision** h01: VCTH-01-01 h02: VCTH-02-01 h03: VCTH-03-01 h04: VCTJ-01-01 h05: VCTJ-02-01 h06: VCTH-04-01

Table 2–7: Wrongly Documented VSP Registers

Name	Sub	Dir	Sync	Reset	Range	Function
ITU						
EN_656[1:0]	h50[1:0]	RW	VS_ITU	0	0,1,2,3	**Enable ITU656 Interface** 00: input & output disabled **01: output enabled** **10: input enabled** 11: input & output enabled

Table 2–8: Deleted VSP Registers

Sub	Data Bits																Reset
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
h20	LINELENH50[3:0]				LINELENH60[3:0]				REMDEL 2	REMDEL 1	INCOMB[1:0]				~~VCR DET HD~~	YCT-COMB	hC300
h21																~~TVM ODE~~	

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2.1.3. DPS Part

Table 2–9: New DPS Registers

Name	Sub	Dir	Sync	Reset	Range	Function
DEFL						
FBOUTEN	hD3[0]	RW	VS_DEFL	0	0,1	**FBOUT Enable at PWMV pin** 0: PWMV to Port Mux 1: FBOUT to Port Mux

Table 2–10: Undocumented DPS Registers (already available in Dx versions)

Name	Sub	Dir	Sync	Reset	Range	Function
LLPLL						
IICINCR[18:3]	h00[15:0]	RW	load_iicincr	32768	0..65535	**HDTO Increment High** controls center frequency of LLPLL clkhll = IICINCR* 648*10**6/1048576 beclk = clkhll / 8 16384: beclk = 1.27 MHz 174763: beclk = 13.5MHz 262144: beclk = 20.25 MHz 349525: beclk = 27MHz 524287: beclk = 40.5 MHz
IICINCR[2:0]	h01[2:0]	RW	load_iicincr	0	0..7	**HDTO Increment Low**
PPLIP[11:0]	h02[11:0]	RW		1296	0..4095	**Pixel per Line Input Processing** must be equal to PPLOP !!!
ODC						
PPLOP[11:0]	h17[11:0]	RW	upd_pplop	1296	0..4095	**Pixel Per Line Output** must be equal to PPLIP !!!
BLE						
MINRED	h3E[13]	RW	VS_DP	0	0,1	**Enable Entropy Adaption** 0: entropy adaption off 1: entropy adaption on
LUMAMIX						
LMIXMODE	h47[14]	RW	VS_DP	1	0,1	**Luminance Mixer Mode** 0: static mixer 1: amplitude adaptive mixer
LMIXCOF[5:0]	h47[13:8]	RW	VS_DP	0	0..63	**Luminance Mixer Coefficient** static mixer coefficient (used if LMIXMODE=0) 0: 100% peaking ... 63: 100% LTI
PIXMIX						
PATTSIZE	h60[11]	RW	VS_DP	1	0,1	**Test Pattern Size** 0: 720 pixel/line 1: 1080 pixel/line

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2.1.4. XDFP Part

Table 2–11: New XDFP Registers

Name	Sub	Dir	Sync	Reset	Range	Function
Measurement						
HVBLKDIS	hF2	h01C2[11]	RW	0	0,1	**Horizontal & Vertical Blanking Disable**
Analog RGB						
NEWCALIB	hF2	h01DE[11]	RW	1	0, 1	**New Calibration Method** for compatibility of different MSPH and VCTH versions 0: use old VCTH with new MSPH 1: any other combination

Table 2–12: Undocumented XDFP Registers (already available in Dx versions)

Name	Sub	Dir	Sync	Reset	Range	Function
Horizontal Deflection						
PER_MIN[10:0]	hF2	h0183[10:0]	RW	1140	0..2047	**HSync Period Minimum**
PER_MAX[10:0]	hF2	h0184[10:0]	RW	1426	0..2047	**HSync Period Maximum**

2.1.5. TVT Part

Table 2–13: Wrongly Documented TVT Registers

Name	Addr	Dir	Reset	Range	Function
RTC					
RTCRW	h8F[4]	RW	0	0,1	**RTC Read/Write**
RTCSUB[3:0]	h8F[3:0]	RW	0	0..15	**RTC Subaddress**
MEMORY					
INTSRC0	hE8[5]	RW	0	0,1	**Interrupt 0 Source** 0: Int0 is source 1: CRT is source
INTSRC1	hE8[4]	RW	0	0,1	**Interrupt 1 Source** 0: Int1 is source 1: CRT is source
PATCH	hE8[3]	RW	0	0,1	**Patch Modul** 0: enable 1: disable

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