# 5 CIRCUIT OPERATIONS

5.1. CONNECTION DIAGRAM
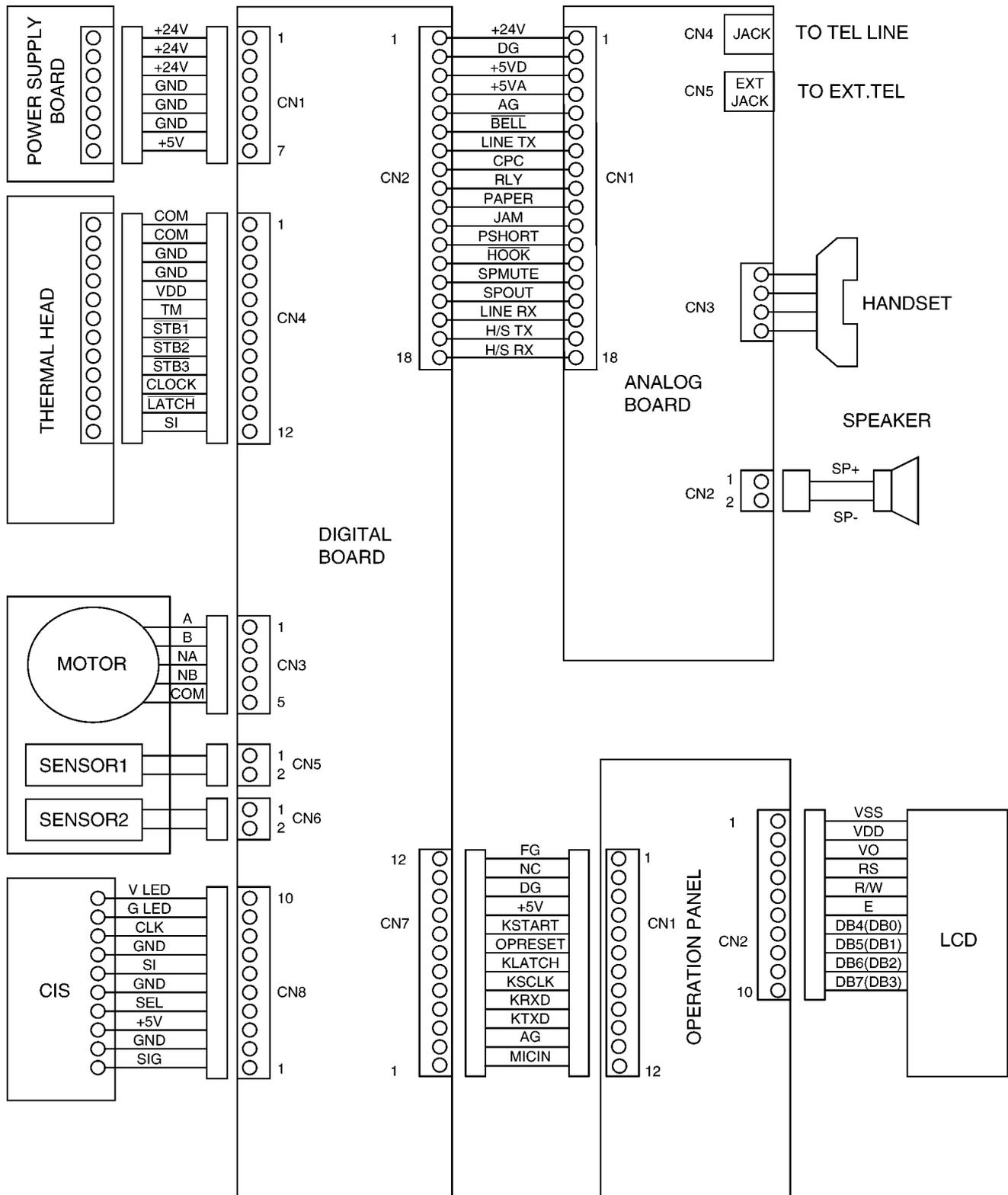
5.2. GENERAL BLOCK DIAGRAM

The control section will be explained as shown in the block diagram.

1. ASIC (IC1)

   Composed mainly of an address decoder, modem control section, CPU and RTC.

   Controls the general FAX operations.

   Controls the operation panel I/F.

   Controls the thermal head I/F and CIS I/F.

   Executes image processing.

   TAM monitor and the H/S volume.

   I/O ports

2. ROM (IC2)

   Contains all of the program instructions for unit operations.

3. Static RAM (IC4)

   This memory is used mainly for the parameter working storage area.

4. MODEM (IC5)

   Modem for the FAX.

5. Read Section

   Contact Image Sensor (CIS) to read transmitting documents.

6. Thermal Head

   Contains heating elements for dot matrix image printing.

7. Motor driver (IC8)

   Drives the motor.

8. Reset circuit (IC3)

   Detects voltage at 5V power source, outputs the signal, which provides the reset signal for each IC to IC1.

9. Analog board

   Composed of an ITS circuit and NCU circuit.

10. Sensor Section

    Composed of a document sensor, recording paper sensor, motor position sensors, read position sensor.

11. Power supply switching board section

    Supplies +5V and +24V to the unit.

12. FLASH MEMORY (IC6)

    Saves TAM voice data.

5.2.1. GENERAL BLOCK DIAGRAM
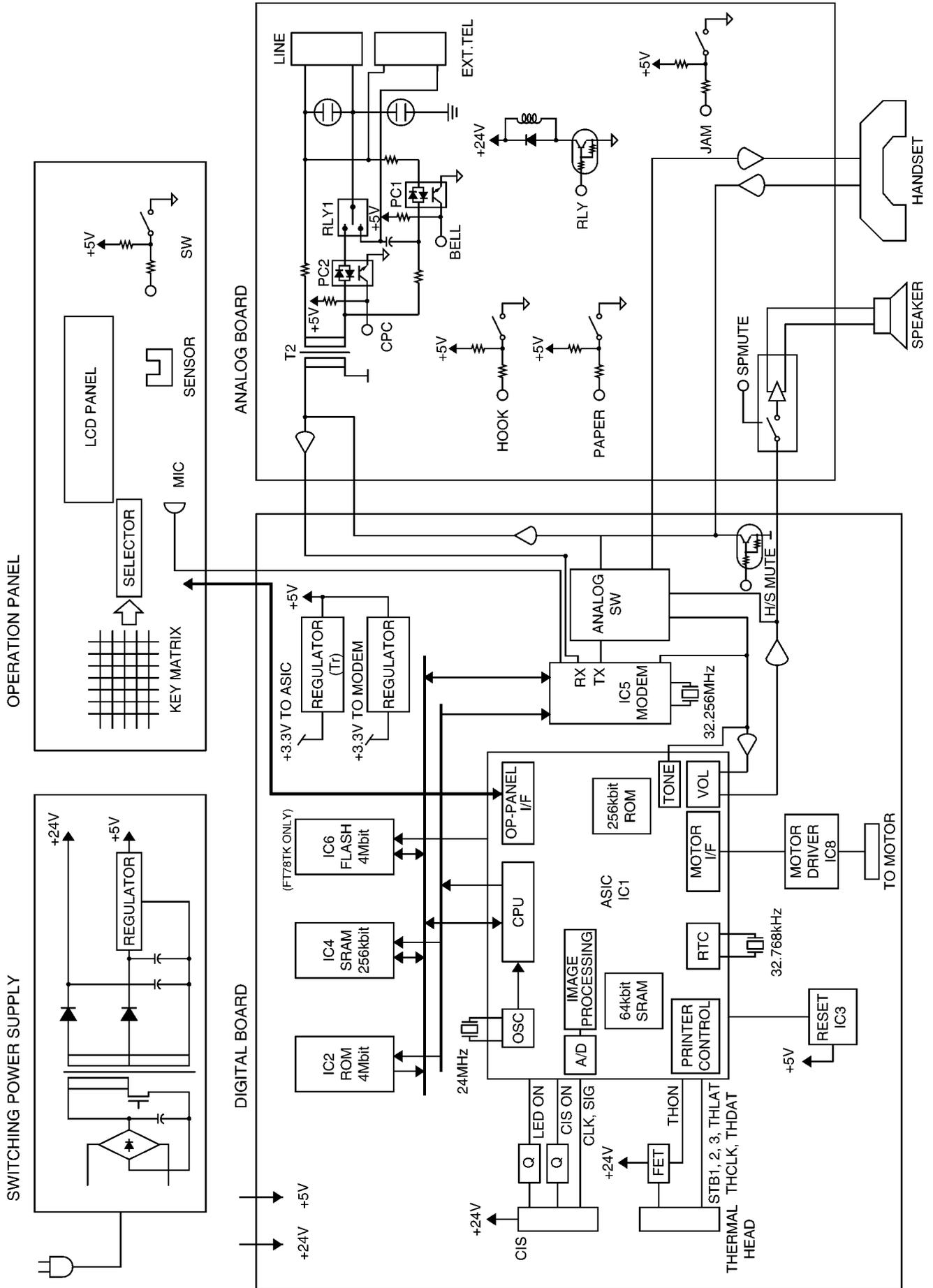
5.3. CONTROL SECTION

5.3.1. BLOCK DIAGRAM
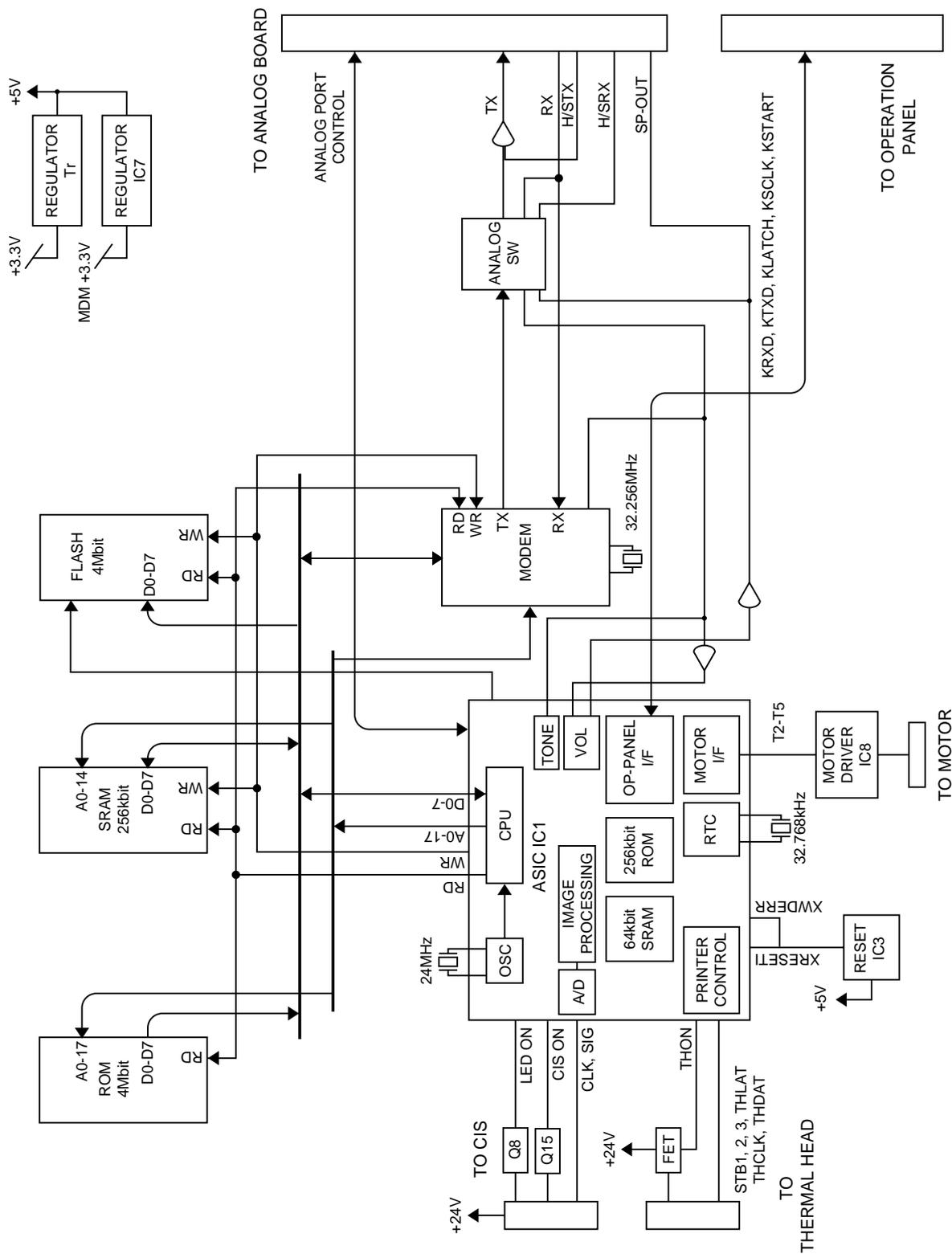
KX- FT78CE/HG-B DIGITAL BOARD: BLOCK DIAGRAM

5.3.2. ASIC (IC1)

This custom IC is used for general FAX operations.

1. CPU

   This model uses a Z80 equivalent CPU operating at 8MHz.
   Many of the peripheral functions are handled by custom designed LSIs. As a result, the CPU only needs to process the result.

2. RTC

   Real time clock.

3. DECODER

   Decodes the address.

4. ROM/RAM I/F

   Controls the SELECT signal of ROM or RAM and bank switching.

5. CIS I/F

   Controls document reading.

6. IMAGE DATA RAM

   This is inside the ASIC and has 8KB which is used for image processing.

7. THERMAL HEAD I/F

   Transmits the recorded data to the thermal head.

8. MOTOR I/F

   Controls the motor which feeds the document and feeds the reading document.

9. OPERATION PANEL I/F

   Control port for Operation Panel.

10. I/O PORT

    I/O Port Interface (for analog board port control).

11. ANALOG BLOCK

    Electronic volume for the handset and TAM monitor.
    Sends beep tones, etc.

Descriptions of Pin Distribution (IC1)

NO	SIGNAL	I/O	POWER SUPPLIED VOLTAGE	DESCRIPTION
1	AIN1	A	3.3V	CCD IMAGE SIGNAL INPUT
2	AIN2	A	3.3V	THERMISTOR TEMPERATURE WATCH INPUT
3	AIN3	A	3.3V	
4	AMON	A	3.3V	ANALOG SIGNAL MONITOR TERMINAL
5	VSSB		GND	POWER SOURCE (ANALOG GND)
6	VDDB		3.3V	POWER SOURCE (ANALOG 3.3V)
7	VDD(3.3V/B)		3.3V/BATT	POWER SOURCE (+3.3V/LITHIUM BATTERY)
8	X32OUT	O	3.3V/BATT	RTC (32.768KHz) CONNECTION
9	X32IN	I	3.3V/BATT	RTC (32.768KHz) CONNECTION
10	VSS		GND	GND
11	XBACEN	I	5V/BATT	BACKUP ENABLE
12	VDD(5V/B)		5V/BATT	POWER SOURCE (+5V/LITHIUM BATTERY)
13	XRAMCS	O	5V/BATT	RAM (IC4) CHIP SELECT
14	FTG	O	5V	SH SIGNAL OUTPUT FOR CIS (SI)
15	F1	O	5V	01SIGNAL OUTPUT FOR CIS(CLK)
16	F2/OP	O	5V	OUTPUT PORT (LED ON)
17	FR/OP	O	5V	ACK (DTMF RECEIVER CONTROL)
18	CPC	I	5V	INPUT PORT (CPC)
19	VDD(5V)		5V	POWER SOURCE (+5V)
20	VSS		5V	POWER SOURCE (GND)
21	RVN	I	5V	INPUT PORT (CISSEL)
22	IRDATXD/IOP	I	5V	INPUT PORT (JAM)
23	IRDARXD/IOP80	O	5V	OUTPUT PORT (H/S MUTE)
24	TXD/IOP	O	5V	OUTPUT PORT
25	RXD/IOP	O	5V	OUTPUT PORT (TELRXENB)
26	XRTS/IOP	O	5V	OUTPUT PORT (P-SHORT)
27	XCTS/IOP	O	5V	OUTPUT PORT (MDMTXENB)
28	MIDAT/IOP	O	5V	OUTPUT PORT (TONE1ENB)

NO	SIGNAL	I/O	POWER SUPPLIED VOLTAGE	DESCRIPTION
29	MICLK/IOP	O	5V	OUTPUT PORT (TONE2ENB)
30	TONE1	A	5V	TONE OUTPUT
31	TONE2	A	5V	TONE OUTPUT
32	VOLUREF	A	5V	ANALOG REF VOLTAGE
33	VOLUOUT	A	5V	VOLUME OUTPUT
34	VOLUIN	A	5V	VOLUME INPUT
35	MILAT/IOP	O	5V	OUTPUT PORT (H/S RXENB)
36	XNMI	I	5V	HIGH FIXED
37	FMEMDO/IOP	O	5V	ALE (FLASH MEMORY CONTROL)
38	FMEMDI/IOP	O	5V	FLASH MEMORY (IC6) CHIP SELECT
39	FMEMCLK/IOP	I	5V	INPUT PORT (BELL) R/B (FLASH MEMORY CONTROL)
40	VSS		GND	POWER SOURCE (GND)
41	VDD(5V)		5V	POWER SOURCE (+5V)
42	20KOSC/IOP	O	5V	CLE (FLASH MEMORY CONTROL)
43	XWAIT	I	5V	INPUT PORT (HOOK)
44	HSTRD/IOP	O	5V	FRD (FLASH MEMORY RD)
45	HSTWR/IOP	O	5V	FWR (FLASH MEMORY WR)
46	XOPRBE	O	5V	OUTPUT PORT (SP-MUTE)
47	ADR15	O	5V	CPU ADDRESS BUS 15 (NOT USED)
48	ADR14	O	5V	CPU ADDRESS BUS 14 (NOT USED)
49	ADR13	O	5V	CPU ADDRESS BUS 13 (NOT USED)
50	VDD(3.3V)		3.3V	POWER SOURCE (+3.3V)
51	XOUT	O	3.3V	SYSTEM CLOCK (24MHz)
52	XIN	I	3.3V	SYSTEM CLOCK (24MHz)
53	VSS		GND	POWER SOURCE (GND)
54	VDD(5V)		5V	POWER SOURCE (+5V)
55	XTEST	O	5V	24MHz CLOCK
56	TEST1	I	5V	HIGH FIXED
57	TEST2	I	5V	HIGH FIXED
58	TEST3	I	5V	HIGH FIXED
59	TEST4	I	5V	HIGH FIXED
60	XMDMINT	I	5V	MODEM INTERRUPT
61	XMDMCS	O	5V	MODEM (IC5) CHIP SELECT
62	VSS		GND	POWER SOURCE (GND)
63	VDD(3.3V)		3.3V	POWER SOURCE (+3.3V)
64	XRAS/IOP	O	5V	MODEM RESET
65	XCAS1/IOP	O	5V	SD (Serial Data from DTMF Receiver)
66	XCAS2/IOP	I	5V	INPUT PORT (BELL)
67	XRESCS2	O	5V	OPRESET
68	DB3	I/O	5V	CPU DATA BUS 3
69	DB2	I/O	5V	CPU DATA BUS 2
70	DB4	I/O	5V	CPU DATA BUS 4
71	DB1	I/O	5V	CPU DATA BUS 1
72	DB5	I/O	5V	CPU DATA BUS 5
73	DB0	I/O	5V	CPU DATA BUS 0
74	DB6	I/O	5V	CPU DATA BUS 6
75	VSS		GND	POWER SOURCE (GND)
76	VDD (3.3V)		3.3V	POWER SOURCE (+3.3V)
77	DB7	I/O	5V	CPU DATA BUS 7
78	XROMCS	I/O	5V	ROM (IC2) CHIP SELECT
79	RD	O	5V	CPU RD
80	WR	O	5V	CPU WR
81	VSS		GND	POWER SOURCE (GND)
82	VDD (5V)		5V	POWER SOURCE (+5V)
83	ADR0	O	5V	CPU ADDRESS BUS 0
84	ADR1	O	5V	CPU ADDRESS BUS 1
85	ADR2	O	5V	CPU ADDRESS BUS 2
86	ADR3	O	5V	CPU ADDRESS BUS 3
87	ADR4	O	5V	CPU ADDRESS BUS 4
88	ADR5	O	5V	CPU ADDRESS BUS 5
89	ADR6	O	5V	CPU ADDRESS BUS 6
90	ADR7	O	5V	CPU ADDRESS BUS 7
91	ADR8	O	5V	CPU ADDRESS BUS 8
92	ADR9	O	5V	CPU ADDRESS 9
93	ADR10	O	5V	CPU ADDRESS 10

NO	SIGNAL	I/O	POWER SUPPLIED VOLTAGE	DESCRIPTION
94	ADR11	O	5V	CPU ADDRESS 11
95	ADR12	O	5V	CPU ADDRESS 12
96	VSS		GND	POWER SOURCE (GND)
97	VDD (5V)		5V	POWER SOURCE (+5V)
98	RBA0	O	5V	ROM/RAM BANK ADDRESS 0
99	RBA1	O	5V	ROM/RAM BANK ADDRESS 1
100	RBA2	O	5V	ROM/RAM BANK ADDRESS 2
101	RBA3	O	5V	ROM/RAM BANK ADDRESS 3
102	RBA4	O	5V	ROM/RAM BANK ADDRESS 4
103	RBA5	O	5V	ROM/RAM BANK ADDRESS 5
104	RBA6/IOP96	I	5V	INPUT PORT (PAPER)
105	STB1	O	5V	STROBE SIGNAL OUTPUT TO THERMAL HEAD
106	STB2	O	5V	STROBE SIGNAL OUTPUT TO THERMAL HEAD
107	STB3	O	5V	STROBE SIGNAL OUTPUT TO THERMAL HEAD
108	XRESET	I	5V	RESET INPUT
109	XORESET	O	5V	RESET OUTPUT
110	VDD (5V)		5V	POWER SOURCE (+5V)
111	VSS		GND	POWER SOURCE (GND)
112	XRESET1	I	5V	RESET INPUT
113	WDERR	O	5V	WATCHED ERROR OUTPUT SIGNAL
114	THDAT	O	5V	RECORDED IMAGE OUTPUT
115	THCLK	O	5V	CLOCK OUTPUT FOR DATA TRANSFER
116	VDD (3.3V)		3.3V	POWER SOURCE (3.3V)
117	VSS		GND	POWER SOURCE (GND)
118	THLAT	O	5V	PULSE OUTPUT FOR DATA LATCH
119	STBNP	I	5V	INPUT PORT (MOTOR POS.)
120	RM0/IOP	O	5V	MOTOR CONTROL (D)
121	RM1/IOP	O	5V	MOTOR CONTROL (C)
122	RM2/IOP	O	5V	MOTOR CONTROL (B)
123	RM3/IOP	O	5V	MOTOR CONTROL (A)
124	RXE/IOP	O	5V	MOTOR ENABLE SIGNAL
125	TMO	O	5V	OUTPUT PORT (THON)
126	VDD (5V)		5V	POWER SOURCE (+5V)
127	VSS		GND	POWER SOURCE (GND)
128	TM1/IOP	I	5V	OUTPUT PORT
129	TM2/IOP	I	5V	INPUT PORT (CIS ON)
130	TM3/IOP	O	5V	OUTPUT PORT (RLY)
131	TXE/IOP	I	5V	INPUT PORT (CUT. POS.)
132	KSTART	O	5V	OPERATION PANEL CONTROL
133	KLATCH	O	5V	OPERATION PANEL CONTROL
134	KSCLK	O	5V	OPERATION PANEL CONTROL
135	KTXD	O	5V	OPERATION PANEL CONTROL
136	KRXD	I	5V	OPERATION PANEL CONTROL
137	ADSEL1	O	5V	CHANNEL SELECT SIGNAL FOR AIN2
138	VSSC		GND	POWER SOURCE (ANALOG GND)
139	VDDC		3.3V	POWER SOURCE (ANALOG +3.3V)
140	VSSA		GND	POWER SOURCE (ANALOG GND)
141	VDDA		3.3V	POWER SOURCE (ANALOG +3.3V)
142	VREFB	A	3.3V	A/D CONVERTER´S ZERO STANDARD VOLTAGE OUTPUT
143	VCL	A	3.3V	ANALOG PART STANDARD VOLTAGE SIGNAL
144	VREFT	A	3.3V	A/D CONVERTER´S FULL SCALE VOLTAGE OUTPUT

5.3.3. ROM (IC2)

This 512 KB ROM (OTPROM or MASKROM) has 32 KB of common area and bank area (BK4~BK 63).
 The capacity of each bank is 8 KB.
The addresses of the common area are from 0000H to 7FFFH, and addresses 8000H to 9FFFH are for the bank area.

5.3.4. RAM (IC4)

This 32 KB RAM has 8 KB of common area and bank area (BK0, BK1).
 The capacity of each bank is 12 KB.
 The addresses of the common area are from D000H to EFFFH, and addresses A000H to CFFFH are for the bank area.

5.3.5. RESET CIRCUIT

The output from pin 1 of the Reset IC (IC3) resets the gate array (IC1).

1. During a power surge, a positive reset pulse of 50 msec or more is generated and the system is reset completely.
   This is done to prevent partial resetting and system runaway during a power fluctuation.

Timing Chart
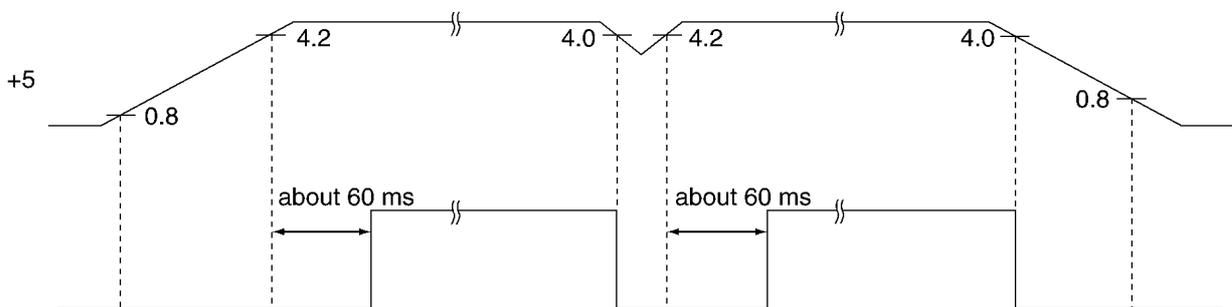
2. When pin 1 of IC3 becomes low, it will prohibit the RAM (IC4) from changing data.
   The RAM (IC4) will go into the backup mode, when it is backed up by a lithium battery.

Circuit Diagram
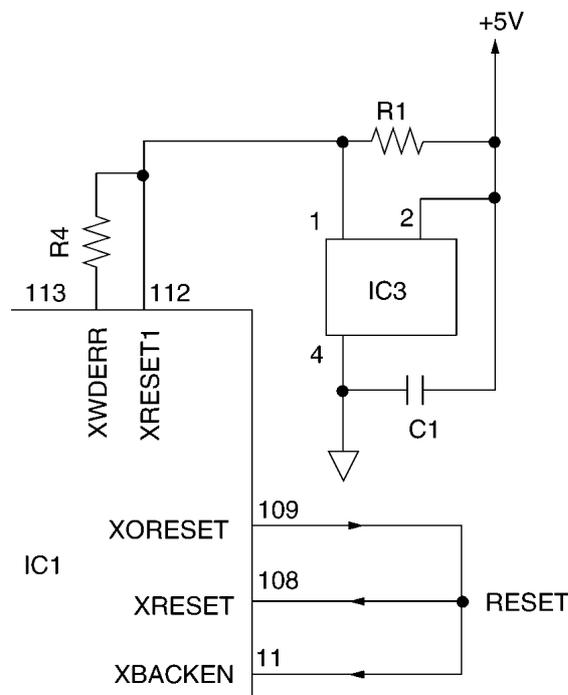
3. The watch dog timer, built-in the gate array (IC1), is initialized about every 1.5 ms.
   When a watch dog error occurs, pin 113 of the gate array (IC1) becomes low.
   The terminal of the WDERR signal is connected to the reset line so the WDERR signal works as the reset signal.

5.3.6. SRAM and RTC BACK UP CIRCUIT

1. **Function**

This unit has a lithium battery (BAT1) which works for the RAM (IC4) and Real Time Clock (RTC, Integrated into ASIC:IC1).
The user parameter for auto dial numbers, the transmission ID, the system setup date and so on are stored in the RAM (IC4).
The RTC continues functioning, even when the power switch is OFF, backed up by a lithium battery.

2. **Circuit Operation**

When the power is turned ON, power is supplied RAM (IC4) and RTC (IC1).
At this time, the voltage at pin 28 of RAM is +5V and pin 7 of RTC (IC1) is +3.3V. When the power is turned OFF, the battery supplies the power to RAM and RTC through J1, R24, D1 or DA1. At that time, the voltage at pin 28 of RAM and pin 7 of IC1 are about +2.5V. When the power is OFF and the +5V and +3.3V voltages decrease, IC3 detects them and LOW is input to pin 112 of IC1. Pin 109 of IC1 outputs the reset signals. Pin 28 of RAM (IC4) and pin 11 of IC1 become low, then RAM and RTC (IC1) go into the back up mode, when the power consumption is lower.

Circuit Diagram
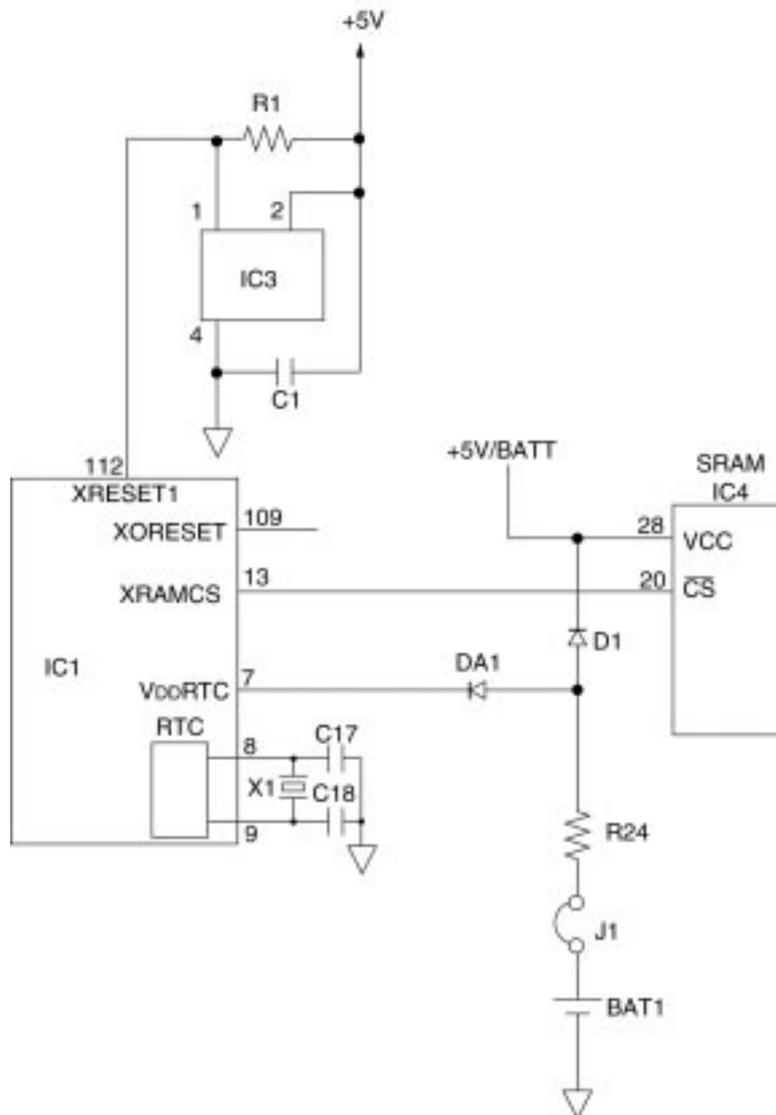
5.3.7. SUPERVISION CIRCUIT FOR THE THERMAL HEAD TEMPERATURE

1. **Function**

The thermistor changes the resistor according to the temperature and uses the thermistor´s characteristics.
The output of pin 137 of IC1 becomes a low level.
Then when it becomes a high level, it triggers point (A).
In point (C), according to the voltage output time, the thermal head´s temperature is detected.

After the thermal head temperature is converted to voltage in (B), it is then changed to digital data in the A/D converter inside IC1. The CPU decides the strobe width of the thermal head according to this value. Therefore, this circuit can keep the thermal head at an even temperature in order to stabilize the printing density and prevent the head from being overheated.

Circuit Diagram
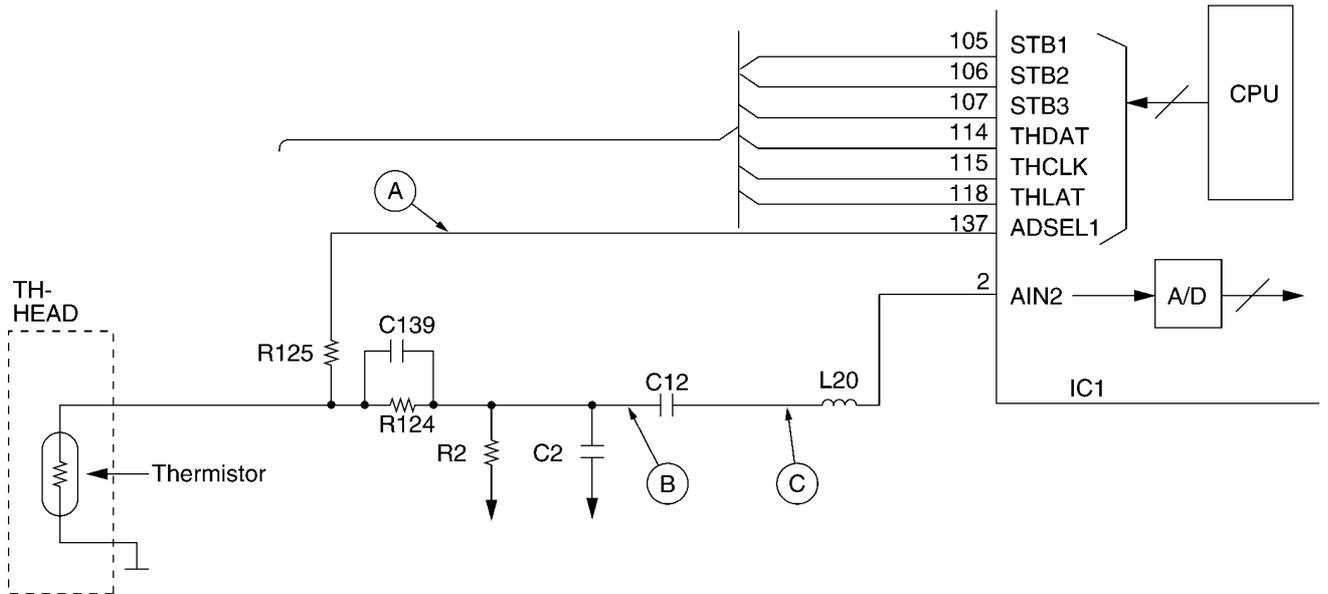
Timing Chart
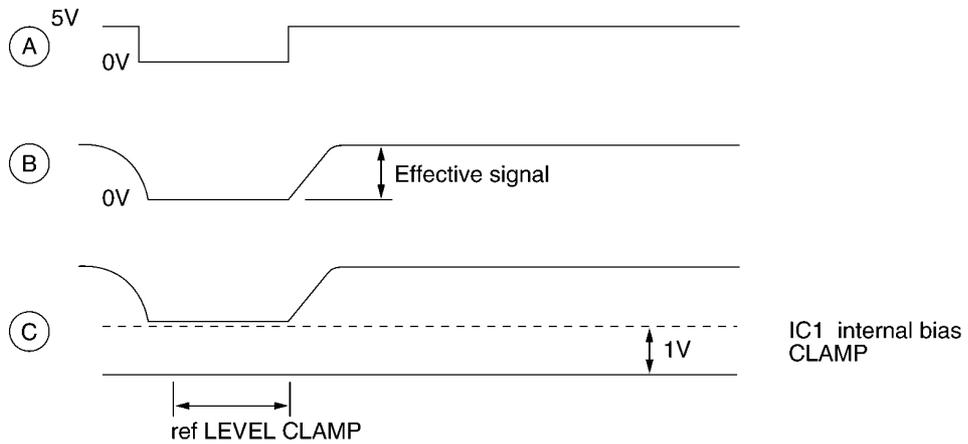
5.3.8. LED ARRAY(CIS)

The LED ARRAY will light during transmission and copying as a light source to recognize document characters, patterns, or graphics on a document.

It is also possible to light the LED ARRAY in the test mode.

Circuit Diagram
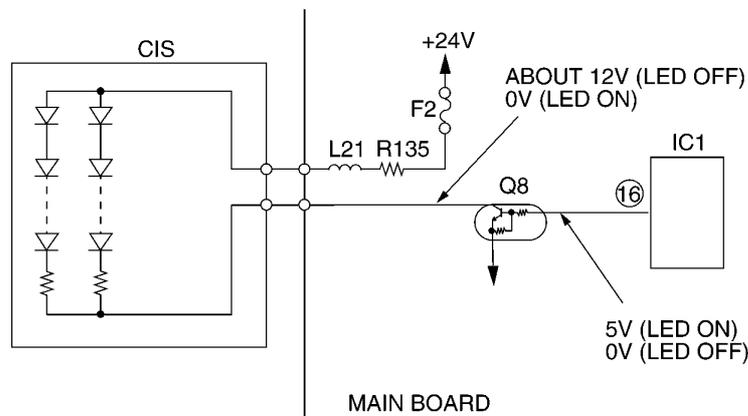
5.4. FACSIMILE SECTION

5.4.1. IMAGE DATA FLOW DURING FACSIMILE OPERATION

COPY (Fine, Super-Fine, photo)

1. Line information is read by CIS, via route (1), and is input to IC1.

2. In IC1, the data is adjusted to a suitable level for A/D conversion in the Analog Signal Processing Section, and via route (2) it is input to A/D conversion (8 bit). After finishing A/D conversion, the data is input to the Image Processing Section via route (3). Then via routes (4) and (5), it is stored in RAM as shading data.

3. The draft´s information that is read by CIS is input to IC1 via route (1). After it is adjusted to a suitable level for A/D conversion via route (2), the draft´s information is converted to A/D (8 bit), and it is input to the Image Processing Section. The other side, the shading data which flows from RAM via routes (6) and (7), is input to the Image Processing Section. After finishing the draft´s information image processing, white is regarded as "0" and black is regarded as "1". Then via routes (4) and (5), they are stored in RAM.

4. The white/black data stored as above is input to the P/S converter via routes (6) and (8). The white/black data converted to serial data in the P/S converter is input to the Thermal Head via route (9) and is printed out on recording paper.

   Note:

   Standard: Reads 3.85 times/mm

   Fine: Reads 7.7 times/mm

   Super-Fine: Reads 15.4 times/mm

Transmission

1. Same processing as COPY items 1) - 3).

2. The data stored in RAM of IC1 is output from IC1 via routes (6) and (10), and is stored in the system bus. Via route (11), it is stored in the communication buffer inside RAM (IC4).

3. While fetching data stored in the communication buffer synchronous with the modem, the CPU inputs data to the modem along route (12). It is converted to serial analog data and forwarded over telephone lines via the NCU Section.

Reception

1. The serial analog image data is received over telephone lines and input to the modem IC (IC5) via the NCU section, where it is demodulated to parallel digital data. The balance data is sent to the modem. Then the CPU stores the data in the communication buffer of RAM (IC4) along route (11).

2. The data stored in RAM (IC4) is decoded by the CPU via route (12), and is stored in RAM by routes (13) and (5).

3. Same processing as **COPY** item 4).

5.4.2. BLOCK DIAGRAM

SYSTEM
BUS

IC1

A/D

② ① CONTACT
IMAGE
SENSOR

③

ANALOG
SIGNAL

PROCESSING
SECTION

IC4

RAM

⑫
⑪

IMAGE
PROCESSING
SECTION

IC2

ROM

CPU

⑦ ④

⑬

⑤

RAM

⑩

⑥

⑧

IC5

MODEM

P/S
CONVERTER

THERMAL
HEAD

⑨

NCU

TEL.LINE
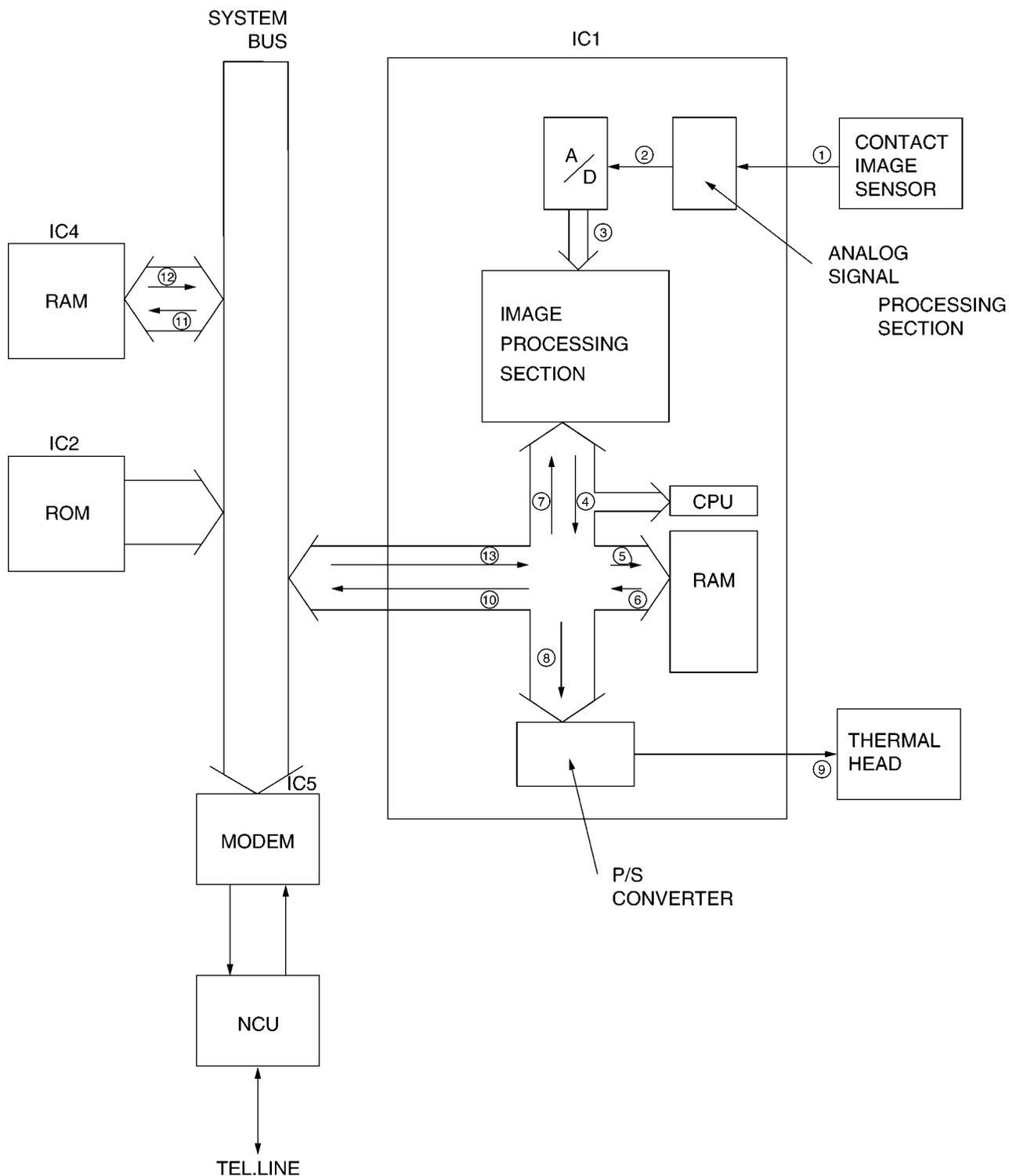
5.4.3. THERMAL HEAD

1. **Function**

This unit utilizes state of the art thermal printer technology.

The recording paper (roll paper) is chemically processed. When the thermal head contacts this paper it emits heat momentarily, and black dots (appearing like points) are printed on the paper. If this continues, letters and/or diagrams appear, and the original document is reproduced.

COMPOSITION OF THE RECEIVE RECORD SECTION (THERMAL RECORDING FORMAT)
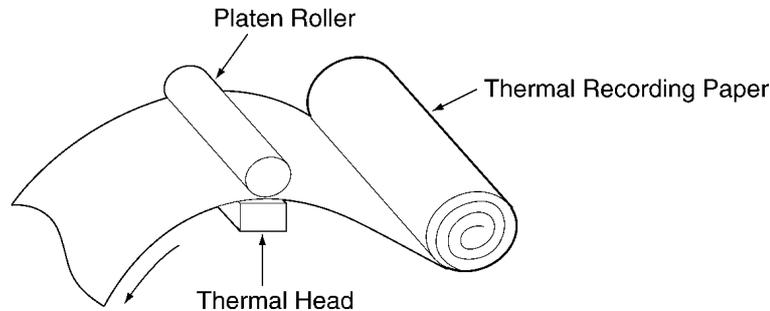
2. **Circuit Operation**

There are 27 driver ICs aligned horizontally on the thermal head and each one of these ICs can drive 64 heat emitting registers. This means that one line is at a density of 64×27=1728 dots=(8 dots/mm).

White/Black (white=0, black=1) data in one line increments is synchronized at IC1 pin 115 (THCLK), and sent from IC1 pin 114 (THDAT) to the shift register of the ICs. The shift registers of the 27 ICs are connected in series, and upon the shift of dot increment 1728, all the shift registers become filled with data, and a latch pulse is emitted to each IC from IC1 pin 118 (THLAT).With this latch pulse, all the contents of the shift registers are latched to the latch registers. Thereafter, through the addition of strobes from the IC1 pins (105 - 107) only black dot locations (=1) among latched data activates the driver, and the current passes to heat the emitting body causing heat emission.

Here, the three line strobes, STB1 to STB3, impress at intervals of 9.216 msec, as required for one-line printout.

The sequence is shown on the next page. [Moreover, for the strobe width, the thermistor value inside the thermal head is detected according to IC1 pin 2. (See **BLOCK DIAGRAM** (P.113).) Depending on that value, the strobe width is recorded in ROM (IC2).

Accordingly, the strobe width is determined.

When the thermal head is not used, the IC1 (125, THON) becomes low, Q9 turns OFF, Q12 turns OFF, and the +24 V power supply for the thermal head driver is not impressed to protect the IC.

Circuit Diagram
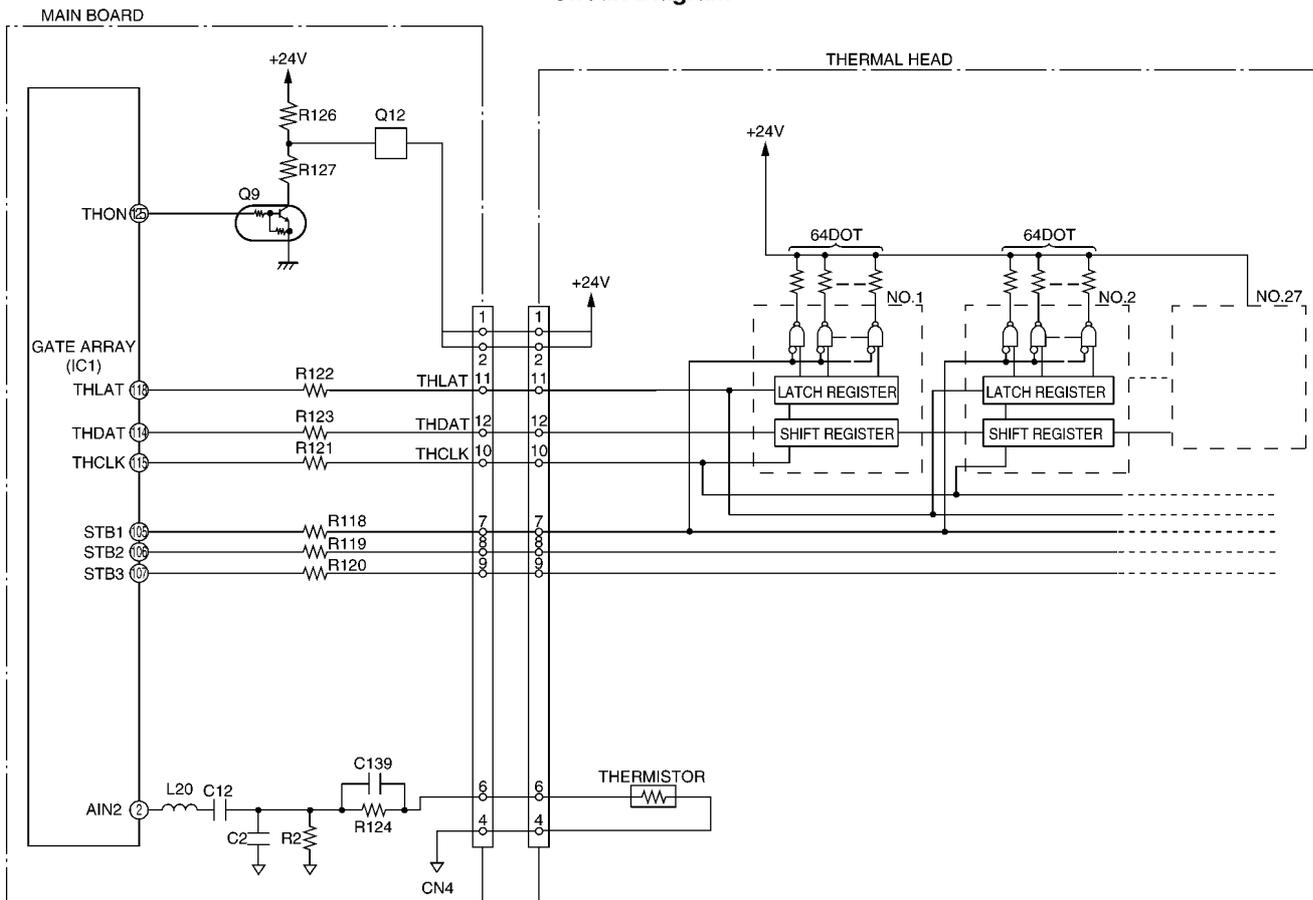
Timing Chart
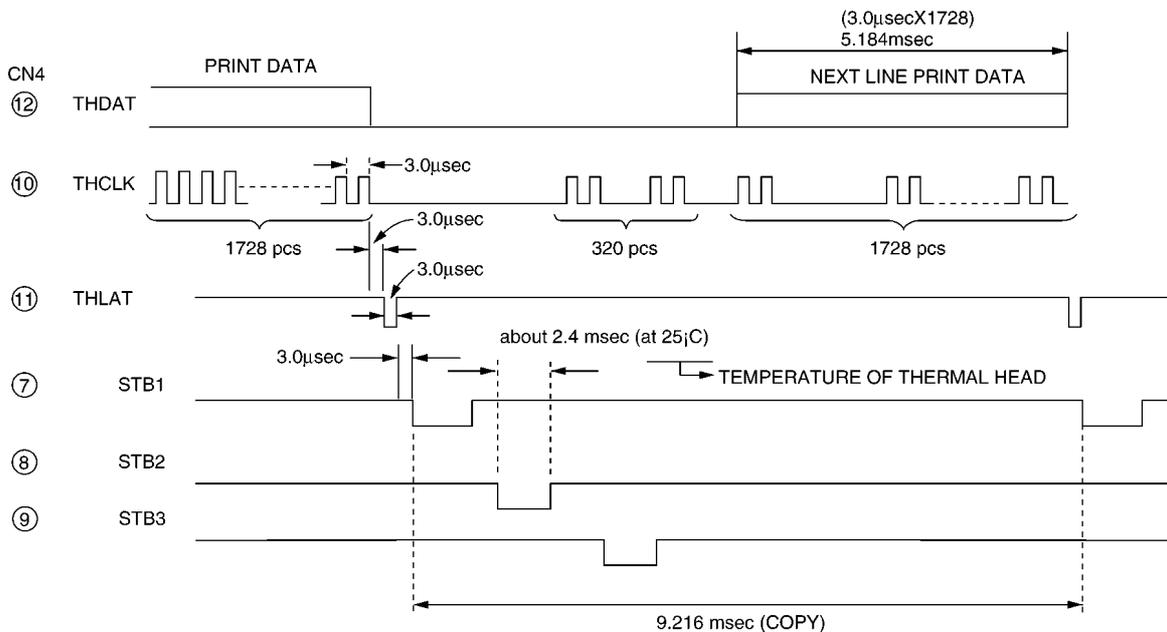
5.4.4. SCANNING BLOCK

The scanning block of this device consists of a control circuit and a contact image sensor made up of a celfoc lens array, an LED array, and photoelectric conversion elements.

Circuit Diagram
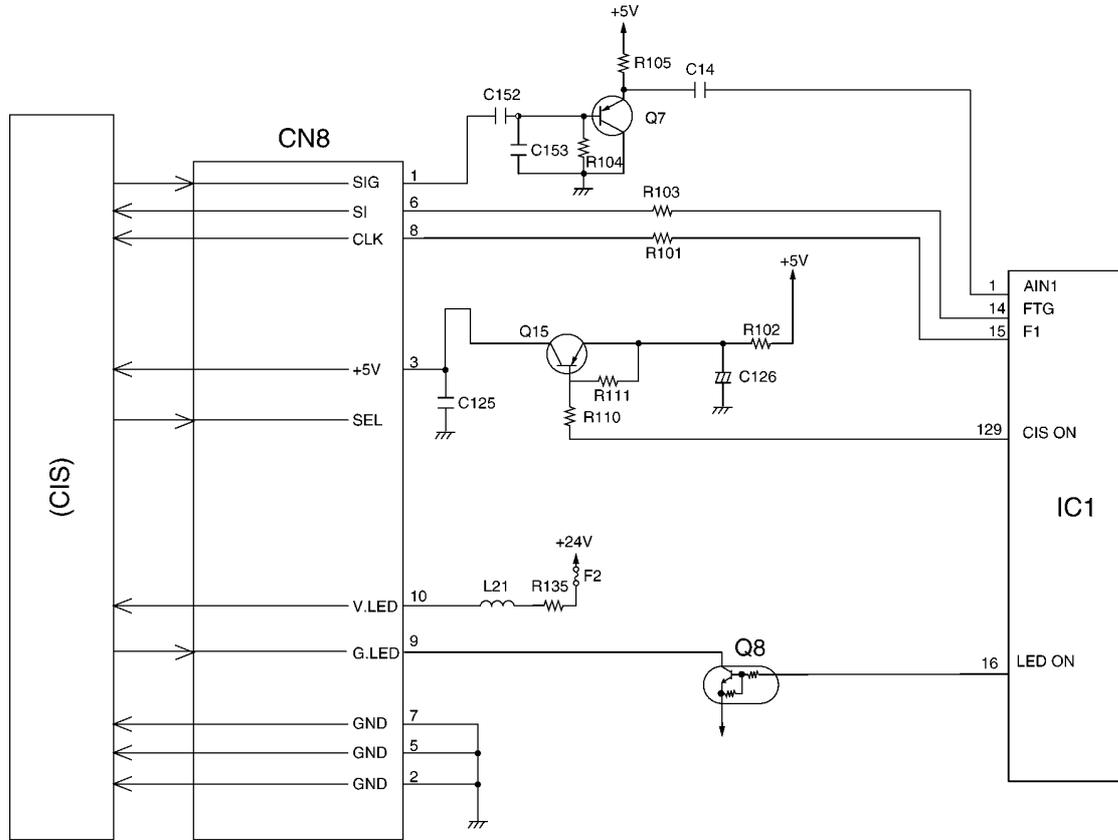
When an original is inserted and the start button pressed, pin 16 of IC1 goes to a high level and the transistor Q8 turns on and pin 129 of IC1 goes to a low level and the transister Q15 turns on. This applies voltage to the LED array to light it and the voltage (+5v) of CIS turns on. The contact image sensor is driven by each of the FTG-F1 signals output from IC1, and the original image illuminated by the LED array undergoes photoelectric conversion to output an analog image signal. The analog image signal is input to the system LSI (IC1) on AIN1 (pin 1 of IC1) and converted into 8-bit data by the A/D converter inside IC1. Then this signal undergoes digital processing in order to obtain a high-quality image.

5.4.5. STEPPING MOTOR DRIVE CIRCUIT

1. **Function**

   One individual stepping motor is used for transmission and reception. It feeds the document or recording paper synchronized for reading or printing.

2. **Circuit Operation**

   During motor drive, gate array IC1 pin 124 becomes a high level, and Q11 and Q10 go ON as a result. +24 V is supplied to the motor coil.

   Stepping pulses are output from gate array IC1, causing driver IC8 to go ON. The motor coil is energized sequentially in 2 phase increments or 1-2 phase increments, which causes a 1-step rotation. A 1-step rotation is 0.13mm of recording paper or document paper. The timing chart is below.

Timing chart (2 Phase)   1-2. Phase (Asic T2-T5, output)
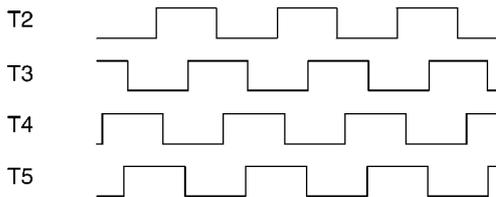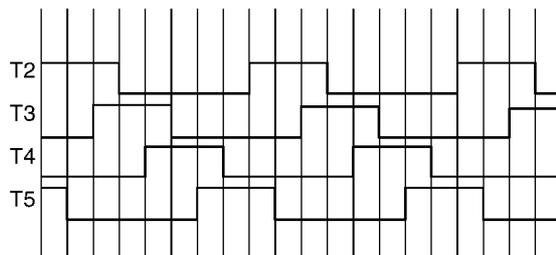
Stepping Motor Phase Pattern

Function	Mode	Phase Pattern	Speed
Copy	Fine/Half Tone	1-2	432 pps
	Super Fine	1-2	216 pps
FAX	STD	2	432 pps
	Fine/Half Tone	1-2	432 pps
	Super Fine	1-2	216 pps
————	Paper Feed	2	432 pps

Circuit Diagram
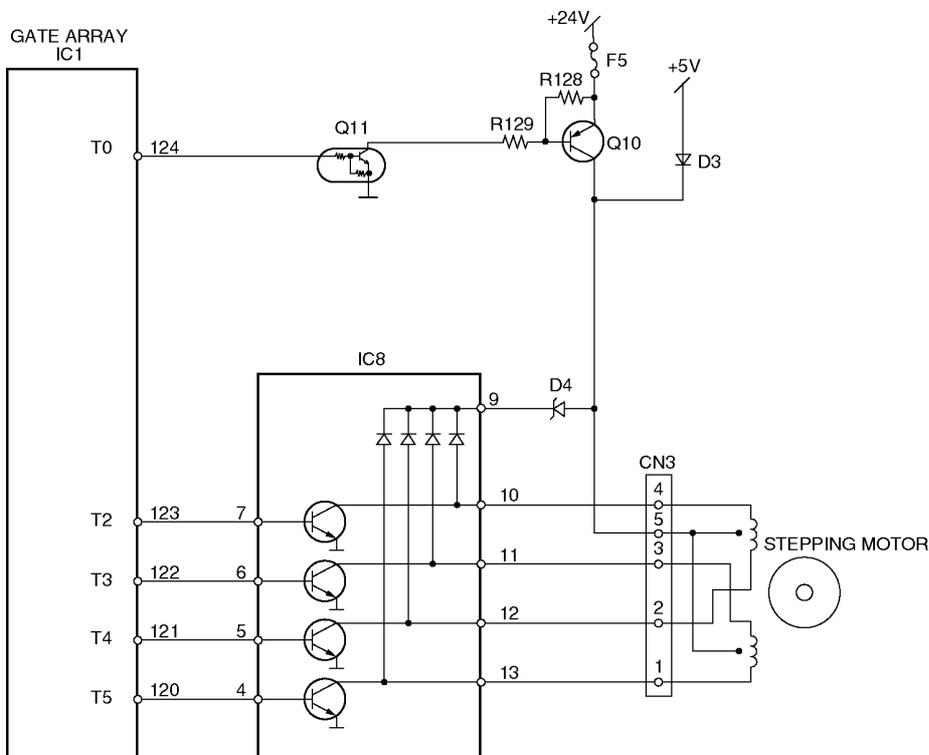
When the motor is OFF, gate array IC1 pin 124 becomes a low level and Q11 and Q10 also turns OFF. Instead of +24V, +5V is supplied through D3 so that the motor is held in place.

5.4.6. GEAR SECTION

This section shows how the motor-driven gear mechanism works in the main operations: FAX transmission, FAX reception the motor and copying.

5.4.6.1. MODE SELECTION

When the motor attached to the Drive Motor Gear rotates counterclockwise (CCW), Swing Gear A engages the CAM and the CAM turns counterclockwise to select a mode. (See **Fig. A**.) There are three mode options controlled by the Switch: **A**: Transmit mode, **B**: Receive mode and **C**: Copy mode. In **Fig. B**, you can see which mode is selected by the position of the rib in the CAM.
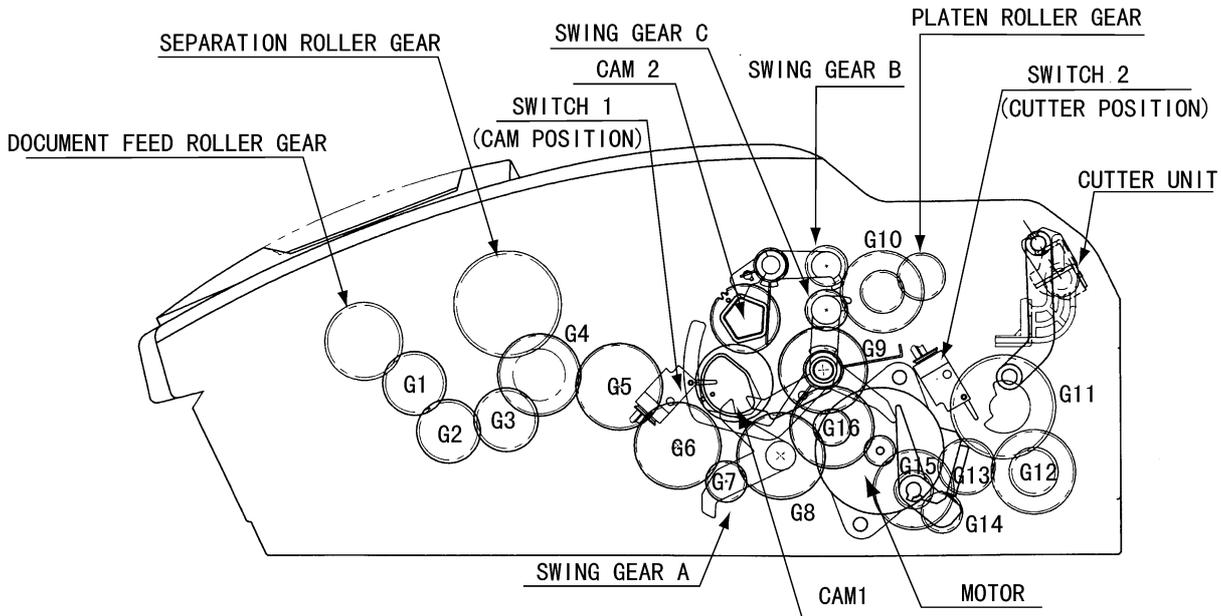

Fig. A [The operation is in the Transmit mode (a)]

COPY MODE   RECEIVE MODE   REVERSE MODE   CUTTER MODE   TRANSMIT MODE
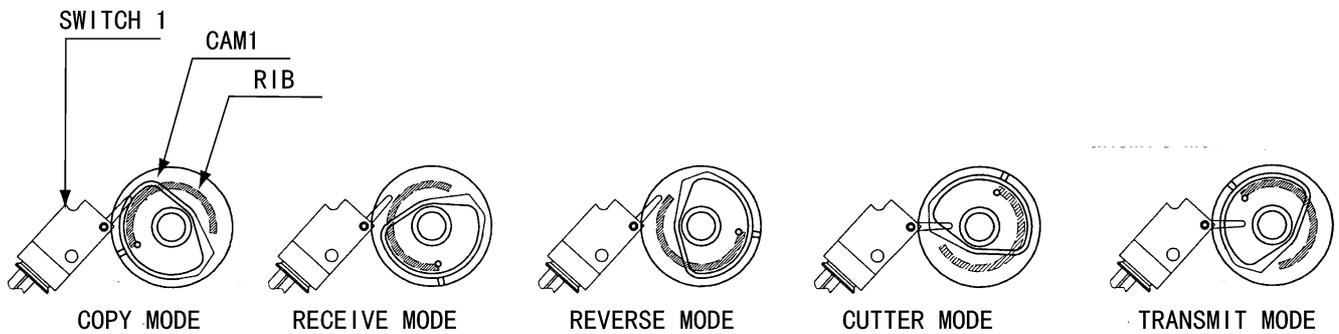
Fig. B

5.4.6.2. MODE OPERATION

Once a mode is selected, the Drive Motor Gear rotates clockwise (CW) and then the Swing Gear A-1 controls the mode operation.

A: Transmit mode

Swing Gear A-1 engages G6 and conveys its drive power to the Separation Roller Gear for pre-feeding documents.

B: Receive mode

Swing Gear B engages G8 and conveys its drive power to the Platen Roller Gear for printing the received data.

C: Copy mode

Swing Gear A-1 and B engage Gears 6 and 8 respectively and drive both the Separation Roller Gear and the Platen Roller Gear for feeding documents and recording paper in the copying operation.

5.4.6.3. MECHANICAL MOVEMENTS IN THE MAIN OPERATIONS

5.4.6.3.1. IDLE STATUS

5.4.6.3.2. SCANNING

```
┌─────────────────────────────────┐
│ When the document is set in the │  NO
│ paper tray, does the Document   │ ─────►  See 2.3.11. SENSOR SECTION
│ Sensor (PS1) turn ON ?          │
└─────────────────────────────────┘
              │ YES
              ▼
┌─────────────────────────────────┐
│ The motor rotates CW and the    │
│ document is pre-fed.            │
└─────────────────────────────────┘
              │
              ▼
┌─────────────────────────────────┐
│ Press the dial key.            │
└─────────────────────────────────┘
              │
              ▼
┌─────────────────────────────────┐
│ Press the start key.           │
└─────────────────────────────────┘
              │
              ▼
┌─────────────────────────────────┐
│ Does the motor rotate CW and    │  NO
│ is the Read Position Sensor     │ ─────►  Error is displayed.
│ (SW42) ON?                      │
└─────────────────────────────────┘
              │ YES
              ▼
┌─────────────────────────────────┐
│ The motor rotates CW and the    │
│ document data is scanned by the │
│ Image Sensor until the Read     │
│ Position Sensor (SW42) turns OFF.│
└─────────────────────────────────┘
              │
              ▼
┌─────────────────────────────────┐
│ The motor rotates ccw and the   │
│ document is ejected.           │
└─────────────────────────────────┘
              │
              ▼
┌─────────────────────────────────┐
│             END                 │
└─────────────────────────────────┘
```

CROSS REFERENCE:

  SENSOR SECTION (P.79)

5.4.6.3.3. PRINTING

```
┌─────────────────────────────────┐
│ Is the recording paper installed│
│ in the paper cassette properly ?│
└─────────────────────────────────┘
              │ YES
              ▼
┌─────────────────────────────────┐
│ Is the data received ?          │
└─────────────────────────────────┘
              │ YES
              ▼
┌─────────────────────────────────┐
│ The motor rotates CCW and the   │
│ CAM is set to the Receive mode (B).│
└─────────────────────────────────┘
              │
              ▼
┌─────────────────────────────────┐
│ The motor rotates CW and the    │
│ received document is printed.   │
└─────────────────────────────────┘
              │
              ▼
┌─────────────────────────────────┐
│ The motor rotates CCW and the   │
│ recording paper is ejected.     │
└─────────────────────────────────┘
              │
              ▼
┌─────────────────────────────────┐
│ The motor rotates CW and the    │
│ CAM is set to the Transmit mode (A).│
└─────────────────────────────────┘
              │
              ▼
┌─────────────────────────────────┐
│             END                 │
└─────────────────────────────────┘
```
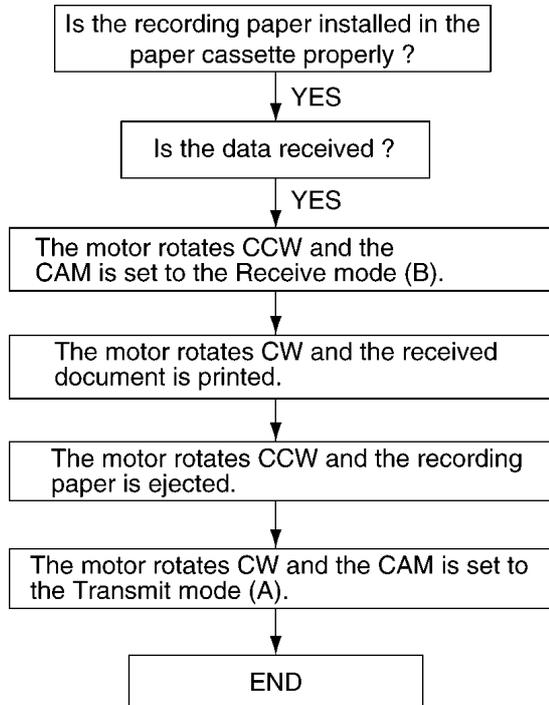
Note:

  See **6.5. SENSERS AND SWITCHES**.

5.4.6.3.4. COPYING

When the document is set in the paper tray, does the Document Sensor (PS1) turn ON ? ──NO──→ See **SENSOR SECTION**

│ YES

The motor rotates cw and the document is pre-fed.

Press the start key.

The motor rotates cw and the Read Position Sensor (SW42) is ON.

The motor rotates ccw and the CAM is set to the Copy mode (C).

The motor rotates ccw and the document data is scanned by the Image Sensor and the recording paper is printed until the Read Position Sensor (SW42) turns OFF.

The motor rotates ccw and the CAM is set to the Receive mode (B).

The motor rotates cw and the recording paper is ejected.

The motor rotates cw and the CAM is set to the Transmit mode (A).

The motor rotates ccw and the document is ejected.

END

CROSS REFERENCE:

SENSOR SECTION (P.79)

5.5. SENSORS AND SWITCHES

All of the sensor and switches are shown below.

Sensor Circuit Location	Sensor	Sensor or Switch Name	Message Error
DIGITAL	SW1	Motor Position	[CALL SERVICE 2] (LLAME SERVICIO 2)
	SW2	Cotter Position	[PAPER JAMED]
ANALOG	SW1	Cover Open and Paper set	[CHECK COVER] and [OUT OF PAPER] (REVISAR LA TAPA) and (SIN PAPEL)
	SW2	Hook SW	———
	SW3	JAM set	[PAPER JAMED] (PAPEL ATAS CADO)
Operation Panel	SW32	Document Read Position	[REMOVE DOCUMENT] (REMOVER DOC)
	PS1	Document set	[CHECK DOCUMENT] (REVISAR DOC)

Sensor Locations
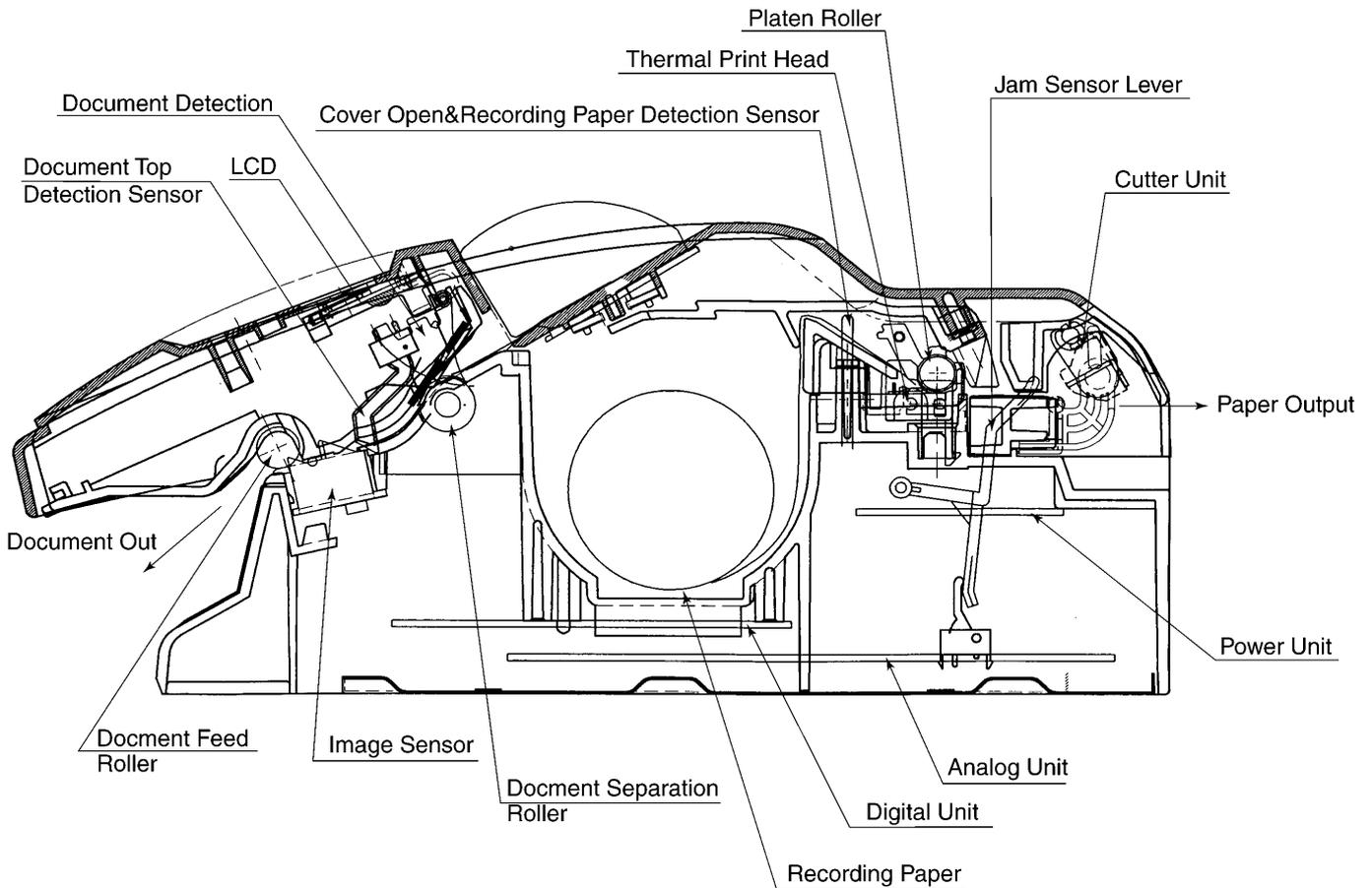
5.5.1. MOTOR POSITION SENSOR

This sensor is a detection switch for recording the position of the CAM.
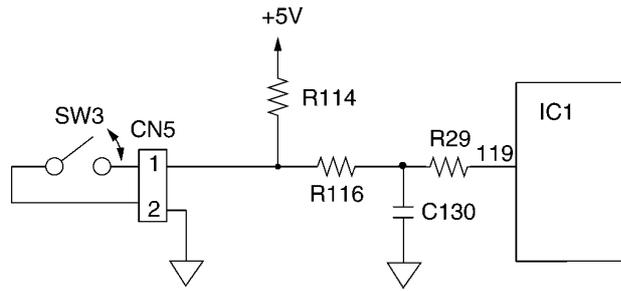
Digital Board	
	Signal (IC1-119 Pin)
Home position	Low level
Other	High level

5.5.2. CUTTER POSITION SENSOR
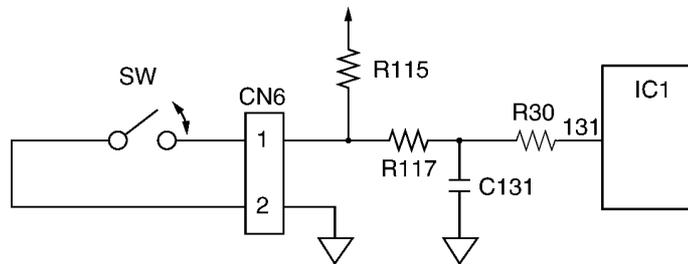
Digital Board	
	Signal (IC1-131 Pin)
Home position	Low level
Other	High level

5.5.3. RECORDING PAPER SENSOR (SW1)

When there is no recording paper, the plate is separated from the switch lever and the switch turns off. Pin 10 of CN1 (Analog board) becomes a high level. When there is recording paper, the plate pushes the switch lever and the switch turns ON. Pin 10 of CN1 (Analog board) becomes a low level.
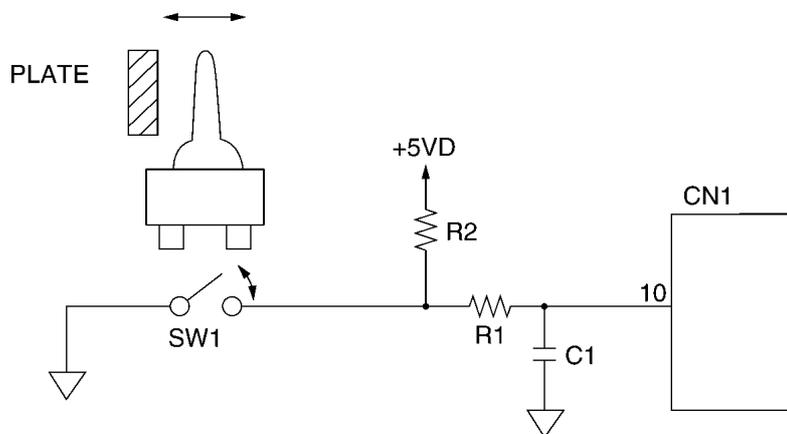
| Analog Board	
	Signal (CN1-10 Pin)
Paper	Low level
No paper	High level

5.5.4. JAM SENSOR (SW3)

The JAM sensor is a detection switch for determining whether the recording paper edge is in the correct position or not. If the recording paper cannot be detected correctly at the JAM sensor position even when recording paper is present, then JAM is displayed. If the recording paper is at the sensor position, then the switch turns on the CN1-11pin (Analog) switches to a high level.
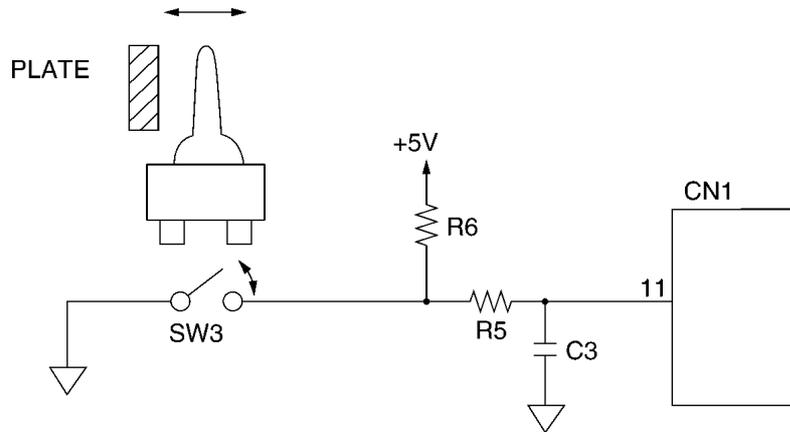
| Analog Board	
	Signal (CN1-11 Pin)
Paper	Low level
No paper	High level

5.5.5. DOCUMENT TOP SW (SW32)

When a document is brought to the read position, the SW becomes ON, and the input signal of IC1-21pin (Operation) becomes a low level. When there is no document at the read position, the SW becomes OFF, and the input signal of IC1-21 pin (Operation) becomes a high level.
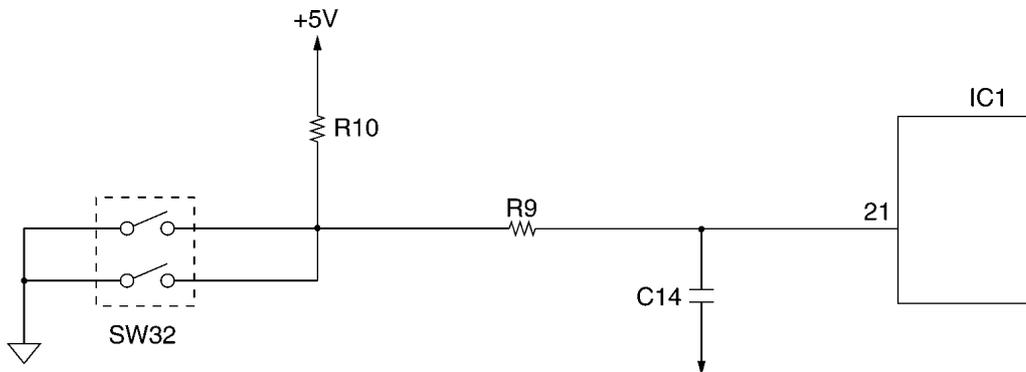
Operation Board	
	Signal (IC1-21 pin)
Out of the Read Position	High level
At the Read Position	Low level

5.5.6. DOCUMENT SET SENSOR (PS1)

When a document is set, the shelter plate closes the sensor light, the photo transistor becomes OFF, and the input signal of the IC1-15 pin (Operation) becomes a high level. When there is no document, the shelter plate passes the sensor light, the photo transistor becomes ON, and the input signal of the IC1-15 pin (Operation) becomes a low level. (When checking this sensor, the IC1-41 pin becomes a low level.)
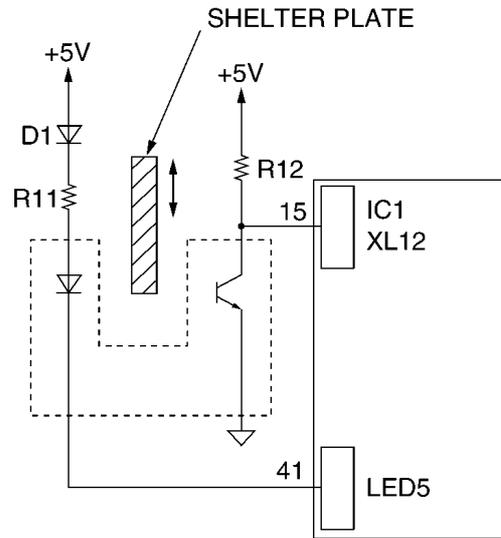
Operation Board		
	Photo transistor	Signal (IC1-15 Pin)
No document	ON	Low level
Set document	OFF	High level

5.6. MODEM SECTION

5.6.1. FUNCTION

The unit uses a 1 chip modem (IC5), enabling it to act as an interface between the control section for FAX sending and receiving, and the telephone line. During a sending operation, the digital image signals are modulated and sent to the telephone line. During a receiving operation, the analog image signals which are received via the telephone line are demodulated and converted into digital image signals. The communication format and procedures for FAX communication are standardized by ITU-T. This 1 chip modem (IC5) has hardware which sends and detects all of the necessary signals for FAX communication and DTMF.

It can be controlled by writing commands from the ASIC (IC1) to the register in the modem (IC5).

This modem (IC5) also sends DTMF signals, and detects busy tones, dial tones and DTMF.

Overview of Facsimile Communication Procedures (ITU-T Recommendation):

1. **ON ITU-T (International Telecommunications´ Union.)**

   The No. XIV Group of ITU-T, one of the four permanent organizations of the International Telecommunications Uniib (ITU), investigates and make recommendations on international standards for facsimiles.

2. **Definition of Each Group**

・Group I (G1)

A-4 size documents without using formats which reduce the band width of a signal sent over telephone lines.
Determined in 1968.
Transmission for about 6 minutes at scanning line density of 3.85 lines/mm.

・Group II (G2)

Using reduction technology in the modulation/demodulation format, an A-4 size document is sent at an official scanning line density of 3.85 lines/mm for about 3 minutes.
Methods to suppress redundancy are not used.
Determined in 1976.

・Group III (G3)

A method of suppressing redundancy in the image signal prior to modulation is used. An A-4 size document is sent with about one minute.
Determined in 1980.

・Group IV (G4)

Transmission is via the data network. A method is provided for suppressing redundancy in signals prior to transmission, and error-free reception of transmission is possible.
The scope of these facsimile applications is not limited simply to transmission of written statements. Through symbiotic linkages with other communication methods, it can be expected to expand to include integrated services.

3. **Facsimile Call Time Series**

As shown in the following diagram, the facsimile call time series is divided into five phases.
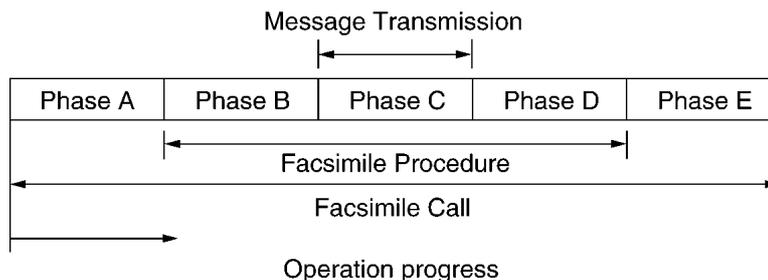
Phase A : Call setting

Call setting can be manual/automatic.

Phase B : Pre-message procedure

Phase B is a pre-processing procedure and sequence for confirming the status of the terminal, transmission route, etc. and for terminal control. It implements the terminal preparation status, determines and displays terminal constants, confirms synchronization status, etc. and prepares for transmission of facsimile messages.

Phase C : Message transmission

Phase C is the procedure for transmitting facsimile messages.

Phase D : Post message procedure

Phase D is the procedure for confirming that the message is completed and received. For continuous transmission, phase B or phase C are repeated for transmission.

Phase E : Call retrieval

Phase E is the procedure for call retrieval, that is for circuit disconnection.

4. **Concerning Transmission Time**

$$\boxed{\text{Transmission Time}} = \boxed{\text{Control Time}} + \boxed{\text{Image Transmission Time}} + \boxed{\text{Hold Time}}$$

Transmission time consists of the following.

Control time:

This is time at the start of transmission when the functions at the sending and receiving sides are confirmed, the transmission mode is established, and transmission and reception are synchronized.

Image transmission time:

This is the time required for the transmission of document contents (image data). In general, this time is recorded in the catalog, etc.

Hold time:

This is the time required after the document contents have been sent to confirm that the document was in fact sent, and to check for telephone reservations and/or the existence of continuous transmission.

5. **Facsimile Standards**

| Item	Telephone Network Facsimile
	G3 Machine
Connection Control Mode	Telephone Network Signal Mode
Terminal Control Mode	T. 30 Binary
Facsimile Signal Format	Digital
Modulation Mode	PSK (V. 27 ter) or QAM (V. 29)
Transmission Speed	300 bps (Control Signal) 2400, 4800, 7200, 9600 bps (FAX Signal)
Redundancy Compression Process (Coding Mode)	1 dimension: MH Mode 2 dimension: MR Mode (K=2.4)
Resolution	Main Scan: 8 pel/mm Sub Scan: 3.85, 7.7l/mm
Line Synchronization Signal	EOL Signal
1 Line Transmission Time [ms/line]	Depends on the degree of data reduction. Minimum Value: 10, 20 Can be recognized in 40ms.

6. Explanation of Technology

a. G3 Communication Signals (T. 30 Binary Process)

For G3 facsimile communication, this is the procedure for exchanging control signals between the sending and receiving machines both before and after transmission of image signals.

Control signals at 300 bps FSK are: 1850 Hz...0, 1650Hz...1.

An example of the binary process in G3 communication is shown below.
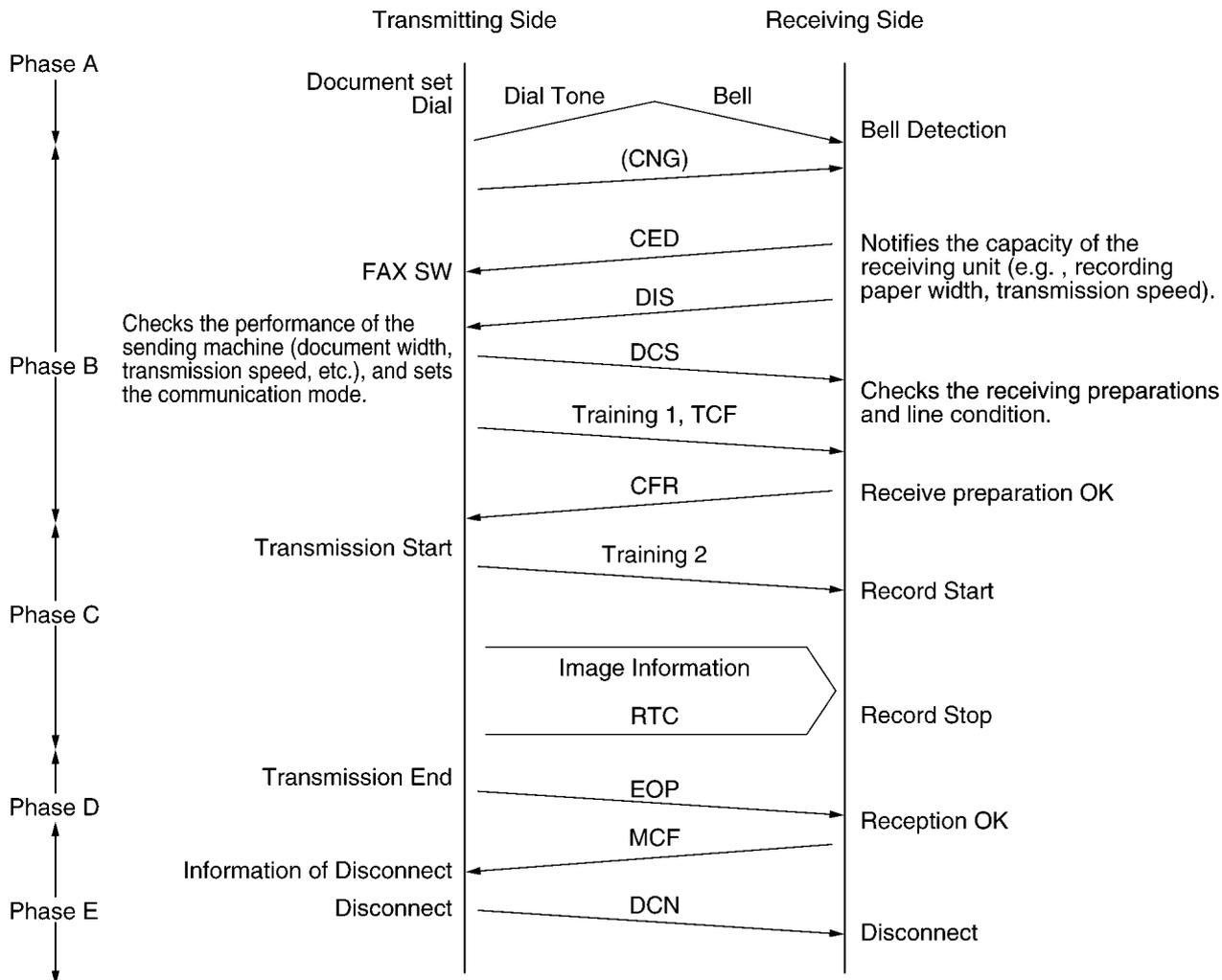
Explanation of Signals

Control signals are comprised mainly of 8-bit identification signals and of the data signals added to them. Data signals are added to DIS and DCS signals.

Signal.....DIS (Digital Identification Signal)
Identification Signal Format.....00000001

Function:
Notifies the capacity of the receiving unit. The added data signals are as follows.

(Example)

Bit No.	DIS/DTC	DCS
1	Transmitter - T.2 operation	
2	Receiver - T.2 operation	Receiver - T.2 operation
3	T.2 IOC = 176	T.2 IOC = 176
4	Transmitter - T.3 operation	
5	Receiver - T.3 operation	Receiver - T.3 operation
6	Reserved for future T.3 operation features.	
7	Reserved for future T.3 operation features.	
8	Reserved for future T.3 operation features.	
9	Transmitter - T.4 operation	
10	Receiver - T.4 operation	Receiver - T.4 operation
11, 12 (0, 0) (0, 1) (1, 0) (1, 1)	Data signaling rate V.27 ter fall back mode V.27 ter V.29 V.27 ter and V.29	Data signaling rate 2400 bit/s, V.27 ter 4800 bit/s, V.27 ter 9600 bit/s, V.29 7200 bit/s, V.29
13	Reserved for the new modulation system.	
14	Reserved for the new modulation system.	
15	Vertical resolution = 7.7 line/mm	Vertical resolution = 7.7 line/mm
16	Two-dimensional coding capability	Two-dimensional coding
17, 18 (0, 0) (0, 1) (1, 0) (1, 1)	Recording width capabilities 1728 picture elements along scan line length of 215 mm ± 1% 1728 picture elements along scan line length of 215 mm ± 1% and 2048 picture elements along scan line length of 255 mm ± 1% and 2432 picture elements along scan line length of 303 mm ± 1% 1728 picture elements along scan line length of 215 mm ± 1% and 2048 picture elements along scan line length of 255 mm ± 1% Invalid	Recording width 1728 picture elements along scan line length of 215 mm ± 1% 2432 picture elements along scan line length of 303 mm ± 1% 2048 picture elements along scan line length of 255 mm ± 1% Invalid
19, 20 (0, 0) (0, 1) (1, 0) (1, 1)	Maximum recording length capability A4 (297 mm) Unlimited A4 (297 mm) and B4 (364 mm) Invalid	Maximum recording length A4 (297 mm) Unlimited B4 (364 mm) Invalid

Signal.....DCS (Digital Command Signal)

Identification Signal Format.....X1000001

Function:

Notifies the capacity of the receiving machine obtained at DIS and announces the transmission mode of the sender. The added data signals are as follows.

(Example)

Bit No.	DIS/DTC	Standard setting	DCS
21, 22, 23 (0, 0, 0) (0, 0, 1) (0, 1, 0) (1, 0, 0) (0, 1, 1) (1, 1, 0) (1, 0, 1) (1, 1, 1)	Minimum scan line time capability of the receiver 20 ms at 3.85 l/mm: T7.7 = T3.85 40 ms at 3.85 l/mm: T7.7 = T3.85 10 ms at 3.85 l/mm: T7.7 = T3.85 5 ms at 3.85 l/mm: T7.7 = T3.85 10 ms at 3.85 l/mm: T7.7 = 1/2 T3.85 20 ms at 3.85 l/mm: T7.7 = 1/2 T3.85 40 ms at 3.85 l/mm: T7.7 = 1/2 T3.85 0 ms at 3.85 l/mm: T7.7 = T3.85		Minimum scan line time 20 ms 40 ms 10 ms 5 ms 0 ms
24	Extend field	1	Extend field
25	2400 bit/s handshaking	0	2400 bit/s handshaking
26	Uncompressed mode	0	Uncompressed mode
27	Error correction mode	0	Error correction mode
28	Set to "0".	0	Frame size 0 = 256 octets 1 = 64 octets
29	Error limiting mode	0	Error limiting mode
30	Reserved for G4 capability on PSTN	0	Reserved for G4 capability on PSTN
31	Unassigned	0	
32	Extend field	1	Extend field
33 (0) (1)	Validity of bits 17, 18 Bits 17, 18 are valid Bits 17, 18 are invalid	0	Recording width Recording width indicated by bits 17, 18 Recording width indicated by this field bit information

Bit No.	DIS/DTC	Standard setting	DCS
34	Recording width capability 1216 picture elements along scan line length of 151 ± mm 1%	0	Middle 1216 elements of 1728 picture elements
35	Recording width capability 864 picture elements along scan line length of 107 ± mm 1%	0	Middle 864 elements of 1728 picture elements
36	Recording width capability 1728 picture elements along scan line length of 151 ± mm 1%	0	Invalid
37	Recording width capability 1728 picture elements along scan line length of 107 ± mm 1%	0	Invalid
38	Reserved for future recording width capabilities.	0	
39	Reserved for future recording width capabilities.	0	
40	Extend field	1	Extend field
41	Semi super time / mm	1	
42	Semi super time / mm	0	
43	Super time	0	
44	Inch	0	
45	mm	1	
46	MSC/SF	0	
47	Select Polling	0	
48	EXT	0	

Note 1 - Standard facsimile units conforming to T.2 must have the following capability: Index of cooperation (IOC)=264.

Note 2 - Standard facsimile units conforming to T.3 must have the following capability: Index of cooperation (IOC)=264.

Note 3 - Standard facsimile units conforming to T.4 must have the following capability: Paper length=297 mm.

Signal	Identification Signal Format	Function
Training 1	——————	A fixed pattern is transmitted to the receiving side at a speed (2400 to 9600 bps) designated by DCS, and the receiving side optimizes the automatic equalizer, etc., according to this signal.
TCF (Training Check)	——————	Sends 0 continuously for 1.5 seconds at the same speed as the training signal.
CFR (Confirmation to Receive)	X0100001	Notifies the sending side that TCF has been properly received. If TCF is not properly received, FTT (Failure To Train) X0100010 is relayed to the sender. The sender then reduces the transmission speed by one stage and initiates training once again.
Training 2	——————	Used for reconfirming the receiving side like training 1.
Image Signal	Refer to the next page.	——————
RTC (Return to Control)	——————	Sends 12 bits (0...01 × 6 times) to the receiver at the same speed as the image signal and notifies completion of transmission of the first sheet.
EOP (End of Procedure)	X1110100	End of one communication
MCF (Message Confirmation)	X0110001	End of 1 page reception
DCN (Disconnect)	X1011111	Phase E starts.
MPS (Multi-Page Signal)	X1110010	Completion of transmission of 1 page. If there are still more documents to be sent, they are output instead of EOP. After MCF reception, the sender transmits an image signal of the second sheet.
PRI-EOP (Procedural Interrupt-EOP)	X1111100	If there is an operator call from the sender, it is output after RTC.
PIP (Procedural Interrupt Positive)	X0110101	This is output when an operator call is received.

b. **Redundancy Compression Process Coding Mode**

This unit uses one-dimensional MH format.

Modified Huffman (MH) Code		
Run length	Code for White Line	Code for Black Line
0	00110101	000011011
1	000111	010
2	0111	11
3	1000	10
4	1011	011
5	1100	0011
6	1110	0010
7	1111	00011
8	10011	000101
9	10100	000100
10	00111	0000100
11	01000	0000101
12	001000	0000111
13	000011	00000100
14	110100	00000111
15	110101	000011000
16	101010	0000010111
17	101011	0000011000
18	0100111	0000001000

(a) Document

Basic Facsimile Technique

(b) Part of document

Facsimile

(c) Run length and image signals equivalent to (b)

Black 4 2 4 2 8 3
White 15 12 16 18 13

(d) Codification of (c) according to MH formula

00110111101010 011 110101 11 001000 011 101010
(White 400) (Black 4) (White 15) (Black 2) (White 12) (Black 4) (White 16)

11 0100111 000101 000011 10
(Black 2) (White 18) (Black 8) (White 13) (Black 3)

(c) Total bit number before MH codification (497 bit)
(d) Total bit number after MH codification (63 bit)

5.6.2. MODEM CIRCUIT OPERATION

The modem (IC5) has all the hardware satisfying the ITU-T standards mentioned previously.

When the ASIC IC1 (61) is brought to a low level, the modem (IC5) is chip-selected and the resistors inside IC are selected by the select signals from ASIC (IC1) ADR0-ADR4. The commands are written through the data bus, and all the processing is controlled by the ASIC (IC1) according to ITU-T procedures. The INT signal dispatched from IRQ1, 2 (pins 108 and 121 of IC5) to ASIC (IC1) when the transmission data is accepted and the received data is demodulated, the ASIC (IC1) implements post processing. This modem (IC5) has an automatic application equalizer.

With training signal 1 or 2 during G3 reception, it can automatically establish the optimum equalizer. The modem (IC5) operates using the 32.256 MHz clock (X3).

1. **Facsimile Transmission**

   The digital image data on the data bus is modulated in the modem (IC5), and sent from pin 69 via analog SW (IC9) and amplifier IC10 and the NCU section to the telephone line.

   Refer to **CHECK SHEET** (P.70)

2. **Facsimile Reception**

   The analog image data which is received from the telephone line passes through the NCU section and enters pin 60 of the modem (IC5). The signals that enter pin 60 of the modem (IC5) are demodulated in the board to digital image signals, then placed on the data bus.

   In this case, the image signals from the telephone line are transmitted serially. Hence, they are placed on the bus in 8 bit units. Here, the internal equalizer circuit reduces the image signals to a long-distance receiving level.

   This is designed to correct the characteristics of the frequency band centered about 3 kHz and maintain a constant receiving sensitivity. It can be set in the service mode.

   Refer to **CHECK SHEET** (P.70)

3. **DTMF Transmission (Monitor tone)**

   The DTMF signal generated in the modem (IC5) is output from pin 69, and is then sent to the circuit on the same route as used for facsimile transmission.

   Refer to **CHECK SHEET** (P.70)

   (DTMF Monitor Tone)
   Refer to **CHECK SHEET** (P.70)

4. **Busy/Dial Tone Detection**

   The path is the same as FAX receiving. When it is detected, the carrier detect bit of the resistor in the modem (IC5) becomes 1, and this status is monitored by the ASIC (IC1).