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MS-7357

uATX Version: 1.0

CPU: Intel, Socket 775 (Intel Core 2 Duo Processors, Intel Pentium D Processors, Intel Pentium 4 Processors, Intel Celeron D Processors)--
65-130 watts Intel Core 2 Duo, Pentium D, Celeron D

System Chipset:

Intel Bearlake - Q (North Bridge)
Intel ICH9 (South Bridge)

On Board Device:

CLOCK Gen -- ICS9LPRS906
LPC Super I/O -- Fintek F71882FG
IEEE1394 -- VIA VT6308
Storage controller -- Marvell 88SE6111
LAN -- Marvell 88E8071/8056/8039
HD Audio Codec -- ALC888

Main Memory:

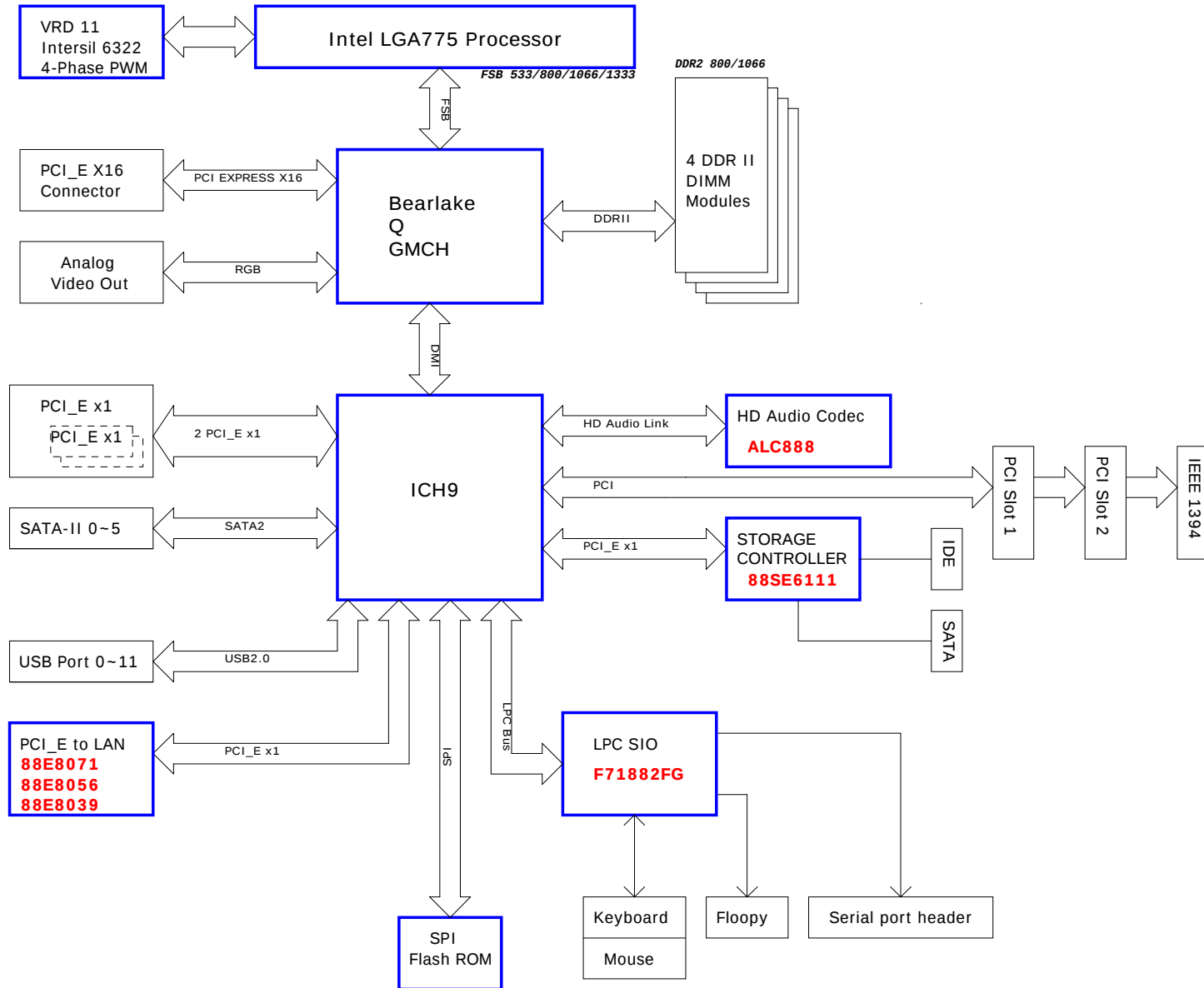
Dual-channel DDR-II * 4

Expansion Slots:

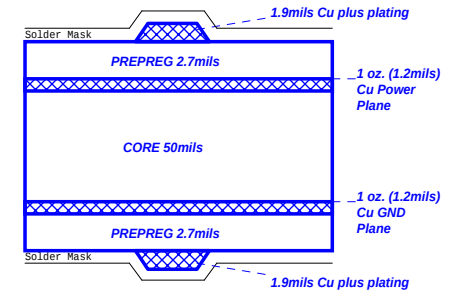
PCI EXPRESS X16 SLOT *1
PCI EXPRESS X1 SLOT * 1
PCI SLOT * 2

PWM: VRD11 Intersil 6322 4Phase

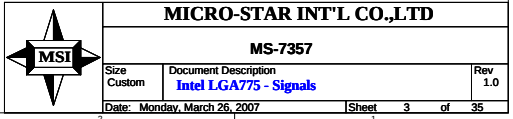
Block Diagram

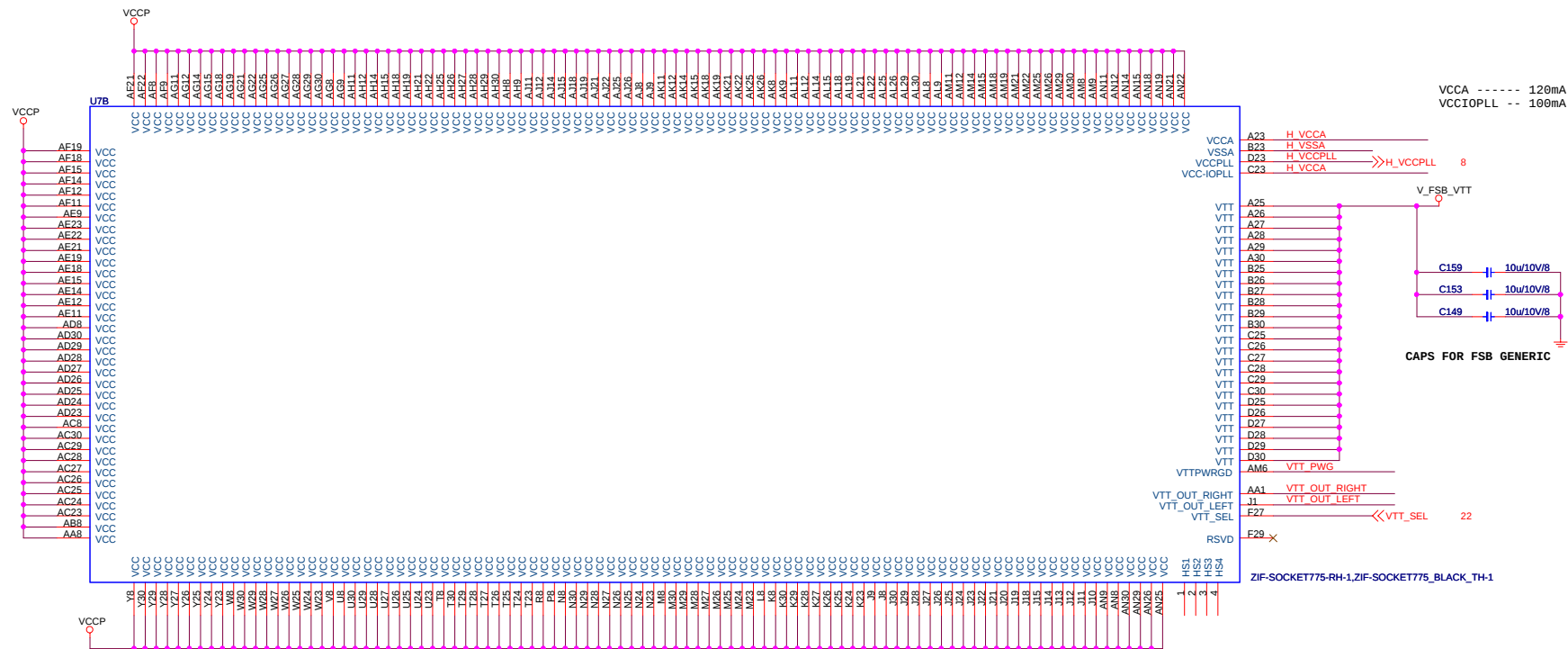


Board Stack-up (1080 Prepreg Considerations)



Single End 50ohm Top/Bottom : 4mils
 USB2.0 - 90ohm : 15/7.5/4.5/7.5/15
 SATA - 95ohm : 15/8/4/8/15
 LAN - 100ohm : 15/10/4/10/15
 PCIE - 95ohm : 15/8/4/8/15





Follow Intel suggestion document to set CPU_GTLREF[3:0] to 63.5%.

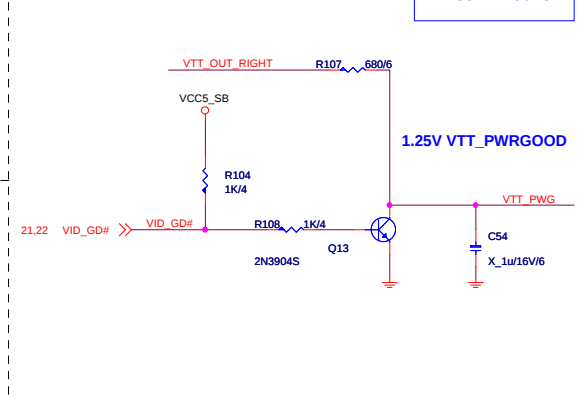
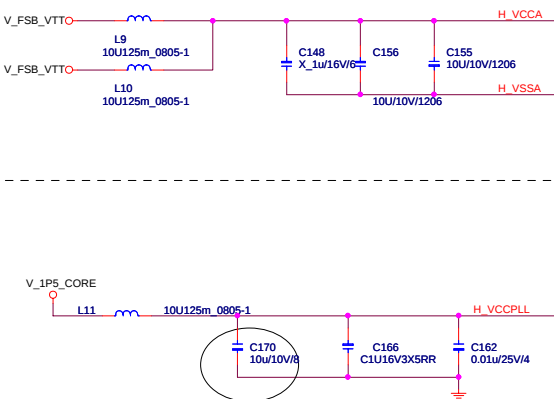
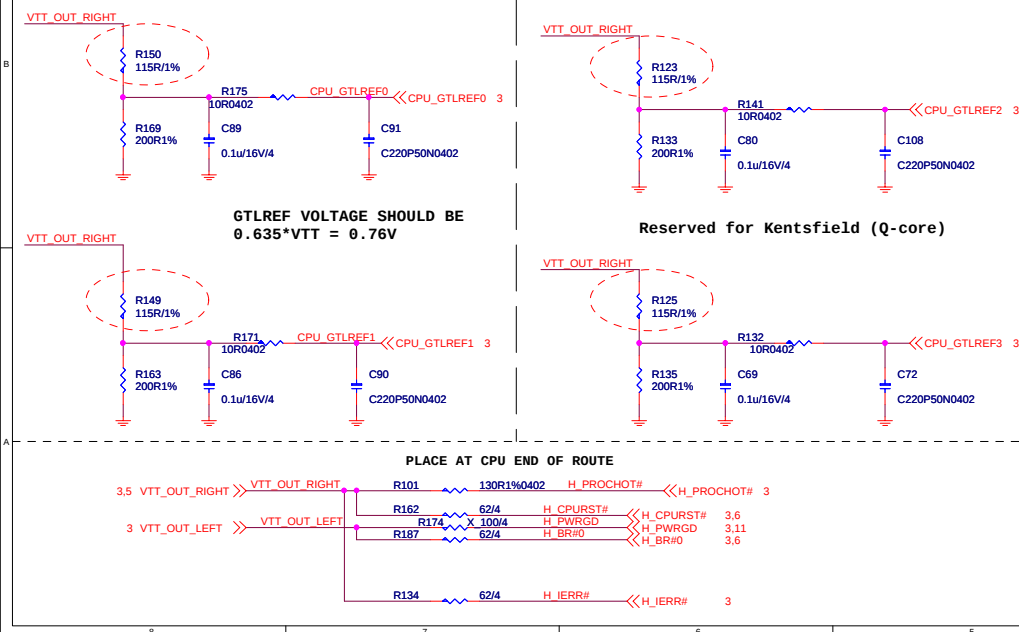
* Use 57.6 Ohm 1% resistor over 100 Ohm 1% resistor.

* Divider could also be 115 Ohm 1% resistor over 200 Ohm 1% resistor.

2007/4/3 R(123,125,149,150) change to 115 ohm 1%.

PLACE COMPONENTS AS CLOSE AS POSSIBLE TO PROCESSOR SOCKET

TRACE WIDTH TO CAPS MUST BE SMALLER THAN 12MILS





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Custom	Intel LGA775 CPU - GND	1.0
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ZIF-SOCKET775-RH-1,ZIF-SOCKET775_BLACK_TH-1

B1

B14

B5

B24

B8

C10

C13

C16

C19

C22

C4

C7

D12

D15

D18

D21

D24

D3

D5

D6

D8

E11

E14

E17

E2

E20

E25

E26

E27

E28

E8

F10

F13

F16

F19

F22

F4

F7

G1

H10

H11

H12

H13

H14

VSS

VSS

VSS

VSS

VSS

VSS

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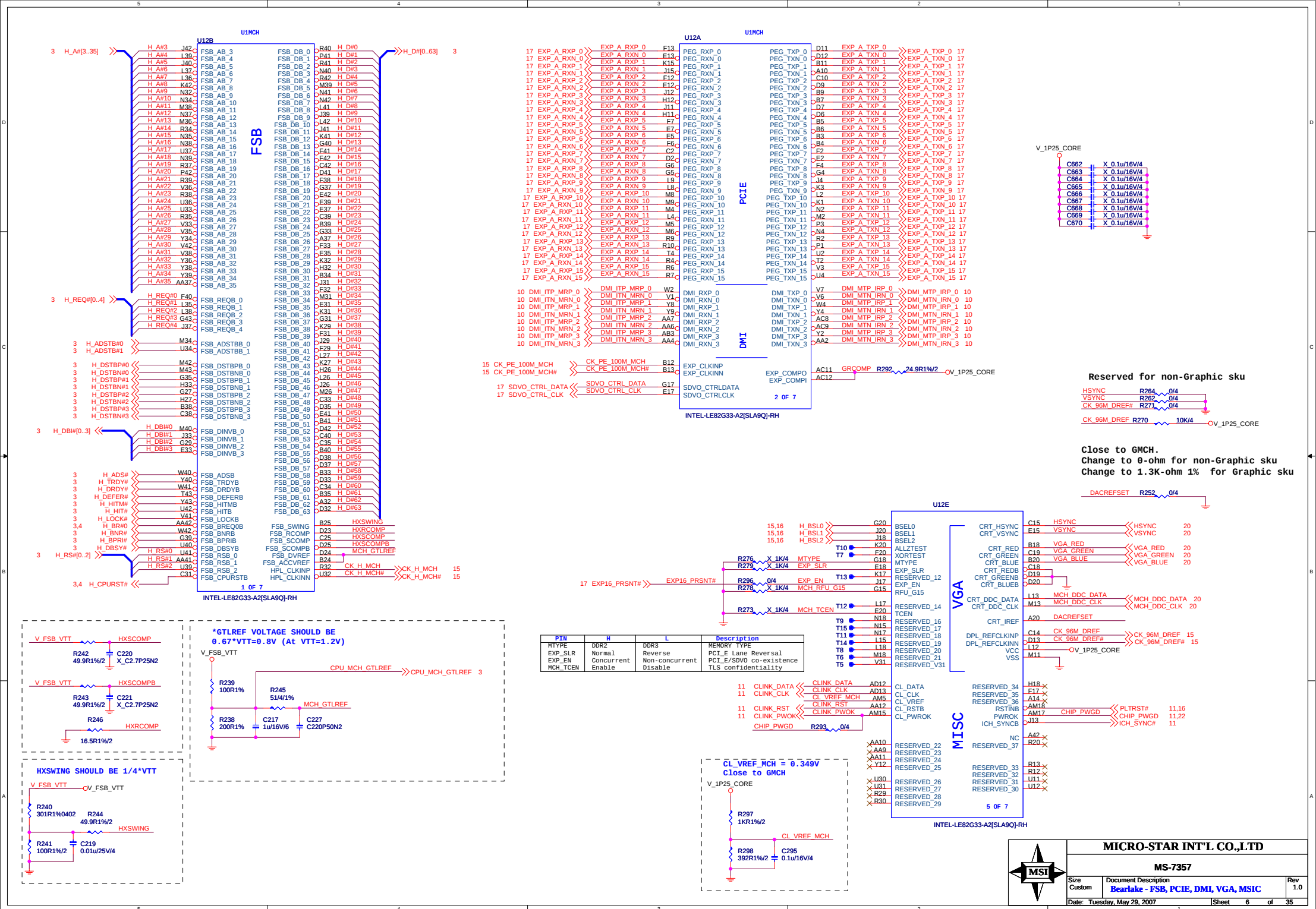
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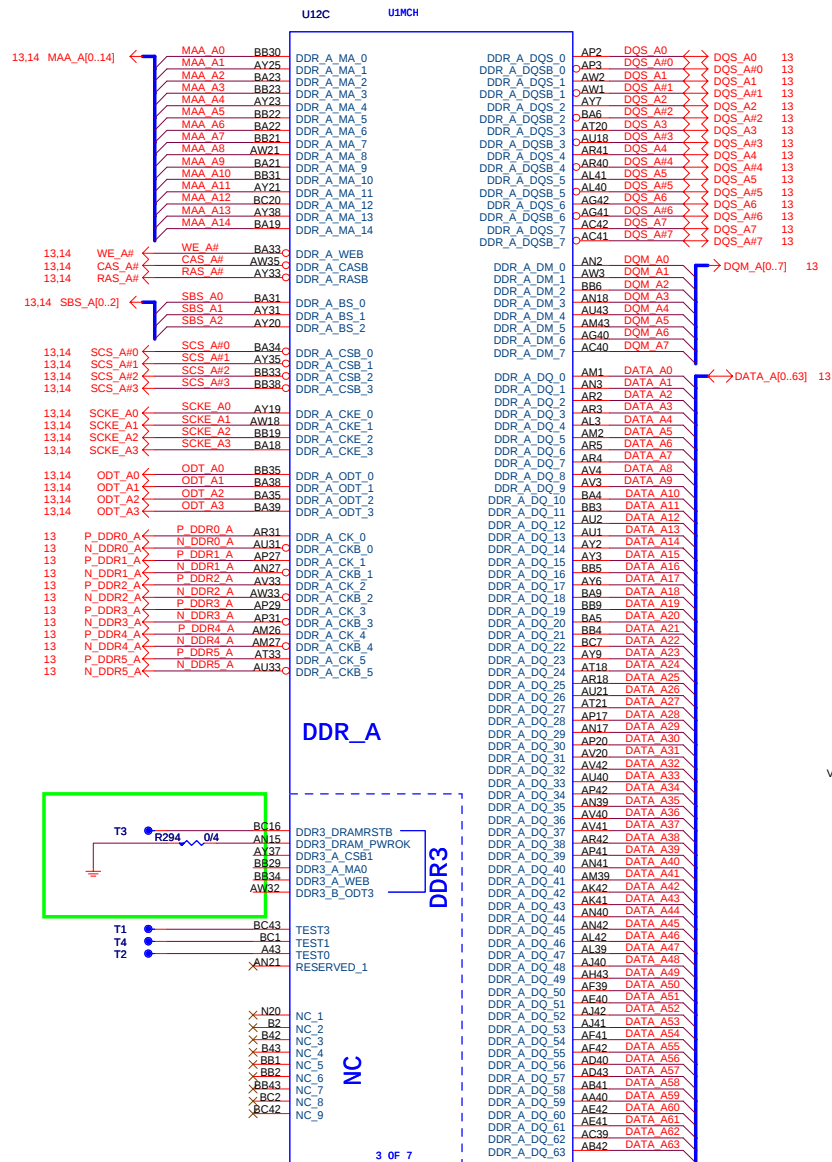
VSS

VSS

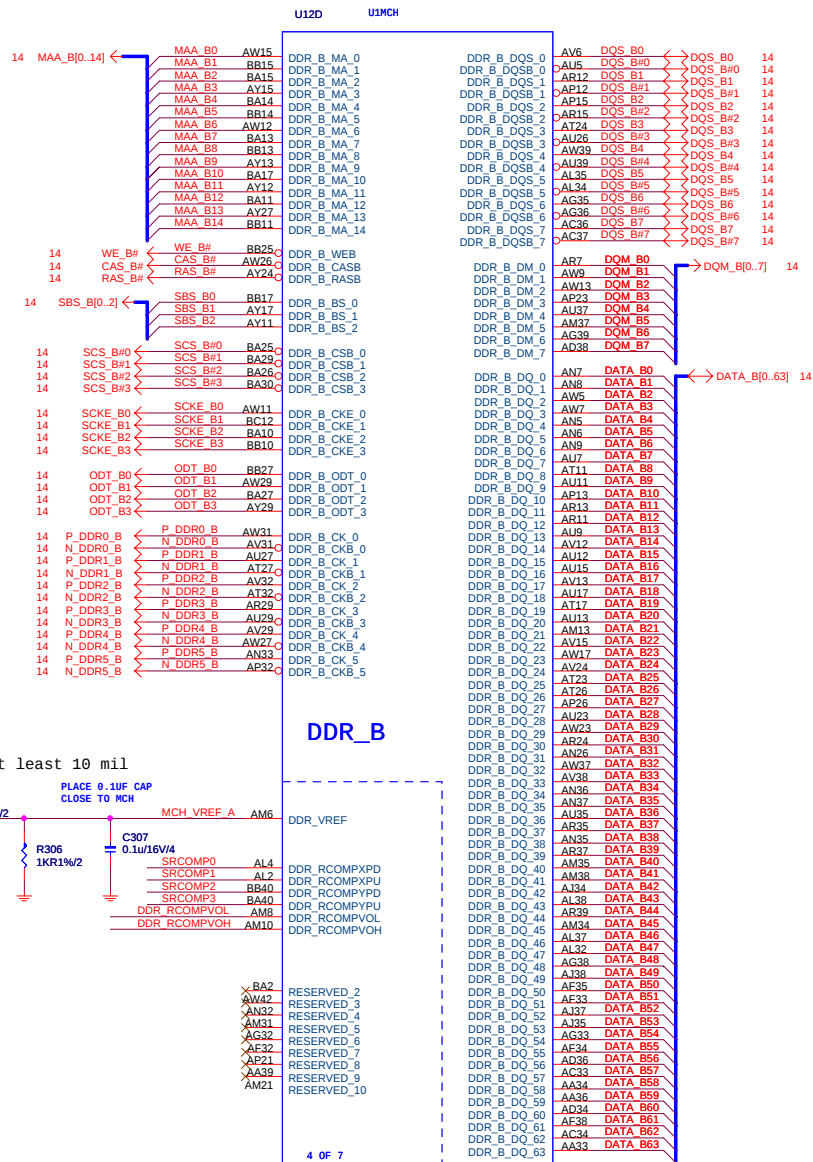
VSS

VSS

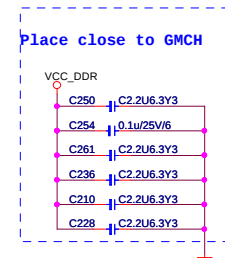
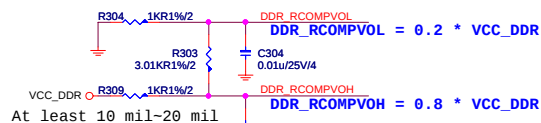
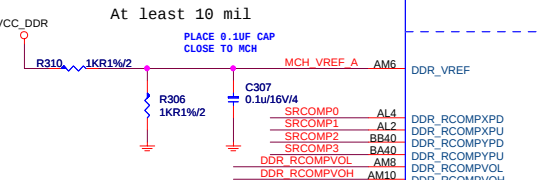




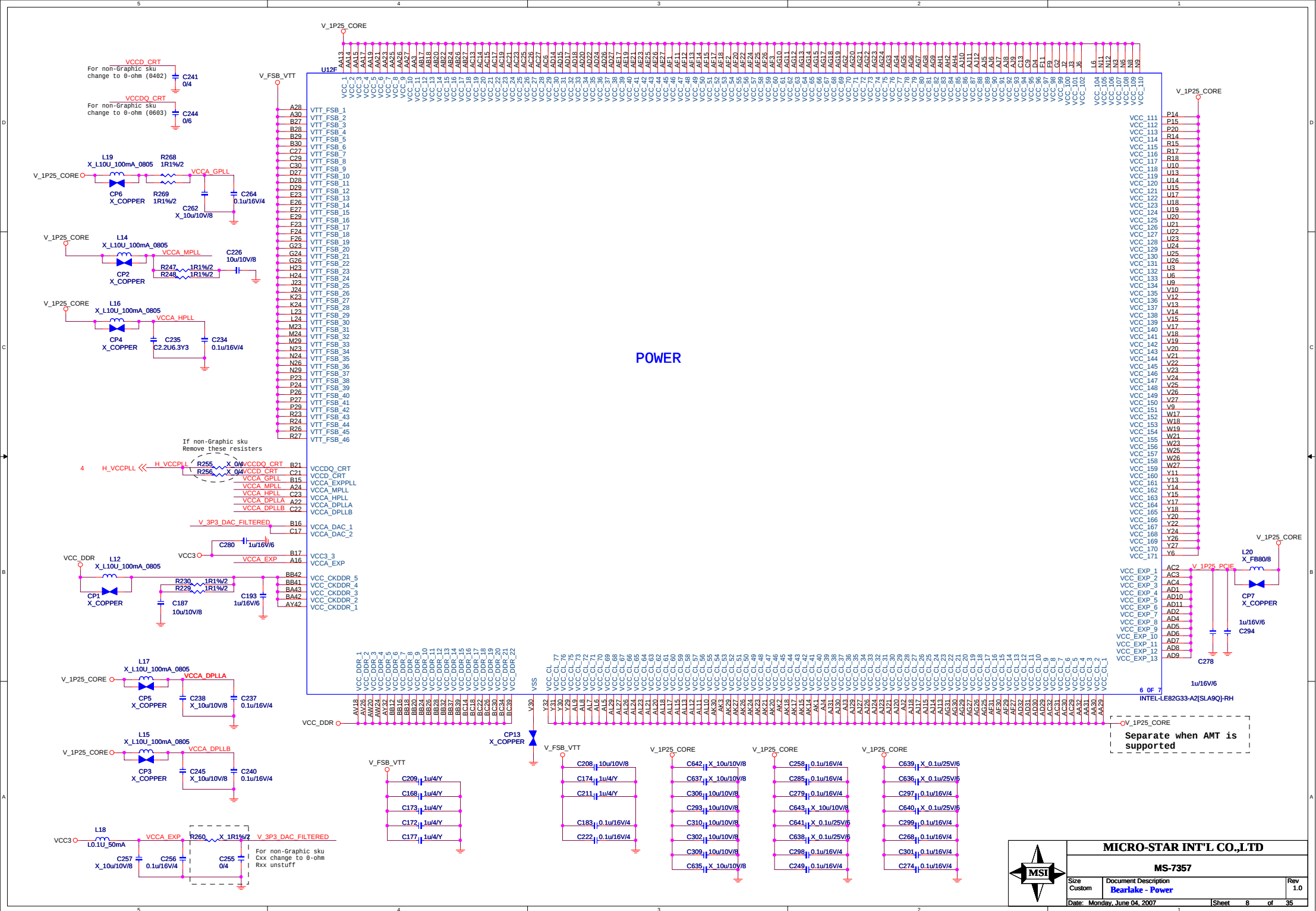
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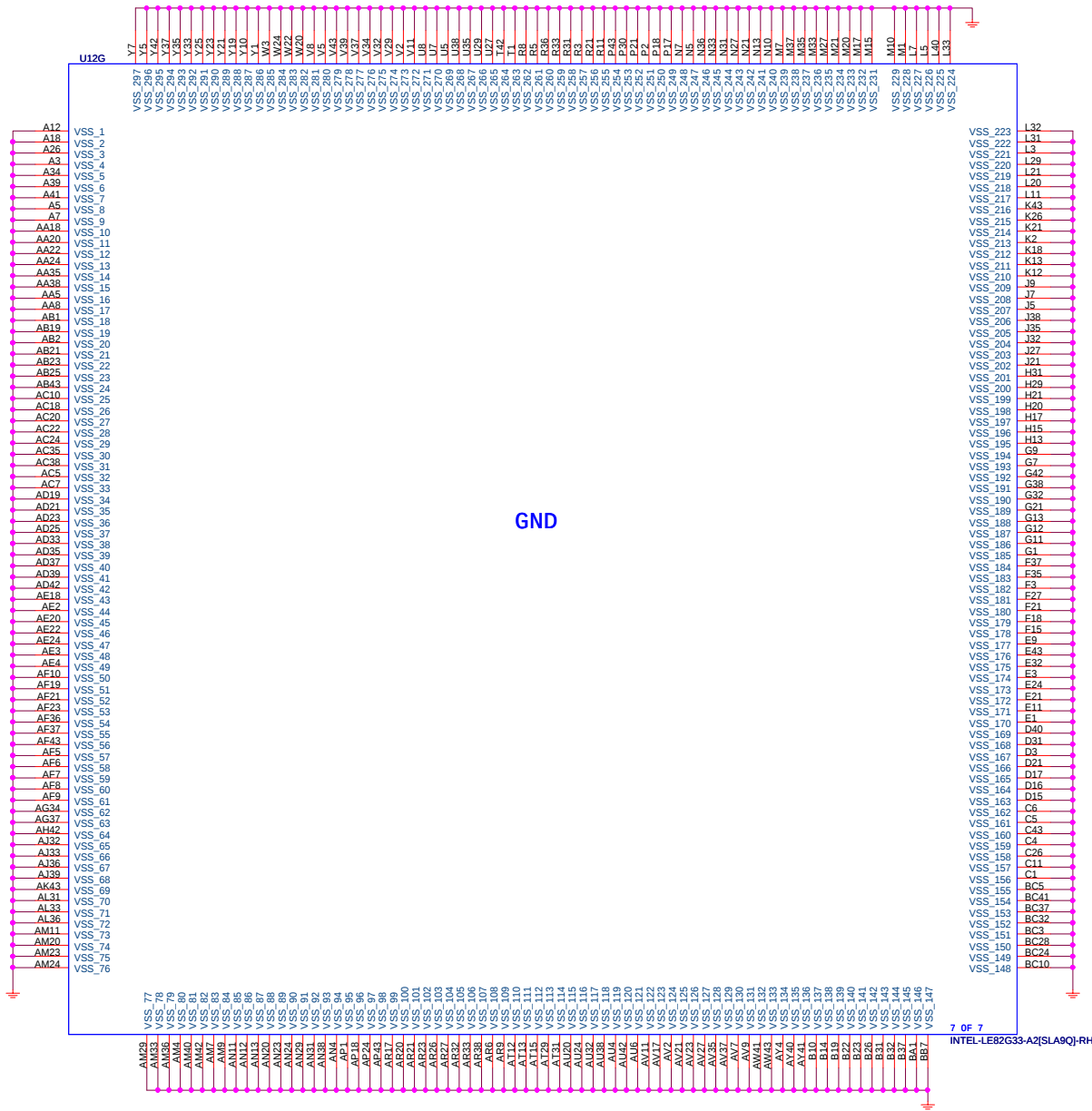


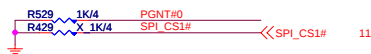
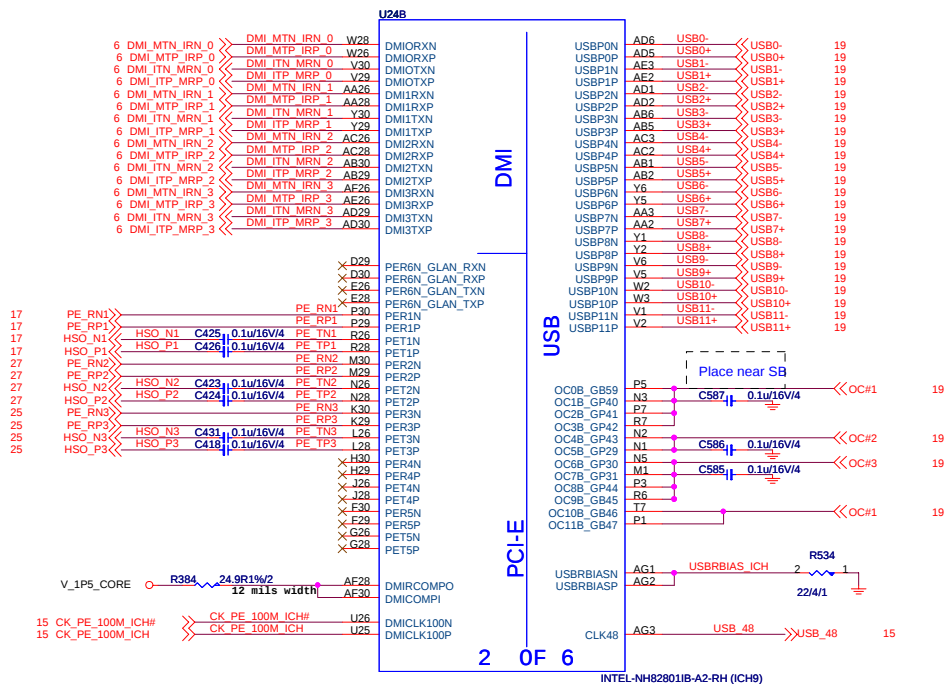
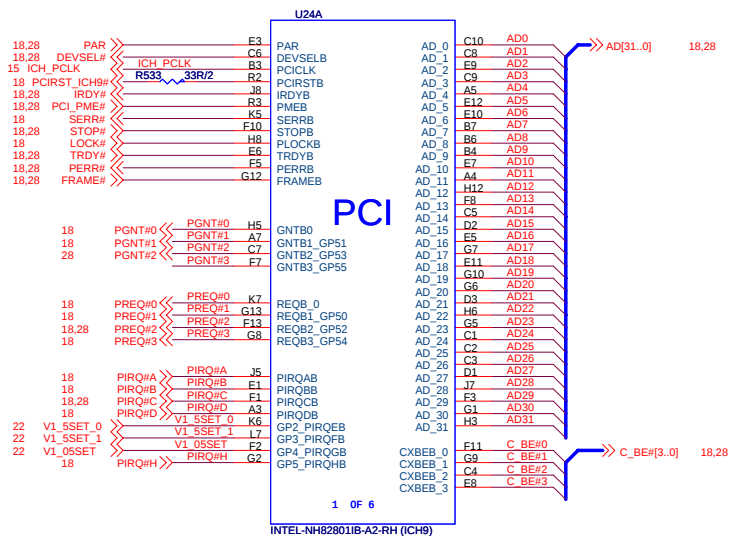
INTEL-E82G33-A2[SLA9Q]-RH



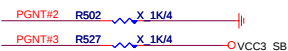
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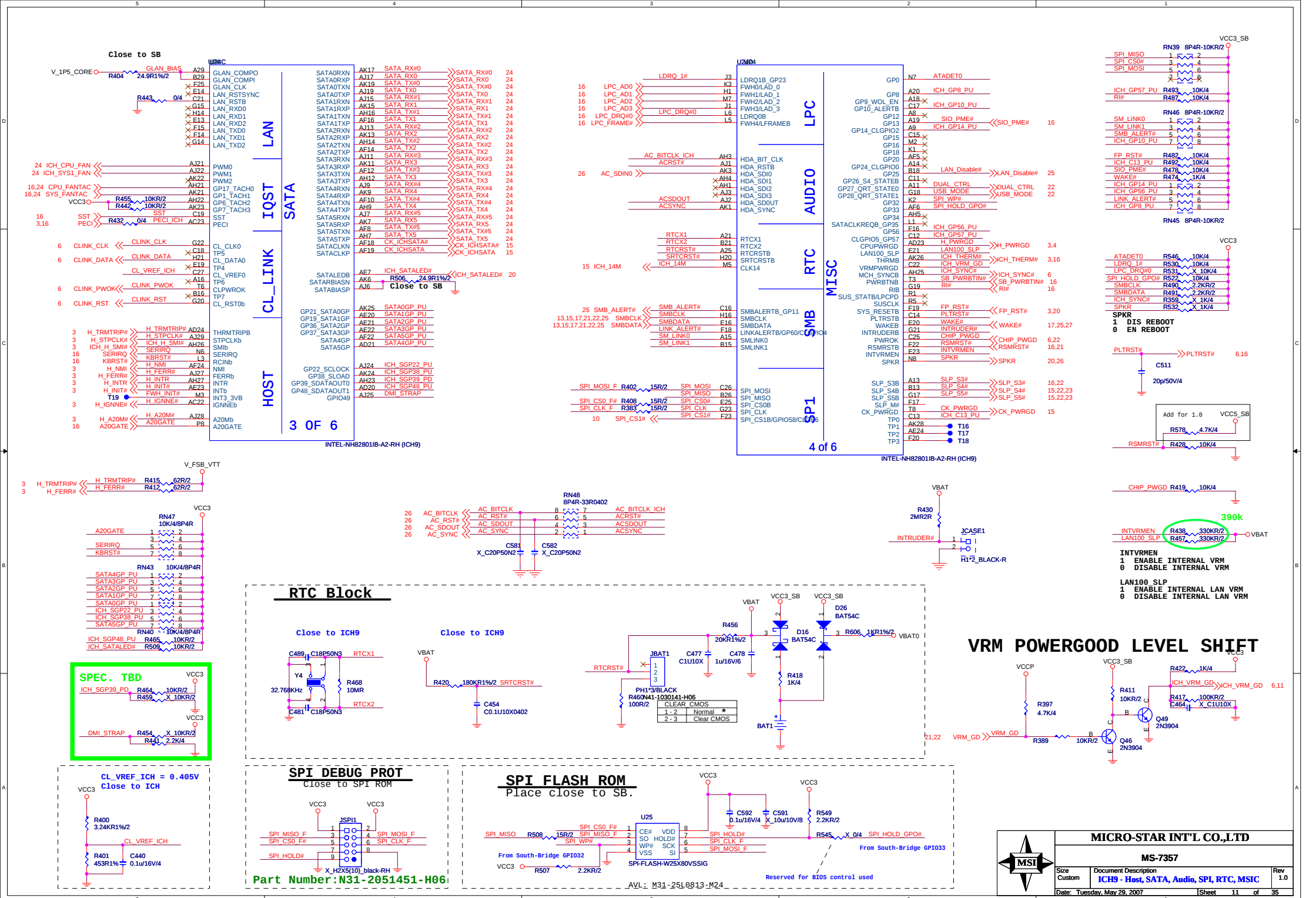




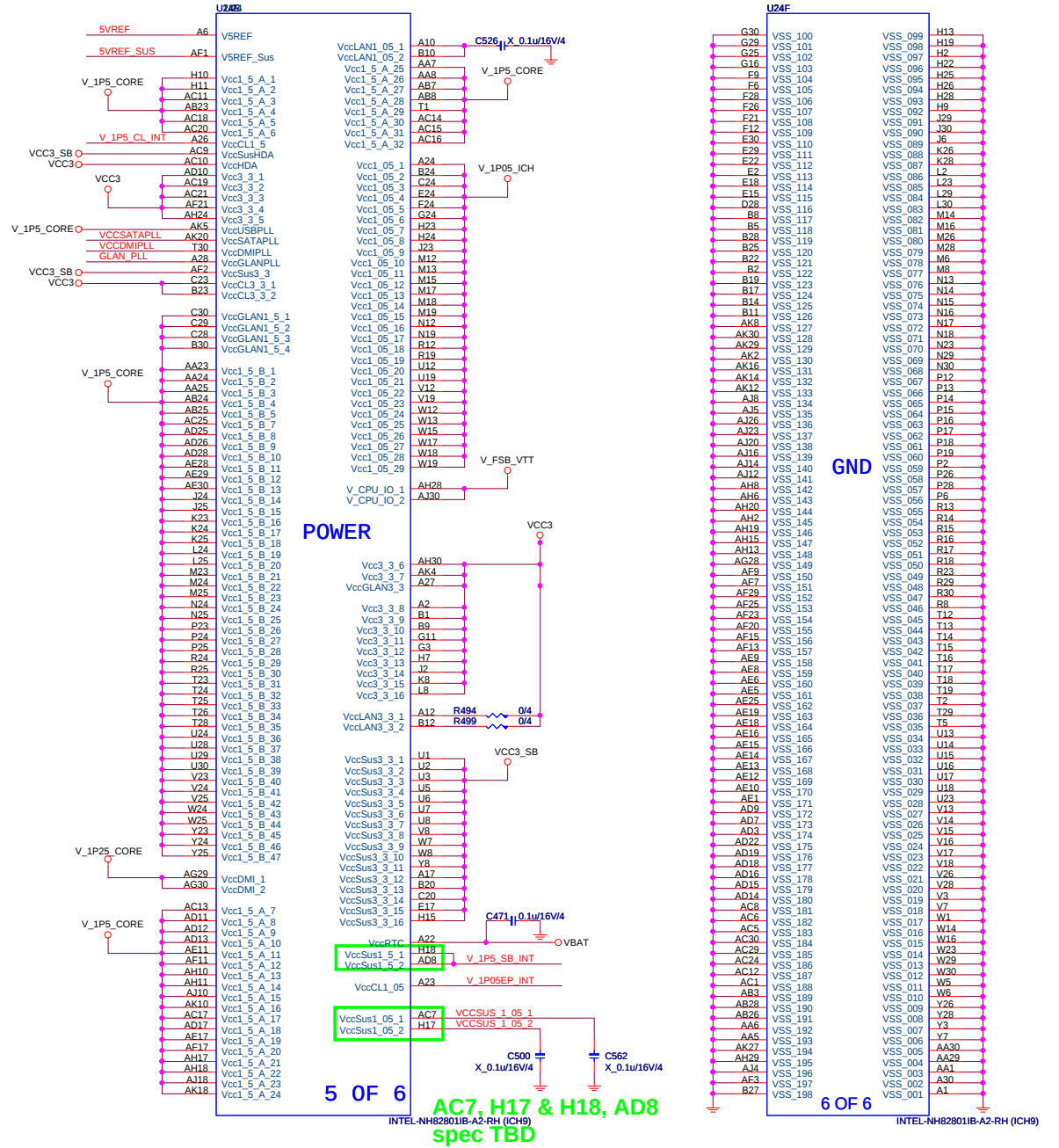
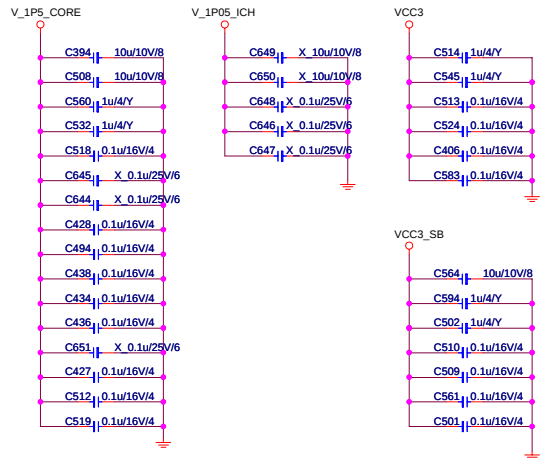
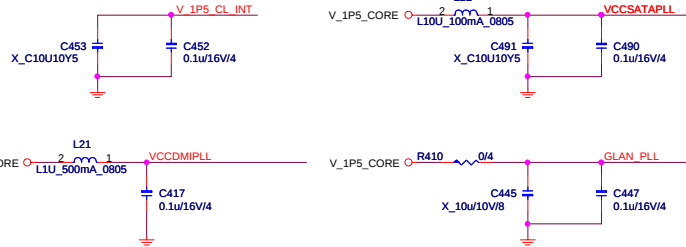
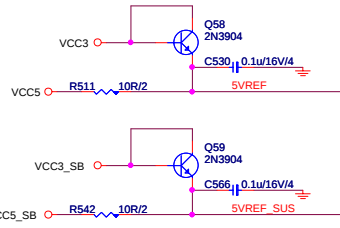
BOOT SELECT STRAPS			
BOOT DEVICE	GNT#0	SPI_CS1#	
FWH	1	1	
SPI	0	X	
PCI	1	0	



SIGNAL	H	L	DES.
GNT3	DIS	EN	A16 OVERRIDE
GNT2	N/A	SET BIT	PCIE PORT CONFIG 2 BIT 0 (5-6)



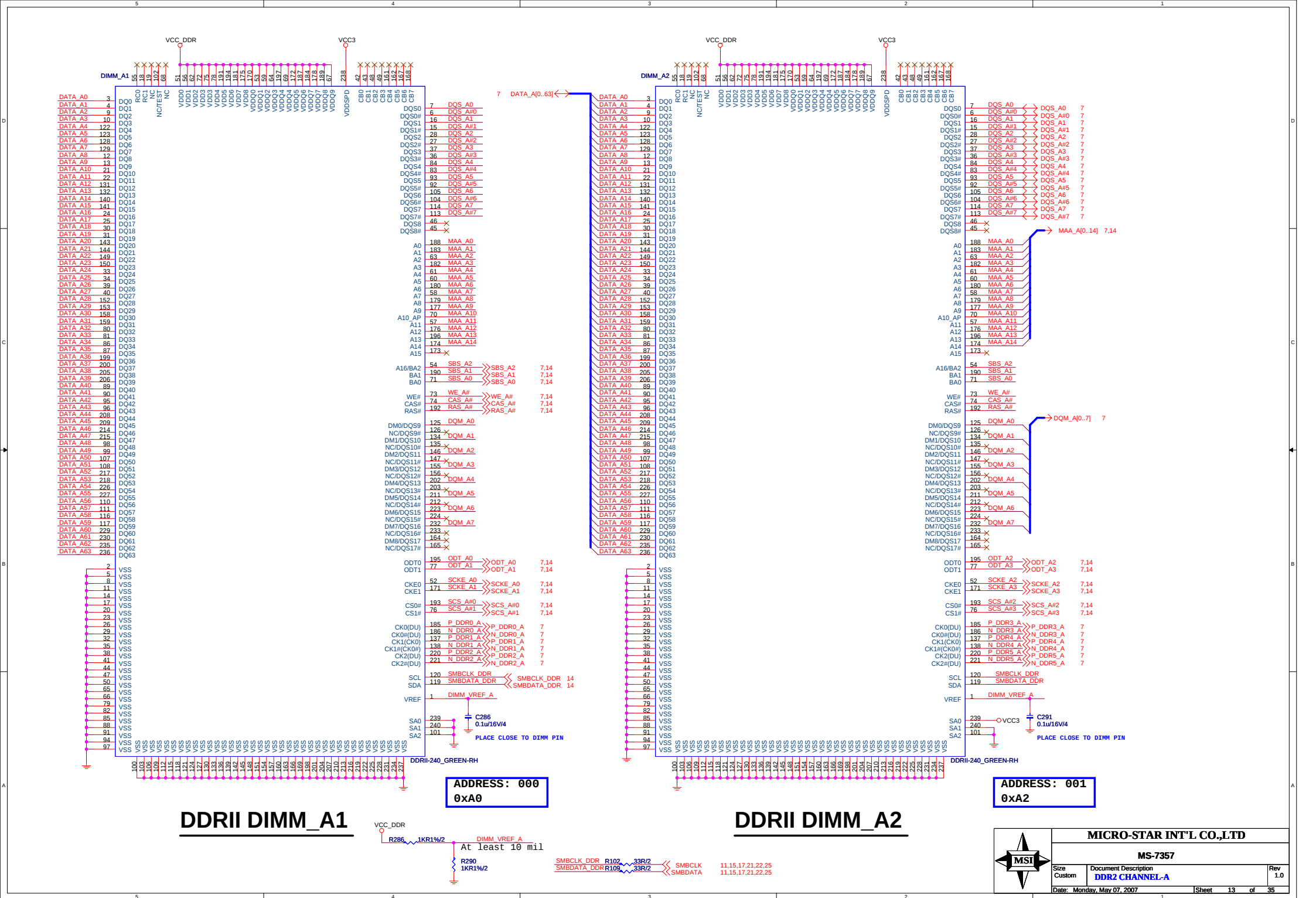
5VREF & 5VREF_SUS Sequencing Circuit



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Non used COM2 must pull high

LPC I/O STRAPPING RESISTOR

DTRB#(FWH TRAP)
HI : SPI as a backup BIOS (Default)
LO : SPI as a primary BIOS

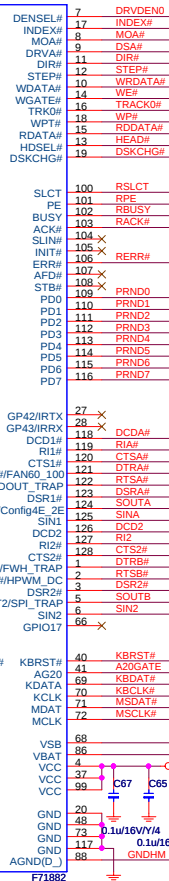
RTSB#(HPWM DC)
 HI : FAN control with PWM mode (Default)
 LO : FAN control with Linear mode

SOUTB(SPI_TRAP)
HI : SPI function disable (Default)
LO : SPI function enable

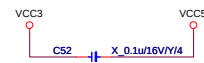
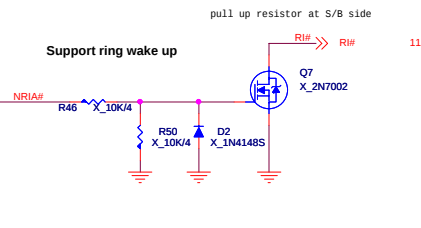
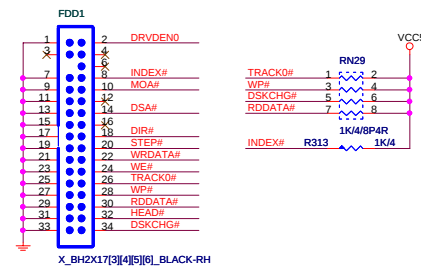
RTSA#(VIDOUT)
 HI : 6 pins VIDIN and 6 pins VIDOUT (Default)
 LO : VIDIN/VIDOUT on 6 pins, Original
 VIDOUT pins will be GPIO pins

SOUTA(Config4E_2E)
 HI : Configuration Register I/O port is 4E/4F (Default)
 LO : Configuration Register I/O port is 2E/2F

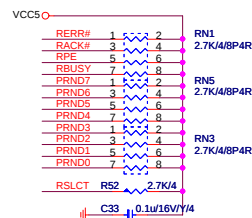
DTRA#(FAN60_100)
 HI : Power on FAN speed default duty is 60% (PWM) (Default)
 LO : Power on FAN speed default duty is 100% (PWM)



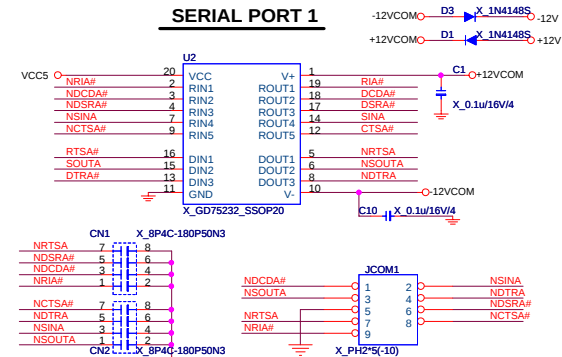
FLOPPY CONNECTOR



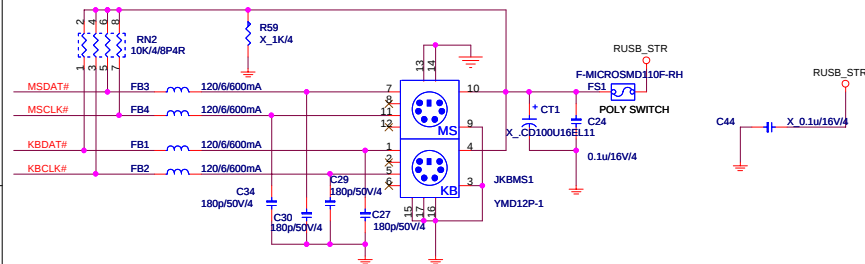
PARALLAL PORT



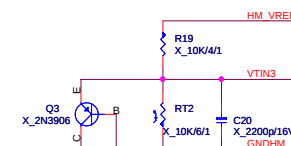
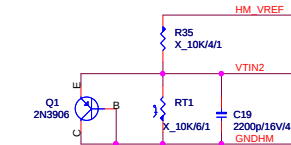
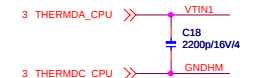
SERIAL PORT 1



PS2 KEYBOARD & MOUSE CONNECTOR



Thermal Resistor



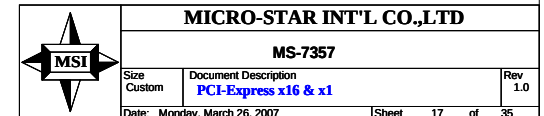
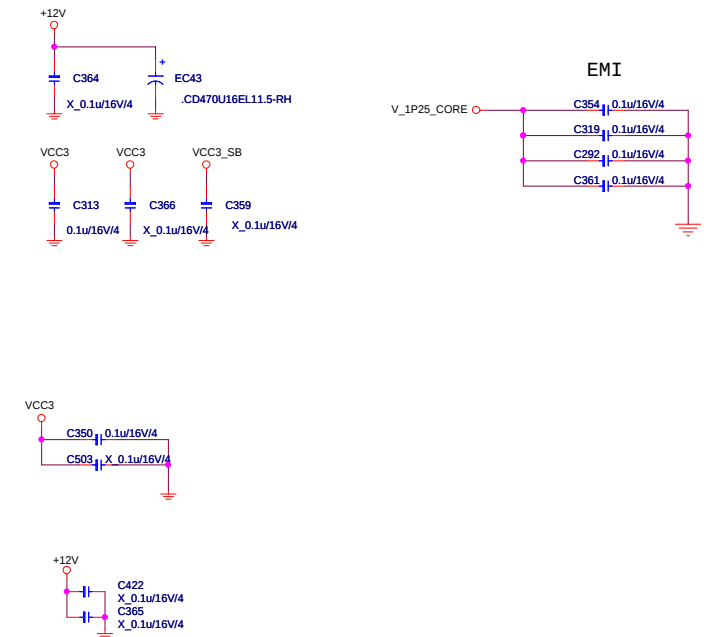
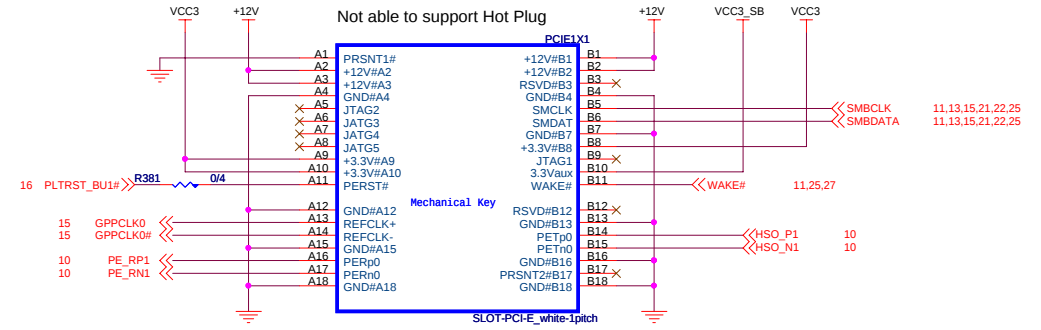
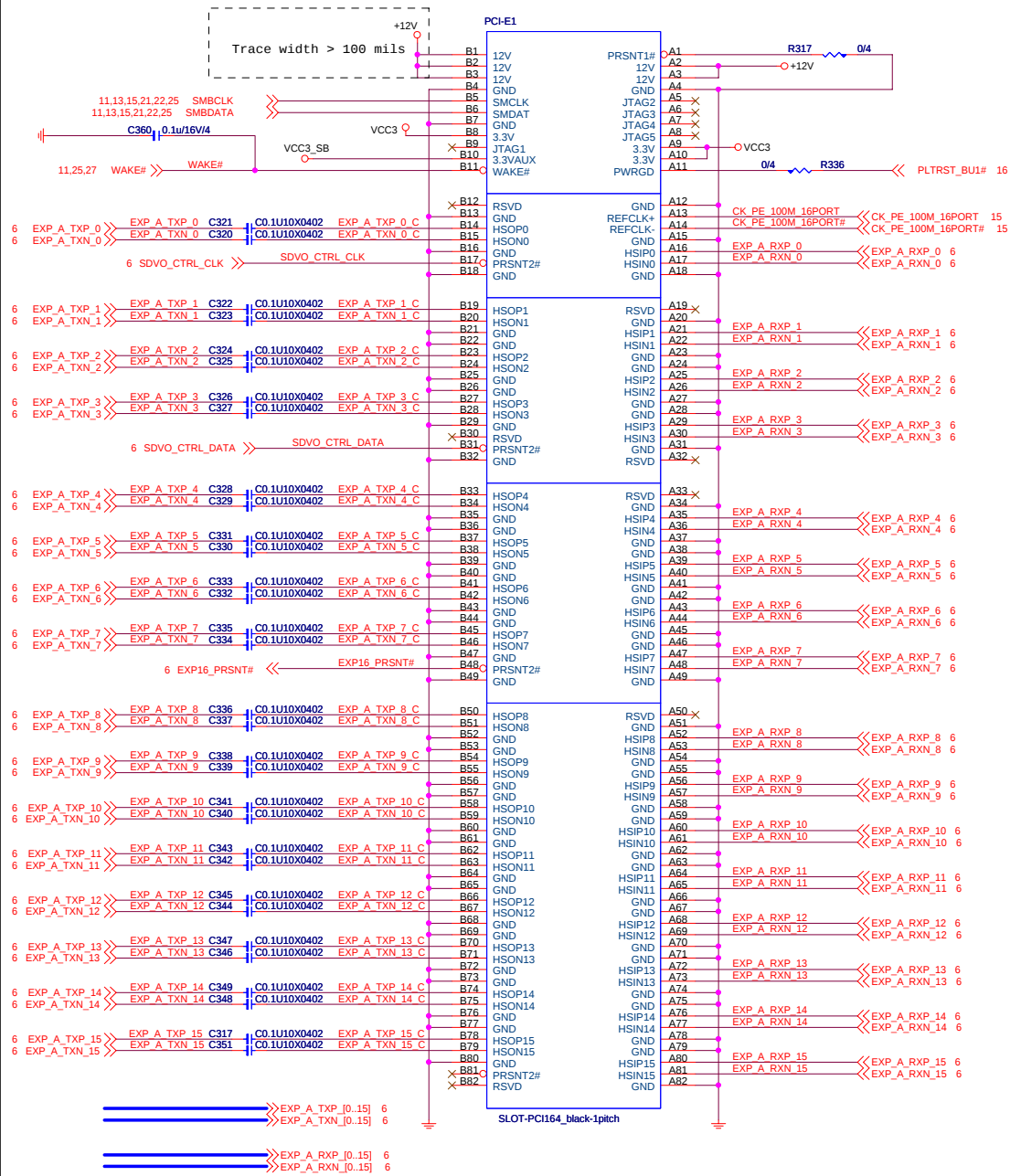
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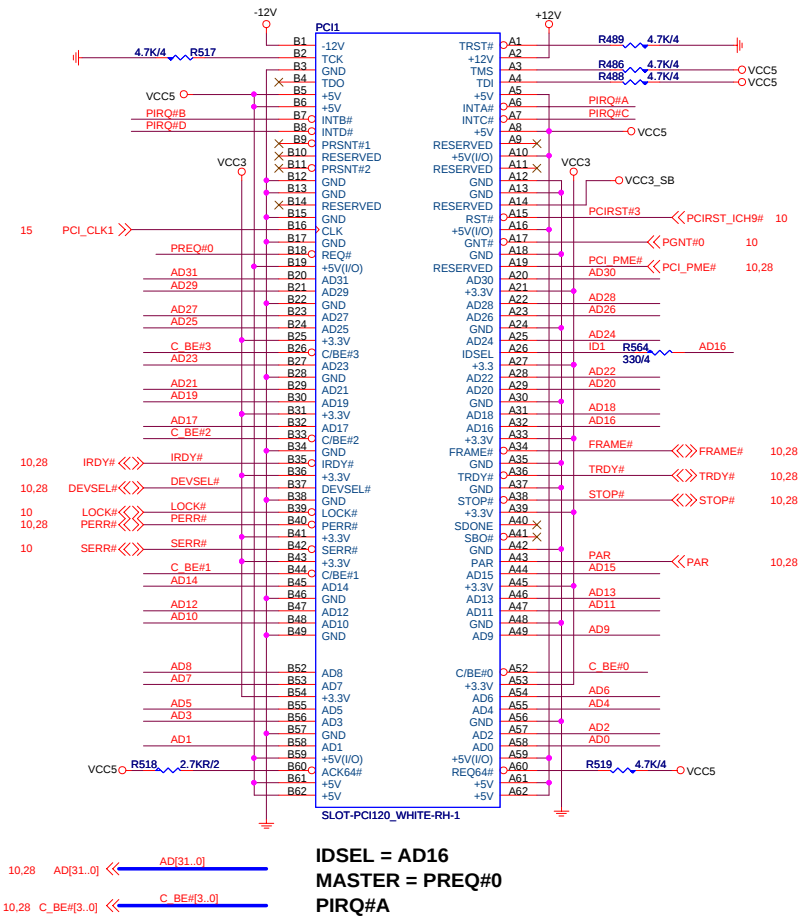
Size	Document Description
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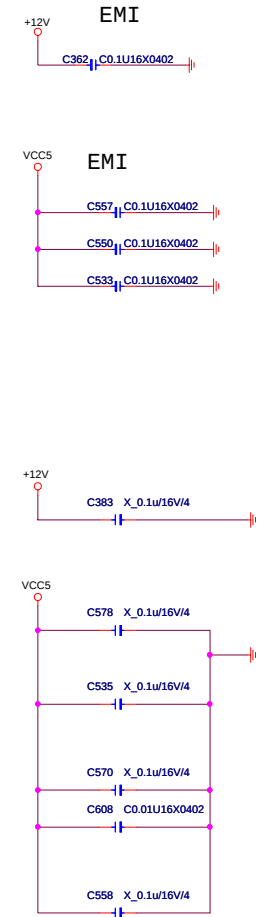
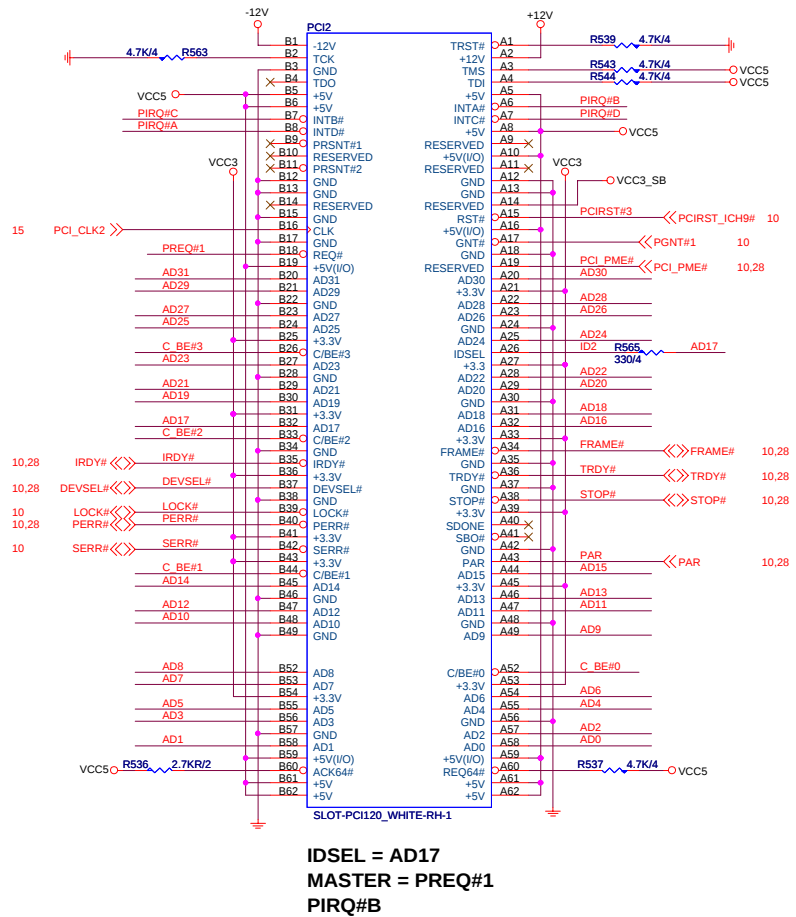
PCI EXPRESS 16-PORT



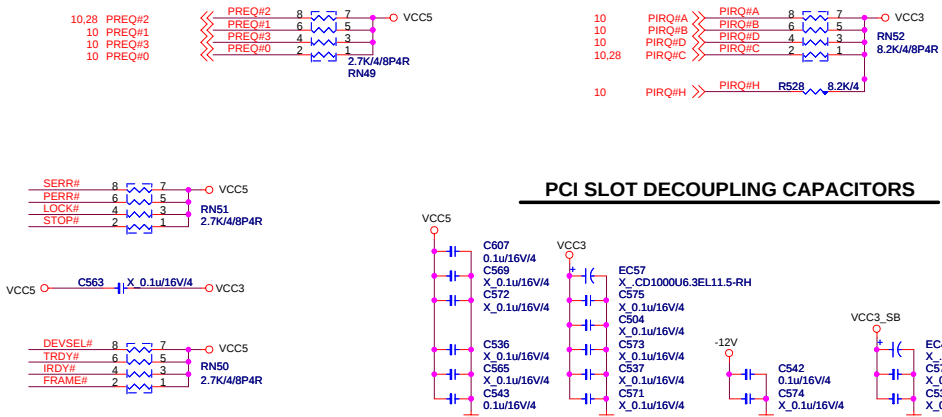
PCI SLOT 1 (PCI VER: 2.2 COMPLY)



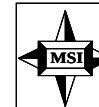
PCI SLOT 2 (PCI VER: 2.2 COMPLY)



PCI PULL-UP / DOWN RESISTORS

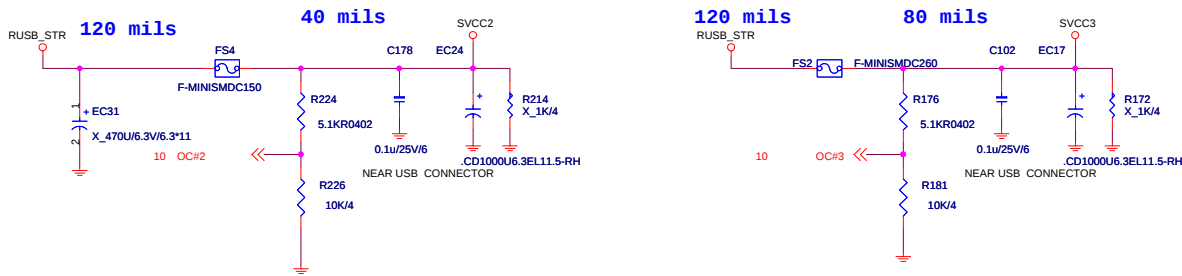


EMI

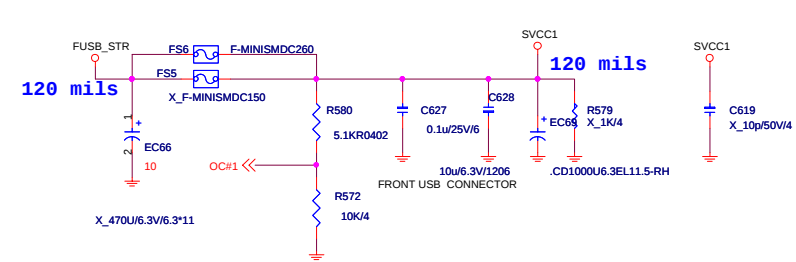


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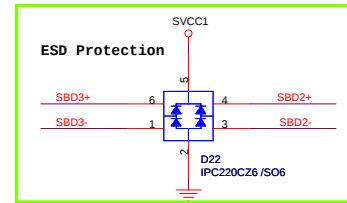
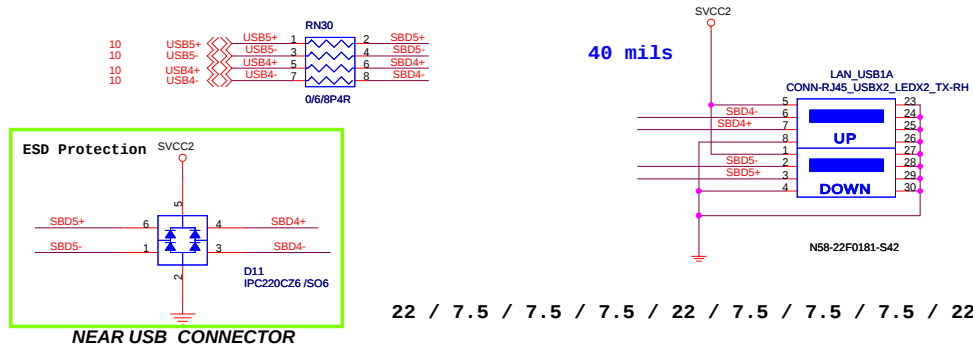
POWER CIRCUIT FOR USB PORT 4-7



POWER CIRCUIT FOR USB PORT 0-3

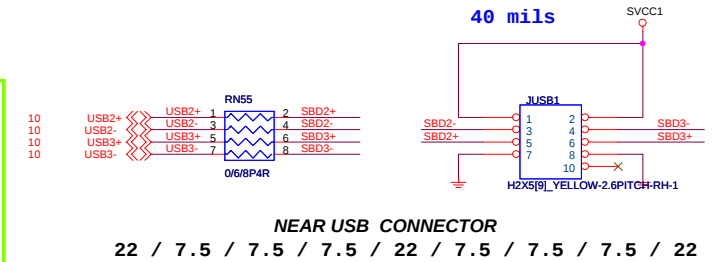


REAR PANEL USB CONNECTOR FOR USB PORT 4,5

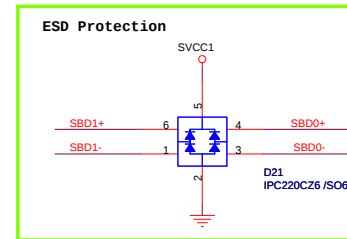
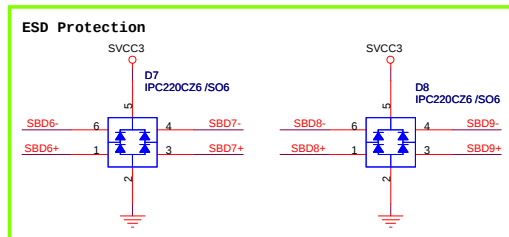
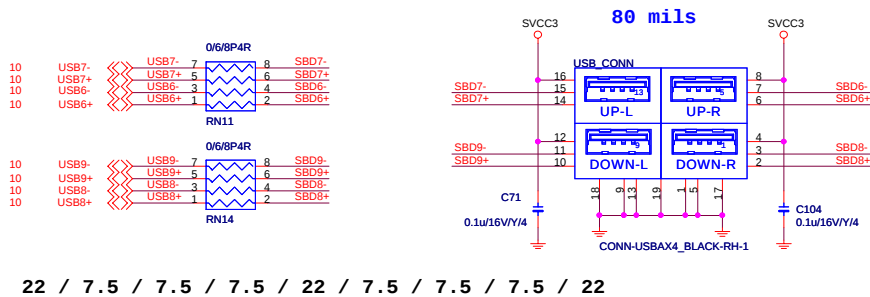


FRONT PANEL USB CONNECTOR FOR USB PORT 2,3

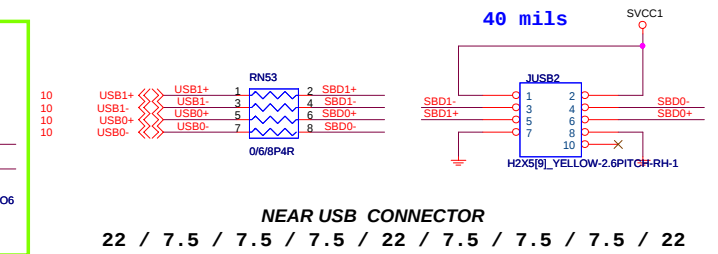
Reserved, can be taken off riser card within bead



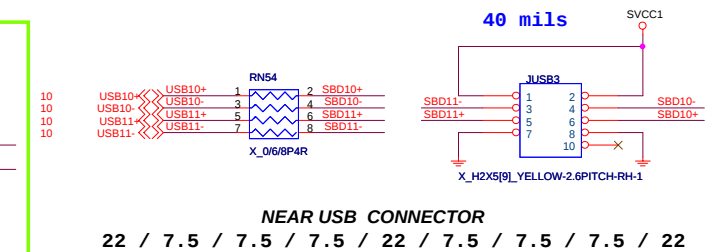
REAR PANEL USB CONNECTOR FOR USB PORT 6,7,8,9



FRONT PANEL USB CONNECTOR FOR USB PORT 0,1

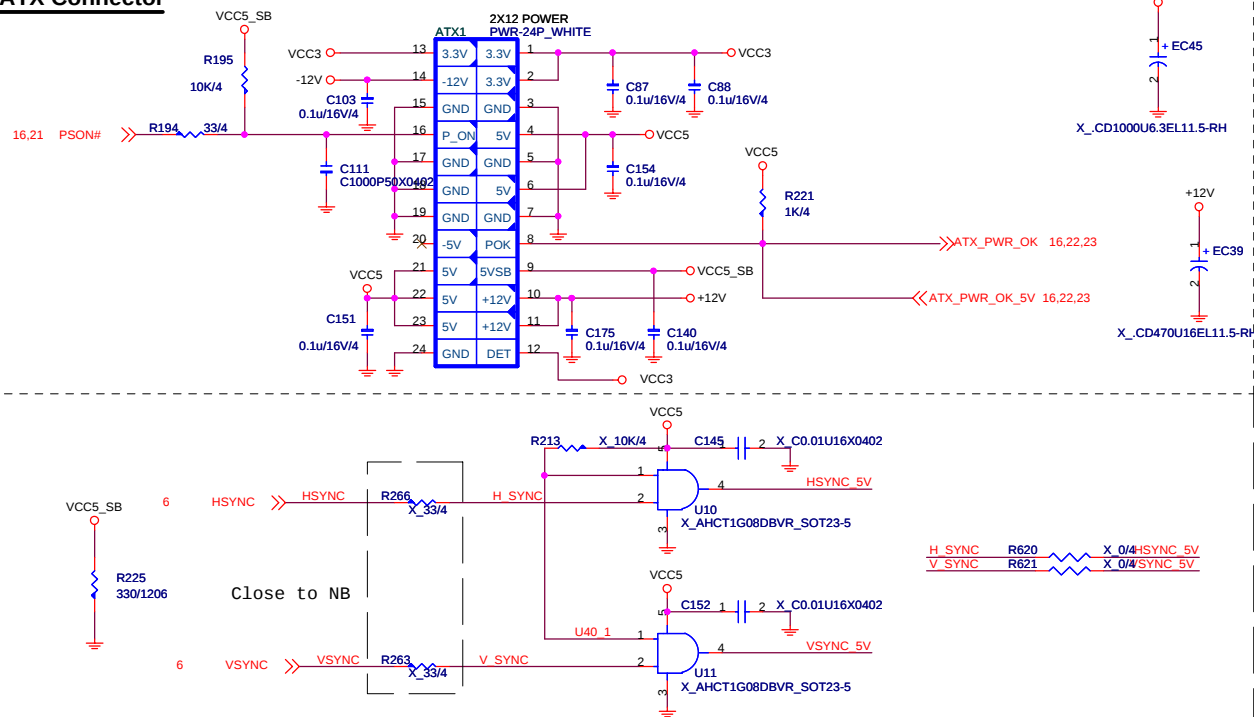


FRONT PANEL USB CONNECTOR FOR USB PORT 0,1

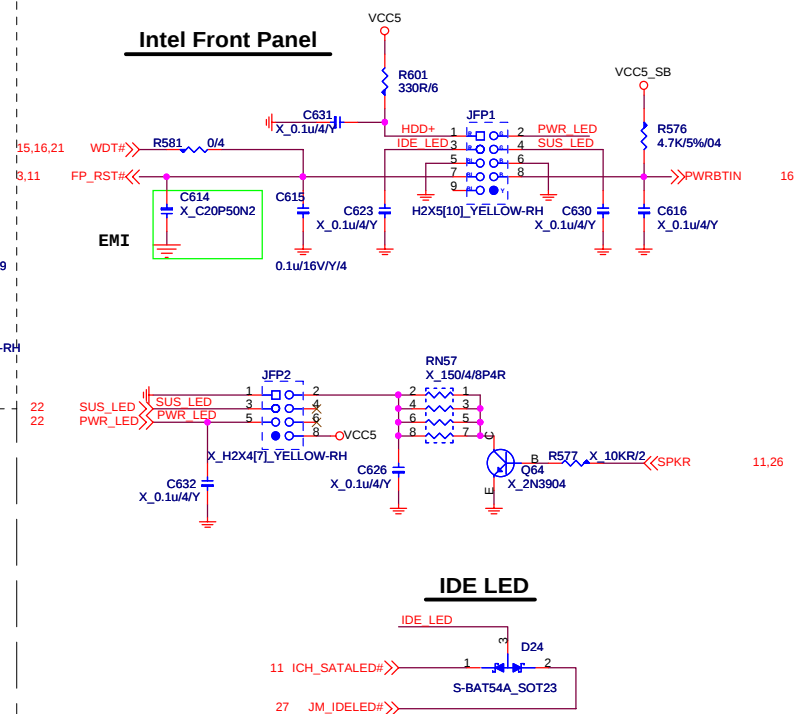


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Custom	USB CONNECTORS	1.0	
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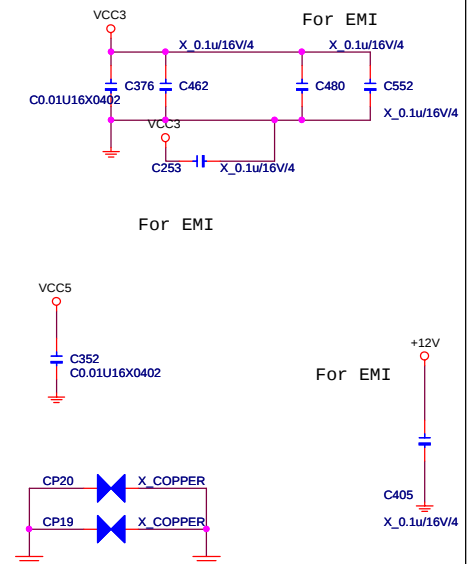
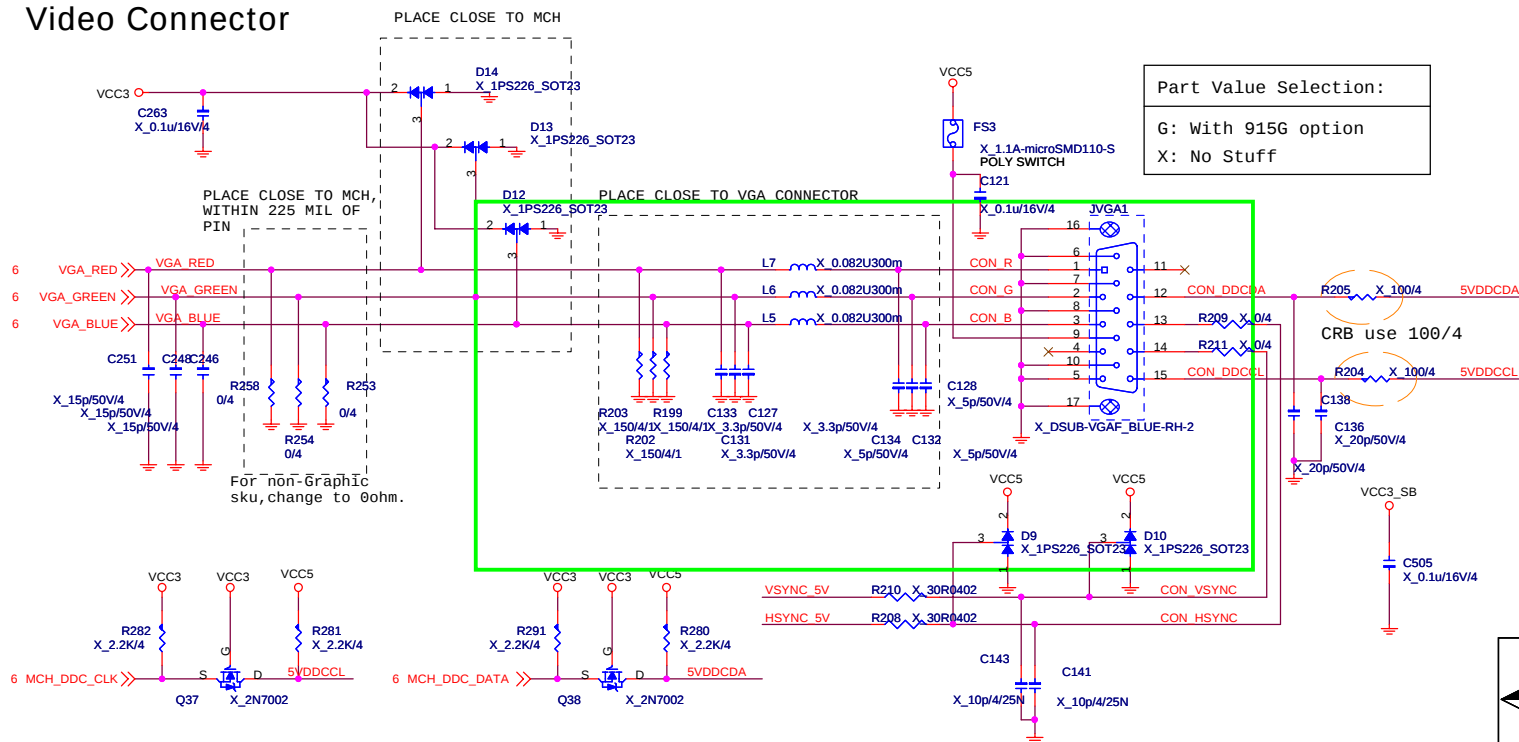
ATX Connector



Intel Front Panel



Video Connector



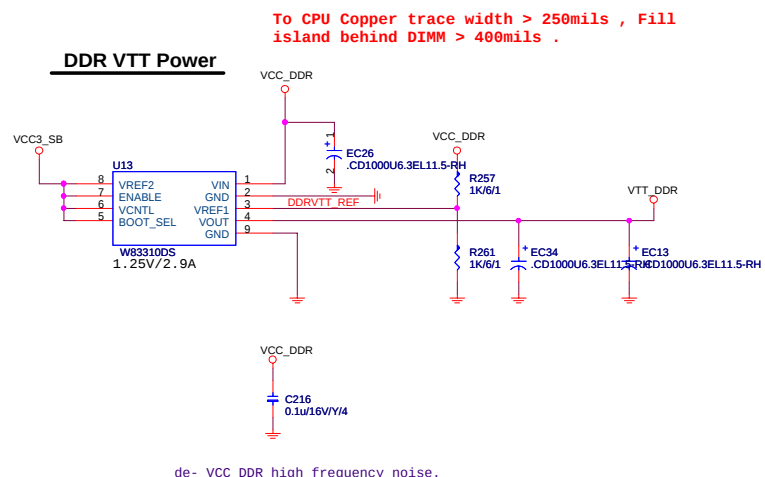
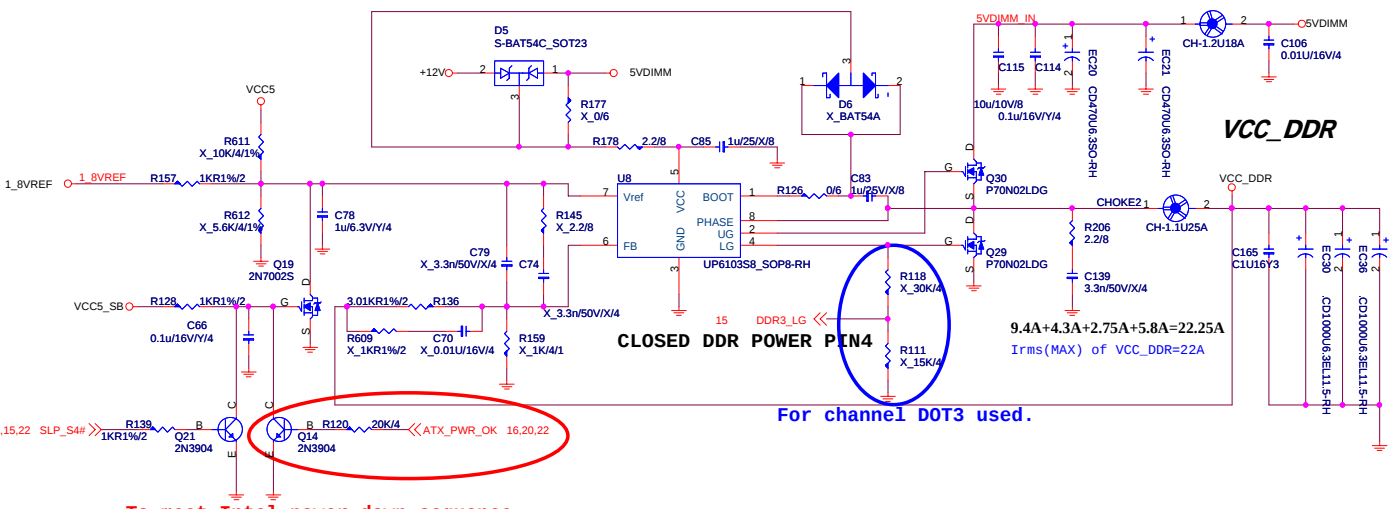
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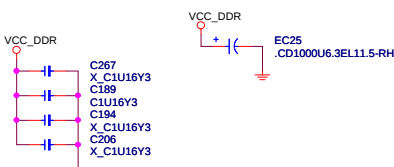
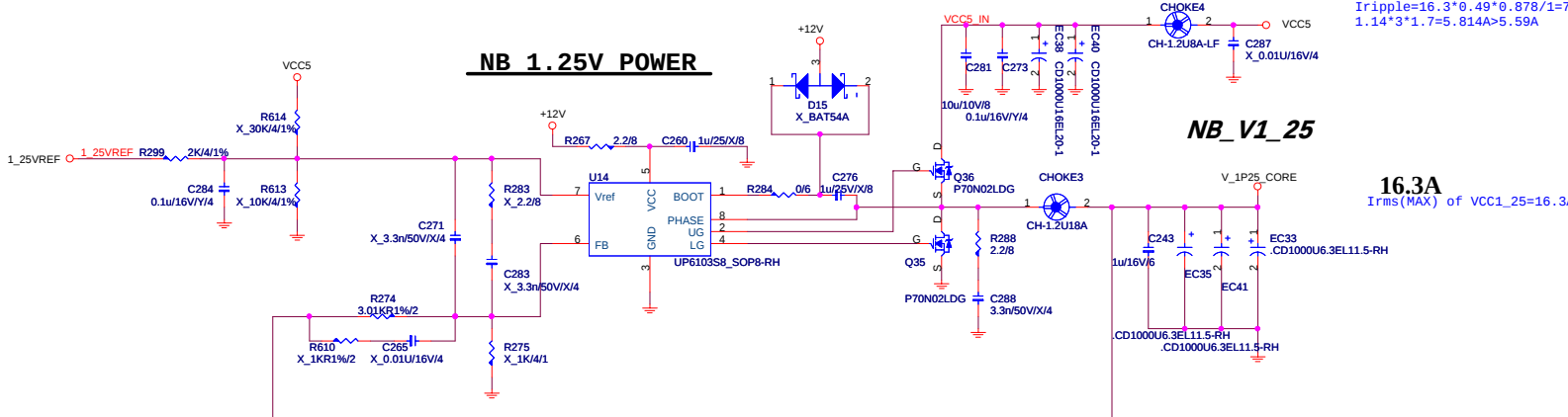
Size Custom	Document Description ATX,Front Panel & VGA Conn	Rev 1.0
Date: Monday, June 04, 2007		Sheet 20 of 35

Rev
1.0

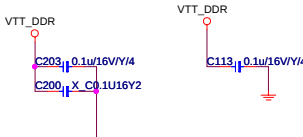
DDR II 1.8V POWER



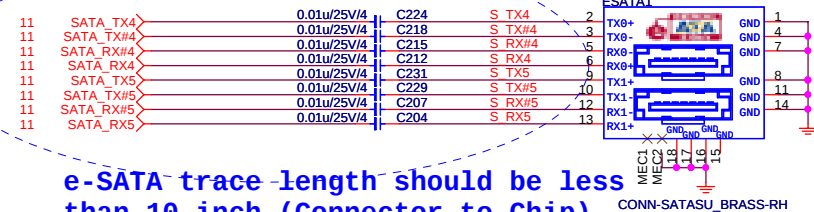
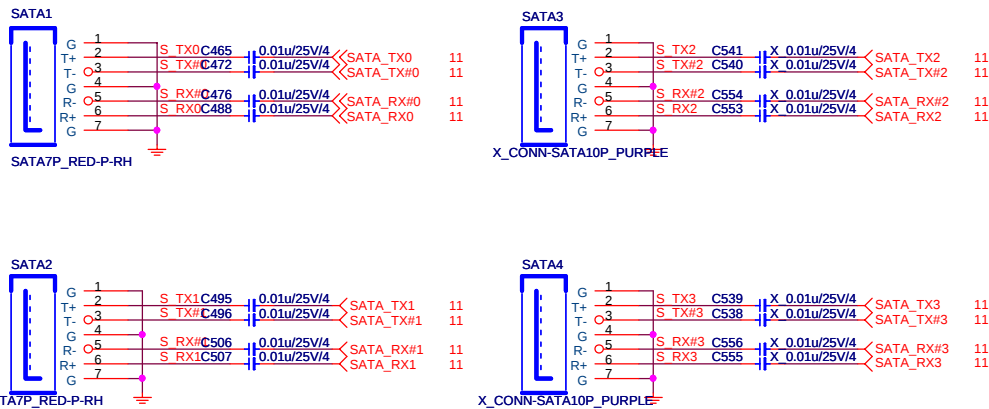
NB 1.25V POWER



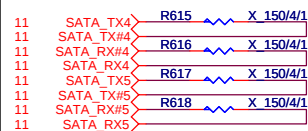
CHANNEL B V_SM_VTT
DECOUPLING CAPS



SERIAL ATA CONNECTOR BLOCK

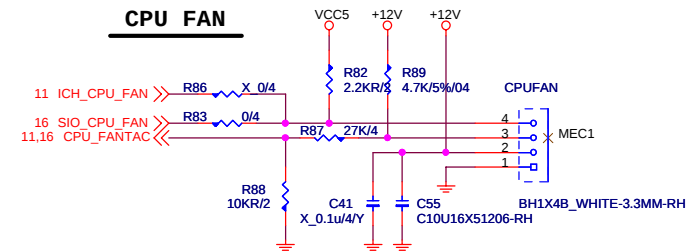


e-SATA trace length should be less than 10 inch.(Connector to Chip)

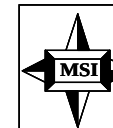
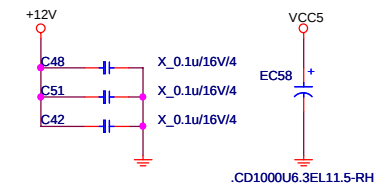
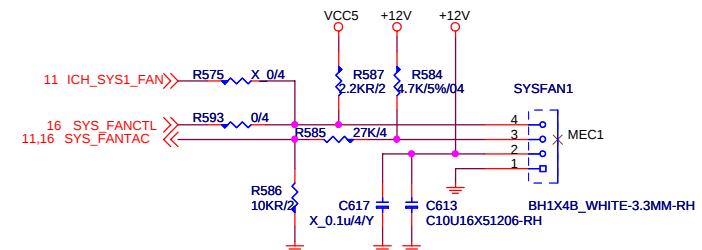


Reserved for EMI

CPU FAN



SYS FAN

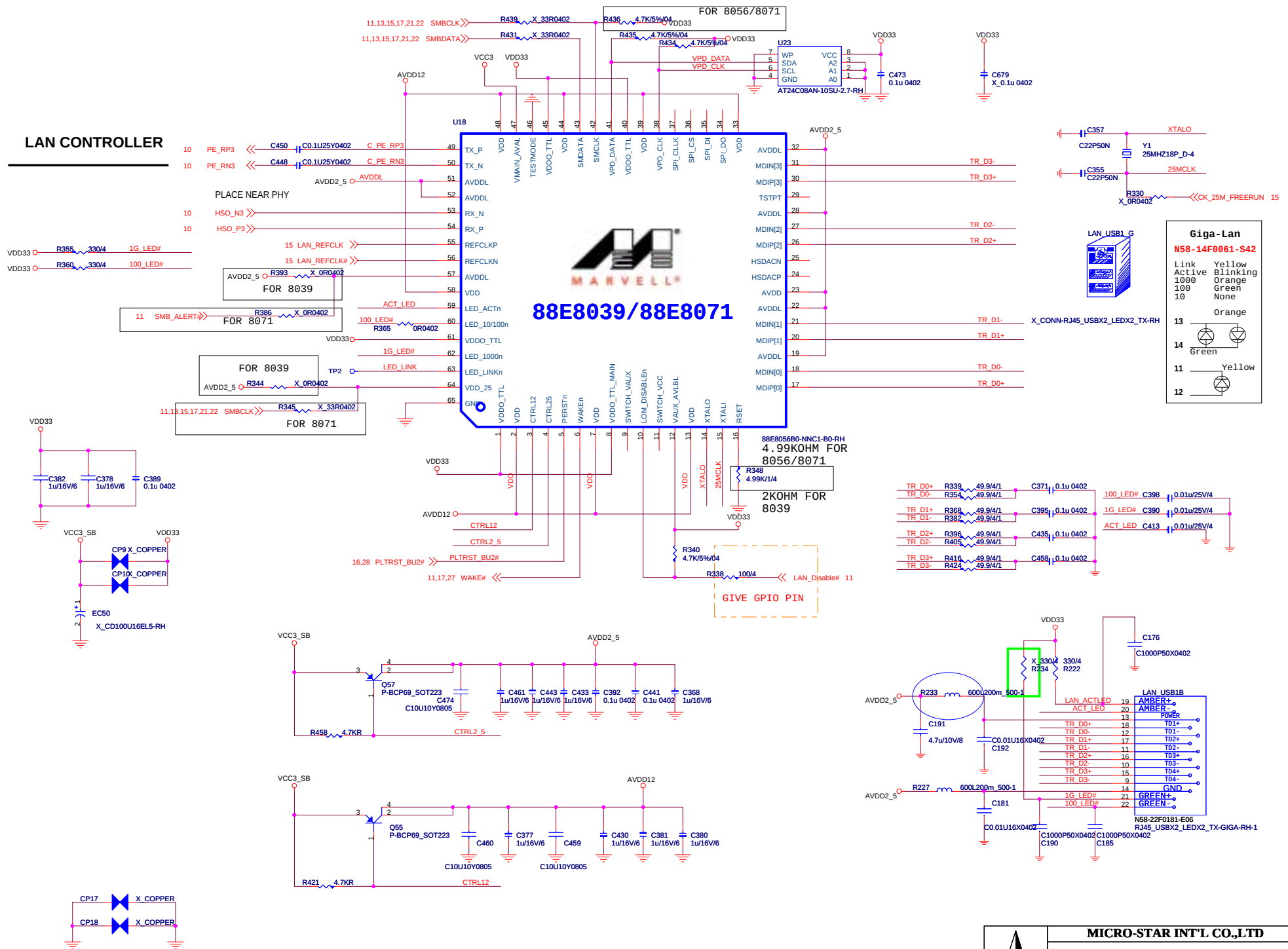


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Size	Document Description	Rev
Custom	FAN & SATA	1.0
Date: Tuesday, May 29, 2007	Sheet 24 of 35	

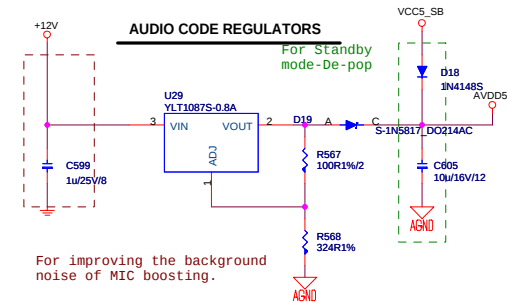
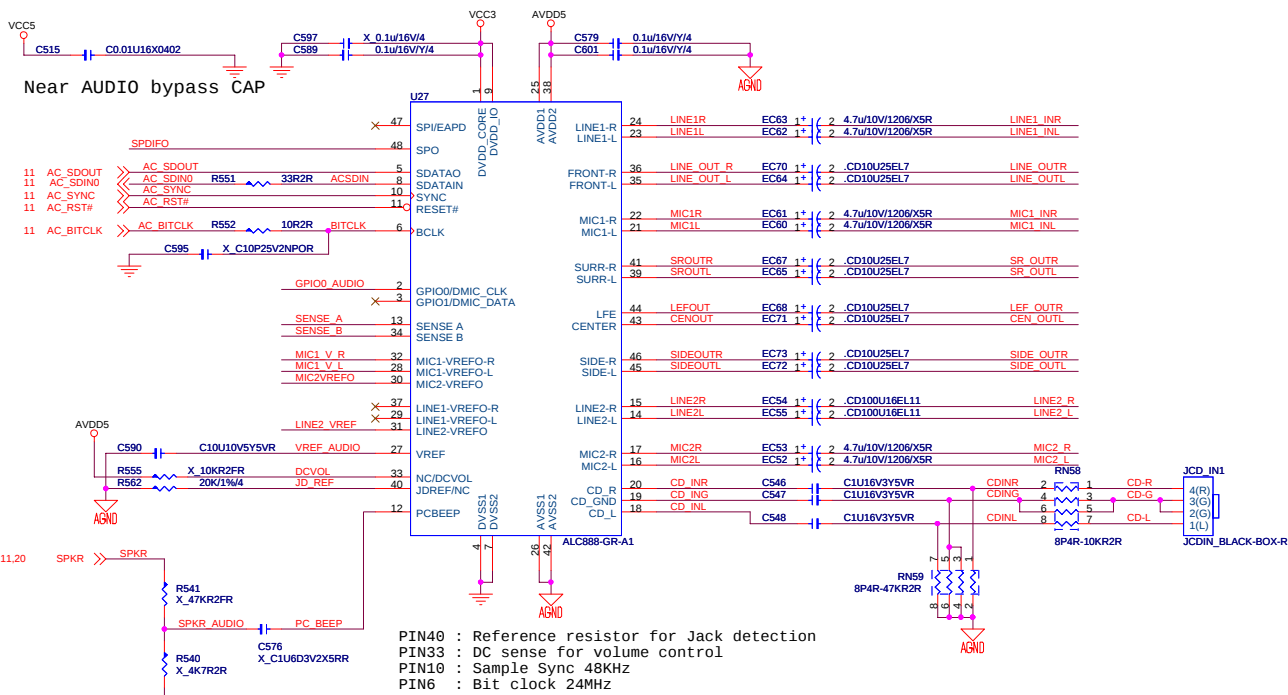
LAN CONTROLLER



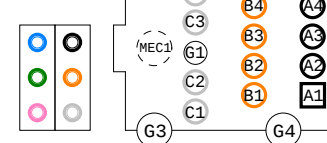
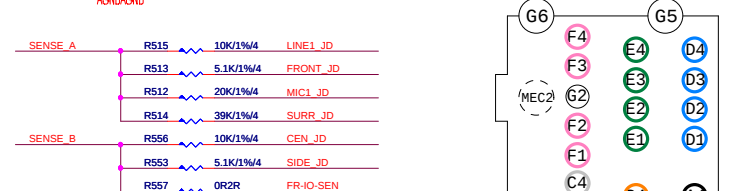
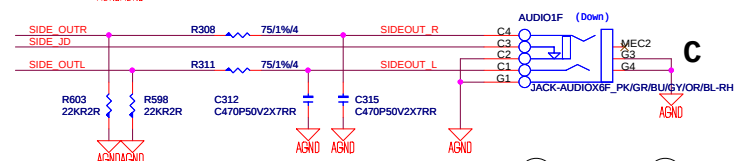
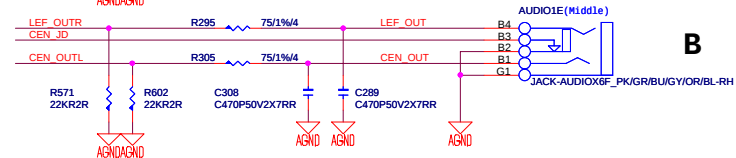
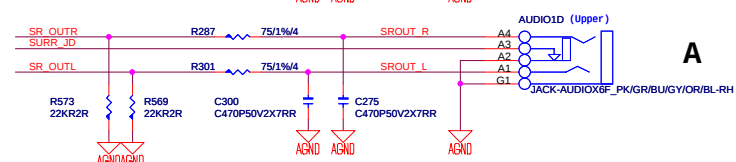
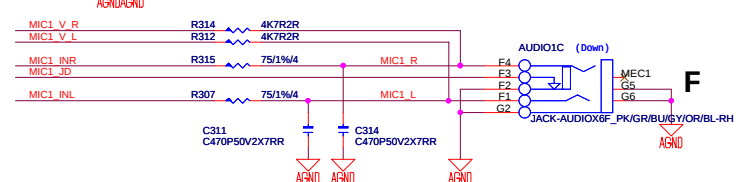
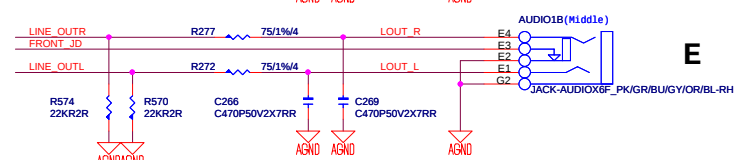
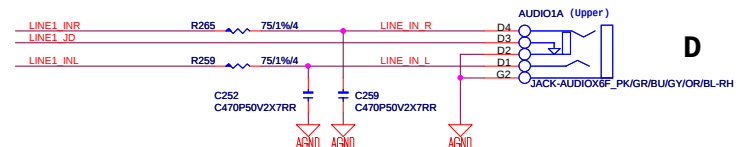
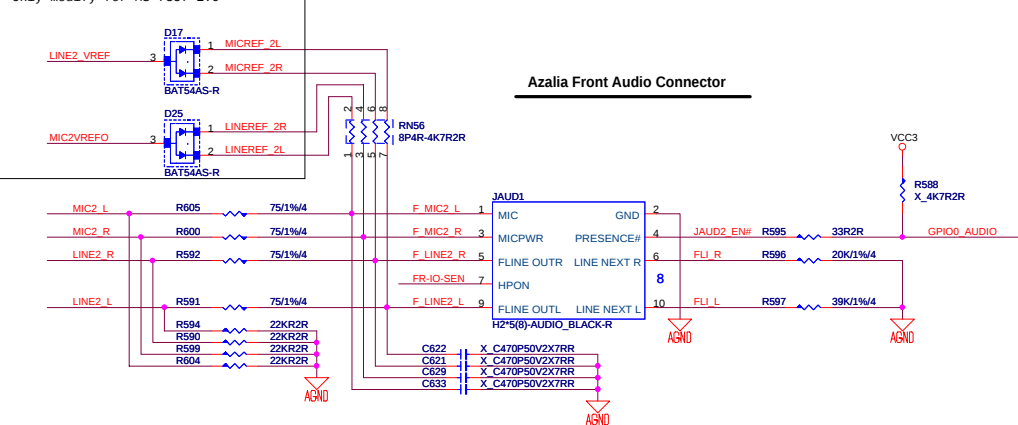
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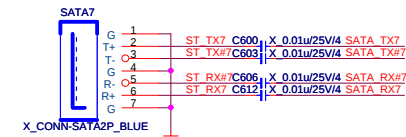
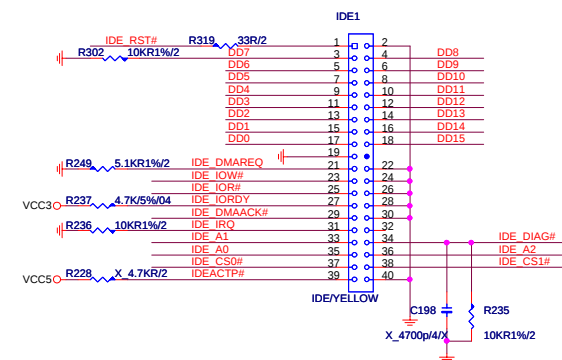
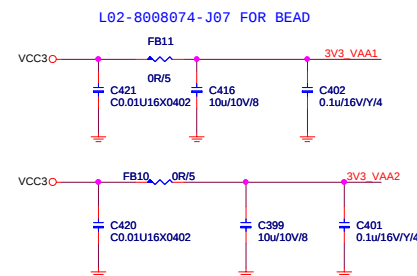
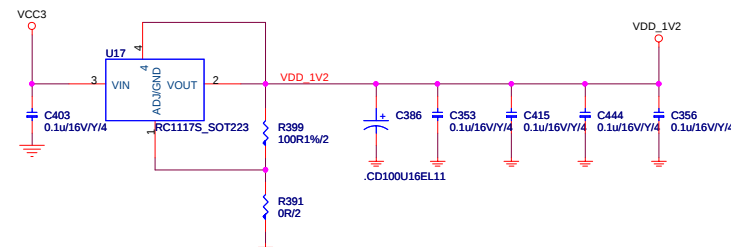
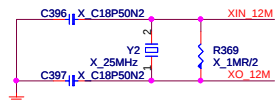
Size	Document Description	Rev
Custom	MARVELL 88E8039 / 56 / 71	1.0
Date: Tuesday, May 29, 2007	Sheet 25 of 35	



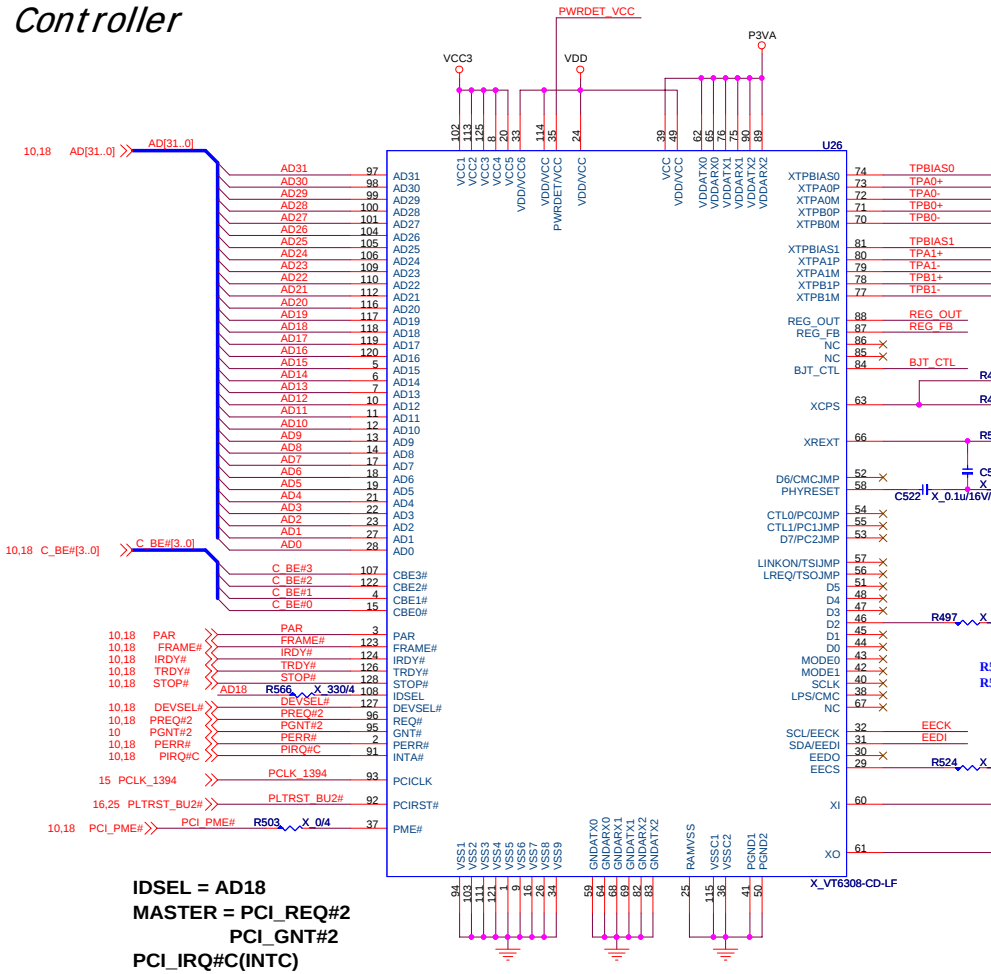
Only modify for MS-7357 1.0



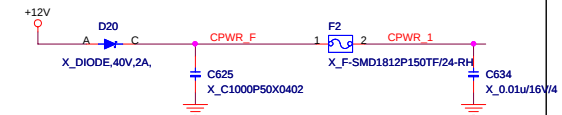
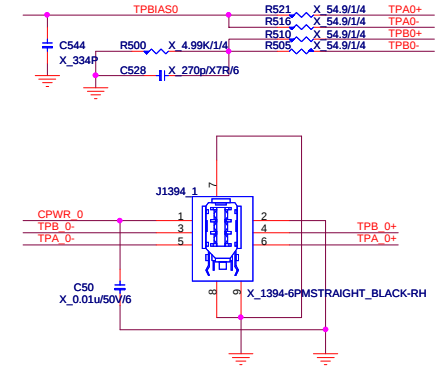
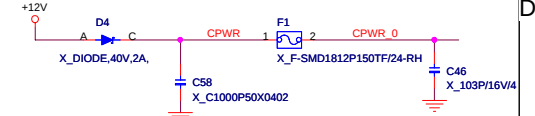
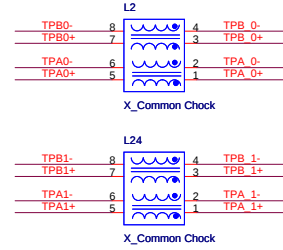
```
REF_CFG[1:0] =  
00:20MHz  
01:25MHz
```



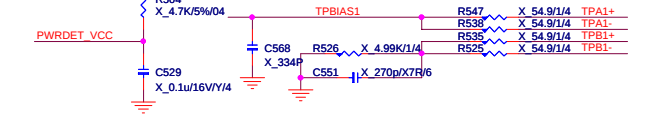
1394a OHCI Link Layer Controller



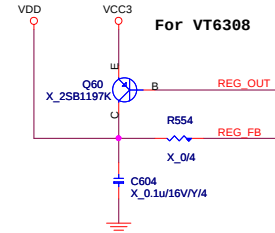
Used 0ohm to instead of common choke



For VT6308



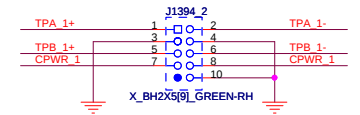
For VT6308



For VT6308



For Intel 1394 pinheader



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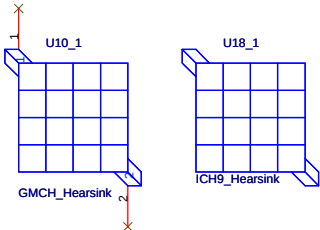
MS-7357

Size	Document Description	Rev
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Date: Tuesday, May 29, 2007	Sheet 28 of 35	

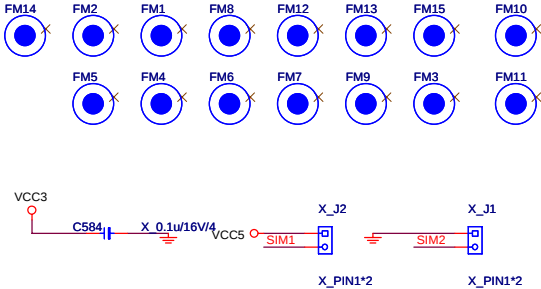
MANUAL PART



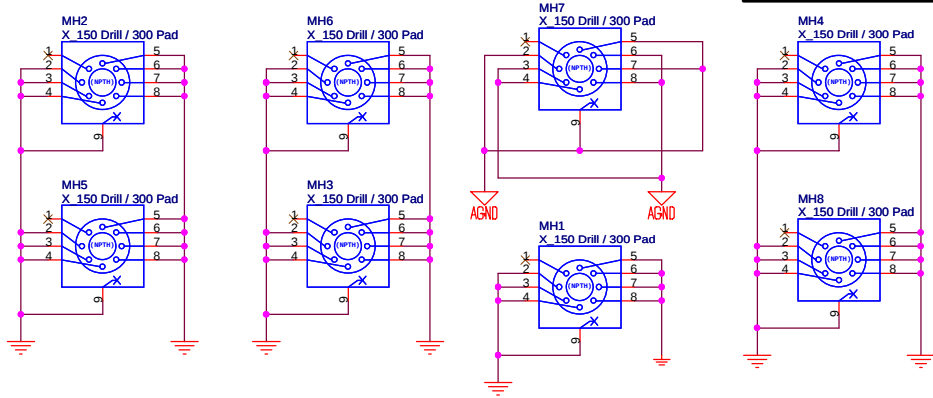
P80-0735710-E48, 競華
P80-0735710-G37, 精成
P80-0735710-D05, 昆穎
P80-0735710-Y34, 元茂



Optical Fiducial Marks



Mounting Holes



ICH9	GPIO	Alt Func	Pin	I/O/NC	Power	PU	ToI	Default	Signal Name or condition
	GPIO[0]	ATADET0	N7	I/O	Vcc3	Y	3.3	INPUT	ATADET0
	GPIO[1]	PULL HIGH	AK21	I/O	Vcc3	Y	3.3	INPUT	PULL HIGH 10K
	GPIO[2]	PIRQ#E	K6	I/O	Vcc3	Y	3.3	INPUT	PULL HIGH 8.2K
	GPIO[3]	PIRQ#F	L7	I/O	Vcc3	Y	3.3	INPUT	PULL HIGH 8.2K
	GPIO[4]	PIRQ#G	F2	I/O	Vcc3	Y	3.3	INPUT	PULL HIGH 8.2K
	GPIO[5]	PIRQ#H	G2	I/O	Vcc3	Y	3.3	INPUT	PULL HIGH 8.2K
	GPIO[6]	PULL HIGH	AH22	I/O	Vcc3	Y	3.3	INPUT	PULL HIGH 10K
	GPIO[7]	PULL HIGH	AK23	I/O	Vcc3	Y	3.3	INPUT	PULL HIGH 10K
	GPIO[8]	ICH_GP8_PU	A20	I/O	Vcc3SB	Y	3.3	INPUT	PULL HIGH 10K
	GPIO[9]	NC	A18	NC	Vcc3	N	3.3	WOL_EN	NC
	GPIO[10]	ICH_GP10_PU	C17	I/O	Vcc3SB	Y	3.3	INPUT	PULL HIGH 10K
	GPIO[11]	SMB_ALERT#	C16	I/O	Vcc3SB	Y	3.3	SMB_ALERT#	PULL HIGH 10K
	GPIO[12]	NC	A8	NC	Vcc3SB	N	3.3	OUTPUT	NC
	GPIO[13]	SI0_PME#	A19	I/O	Vcc3SB	Y	3.3	INPUT	SI0_PME#
	GPIO[14]	ICH_GP14_PU	A9	I/O	Vcc3SB	Y	3.3	INPUT	PULL HIGH 10K
	GPIO[15]	NC	C15	NC	Vcc3SB	Y	3.3	STP_PCI#	NC
	GPIO[16]	NC	M2	NC	Vcc3	Y	3.3	OUTPUT	NC
	GPIO[17]	PULL HIGH	AH21	I/O	Vcc3	Y	3.3	INPUT	PULL HIGH 10K
	GPIO[18]	NC	K1	NC	Vcc3	N	3.3	OUTPUT	NC
	GPIO[19]	SATA1GP_PU	AE20	I/O	Vcc3	Y	3.3	INPUT	PULL HIGH 10K
	GPIO[20]	NC	AF5	NC	Vcc3	N	3.3	OUTPUT	NC
	GPIO[21]	SATA0GP_PU	AK25	I/O	Vcc3	Y	3.3	INPUT	PULL HIGH 10K
	GPIO[22]	ICH_SGP22_PU	AJ24	I/O	Vcc3	Y	3.3	INPUT	PULL HIGH 10K
	GPIO[23]	LDRQ_1#	J3	I/O	Vcc3	Y	3.3	LDRQ_1#	PULL HIGH 10K
	GPIO[24]	NC	A14	NC	Vcc3SB	N	3.3	OUTPUT	NC
	GPIO[25]	NC	B18	NC	Vcc3SB	N	3.3	STP_CPU#	NC
	GPIO[26]	NC	C11	NC	Vcc3SB	N	3.3	S4_STATE#	NC
	GPIO[27]	NC	A11	NC	Vcc3SB	N	3.3	QRT_STATE0	NC
	GPIO[28]	NC	G18	NC	Vcc3SB	N	3.3	QRT_STATE1	NC
	GPIO[29]	OC#2	N1	I/O	Vcc3SB	Y	3.3	OC#2	OC#2
	GPIO[30]	OC#3	N5	I/O	Vcc3SB	Y	3.3	OC#3	OC#3
	GPIO[31]	OC#3	M1	I/O	Vcc3SB	Y	3.3	OC#3	OC#3
	GPIO[32]	SPI_WP#	K2	I/O	Vcc3	N	3.3	OUTPUT	SPI_WP#
	GPIO[33]	SPI_HOLD_GP0#	AF6	I/O	Vcc3	N	3.3	OUTPUT	SPI_HOLD_GP0#
	GPIO[34]	LAN_Disable#	AH5	I/O	Vcc3	N	3.3	OUTPUT	LAN_Disable#
	GPIO[35]	NC	L1	NC	Vcc3	N	3.3	OUTPUT	NC
	GPIO[36]	SATA2GP_PU	AE21	I/O	Vcc3	Y	3.3	INPUT	SATA2GP_PU
	GPIO[37]	SATA3GP_PU	AE22	I/O	Vcc3	Y	3.3	INPUT	SATA3GP_PU
	GPIO[38]	ICH_SGP38_PU	AK24	I/O	Vcc3	Y	3.3	INPUT	ICH_SGP38_PU
	GPIO[39]	ICH_SGP39_PD	AH23	I/O	Vcc3	Y	3.3	SDATAOUT0	ICH_SGP39_PD
	GPIO[40]	OC#1	N3	I/O	Vcc3SB	Y	3.3	OC#1	OC#1
	GPIO[41]	OC#1	P7	I/O	Vcc3SB	Y	3.3	OC#1	OC#1
	GPIO[42]	OC#1	R7	I/O	Vcc3SB	Y	3.3	OC#1	OC#1
	GPIO[43]	OC#2	N2	I/O	Vcc3SB	Y	3.3	OC#2	OC#2
	GPIO[44]	OC#3	P3	I/O	Vcc3SB	Y	3.3	OC#3	OC#3
	GPIO[45]	OC#3	R6	I/O	Vcc3SB	Y	3.3	OC#3	OC#3
	GPIO[46]	PULL HIGH	T7	I/O	Vcc3SB	Y	3.3	OC#	PULL HIGH 10K
	GPIO[47]	PULL HIGH	P1	I/O	Vcc3SB	Y	3.3	OC#	PULL HIGH 10K
	GPIO[48]	ICH_SGP48_PD	AD20	I/O	Vcc3	Y	3.3	SDATAOUT1	PULL HIGH 10K
	GPIO[49]	DMI_STRAP	AJ25	I/O	Vcc3	N	3.3	OUTPUT	PULL LOW 2.2K
	GPIO[50]	PREQ#1	G13	I/O	Vcc5	Y	5.5	PREQ#1	PULL HIGH 2.7K
	GPIO[51]	NC	A7	I/O	Vcc3	N	3.3	PGNT#1	NC
	GPIO[52]	PREQ#2	F13	I/O	Vcc5	Y	5.5	PREQ#2	PULL HIGH 2.7K
	GPIO[53]	PGNT#2	C7	I/O	Vcc3	N	3.3	PGNT#2	STRAP PIN
	GPIO[54]	PREQ#3	G8	I/O	Vcc5	Y	5.5	PREQ#3	PULL HIGH 2.7K
	GPIO[55]	PGNT#3	F7	I/O	Vcc3	N	3.3	PGNT#3	STRAP PIN
	GPIO[56]	ICH_GP56_PU	F16	I/O	Vcc3SB	Y	3.3	GPIO_SEL	PULL HIGH 10K
	GPIO[57]	ICH_GP57_PU	C12	I/O	Vcc3SB	Y	3.3	INPUT	PULL HIGH 10K
	GPIO[58]	SPI_CS1#	F23	I/O	Vcc3SB	Y	3.3	SPI_CS1#	SPI_CS1#
	GPIO[59]	OC#1	P5	I/O	Vcc3SB	Y	3.3	OC#1	OC#1
	GPIO[60]	LINK_ALERT#	F18	I/O	Vcc3SB	Y	3.3	LINK_ALERT#	LINK_ALERT#

PCI Config.

DEVICE	Interrupt Request Pin	REQ# /GNT#	IDSEL	CLOCK
PCI1	PIRQ#A PIRQ#B PIRQ#C PIRQ#D	PREQ#0 PGNT#0	AD16	PCI_CLK1
PCI2	PIRQ#B PIRQ#C PIRQ#D PIRQ#A	PREQ#1 PGNT#1	AD17	PCI_CLK2
IEEE-1394	PIRQ#C	PREQ#2 PGNT#2	AD18	PCI_CLK3

DDRII DIMM Config.

DEVICE	ADDRESS	CLOCK
DIMM 1	A0H	MCLK_A0/MCLK_A#0 MCLK_A1/MCLK_A#1 MCLK_A2/MCLK_A#2
DIMM 2	A2H	MCLK_A1/MCLK_A#3 MCLK_A2/MCLK_A#4 MCLK_A2/MCLK_A#5
DIMM 3	A4H	MCLK_B0/MCLK_B#0 MCLK_B2/MCLK_B#1 MCLK_B1/MCLK_B#2
DIMM 4	A6H	MCLK_B0/MCLK_B#3 MCLK_B1/MCLK_B#4 MCLK_B2/MCLK_B#5

JUMPER SETTING

JBAT1	(1-2)NORMAL	(2-3)CLEAR
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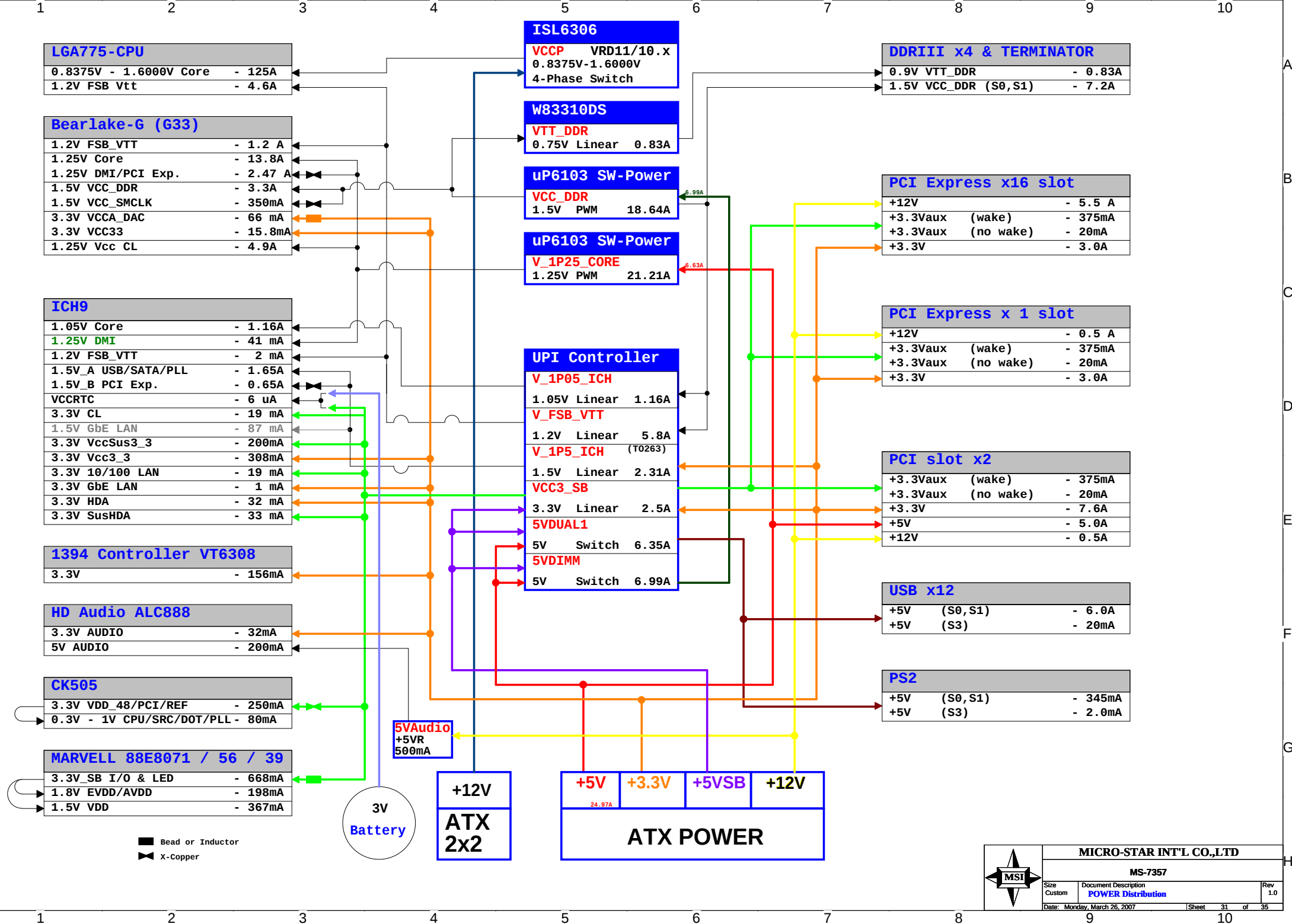
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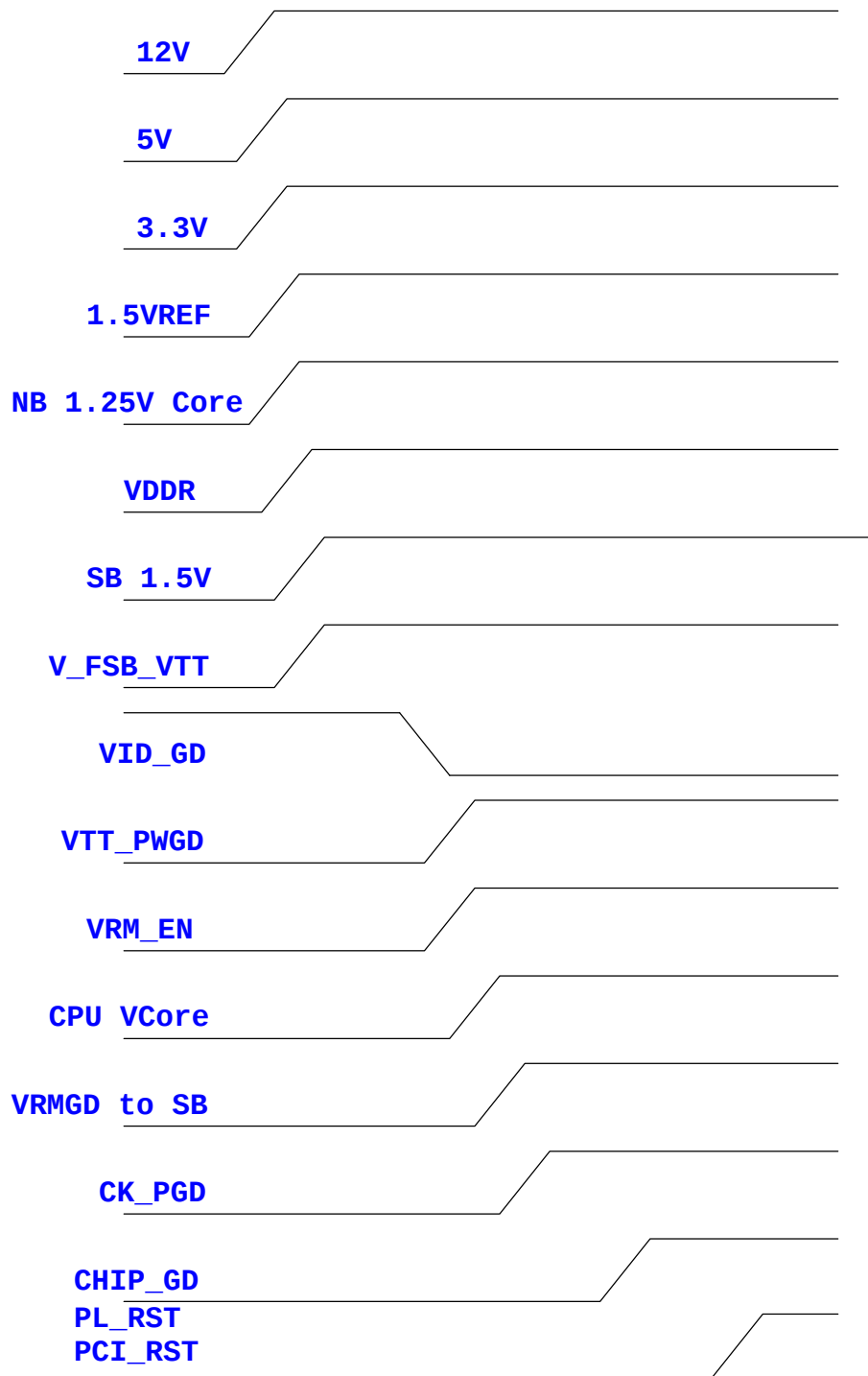
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GPIO & Jumper setting

Rev 1.0

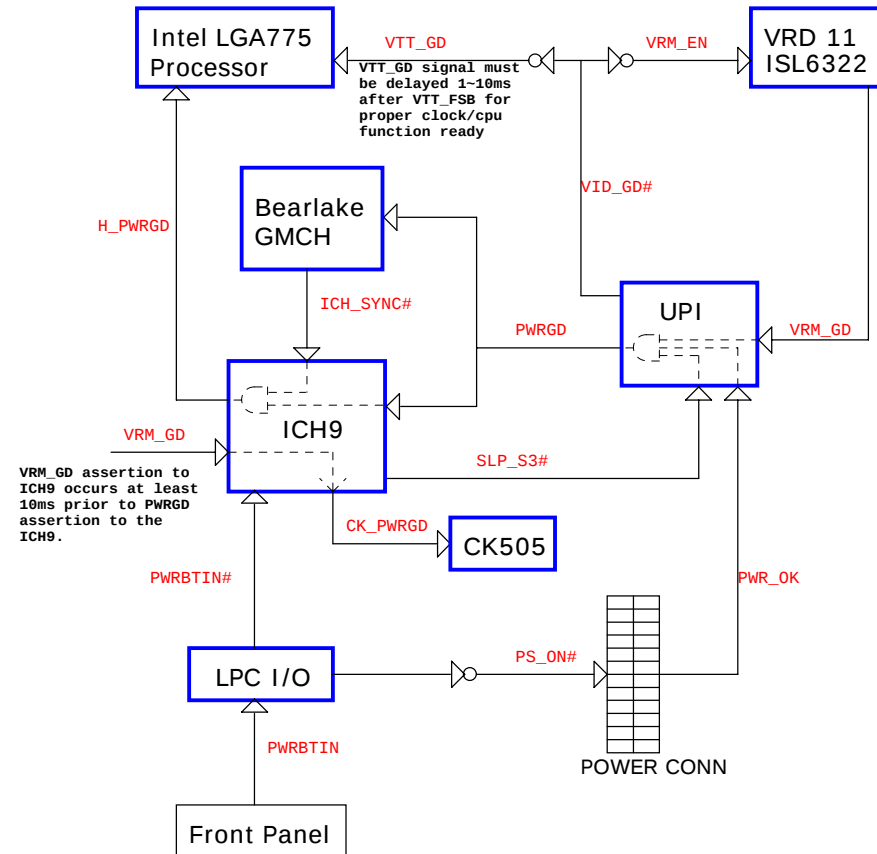
Date: Monday, March 26, 2007

Sheet 30 of 35





PWROK MAP

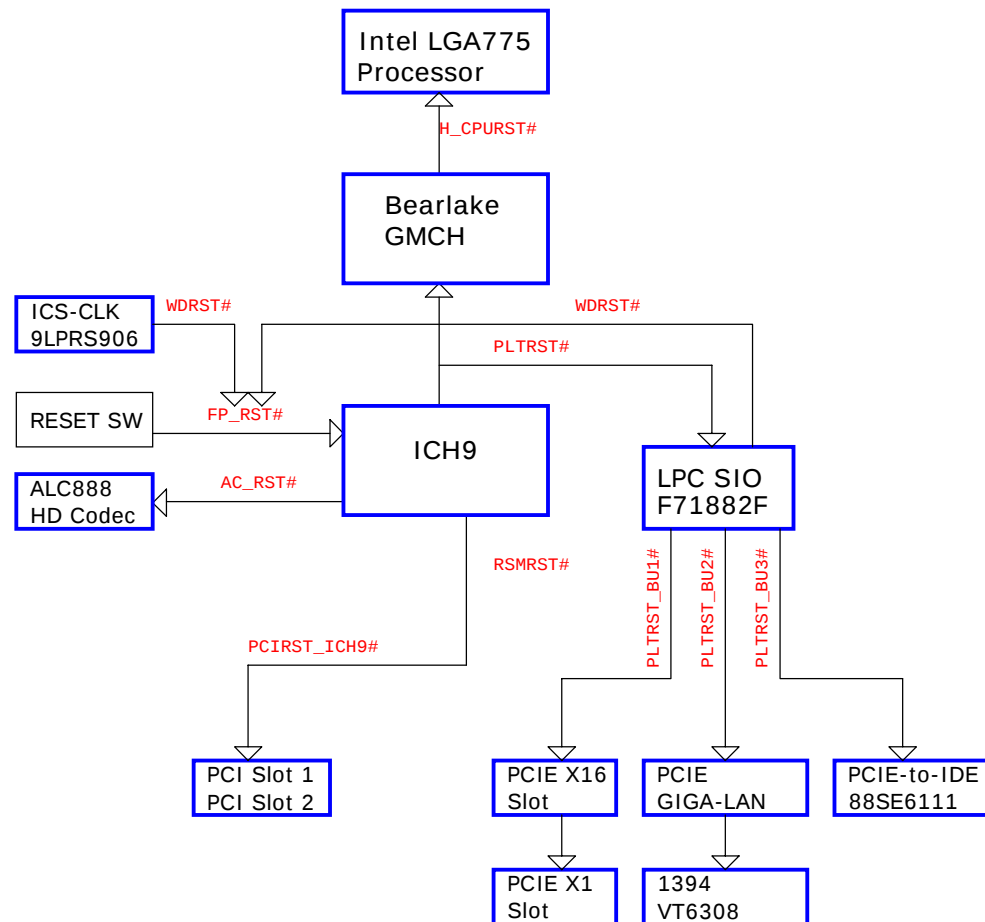


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RESET MAP



MICRO-STAR INT'L CO.,LTD

MS-7357

Size Custom	Document Description RESET MAP	Rev 1.0
Date: Monday, March 26, 2007	Sheet 33 of 35	

0A change to 1.0

2007/03/19

1. Page15 : CLOCK GEN NEW P/N UPDATE TO ver: C (I11-RS90622-I02).
2. Page16 : COM port connector change to N51-09M0091-A10 , channel suggestion part.
3. Page16 : Remove beep circuit with F71882.
4. Page11 : Add a pull-hi to VCC5_ SB resistor(4.7K) for RSMRST# (R578).
5. Page22 : Reserve option resistor for UP7501 pin6, to select control by SLP_S4# or SLP_S5# (R607,R608).
6. Modify power solution.(Page21,22,23)
 - 1). Uninstall parts (R44 , RT3 , R10).
 - 2). R9 change to 0ohm.
 - 3). R48 install 82.5K resistor.
 - 4). C17 change to 33pf.
 - 5). R11 change to 2.49K ohm.
 - 6). R12 change to 15K ohm.
 - 7). C400,C432 change to 0.1uF.
 - 8). R343 install a 20K ohm resistor.
 - 9). R388 change to 4.22K ohm.
 - 10). R387 change to 1K ohm.
 - 11). Remove C230 , C624 , C70 , C265.
 - 12). R164 change to 510 ohm.
 - 13). R160 change to 10K ohm.
 - 14). R299 change to 2K ohm.
 - 15). C78 change to 1uF.
7. Page15 : Uninstall F75133 circuit.

2007/03/28

1. Page26 : D17 pin3 connect to LINE2_VREF & D25 pin3 connect to MIC2VREF0.

2007/03/30

1. Page23 : EC20,EC21,EC40,EC38 change footprint to 560UF_4V_R71D55.
2. Page20 : Add 2 resistors for H_SYNC & V_SYNC.
3. Page10-12 : SB change to ICH9.
4. Page24 : Uninstall SATA3 & SATA4.
5. Page10 : R534 change to 22 ohm 0402 1%.
6. Page6 : Follow Intel suggestion document to set CPU_GTLREF[3:0] to 63.5%.

2007/05/07

1. Modify part number to meet channel's suggestion.
 - 1). JVGAI change to N51-15F0391-F02 .
 - 2). DIMM_A1 & DIMM_A2 change to N13-2400301-L06.
 - 3). DIMM_A1 & DIMM_A2 change to N13-2400351-L06.
 - 4). LAN_USB1 change to N58-22F0181-E06.
2. Page16 : FDD1 change to N32-2174011-H06.
3. Page16 : FS1 change to D08-0100200-P16.
4. Page21 : Uninstall R48 and install R44 with 39.2K 1%.
5. Modify power team solution.
 - 1). R12 change to 18K.
 - 2). Install 100ohm resistor on R29.
 - 3). Install 220pF cap on C9.
 - 4). C17 change to 15pf.
 - 5). R27 change to 90.9ohm.
 - 6). R95 change to 20ohm.
 - 7). R28 change to 10ohm.
 - 8). Uninstall EC(2,5,6) & C(109,676).

2007/05/15

1. Page27 : SATA5 location name change to SATA7.
2. Page6-9 : Northbridge change new P/N to B01-LE82G25-I06.
3. Page16 : FS1 change to D08-0100210-P16 (RoHS).

2007/05/29 Create a new BOM for OEM customer Dixon.

1. Page16 : Remove JCOM1 & FDD1.
2. Page24 : SATA1 & SATA2 change color to RED (N5N-07M0311-H06).
3. Page27 : Remove SATA7.
4. Page11 : Remove JSPD1.
5. Page28 : Remove IEEE1394.
6. Page19 : Remove USB3.
7. Page6 & 20 : Remove onboard VGA function.

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