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LCD TV

Schematics & Exploded View with P/N

CHASSIS : LA12C

MODEL : 55LW5700 55LW5700-UE

CAUTION
BEFORE SERVICING THE CHASSIS,
READ THE SAFETY PRECAUTIONS IN THIS MANUAL.

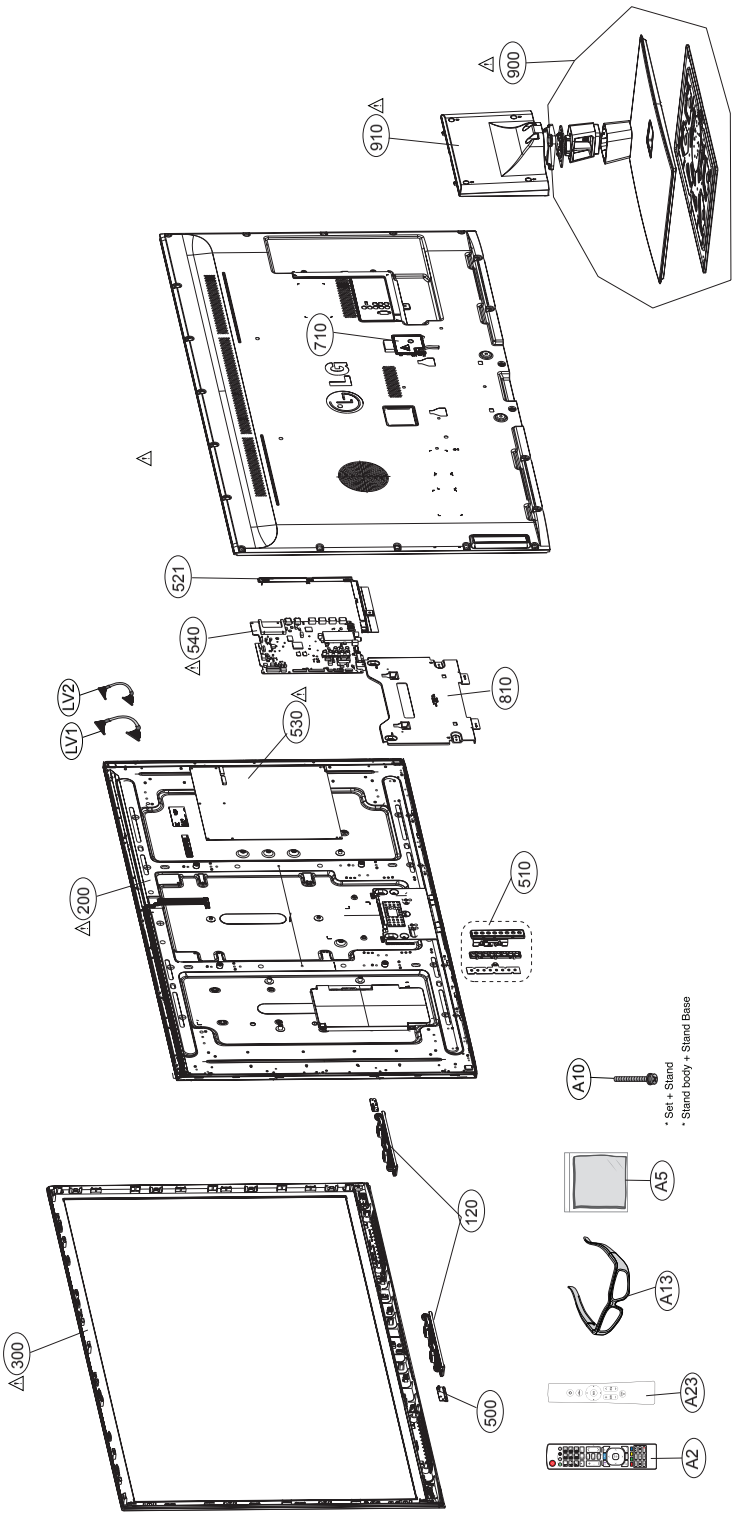
P/NO : MFL66980409 (1103-REV00)

Printed in Korea

EXPLODED VIEW

IMPORTANT SAFETY NOTICE

Many electrical and mechanical parts in this chassis have special safety-related characteristics. These parts are identified by ⚠ in the Schematic Diagram and EXPLODED VIEW.
It is essential that these special safety parts should be replaced with the same components as recommended in this manual to prevent X-RADIATION, Shock, Fire, or other Hazards.
Do not modify the original design without permission of manufacturer.



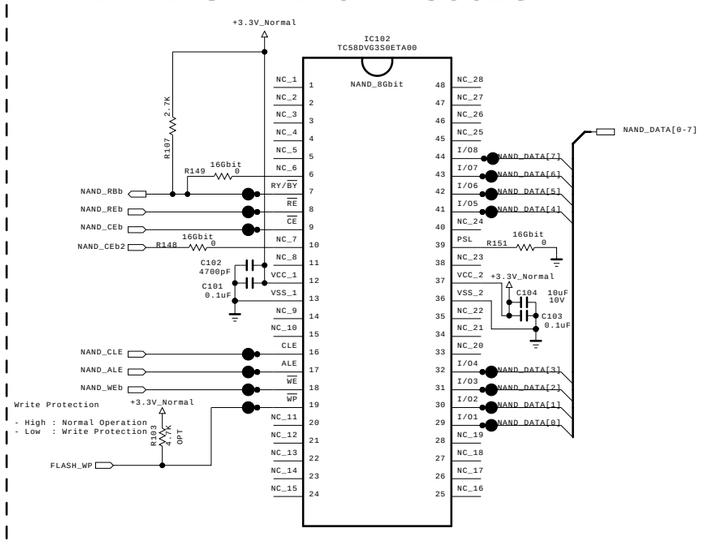
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Only for training and service purposes

LGE Internal Use Only

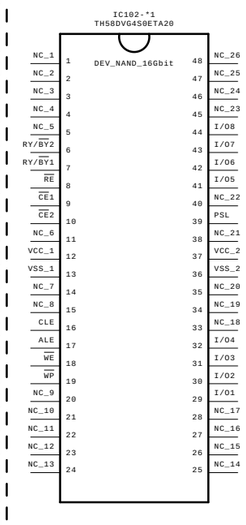
55LW5700-UE.AUSYLUR EXPLODED VIEW PARTS LIST

Loc No	Part No	Description(English)	Specification
120	EAB62088401	Speaker,Full Range	EN1080C-6795 ND 10W 8OHM 79DB 150HZ 200x25x27 CONTACT KOREA TOP TONE CO.,LTD.
200	EAJ61750001	LCD,Module-TFT	LC550EUF-SDF1 FHD 55.0INCH 1920X1080 400CD COLOR 99% 16/9 1600:1 240Hz(T) Inverter N 10bit(D) NRT-AGP 178/178 MPRT 6ms Edge 160PKG 10000K LVDS 4port (108.5W) 14.4Kg V6 LG Display Co. Ltd.
200	CDR30558601	LCD,Module-TFT (Recycled)	LC550EUF-SDF1 FHD 55.0INCH 1920X1080 400CD COLOR 99% 16/9 1600:1 240Hz(T) Inverter N 10bit(D) NRT-AGP 178/178 MPRT 6ms Edge 160PKG 10000K LVDS 4port (108.5W) 14.4Kg V6 LG Display Co. Ltd.
200	EAJ61928201	LCD,Module-TFT	LC550EUF-SDF2 FHD 55.0INCH 1920X1080 400CD COLOR 99% 16/9 1600:1 240Hz(T) Inverter N 10bit(D) NRT-AGP 178/178 MPRT 6ms Edge 160PKG 10000K LVDS 4port (108.5W) 14.4Kg V6 LW4/LW5 Series LG Display Co. Ltd.
200	CDR30563301	LCD,Module-TFT (Recycled)	LC550EUF-SDF2 FHD 55.0INCH 1920X1080 400CD COLOR 99% 16/9 1600:1 240Hz(T) Inverter N 10bit(D) NRT-AGP 178/178 MPRT 6ms Edge 160PKG 10000K LVDS 4port (108.5W) 14.4Kg V6 LW4/LW5 Series LG Display Co. Ltd.
300	ABJ73389507	Cabinet Assembly	55LW5700 . 55" Cabinet assy(E Type-Black), XG569C(HB), RS Local
400	ACQ84673618	Cover Assembly,Rear	55LW5700 . 55" 55LW5700 Back Cover assy_RS_LOCAL_Phantom
500	EBR72670801	PCB Assembly,Sub Sub Front IR	LW5700 IR + EYE Q ASS'Y CONTROL T.T . LW5700 . LW5700 IR ASS'Y ONLY CHEMTRONICS CO., LTD
510	EBR73361101	PCB Assembly, Key Board	Front IR CONTROL PAKING LA12C LW5700-UE Sxxx, Kxxx -
521	MGJ62689302	Plate,Shield	PRESS EGI 0.5 SHIELD EGI LV5 Side AV Metal Bracket(NTSC)_CSKD of "01"
530	EAY62169901	Power Supply Assembly	LGP55-11SLPB FREE LGP55-11SLPB LCD HNE/YUYANG/LGIT/LIENCHANG - H&E CO.,LTD
530	CRB31006801	Power Supply Assembly (Recycled)	LGP55-11SLPB FREE LGP55-11SLPB LCD HNE/YUYANG/LGIT/LIENCHANG - H&E CO.,LTD
540	EBT61410207	Chassis Assembly	MAIN LA12C 55LW5700-UE.Kxxx
710	MAZ62827604	Bracket	MOLD ABS AF-312 BRACKET 47LW7500 - ABS Cord BRK_Non Flame_C/SKD
810	MJH62256302	Supporter	PRESS EGI 2.0 Supporter EGI HGI, 55LW7500, Metal stand guide_ CSKD
900	AAN73489004	Base Assembly	STAND 55LV35 - Stand assy XG570_CSKD
910	MJH62256203	Supporter	MOLD LUPOY Supporter PC 55LV3500, stand body top, PC+GF20%_CSKD of 01
A2	AKB72915238	Remote Controller Assembly	LCD CI S-Con(LW5600) USA,3D,BB
A3	EAD60817902	Power Cord	P090376 LP-30B 90011HS-H03D(90011TS-D) 1.625M 75MM 125V 10A SVT 18AWG 3C BLACK. UL/CSA
A10	FAB30016104	Screw Assembly	FAB30016104 MACHINE TYPE D4.0 L12.0 WASHER D8.5 t0.6 SEUNGBO MECHA TECH CO.,LTD
A13	EBX61268401	Accessory,3D Glasses	3D Passive Glasses 47LH503D-ND 3D Passive Glasses_for adult(Black) SEESUN CO.,LTD
A21	MCK62976201	Cover,Rear	MOLD ABS CI S-con ABS CI S-con Battery cover
A23	EAT60713301	Dongle Module,Assembly	WN8522B2-LF-19 AN-WF100 UPC Code (719192578838) BCM4323 802.11a/b/g/n Dual Band Wi-Fi USB Dongle Arcadyan
A23	EAT60713302	Dongle Module,Assembly	WN8522B2-LF-19 EAN AN-WF100 EAN Code(8808992870876) BCM4323 802.11a/b/g/n Dual Band Wi-Fi USB Dongle Arcadyan Technology Corporation
A23	EAT60713304	Dongle Module,Assembly	WN8522B2-LF-19 Dongle Only AN-WF100 BCM4323 802.11a/b/g/n Dual Band Wi-Fi USB Dongle Arcadyan Technology Corporation
LV1	EAD61668619	LVDS Cable to P3501	EAD61668619 415MM 0.50MM 51P WHITE UL20861 Reverse Locking A: 125mm B: 210mm C: 100mm D: 70mm YOUNG SHIN CO.LTD
LV2	EAD61652507	LVDS Cable to P3502	EAD61652507 505MM 0.50MM 41P WHITE UL20861 Reverse A: 125mm B: 250mm C: 135mm D: 70mm YOUNG SHIN CO.LTD

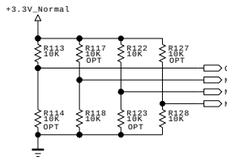
NAND FLASH MEMORY 8Gbit



16Gbit

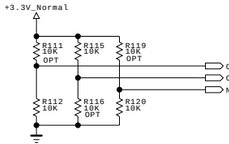


Boot ROM Device Select - (FA4,FAD7,FAD2,FAD1)



0000: ST Micro M25P or compatible Serial Flash
0010: 8-bit 512Mbit 512B page SLC NAND Flash devices
0100: 8-bit 128, 256Mbit 512B page SLC NAND Flash devices
0110: 8-bit 1Gbit 2KB page SLC NAND Flash devices
1000: 8-bit 2Gbit, 4Gbit, 8Gbit 2KB page SLC NAND Flash devices
1010: 8-bit 16Gbit, 32Gbit 4KB page SLC NAND Flash devices (O)
0001: 8-bit 8/16/32Gbit 2KB page MLC NAND Flash devices
0011: 8-bit 16/32Gbit 4KB page MLC NAND Flash devices
0101: 8-bit 32Gbit 8KB page MLC NAND Flash devices
0111: 3B dual IO Serial Flash
1001: BB dual IO Serial Flash
1011: fast Serial Flash > 50Mhz
1100: OneNAND Flash (always 16-bit)
1110: Reserved
1101, 1111: Reserved

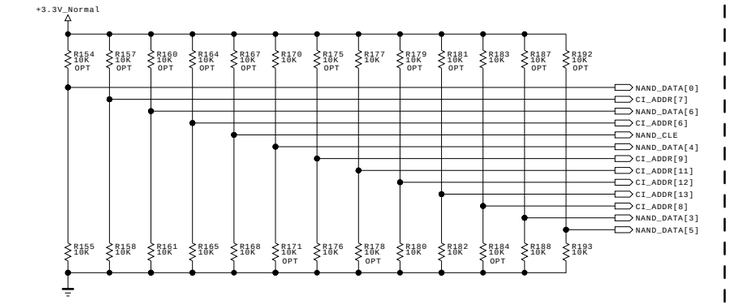
NAND ECC (FA3, FA2, FALE)



000 = ECC disabled
001 = ECC 1-bit repair
010 = ECC 4-bit BCH (O)
011 = ECC 8-bit BCH, 27 byte spare
100 = ECC 12-bit BCH, 27 byte spare
101 = ECC 8-bit BCH, 16 byte spare
110, 111 = Reserved

DUAL COMPONENT	
IC102	1ST : EAN61000101 2ND : T-TH58DVG4S0ETA20
IC102-*1	

Strap Setting



NAND_DATA[0]:
0: System is LITTLE endian (O)
1: System is BIG endian

CI_ADDR[7]:
0: Disable EDID automatic Downloading from Flash (O)
1: Enable EDID automatic Downloading from Flash

NAND_DATA[6] :
0: Disable OSC clock output on chip Pin (O)
1: Enable OSC clock output on chip pin.

CI_ADDR[6]:
0: Host MIPS run at 500 MHz (O)
1: Host MIPS run at 250 MHz

NAND_CLE:
0: Differential Oscillators TVM not bypassed (O)
1: Differential Oscillators TVM bypassed

NAND_DATA[4]:
0: 27MHz TVM Crystal Frequency
1: 54MHz TVM Crystal Frequency (O)

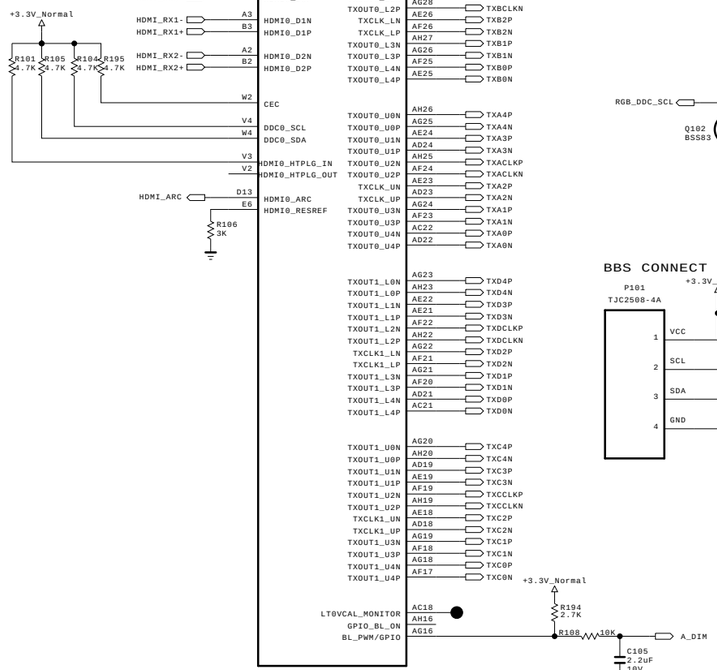
CI_ADDR[9],CI_ADDR[11],CI_ADDR[12],CI_ADDR[13]
TVM Crystal oscillator bias/gain control
0000: 210uA
0001: 390uA
0010: 570uA
0011: 730uA
0100: 890uA (O)
0111: 1290uA
1000: 1416uA
1111: 2196uA
0101, 0110, 1001, 1010, 1011, 1100, 1101, 1110: Reserved

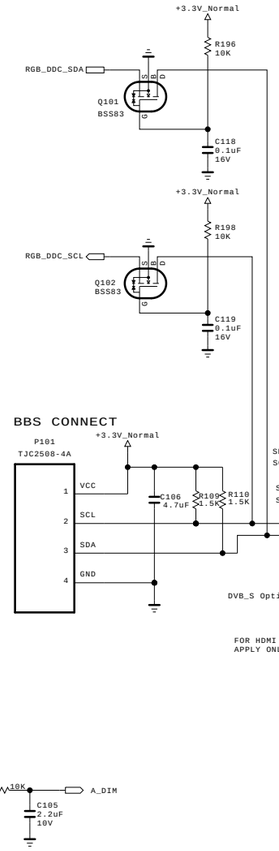
CI_ADDR[8]:
0: RESETOUTb (in On/Off only) stay asserted until software releases them.
1: Fix amount of delay for de-assertion on RESETOUTb (in On/IOff only) at end of RESETb pulse (O)

NAND_DATA[3]:
0: MIPS will boot from external flash (O)
1: MIPS will boot from ROM

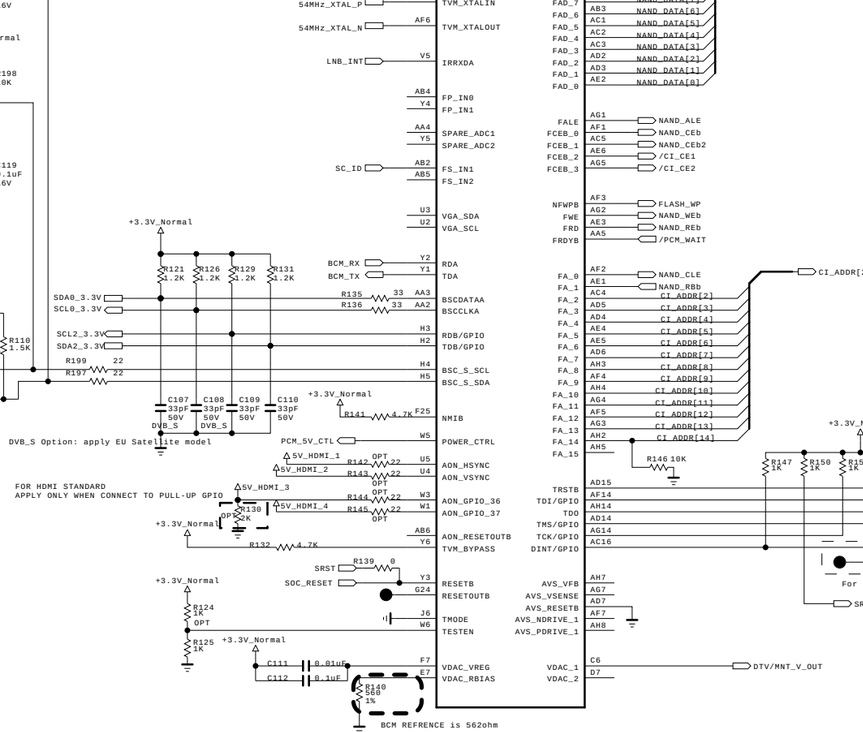
NAND_DATA[5]:
0: FLASH MODE (O)
1: BSC_SLAVE(BBS) MODE

IC101 LGE35230(BCM35230KFSBG)

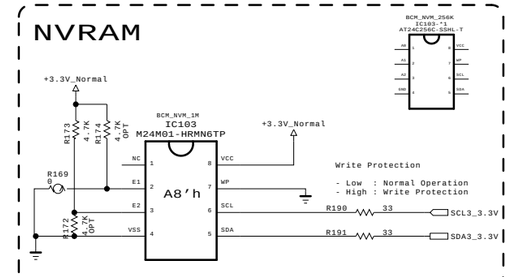




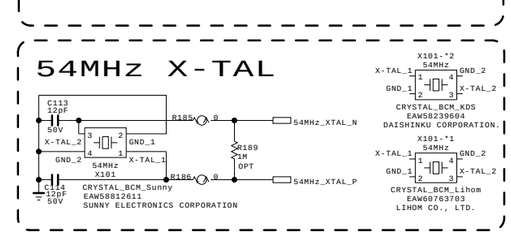
BBS CONNECT



NVRAM



54MHz X-TAL

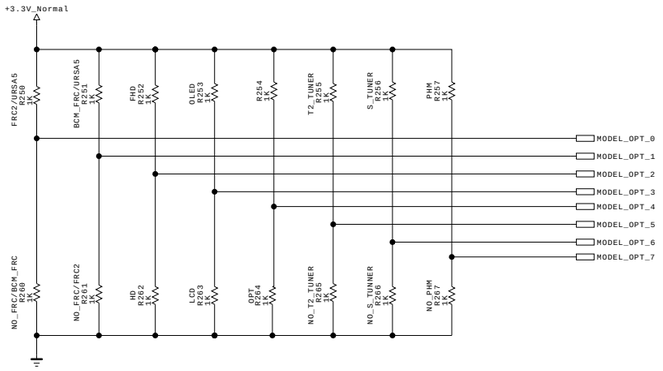


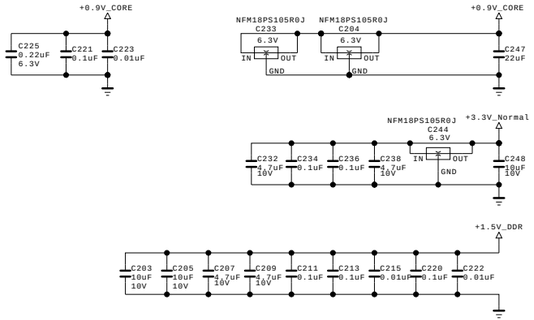
THE ⚠ SYMBOL MARK OF THIS SCHEMETIC DIAGRAM INCORPORATES SPECIAL FEATURES IMPORTANT FOR PROTECTION FROM X-RADIATION. FILRE AND ELECTRICAL SHOCK HAZARDS, WHEN SERVICING IF IS ESSENTIAL THAT ONLY MANUFATURES SPECFIED PARTS BE USED FOR THE CRITICAL COMPONENTS IN THE ⚠ SYMBOL MARK OF THE SCHEMETIC.

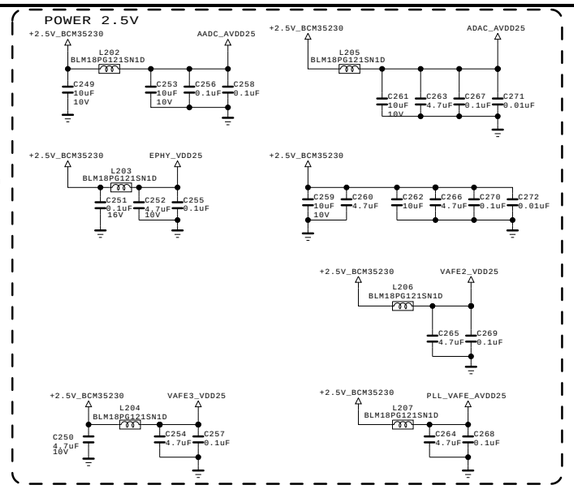
SECRET
LGElectronics

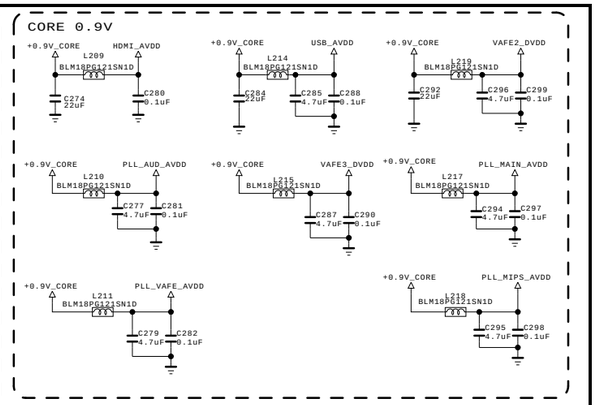
LG ELECTRONICS

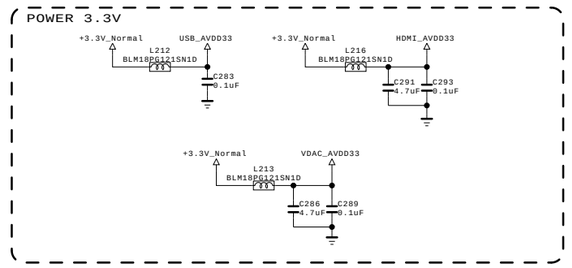
MODEL	BCM35230	DATE	2010.09.18
BLOCK	MAIN & NAND FLASH	SHEET	1 /







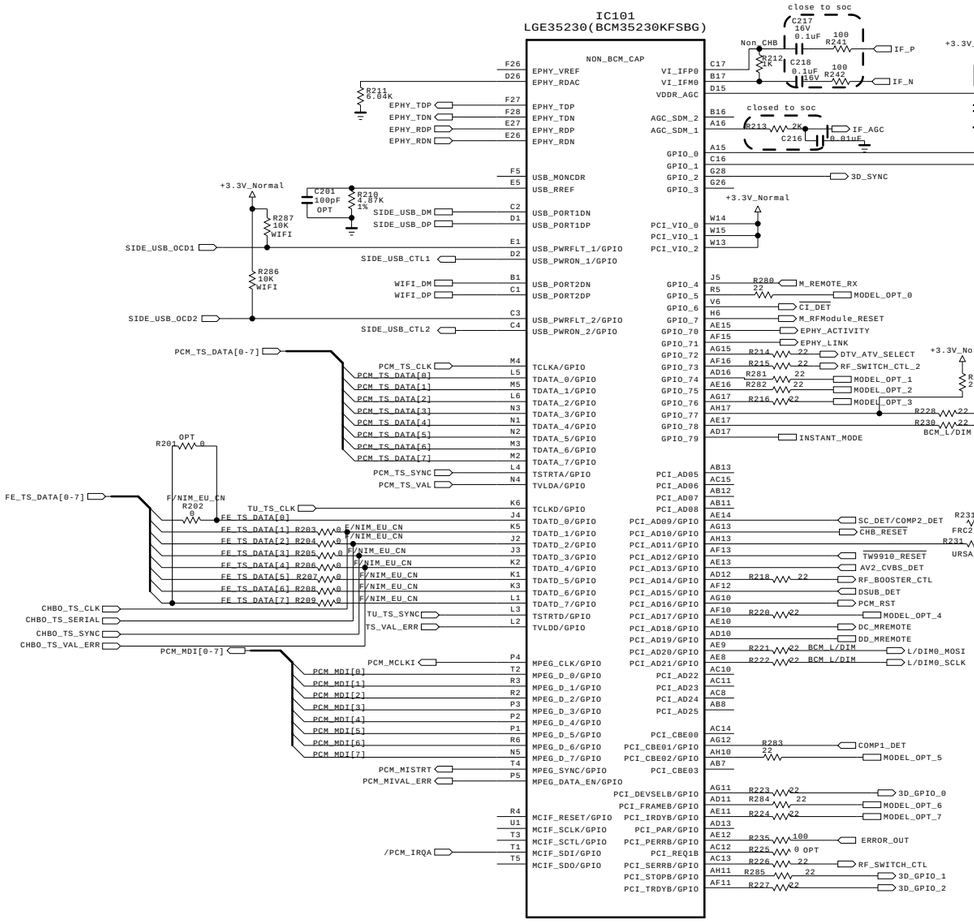


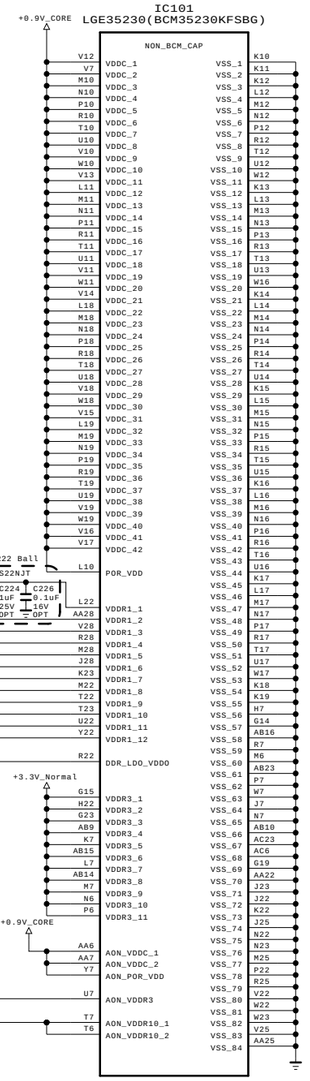


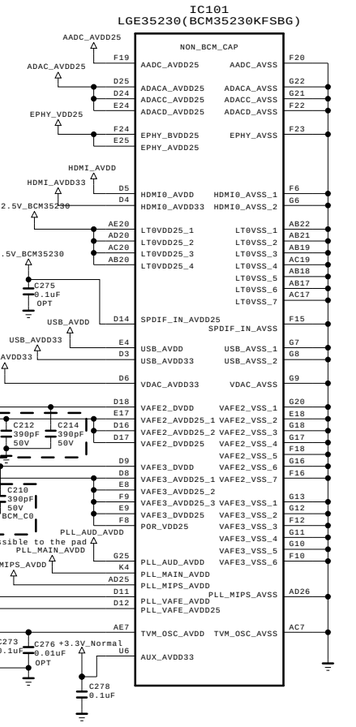
MODEL OPTION

	NO_FRC	BCM internal FRC	LG FRC2	external URSA5
MODEL_OPT_0	0	0	1	1
MODEL_OPT_1	0	1	0	1

		HIGH	LOW
MODEL_OPT_2		FHD	HD
MODEL_OPT_3		OLED	LCD
MODEL_OPT_4	DDR speed	1333	1600
MODEL_OPT_5	T2 Tuner	Support	Not Support
MODEL_OPT_6	S Tuner	Support	Not Support
MODEL_OPT_7	PHM	Enable	Disable







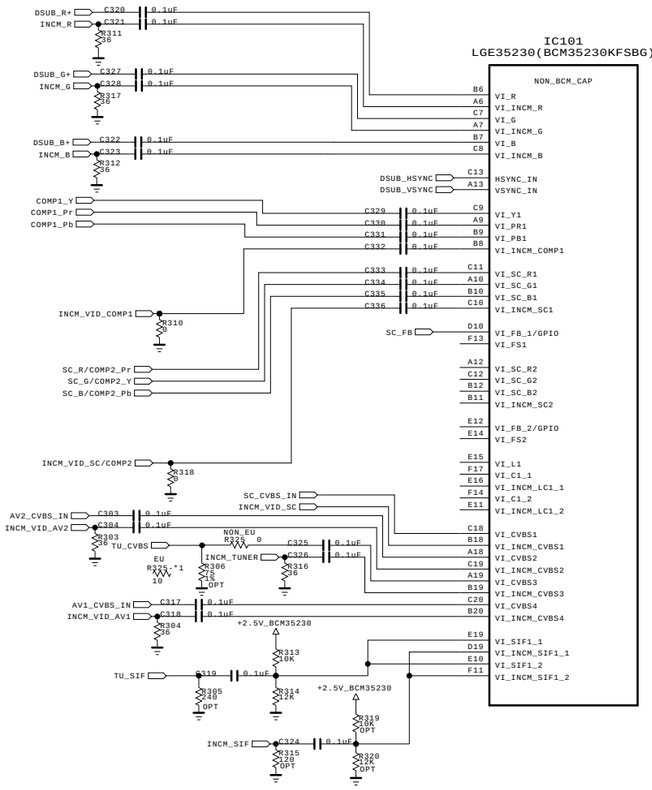
THE ⚠ SYMBOL MARK OF THIS SCHEMETIC DIAGRAM INCORPORATES SPECIAL FEATURES IMPORTANT FOR PROTECTION FROM X-RADIATION. FILRE AND ELECTRICAL SHOCK HAZARDS, WHEN SERVICING IF IS ESSENTIAL THAT ONLY MANUFATURES SPECFIED PARTS BE USED FOR THE CRITICAL COMPONENTS IN THE ⚠ SYMBOL MARK OF THE SCHEMETIC.

SECRET

LGElectronics

LG ELECTRONICS

MODEL	BCM35230	DATE	
BLOCK	MAIN POWER	SHEET	2 / 50



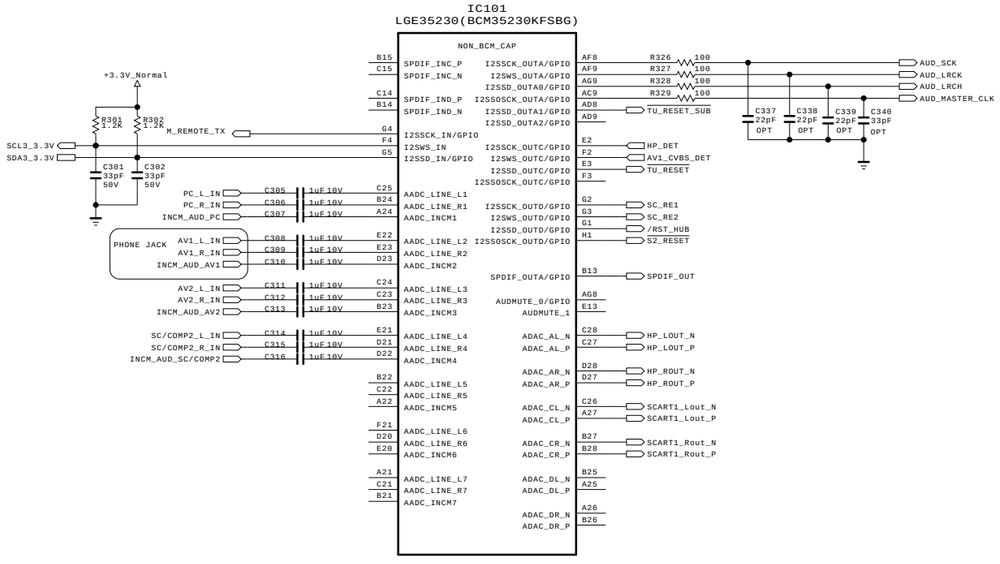
VIDEO INCM

Near P801	Run Along DSUB_R Trace	INCM_R
Near P801	Run Along DSUB_G Trace	INCM_G
Near P801	Run Along DSUB_B Trace	INCM_B
Near JK1101	Run Along COMP_Y_IN,COMP_Pr_IN,COMP_Pb_IN Trace	INCM_VID_COMP1
Near JK1104	Run Along AV2_CVBS Trace	INCM_VID_AV2
Near TU2101/2 TU2201/2/3	Run Along TUNER_CVBS_IF_P Trace	INCM_TUNER
Near JK1102	Run Along AV1_CVBS Trace	INCM_VID_AV1
Near JK1103 JK2501	Run Along COMP_Y_IN,COMP_Pr_IN,COMP_Pb_IN/SC_R,G,B Trace	INCM_VID_SC/COMP2

BCM35230_with_CAP_220pF

IC101-*1
LGE35230

NON_BCM_CAP
VI_R
VI_INCM_R
VI_G
VI_INCM_G
VI_B
VI_INCM_B
HSYNC_IN
VSYNC_IN
VI_Y1
VI_PR1
VI_PB1
VI_INCM_COMP1
VI_SC_R1
VI_SC_G1
VI_SC_B1
VI_INCM_SC1
VI_FB_1/GPIO
VI_FS1
VI_SC_R2
VI_SC_G2
VI_SC_B2
VI_INCM_SC2
VI_FB_2/GPIO
VI_FS2
VI_L1
VI_C1_1
VI_INCM_LC1_1
VI_C1_2
VI_INCM_LC1_2
VI_CVBS1
VI_INCM_CVBS1
VI_CVBS2
VI_INCM_CVBS2
VI_CVBS3
VI_INCM_CVBS3
VI_CVBS4
VI_INCM_CVBS4
VI_SIF1_1
VI_INCM_SIF1_1
VI_SIF1_2
VI_INCM_SIF1_2



AUDIO INCM

Near JK1102	R321 0	Route Between AV1_L_IN & AV1_R_IN Trace	INCM_AUD_AV1
Near JK1103 JK2501	R322 0	Route Between SC/COMP2_L_IN & SC/COMP2_R_IN Trace	INCM_AUD_SC/COMP2
Near JK1104	R323 0	Route Between AV2_L_IN & AV2_R_IN Trace	INCM_AUD_AV2
Near JK801	R324 0	Route Between PC_L_IN & PC_R_IN Trace	INCM_AUD_PC
Near TU2101/2 TU2201/2/3		Route Along With TUNER_SIF_IF_N	INCM_SIF

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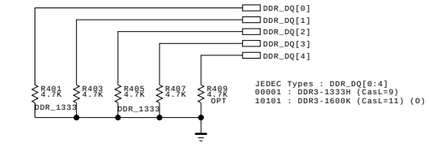
SECRET
LGElectronics

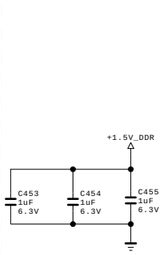
LG ELECTRONICS

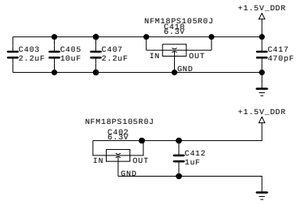
MODEL	BCM35230	DATE	
BLOCK	MAIN AUDIO/VIDEO	SHEET	3 / 50

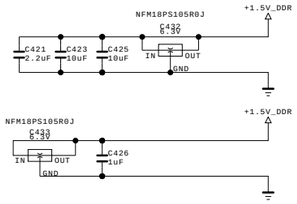
DUAL COMPONENT	
IC401,IC402	1ST : EAN61667501, 2ND : EAN61570701
IC401-*1 IC402-*1	1ST : T-K4B2G1646B_HCK0, 2ND : T-H5TQ2G63BFR-PBC

DDR STRAP

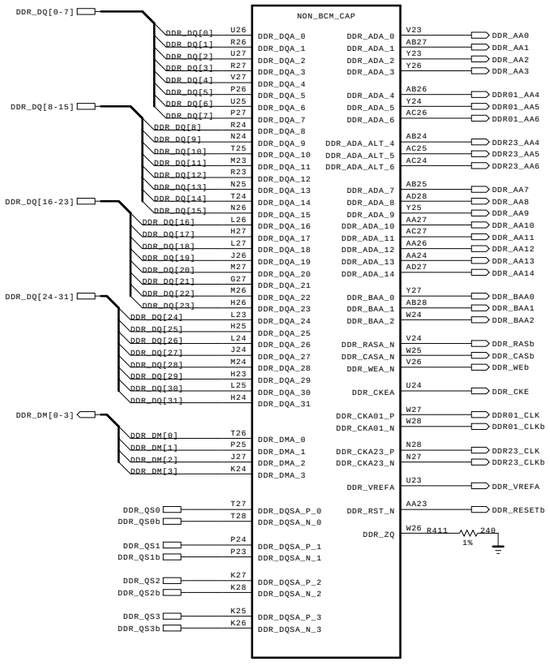




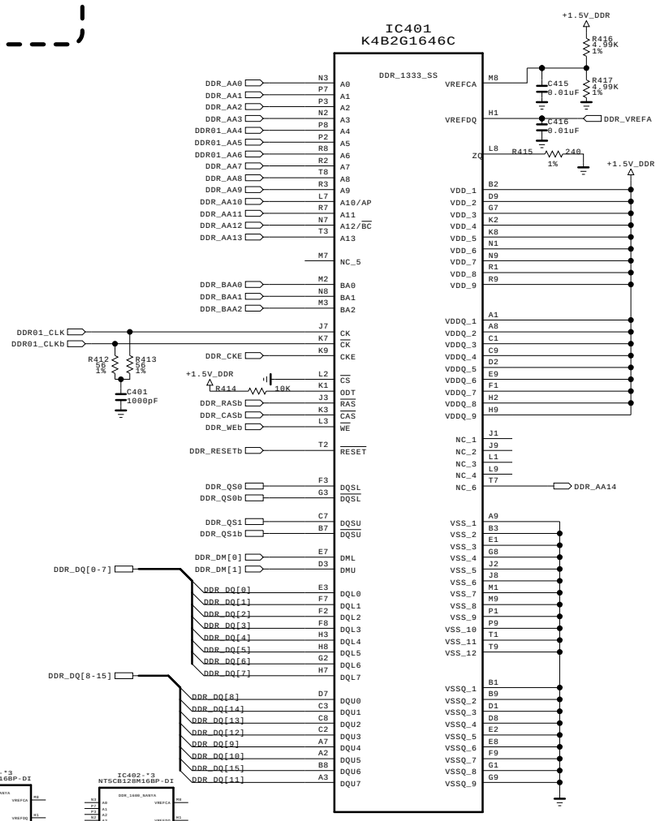




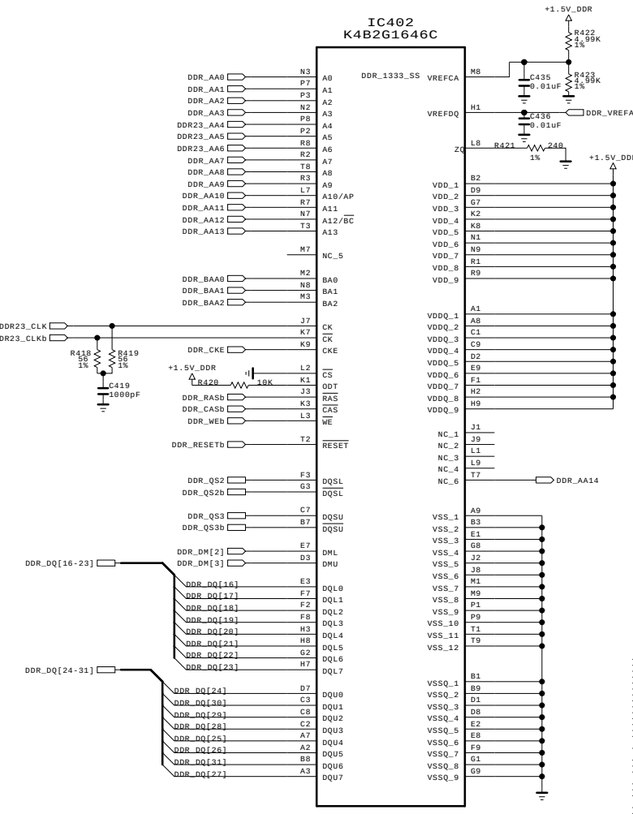
IC101
LGE35230(BCM35230KFSBG)

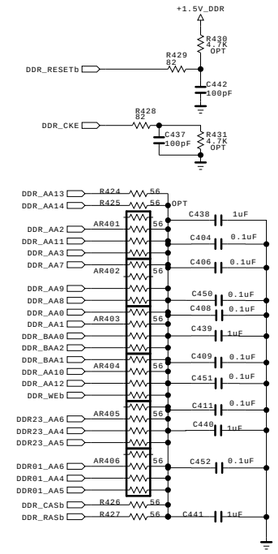


IC401
K4B2G1646C



IC402
K4B2G1646C





IC401-*2
NT5CB128M16BP-CG



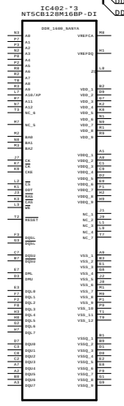
IC402-*2
NT5CB128M16BP-CG



IC401-*3
NT5CB128M16BP-DI



IC402-*3
NT5CB128M16BP-DI



IC401-*1
K4B2G1646C-HCK0



IC402-*1
K4B2G1646C-HCK0



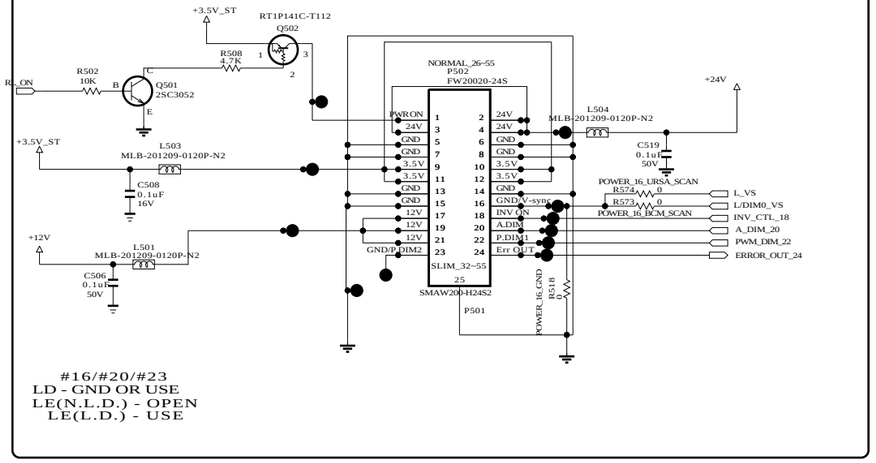
THE ⚠ SYMBOL MARK OF THIS SCHEMETIC DIAGRAM INCORPORATES SPECIAL FEATURES IMPORTANT FOR PROTECTION FROM X-RADIATION. FILRE AND ELECTRICAL SHOCK HAZARDS, WHEN SERVICING IF IS ESSENTIAL THAT ONLY MANUFATURES SPECFIED PARTS BE USED FOR THE CRITICAL COMPONENTS IN THE ⚠ SYMBOL MARK OF THE SCHEMETIC.

SECRET
LGElectronics

LG ELECTRONICS

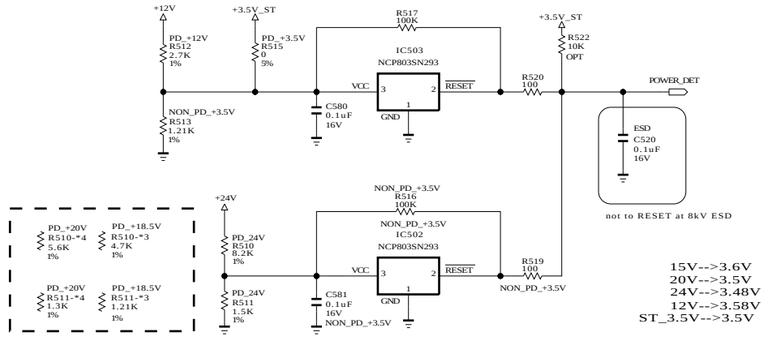
MODEL	BCM35230	DATE	
BLOCK	MAIN DDR	SHEET	4 / 50

FROM LIPS & POWER B/D



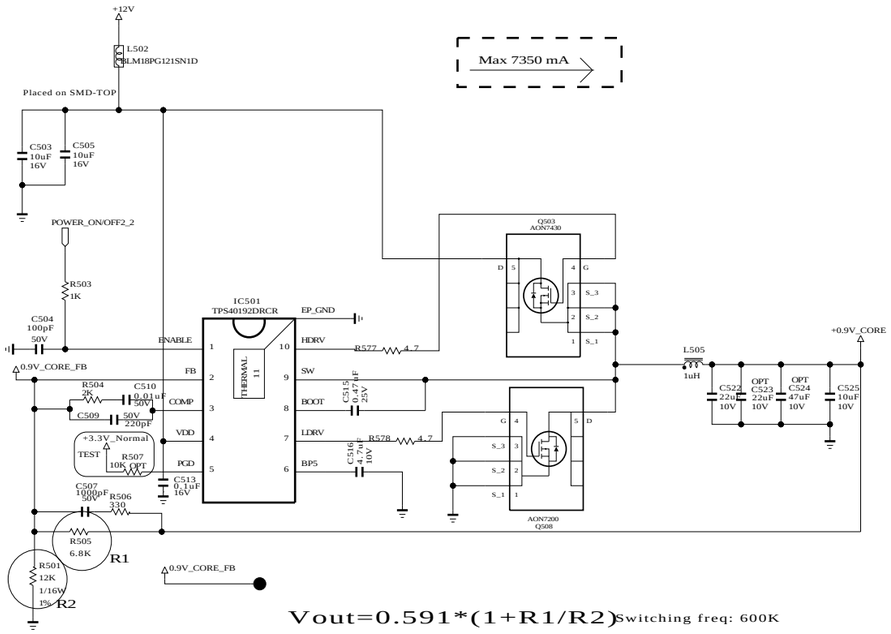
#16/#20/#23
LD - GND OR USE
LE(N.L.D.) - OPEN
LE(L.D.) - USE

Power_DET



15V-->3.6V
20V-->3.5V
24V-->3.48V
12V-->3.58V
ST_3.5V-->3.5V

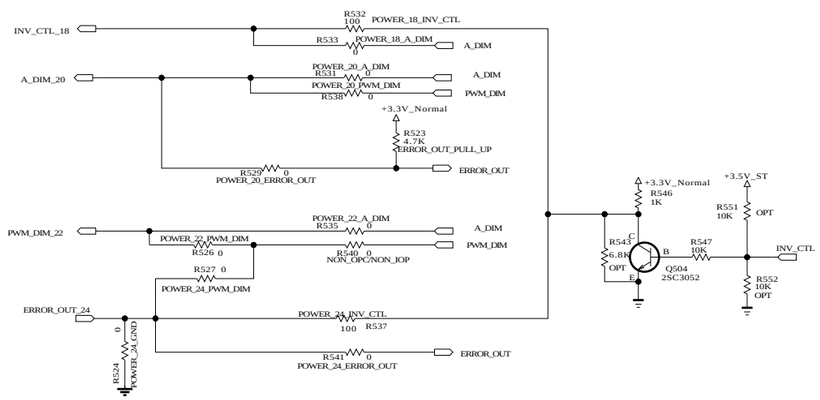
+0.9V_CORE_BCM35230



Vout=0.591*(1+R1/R2)
Switching freq: 600K

DUAL COMPONENT	
Q501,Q504, Q505,Q506	1ST : 0TRIY80001A 2ND : 0TR387500AA
Q502	1ST : 0TRIH80004A, 2ND : EBK61012501, 3RD : 0TR102009AM
Q507	1ST : EBK60752501, 2ND : EBK61011501
IC502,IC503	1ST : EAN61151001, 2ND : EAN60670101

OS Module OPT



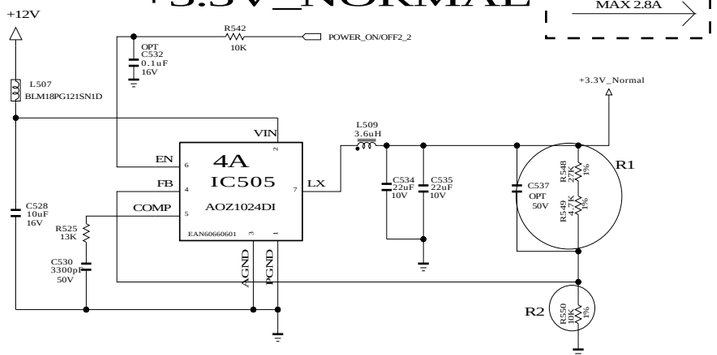
<OS MODULE PIN MAP>

PIN No	LGD	CMO(09)	AUO	SHARP
18	INV_ON	A-DIM	INV_ON	INV_ON
20	V4:VBR-A V5:NC	NC	Err_out	Err_out
22	PWM_DIM	PWM_DIM	A-DIM	PWM_DIM
24	Err_out LED:GND	INV_ON	PWM_DIM	GND

CHECK PWR/MODULE PIN MAP

+3.3V_NORMAL

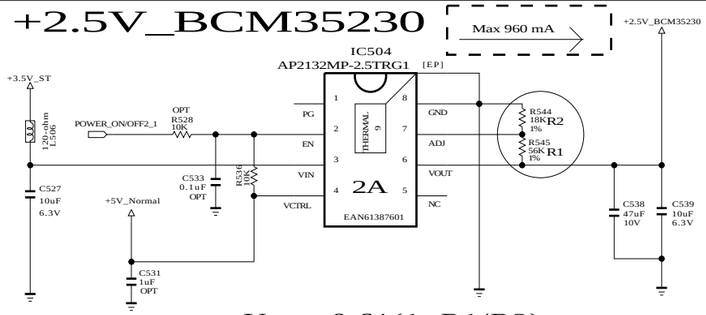
Vout=0.8*(1+R1/R2)
MAX 2.8A



Vout=0.8*(1+R1/R2)
Switching freq: 500K

+2.5V_BCM35230

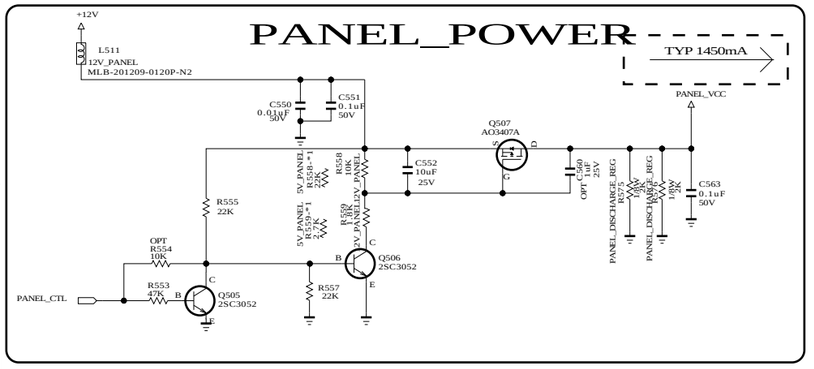
Max 960 mA



Vout=0.6*(1+R1/R2)

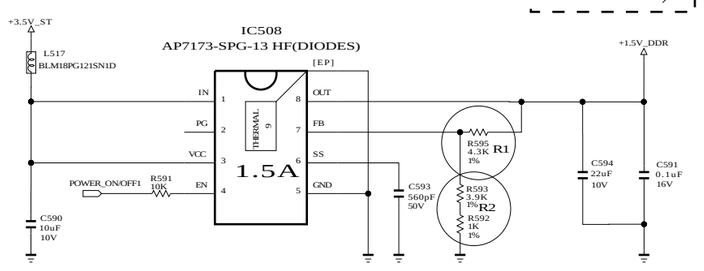
PANEL_POWER

TYP 1450mA



+1.5V_DDR

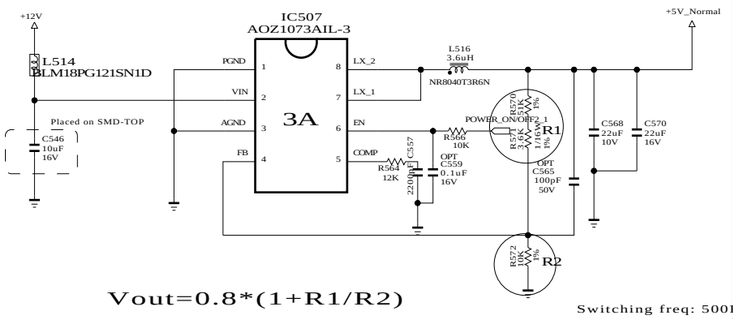
Max 800mA



Vout=0.8*(1+R1/R2)

+5V_Normal

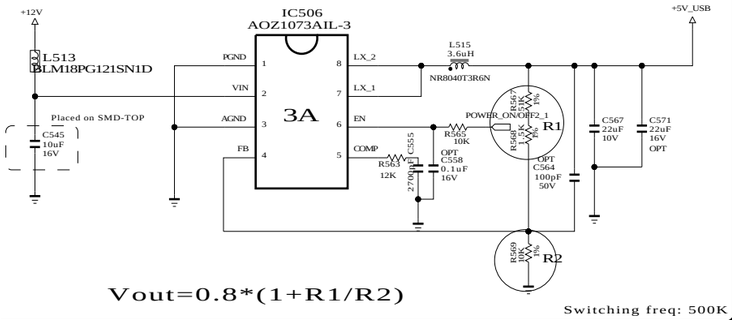
MAX 1A



Vout=0.8*(1+R1/R2)
Switching freq: 500K

+5V_USB+WIFI

MAX 1.9A



Vout=0.8*(1+R1/R2)
Switching freq: 500K

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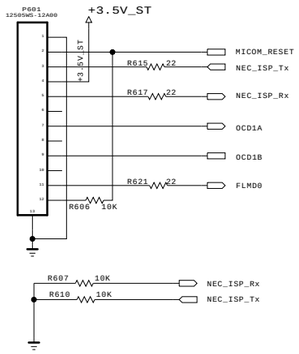
SECRET
LGElectronics

LG ELECTRONICS

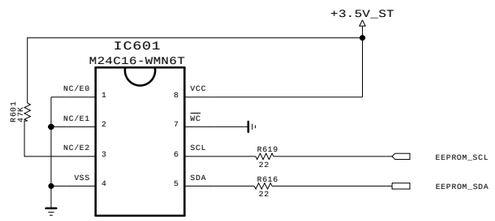
MODEL	BCM35230	DATE	
BLOCK	POWER	SHEET	5 / 58

NEC MICOM

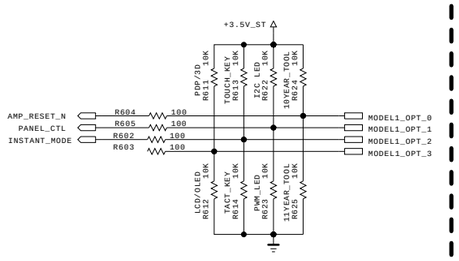
For Debug



EEPROM for Micom



MICOM MODEL OPTION

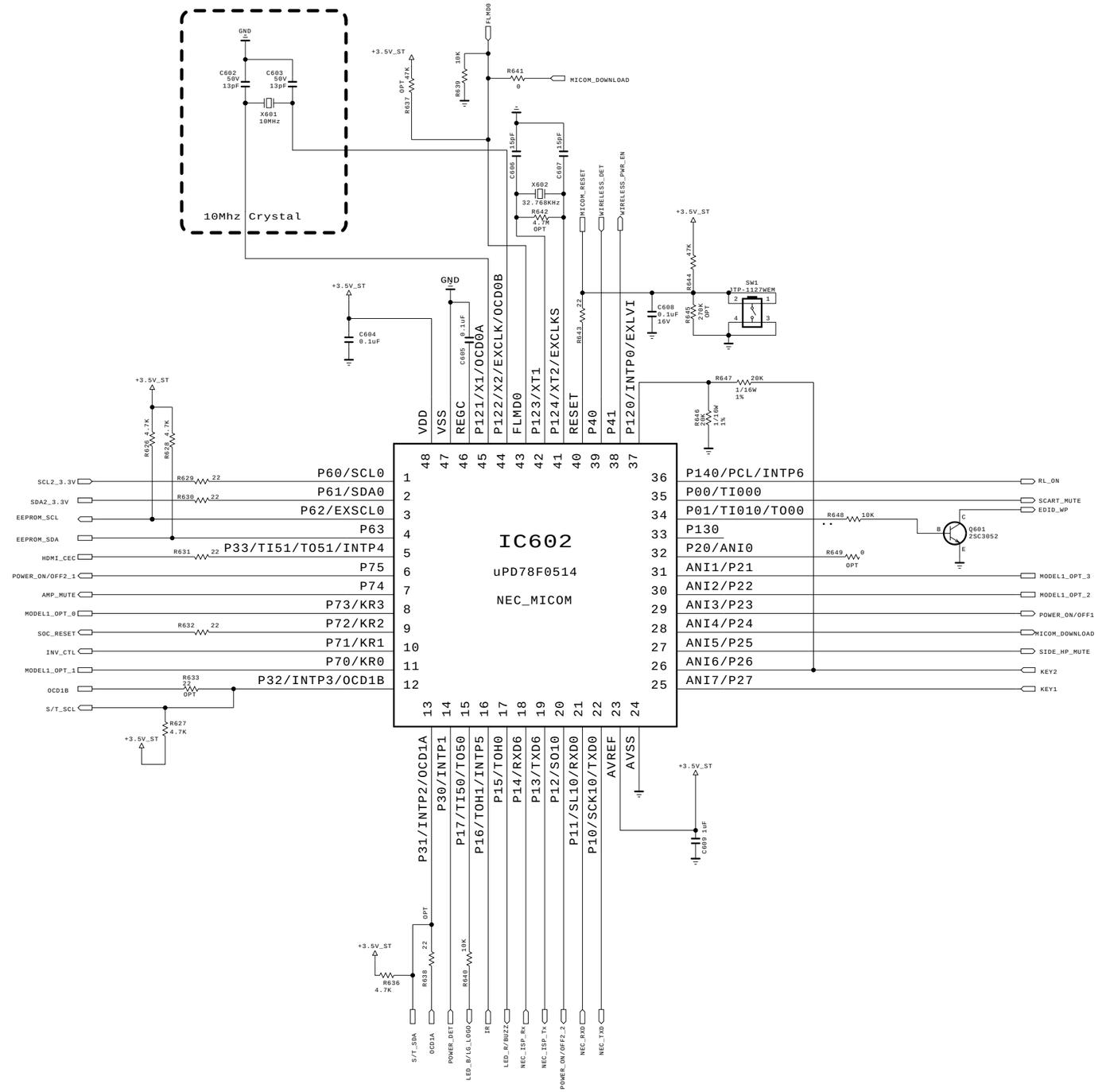


MODEL OPTION

PIN NAME	PIN NO.	HIGH	LOW
MODEL_OPT_0	8	10YEAR_TOOL (10 SENSOR)	11YEAR_TOOL (11 SENSOR)
MODEL_OPT_1	11	I2C_LED	PWM_LED
MODEL_OPT_2	30	TOUCH_KEY	TACT_KEY
MODEL_OPT_3	31	PDP/3D	LCD/OLED

	LCD	PDP	OLED	3D
MODEL_OPT_3	0	1	0	1

	LOW	LOW_SMALL	TBD	HIGH
MODEL_OPT_1	0	0	1	1
MODEL_OPT_2	0	1	0	1



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SECRET

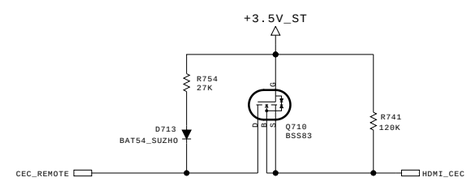
LGElectronics

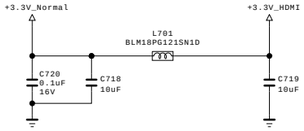
LG ELECTRONICS

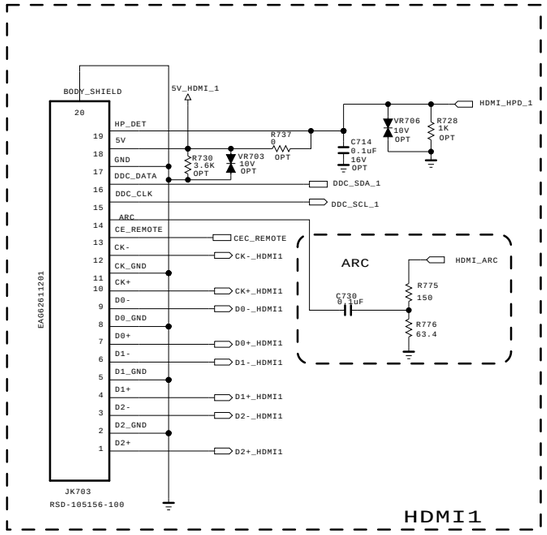
MODEL	BCM35230	DATE	
BLOCK	MICOM	SHEET	6 / 50

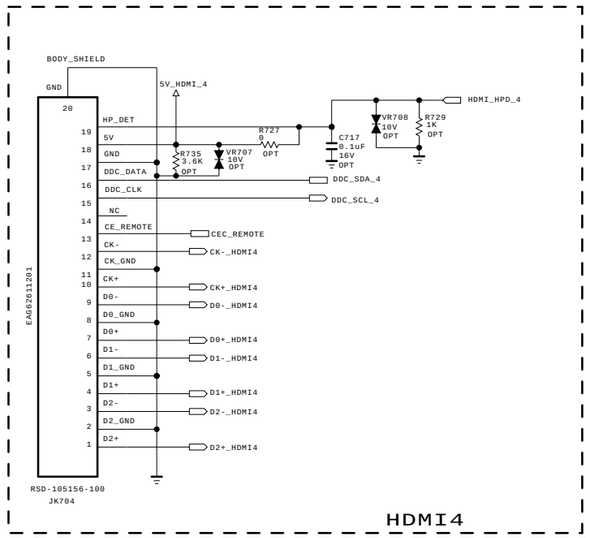
DUAL COMPONENT	
D707,D708 D710,D711	1ST : 0DD184009AA 2ND : 0DSIH00028A
D713	1ST : T-BAT54_SUZHO, 2ND : 0DSON00138A

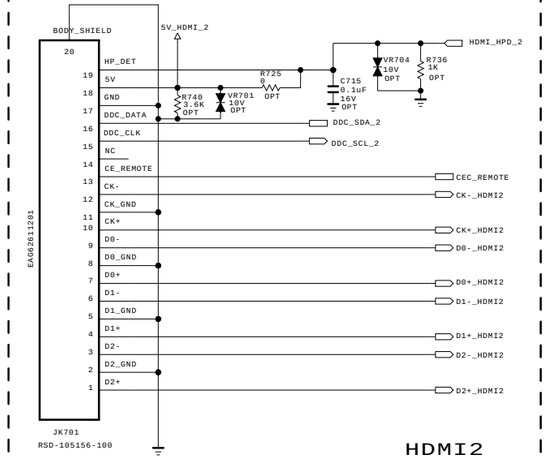
* HDMI CEC

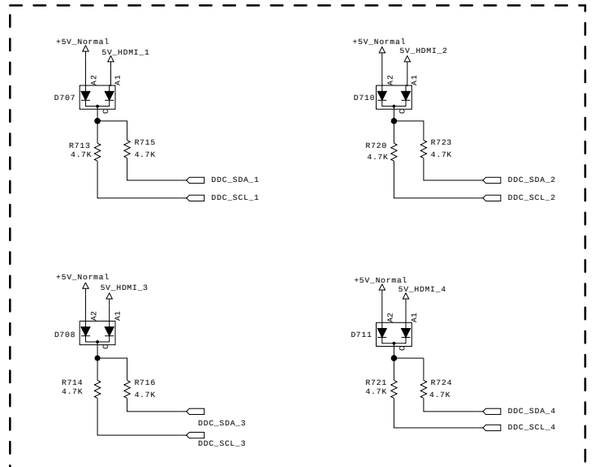


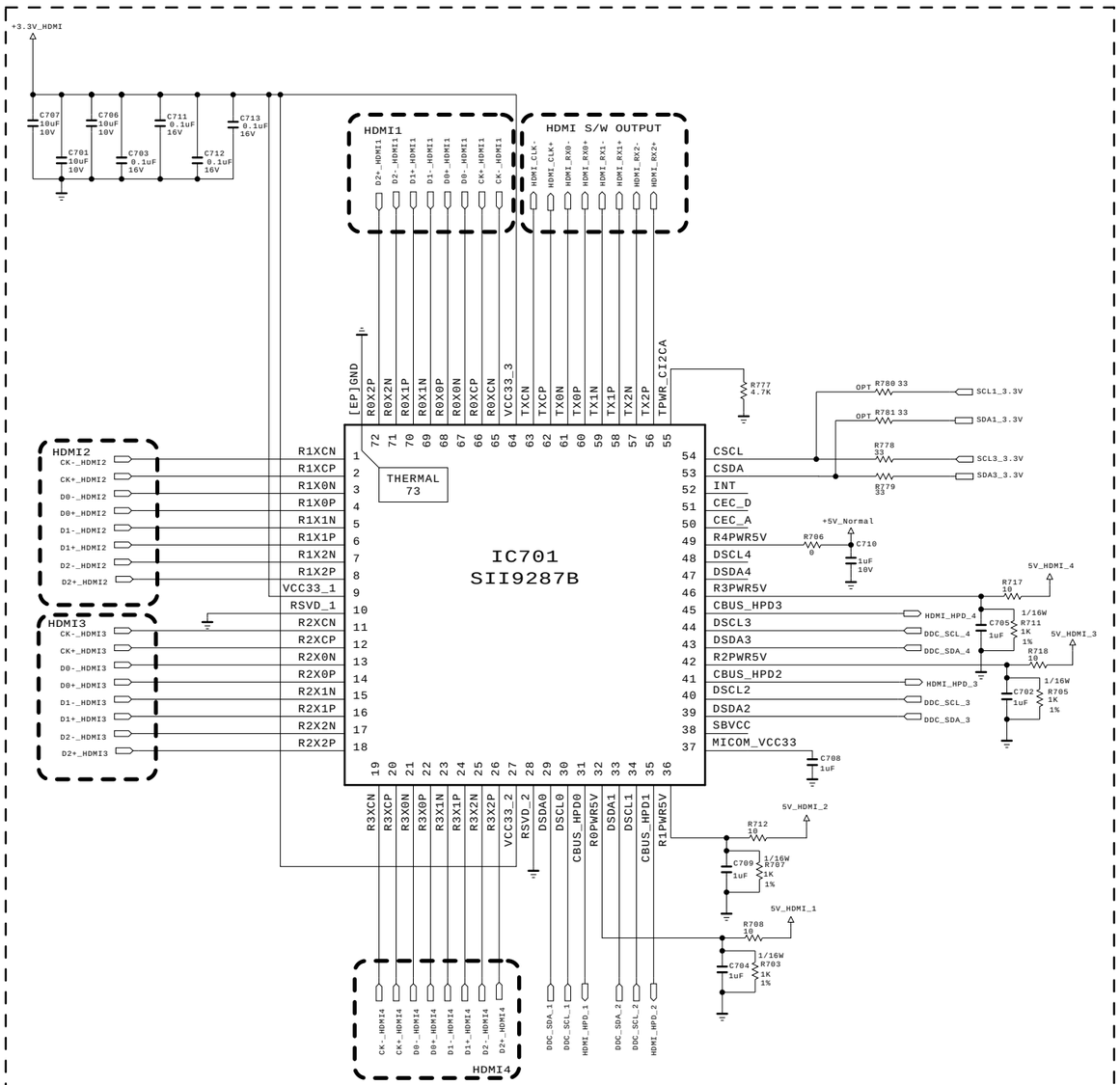












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SECRET

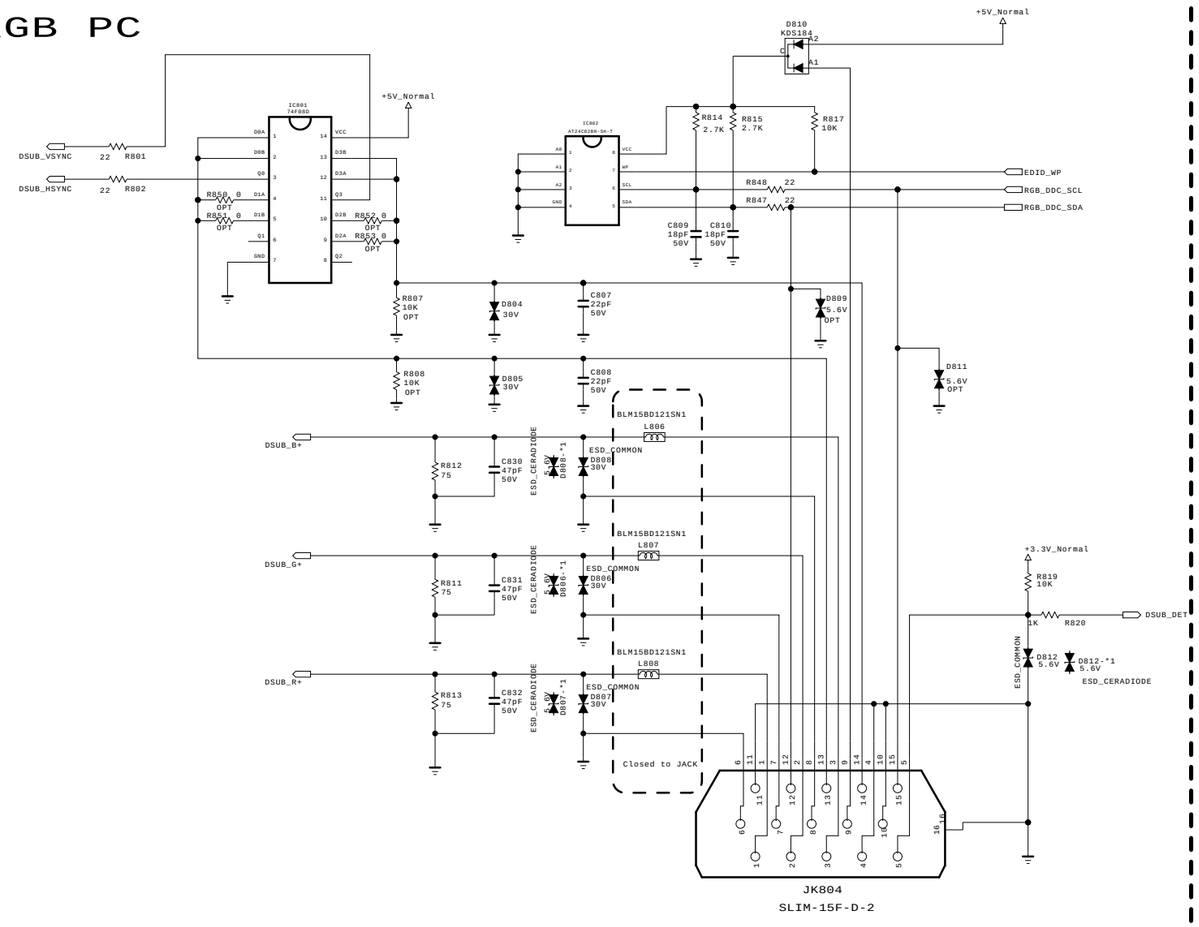
LGElectronics

LG ELECTRONICS

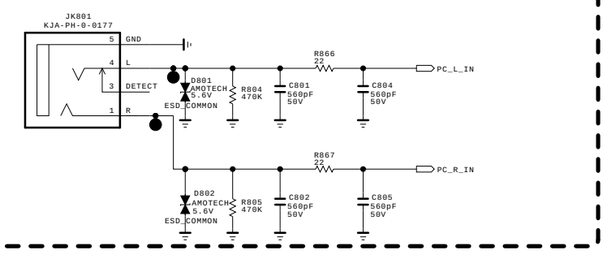
MODEL	BCM35230	DATE	
BLOCK	HDMI	SHEET	7 / 31

RGB/ PC AUDIO/ SPDIF/ EARPHONE/ RS232C

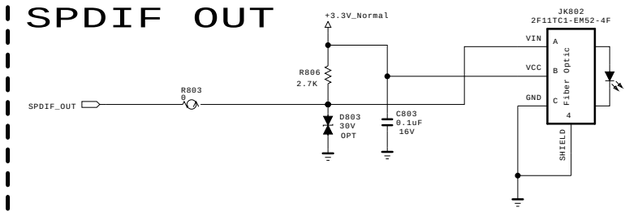
RGB PC



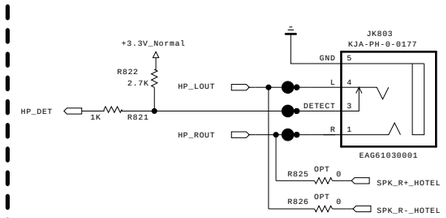
PC AUDIO



SPDIF OUT

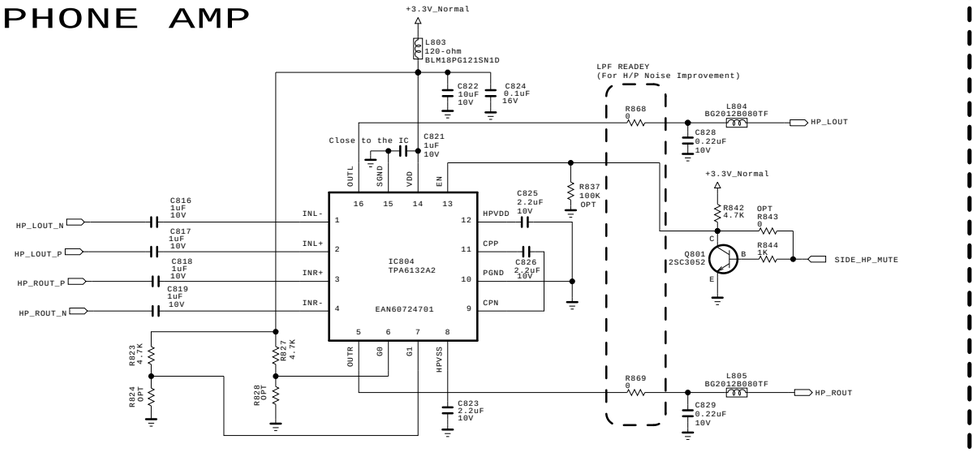


EARPHON JACK

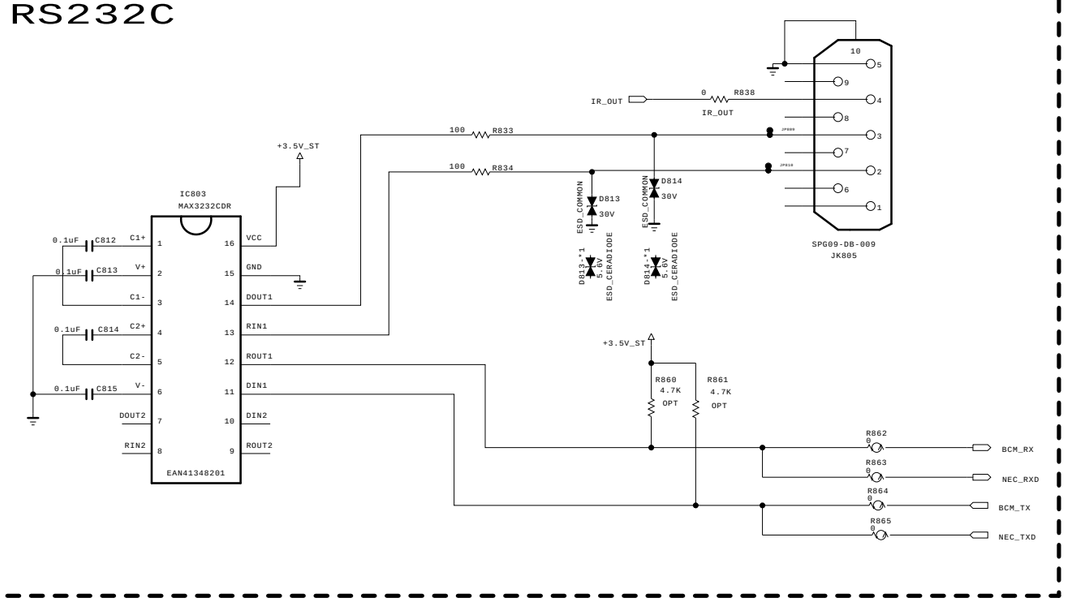


DUAL COMPONENT	
D804,D805,D806 D807,D808,D813 D814	1ST : EAH39491601, 2ND : EAH33945901
D810	1ST : 0DD184009AA, 2ND : 0DSIH00028A
Q801	1ST : 0TRIY80001A, 2ND : 0TR387500AA
IC805	1ST : EAN61151201, 2ND : EAN61130001

EARPHONE AMP



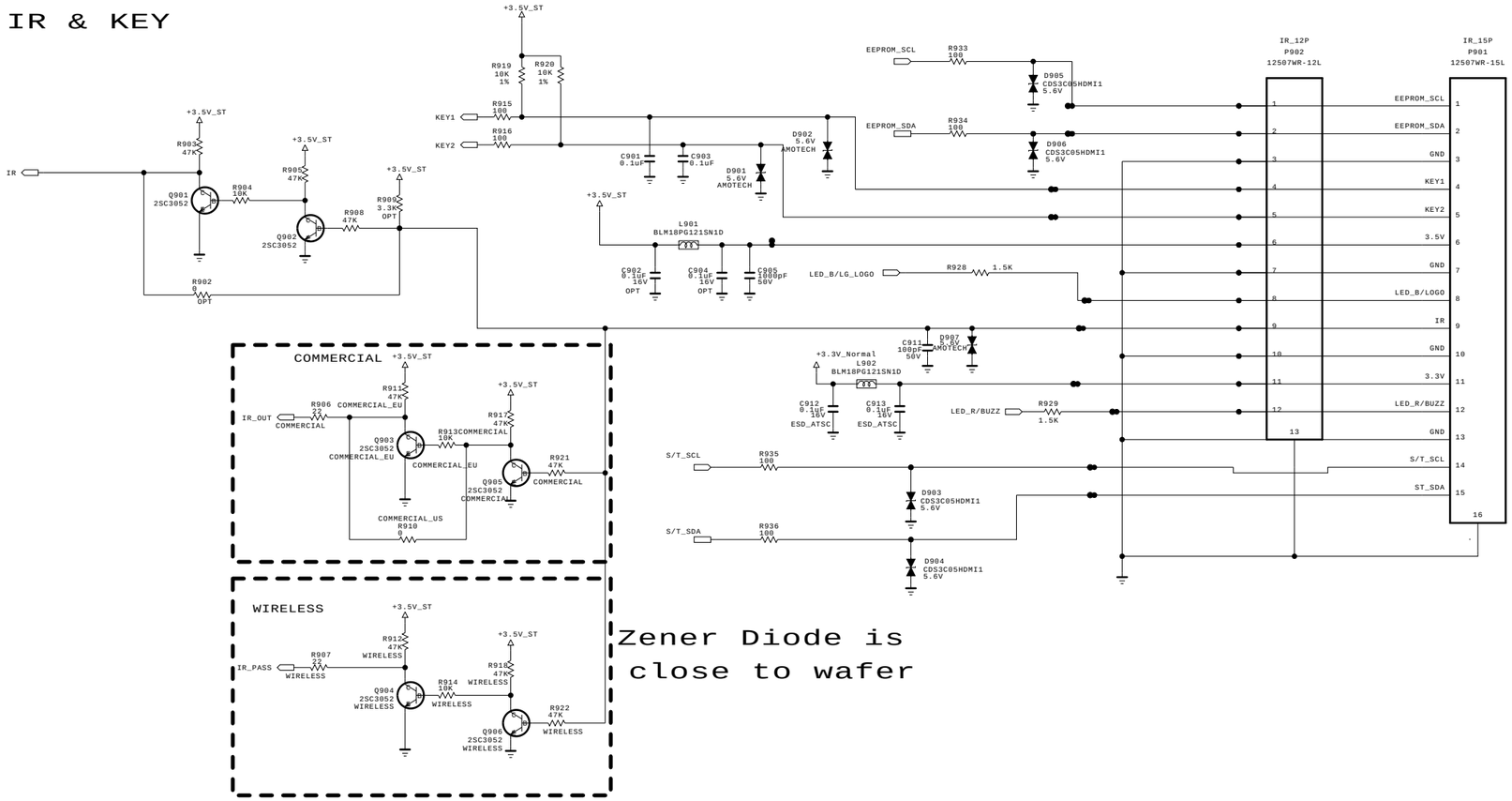
RS232C



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DUAL COMPONENT	
Q901,Q902,Q903 Q904,Q905,Q906	1ST : 0TRIY80001A 2ND : 0TR387500AA
D903,D904 D905,D906	1ST : EAH42720601, 2ND : EAH60994401

IR & KEY



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SECRET

LGElectronics

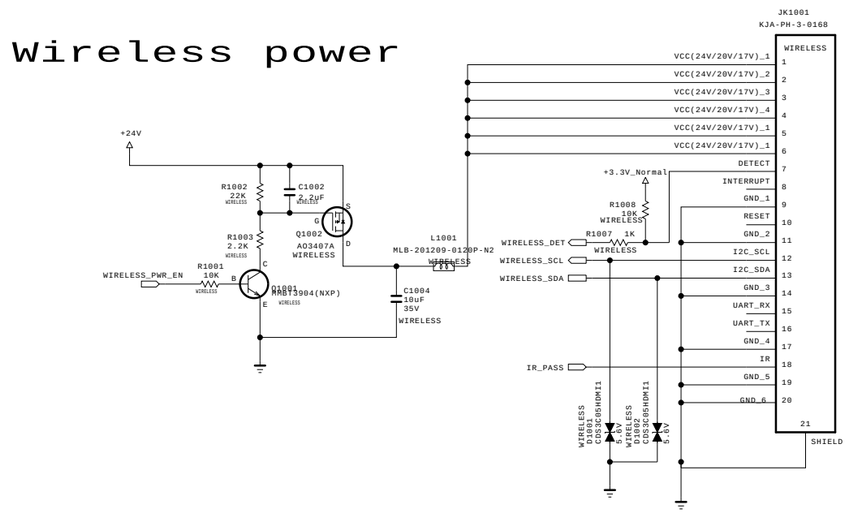
LG ELECTRONICS

MODEL	BCM35230	DATE	
BLOCK	IR/KEY	SHEET	9 / 50

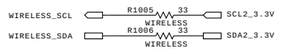
WIRELESS READY MODEL

DUAL COMPONENT	
D1001,D1002	1ST : EAH42720601 2ND : EAH60994401
Q1001	1ST : EBK61012601, 2ND : 0TRDI80002A
Q1002	1ST : EBK60752501, 2ND : EBK61011501

Wireless power



Wireless I2C connection with I2C_1
Address : 0X20

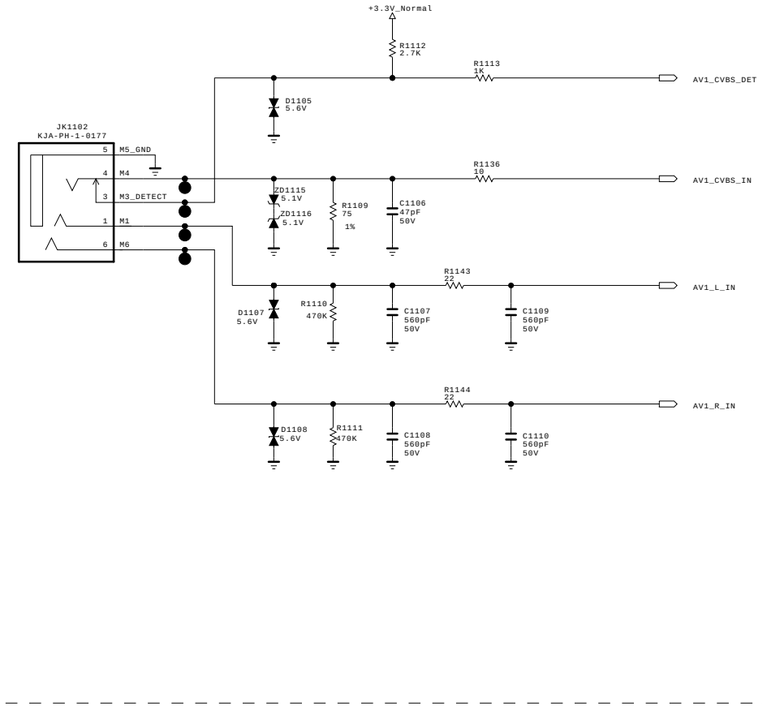


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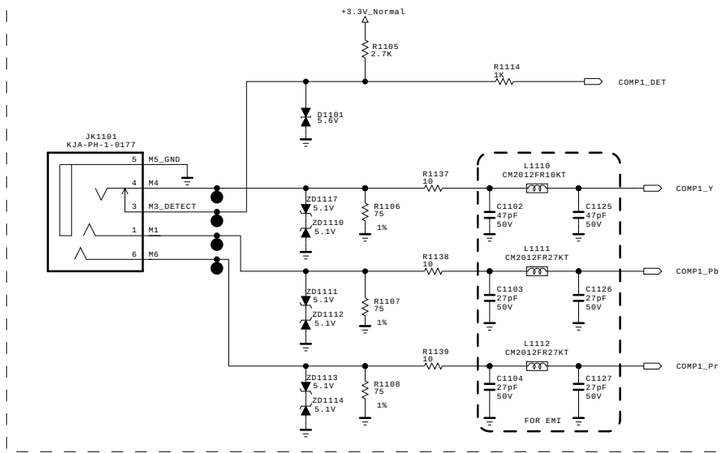
SECRET
LGElectronics

LG ELECTRONICS

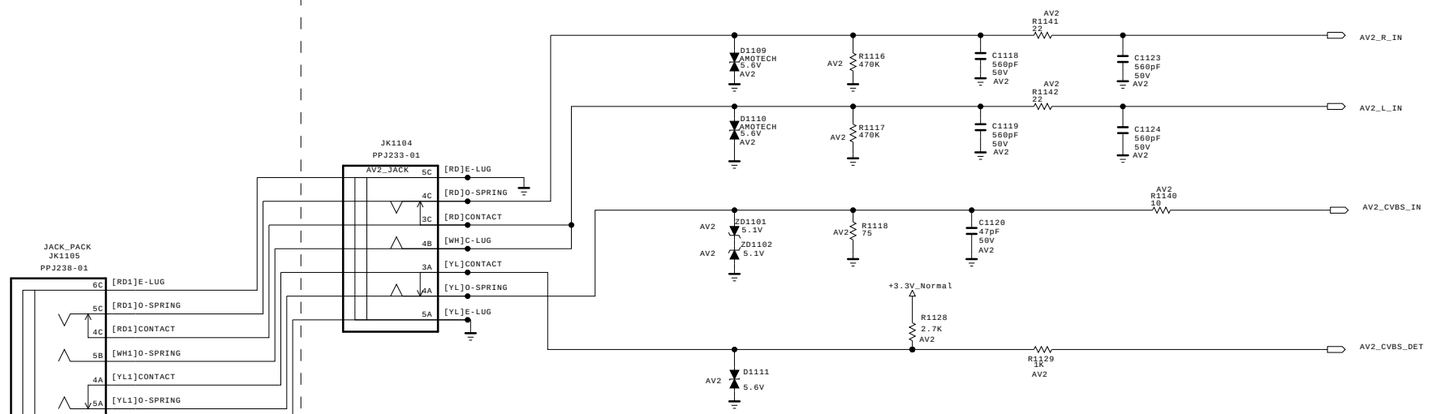
CVBS 1 PHONE JACK



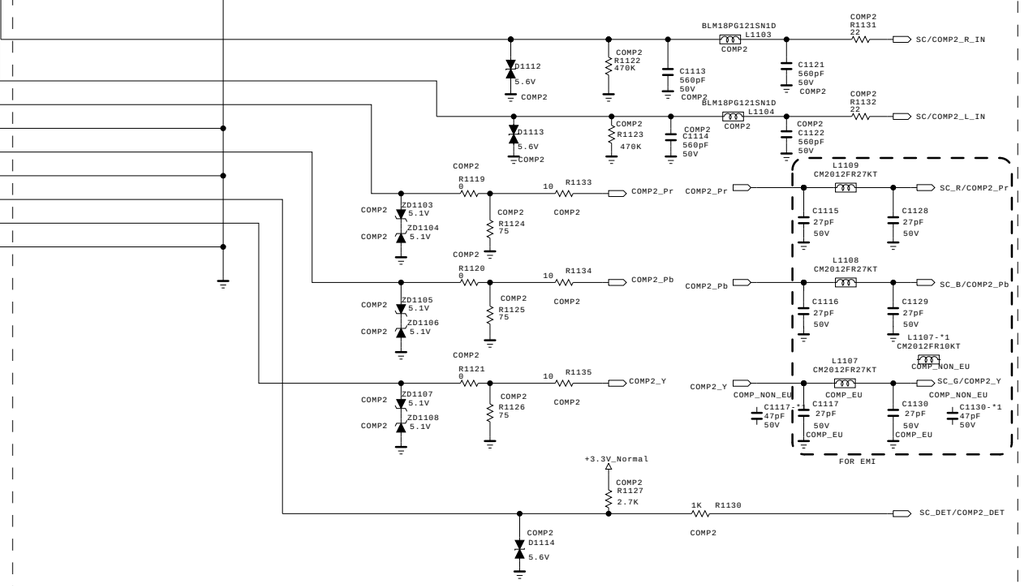
COMPONENT 1 PHONE JACK



CVBS2 REAR JACK



COMP2 REAR JACK



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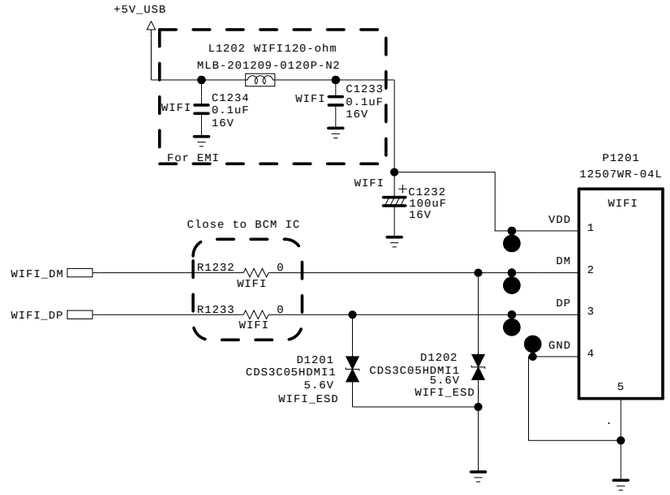
SECRET

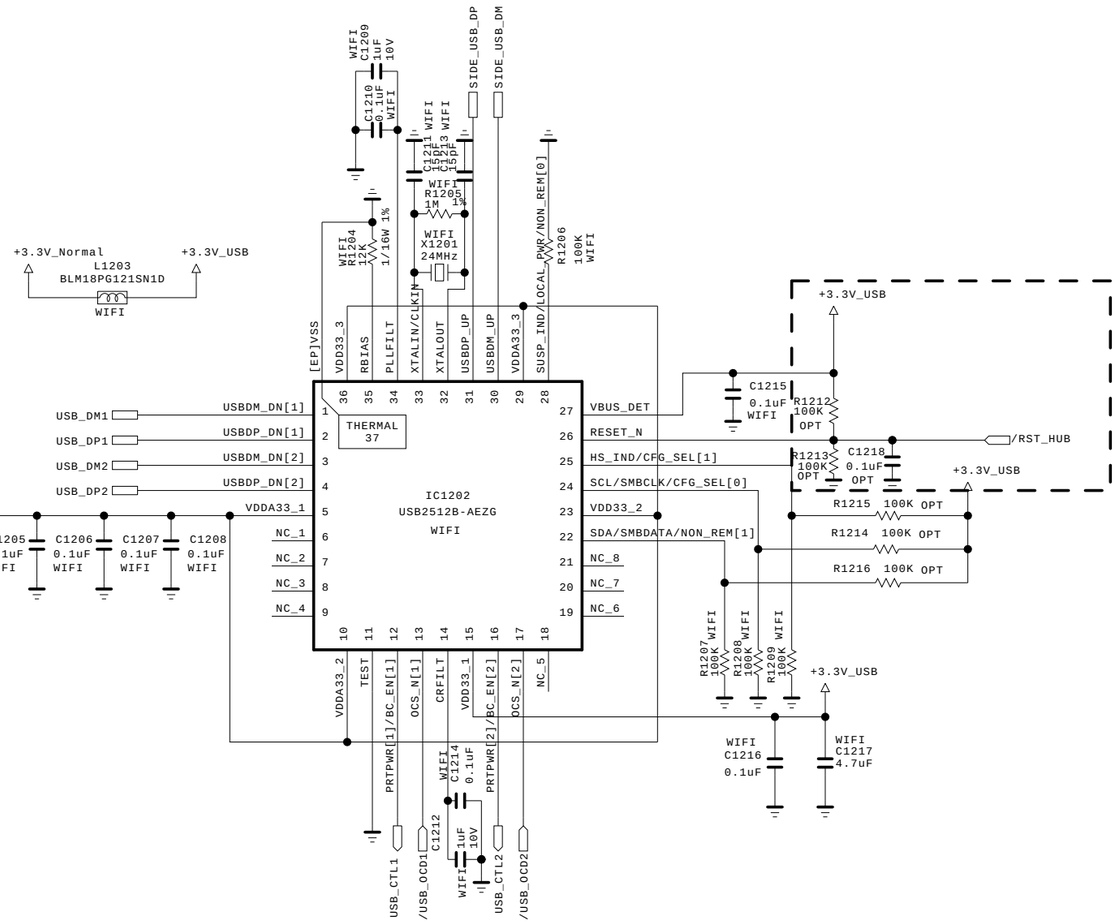
LGElectronics

LG ELECTRONICS

MODEL	BCM35230	DATE	
BLOCK	COMP/AV	SHEET	11 / 50

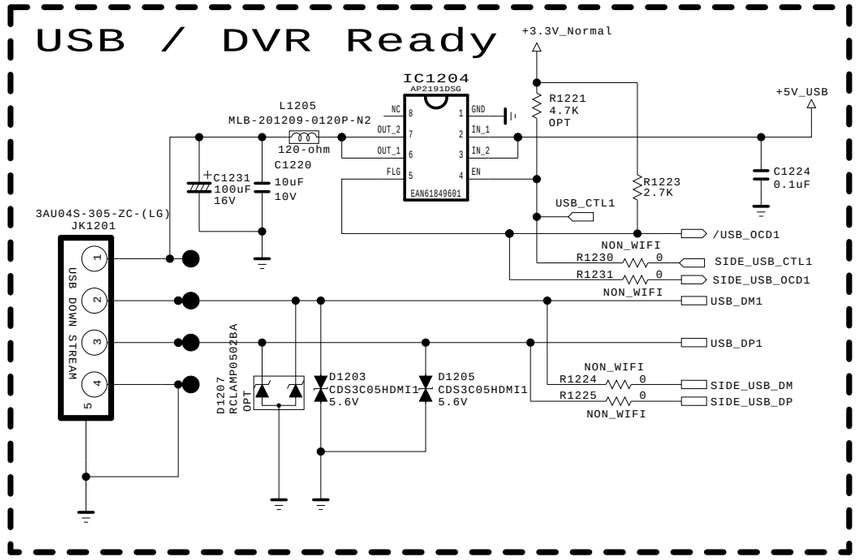
USB_WIFI



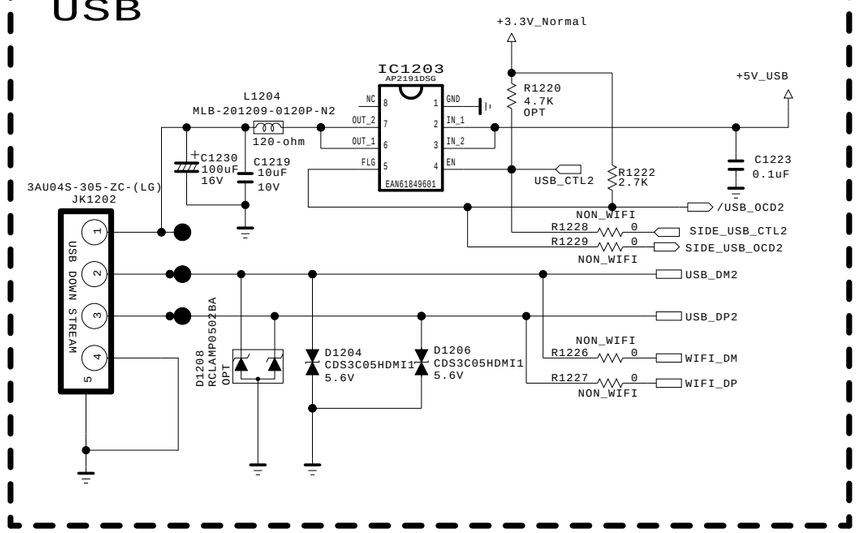


DUAL COMPONENT	
D1201,D1202 D1203,D1204 D1205,D1206	1ST : EAH42720601 2ND : EAH60994401

USB / DVR Ready



USB



THE ⚠ SYMBOL MARK OF THIS SCHEMETIC DIAGRAM INCORPORATES SPECIAL FEATURES IMPORTANT FOR PROTECTION FROM X-RADIATION. FILRE AND ELECTRICAL SHOCK HAZARDS, WHEN SERVICING IF IS ESSENTIAL THAT ONLY MANUFATURES SPECFIED PARTS BE USED FOR THE CRITICAL COMPONENTS IN THE ⚠ SYMBOL MARK OF THE SCHEMETIC.

SECRET

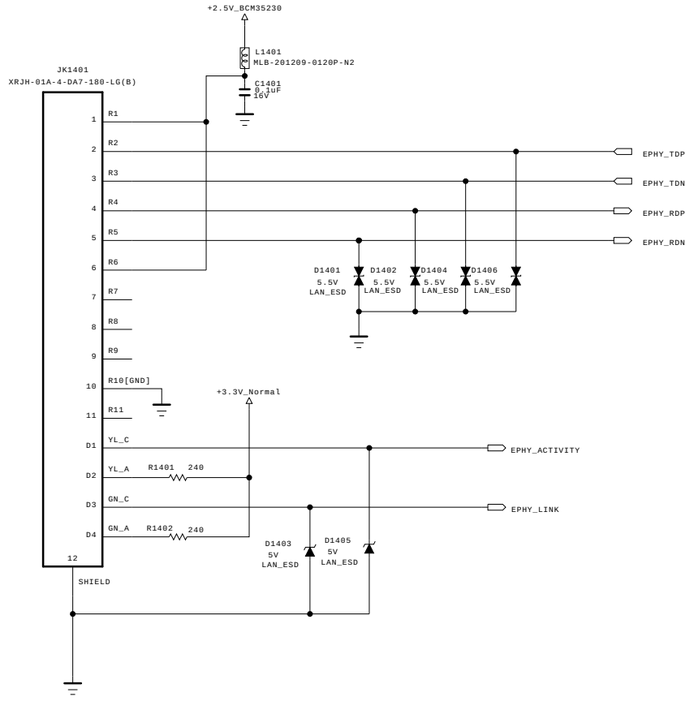
LGElectronics

LG ELECTRONICS

MODEL	BCM35230	DATE	
BLOCK	USB + WIFI	SHEET	12

Ethernet Block

DUAL COMPONENT	
D1401,D1402 D1403,D1404 D1405,D1406	1ST : EAH42720601 2ND : EAH60994401



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SECRET

LGElectronics

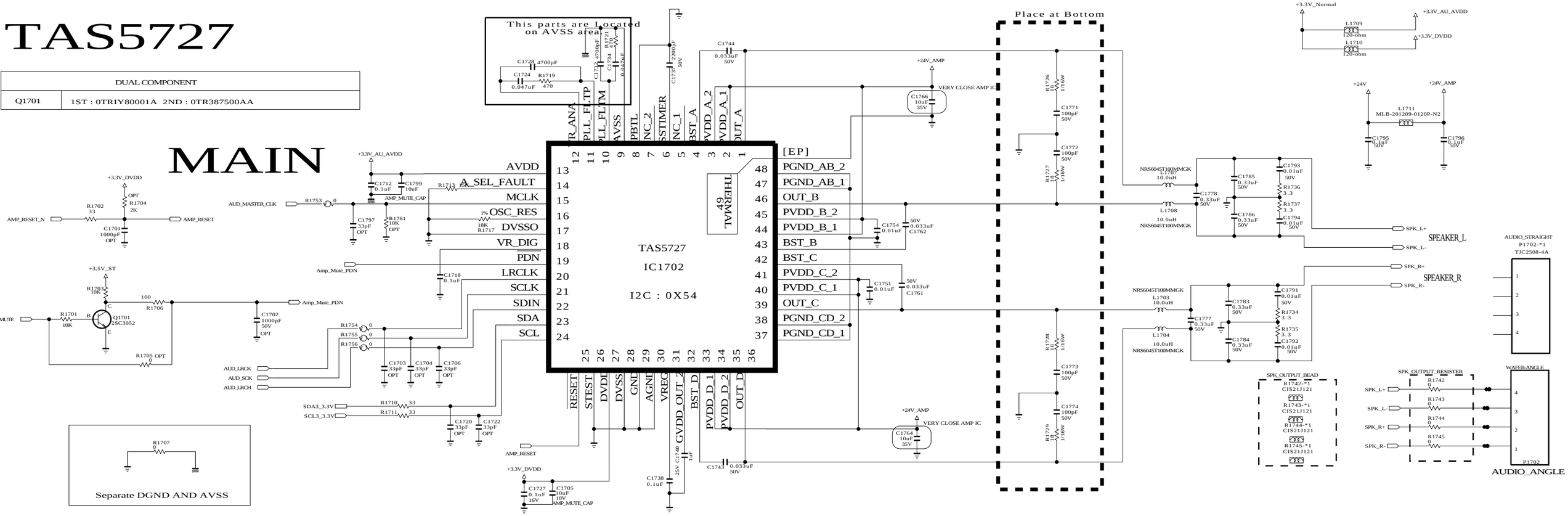
LG ELECTRONICS

MODEL	BCM35230	DATE	
BLOCK	ETHERNET	SHEET	14 / 50

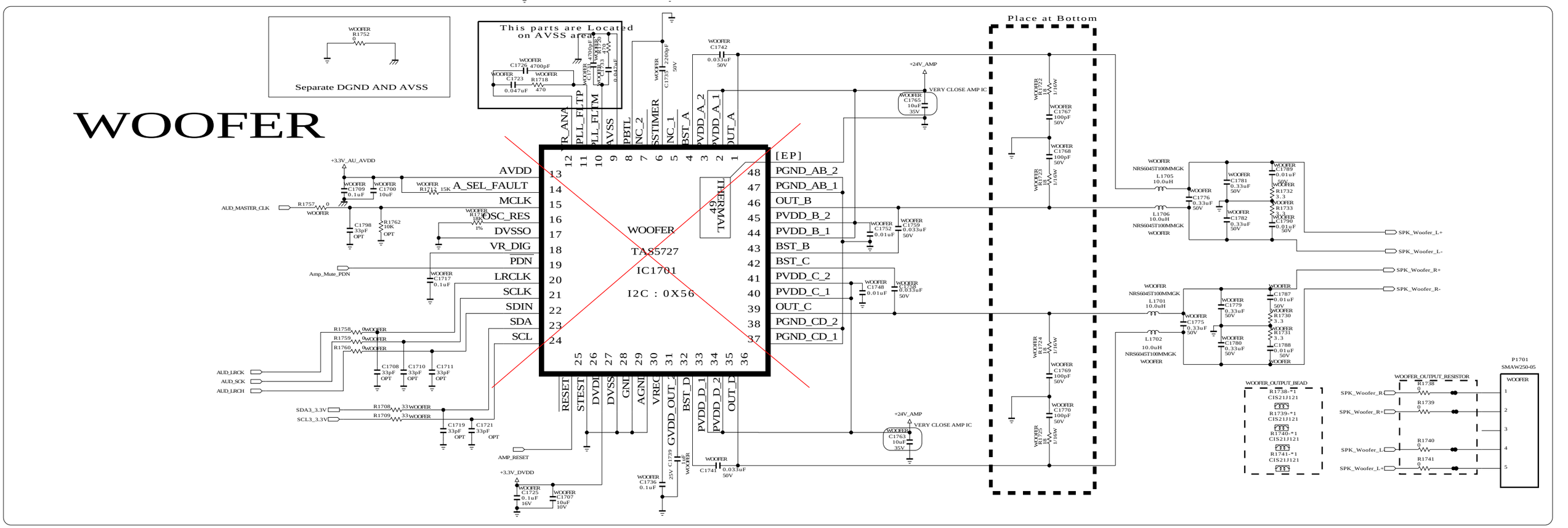
TAS5727

DUAL COMPONENT	
Q1701	1ST : 0TRIY80001A 2ND : 0TR387500AA

MAIN



WOOFER



THE ⚠ SYMBOL MARK OF THIS SCHEMETIC DIAGRAM INCORPORATES SPECIAL FEATURES IMPORTANT FOR PROTECTION FROM X-RADIATION. FILRE AND ELECTRICAL SHOCK HAZARDS, WHEN SERVICING IF IS ESSENTIAL THAT ONLY MANUFATURES SPECFIED PARTS BE USED FOR THE CRITICAL COMPONENTS IN THE ⚠ SYMBOL MARK OF THE SCHEMETIC.

SECRET

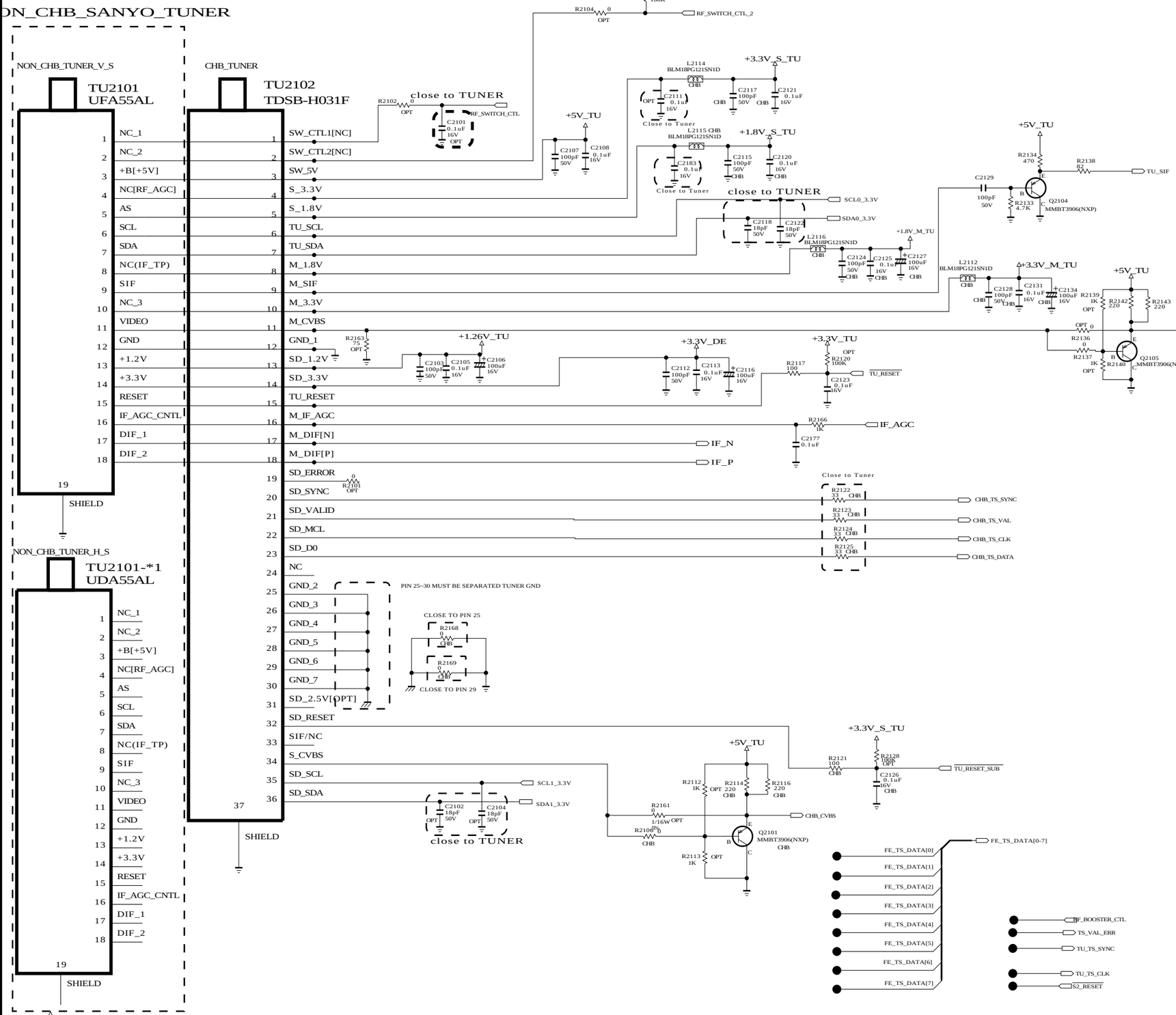
LGElectronics

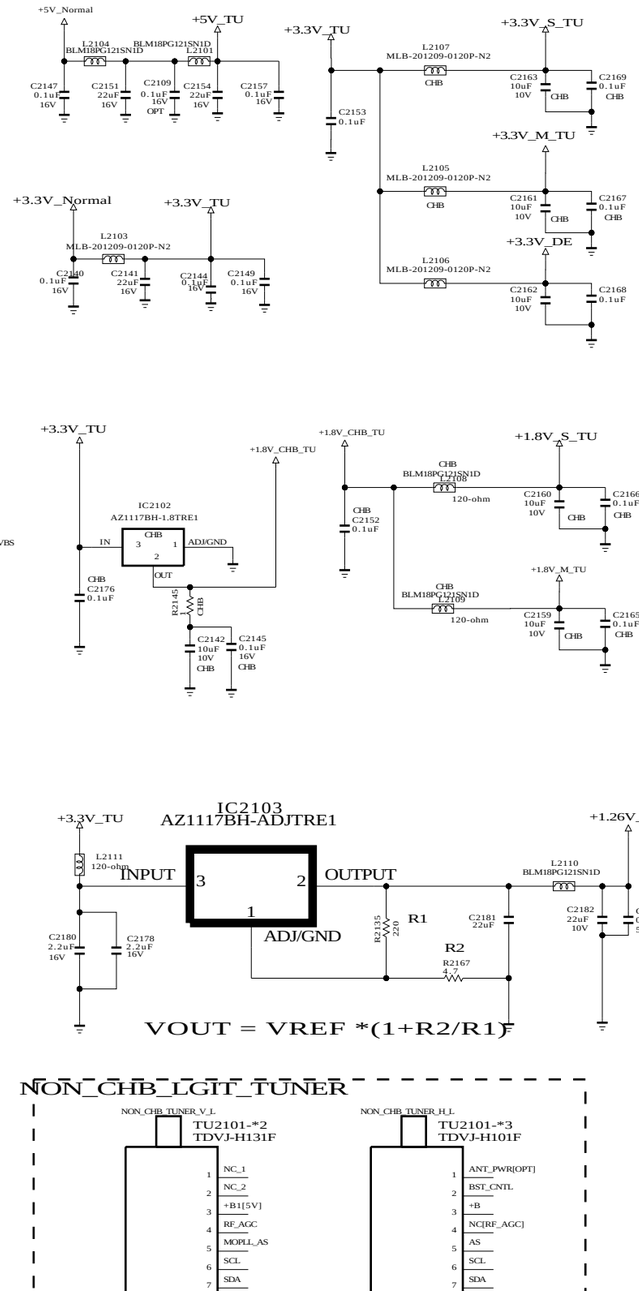
LG ELECTRONICS

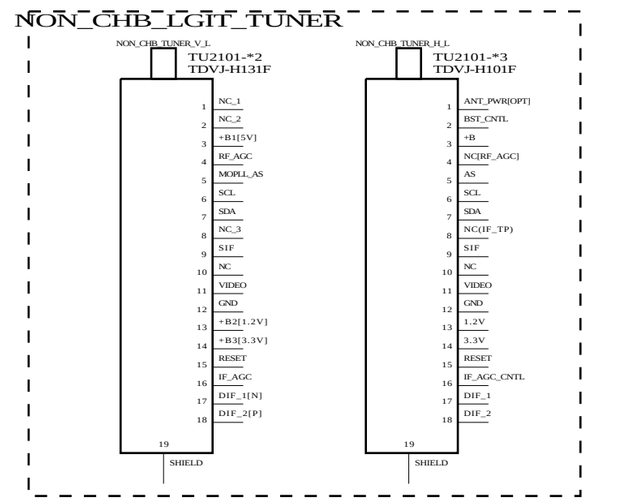
MODEL	BCM35230	DATE	
BLOCK	AUDIO[TI]	SHEET	17 / 50

NON_CHB & CHB TUNER (KOR/USA)

DUAL COMPONENT	
IC2102	1ST : EAN61829801, 2ND : EAN544289201
IC2103	1ST : EAN61507501, 2ND : EAN54428101







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SECRET

LGElectronics

LG ELECTRONICS

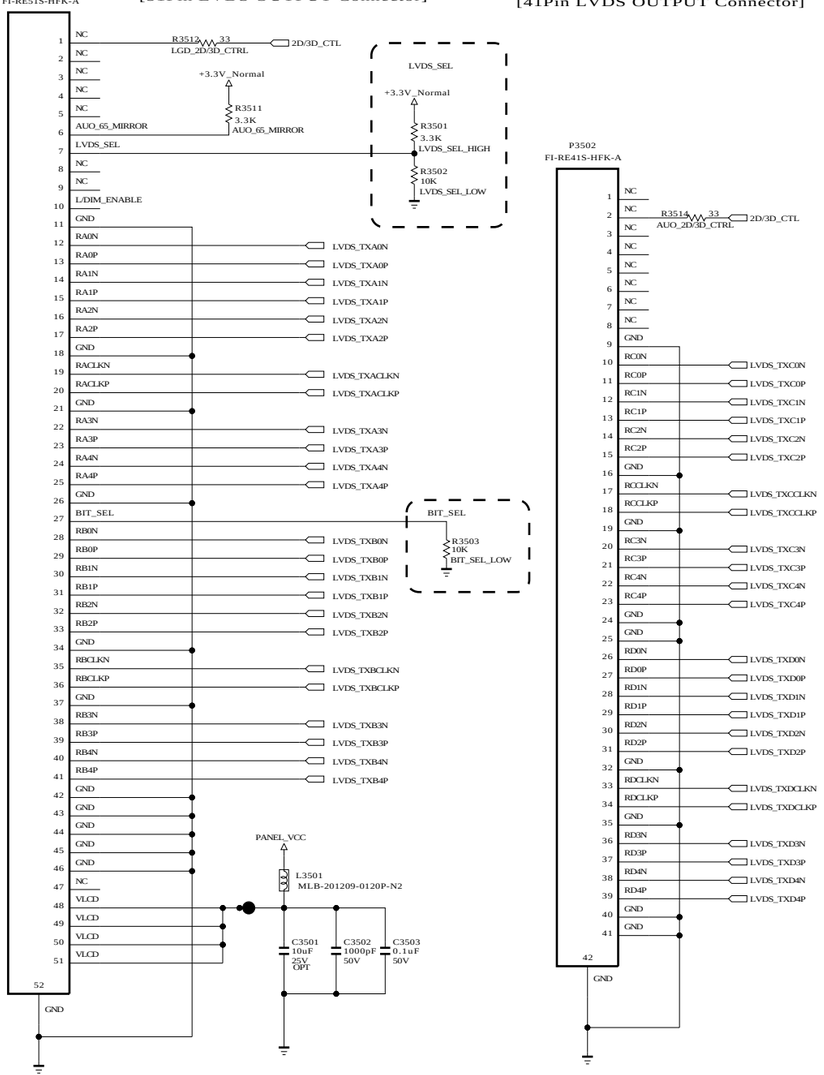
MODEL	BCM35230	DATE	
BLOCK	ATSC_TUNER	SHEET	21 / 50

LVDS

P3501
FI-RE51S-HFK-A

[51Pin LVDS OUTPUT Connector]

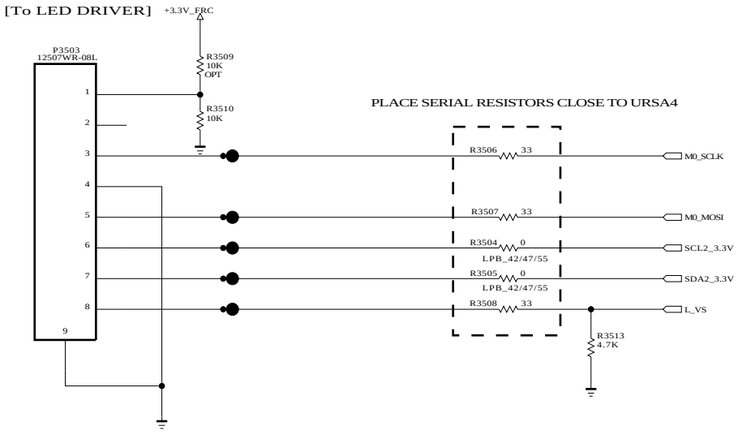
[41Pin LVDS OUTPUT Connector]



P3502
FI-RE41S-HFK-A

LOCAL DIMMING

[To LED DRIVER]



NON USED L/DIMMING (FOR EDGE_LED)

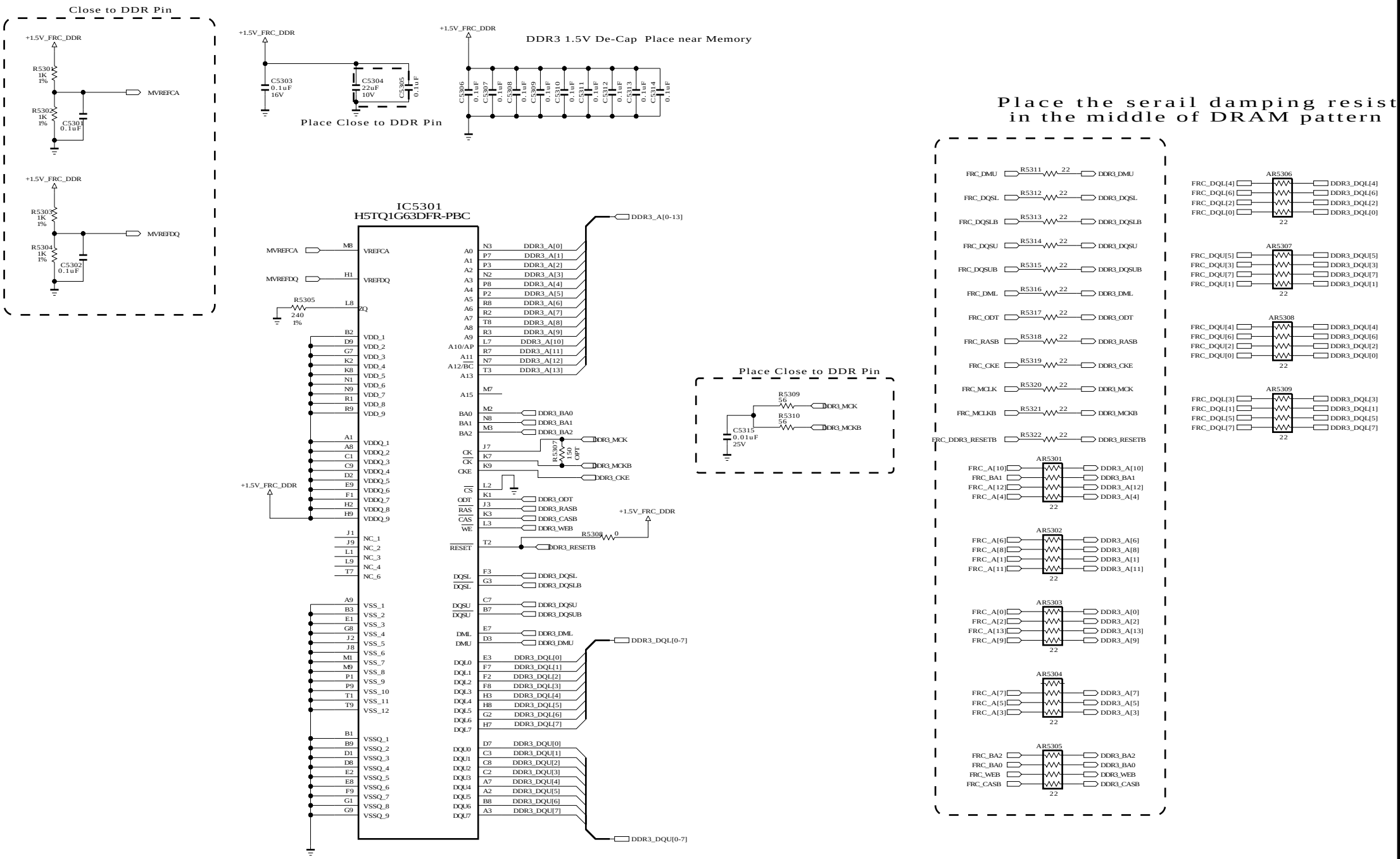


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SECRET
LGElectronics

LG ELECTRONICS

+1.26V_FRC
L5205 CIC21J501NE
C5201 0.1uF
C5210 22uF 10V
C5211 22uF 10V
VDDC10
C5243 6.3V
C5225 0.1uF
C5228 0.1uF
+1.5V_FRC_DDR
C5213 0.1uF
C5244 0.22uF 6.3V
C5231 0.1uF
C5232 0.1uF
C5234 0.1uF
C5247 1uF 6.3V
+1.26V_FRC
L5201 CIC21J501NE
C5202 0.1uF
C5246 22uF 10V
C5206 0.1uF
DVDD_DDR_1V
Place Close to Bead
+3.3V_FRC
L5202 CIC21J501NE
C5203 0.1uF
C5207 0.1uF
VDD33
C5214 0.1uF
C5219 0.1uF
C5245 0.22uF 6.3V
VDD33 (VDDP)
+3.3V_FRC
L5206 CIC21J501NE
C5233 0.1uF
C5236 0.1uF
AVDD33
C5238 0.1uF
C5239 0.1uF
AVDD33
+3.3V_FRC
L5203 CIC21J501NE
C5204 0.1uF
C5208 0.1uF
AVDD_PLL
C5215 10uF 6.3V
C5217 0.1uF
AVDD_PLL
+3.3V_FRC
L5204 CIC21J501NE
C5205 0.1uF
C5209 0.1uF
AVDD_LVDS_3.3V
C5216 0.1uF
C5220 0.1uF
C5223 0.1uF
C5227 0.1uF
AVDD_LVDS_3.3V
GPIO1 : HI => B8/94, LOW => B4/98
CHIP_CONF : {GPIO8, PWM1, PWM0}
CHIP_CONF = 3'd5 : boot from interal SRAM
CHIP_CONF = 3'd6 : boot from EEPROM
CHIP_CONF = 3'd7 : boot from SPI Flash
URSA5 CONFIGURATION
+3.3V_FRC
R5210 10K
R5211 10K OPT
R5212 10K OPT
R5213 10K
PWM0
PWM1
GPIO[8]
GPIO[1]
R5208 10K
R5209 10K OPT
R5214 10K OPT
R5215 10K
URSA5 H/W OPTION
+3.3V_FRC
LVDS_EXT_URSA5 4.7K/5%
LVDS_S7M_PLUS 4.7K/5%
L/DIM_EDGE_32/37
L/DIM_EDGE_42/47/55
R5216 10K
R5217 10K
R5218 10K
R5219 10K OPT
R5220 10K
R5221 10K OPT
R5222 10K
R5223 10K OPT
URSA_MODEL_OPT_0
URSA_MODEL_OPT_1
URSA_MODEL_OPT_2
2D/3D_CTL
MODEL OPTION
PIN NAME | P1N NO. | HIGH | LOW
MODEL_OPT_0 | D10 | L/DIM_10BLOCK | L/DIM_16BLOCK
MODEL_OPT_1 | D11 | RESERVED | RESERVED
MODEL_OPT_2 | D12 | LVDS_EXT_URSA5 | LVDS_S7M_PLUS
MODEL_OPT_3 | D13 | RESERVED | RESERVED
Debugging for URSA5
P5201
12507WR-04L
URSA5_DEBUG
URSA5_DEBUG R5201 22 SCL2_+3.3V_DB
URSA5_DEBUG R5202 22 SDA2_+3.3V_DB
SW5201
JS2235S
SCL2_3.3V
R5258 0 URSA5_MP
SCL2_+3.3V_URSA
R5260 0 OPT
SCL2_+3.3V_DB
URSA5_DEBUG
R5259 0 URSA5_MP
SDA2_3.3V
SDA2_+3.3V_URSA
R5261 0 OPT
SDA2_+3.3V_DB
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PLACE TERMINATION RESISTORS CLOSE TO URSA5
AVDD33 F4 F5
1.5V_FRC_DDR F10 G10 F11 F12 G11 G12
AVDD_LVDS_3.3V D4 D5 E4 E5
AVDD_PLL M5 L4 L5
VDDP_DDR_1V L10 K9 M4 N4 N5
VDD33 M9 M10 N9 N10 N11 P10 P11
VDDC10
DDR3_A0/DDR2_NC
DDR3_A1/DDR2_A8
DDR3_A2/DDR2_NC
DDR3_A3/DDR2_A10
DDR3_A4/DDR2_A2
DDR3_A5/DDR2_A3
DDR3_A6/DDR2_A4
DDR3_A7/DDR2_A5
DDR3_A8/DDR2_A6
DDR3_A9/DDR2_A9
DDR3_A10/DDR2_RASZ
DDR3_A11/DDR2_A11
DDR3_A12/DDR2_A0
DDR3_A13/DDR2_A12
FRC_A[0-13]
FRC_A[0] P14
FRC_A[1] G15
FRC_A[2] N14
FRC_A[3] L15
FRC_A[4] H15
FRC_A[5] L14
FRC_A[6] G14
FRC_A[7] N12
FRC_A[8] G13
FRC_A[9] N13
FRC_A[10] H14
FRC_A[11] F15
FRC_A[12] H13
FRC_A[13] P13
FRC_BA0 M12
FRC_BA1 H12
FRC_BA2 L13
DDR3_BA0/DDR2_BA2
DDR3_BA1/DDR2_CASZ
DDR3_BA2/DDR2_A1
FRC_MCLK F16
FRC_MCLKB F17
FRC_CKE J13
DDR3_MCLK/DDR2_MCLK
DDR3_MCLKZ/DDR2_MCLKZ
DDR3_CKE/DDR2_ODT
FRC_ODT K12
FRC_RASB L12
FRC_CASB K13
FRC_WEB K14
DDR3_ODT/DDR2_CKE
DDR3_RASZDDR2_WEZ
DDR3_CASZ/DDR2_BA1
DDR3_WEZ/DDR2_BA0
FRC_DDR3_RESETB M14
DDR3_RESET/DDR2_A7
FRC_DQSL N16
FRC_DQSU M17
DDR3_DQSL/DDR2_DQSL
DDR3_DQSU/DDR2_DQSU
FRC_DQSLB M16
FRC_DQSUB M15
DDR3_DQSBL/DDR2_DQSBL
DDR3_DQSBU/DDR2_DQSBU
FRC_DML J15
FRC_DMU R16
DDR3_DQML/DDR2_DQU5
DDR3_DQMU/DDR2_DQU4
FRC_DQL[0-7]
FRC_DQL[0] R17
FRC_DQL[1] H17
FRC_DQL[2] R15
FRC_DQL[3] J17
FRC_DQL[4] T17
FRC_DQL[5] H16
FRC_DQL[6] T15
FRC_DQL[7] G16
DDR3_DQL0/DDR2_DQU3
DDR3_DQL1/DDR2_DQL0
DDR3_DQL2/DDR2_DQL6
DDR3_DQL3/DDR2_DQL7
DDR3_DQL4/DDR2_DQL3
DDR3_DQL5/DDR2_DQL2
DDR3_DQL6/DDR2_DQL1
DDR3_DQL7/DDR2_DQL5
FRC_DQU[0-7]
FRC_DQU[0] K15
FRC_DQU[1] N15
FRC_DQU[2] K17
FRC_DQU[3] P17
FRC_DQU[4] L17
FRC_DQU[5] P16
FRC_DQU[6] K16
FRC_DQU[7] P15
DDR3_DQU0/DDR2_DQU7
DDR3_DQU1/DDR2_DQML
DDR3_DQU2/DDR2_DQU2
DDR3_DQU3/DDR2_DQU6
DDR3_DQU4/DDR2_NC
DDR3_DQU5/DDR2_DQU1
DDR3_DQU6/DDR2_DQU0
DDR3_DQU7/DDR2_DQMU
DDR3_NC/DDR2_A13
DDR3_NC/DDR2_DQL4
+3.3V_FRC
R5220 4.7K OPT
R5221 4.7K OPT
SCL2_+3.3V_URSA
SDA2_+3.3V_URSA
R5222 33 P1
R5223 33 P2
I2CM_SCL D14
I2CM_SDA D15
I2CS_SCL P1
I2CS_SDA P2
TXDCLKP TXDCLKN TXD0P TXD0N TXD1P TXD1N TXD2P TXD2N TXD3P TXD3N TXD4P TXD4N
R5224 100
R5225 100
R5226 100
R5227 100
R5228 100
R5229 100
TXACLKP TXACLKN TXA0P TXA0N TXA1P TXA1N TXA2P TXA2N TXA3P TXA3N TXA4P TXA4N
R5230 100
R5231 100
R5232 100
R5233 100
R5234 100
R5235 100
C5241 13pF
X5201 24MHz
C5242 13pF
1M R5237
R5238 0
GPIO[11] GPIO[10] GPIO[8]
L_VS
R5239 33
R2 R3 R4 R5 T4 U4 U3 T3 T2 U2 T1 R1
R6 R7 R8 R9 T8 U8 T7 T6 U6 U5 T5
J1 J2 R13 P9 T13 U15 R14 N2 N1 P8 U14 U13 R12 P11
RXBCLKP RXBCLKN RXB0P RXB0N RXB1P RXB1N RXB2P RXB2N RXB3P RXB3N RXB4P RXB4N
RXACLKP RXACLKN RXA0P RXA0N RXA1P RXA1N RXA2P RXA2N RXA3P RXA3N RXA4P RXA4N
XTALO XTALI
GPIO0/(UART_RX/S_PIF_DA0) GPIO1 GPIO2/(S_PIF_CLK) GPIO3/(LTD_DA1) GPIO4/(LTD_DE) GPIO5/(LTD_CLK) GPIO6/(LTD_DA0) GPIO7/(3D_FLAG) GPIO8 GPIO9/(UART_TX/S_PIF_DA1) GPIO10/(S_PIF_CS) GPIO11/(S_PIF_DC) VSYNC_LIKE
M_S_PIF_CLK M_S_PIF_CS M_S_PIF_DA0 M_S_PIF_DA1 M_S_PIF_FC
S_M_PIF_CLK S_M_PIF_CS S_M_PIF_DA0 S_M_PIF_DA1 S_M_PIF_FC
L1 M2 K2 K3 L3
SPDIF_IST_L SPDIF_IST_R
R10 T11
DP_SYNC_L DP_SYNC_R
TXA0P/GCLK6/BLUE[7] C8
TXA0N/GCLK5/BLUE[6] C9
TXA1P/OPT_N/LK3/BLUE[9] B8
TXA1N/FLK/BLUE[8] A8
TXA2P/GREEN[1] A7
TXA2N/OPT_P/LK2/GREEN[0] B7
TXACLKP/RLV0N/GREEN[3] C6
TXACLKN/RLV0P/GREEN[2] C7
TXA3P/RLV1N/GREEN[5] B6
TXA3N/RLV1P/GREEN[4] A6
TXA4P/RLV2N/GREEN[7] A5
TXA4N/RLV2P/GREEN[6] B5
TXB0P/RLV3N/GREEN[9] C4
TXB0N/RLV3P/GREEN[8] C5
TXB1P/RLVCLKN/RED[1] B4
TXB1N/RLVCLKP/RED[0] A4
TXB2P/RLV4P/RED[3]/EPI_A3P A3
TXB2N/RLV4N/RED[2]/EPI_A3N B3
TXBCLKP/RLV5N/RED[5]/EPI_A2P C2
TXBCLKN/RLV5P/RED[4]/EPI_A2N C3
TXB3P/RLV6N/RED[7]/EPI_A1P B2
TXB3N/RLV6P/RED[6]/EPI_A1N A2
TXB4P/RLV7N/RED[9]/EPI_A0P C1
TXB4N/RLV7P/RED[8]/EPI_A0N B1
TXC0P/SOE C16
TXC0N/POL B17
TXC1P/GSP_R B16
TXC1N/GSP/VST A16
TXC2P/GOE/GCLK1 A15
TXC2N/GSC/GCLK3 B15
TXCCLKP/LLV0N C14
TXCCLKN/LLV0P C15
TXC3P/LLV1N B14
TXC3N/LLV1P A14
TXC4P/LLV2N A13
TXC4N/LLV2P B13
TXD0P/LLV3N C12
TXD0N/LLV3P C13
TXD1P/LLVCLKN B12
TXD1N/LLVCLKP A12
TXD2P/LLV4N/EPI_B3P A11
TXD2N/LLV4P/EPI_B3N B11
TXDCLKP/LLV5N/BLUE[1]/EPI_B2P C10
TXDCLKN/LLV5P/BLUE[0]/EPI_B2N C11
TXD3P/LLV6N/BLUE[3] B10
TXD3N/LLV6P/BLUE[2]/EPI_B1N A10
TXD4P/LLV7N/BLUE[5]/EPI_B0P A9
TXD4N/LLV7P/BLUE[4]/EPI_B0N B9
MOD_GPIO0/VDD_ODD/HSYNC D10
MOD_GPIO1/VDD_EVEN/VSYNC D11
MOD_GPIO2/PWM13/GCLK4/LCK D12
MOD_GPIO3/PWM14/GCLK2/LDE D13
PWM0/SCAN_BLK1 U12
PWM1/SCAN_BLK2 T12
LPLL_FBCLK G3
LPLL_OUTCLK E17
LPLL_REFIN H3
R5253 3D_SG 33 3D_SYNC_RF
R5250 33 PWM0
R5251 33 PWM1
VSS_1 D6
VSS_2 D7
VSS_3 D9
VSS_4 E6
VSS_5 E7
VSS_6 E8
VSS_7 E9
VSS_8 E10
VSS_9 E16
VSS_10 F3
VSS_11 F4
VSS_12 F7
VSS_13 F8
VSS_14 F9
VSS_15 G1
VSS_16 G2
VSS_17 G4
VSS_18 G5
VSS_19 G6
VSS_20 G7
VSS_21 G8
VSS_22 G9
VSS_23 G17
VSS_24 H1
VSS_25 H2
VSS_26 H4
VSS_27 H5
VSS_28 H6
VSS_29 H7
VSS_30 H8
VSS_31 H9
VSS_32 H10
VSS_33 H11
VSS_34 J4
VSS_35 J5
VSS_36 J6
VSS_37 J7
VSS_38 J8
VSS_39 J9
VSS_40 J10
VSS_41 J11
VSS_42 J12
VSS_43 J14
VSS_44 J16
VSS_45 K4
VSS_46 K5
VSS_47 K6
VSS_48 K7
VSS_49 K8
VSS_50 K11
VSS_51 K16
VSS_52 L7
VSS_53 L8
VSS_54 L11
VSS_55 L16
VSS_56 M6
VSS_57 N6
VSS_58 M8
VSS_59 M11
VSS_60 N6
VSS_61 N7
VSS_62 N8
VSS_63 N17
VSS_64 P3
VSS_65 P4
VSS_66 P5
VSS_67 P6
VSS_68 P7
VSS_69 P12
VSS_70 U16
VSS_71
VSS_72
NC L9
J3
HW_RESET D1
TESTPIN_1 D2
TESTPIN_2 D3
TESTPIN_3 E1
TESTPIN_4 E2
TESTPIN_5 F1
TESTPIN_6 F2
TESTPIN_7 C17
TESTPIN_8 D16
M0_SCLK D17
M0_MOSI E15
M1_SCLK E14
M1_MOSI E13
M2_SCLK E12
M2_MOSI F13
M3_SCLK T9
M3_MOSI T10
SPI_CK R5247 33
SPI_CZ R5248 33
SPI_DI R5249 33
SPI_DO
[SPI FLASH(2Mbit)]
+3.3V_FRC
IC5202 W25X20BVSNIG
R5244 4.7K
R5246 10K
SPI_CS
R5245 33
SPI_DO
CS 1
DO 2
WP 3
GND 4
VCC 8
HOLD 7
CLK 6
DIO 5
R5252 3.3K
SPI_SCLK
SPI_DI
URSA5_FLASH_WINBOND_2M
IC5202-*1
MX25L2006EM1I-12G, HF
CS 1
SO/SIO1 2
WP 3
GND 4
VCC 8
HOL 7
SCL 6
SI/S 5
URSA5_FLASH_MACRONIX_2M
IC5201
LGE7303C
Q5202 AO3407A
R5219 10K OPT
R5255 22K URSA5_UO2_RESET
C5212 4.7uF 16V URSA5_UO2_RESET
URSA5_UO2_RESET
R5262 2.2K URSA5_UO2_RESET
FRC_RESET
R5254 4.7K URSA5_UO2_RESET
Q5201 2SC3052 URSA5_UO2_RESET
R5256 10K OPT
R5243 33 URSA5_UO3_RESET
NON USED
BCM35230 LVDS CHC/D
TXC0N TXC0P TXC1N TXC1P TXC2N TXC2P TXCCLKN TXCCLKP TXC3N TXC3P TXC4N TXC4P TXD0N TXD0P TXD1N TXD1P TXD2N TXD2P TXDCLKN TXDCLKP TXD3N TXD3P TXD4N TXD4P
SECRET
LGElectronics
LG ELECTRONICS
MODEL | MStar URSA5 | DATE | 2010. 08.18
BLOCK | FRC block | SHEET | 52 / 55



THE ⚠ SYMBOL MARK OF THIS SCHEMETIC DIAGRAM INCORPORATES SPECIAL FEATURES IMPORTANT FOR PROTECTION FROM X-RADIATION. FILRE AND ELECTRICAL SHOCK HAZARDS, WHEN SERVICING IF IS ESSENTIAL THAT ONLY MANUFATURES SPECFIED PARTS BE USED FOR THE CRITICAL COMPONENTS IN THE ⚠ SYMBOL MARK OF THE SCHEMETIC.

SECRET

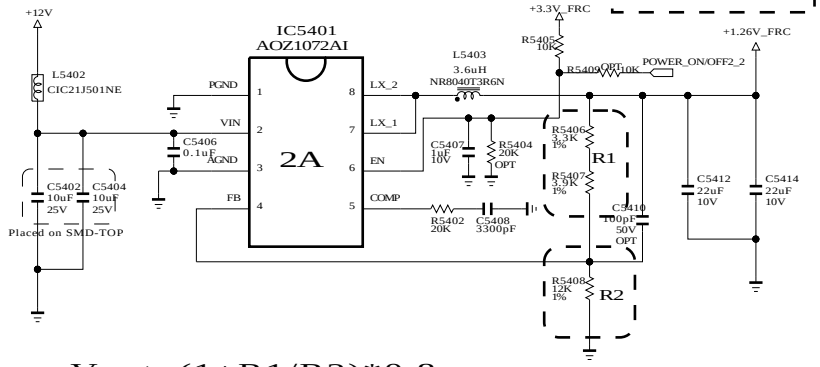
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MODEL	MStar URSA5	DATE	2010. 08.18
BLOCK	DDR3 4Mbit	SHEET	53 / 55

CORE +1.26V_FRC

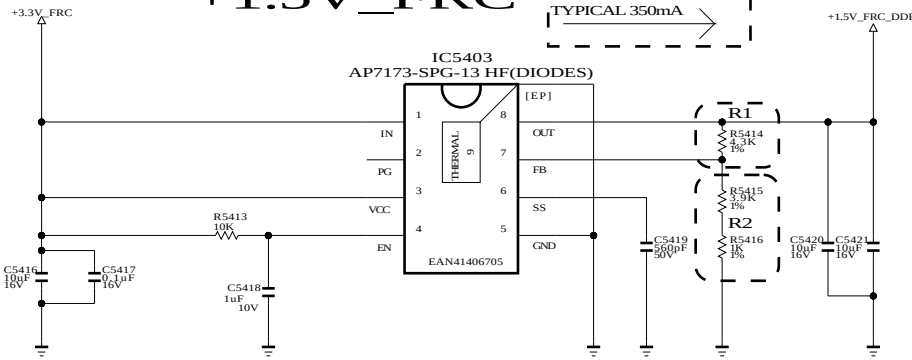
TYPICAL 980mA



Vout=(1+R1/R2)*0.8

+1.5V_FRC

TYPICAL 350mA

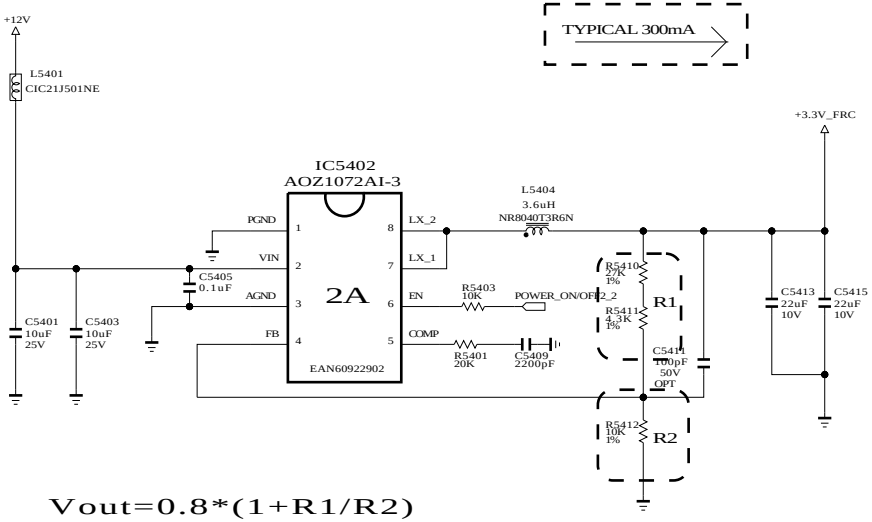


Vout=0.6*(1+R1/R2)

+1.5V of DDR&URSA5 uses same power line

+3.3V_FRC

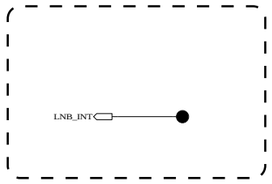
TYPICAL 300mA



Vout=0.8*(1+R1/R2)

THE ⚠5 SYMBOL MARK OF THIS SCHEMETIC DIAGRAM INCORPORATES SPECIAL FEATURES IMPORTANT FOR PROTECTION FROM X-RADIATION. FILRE AND ELECTRICAL SHOCK HAZARDS, WHEN SERVICING IF IS ESSENTIAL THAT ONLY MANUFATURES SPECFIED PARTS BE USED FOR THE CRITICAL COMPONENTS IN THE ⚠1 SYMBOL MARK OF THE SCHEMETIC.

Non_DVB-S2 LNB Part_Allegro

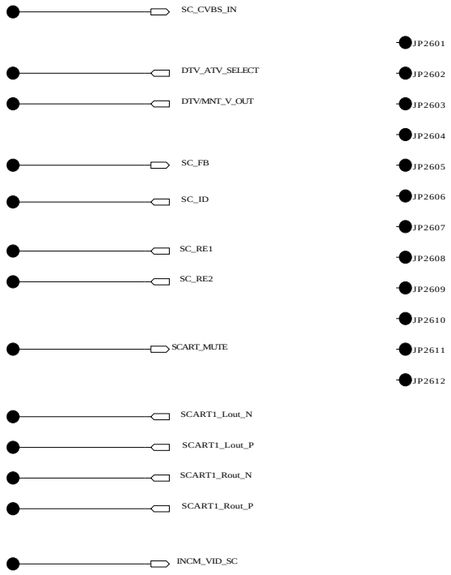


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MODEL	BCM35230	DATE	
BLOCK	NON LNB	SHEET	24 / 50



THE ⚠SYMBOL MARK OF THIS SCHEMETIC DIAGRAM INCORPORATES SPECIAL FEATURES IMPORTANT FOR PROTECTION FROM X-RADIATION. FILRE AND ELECTRICAL SHOCK HAZARDS, WHEN SERVICING IF IS ESSENTIAL THAT ONLY MANUFATURES SPECFIED PARTS BE USED FOR THE CRITICAL COMPONENTS IN THE ⚠SYMBOL MARK OF THE SCHEMETIC.

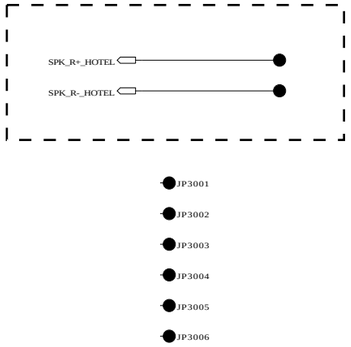
SECRET

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MODEL	BCM35230	DATE	
BLOCK	NON SCART	SHEET	26 / 50

NON CHINA HOTEL



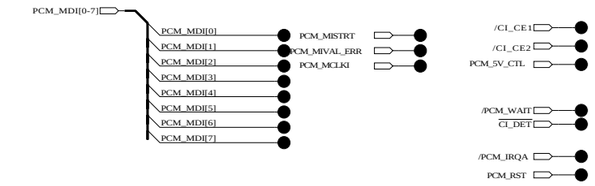
THE ⚠SYMBOL MARK OF THIS SCHEMETIC DIAGRAM INCORPORATES
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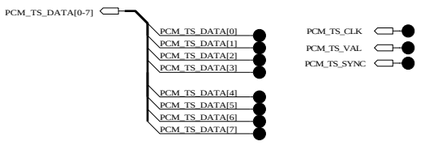
SECRET
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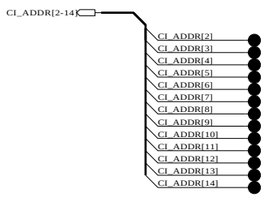
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MODEL	BCM35230	DATE	
BLOCK	NON CHINA HOTEL	SHEET	30 / 50

NON CI







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SECRET

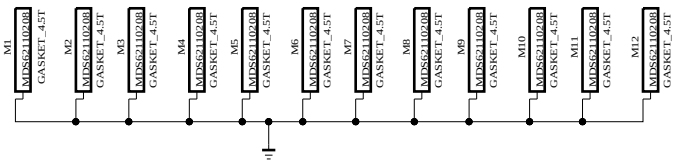
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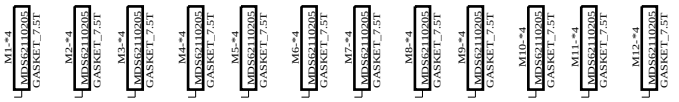
MODEL	BCM35230	DATE	
BLOCK	NON CI	SHEET	20 / 50

SMD GASKET

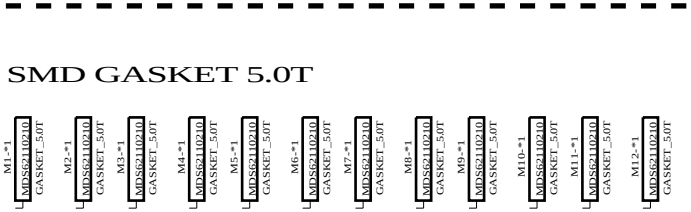
SMD GASKET 4.5T



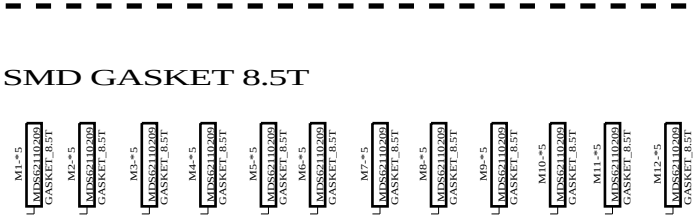
SMD GASKET 7.5T



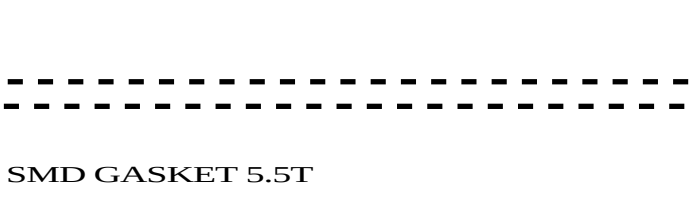
SMD GASKET 5.0T



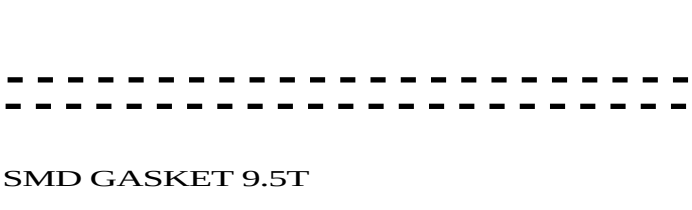
SMD GASKET 8.5T



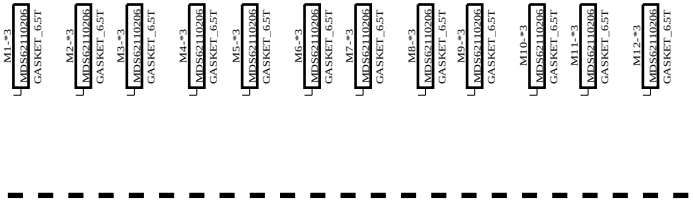
SMD GASKET 5.5T

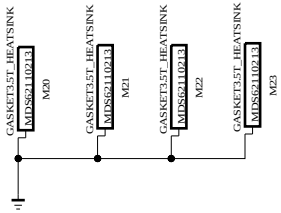


SMD GASKET 9.5T



SMD GASKET 6.5T





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SECRET

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MODEL	BCM35230	DATE	2010. 09. 18
BLOCK	SMD GASKET	SHEET	56 / 56