WM8521

Stereo DAC With Integrated Output Stage for 2Vrms LINE OUT

DESCRIPTION

The WM8521 is a 96kHz stereo DAC with an integrated output op-amp stage, designed to generate a 2.0Vrms output signal directly, so reducing external component requirements in digital audio applications.

WM8521 comes into two variants WM8521HC and WM8521H9 which offers different line drive output capabilities. WM8521HC outputs 2Vrms at 12V supply, while WM8521H9 outputs 2.0Vrms at 9V supply. WM8521HC/H9 are designed for cost sensitive consumer digital audio applications requiring 2Vrms line output.

A 24-bit multi-bit sigma delta DAC is used with oversampling digital interpolation filters. Digital audio input word lengths from 16-32 bits and sampling rates from 8kHz to 96kHz are supported.

The audio interface supports I^2S, Right Justified and DSP digital audio formats.

The devices are controlled via a hardware interface which provides access to features including de-emphasis, mute and data formats. These devices are pin equivalent and are available in a 14-pin SOIC package.

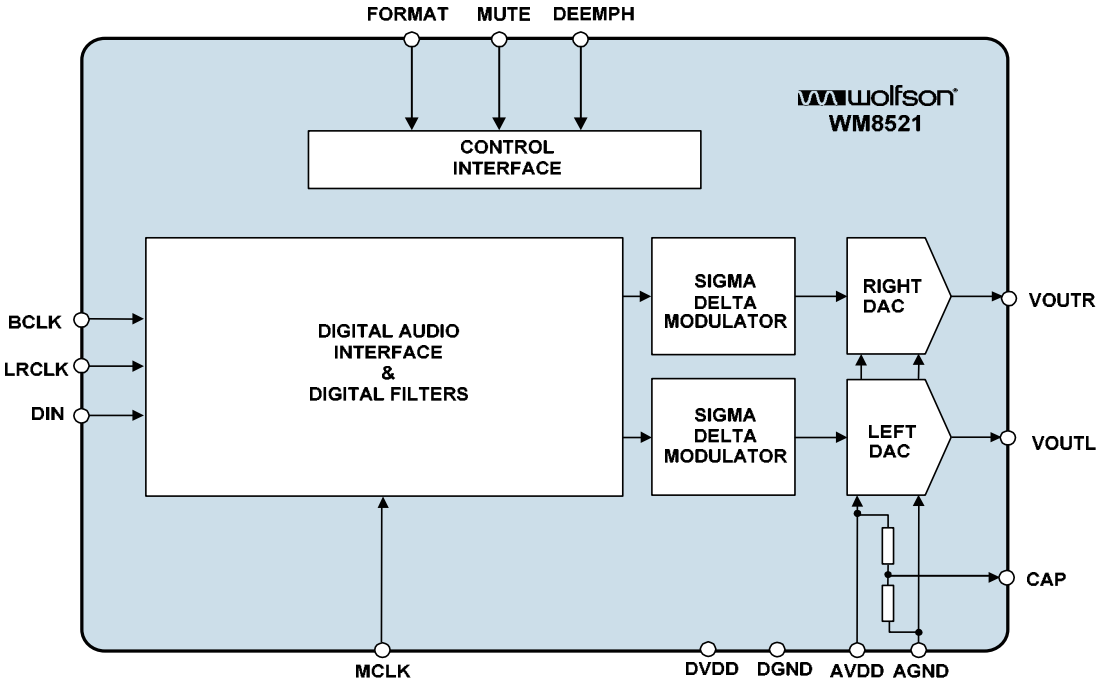
FEATURES

- Audio Performance
  - DAC SNR 98dB ('A' weighted @ 48kHz)
  - THD -81dB ('A' weighted @ 48kHz)
- DAC Sampling Frequency: 8kHz – 96kHz
- Pin Selectable Audio Data Interface Format
  - I^2S, 16-bit Right Justified or 16bit DSP
- 2.0 Vrms output at 12V or 9V supply
- 8.2V to 13.2V Analogue, 2.7V to 3.6 Digital Supply
- 14-pin SOIC Package

APPLICATIONS

- Consumer digital audio applications requiring 2 Vrms output
  - DVD Players
  - Digital TV
  - Digital Set Top Boxes
  - A/V Receivers

BLOCK DIAGRAM

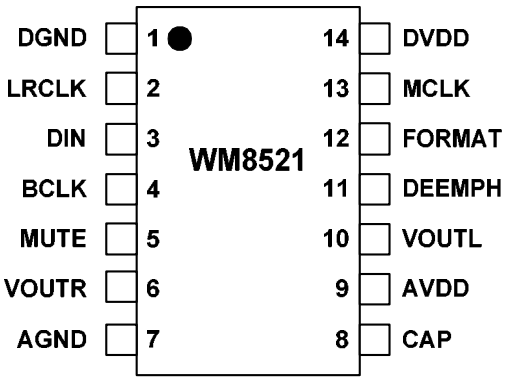


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PIN CONFIGURATION



ORDERING INFORMATION

DEVICE	TEMPERATURE RANGE	PACKAGE	MOISTURE SENSITIVITY LEVEL	PEAK SOLDERING TEMPERATURE
WM8521HCED/V	-25 to +85°C	14-pin SOIC	MSL1	240°C
WM8521HCED/RV	-25 to +85°C	14-pin SOIC (tape and reel)	MSL1	240°C
WM8521HCGED/V	-25 to +85°C	14-pin SOIC (lead free)	MSL1	260°C
WM8521HCGED/RV	-25 to +85°C	14-pin SOIC (lead free, tape and reel)	MSL1	260°C
WM8521H9ED/V	-25 to +85°C	14-pin SOIC	MSL1	240°C
WM8521H9ED/RV	-25 to +85°C	14-pin SOIC (tape and reel)	MSL1	240°C
WM8521H9GED/V	-25 to +85°C	14-pin SOIC (lead free)	MSL1	260°C
WM8521H9GED/RV	-25 to +85°C	14-pin SOIC (lead free, tape and reel)	MSL1	260°C

Note:

1. Reel quantity = 3,000
2. WM8521H9: 2Vrms output at 9V supply
3. WM8521HC: 2Vrms output at 12V supply

PIN DESCRIPTION

PIN	NAME	TYPE	DESCRIPTION
1	DGND	Supply	Digital Negative supply
2	LRCLK	Digital input	Sample rate clock input
3	DIN	Digital input	Serial audio data input
4	BCLK	Digital input	Bit clock input
5	MUTE	Digital input	Soft mute control, Internal pull down High Impedance = Automute High = Mute ON Low = Mute OFF
6	VOUTR	Analogue output	Right channel DAC output
7	AGND	Supply	Analogue Negative supply
8	CAP	Analogue output	Analogue internal reference
9	AVDD	Supply	Analogue Positive supply
10	VOUTL	Analogue output	Left channel DAC output
11	DEEMPH	Digital input	De-emphasis select, Internal pull down High = de-emphasis ON Low = de-emphasis OFF
12	FORMAT	Digital input	Data input format select, Internal pull up Low = 16-bit right justified or 16bit DSP 'late' High = 16-32-bit I^2S or 16bit DSP 'early'
13	MCLK	Digital input	Master clock input
14	DVDD	Supply	Digital Positive supply

Note:

1. Digital input pins have Schmitt trigger input buffers.

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified.



ESD Sensitive Device. This device is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device.

Wolfson tests its package types according to IPC/JEDEC J-STD-020B for Moisture Sensitivity to determine acceptable storage conditions prior to surface mount assembly. These levels are:

MSL1 = unlimited floor life at <30°C / 85% Relative Humidity. Not normally stored in moisture barrier bag.
MSL2 = out of bag storage for 1 year at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.
MSL3 = out of bag storage for 168 hours at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.

The Moisture Sensitivity Level for each package type is specified in Ordering Information.

CONDITION	MIN	MAX
Analogue Supply Voltage (AVDD)	-0.3V	+15V
Digital Supply voltage (DVDD)	-0.3V	+4.2V
Voltage range digital inputs	DGND -0.3V	DVDD +0.3V
Master Clock Frequency		50MHz
Operating temperature range, T_A	-25°C	+85°C
Storage temperature prior to soldering	30°C max / 85% RH max	
Storage temperature after soldering	-65°C	+150°C

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
WM8521HC Analogue supply range	AVDD		8.2	12	13.2	V
WM8521H9 Analogue supply range	AVDD		8.2	9	13.2	V
Digital supply range	DVDD		2.7	3.3	3.6	V
Ground	AGND / DGND			0		V
WM8521HC Supply current		AVDD = 12V DVDD = 3.3V		32.0		mA
WM8521H9 Supply current		AVDD = 9V DVDD = 3.3V		24.9		mA
WM8521HC Power down current (note 4)		AVDD = 12V DVDD = 3.3V		23.7		mA
WM8521H9 Power down current (note 4)		AVDD = 9V DVDD = 3.3V		17.9		mA

ELECTRICAL CHARACTERISTICS

Test Conditions

WM8521HC: AVDD = 12V, DVDD = 3.3V, AGND / DGND = 0V, T_A = +25°C, fs = 48kHz, MCLK = 256fs unless otherwise stated.

WM8521H9: AVDD = 9V, DVDD = 3.3V, AGND / DGND = 0V, T_A = +25°C, fs = 48kHz, MCLK = 256fs unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Digital Logic Levels (CMOS Levels)						
Input LOW level	V_{IL}				0.7 x DVDD	V
Input HIGH level	V_{IH}		0.3 x DVDD			V
Output LOW	V_{OL}	I_{OL} = 1mA			0.1 x DVDD	V
Output HIGH	V_{OH}	I_{OH} = -1mA	0.9 x DVDD			V
Analogue Reference Levels						
Reference voltage (CAP)				AVDD/2		V
Potential divider resistance	R_{CAP}	VDD to CAP and CAP to GND		50		kΩ
DAC Output (Load = 10kΩ. 50pF)						
WM8521HC 0dBFs Full scale output voltage		At DAC outputs		2.0		V_{rms}
WM8521H9 0dBFs Full scale output voltage		At DAC outputs		2.0	2.64 @ 12V AVDD	V_{rms}
SNR (Terminology Note 1,2,3)		A-weighted, @ fs = 48kHz	95	98		dB
SNR (Terminology Note 1,2,3)		A-weighted @ fs = 96kHz		98		dB
SNR (Terminology Note 1,2,3)		Non 'A' weighted @ fs = 48kHz		95		dB
THD (Note 3)		1kHz, 0dBFs		-81		dB
Dynamic Range (Note 2)		1kHz, THD+N @ -60dBFs	91	98		dB
DAC Channel Separation		1kHz, 0dBFs		93		dB

Test Conditions

WM8521HC: AVDD = 12V, DVDD = 3.3V, AGND / DGND = 0V, T_A = +25°C, fs = 48kHz, MCLK = 256fs unless otherwise stated.

WM8521H9: AVDD = 9V, DVDD = 3.3V, AGND / DGND = 0V, T_A = +25°C, fs = 48kHz, MCLK = 256fs unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Analogue Output Levels						
Gain Mismatch Channel-to-channel				±1		%FSR
Minimum Resistance Load		To midrail or a.c. coupled		5		kΩ
Maximum Capacitance Load				220		pF
Output d.c. Level				AVDD/2		V
Power On Reset (POR)						
POR Threshold		DVDD		1.64		V

Notes:

1. Ratio of output level with 1kHz full scale input, to the output level with all zeros into the digital input, measured 'A' weighted over a 20Hz to 20kHz bandwidth.
2. All performance measurements done with 20kHz low pass filter, and where noted an A-weight filter. Failure to use such a filter will result in higher THD+N and lower SNR and Dynamic Range readings than are found in the Electrical Characteristics. The low pass filter removes out of band noise; although it is not audible it may affect dynamic specification values.
3. CAP pin decoupled with 10uF and 0.1uF capacitors (smaller values may result in reduced performance).
4. Digital reset occurs 1.5µs after MCLK is stopped.

TERMINOLOGY

1. Signal-to-noise ratio (dB) - SNR is a measure of the difference in level between the full scale output and the output with no signal applied. (No Auto-zero or Automute function is employed in achieving these results).
2. Dynamic range (dB) - DNR is a measure of the difference between the highest and lowest portions of a signal. Normally a THD+N measurement at 60dB below full scale. The measured signal is then corrected by adding the 60dB to it. (e.g. THD+N @ -60dB= -32dB, DR= 92dB).
3. THD+N (dB) - THD+N is a ratio, of the rms values, of (Noise + Distortion)/Signal.
4. Stop band attenuation (dB) - Is the degree to which the frequency spectrum is attenuated (outside audio band).
5. Channel Separation (dB) - Also known as Cross-Talk. This is a measure of the amount one channel is isolated from the other. Normally measured by sending a full scale signal down one channel and measuring the other.

MASTER CLOCK TIMING

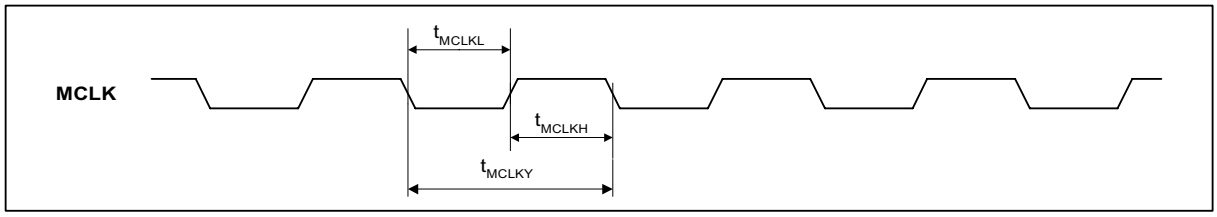


Figure 1 Master Clock Timing Requirements

Test Conditions

AVDD = 12V, DVDD = 3.3V, AGND / DGND = 0V, T_A = +25°C, fs = 48kHz, MCLK = 256fs unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
System Clock Timing Information						
MCLK Master clock pulse width high	t_{MCLKH}		11			ns
MCLK Master clock pulse width low	t_{MCLKL}		11			ns
MCLK Master clock cycle time	t_{MCLKY}		28			ns
MCLK Duty cycle			40:60		60:40	
Time from MCLK stopping to digital reset			1.5		12	µs

DIGITAL AUDIO INTERFACE

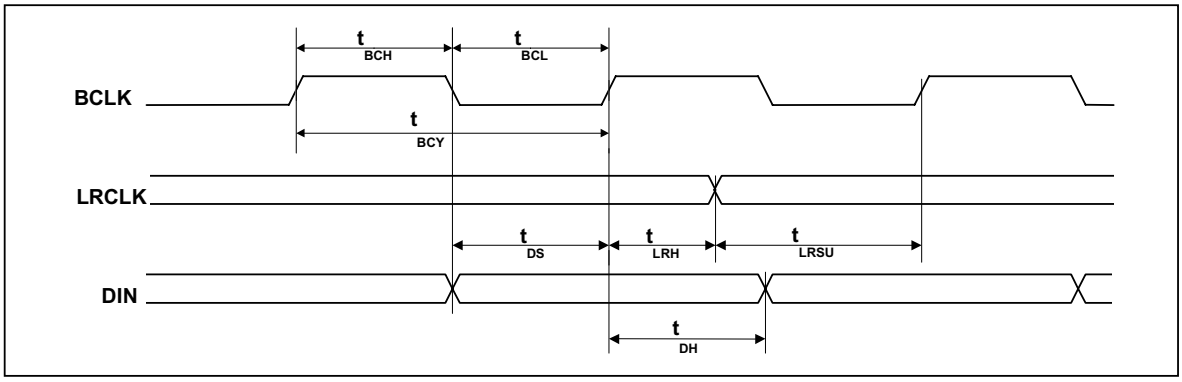


Figure 2 Digital Audio Data Timing

Test Conditions

AVDD = 12V, DVDD = 3.3V, AGND / DGND = 0V, T_A = +25°C, fs = 48kHz, MCLK = 256fs unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Audio Data Input Timing Information						
BCLK cycle time	t_{BCY}		50			ns
BCLK pulse width high	t_{BCH}		20			ns
BCLK pulse width low	t_{BCL}		20			ns
LRCLK set-up time to BCLK rising edge	t_{LRSU}		10			ns
LRCLK hold time from BCLK rising edge	t_{LRH}		10			ns
DIN set-up time to BCLK rising edge	t_{DS}		10			ns
DIN hold time from BCLK rising edge	t_{DH}		10			ns

DEVICE DESCRIPTION

GENERAL INTRODUCTION

The WM8521 is a high performance DAC designed for digital consumer audio applications requiring a 2Vrms output. The range of features make it ideally suited for use in DVD players, Digital TV, Digital Set Top Boxes, AV receivers and other consumer audio equipment.

The WM8521 is a complete 2-channel stereo audio digital-to-analogue converter, including digital interpolation filter, multi-bit sigma delta with dither, switched capacitor multi-bit stereo DAC and output smoothing filters combined with 2Vrms outputs. It is fully compatible and an ideal partner for a range of industry standard microprocessors, controllers and DSPs. A novel multi bit sigma-delta DAC design is used, utilising a 128x oversampling rate, to optimise signal to noise performance and offer increased clock jitter tolerance.

Control of internal functionality of the device is provided by hardware control (pin programmed).

Operation using master clocks of 256fs, 384fs, 512fs or 768fs is provided, selection between clock rates being automatically controlled. Sample rates (fs) from 8kHz to 96kHz are allowed provided the appropriate system clock is input.

The audio data interface supports 16-bit right justified or 16-, 20-, 24-, 32-bit I^2S (Philips left justified, one bit delayed) interface formats. A 16bit DSP interface is also supported, enhancing the interface options for the user.

The device is packaged in a small 14-pin SOIC.

DAC CIRCUIT DESCRIPTION

The WM8521 DAC is designed to allow playback of 24-bit PCM audio or similar data with high resolution and low noise and distortion. Sample rates from 8kHz to 96kHz may be used provided that the ratio of sample rate (LRCLK) to master clock (MCLK) is maintained at one of the required rates.

The two DACs on the WM8521 are implemented using sigma-delta oversampled conversion techniques. These require that the PCM samples are digitally filtered and interpolated to generate a set of samples at a much higher rate than the input rate. This sample stream is then digitally modulated to generate a digital pulse stream that is then converted to analogue signals in a switched capacitor DAC. The advantage of this technique is that the DAC is linearised using noise shaping techniques, allowing the 24-bit resolution to be met using non-critical analogue components. A further advantage is that the high sample rate at the DAC output means that smoothing filters on the output of the DAC need only have fairly crude characteristics in order to remove the characteristic steps, or images on the output of the DAC. To ensure that generation of tones characteristic to sigma-delta convertors is not a problem, dithering is used in the digital modulator along with a higher order modulator. The multi-bit switched capacitor technique used in the DAC reduces sensitivity to clock jitter, and dramatically reduces out of band noise compared to switched current or single bit techniques used in other implementations.

The voltage on the CAP pin is used as the reference for the DACs. Therefore the amplitude of the signals at the DAC outputs will scale with the amplitude of the voltage at the CAP pin. An external reference could be used to drive into the CAP pin if desired, with a value typically of about midrail ideal for optimum performance. However driven in normal operation, an internal divider will set a valve of AVDD/2 on the cap pin.

Typically an external low pass filter circuit will be used to remove residual out of band noise characteristic of delta sigma converters. However, the advanced multi-bit DAC used in WM8521 produces far less out of band noise than single bit traditional sigma delta DACs, and so in many applications this filter may be removed, or replaced with a simple RC pole.

CLOCKING SCHEMES

In a typical digital audio system there is only one central clock source producing a reference clock to which all audio data processing is synchronised. This clock is often referred to as the audio system's Master Clock. The external master clock can be applied directly through the MCLK input pin with no configuration necessary for sample rate selection.

Note that on the WM8521, MCLK is used to derive clocks for the DAC path. The DAC path is affected by DAC sampling clock, DAC digital filter clock and DAC digital audio interface timing. In a system where there are a number of possible sources for the reference clock it is recommended that the clock source with the lowest jitter be used to optimise the performance of the DAC.

The device can be reset by stopping MCLK. In this state the power consumption is substantially reduced.

DIGITAL AUDIO INTERFACE

Audio data is applied to the internal DAC filters via the Digital Audio Interface. Three interface formats are supported:

- I^2S mode
- Right Justified mode
- DSP mode

All formats send the MSB first. The data format is selected with the FORMAT pin. When FORMAT is LOW, right justified data format is selected and word lengths up to 16-bits may be used. If a word length shorter than 16-bits is used, the unused bits should be padded with zeroes. When the FORMAT pin is HIGH, I^2S format is selected and word length of any value up to 32-bits may be used. Unless in 16-bit 'packed' mode, if a word length shorter than 24-bits is used, the unused bits should be padded with zeros. If LRCLK is 4 BCLKs or less duration, the 16bit DSP compatible format is selected. Early and Late clock formats are supported, selected by the state of the FORMAT pin.

I^2S MODE INPUT FORMAT

The WM8521 supports word lengths of 16-32 bits in I^2S mode.

In I^2S mode, the digital audio interface receives data on the DIN input. Audio Data is time multiplexed with LRCLK indicating whether the left or right channel is present. LRCLK is also used as a timing reference to indicate the beginning or end of the data words.

25-32 bits: LRCLK must be high for a minimum of data wordlength BCLKs and low for a minimum of data wordlength BCLKs. The LSBs will be truncated and the most significant 24 bits will be used by the internal processing.

24 bits: LRCLK must be high for a minimum of 24 BCLKs and low for a minimum of 24 BCLKs.

17-23 bits: Data must be zero padded to 24 bits and LRCLK must be high for a minimum of 24 BCLKs and low for a minimum of 24 BCLKs.

Up to 16 bits: EITHER data must be zero padded to 24 bits and LRCLK must be high for minimum 24 BCLKs and low for 24 BCLKs,

OR data must be zero padded to 16 bits and LRCLK must be high for exactly 16 BCLKs and low for exactly 16 BCLKs. The device auto-detects this '16-bit packed' mode and switches to 16-bit data length.

Any mark to space ratio on LRCLK is acceptable provided the above requirements are met.

In I²S mode, the MSB is sampled on the second rising edge of BCLK following a LRCLK transition. LRCLK is low during the left samples and high during the right samples.

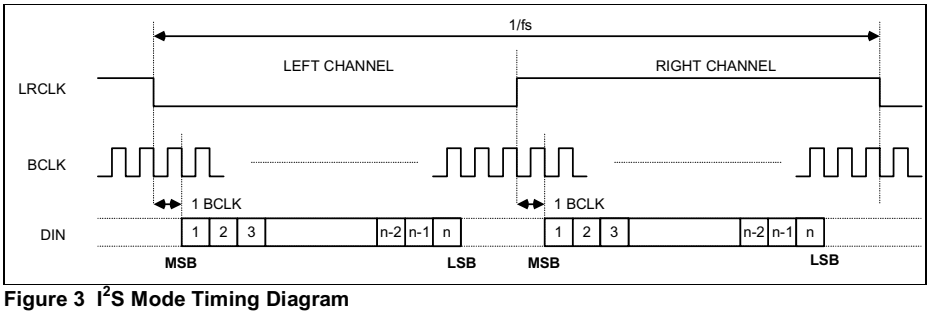


Figure 3 I²S Mode Timing Diagram

RIGHT JUSTIFIED MODE INPUT FORMAT

The WM8521 supports word lengths of up to 16-bits in right justified mode. If a word length shorter than 16-bits is used, the unused bits should be padded with zeroes.

In right justified mode, LRCLK must be high for a minimum of 16 BCLKs and low for a minimum of 16 BCLKs. Any mark to space ratio on LRCLK is acceptable provided the above requirement is met.

The digital audio interface receives data on the DIN input. Audio Data is time multiplexed with LRCLK indicating whether the left or right channel is present. LRCLK is also used as a timing reference to indicate the beginning or end of the data words.

In right justified mode, the LSB is sampled on the rising edge of BCLK preceding a LRCLK transition. LRCLK is high during the left samples and low during the right samples.

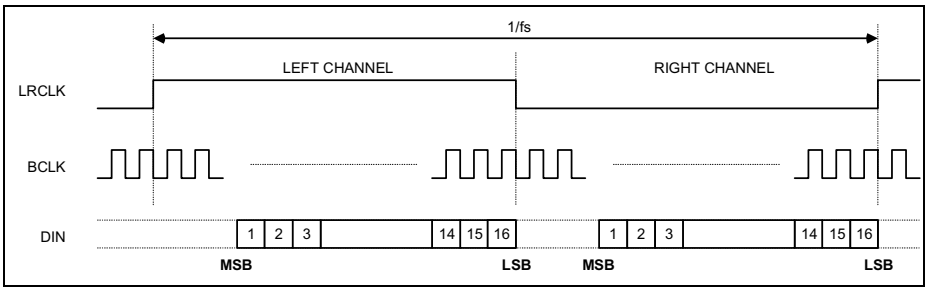


Figure 4 Right Justified Mode Timing Diagram

DSP MODE INPUT FORMAT

A DSP compatible, time division multiplexed format is also supported by the WM8521.

This format is of the type where a 'synch' pulse is followed by two data words (left and right) of 16 bit word length. The 'synch' pulse replaces the normal duration LRCLK, and DSP mode is auto-detected by the shorter than normal duration of the LRCLK. If LRCLK is of 4 BCLK or less duration, the DSP compatible format is selected. Early and Late clock formats are supported, selected by the state of the FORMAT pin.

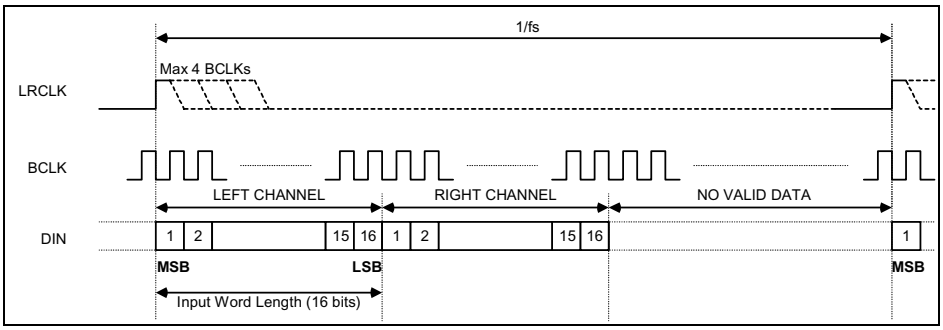


Figure 5 DSP 'Late' Mode Timing

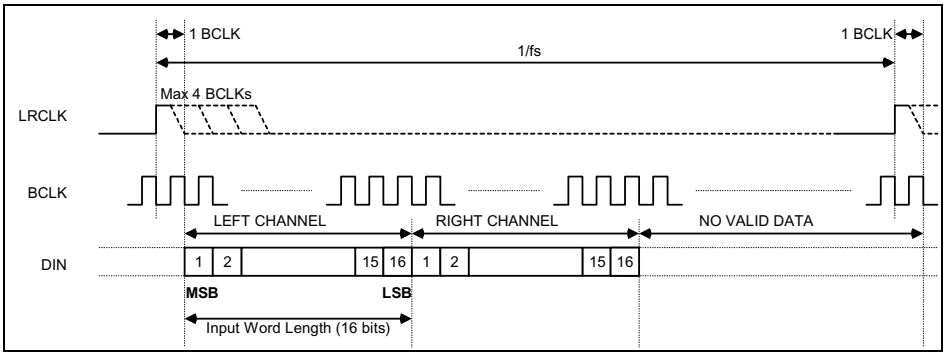


Figure 6 DSP 'Early' Mode Timing

AUDIO DATA SAMPLING RATES

The master clock for WM8521 supports audio sampling rates from 256fs to 768fs, where fs is the audio sampling frequency (LRCLK) typically 32kHz, 44.1kHz, 48kHz or 96kHz. The master clock is used to operate the digital filters and the noise shaping circuits.

The WM8521 has a master clock detection circuit that automatically determines the relationship between the master clock frequency and the sampling rate (to within +/- 32 master clocks). If there is a greater than 32 clocks error, the master clock defaults to 768fs. The master clock should be synchronised with LRCLK, although the WM8521 is tolerant of phase differences or jitter on this clock.

SAMPLING RATE (LRCLK)	MASTER CLOCK FREQUENCY (MHz) (MCLK)			
	256fs	384fs	512fs	768fs
32kHz	8.192	12.288	16.384	24.576
44.1kHz	11.2896	16.9344	22.5792	33.8688
48kHz	12.288	18.432	24.576	36.864
96kHz	24.576	36.864	Unavailable	Unavailable

Table 1 Master Clock Frequencies Versus Sampling Rate

Note:

For sample rates down to 8k, scale MCLK accordingly.

HARDWARE CONTROL MODES

The WM8521 is hardware programmable providing the user with options to select input audio data format, de-emphasis and mute.

MUTE AND AUTO MUTE OPERATION

Pin 5 (MUTE) controls the mute function, or can be used as an output to monitor the state of the automuted signal.

MUTE PIN	DESCRIPTION
0	Normal Operation, MUTE off
1	Mute DAC channels
Floating	Enable IZD, MUTE becomes an output to indicate when IZD occurs.

Table 2 Mute and Automute Control

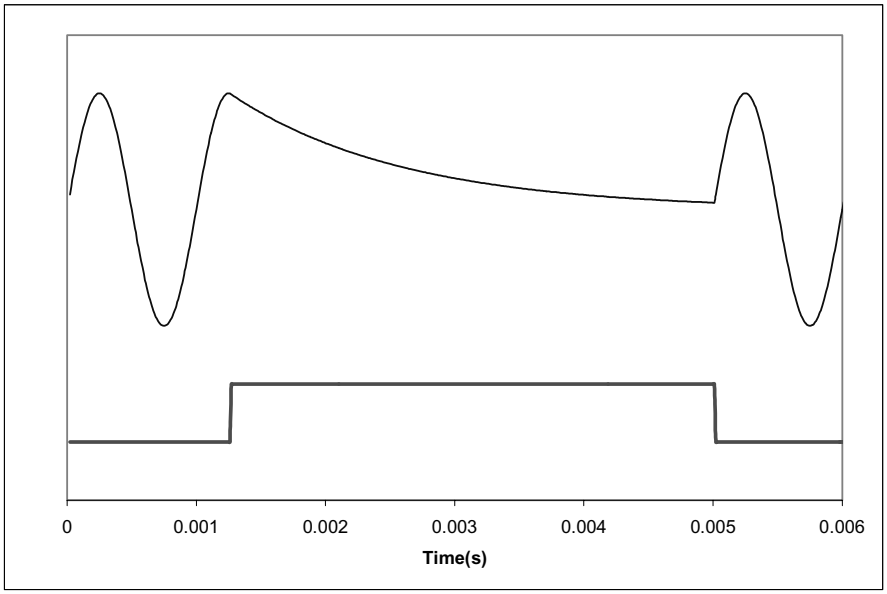


Figure 7 Application and Release of MUTE

MUTE is active high; taking the pin high causes the filters to soft mute, ramping down the audio signal over a few milliseconds. Taking MUTE low again allows data into the filter. Refer to Figure 7.

Therefore if MUTE is tied low then mute is disabled and the automute function is overridden.

If MUTE is floating or connected to a high impedance then the automute function will operate. The AUTOMUTED internal signal, which is generated by the IZD function, is connected to the MUTE pin internally via a 10k resistor. This can provide a weak output (10k source impedance) which can be used to drive external mute circuits. Refer to Figure 8.

The Infinite Zero Detect (IZD) function detects 1024 zero value audio samples applied to both channels. After such an event, a latch is set whose output is the AUTOMUTED internal signal. AUTOMUTED will be reset as soon as either channel receives a non-zero input.

A diagram showing how the various Mute modes interact is shown below in Figure 8.

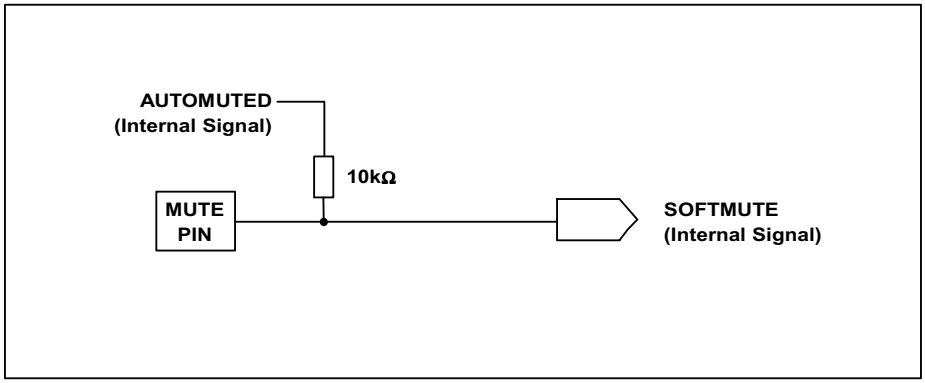


Figure 8 Selection Logic for MUTE Modes

INPUT AUDIO FORMAT SELECTION

FORMAT (pin 12) controls the data input format.

FORMAT	INPUT DATA MODE
0	16 bit right justified
1	16–32 bit I^2S

Table 3 Input Audio Format Selection

INPUT DSP FORMAT SELECTION

FORMAT	LRCLK DATAWIDTH BCLKS	LRCLK OF 4 BCLK OR LESS DURATION
0	16 bit (MSB-first, right justified)	16 bit DSP format – 'late' mode
1	I^2S format up to 24 bit (Philips serial data protocol)	16 bit DSP format – 'early' mode

Table 4 DSP Interface Formats

DE-EMPHASIS CONTROL

DEEMPH (pin 11) is an input control for selection of de-emphasis filtering to be applied.

DEEMPH	DE-EMPHASIS
0	Off
1	On

Table 5 De-emphasis Control

DIGITAL FILTER CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Passband Edge		-3dB		0.487fs		
Passband Ripple		f < 0.444fs			±0.05	dB
Stopband Attenuation		f > 0.555fs	-60			dB

Table 6 Digital Filter Characteristics

DAC FILTER RESPONSES

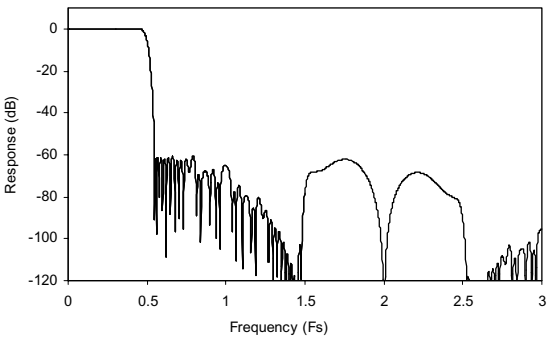


Figure 9 DAC Digital Filter Frequency Response –44.1,48 and 96kHz

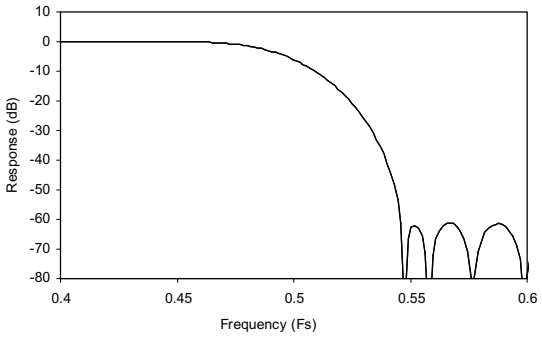


Figure 10 DAC Digital Filter Transition Band –44.1,48 and 96kHz

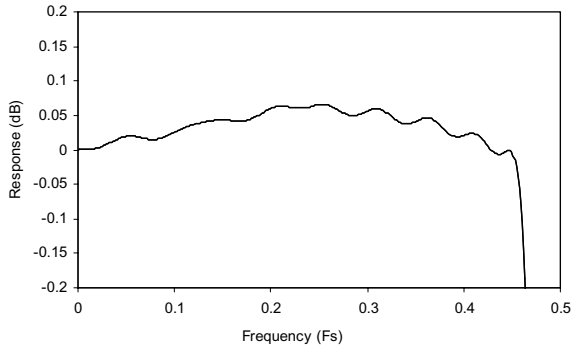


Figure 11 DAC Digital Filter Ripple – 44.1, 48 and 96kHz

DIGITAL DE-EMPHASIS CHARACTERISTICS

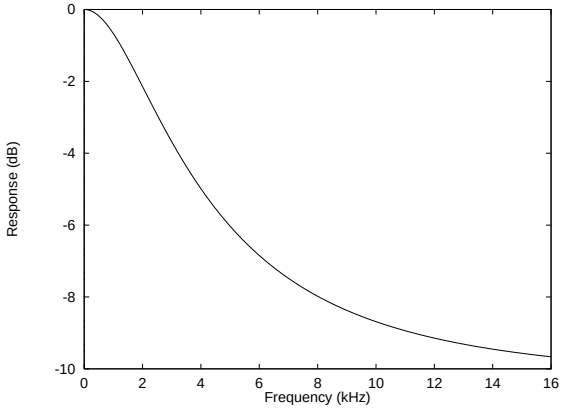


Figure 12 De-Emphasis Frequency Response (32kHz)

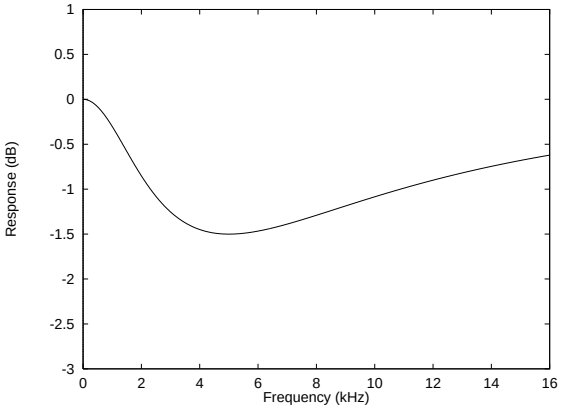


Figure 13 De-Emphasis Error (32KHz)

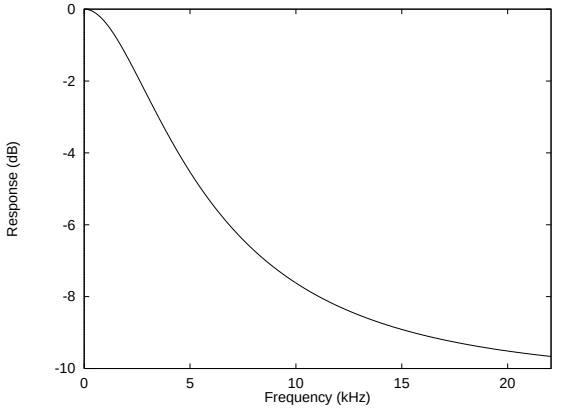


Figure 14 De-Emphasis Frequency Response (44.1KHz)

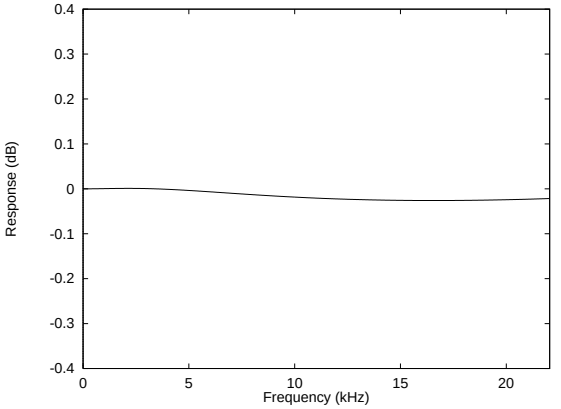


Figure 15 De-Emphasis Error (44.1KHz)

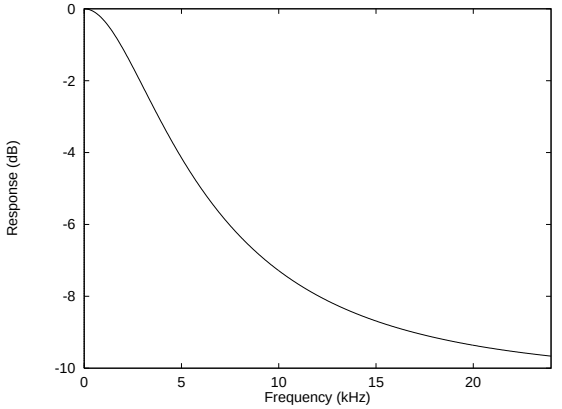


Figure 16 De-Emphasis Frequency Response (48kHz)

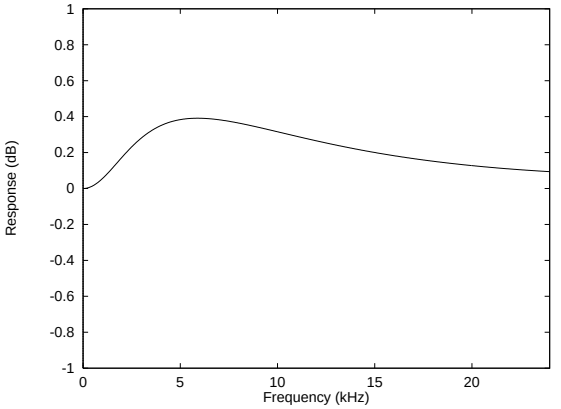
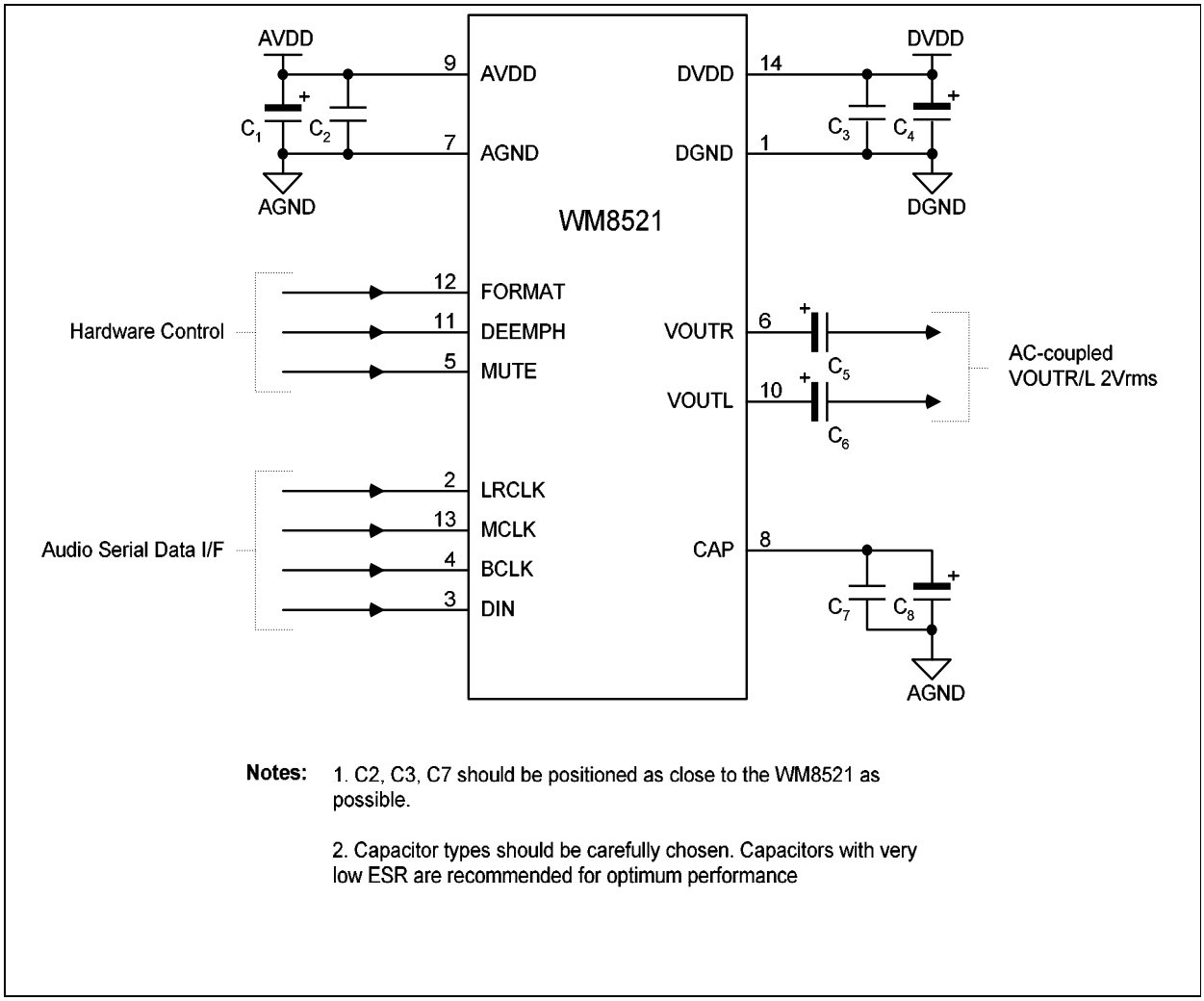


Figure 17 De-Emphasis Error (48kHz)

APPLICATIONS INFORMATION

RECOMMENDED EXTERNAL COMPONENTS



Notes: 1. C2, C3, C7 should be positioned as close to the WM8521 as possible.

2. Capacitor types should be carefully chosen. Capacitors with very low ESR are recommended for optimum performance

Figure 18 Recommended External Components

RECOMMENDED EXTERNAL COMPONENTS VALUES

COMPONENT REFERENCE	SUGGESTED VALUE	DESCRIPTION
C1	10µF	De-coupling for AVDD
C2	0.1µF	De-coupling for AVDD
C3	10µF	De-coupling for DVDD
C4	0.1µF	De-coupling for DVDD
C5 and C6	10µF	Output AC coupling caps to remove midrail DC level from outputs
C7	0.1µF	Reference de-coupling capacitors for CAP pin
C8	10µF	

Table 7 External Components Description

RECOMMENDED ANALOGUE LOW PASS FILTER

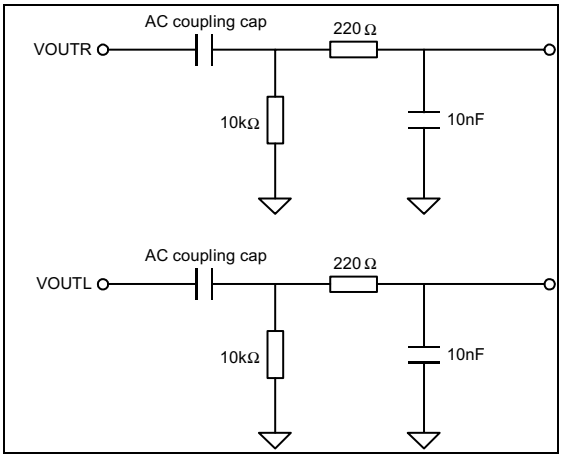


Figure 19 Recommended 1st Order Low Pass Filter

An external single pole RC filter is recommended (see Figure 19) if the device is driving a wideband amplifier. However the WM8521 does contain an internal low pass filter which should be adequate in most applications.

PCB LAYOUT RECOMMENDATIONS

Care should be taken in the layout of the PCB that the WM8521 is to be mounted to. The following notes will help in this respect:

The VDD supply to the device should be as noise free as possible. This can be accomplished to a large degree with a 10uF bulk capacitor placed locally to the device and a 0.1uF high frequency decoupling capacitor placed as close to the VDD pin as possible. It is best to place the 0.1uF capacitor directly between the VDD and GND pins of the device on the same layer to minimize track inductance and thus improve device decoupling effectiveness.

The CAP pin should be as noise free as possible. This pin provides the decoupling for the on chip reference circuits and thus any noise present on this pin will be directly coupled to the device outputs. In a similar manner to the VDD decoupling described in 1. above, this pin should be decoupled with a 10uF bulk capacitor local to the device and a 0.1uF capacitor as close to the CAP pin as possible.

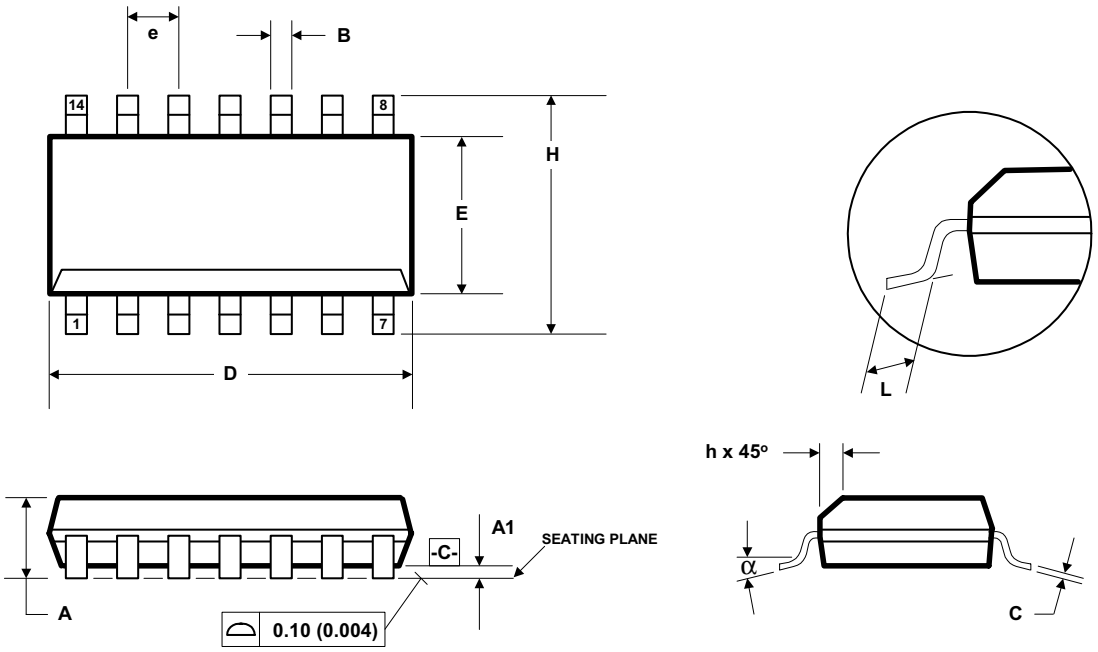
Separate analogue and digital track routing from each other. The device is split into analogue (pins 5 – 10) and digital (pins 1 – 4 & pins 11 – 14) sections that allow the routing of these signals to be easily separated. By physically separating analogue and digital signals, crosstalk from the PCB can be minimized.

Use an unbroken solid GND plane. To achieve best performance from the device, it is advisable to have either a GND plane layer on a multilayer PCB or to dedicate one side of a 2 layer PCB to be a GND plane. For double sided implementations it is best to route as many signals as possible on the device mounted side of the board, with the opposite side acting as a GND plane. The use of a GND plane greatly reduces any electrical emissions from the PCB and minimizes crosstalk between signals.

An evaluation board is available for the WM8521 that demonstrates the above techniques and the excellent performance achievable from the device. This can be ordered or the User manual downloaded from the Wolfson web site at www.wolfsonmicro.com

PACKAGE DRAWING

D: 14 PIN SOIC 3.9mm Wide Body **DM001.C**



Symbols	Dimensions (MM)		Dimensions (Inches)	
	MIN	MAX	MIN	MAX
A	1.35	1.75	0.0532	0.0688
A1	0.10	0.25	0.0040	0.0098
B	0.33	0.51	0.0130	0.0200
C	0.19	0.25	0.0075	0.0098
D	8.55	8.75	0.3367	0.3444
E	3.80	4.00	0.1497	0.1574
e	1.27 BSC		0.05 BSC	
H	5.80	6.20	0.2284	0.2440
h	0.25	0.50	0.0099	0.0196
L	0.40	1.27	0.0160	0.0500
α	0°	8°	0°	8°
REF:	JEDEC.95, MS-012			

NOTES:
A. ALL LINEAR DIMENSIONS ARE IN MILLIMETERS (INCHES).
B. THIS DRAWING IS SUBJECT TO CHANGE WITHOUT NOTICE.
C. BODY DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSION, NOT TO EXCEED 0.25MM (0.010IN).
D. MEETS JEDEC.95 MS-012, VARIATION = AB. REFER TO THIS SPECIFICATION FOR FURTHER DETAILS.

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