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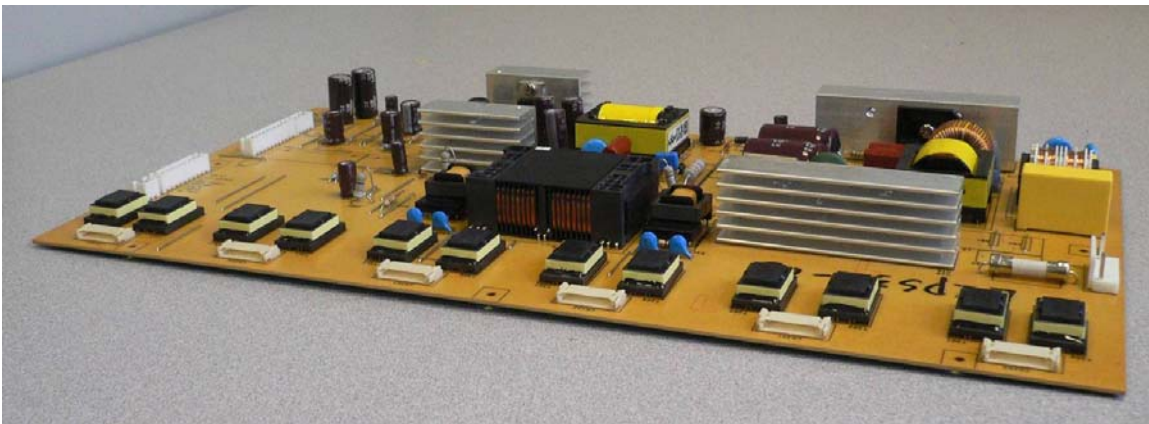
GreenPoint™
From ON Semiconductor

Up to 180 W High Voltage LCD TV Power and Integrated Inverter Supply

12 February 2009

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Overview

This reference document describes a built-and-tested, GreenPoint™ solution for and ⅬCD-TV Ⅰntegrated Ⲣower Ⴝupply (LIPS) that combines the main system power with the backlight inverter. In this architecture the inverter is directly powered from a Ⱨigh ⱴoltage rail (HV-LIPS) to improve the system power conversion efficiency and simplify the overall architecture by eliminating a power conversion stage. In this reference design, the inverter is configured to power 12 cold cathode fluorescent lamps (CCFL). All the circuitry is resident in on a single PCB as might be found in a 32" LCD-TV.   This reference design circuit consists of a single-sided 175 mm x 330 mm printed circuit board designed to fit into the chassis of a LCD-TV. The height is 25 mm.

Figure 1 illustrates the basic system architecture. As shown, ON Semiconductor devices are combined with a next generation backlight controller from Microsemi to provide a complete power solution. This design has been engineered to achieve optimum performance compared to traditional LCD-TV power architectures and at the same time simplify the overall bill of materials by selecting a proprietary high efficiency fly-back controller topology that eliminated the need for a dedicated standby power stage and still meets global standby power requirements for television sets.
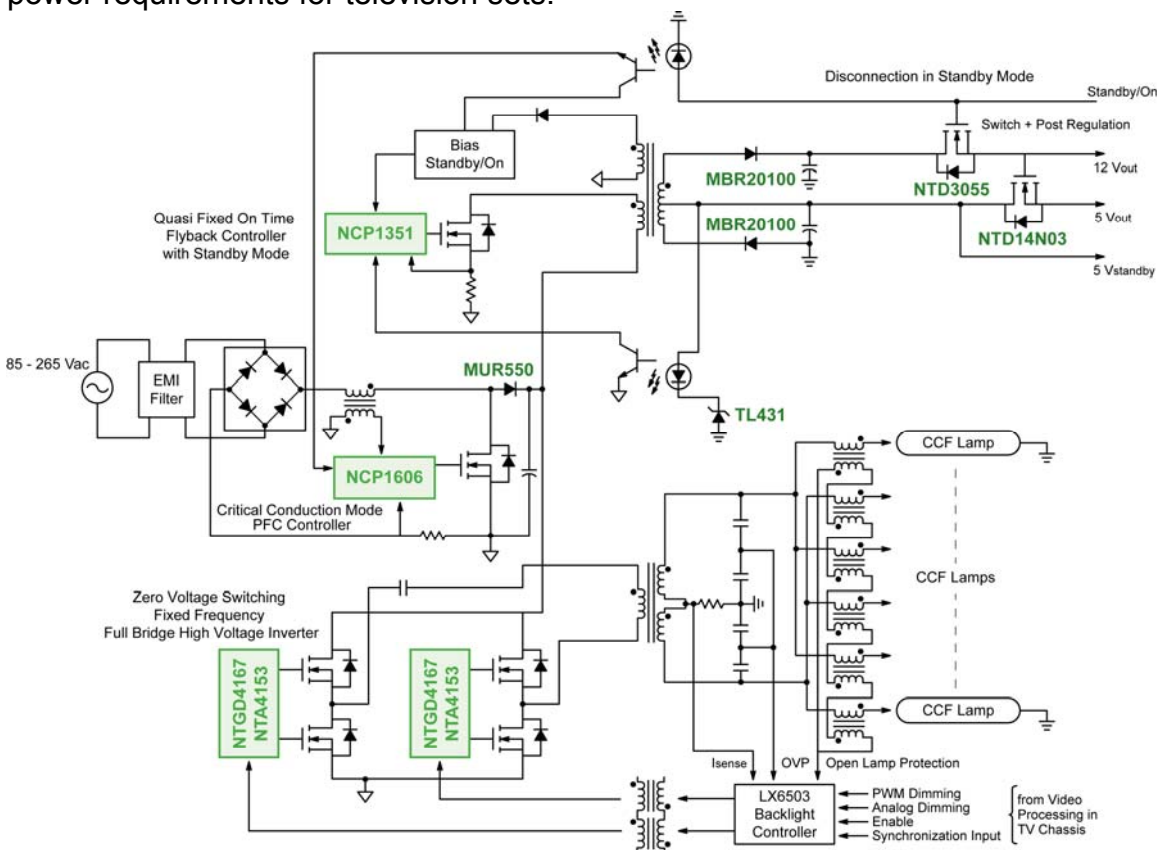

Figure 1: Overall System Block Diagram

LCD-TV Power Architecture and Evolution

One of the key differentiating factors of a flat TV over a classical TV is the thickness of the cabinet - the thinner the better. This involves several considerations:

- The amount of power to be delivered is relatively large: the number of watts per cm^3 is much larger compared to the one in a CRT TV.
- Because the TV will be used in the living room, audible noise can be a problem, and the use of fans is limited.
- Overall cost in the very competitive environment of the consumer electronics world is critical
- The panel, the power supply and the audio amplifiers are close to each other; therefore the generation of EMI and susceptibility to EMC could have an impact on picture and sound quality.

Mainstream (32"+) Flat TVs power supplies require the generation of several voltage rails to power the various system blocks such as audio, backlighting, and signal processing. The power supply does not generate all the voltages required within the set, instead local linear and DC-DC converters on the signal processing board are used to provide various low voltage rails. It is fairly common for manufacturers to use a universal power supply that supports 90-265 Vac. This allows a single power supply design based on a specific TV size to be used for a series of models for different regions simplifying logistics and reducing development cost. If the LCD-TV is intended for global use and the power is over 75 W, it is necessary to comply with IEC 61000-3-2, the EU standard for harmonic reduction, so an active power factor control stage is used.

The largest single power consuming sub-system within the LCD-TV is the backlight. The majority of LCD-TVs today use an array of CCFL lamps as the backlight light source. These lamps are intended to be driven by a high AC voltage and the current within the lamps is regulated to achieve even backlighting. Historically the inverter was a separate module powered from a nominal 24 V dc supply. An example of the classical 24 V dc architecture can be found in earlier LCD-TV reference designs such as TND316/D. While this approach simplified the design of the LCD-TV because the backlighting requirements are tied to the LCD panel and one power supply design could be used for panels from multiple vendors, the approach was inefficient and added an extra power stage. For example, the AC input is boosted to 400 V dc in the PFC stage and then transformed to 24 V dc with a flyback of resonant LLC half bridge stage. The 24 V dc was then provided to the inverter module which converted the low voltage DC voltage into a high voltage (> 1000 V ac) to drive the lamps. This multi-stage conversion process results in significant losses and increased system cost.

The HV-LIPS architecture employed in this reference design is intended to improve the overall system efficiency by eliminating the 400 to 24 V dc conversion stage and directly power the inverter from the high voltage PFC rail. This requires the merging of the traditional power supply function within the LCD-TV with the inverter in a seamless manner to optimize the overall system solution. This has three primary benefits:

- Increases overall system efficiency
- Reduces active power consumption and heat generation which enhances system reliability and reduces component stress
- Reduces the overall number of parts to improve the overall bill of materials cost

The other drivers for this architecture are increased consumer awareness on the cost of energy and new regulatory considerations that are intended to address overall power consumption of TVs and their impact on environment and the energy infrastructure.

Historically, standby losses in consumer electronics were the primary concern of governmental and power conservation agencies since these devices are always connected to the AC main and always consuming some power, even in off mode. As a result, there are numerous voluntary and regulatory standards around the globe intended to reduce standby power. Some of the typical requirements are listed below.

Region / Country	Program name	Requirements for Televisions
China	CECP	3 W
Korea	Energy Saving	3 W
European Union	EU Eco-Label	1 W or 9 W with an embedded set top box (STB)
European Union	EU Code of Conduct	3 W with a STB
Europe	GEEA	1 W
US	Energy Star®	1 W

Table 1: Example Standby Requirements by Region

As the screen size of direct view flat TVs increases, so does the ON mode power consumption. As a result, regulatory agencies have become concerned about the cumulative impact on the power grid of ON state power as flat TVs gain market share and consumers switch from CRT and projection TVs to large display direct view technologies such as Plasma and LCD-TV.   In the US, the

Environmental Protection Agency (EPA) started a process in 2006 to revise the existing voluntary Energy Star standard for TVs to include active power consumption requirements as part of its criteria for qualifying energy efficiency TVs. This standard was revised and went into effect in November 2008 and now incorporates maximum active power requirements as a function of screen size. As part of the specification development process, existing TVs were evaluated to the proposed standards and at the time, less than 30% of the TVs tested on the market meet the active and standby test requirements. The active power limits in the Version 3 Energy Star standard are listed in the table below. As illustrated, there are a series of equations based on screen area and vertical resolution to determine the active power limit. For example, a 42" High Definition TV can consume no more than 208 W out of the box when tested against an internationally approved audio/video test signal set which are meant to represent a common viewing environment.

Screen Area	Maximum On Mode Power Consumption (A expressed in in^2)	Maximum On Mode Power Consumption (A expressed in cm^2)
Non-High Definition TVs (i.e. <= 480 Native Vertical Resolution)		
All Screen Areas	$P_{Max} = 0.120 * A + 25$	$P_{Max} = 0.01860 * A + 25$
High Definition and Full High Definition TVs (i.e. > 480 Native Vertical Resolution)		
A < 680 $inch^2$ (< 4,387 cm^2)	$P_{Max} = 0.200 * A + 32$	$P_{Max} = 0.03100 * A + 32$
680 $inch^2$ <= A < 1045 $inch^2$ (4,387 cm^2 <= A < 6,742 cm^2)	$P_{Max} = 0.240 * A + 27$	$P_{Max} = 0.03720 * A + 27$
A >= 1045 $inch^2$ (>= 6,742 cm^2)	$P_{Max} = 0.156 * A + 151$	$P_{Max} = 0.02418 * A + 151$

Table 2: Version 3 Energy Star Active Power Limits

Other countries have or are considering changes to their energy regulations to drive the adoption of more power efficient TV products. For example, the Japan Top Runner program takes a holistic approach which considers total energy consumption (kWh/year) on an annual basis assuming 4.5 hours of active use per day. This focuses the attention of TV manufacturers on methods to optimize their system architectures for both active and standby power consumption. Further details of the regional approaches to energy requirements for TVs can be

accessed by referring to appendix. Finally TV manufacturers are starting to market the green aspects of their products to highlight and differentiate their offerings and appeal to consumers who are concerned about the rising cost of energy. While improvements in active power go beyond the power supply, and include the display, backlight source, video and audio signal processing, and control architectures, the HV-LIPS architecture in this reference design is designed from the ground up to save power over the traditional architecture. Moreover it is designed to reduce the total system cost at the complete bill of materials level.

Critical Design Objectives

Input Voltage: Universal input 85-265 V ac, 47-63 Hz

System Supply
- Active Power Factor Corrected, IEC61000-3-2 Compliant
- Maximum steady state power 50 W, 60 W Peak
- 12 V / 4 A Peak
- 5 V / 2.5 A Peak
- 24 V - MOSFET gate drive bias
- Flexibility to be modified to support other voltage/current configurations
- Standby Pin< 400 mW with 50 mW load (5 V at 10 mA)

Inverter Supply
- 100 W Capable
- Strike voltage > 1500 V ac, Operating Voltage >800 V ac
- Fixed frequency inverter adjustable between 40-80 kHz
- Digital and Analog dimming capable
- Capable of synchronization to video clock source

PFC Stage

The heart of the High Voltage LIPS architecture is the active PFC front-end boost stage. First, it allows the design to meet the harmonic content requirements of IEC61000-3-2 which applies to power supplies with input power above 75 W. Secondly, it provides a regulated 400 V dc high voltage rail for the inverter section. The inverter utilizes the Microsemi LX6503 backlight control IC which is configured in a fixed frequency resonant full bridge topology. The backlight controller manages the power conversion process and provides all the necessary control functions to regulate the current to an array of CCFL lamps including the strike and dimming functions necessary for the LCD-TV.

Beyond powering the backlight, the PFC also provides power to an isolated flyback switch mode power converter which generates all the necessary voltage rails to power the digital and analog circuitry that perform the control, interface, signal processing, and audio amplification functions within the LCD-TV. The

power required for this block can vary from 30 – 60 W depending on the set of features and functions that the LCD-TV performances. To simplify and reduce the overall complexity of the power conversion stage, a proprietary high efficiency flyback controller (NCP1351) has been selected which eliminates the need for a dedicated power standby power supply for most LCD-TV applications. The NCP1351 was selected because it utilizes a quasi fixed ON time control scheme which reduces the switching frequency of the flyback converter as the load requirements are reduced. The two additional switches (placed on the secondary) disconnect the main power loads to eliminate parasitic losses in standby mode.

In summary, the architecture combines a front end power factor correction stage with an optimized flyback stage which eliminates the need for a dedicated standby power supply and a highly efficient, full featured inverter with current balancing to drive the CCFL lamps which backlight the LCD-TV panel. All these functions are integrated on a single PCB which includes the JIN-current balancers to provide a complete power solution.

EMI filter

The input stage consists of a common mode filter (L5) combined with a differential filter composed of L1 (150 µH) and filter capacitors C1 and C3 (2 x 470 nF) which have been added to filter the low frequency EMI due to the discontinuous mode PFC. Varistor RV1 is used to suppress high energy pulses and mains surges which may disturb overall operation. Resistors (R15-R20) have been added to discharge C18 in a reasonable time when the mains power is disconnected. This has a minor impact on standby consumption by increasing the power by 59 mW at 230 V ac. A mains voltage is provided to the flyback controller to allow it to start up directly from the line and avoid increased power dissipation during standby.

Figure 2: AC Input Stage

Control Approach

The NCP1606B is a PFC controller designed to operate in variable frequency critical conduction mode (CrM) which is the most appropriate solution for 150 W (< 180 W):

- The discontinuous operation mode does not require a hyper fast diode with t_{rr} < 25 ns (with higher V_f) but allows the use of the latest diodes developed by ON Semiconductor for discontinuous mode PFC circuits.
- The new MUR550 has a V_f < 0.98V for 5A @ 150°C which provide an improved efficiency for this 520 V diode which provide 20% of margin for the 410 V PFC output.
- In CrM, the next switching cycle is initiated when the boost inductor current reaches zero. This control method means that the frequency inherently varies with the line input voltage and the output load. For detailed information on the operation of CrM Boost converter for PFC applications, please refer to AND8123 at www.onsemi.com.
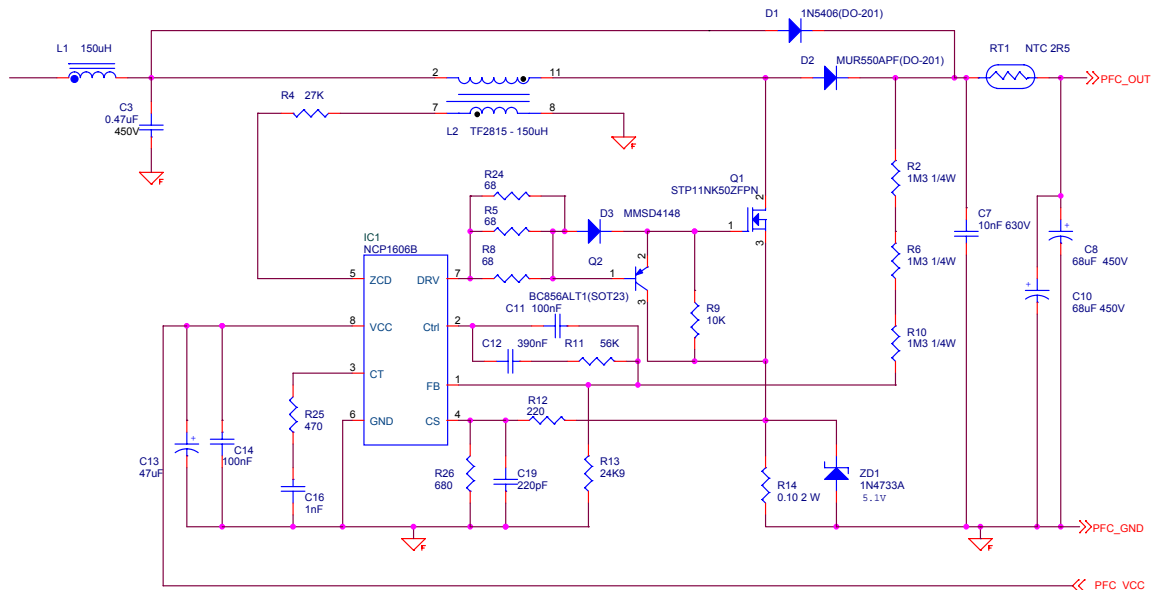
Figure 3: PFC Stage

Pin 1 (FB) senses the boost output voltage through the resistor divider formed by R2, R6, R10 and R13. (The NCP1606B allows 4 time higher impedance than NCP1606A for the same Over Voltage Protection: thus reducing parasitic standby power consumption). This pin is the input of the error amplifier, whose output is pin 2 (Ctrl). A combination of resistor R11 and capacitors C11 and C12 between those pins form a compensation network that sets the bandwidth of the converter. For good power factor, this bandwidth is generally below 20 Hz.

Capacitor C16 is connected to pin 3 (Ct) to set the on time for a given control voltage. The added resistor R25 in series with C16 provides an offset which allow further reduction of T_{on} min to provide better stability during light load and high

mains input voltage. Additional resistors from the input voltage to Ct could improve the power factor performance but in this application it is not necessary. Moreover they would increase power consumption in standby mode.

CS (pin 4) provides cycle by cycle over current protection. This is accomplished with an internal comparator which compares the voltage generated by the switch current and Rsense (R14 through divider R12 and R26) to an internal reference. The NCP1606B has a lower current sense threshold of 0.5 V (compare to 1.7 V for the NCP1606A) to reduce Rsense power dissipation. The added capacitor C19 filters any switching spikes which may impact the operation of the current sense input. Zener ZD1 is added to protect R14 in case of short circuit of the power switch Q1 and avoid damage to the controller with an open power connection.

Pin 5 (ZCD) senses the demagnetization of the boost inductor. The next driver switching cycle begins when the voltage at this pin rises above 2.1 V (typical) and then drops below about 1.6 V (typical). A resistor (R4) from the zero current detection (ZCD) winding limits the current into this pin. By pulling this pin to ground, the driver pulses are disabled and the controller is placed in a low current standby mode.

The NCP1606B features a powerful output driver (pin 7). This driver is capable of switching the gates of large MOSFETs in an efficient manner but to reduce EMI with a long PCB lead trace and high di/dt switching an added PNP transistor Q2 has been added which is placed as close as possible to the power switch Q1. Additionally, the driver incorporates both active and passive pull-down circuitry to prevent the output from floating high when Vcc is off.

Pin 8 (Vcc) powers the controller. When Vcc is below its turn on level - Vcc(on), typically 12 V dc - the current consumption of the part is limited to < 50 uA. Vcc is directly supplied from the flyback converter through signal transistor Q108 controlled by the optocoupler PC101 which is OFF in Standby mode:

- Both Vcc (Flyback and PFC) are compatible
- The PFC is switching OFF so that the flyback is directly supply by the mains voltage without boost operation in Standby mode
- This approach improves further standby power performance thanks to the two stage SMPS system

Design Procedure

The design of a CRM Boost PFC circuit has been discussed in several ON Semiconductor application notes (see appendix). This section will briefly go through the design procedure for a 400 V, 180 W converter based on the NCP1606B PFC controller. A design tool, which gives these equations and results, is available at www.onsemi.com.

Step 1: Define the boost parameters

Minimum AC Line Voltage	Vac_{LL}	88	Vrms
Maximum AC Line Voltage	Vac_{HL}	264	Vrms
Line Frequency	f_{LINE}	47-63	Hz
Boost PFC Output Voltage	Vout	400	V dc
Maximum Output Voltage	Vout(max)	430	V dc
Boost Output Power	Pout	170	W
Minimum Frequency	f(min)	90	kHz
Estimated Efficiency	η	95	%

Step 2: Calculate the Boost inductor and peak currents

The inductor's peak current is greatest at full load and low line. The value is calculated with eq 1:

$$Ipk(\max) = \frac{2 \cdot \sqrt{2} \cdot Pout}{\eta \cdot Vac_{LL}} = 5.8 \text{ A} \tag{1}$$

Now, the maximum boost inductor can be calculated:

$$L \leq \frac{2 \cdot Vac_{LL}{}^2 \cdot (\frac{Vout}{\sqrt{2}} - Vac_{LL})}{Vout \cdot Vac_{LL} \cdot Ipk(\max) \cdot f(\min)} = 164 \mu H \tag{2}$$

A value of 150 µH was selected.

The f_{min} may be considered high but this allows the use a small / cost effective PFC coil without major impact on both efficiency and EMI.

Step 3: Size the power components

The power components must be properly sized for the necessary current and voltages which they will experience.

1. The Boost inductor, L

The inductor's peak current is greatest at full load and low line. The value is calculated with eq 1:

$$Icoil_{RMS} = \frac{2 \cdot Pout}{\sqrt{3} \cdot Vac_{LL} \cdot \eta} = 2.35 \text{ A} \tag{14}$$

An ER28 core was selected as it is a high volume commonly available product with a total height < 23 mm. The 150 µH is build with 55 turns of 0.10 mm x 70, is able to manage up to 7 A for L > 80% @ 100°C with limited power dissipation thanks to the very good wire. The auxiliary winding for ZCD has 6 turns of 0.22 mm wire. The reference of the coil is JLC2832 and is available from Shenzhen Jewel Electric.

2. The Boost Diode, D_{BOOST} D2

$$Id_{MAX}(rms) = \frac{4}{3} \cdot \sqrt{\frac{2 \cdot \sqrt{2}}{\pi} \cdot \frac{Pout}{\eta \cdot \sqrt{Vac_{LL} \cdot Vout}}} = 1.2 \text{ A} \qquad (15)$$

The MUR550APF, axial type in DO-221 was selected as it has a much lower V_f than standard ultra fast diodes and is specially designed for CrM / DCM PFC, thus improving the boost stage efficiency without cost increase.

3. The MOSFET, Q1

$$I_M(rms) = \sqrt{\frac{4}{3} \cdot \left(\frac{Pout}{\eta \cdot Vac_{LL}}\right)^2 \cdot \left[1 - \left(\frac{8 \cdot \sqrt{2} \cdot Vac_{LL}}{3 \cdot \pi \cdot Vout}\right)\right]} = 2 \text{ A} \qquad (16)$$

The MOSFET will see a maximum voltage equal to the Vout overvoltage level (430 V dc for this example). If 90% derating is used for the MOSFET BV_{DSS}, then a 500 V FET is necessary to give adequate margin.

A STP11NK50ZFPN with 11 A capability and an R_{DSON} < 0.52R @ 10 A was selected to minimize power dissipation. This power MOSFET is housed in a TO-220FP and is mounted on a heat-sink to improved power dissipation.

4. The sense resistor, R_{SENSE}

$$R_{SENSE} = \frac{Vcs(\lim it)}{Ipeak} = 0.087 \text{ } \Omega \qquad (17)$$

For the NCP1606B, Vcs(limit) = 0.5 V (typ)

To simplify design / procurement issues, a standard 0.1R with resistor divider (R12 & R26) can be used to adjust the current limit to the desired threshold level.

$$P_{Rsense} = I_M(rms)^2 \cdot R_{SENSE} = 0.4 \text{ W} \qquad (18)$$

5. The bulk capacitor, C_{BULK}

$$Ic(rms) = \sqrt{\frac{32 \cdot \sqrt{2} \cdot Pout^2}{9 \cdot \pi \cdot Vac_{LL} \cdot Vout \cdot \eta^2} - (I_{LOAD}(rms))^2} = 1.13 \text{ A} \qquad (19)$$

The bulk cap value was calculated to give acceptable ripple voltage while avoiding triggering the output over voltage protection. To avoid expensive low profile Snap-in types and stay below the 25 mm height maximum of this design, two standard capacitors (C08/C10) are used in parallel and mounted flat on the board to achieve the target ripple current while offering a cost effective solution.

The capacitors selected are KXG 68μF 450 V 18*20 or 18*25 mm 0.58 A rms from Nippon Chemi-con.

Step 4: Supply Vcc to Bias the PFC
Generally, the most straightforward way to bias the PFC chip is with a resistor connected between the AC input and Vcc (pin 8) to charge the Vcc cap. For the LCD-TV application, there is a flyback converter that is always on even when the TV is in standby. As a result, the PFC controller is supplied directly from the auxiliary winding of the flyback converter thought and optocoupler which switches OFF the PFC when the TV is powered down and enters standby mode.
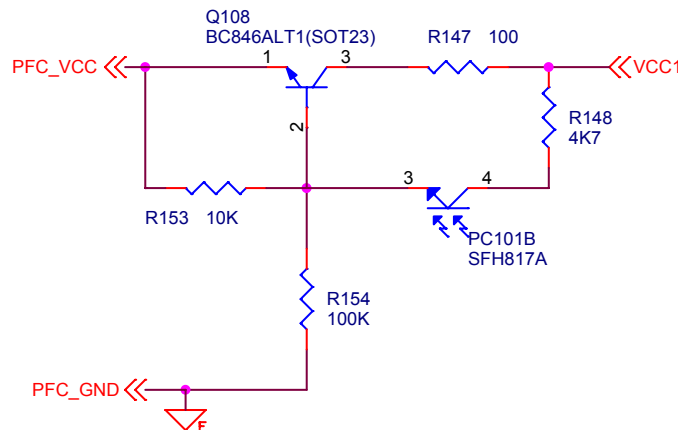
Figure 4: PFC Bias Control

When the TV set must be started, the microprocessor provides an ON signal which drives the optocoupler PC101 on; so that the flyback Vcc is apply to the PFC Vcc through Q108. When the Vcc voltage exceeds the Vcc(on) level (12 V dc typical), the internal references and logic of the NCP1606 turn on. The controller has an under-voltage lockout (UVLO) feature which keeps the part active until Vcc drops below about 9 V dc. This hysteresis is large enough to handle the flyback Vcc variation under normal load variation.

Step 5: Limit the Inrush Current
The sudden application of the mains to a PFC circuit can result in a large in-rush current and voltage overshoot. To resize the power components to handle this transient event is cost prohibitive. Furthermore, since the PFC is configured in a boost topology, the controller cannot do anything to protect against this since the voltage is applied through the inductor and rectifier to the output capacitor of the boost converter. To address this, a rectifier D1 is added from the input voltage to the output voltage bypassing the inductor and diverting the startup current to the bulk capacitor. The bulk capacitor is then charged to the peak AC line voltage without resonant overshoot and without excessive inductor current. After startup, D_{BYPASS} will be reverse biased and will not interfere with the boost converter.

Moreover, to further reduce the in-rush current which can be critical   for the mains fuse (limited I^2xt), a 2.5R NTC (negative temperature coefficient)

thermistor (RT1) is placed in series with the mains connection (before the bridge) to limit the in-rush current. The resistance value drops from a few ohms to a few milliohms as the device is heated by the I^2R power dissipation. Alternatively (as used in our application), this NTC can be placed in series with the boost diode. This improves the active efficiency as the resistor only sees the output current-- instead of the input current (particularly interesting for low US mains supply). However, in this configuration, NTC resistor may not be able to fully protect the inductor and bulk capacitor against in-rush current during a brief interruption of the mains, such as during line drop out and recovery.

Test Results

For figures 5-6, the signals illustrated in plots from top to bottom are as follows

- STANDBY   5V/div
- +5 V   5 V/div
- PFC VCC   10 V/div
- PFC-OUT   200 V/div

| 20 ms/div | 1 ms/div (expanded scale) |
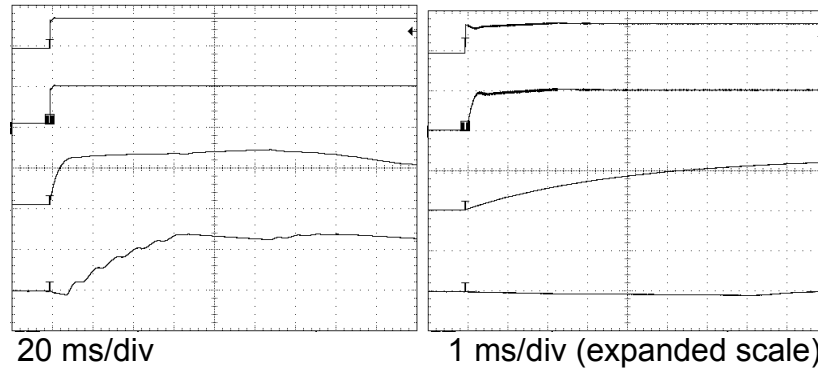
Figure 5: Starting phase from Standby to ON

1 s/div
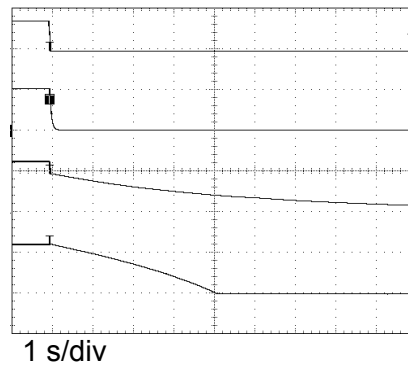
Figure 6: Switching OFF from ON to Standby

Mains current 0.5 A/div   F min 208 kHz (1 µs/div)   Fmax 295 kHz (1 µs/div)
Vin = 110 V ac, Pout = 75 W
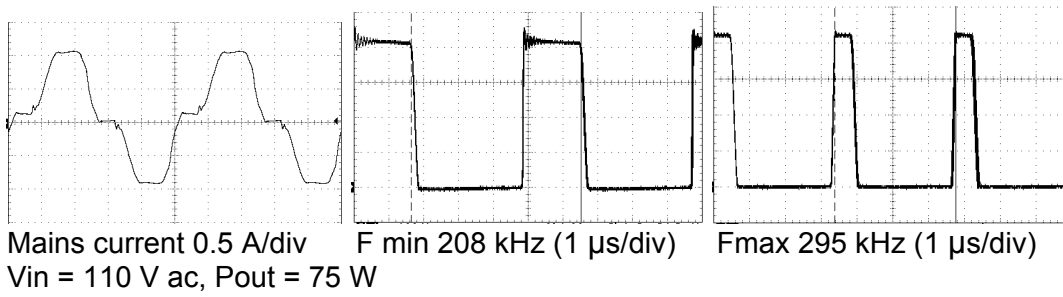
Figure 7: Input AC Current, PFC Switch Frequency (Drain Voltage of Q1)

Mains current 0.5 A/div   Fmin 297 kHz (1 µs/div)   Fmax 450 kHz (1 µs/div)
Vin = 230 V ac, Pout = 75 W
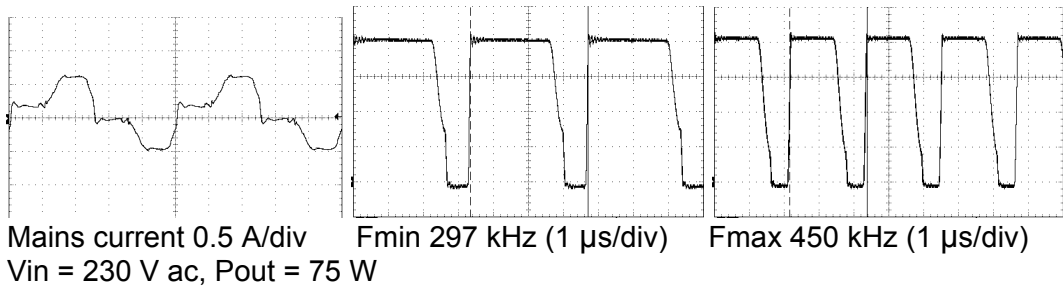
Figure 8: Input AC Current, PFC Switch Frequency (Drain Voltage of Q1)

Mains current 1 A/div   Fmin 105 kHz (2 µs/div)   Fmax 158 kHz (2 µs/div)
Vin = 110 V ac, Pout = 180 W
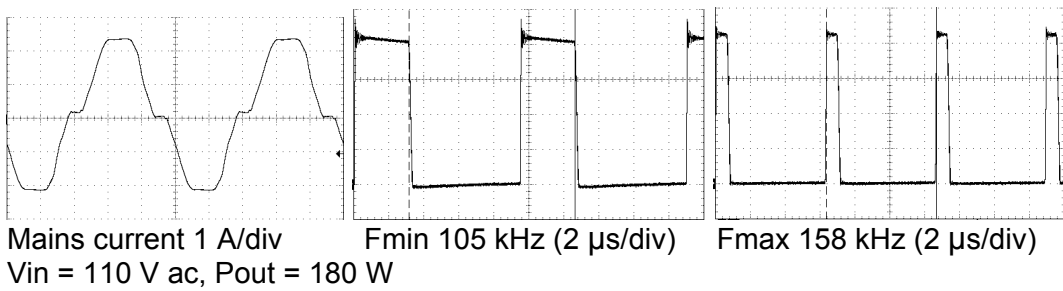
Figure 9: Input AC Current, PFC Switch Frequency (Drain Voltage of Q1)

Mains current 1 A/div   Fmin 158 kHz (2 µs/div)   Fmax 562 kHz (0.5 µs/div)
Vin = 230 V ac, Pout = 180 W
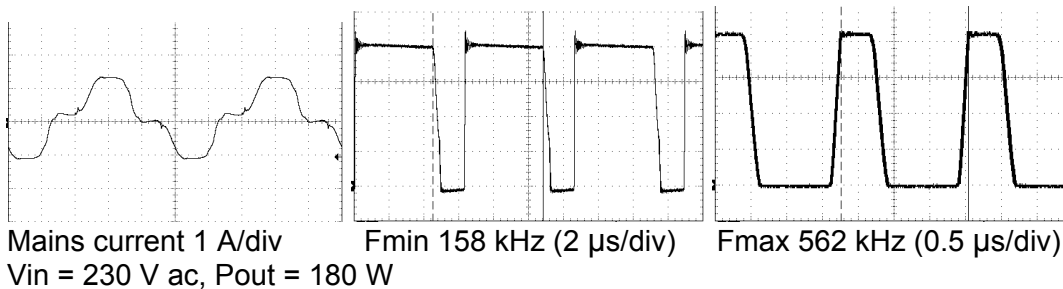
Figure 10: Input AC Current, PFC Switch Frequency (Drain Voltage of Q1)

Flyback Stage for Control, Signal & Audio Power

With a dedicated dc-ac converter to supply the lamps, the flyback SMPS is used to provide power to all the analog and digital blocks use for control, signal processing and audio amplification. With a limited overall requested power (< 60 W), it is possible to consider a flyback with standby mode without the need of a dedicated standby SMPS which improves the overall cost effectiveness of the solution. To achieve such a feat requires a controller architecture that is optimized for high efficiency at light load conditions.

NCP1351 variable OFF time PWM controller

The NCP1351 is a variable frequency controller implementing a fixed peak current (quasi-fixed-Ton) together with a variable off time technique. It is tailored for low power applications, mainly off line flyback power supplies below 80 W.

Based on a fixed peak current technique, the NCP1351B decreases its switching frequency as the load becomes lighter. As a result, a power supply using this solution naturally offers excellent no-load power consumption, while optimizing the efficiency under other loading conditions. As the frequency decreases, the peak current is gradually reduced to approximately 30% of the maximum peak current to prevent transformer mechanical resonance. The risk of acoustic noise is thus greatly diminished while achieving overall good standby power performance.
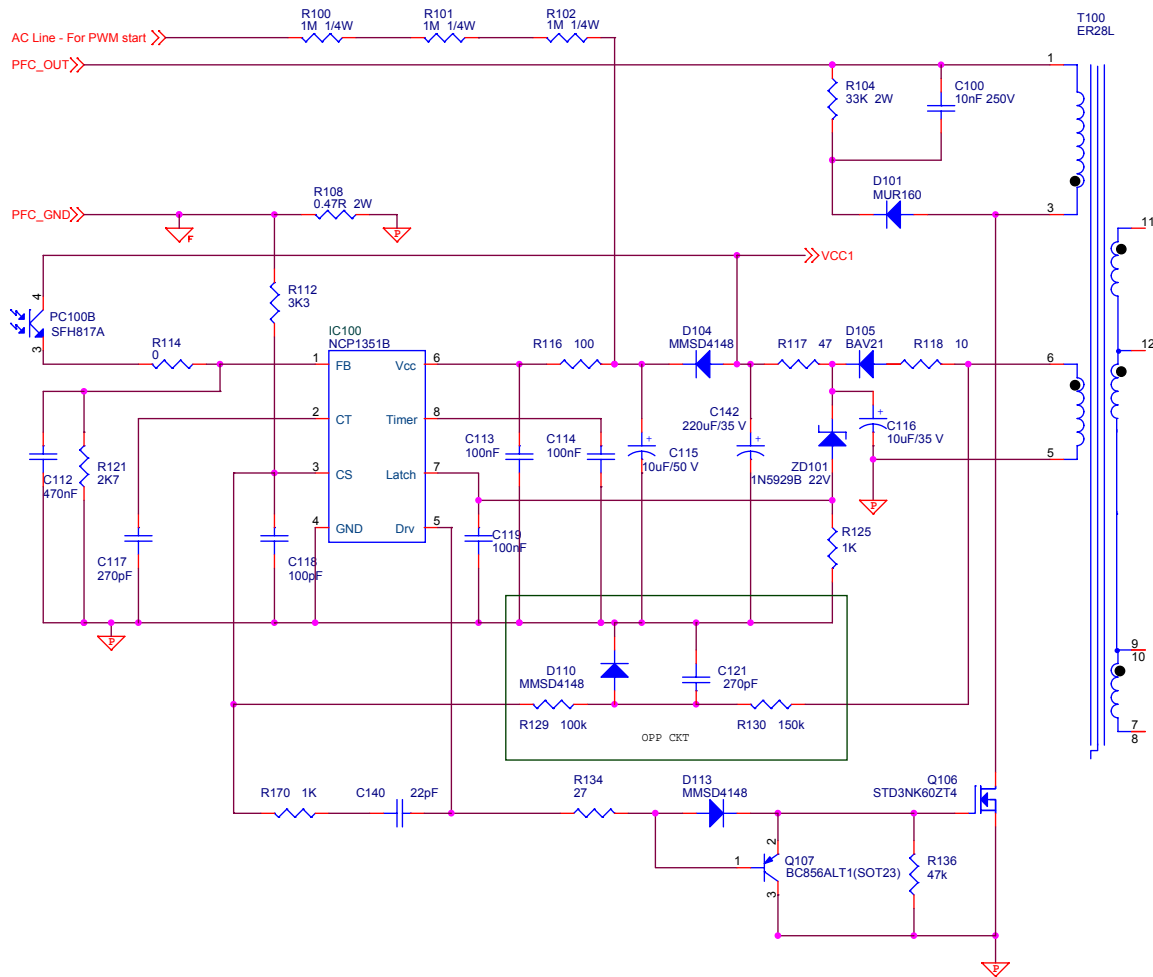
Figure 11: Primary side of the flyback converter

A 270 pF capacitor (C117) connected on pin 2 (Ct) defines the maximum frequency without feedback information. An adjustable timer permanently monitors the feedback activity and protects the supply in the presence of a short circuit or overload. The feedback is completely independent of the coupling between transformer windings. Once the timer elapses (capacitor C114 100 nF connected on pin 8 "Latch" reaches 5 V dc), the NCP1351 stops switching and tries to restart. On the NCP1351A, the protection is latched, and on the NCP1351B it has auto-recovery which is optimum for LCD-TV applications.

The Latch fault input (pin 7) is available to provide additional protection functions such as over-voltage protection (OVP) by sensing the primary auxiliary fly-back voltage. A fault is detected when pin 7 exceeds 5 V dc. The OVP detect signal is generated when the zener diode ZD101 starts to conduct current indicating the OVP fault. Note that neither the NCP1351A & B will auto-restart when the fault is removed due the latch function on pin 7 as a result the AC power must be disconnected to reset the NCP1351.

The internal structure features an optimized arrangement which results in an extremely low start-up current, a fundamental consideration when designing a power supply to achieve low standby mode. The starting resistors R100-101-102 (3 x 1MR) are connected directly to the mains to limit power consumption in standby. To reduce the starting time, the above starting resistors charge a small 10 µF capacitor (C115). Once the SMPS has started up, the voltage from the auxiliary winding supplies the Vcc pin through diode D105. To avoid any startup issues under light switching, a larger capacitor C142 is connected through the isolation diode D104 to allow a smaller capacitor value to start the IC quickly.

The negative current sensing technique minimizes the impact of the switching noise on the controller operation and allows the user to select the maximum peak voltage across the current sense resistor R108. Its power dissipation can be optimized and adjusted by R112. Lossless mains over-power-protection is provided through a network of R130, C121, D110 and R129 which is connected to the auxiliary flyback winding. Finally, the bulk input ripple ensures a natural frequency dithering which smoothes the EMI signature.

To provide better noise immunity in the PCB layout, an additional RC network R170 & C140 between DRV pin 5 and CS pin 3 provides leading edge blanking (LEB) which avoids instability due to noise on CS. While this may not normally be required with a negative current sense, in this case it improves performance without shortening switching cycles. Due to the negative current sense, the LEB is implemented with positive information from the DRV signal.

The feedback pin 1 (FB) operates based on a current signal that allows a direct connection to the optocoupler. C112 and R121 are used to define the regulation loop response time. Although the Driver pin 5 (DRV) is capable of driving directly the Power MOSFET Q106, an additional PNP bipolar transistor Q107, placed very close to the MOS, is used to switch OFF the MOSFET and avoid high di/dt on long PCB tracks thus reducing EMI generation. As illustrated, the 8 pin SOIC based NCP1351 provides all the basic SMPS control functions and give the user the option to implement numerous protection features to ease the design of a rugged and reliable low power switching power supply.

ON Mode Operation

Since the controller operates in quasi-fixed-Ton the switching frequency does vary with load. For light loads, the flyback converter operates in discontinuous mode (DCM). As the load increases the frequency increases until the controller enters continuous conduction mode (CCM) which is optimal for highest efficiency. The SMT (Switch Mode Transformer) has been designed to operate in both DCM and CCM to maximize performance.

In CCM higher inductance is required which increases the number of turns in the transformer, this mode provides better cross regulation due to the lower voltage per turn which allows better adjustment of the multiple output voltages and

increase the coupling between all secondary windings and between primary to secondary. This avoids a dead time which improves overall current form factor and reduces overall peak current in the system (MOS, transformer, diodes and capacitors). A possible drawback of approach is the recovery time of secondary rectifier power diodes, but this issue does not exist here since all secondary diodes use schottky technology in view of the output current required. The primary / secondary turn's ratio has been choosing allow the use of high volume cost effective 600 V MOSFET. The transformer has a primary inductance of 2.5 mH which allows it to be in DCM for low power and enter CCM around 35 W output. The primary current is around 1.6 A for 60 W.

Build on an EER28L, the transformer design consists of the following:

- Primary has 2 x 55 turns
- Auxiliary Vcc has 26 turns
- 5V secondary has 9 turns
- 12V secondary build on top of 5V has 9 turns

The reference of the transformer is BCK-28-1050 and is available from Shenzhen Jewel Electric.

Cross Regulation Considerations

Achieving good cross regulation is a design challenge in LCD-TV applications as the tolerances are tight, typically +/- 5% and the dynamic operation can vary widely due to the high dynamic range of the audio amplification and the variety of signal processing power load depending on the input video source. Below is the typical output voltage and load range for the baseline reference design (SMPS1).

- +5V from 0 to 2.5A
- +12V from 0 to 4A

To improve the overall cross regulation performance, the +5V diode is connected in the ground (GND) of the winding with +12 V on top of the 5 V winding. The drawback of that is that both the +5V and +12V current go through both the 5 V diode and winding (increasing power loses mainly in the +5V diode), the advantage of this configuration is that the 12 V only sees 7 V of variation. An additional advantage of this construction is that the reverse voltage of the 12 V diode is limited by the same difference. Note the transformer was designed with a low turns ratio thus reducing the effective current but increasing the reverse voltage of the diode. In the reference design, a 100 V is used to ensure adequate design margin and avoid the possibility of any reliability issues. This also simplified procurement as the same T0-220 MBR20100CTG diode is used in both outputs.

Flyback Waveforms

Drain voltage   200 V/div
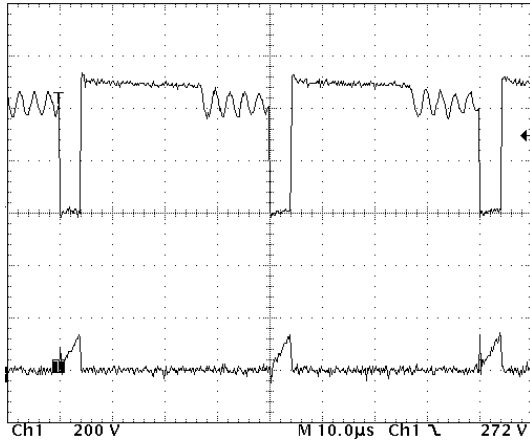
Drain current   1 A/div

Ch1   200 V   M 10.0µs Ch1 ⌐   272 V

Figure 11: 25 kHz Operation (DCM)

PFC = 400 Vdc, 5 V@ 0.5 A and 12 V @ 0.5 A

Drain voltage   200 V/div
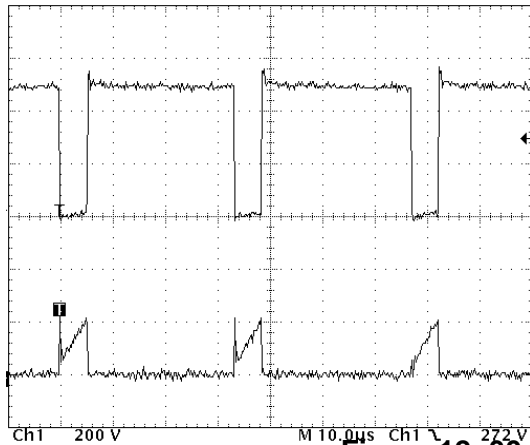
Drain current   1 A/div

Ch1   200 V   M 10.0µs Ch1 ⌐   272 V

Figure 12: 30 kHz Operation (CCM)

PFC = 400 Vdc, 5 V@ 1 A and 12 V @ 2 A

Drain voltage   200 V/div
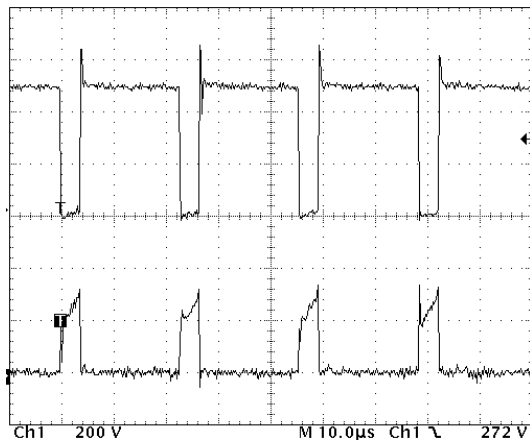
Drain current   1 A/div

Ch1   200 V   M 10.0µs Ch1 ⌐   272 V

Figure 13: 43.8 kHz Operation (CCM)

PFC = 400 V dc, 5 V@ 2 A and 12 V @ 4 A

5 V diode D111, Vrr = 40 V Max   12 V diode D107, Vrr = 52 V Max
10 V/div   10 µs / div
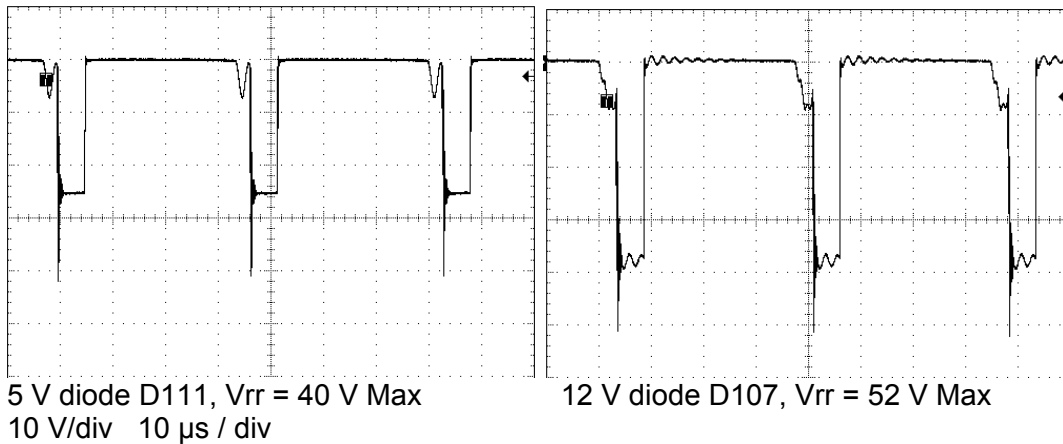
Figure 14: 17 W load: 5 V@ 1 A and 12 V @ 1 A (DCM mode)

5 V diode D111, Vrr = 35 V Max   12 V diode D107, Vrr = 50 V Max
10 V/div   4 µs / div
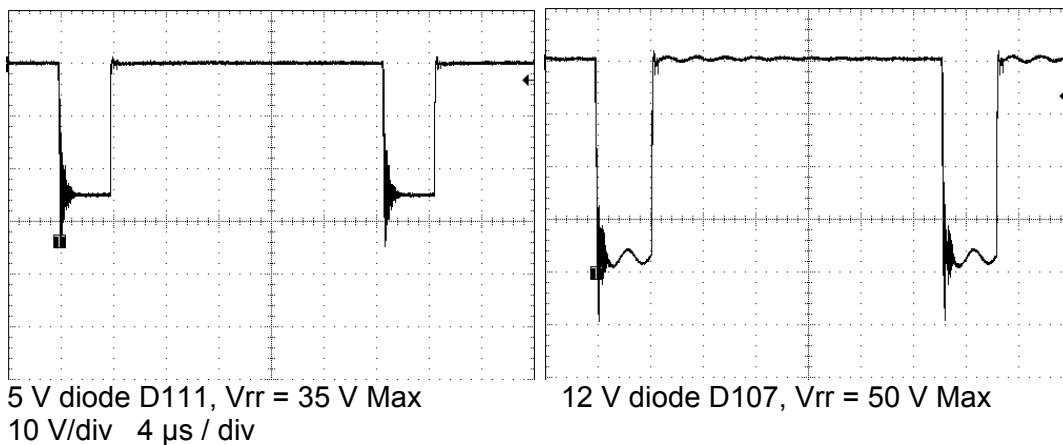
Figure 15: 52 W output: 5 V @ 2 A and 12 V @ 3.5 A (CCM mode)

Standby Mode Considerations

The architectural approach used in the NCP1351 is optimized to achieve optimal performance for light load efficiency. As a result, a dedicated standby flyback converter is not required in this reference design. In standby mode, there is limited power required to keep the microprocessor and control circuitry biased when the LCD-TV is switched off. To achieve this low standby performance, it is necessary to have additional switches on the secondary side to disconnect both 5 V dc (Q113) and 12 V dc (Q114) so that only the 5 V dc standby power rail remains connected. Those two switches are supply with VS4 from a charge pump (CC103, D100, ZD100 and C101) to avoid an additional winding on the transformer T100.

This available higher voltage allows the use of NMOS switches instead of PMOS switches for the high side switches power rails. Avoiding PMOS switches reduces cost and solved additional safety issues in the event of an overload or output short circuit since the PMOS switches could go out of saturation and enter

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the linear region resulting in increased power dissipation and possible overheating.

Figure 16: Secondary side rectification of the Flyback converter

The charge pump voltage VS4 is always available (even in Standby mode). There is no need for a switch to disconnect in Standby as the charge pump provides a fixed amount of energy per cycle and thanks to the very low frequency operation in Standby, the power is very limited, VS4 is very low and does not have a appreciable impact on overall Standby power efficiency.
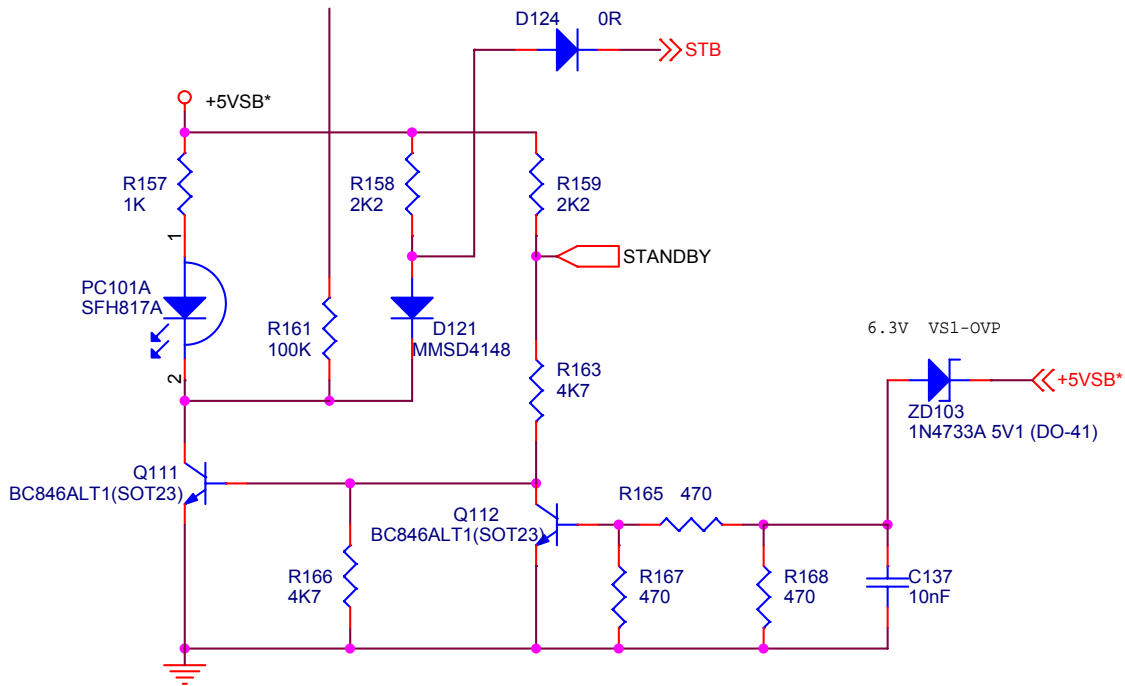
Figure 17: Secondary side Standby / ON control of the Flyback

The system microprocessor generates an open collector "STANDBY" signal that pulls R159 low when the system is in standby. When the STANDBY signal is released, Q111 is switched on to drive optocoupler PC101 which allows the PFC controller to be biased on (as explain in PFC part). The state of Q111 also controls signal "STB" which goes up in Standby. The STB is applied to diode D108 which provides a higher voltage than the regulated one on comparator Q103 which drives down the gate of Q114 to switch OFF the +12 V. The 'STB' going down in ON mode, allowing the +12 V to be switch ON as a supply from the charge pump VS4. The +5 V switch Q113, is directly drive by the +12 V.

Typical Standby performance

< 0.3 W (230 V ac) / 0.2 W (110 V ac)	no load
< 0.4 W (230 V ac) / 0.3 W (110 V ac)	5 V dc @ 10 mA (50 mW)
< 0.5 W (230 V ac) / 0.4 W (110 V ac)	5 V dc @ 20 mA (100 mW)
< 1 W (230 V ac) / 0.9 W (110 V ac)	5 V dc @ 96 mA (480 mW)

Note that the standby performance is achieved without the need of a costly relay to disconnect the rest of the supply where additional parasitic power losses occur. This standby performance is below the levels required to achieve < 1 W standby regulatory requirements. Note that further improvements could be achieved with modifications of the clamping network. To protect the MOSFET and prevent the voltage to be higher than the BVdss, the existing RC network (R104 & C100) could be replaced by a 200 V TVS to clamp the overshoot. This will reduce the

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standby power, as there is no power loss in the clamping network under no-load / light load conditions. If ultra low standby is required then a dedicated flyback could be added which would increase the overall system cost.

90 V ac 50 mW output 3.76 kHz	90 V ac 500 mW output 12.5 kHz
230 V ac 50 mW output 2.9 kHz	230 V ac 500 mW output 9.35 kHz
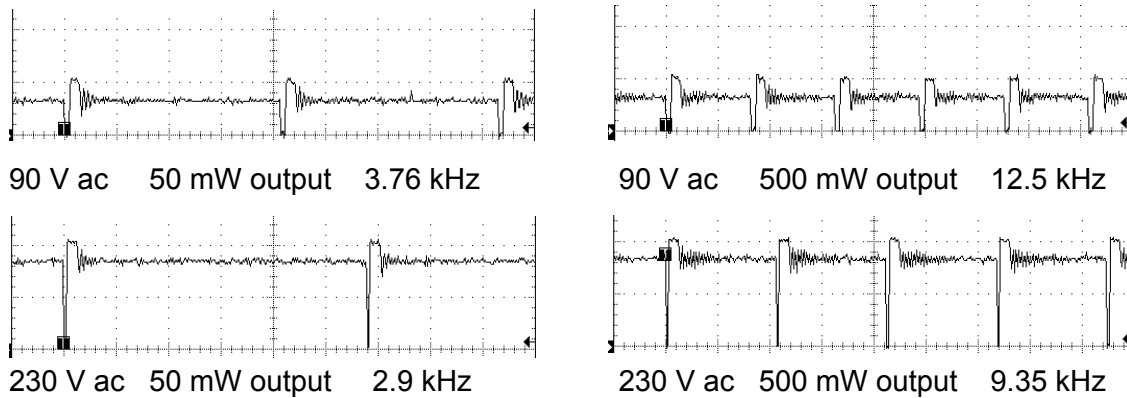
Figure 18: Flyback switching waveforms under different load conditions

Higher Standby power capability solution

In standby, the SMPS is operating in the audio range. As a result depending on the transformer construction and mechanical design there is the possibility of some audible noise. The most sensitive range for most people is in the 7 – 13 kHz range. This specific design has been implementation for a nominal standby load of 50-75 mW so that the frequency in standby is < 5 kHz. If the required standby power is higher, the converter may work in the critical audible range. To avoid this issue, we can change the current limit in standby mode to reduce the energy transferred by cycle so that frequency increases above the sensitive range (>15 kHz) to provide the overall requested power. This increased switching frequency does have a minor negative impact on efficiency in standby. The section describes how the standby current and frequency can be adapted to avoid the most critical 7 – 13 kHz range in standby.
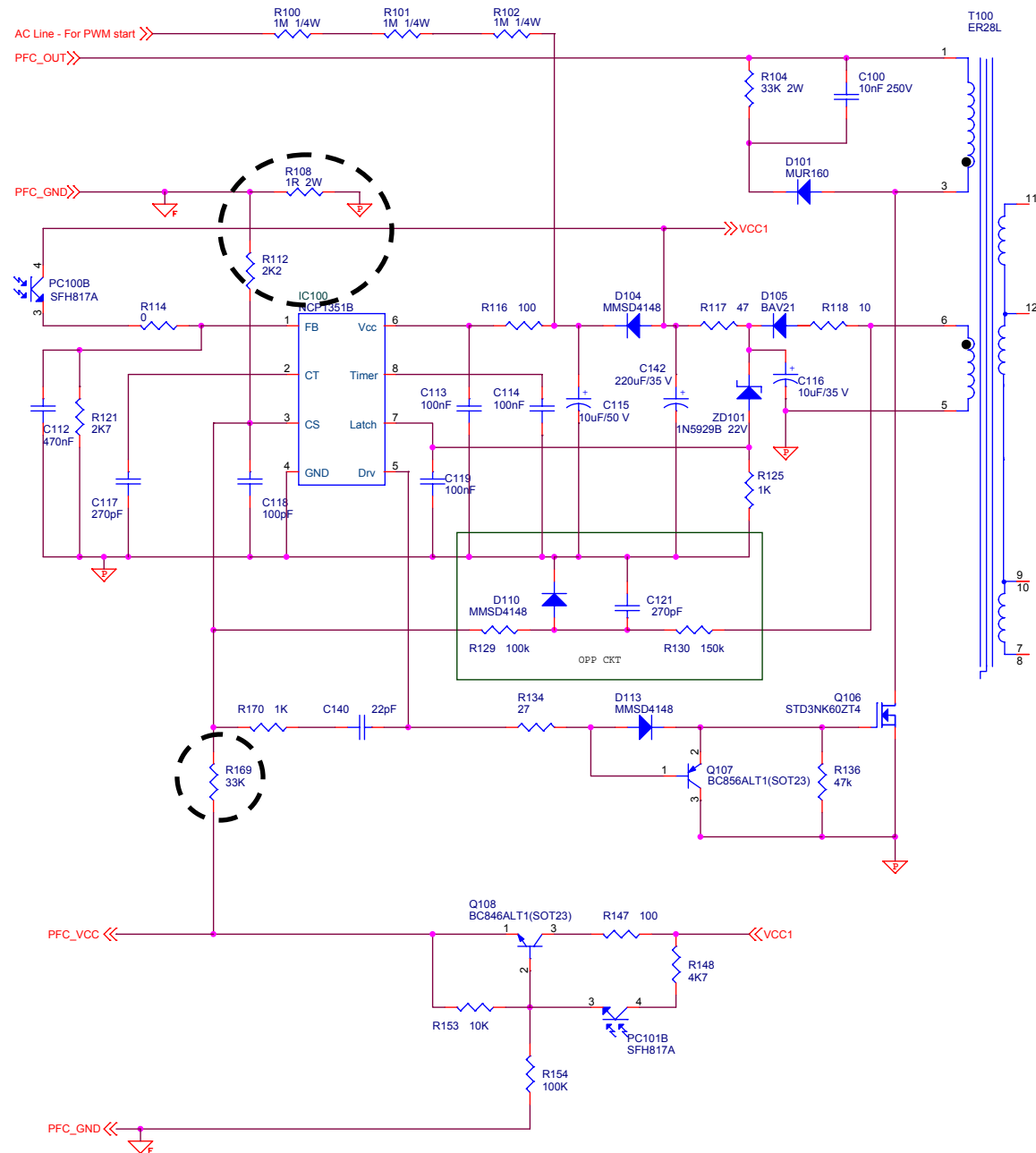
Figure 19: Modifications of the Flyback to increase standby frequency

The Rsense resistor R108 is increased from 0.47R to 1R which provides more voltage information and reduces the current (typically 1/2) in standby mode. To maintain the same operating current in ON mode, a positive current from R139 is generated when PFC_VCC is on which will compensate for the larger negative voltage developed by the larger sense resistance R108: The variation of this voltage between both ON and standby mode allows easy configuration. The changes were minor as R112 was reduced from 3K3 to 2K2 and R139 (33 K) was added. This provides up to 60 W power capability in ON mode with the same

current limit. The standby operating frequency is now 16.6 kHz with 160 mA in the Flyback Power MOS which is an increase from the 7 kHz in the original solution. This changes was implemented and tested and the results were excellent despite a small impact on efficiency (+ 50 mW on mains input compare to previous lower frequency mode).

200 V/div,   200 mA/div,   10 µs/div   200 V/div,   200 mA/div   1 µs/div
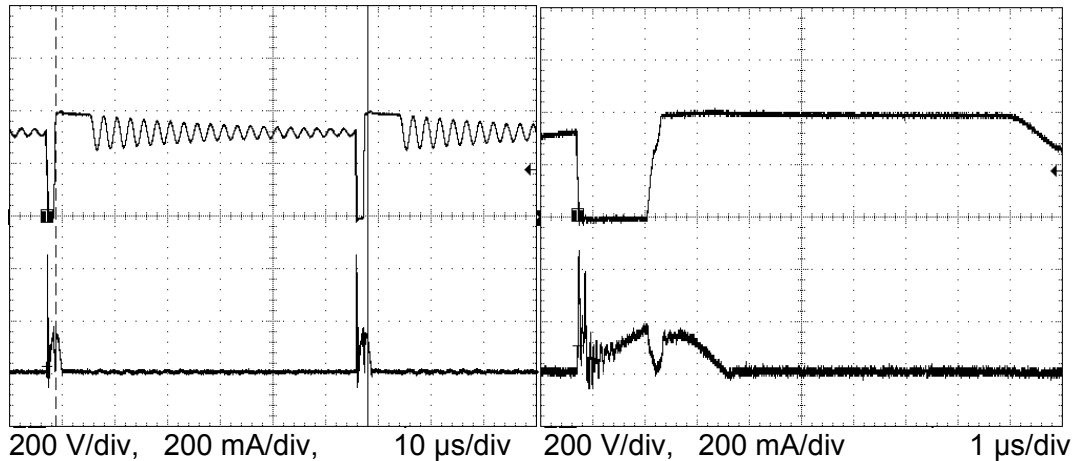
Figure 20:   Switching Waveforms with 400 mW output, Pin = 1 W
Vin = 230 Vac, Fsw = 16.6 kHz

100 V/div,   200 mA/div,   10 µs/div
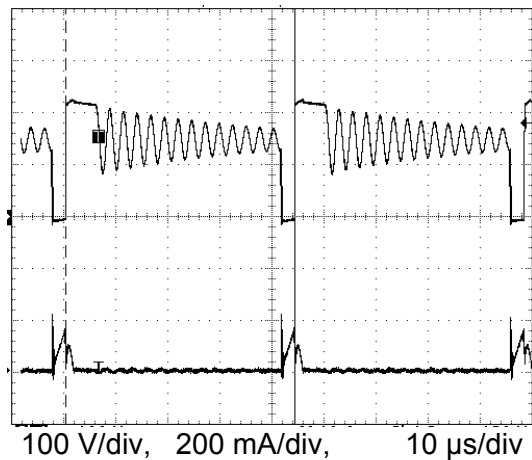
Figure 21:   Switching Waveforms with 400 mW output, Pin = 810 mW

Vin = 110 V ac, Fsw = 27 kHz

Configuring the Flyback for other output voltages

The required voltage rails and currents needed for the LCD-TV signal processing, audio and standby power are driven by the system architecture. As a result the reference design incorporates sufficient flexibility to support multiple output configurations with simple bill of material changes.   The NCP1351B flyback

design includes flexibility to support up to 4 unique voltage rails. The standard configuration (SMPS1) that the reference design uses has a 5 V dc and 12 V dc output as well as a 24 V dc Driver rail. The table lists numerous alternate configurations that can be realized to support different power schemes including a variety of different audio amplifier output rails range from 12 to 24 V dc.

The below table provides most of the possible solutions. In all cases, the overall power must be limited to < 60 W and < 4 A for both VS1 and VS2 and < 1.5A for the VS3 output. The current on V Dr is limited to approximately 5 mA according to the charge pump components used.

	SMPS1	SMPS2	SMPS3	SMPS4	SMPS5	SMPS6	SMPS7	SMPS8	SMPS9
V Dr	**24V**	36V	26V	24V	36V	24V	28V	24V	36V
VS3		24V ON	14V ON	12V ON	24V ON		15V ON		24V ON
VS2	**12V ON**	12V ON	12V ON	5V ON	12V ON	12V ON	12V ON		
VS1	**5V ON + Standby**	5V ON + Standby	5V ON + Standby	3V3 ON + Standby	3V3 ON + Standby	5V Standby LDO from 12V	5V Standby LDO from 12V	12V ON + Standby	12V ON + Standby

Table 3: Standard and alternative voltage configurations
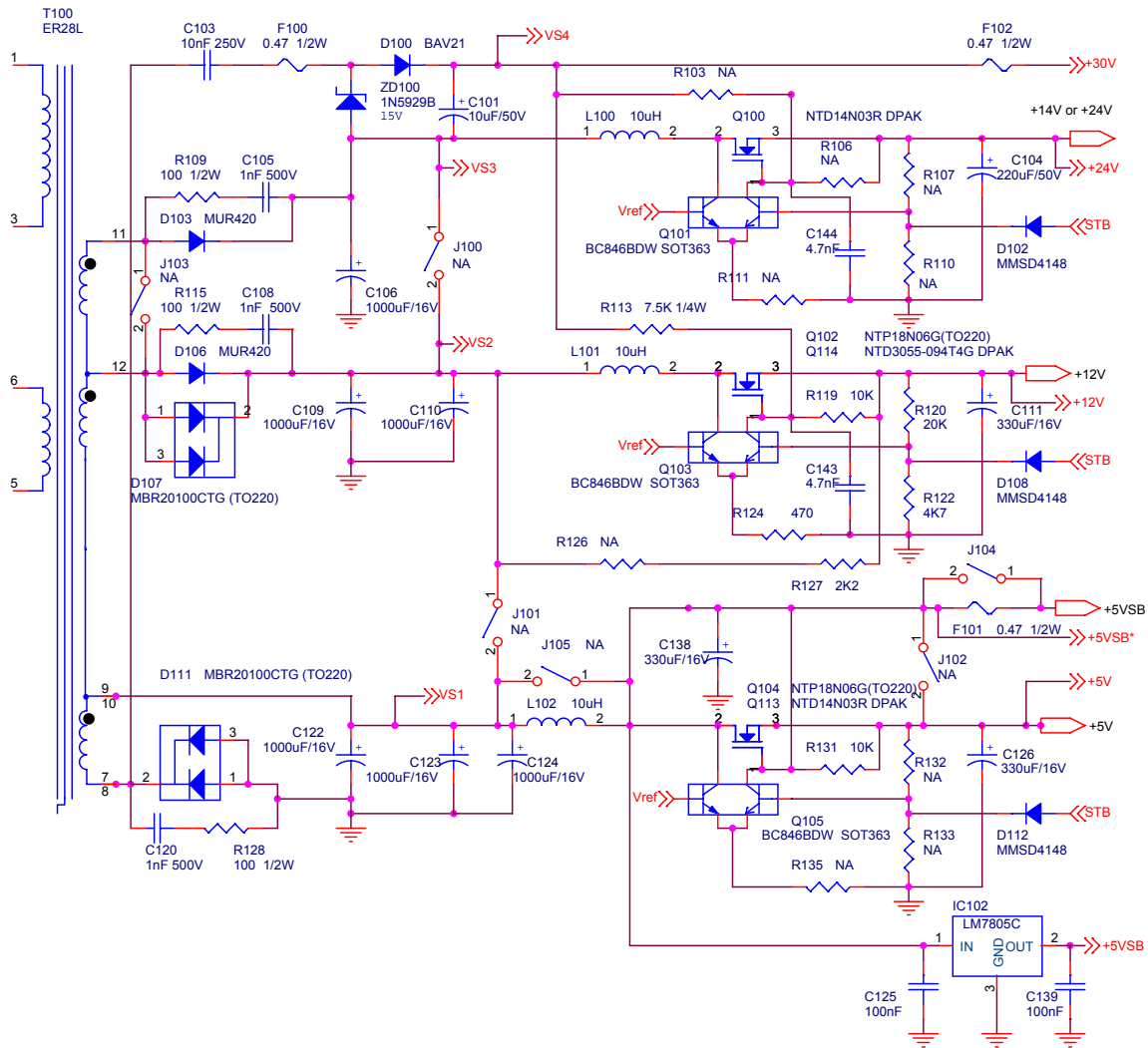
Figure 22: Schematic illustrating range of flexibility in configuring the secondary side rectification of the flyback converter

SMPS 1 to 5 are similar designs with 2 or 3 output voltages with the added Driver output rail to drive all NMOS switches. If VS1 has only one switch Q104 for the standby, both VS2 and VS3 support a linear regulator (function explained below) on top of the discrete switch used for the standby. The third output VS3 is of particular interest when a higher voltage rail is required to power a dedicated audio amplifier. The VS4 has a limited current capability (charge pump solution) but if necessary, the voltage can be push up to 35 V to allow 30 V for tuner through the resistive drop on fuse F102.

To be able to manage the strong load variation due to the wide audio amplifier dynamic behavior, the 12 V dc (VS2 of SMPS1) has been designed as a simple discrete regulator to avoid possible cross regulation issues: an additional discrete comparator forces the switch to operate in linear mode (not full saturated) when

the load becomes so small that the voltage can rise up toward the upper regulation limit. As a result of the transformer design and this discrete circuitry, the 12 V dc output of the SMPS configuration offers excellent load and cross regulation.
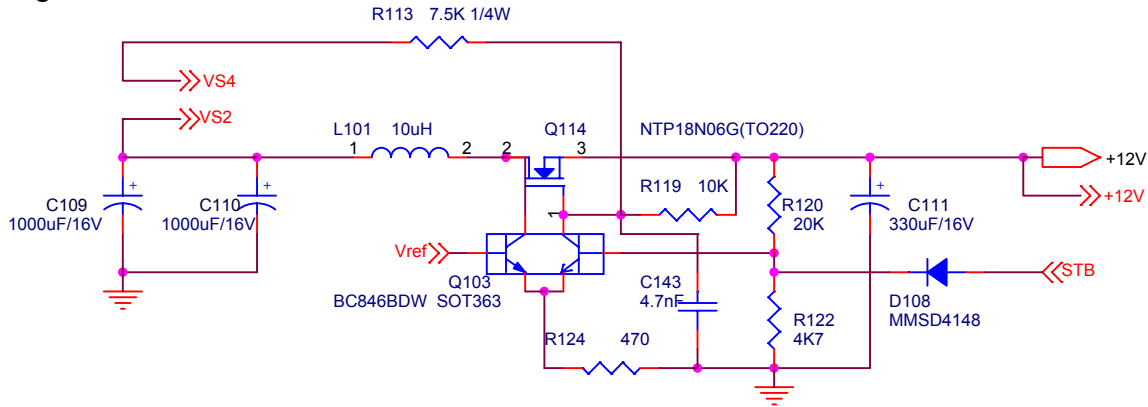
Figure 23: +12 V Discrete switch and linear regulator

The dual transistor Q103 is use as an amplifier to compare information from the +12 V output to the V_{ref} from the TL431 (IC101). This allows regulation on the +12V rail and forces the MOSFET to stay full saturated as much as possible under any condition. The MOSFET is housed in a DPAK so it has good power handling given the maximum current of the output rail. Finally an additional integrated linear regulator IC102 has been planned for SMPS6/7 to allow a simple low current standby supply from the VS1 (adjustable from 5 to 12 V). A modification of the regulation point (R161) in standby (see Figure 24) can reduce the VS1 supply voltage lower to reduce power dissipation across IC102 and improve standby efficiency.

VS1 / 5 Von VS2 / 12 Von VS4 / P 230 V~ I 12 Von	I 5 Von 0.1	0.5	1	1.5	2	2.5
0.1	5.23 / 5.23 12.63 / 12.43 26.09 / 6.799	5.23 / 5.23 12.65 / 12.42 25.91 / 6.8	5.18 / 5.07 12.85 / 12.44 25.93 / 12.3	5.17 / 5 12.92 / 12.45 25.89 / 16.33	5.13 / 4.91 13 / 12.47 26.2 / 19	5.12 / 5.07 13.13 / 12.33 26.93 / 23.25
0.5	5.27 / 5.27 12.54 / 12.4 26.02 / 12.27	5.27 / 5.27 12.55 / 12.39 25.85 / 12.35	5.25 / 5.14 12.68 / 12.42 25.89 / 18.77	5.24 / 5.07 12.74 / 12.43 25.84 / 22.66	5.24 / 5.01 12.78 / 12.45 26.06 / 25.7	5.23 / 4.96 12.84 / 12.31 26.69 / 28.73
1	5.28 / 5.28 12.52 / 12.36 26.06 / 20	5.28 / 5.28 12.53 / 12.36 25.95 / 20.13	5.27 / 5.16 12.63 / 12.4 25.91 / 26.59	5.27 / 5.09 12.68 / 12.41 25.86 / 30.21	5.26 / 5.04 12.71 / 12.43 26.08 / 33.18	5.26 / 4.99 12.76 / 12.29 26.63 / 36.23
1.5	5.29 / 5.29 12.52 / 12.33 26.14 / 27.57	5.29 / 5.29 12.53 / 12.32 26.03 / 27.73	5.27 / 5.17 12.6 / 12.36 26.01 / 33.88	5.26 / 5.09 12.62 / 12.37 25.94 / 37.49	5.25 / 5.03 12.64 / 12.38 26.05 / 40.43	5.24 / 4.96 12.68 / 12.26 26.6 / 44.37
2	5.29 / 5.29 12.51 / 12.27 26.18 / 35	5.29 / 5.28 12.5 / 12.26 26.13 / 35.03	5.26 / 5.16 12.56 / 12.3 26.05 / 41.17	5.26 / 5.09 12.61 / 12.33 25.96 / 45	5.26 / 5.04 12.64 / 12.35 26.05 / 48.08	5.26 / 4.97 12.69 / 12.25 26.6 / 51.55
3	5.27 / 5.27 12.46 / 12.13 26.36 / 49.65	5.27 / 5.27 12.46 / 12.12 26.2 / 49.88	5.28 / 5.17 12.57 / 12.21 26.26 / 56.73	5.28 / 5.11 12.61 / 12.25 26.13 / 60.34	5.28 / 5.06 12.66 / 12.28 26.27 / 63.79	5.29 / 5.01 12.72 / 12.24 26.69 / 67.45
4	5.29 / 5.29 12.49 / 12.03 26.67 / 65.64	5.29 / 5.29 12.48 / 12.02 26.64 / 66.19	5.3 / 5.19 12.6 / 12.12 26.61 / 72.69	5.3 / 5.12 12.64 / 12.15 26.72 / 77.07	5.29 / 5.06 12.65 / 12.16 26.83 / 80.5	5.28 / 4.99 12.67 / 12.11 27.11 / 83.81

ON with 0.32A on 5VStby

Table 4: +5V and +12V Output Performance over Load

The secondary regulation and safety circuit
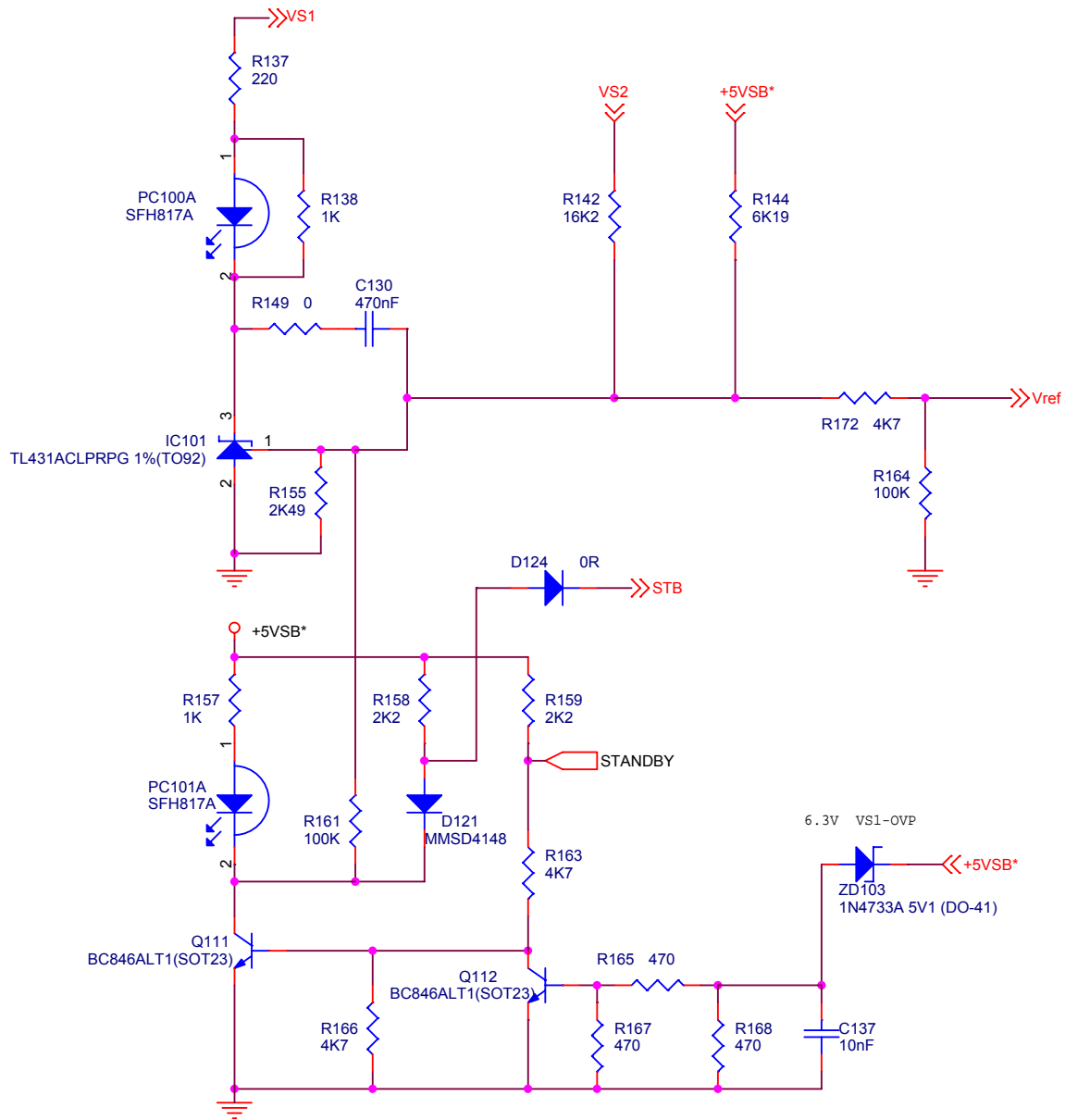
Figure 24: +12V Secondary regulation and safety circuitry

The regulation loop is controlled by a TL431 (IC101) and optocoupler PC100. To reduce consumption as much as possible in standby, the regulation circuit is supply by VS1 (5 V). Note the PCB has been designed with flexibility to allow regulation from any of the output voltages. In the standard configuration, SMPS1, both 5 V and 12 V are regulated with resistor dividers adjusted to have 2/3 on 5 V and 1/3 on 12 V. To compensate for voltage drops due to output filters and cables, the regulation point (reference pin 1 of IC101) is modified with resistor

R161. This has no impact during standby but during ON mode, R161 is in parallel with R155 to increase all output voltages.

The secondary safety circuit provides Over Voltage Protection in the event of an open regulation loop. If the +5 V Standby output exceeds 6.3 V (nom) (5.1 (ZD103) + 1.2 (V_{be} of Q102 following the resistor divider), the overall control circuit recognized the fault and forces the supply into STANDBY thus disconnecting the load, avoiding damage to the signal processing and reducing the power which helps to further increase the voltage to easily detect the issue on the primary and switch OFF the NCP1351 with the OVP and Latch protection (ZD101). To provide full design flexibility, OVP on each output voltage has been planned on the PCB with extra zener diodes (ZD104 on VS2 and ZD105 on VS3).

The high performance of the transformer (CCM) combined with the NMOS switches, does not affect the series impedance during an output short circuit providing rugged short circuit protection. The primary Over Power Limitation time will be controlled by the timer and the converter will stay OFF until the next re-start (for the auto-recovery NCP1351B).

Flyback safety tests

The following plots illustrate operation under unusual fault conditions that the power supply must handle during safety testing that are meant to simulate a possible failure in the field.

A) + 12 V Output short circuit

Figure 25 illustrates the switching behavior when a short is created on the 12 V output. The top waveform on the right is the 12 V output and it is being loaded from 1-8A (scale 5A/div). The next waveform is the drain voltage of Flyback MOSFET Q106 (scale 500 V/div). The bottom two waveforms are the 5 V Standby (5 V/div) and the drain current of Flyback MOSFET Q106 (1A/div). The plot to the left is a longer time frame and it clearly shows that the 45 ms fault timer being activated to disable operation. The third plot on the bottom shows an expanding view of the drain voltage and drain current of Q106 showing the current is limited in a cycle by cycle basis.

10 ms/div   10 µs /div

10 µs /div
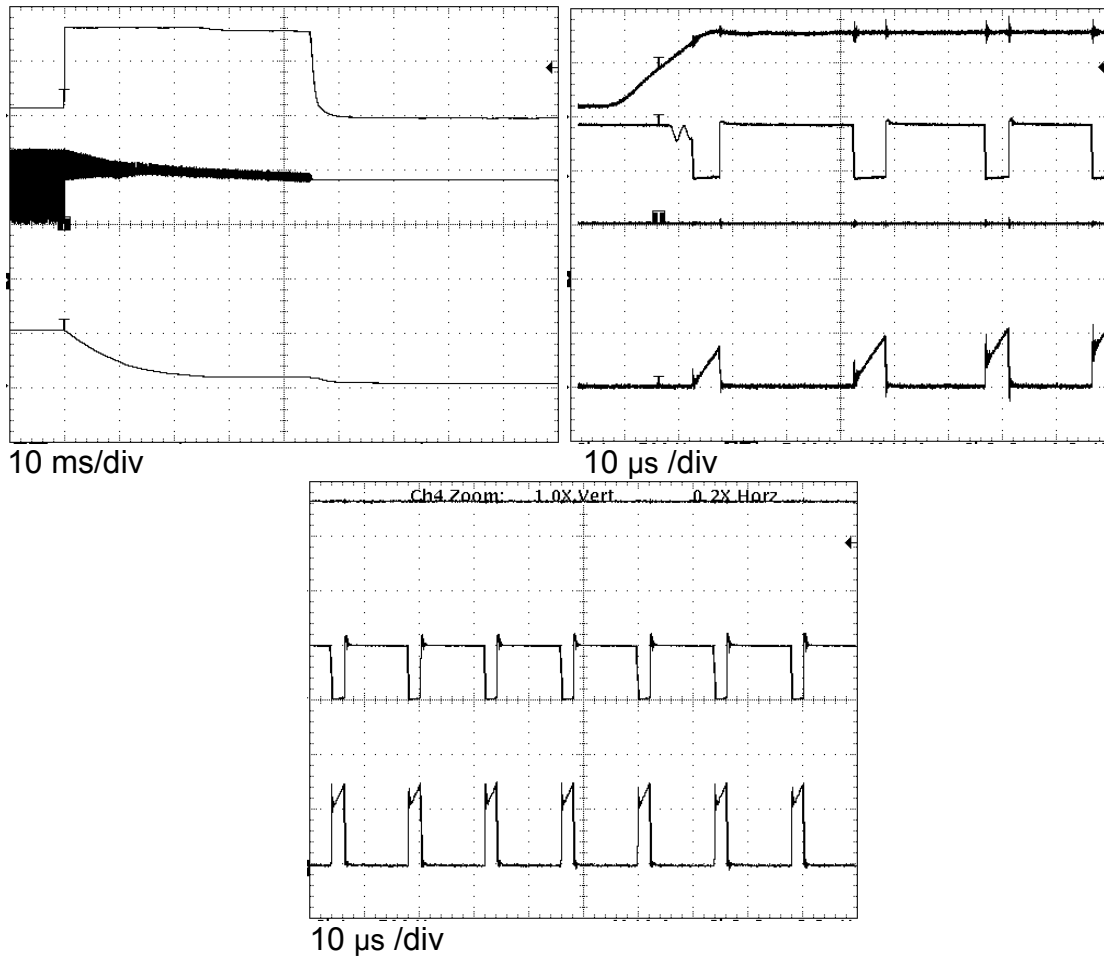
Figure 25: + 12 V Output short circuit behavior

B) + 5 V Output short circuit

Figure 26 illustrates the switching behavior when a short is created on the 5 V output. The top waveform on the right is the 5 V output and it is being loaded from 1-8A (scale 5A/div). The next waveform is the drain voltage of Flyback MOSFET Q106 (scale 500 V/div). The bottom waveform is the drain current of Flyback MOSFET Q106 (1A/div). The plot to the left is a longer time frame and it clearly shows that the 45 ms fault timer being activated to disable operation. In this plot the bottom waveform is the 12 V out and it clearly shows the output decaying after the timer is activated. The plot on the bottom shows an expanding view of the drain voltage and drain current of Q106 showing the current is limited in a cycle by cycle basis.

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10 ms/div   20 µs/div

10 µs /div
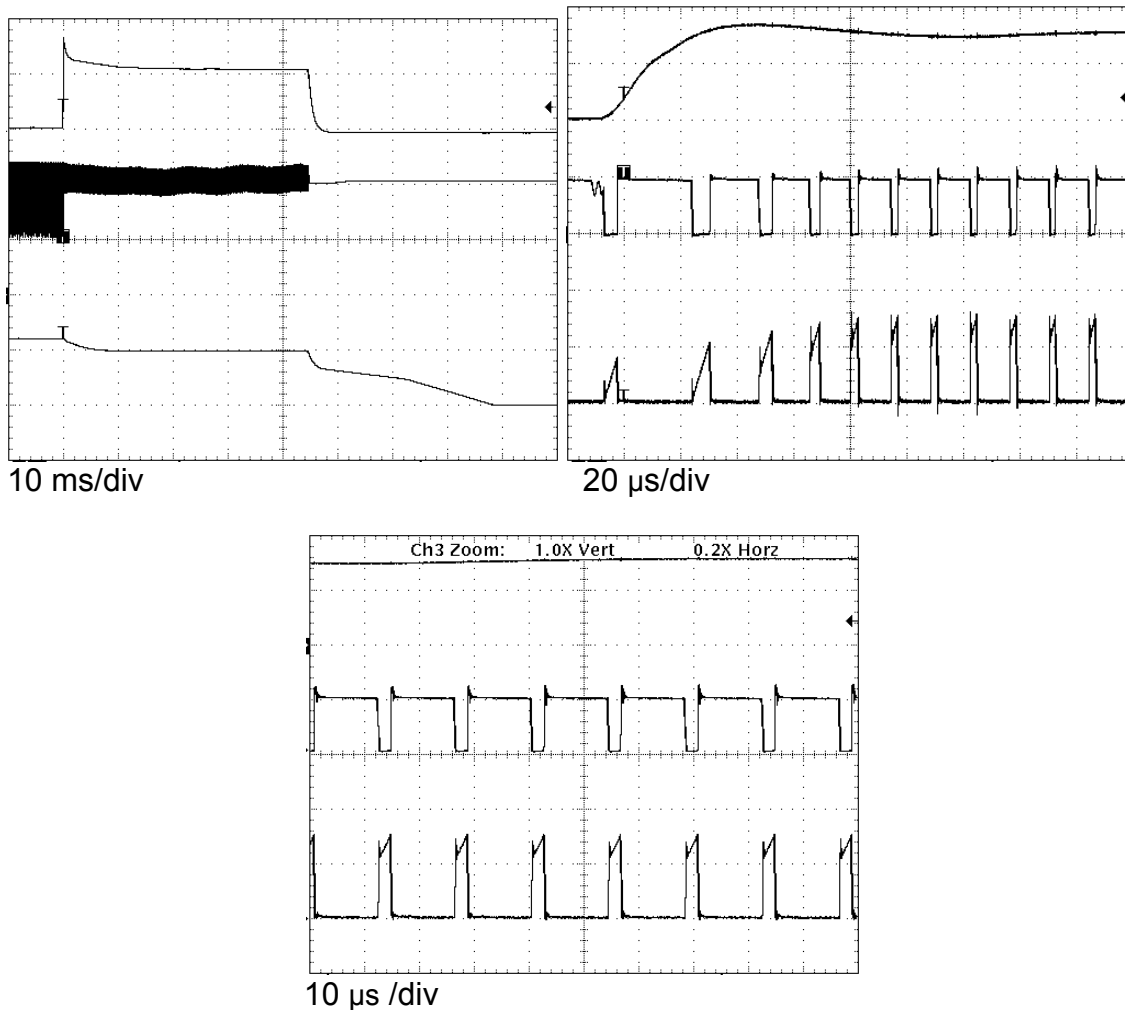
Figure 26: + 5 V Output short circuit behavior

C) PFC behaviors with + 12 V or + 5 V Output short circuit

Figure 27 illustrates the switching behavior of the PFC when either the 12 V or 5 V rail is shorted. The top waveform on the right is the 12 V output and it is being loaded from 1-8A (scale 5A/div). The next waveform is the drain voltage of Flyback MOSFET Q106 (scale 500 V/div). The bottom waveforms consist of the drain voltage of the PFC MOSFET Q1 (500 V/div) and the gated Vcc bias to the PFC stage that is controlled from the 5 V Standby output. The plot to the left is a longer timeframe view and shows the power supply trying to restart from Standby. As illustrated, after the first fault event is detected, the PFC is never restarted as the PFC Vcc will not rise up to the Vcc start level thanks to the coupling of the transformer.

1 s/div   10 ms/div
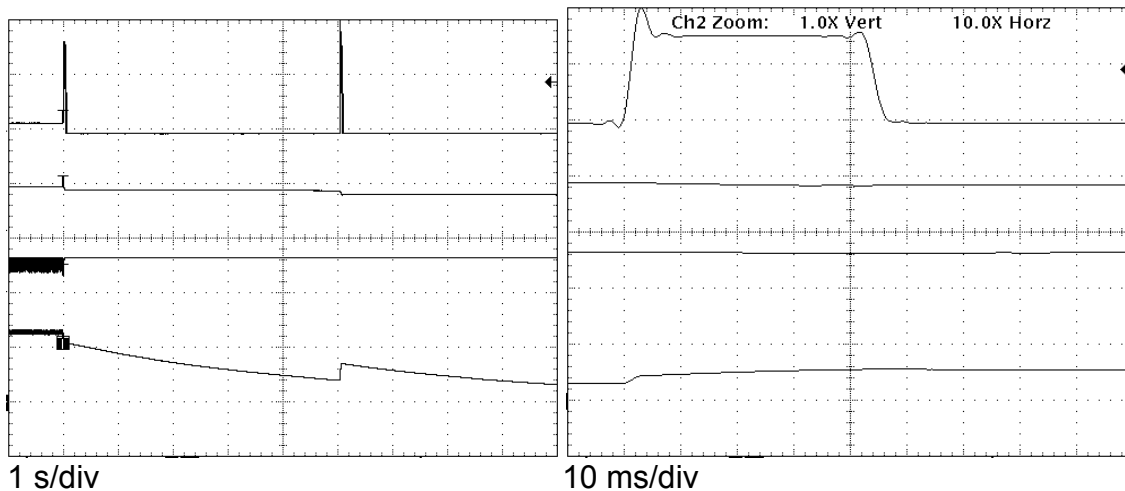
Figure 27: PFC behavior with + 12 V or + 5 V Output short circuit

D) Over Voltage Protection Operation

The following test illustrates how the system protection operates if the regulation fails open. The first section illustrates the protection operation in the event that the fault occurs after the power supply has starting (in ON mode) and operating under normal conditions. When the regulation loop is opened in ON mode, the output voltages rise up.   After 1.5 ms, the 5 V Standby reaches 7 V (typ) and the secondary Over Voltage Protection switches the system into Standby to protect the overall signal processing and the audio amplifier and speed up the primary OVP:

This effect of this is demonstrated in Figure 28a and 28b.

- Both the 12 V and 5 V output start falling
- Both VS1 and VS2 rise as the load is removed
- The Vcc of the PFC decays after the "ON/OFF" optocoupler switches OFF
- After an ~ 2 ms, the primary Over Voltage Protection is activated and the NCP1351 controller immediately switches OFF the Power MOS

For figures 28a, the signals illustrated in the plots (top to bottom) are as follows:

- VS2 (+12 V before switch Q114)   – 10 V/div
- +12 V   – 10 V/div
- +5 V   – 5 V/div
- VS1 (+5 V before switch Q113)   – 5 V/div

100 ms/div   2 ms/div (expanded scale)
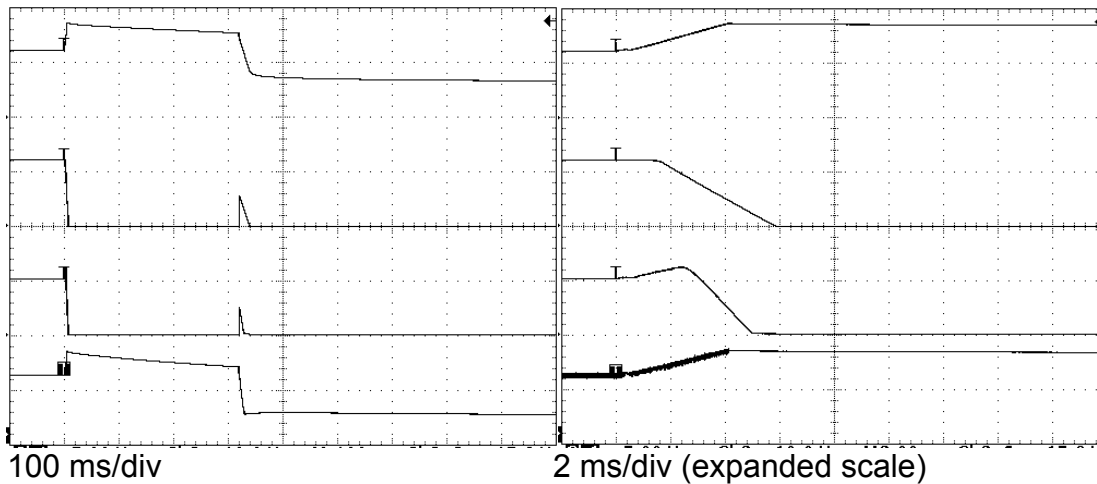
Figure 28a: Output voltage behavior for OVP event (Open regulation loop)

For figures 28b, the signals illustrated in the plots (top to bottom) are as follows:

- VS2 (+12 V before switch Q114)   – 10 V/div
- Vcc PFC   – 10 V/div
- Vcc Flyback   – 5 V/div
- Drain of Flyback MOSFET(Q106)   – 500 V/div

100 ms/div   2 ms/div (expanded scale)
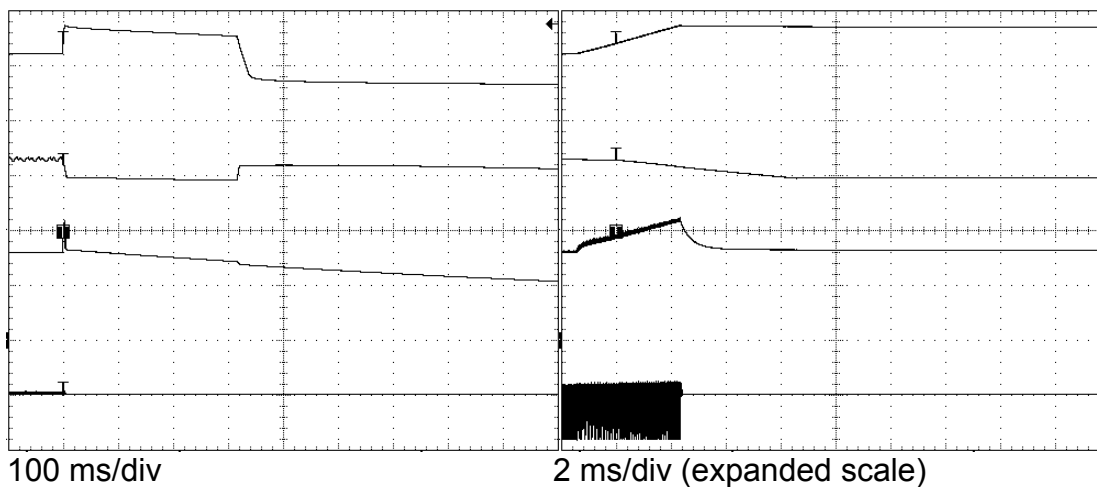
Figure 28b: Output voltage of Vcc for OVP event (Open regulation loop)

The other case occurs if the feedback loop is open at startup. In this scenario both output voltages will rise up. After ~ 7 ms (reference is now the starting point), the 5 V Standby reaches 7 V dc (typ) and the secondary Over Voltage Protection switches the system into Standby:

- Both 12 V and 5 V output are going down (additional delay for the 5 V "supply" a longer time by the 12 V),

- Both VS1 and VS2 go up as the output power has been reduced
- The Vcc of the PFC is not going up as the "ON/OFF" optocoupler has been switched OFF before the PFC has been able to turn on normally
- After an additional ~ 4 ms, the primary Over Voltage Protection is activated and the NCP1351 controller immediately switches OFF the Power MOS

Note, as seen in Figure 29, the time is longer than for the "ON" mode test above. This is due to the time required to charge the primary Vcc capacitors. As a result, the secondary rectified voltage reach a higher level before the system stops (Up to 19 V dc for VS2 and 9 V dc for VS1).

2 ms/div
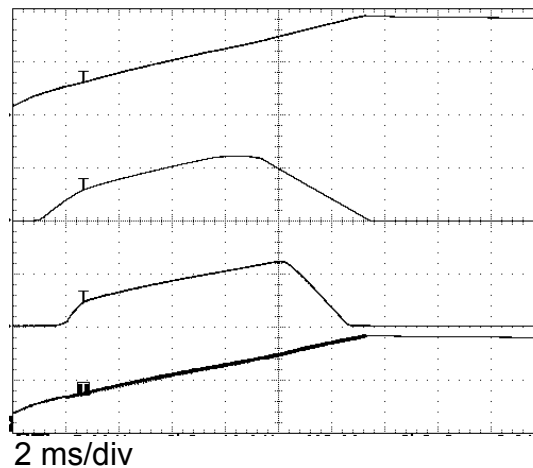
Figure 29a: PFC behavior for OVP event (Same signals as Fig 28a)

2 ms/div
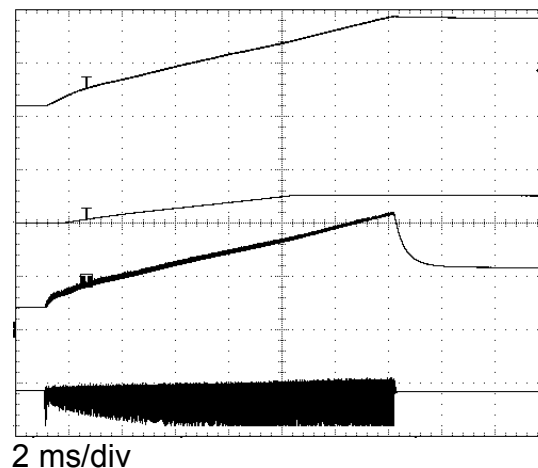
Figure 29b: PFC behavior for OVP event (Same signals as Fig 28b)

Regardless of the source of the over voltage protection fault, when this is detected the NCP1351 enters a latched state. To exit this fault, the primary AC

power has to be removed resulting in a "mains reset". This provides a very robust safety mechanism.

High Voltage Backlight Inverter

The high voltage inverter can be implemented using a half or full bridge topology. The decision on the topology is based on several considerations. With a half bridge topology, if it is operating in a fixed frequency - highly desirable in LCD-TV applications to avoid interference between the backlight and video signal - hard switching of the MOSFET devices is inevitable which causes excessive loss in the MOSFETs and generates severe EMI that must be dealt with to comply with regulatory requirements.
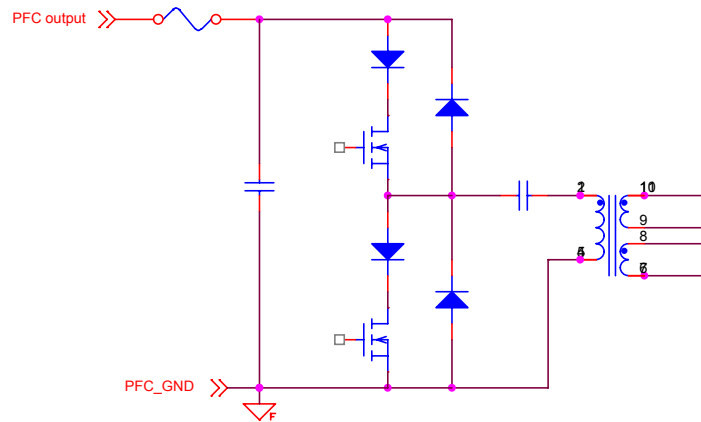
Figure 30: Example of Half Bridge Inverter Power Stage

In addition to the high switching losses of the power MOSFETs, 4 additional ultrafast diodes have to be incorporated to eliminate possible switching oscillation and avoid the risk of cross conduction due to the large stored magnetic energy and poor reverse recovery behavior of the MOSFET body diodes. To avoid these disadvantages a full bridge topology is employed for the backlight inverter power stage. This offers numerous advantages compared to the half bridge:

- Zero Voltage Switching with fixed operating frequency
- Reduced EMI and power losses
- Reduced MOSFET switching stress and heat dissipation
- Improved lamp current form factor (much closer to sinusoidal waveform)
- No need for additional power diodes across the bridge
- Half the current in the MOSFETs and transformer
- Easier to implement primary side Over Current Protection
- Similar cost thanks to the elimination of the fast recovery diodes and reduced heat sinking.

Moreover because the controller is operating at a fixed frequency, it is possible to synchronize the switching frequency to the video frequency and avoid any possibility of the backlight subsystem interference interacting with the video image.

Microsemi LX6503 backlight controller

The LX6503 is a high performance CCFL controller intended for LCD-TV and other multi-lamp LCD display systems. It is particularly optimized to be a cost effective solution for the High Voltage Inverter architecture. The controller provides a pair of push-pull PWM drive signals with sufficient capacity to drive a push-pull, half bridge or full bridge CCFL inverter with the addition of simple external circuit. An on-chip regulator supplies both the operating voltage for the output gate drive and bias to the internal control circuitry. This allows direct connection of the controller to the system supply - up to 27 V without an external regulator. In addition the controller offers a versatile synchronization capability that allows the user to synchronize both the frequency and phase of the lamp current to an external signal coming from the video processor (or other controller).

The lamp current regulation circuit comprises a simple and robust control loop design with excellent regulation accuracy and dynamic response at transient conditions. Furthermore a soft-start feature provides more reliable lamp strike and allows effective control of the possible inverter start-up surge current and lamp current/voltage overshoot. Lamp dimming operation is also well architected to facilitate convenient and flexible digital or analog dimming control with synchronization capability. In addition, reliable fault detection and protection functions are facilitated including open lamp protection, over voltage, short circuit and over current protection. Programmable strike and protection timing and fault indication are also incorporated to provide robust operation. The device is housed in a wide body SOIC-16 surface mount package.
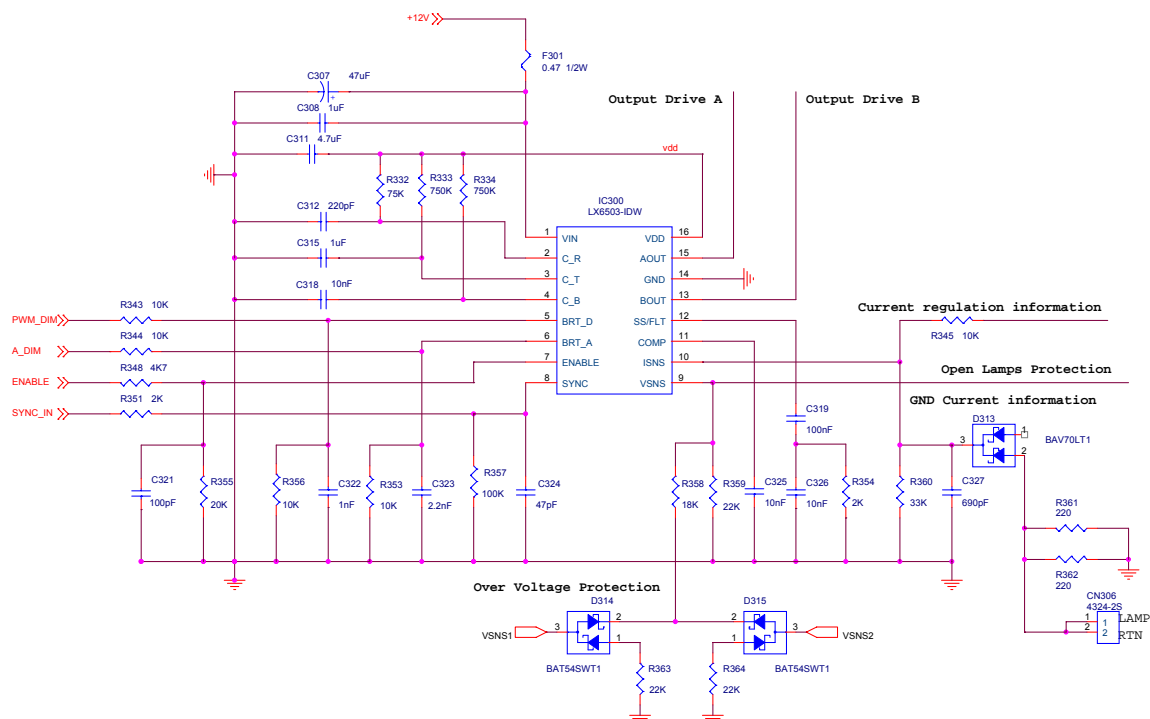
Figure 31: LX6503 Schematic and Control Signals

A typical application circuit is illustrated in Figure 31. A built in regulator is connected to pin 1 (VIN) to step down the input voltage to the internal operating voltage VDD (pin 16). The VIN of the device can range from 6 to 27 V dc. In this application, the VIN is directly supply from the +12 V dc through fuse resistor F301 to protect the system in the event of a short circuit. C307 and C308 provide low impedance filtering. VDD supplies both output gate drivers and the internal control circuitry. The nominal operating voltage of VDD is 5.25 +/- 0.25V. Internal UVLO function is provided to protect the system from under voltage operation. An external low ESR capacitor C311 with lowest possible trace impedance to VDD and GND pin provides good noise decoupling for the internal circuitry. The main operating signals are described as following:

- The operating frequency of the inverter is defined by the RC components connected to the C-R (pin 2). A saw tooth oscillating waveform with 2.5 V peak and 0.5 V valley is generated at this pin by the internal oscillator.

- The lamp strike time and fault timing are programmable based on the components connected to C_T (pin 3). A 5 µA charging current source is connected to this pin internally from VDD.

- Digital dimming can be controlled directly by a PWM signal applied on the BRT_D (pin 5). Alternatively, a DC control signal ranging from 0.5 - 2.5 V can also set the dimming duty from 0 to 100% with the frequency defined by the capacitor on C_B (pin 4).

- In addition, brightness can also be controlled by an analog dimming input on BRT_A (pin 6). A DC voltage from 0.5 - 1.5 V sets the lamp current from zero to maximum.

- ENABLE (pin 7) controls the on/off operation of the inverter. The voltage range from 2 - 4 V also sets the strike frequency of the inverter.

- SYNC (pin 8) allows frequency synchronization with another backlight controller in the system or to the video scanning clock signal to eliminate possible frequency related interference.

- VSNS (pin 9) is voltage sense input for voltage regulation and over voltage protection.

- ISNS (pin 10) is current sense input for lamp current regulation and open lamp, over current detection.

- COMP (pin 11) is the output of the error amplifier. The error amplifier is a voltage controlled current source (GM) type which can normally provide robust regulation control with simple compensation.

- SS/FLT (pin 12) serves the function of soft start, strike frequency ramp and low pass filter function for the synchronization control. During strike mode the ramp signal of this pin controls the soft start of the inverter and the strike frequency sweeping. When synchronization is operating in run mode, the capacitor at this pin provides a low pass filter function for the synchronization loop.

- AOUT (pin 15) and BOUT (pin 13) are the gate driver outputs with source and sink current capability of 0.6 A.

Fixed frequency zero voltage switching Full Bridge
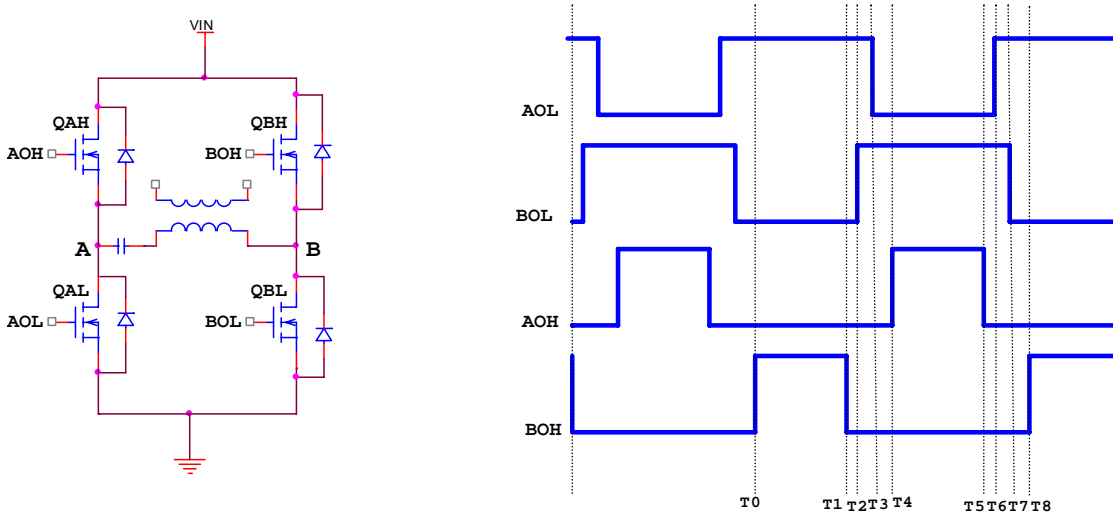
Figure 32: Operating Waveform of Full Bridge
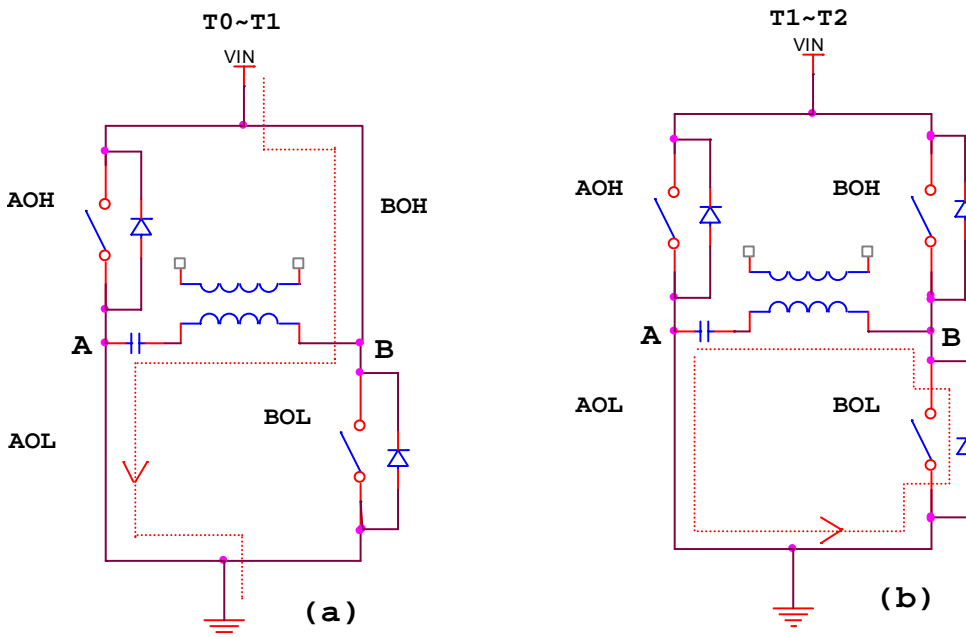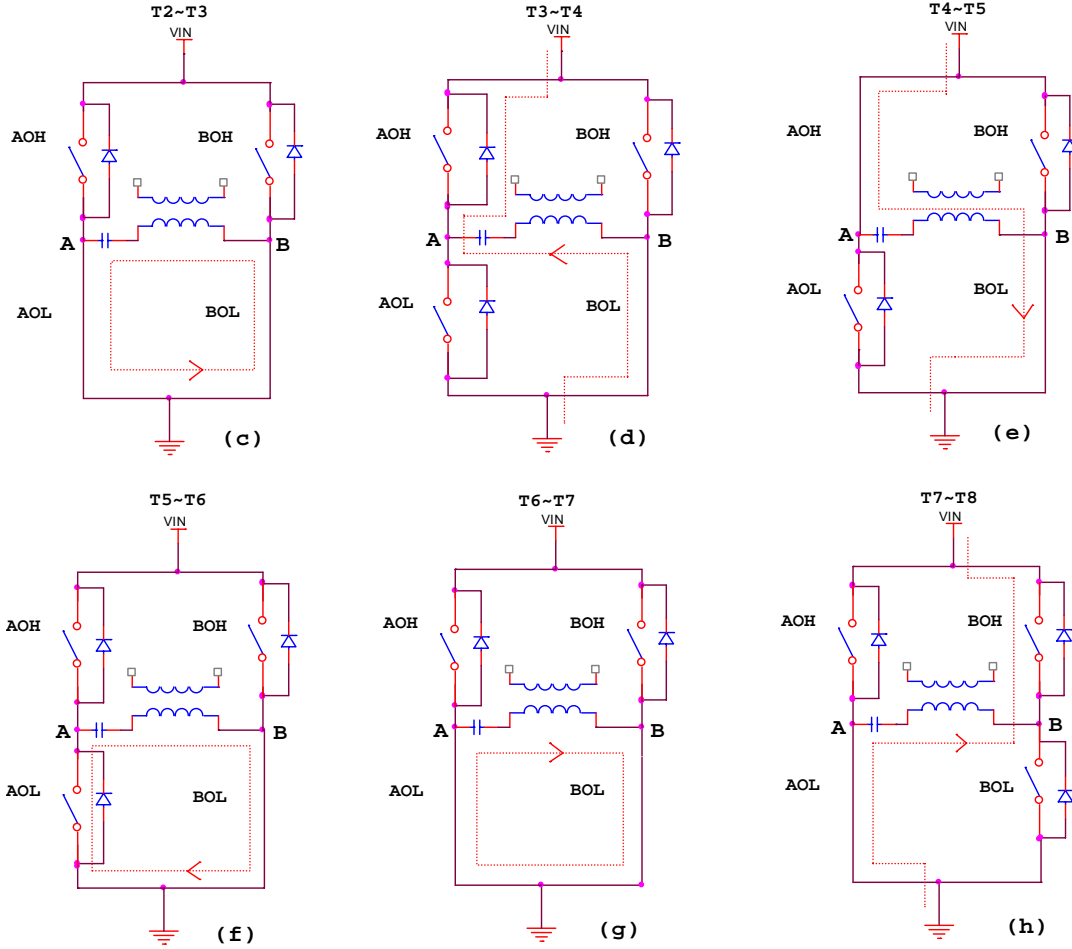
Figure 33: Operating State Of Full Bridge

Figure 32 shows a full bridge circuit and the gate drive waveform on the 4 MOSFETs derived from the LX6503 controller. One important feature should be noted is that the drive signals of high side and low side power switches of the same bridge arm, i.e. AOH, AOL or BOH, BOL, are complementary to each other by neglecting the dead time. With such a feature the stored magnetic energy in the transformer primary winding can be used to push the switching node to the opposite DC rail when a device is turned off, which essentially creates a zero voltage condition across the counterpart device to be turned on next. If the stored magnetic energy is large enough to sustain such condition till the end of the dead time when the counterpart device is turned on, a zero voltage switching operation will be successfully obtained. The detailed operation is described as follows:

Starting from the period from T0 to T1 as indicated in Figure 32, drive signals BOH and AOL turns the diagonal devices QBH and QAL on and the transformer primary winding current flows in the direction as indicated in Figure 33a. At T1 QBH is turned off by BOH and the magnetic energy stored in the leakage inductance and transformer magnetization charges up the body capacitance of

QBH and discharges the body capacitance of QBL, and eventually pushes the switching node B below the ground level. Once this transition is complete the body diode of QBL becomes forward biased to clamp node B near ground level and the current start circulating between QAL and the body diode of QBL as indicated in Figure 33b. During this period the decay of the circulating current is minimal because the rate of decay is inversely proportional to the voltage across the transformer winding which is mainly the body diode forward drop.

It should be noted that it is not granted that the potential of switching node B can always be pushed below ground level. If the stored magnetic energy is not large enough to fully charge/discharge the body capacitance of QBH and QBL, switching node B cannot be pushed below ground level and it will start oscillating and eventually settle at the mid point level of the DC input. It should also be noted that the time for the switching node B to swing to ground level is dependent on the value of the MOSFET body capacitance, the transformer leakage inductance, and the amplitude of the current at T1 instant. Higher current level and LC value will result in a shorter swing time.

After the dead time T2-T1, QBL is turned on by BOL and the primary current continues to circulate through QAL and QBL if it is not yet extinguished, as shown in Figure 28c. Such condition remains through out the period between T2 and T3 during which the voltage across the transformer primary winding is nearly zero. At the moment of T3, QAL is turned off by AOL and the circulating current starts to charge the body capacitance of QAL and discharge the body capacitance of QAH. If the remaining energy is sufficient to complete the charge /discharge it will eventually push the switching node A above the positive DC rail VIN and force the body diode of QAH to conduct. Node A will then be clamped at near VIN level and the circulating current will continue to flow through the new path of QAH body diode, DC input source, and QBL. Here it should be particularly noted that during this period from T3 to T4 the decay of the circulation current is much faster because the voltage across the transformer primary winding has to rise to slightly higher than the DC input voltage in order to maintain the continuous inductive current flow. If the remaining magnetic energy is large enough to maintain the forward bias of QAH body diode and keep the continuous current circulation till AOH goes high, a successful soft switching is obtained to turn on QAH at zero voltage condition. If the remaining magnetic energy is not large enough, however, it may enter the situation that the circulation current extinguishes before full charge/discharge of the MOSFET body capacitance and the switching node A will not be able to swing up to VIN level, or after node A swings above VIN the circulation current extinguishes before AOH comes on and the potential of node A swings back down. Under either circumstance a zero voltage condition across QAH cannot be obtained to realize a soft switching operation.

The above situation is more likely at light load under narrow PWM duty cycle, and low transformer leakage inductance conditions, which generally results in

less stored magnetic energy. Another important factor to successful soft switching is the dead time setting. If the dead time is too long, the inductive circulation current cannot hold its continuity before AOH comes on and hence decay to zero before QAH is turned on. As such the dead time should have an upper limit. On the other hand, when a power switch is turned off, like QBH at T1 and QAL at T3, it takes a certain time for the switching node potential to swing to the opposite DC rail. The swing time could have a wide range with different designs depending on the values of the transformer primary leakage inductance, the MOSFET body capacitance, and transformer primary current level etc. Theoretically the switching node potential swing is part of the resonance cycle at the switching transition. The frequency of the resonance is determined by the transformer primary leakage inductance, the MOSFET body capacitance and other minor parasitic parameters, and the theoretical free resonance peak voltage (Here the free resonance peak means the peak voltage value at the ¼ resonance cycle point if there is no clamping to the DC rail by the MOSFET body diode) which is determined by the L, C, R parameters of the resonance tank and the transformer primary current level. Higher resonance frequency and higher free resonance peak voltage will result in shorter time for the switching node to swing to the opposite DC rail and vise versa. From this point the dead time also needs to be long enough to allow full swing of the switching node potential under a wide range of operating conditions. If the dead time is too short it may enter the situation that the power MOS is turned on before its V_{DS} is pushed to zero by the switching node swing and thus soft switching cannot be realized. Taking account of the above points, a reasonable dead time range for practical CCFL inverter applications lies in the range of about 130 to 400 ns.

In actual application designs as indicated above under specific light load conditions, zero voltage switching might not occur. Under such circumstances, measures have to be taken in the design to ensure successful soft switching operation. One approach is to increase the transformer magnetizing current or the primary leakage inductance. This will increase the stored magnetic energy to maintain the continuity of the inductive current during dead time. Another approach is to increase or decrease the effective dead time of the power switches externally to get the desired switching control timing according to the particular inverter power circuit parameters.

At T4, QAH is turned on by AOH. If the current flowing in the direction as shown in Figure 33d has not decayed to zero at this moment, it will keep flowing until it decays to zero and then reverse the direction as shown in Figure 33e. The following events evolve as shown in Figure 33f,g,h and so on continues the switching operation of the next commutation process that essentially repeats the same transitions as described above.

A typical set of actual waveforms of AOL, BOL, AOH and BOH from the reference design is shown in figures 34-38.

Yellow-AOL; Blue-BOL; Purple-AOH; Green-BOH
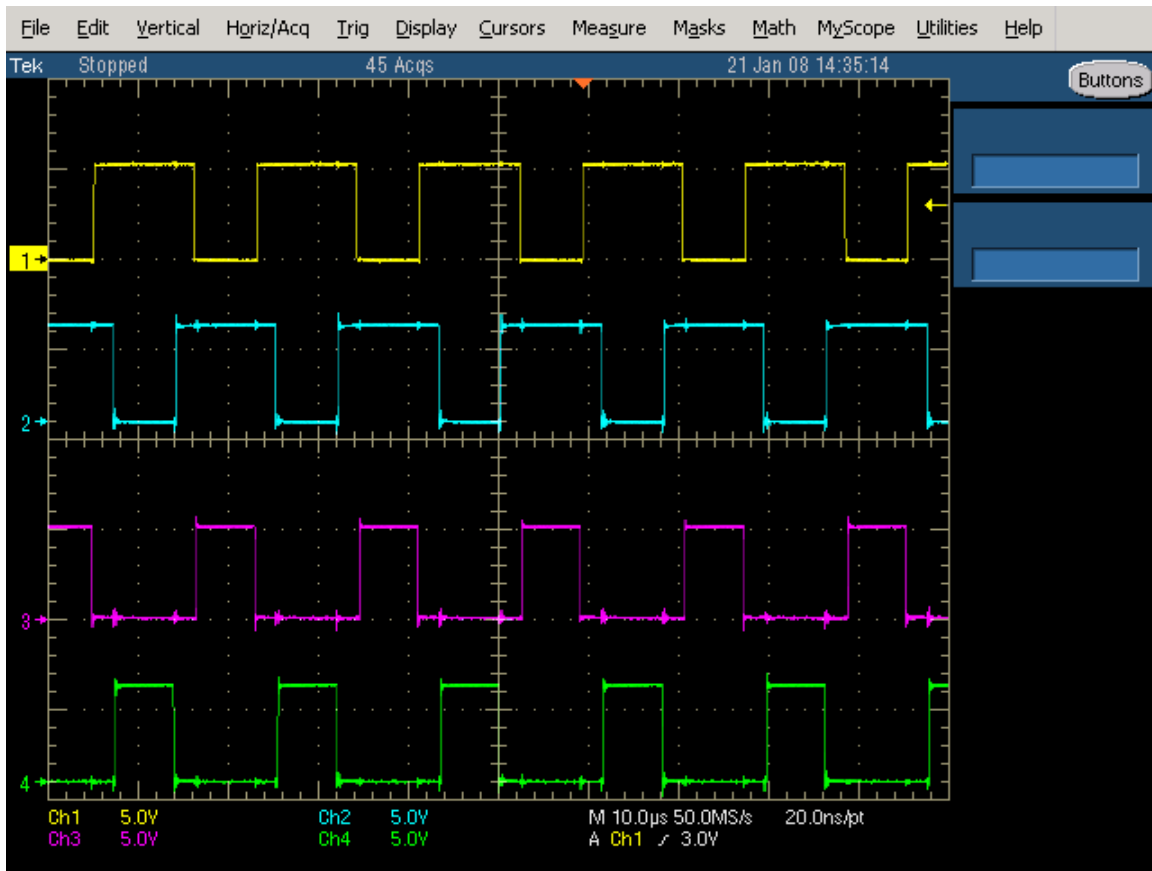
Figure 34: Gate Drive output waveforms

Figure 35: Dead time between AOL (yellow) and AOH (purple): 280 ns
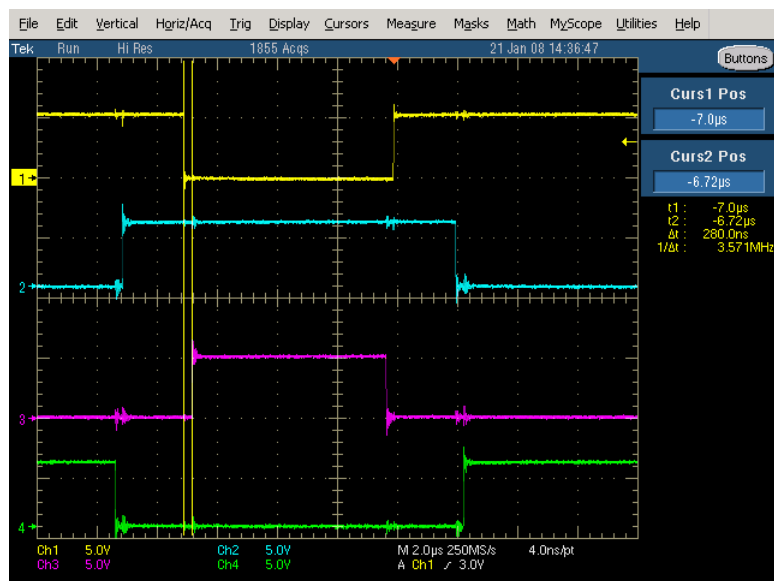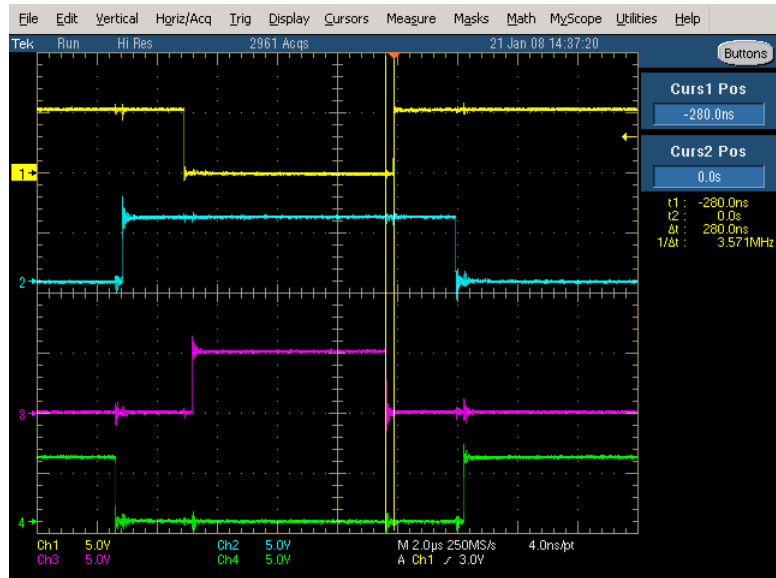
Figure 36: Dead time between AOL (yellow) and AOH (purple): 280 ns
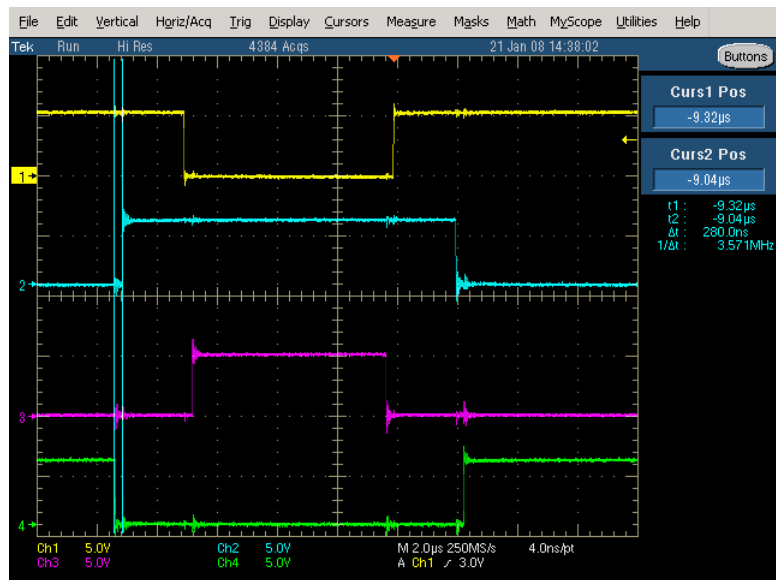
Figure 37: Dead time between BOL (blue) and BOH (green): 280 ns
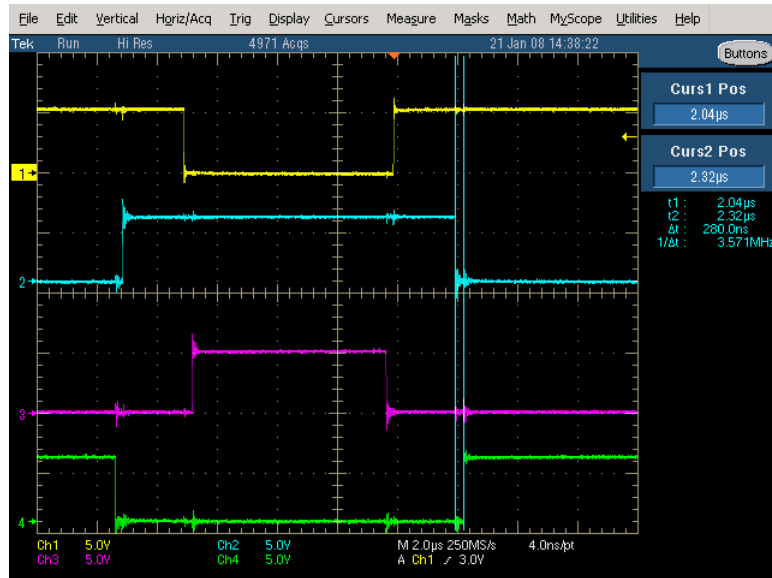
Figure 38**: Dead time between BOL (blue) and BOH (green): 280 ns**

Full Bridge Driver Circuit Description

In a HV-LIPS configuration, the power MOSFETs for the full bridge are located on the primary side and the inverter controller is located on the secondary side across the isolation boundary. The output drive signals employ a push-pull signal format to drive two isolation transformers for the full bridge. The isolation transformer provides two isolation functions: the safety isolation between the primary and secondary, and isolation between the high side and low side MOSFET. Therefore the output signals from the drive transformer can be coupled to the power MOSFETs without the need of level shift function. The remaining function for soft switching full bridge drive is the dead time insertion. Figure 39 illustrates the drive circuit of one arm of the full bridge that incorporates the dead time function.

Figure 39: Full Bridge Zero Voltage Switching Driver Circuit

Since winding 6-7 and 9-10 of T303 have the same phase, MOSFET Q302 is switched ON after the positive going edge from winding 6-7 with a delay time controlled by R318 and C316 together with the gate capacitance of Q302. In the meanwhile, the NMOS (bottom) of driver M300 is switched ON immediately by the positive going edge from winding 9-10 and thus turning OFF MOSFET Q300 quickly. During this time, C300 is also charged to replenish energy for the drive circuit of Q300.

When the voltage of both windings drops to zero, the NMOS driver Q304 comes on to quickly turn off MOSFET Q302: this is done without delay as the discharge loop is a low impedance path. Simultaneously, the NMOS of driver M300 is switched OFF (without delay) while the PMOS of M300 is switched ON with a delay defined by R303 and the input capacitor of its gate.

In such an operating manner the switching OFF of the Power MOSFETs Q300 and Q302 is fast and without any deliberate delay while the switching ON of Q300 and Q302 always has delay. The result is a controlled dead time which prevents shoot through and facilitate zero voltage switching operation of the power switches. With zero voltage switching of the full bridge operation, there is no reverse recovery process for the body diode. Therefore ultra fast Power MOSFETs or external fast recovery diodes are not required. Another advantage of full bridge is that the current of the power MOSFETs and transformer primary winding is half of the half bridge. In the reference design, STD3NK500ZT4 500 MOSFETS are used which are rated at 3 A with an RDS_{ON} of less than 3.3R at

2.3 A. In a half bridge design MOSFETs of RDS$_{ON}$ of 1.65R would have to be used to obtain similar conduction loss. Moreover, due to the low switching losses in this implementation, surface mount DPAK packaging can be used without additional heat sinks.

Full Bridge Zero Voltage Switching Waveforms

For figures 40-43, the top waveform is the current in the primary of the transformer (1 A/div) and the bottom two waveforms are the voltage on bout sides of the HV Transformer (500 V/div).

1 ms/div
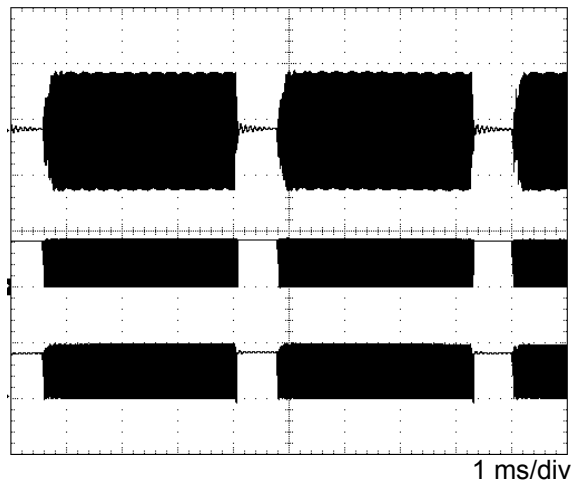
Figure 40: 285 Hz Burst

20 µs/div
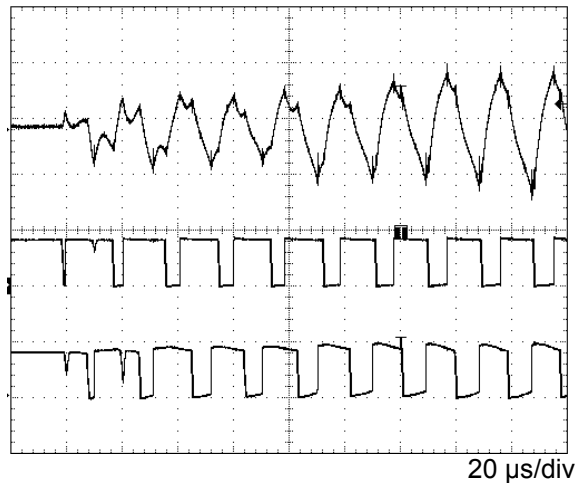
Figure 41: Burst mode soft-start

4 µs/div
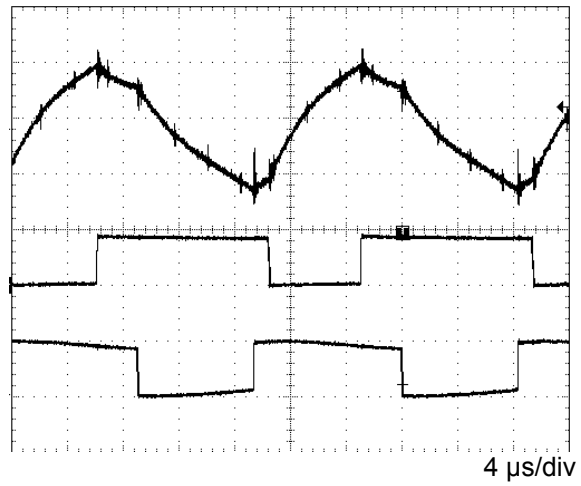
Figure 42: Standard Inverter Drive Cycle (52 kHz)

Ch1 Zoom: 1.0X Vert   0.5X Horz

20 µs/div
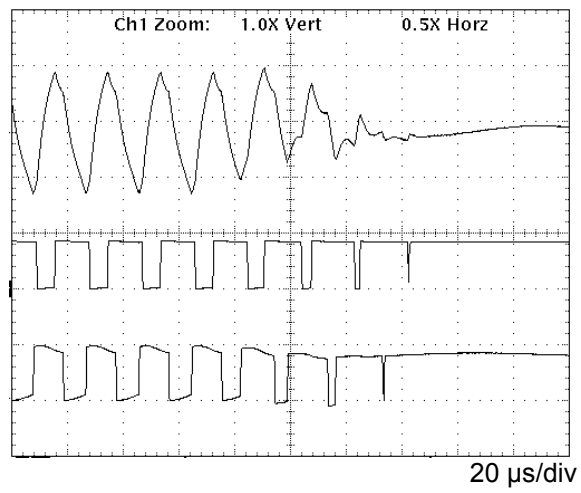
Figure 43: Burst mode soft-stop

High Voltage (HV) Transformer

The HV transformer provides two voltages in the opposite phase (+ and -) to supply the lamps. With such outputs the voltages to the lamps is interleaved in a way that the adjacent lamps are always connected to opposite voltages. Such wiring arrangement will result in the smallest and localized HV electric field and thus minimizes the interference to the LCD panel. In addition, such a configuration can also drive U-shape lamps which will further reduce the overall backlight system cost. In fact, dual phase voltage is the most common approach on the market, and this transformer design offers very competitive cost compared with two transformers or multi-transformer approach.

The high voltage transformer is designed to work in the frequency range of about 40 kHz to 80 kHz with a primary inductance of around 1.8 mH. It is build on a UP34 core and is capable of providing up to 120 W output, which is more than the power requirement of most 32" applications (about 95 W). So it would also be able to drive a 37" without any problem and possibly up to 42" in future while the efficiency of the CCFL backlight systems continually improve and the power consumption reduce further.

The turn ratio has been optimized to get the required voltage / power for the lamps with the target duty cycle. In actual applications, the inverter will operate at higher duty cycle with smaller turns ratio which normally results in better lamp current waveform and better inverter efficiency. But with the reduced headroom of the output voltage there would a chance that the maximum output voltage is not enough to ignite the lamps during strike operation. On the other hand, larger turns ration provides more strike headroom but the inverter efficiency and lamp current form factor will suffer. In this reference design a balancer network has been employed to balance the lamp current. The balancer network has an intrinsic mechanism to help lamp strike. In this sense it allows to use smaller turns ratio for the transformer to get better inverter efficiency and the lamp current waveform.

Basic Transformer Construction
- The turn ratio is 3.76 with 125 turns for the primary and 470 for each secondary with a primary inductance of 1.8 mH
- For reduced losses, the primary wire is a 0.10 mm x 16 while the secondary wire is single 0.15 mm
- To avoid isolation issues which could impact reliability, the secondary is split with a multi-slot bobbin construction with care to avoid crossing wires
- The leakage inductance from the secondary is 19.2 mH for each secondary winding with the primary shorted

The reference of the transformer is PIT 125050-3551 GP and is available from Taipei Multipower Products (TMP) in Taiwan.
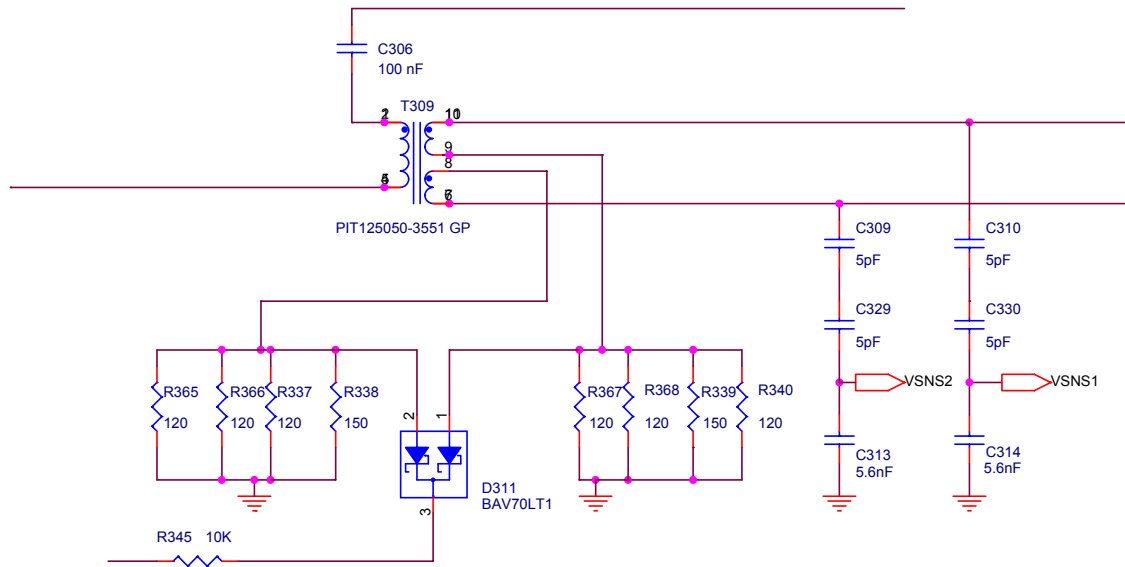
Figure 44: Schematic for both current and voltage sensing

The current and voltage sensing from the transformer is illustrated in Fig. 39. The resistor banks of R355, R366, R337, R338 and R367, R368, R339, R340 at the secondary winding return terminals convert the transformer current to voltage signals. It essentially forms a full wave rectification circuit in combination with D311 to obtain the current sense information of both positive and negative cycles. The transformer output voltage is sensed by the two capacitor divider strings connected to the two HV output terminals. The voltage sense signal from VSNS1 and VSNS2 are fed to the VSNS pin of the controller after rectification. This information is used for voltage regulation as well as over voltage protection.

CCFL Drive and Current Balancing

The specific characteristics of CCFL lamps require special techniques to drive them. The two most important functions required for successful CCFL operation are the lamps strike and lamp current balancing because of the following:

- The CCFL lamp requires a high voltage, normally about 1.5 to 2 times of its normal operating voltage to make the initial gas breakdown inside the lamp to start the normal operating cycle. This process is called strike (or kick off, ignition etc.). Further, because the lamp operating voltage is much lower than strike voltage, in multi-lamp parallel operation the voltage could be clamped by the first striked lamps and the remaining lamps may not be able to strike successfully.

- Due to the very low dynamic impedance characteristics of CCFL, the lamps will enter a "run away" situation, i.e. the current is concentrated to one or a few lamps with lower operating voltage and the other lamps have no current, when the lamps are put in parallel directly.

For to above reasons, lamp strike and current balancing have to be considered carefully in order to get a reliable operation of the backlight system. The Jin Balancer solution employed in this reference design can provide excellent lamp current balancing function and in the meanwhile guarantees reliable lamp strike in combination with the frequency sweeping strike technique. The Jin Balancer technique is based on the electro-magnetic coupling mechanism of the balancing transformer network that generates additional correction voltage to the lamps to equalize the lamp current. The basic configuration of the balancer network is shown in Figure 45. The serial loop of the balancer secondary windings equalizes the primary side current and provides coupling mechanism between the lamp circuits. With such coupling mechanism if a lamp is not stricken, the energy from the stricken lamps will be automatically coupled to the balancer primary winding of the un-stricken lamp circuit to increase the voltage across the lamp and help it to strike. As can be seen from Figure 45 the wiring configuration of the balancer network is uniform regardless the number of lamps. In addition, one type of balancer transformer can fit with almost all the lamp sizes. These features make the Jin balancer solution very flexible in CCFL inverter applications. Apart from the balancing function, the signal from the secondary winding loop can also be used to detect open lamp condition. When a lamp is open, the voltages in the primary and secondary winding of the corresponding balancer rise sharply, because of the significant increase of the magnetic flux in the balancer core due to the disappearance of the primary current. With such an indicator, open lamp detection can be easily accomplished by monitoring the voltage signal from the balancer secondary. Because the primary and secondary winding of the balancer are electrically isolated, the detection function can be easily implemented with low voltage, low cost components in all types of lamp configuration regardless whether the balancers are placed at low voltage or high voltage side of the lamp, or whether the lamps are driven from single side or differentially. Another advantage of this solution is that the lamp current balancing is largely governed by the balancer turns ratio but not the absolute value of the winding inductance. Therefore the solution is insensitive to manufacturing tolerances such as differences in core assembly, or parameter changes during operation such as inductance change with temperature etc.
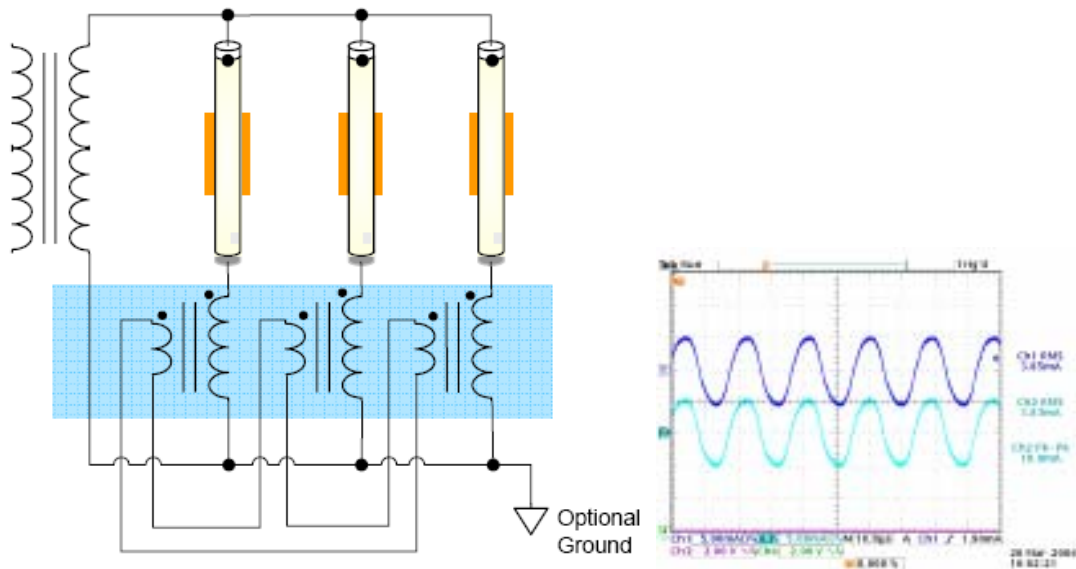
Figure 45: JIN balance Approach

As illustrated in figure 45, each balancer transformer has 2 windings:

- a "primary" winding connected in series with the lamp and
- a "secondary" winding connected in series with all other secondary windings as a closed loop.

The general requirements for the current balancing transformer are listed below. In this specific 32" HV-LIPS application a single PCB is used to house the whole power circuitry including power supply, inverter, and balancer network. As such the balancer transformers uses a through-hole configuration to fit the assembly process. If the design is to be scaled up to a larger panel size, the balancer board might be separated from the main power board. In that case the balancer transformers would be configured in an alternative surface mount packaging.

- Core EFD1215
- Primary: 39 µH +- 30%
- Secondary (high voltage in series with the lamp): 625 mH +/-30%
- Turns ratio: 1/125
- Isolation: winding to core > 1.5 kV, winding to winding > 2.5 kV
- Size: 20.9 x 13.3 x 7.8 mm
- Through hole
- The reference of the balancer transformer is PBT-07087-1322 GP from TMP Taiwan

The below schematic illustrates how the balancer and sensing circuitry are configured to drive four lamps. The resistor divider network from the balancer secondary winding provides the monitor information for open lamp detection. The analog signals from the divider network are OR'ed by the diode D302 and

D305 and fed to the controller to monitor the lamp status during both the strike and run operations.
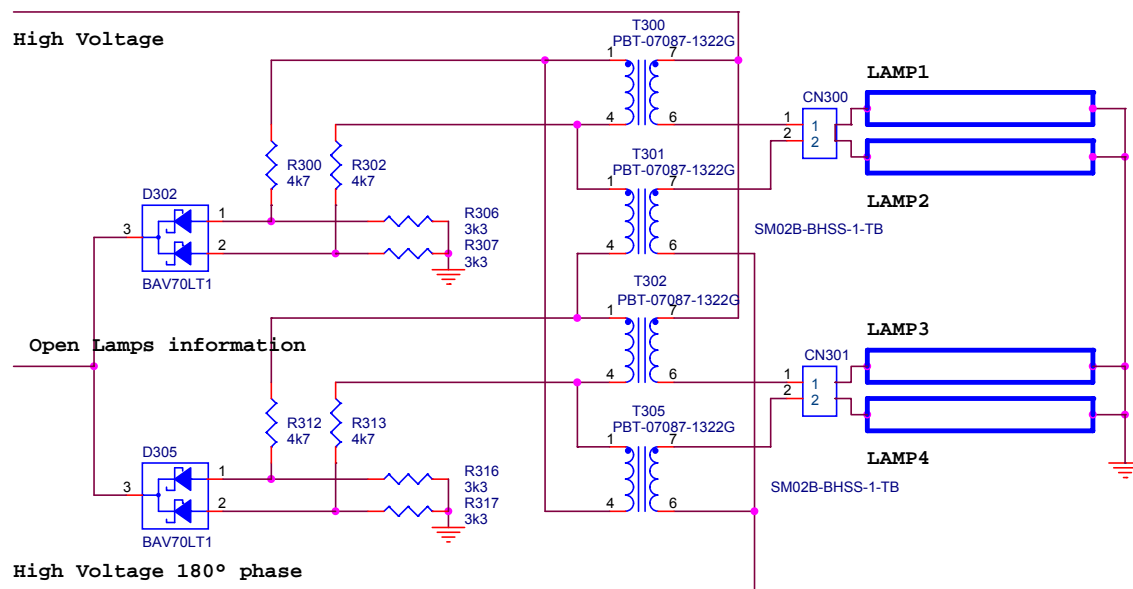
Figure 46: Configuration of Balancer and Open Lamp Monitor

A classic approach for a 32" backlight subsystem is described below.

- 12 single lamps
- All lamps are connected together to a common ground
- The current sense for the system in on the ground wire
- All lamps are driven "in phase" from a single output high voltage transformer

The GreenPoint design has been developed to take advantage of the evolution of lamp configurations and improve the overall system performance and flexibility.

- Provide 2 interleaved + and – phase output to minimize the field interference to the panel, since adjacent lamps are driven with opposite phase voltage and the high voltage field is largely localized.
- Provide 2 interleaved + and – phase output to allow for U shape lamp applications with a virtual ground on the other side of the screen
- Employ current sensing for overall lamp current regulation on the high voltage transformer side instead of the "ground" side of the lamp.

Figure 47 illustrates a U shape lamp solution that cuts the number of current balancers in half. Moreover it is important to see that this approach could be use for 2 straight lamps connected together in an equivalent U lamp like arrangement

(pseudo U-Shape). This only requires minor panel configuration changes to change the lamp connection on the other side of the panel.
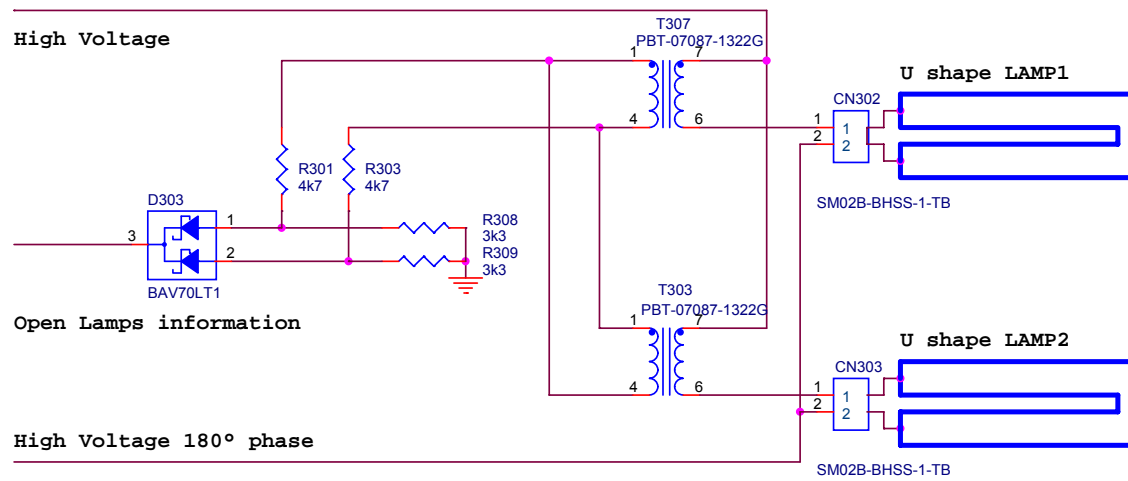
Figure 47: HV-LIPS current balancing for U shape lamps

Overall Efficiency Performance

The focus of the reference design was to provide excellent parametric performance coupled with a high efficiency architecture that operated all the power conversion stages in a low loss manner. Some typical performance data is described in the following table where the flyback and PFC stage were loaded at various test load conditions. The inverter efficiency has been estimated because precise output power measurement directly on the high voltage lamps is difficult and not accurate enough. The PFC efficiency is > 95% over full range of line input at typical load condition and the peak efficiency of the flyback converter under a typical load configuration of 37 W is 78%. This is quite good considering that there are some additional losses in both 5 V and 12 V output based on the cross regulation technique that was used to assure tight regulation accuracy for the 5V and 12 V rails. The efficiency of the inverter is optimized thanks to the full bridge zero voltage switching topology that minimizes the switching losses. A testimony of this is the fact that the full bridge MOSFETs uses surface mount DPAK device and does not require any additional heat sinking.

FLYBACK				INVERTER	PFC				Complete board
Output V x I	Pout	Pin	η	Pin	Pout	Pin		η	Total η *
12,25 x 0,3	12.6	17	74%	100.8	117.8	230V => 120.7		98%	89%
4,97 x 1,8						110V => 123		96%	87%
12.20 x 2	36.8	46.9	78%	100.8	147.7	230V => 150.8		98%	87%
4.94 x 2.5						110V => 154.3		96%	85%
11.94 x 4	60.1	78.2	77%	100.8	179	230V => 182.6		98%	85%
4.95 x 2.5						110V => 188		95%	82%
*									
Total η = (P out Flyback + 94 % Pin inverter) / Pin PFC									
Inverter η is estimated to be 94% (Ouput power on lamps is very difficult to mesure).									

Summary

This complete GreenPoint reference design supports the emerging High Voltage LIPS architecture which powers the inverter directly from the PFC stage thus eliminating a complete power stage. Moreover due to the high efficiency proprietary architecture of the NCP1351 flyback controller, the need and expense associated with a dedicated standby supply is eliminated thus further simplify the solution. The architecture illustrated in this reference design has a high degree of flexibility to support a variety of voltage/current configurations with minor changes to the schematic and components used. Finally thanks to the use of an advanced backlighting controller with a zero voltage switching full bridge topology, the inverter power can be easily scaled up to support a variety of LCD-TV sizes up to 42".

Authors: Jean-Paul Louvel and Bernie Weir

Appendix

The appendix consists of the following sections:

- Photographs of complete board
- Schematics of SMPS1
- Bill of Material of SMPS1
- Supporting Device Literature that is available
- Relevant Global Energy conservation standards
- Schematics of complete design supporting alternative power configurations
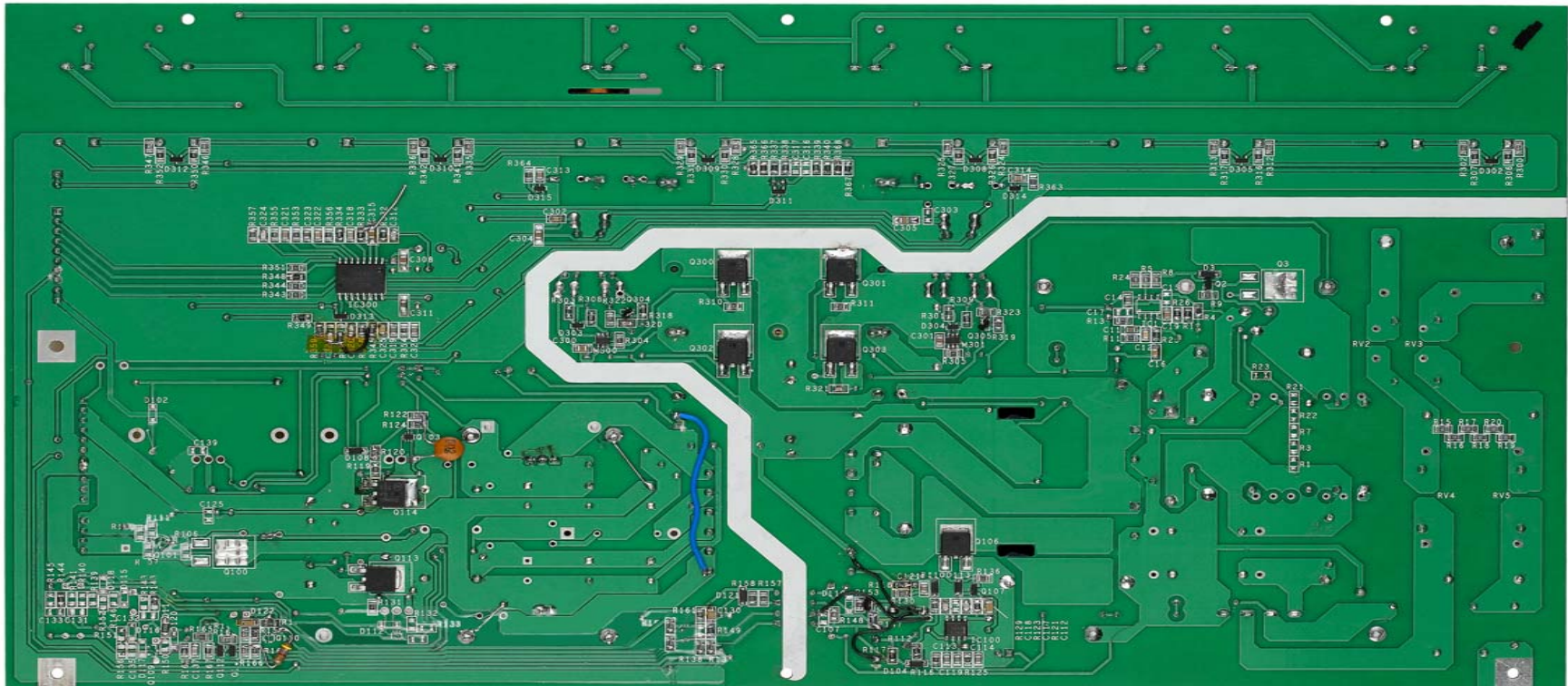
Bottom View of SMPS1
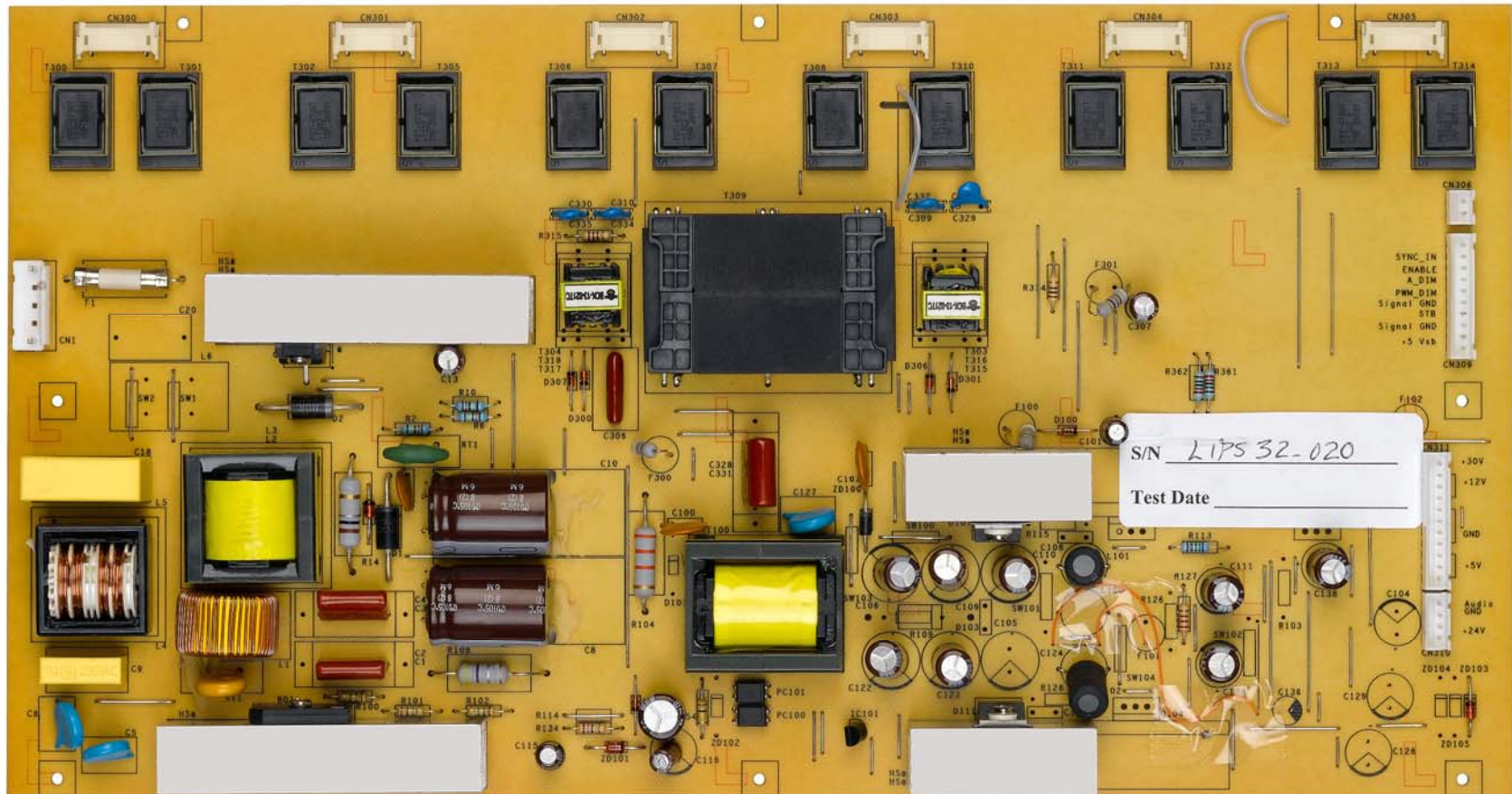
Top View of SMPS1

Schematics of SMPS1

The following four pages contain the schematics for the SMPS1 implementation (see Table 3) of the GreenPoint HV-LIPS design.

Schematic of Greenpoint Reference Board (SMPS1 Configuration)

BD1 GBU806

L1 150uH

D1 1N5406(DO-201)

D2 MUR550APF(DO-201)

RT1 NTC 2R5

PFC_OUT

C1 0.47uF 450V

C3 0.47uF 450V

R4 27K

L2 TF2815 - 150uH

RV1 TVR10471KSY

R2 1M3 1/4W

C7 10nF 630V

C8 68uF 450V

R24 68

R5 68

R8 68

Q1 STP11NK50ZFPN

D3 MMSD4148

Q2

R6 1M3 1/4W

C10 68uF 450V

C5 Y 1nF

C6 Y 1nF

IC1 NCP1606B

BC856ALT1(SOT23)

C11 100nF

R9 10K

R10 1M3 1/4W

C9 X2 100nF 275V

5 ZCD DRV 7

C12 390nF R11 56K

L5 CFS24 - 2mH

RV5 eclat

8 VCC Ctrl 2

RV4 eclat

3 CT FB 1

R12 220

C18 X2 1uF 275V

6 GND CS 4

R13 24K9

R14 0.10 2 W

ZD1 1N4733A 5.1V

C13 47uF

C14 100nF

R25 470

C16 1nF

R26 680

C19 220pF

PFC_GND

R15 150K R16 150K R17 150K

PFC_VCC

R18 150K R20 150K R19 150K

AC Line - For PWM start

J1 A

J2 A

F1 FUSE 4A 250V (Axial Lead)

CN1 4333-W05ST

Schematic for HV-LIPS Greenpoint Reference Board (SMPS1)

Schematic of Greenpoint Reference Board (SMPS1 Configuration)

Schematic for HV-LIPS Greenpoint Reference Board (SMPS1)

AC Line - For PWM start

PFC_OUT

PFC_GND

R100 1M 1/4W
R101 1M 1/4W
R102 1M 1/4W

R104 33K 2W
C100 10nF 250V
D101 MUR160

T100 ER28L

C103 10nF 250V
F100 0.47 1/2W
D100 BAV21
VS4
ZD100 1N5929B 15V
C101 10uF/50V
VS3

VCC1

R108 0.47R 2W

J103 A

J100 A

C106 1000uF/16V
VS2

R113 7.5K 1/4W

PC100B SFH817A
R114 0
R112 3K3
IC100 NCP1351B
FB Vcc 6
CT Timer 8
CS Latch 7
GND Drv 5

R116 100
D104 MMSD4148
R117 47
D105 BAV21
R118 10

D107 MBR20100CTG (TO220)
C109 1000uF/16V
C110 1000uF/16V

L101 10uH
Q114 NTD3055-094T4G DPAK
+12V
+12V

R119 10K
R120 20K
C111 330uF/16V

Vref
BC846BDW Q103 SOT363
C143 4.7nF
STB
R122 4K7
D108 MMSD4148

C112 470nF
R121 2K7
C113 100nF
C114 100nF
C115 10uF/50 V
C142 220uF/35 V
C116 10uF/35 V
ZD101 1N5929B 22V

R124 470
R127 2K2

J104
+5VSB
+5VSB*

C117 270pF
C118 100pF
C119 100nF
R125 1K

C138 330uF/16V

Q113 NTD14N03R DPAK
+5V
+5V

D110 MMSD4148
C121 270pF
R129 100k
R130 150k
OPP CKT

D111 MBR20100CTG (TO220)
C122 1000uF/16V
VS1
L102 10uH
R131 10K
C126 330uF/16V

C123 1000uF/16V

R170 1K
C140 22pF
R134 27
D113 MMSD4148
Q106 STD3NK60ZT4

C127 Y 1nF

R169 NI

Q107 BC856ALT1(SOT23)
R136 47k

R137 220

VS2
+5VSB*

PC100A SFH817A
R138 1K
R142 16K2
R144 6K19

Q108 BC846ALT1(SOT23)
R147 100
VCC1
R148 4K7
R149 0
C130 470nF

R153 10K
PC101B SFH817A
IC101 TL431ACLPRPG 1%(TO92)
Vref
R172 4K7

R154 100K
R155 2K49
R164 100K

PFC_VCC

PFC_GND

D124 0R
STB

+5VSB*
R157 1K
R158 2K2
R159 2K2
STANDBY

PC101A SFH817A
R161 100K
D121 MMSD4148
R163 4K7

6.3V VS1-OVP
ZD103 1N4733A 5V1 (DO-41)
+5VSB*

Q111 BC846ALT1(SOT23)
Q112 BC846ALT1(SOT23)
R165 470

R166 4K7
R167 470
R168 470
C137 10nF

Model Name	ON-MICRO-LIPS-32"	Revision	Pilot 3
Size	B	Date	2009.02.12
Engineer	Dale Tittensor	Reviewer	Jean-Paul Louvel
Subject	SMPS PCB	Sheet	2 of 4

ON SEMICONDUCTOR TWN S.E.C.

Schematic of Greenpoint Reference Board (SMPS1 Configuration)

CN311

4324-11S

1	+30V
2	+12V
3	+12V
4	+12V
5	
6	
7	
8	
9	+5V
10	+5V
11	+5V

CN309

4324-10S

10	+5VSB
9	+5VSB
8	
7	STB
6	
5	PWM_DIM
4	A_DIM
3	ENABLE
2	SYNC_IN
1	SYNC_OUT

Schematic for HV-LIPS Greenpoint Reference Board (SMPS1)

Schematic of Greenpoint Reference Board (SMPS1 Configuration)

Schematic for HV-LIPS Greenpoint Reference Board (SMPS1)

Note:
1. Input Voltage 400V.
2. Output 100W to 200W.
3. ENABLE active above 1.5V.
4. Analog dimming input (A_DIM) 1 to 4VDC, or equivalent PWM signal.
5. PWM dimming input (PWM_DIM) 1 to 4VDC, Controls duty cycle from 0 TO 100%, Above 4V goes into continuous operation.
6. T2 and T3 about EE15 size, 25:38+38.
7. T1 about 108:360

ON SEMICONDUCTOR TWN S.E.C.

Model Name	ON-MICRO-LIPS-32"	Revision	Pilot 3
Size	B	Date	2009.02.12
Engineer	Dale Tittensor	Reviewer	Jean-Paul Louvel
Subject	INVERTER PCB	Sheet	3 of 4

Bill of Materials of the HV-LIPS board (SMPS1 Version)

Designator	Component Type	Value	Rating	Package / Dimensions	Reference	Supplier
BD01	Bridge Rectifier	8A-600V	8A-600V		GBU806	Taiwan Semiconductor
BD01A	Screw			M3*8		
BD01B	Heat-sink			70 mm		YUAN FENG Industrial Co,LTD.
C001,C003	CFS	470 nF	450V	Radial 15mm	MES474K450VDC	Joey Electronics
C005,C006	Y Cap	1 nF	400V / 4KV	Radial 10mm	5SE102MT402A97E	SUCCESS
C007	Ceramic Cap	10 nF	630V	Radial 5mm	10nF 1KV	SUCCESS
C008,C010	Electrolytic 105°C	68 uF	450V	Radial 7.5mm D18x20mm Horizontal insertion:H < 20mm	EKXG451ELL680MM25S	Nippon Chemi Con
C009	X2 Cap	100 nF	275V	Radial 15mm	HQX104K275I04SANYAY	Shanghai Ultra Tech (UTX)
C011	Ceramic Chip Cap	100 nF	10V	805		
C012	Ceramic Chip Cap	390 nF	10V	805		
C013	Electrolytic 105°C	47 uF	25V	Radial 5mm D8mm	EKMG500ELL470MF11D	Nippon Chemi Con
C014	Ceramic Chip Cap	100 nF	16V	805		
C016	Ceramic Chip Cap	1 nF	10V	805		
C018	CPMX-X2	1 uF	275V	Radial 22.5mm	HQX105K275N04SANYAY	Shanghai Ultra Tech (UTX)
C019	Ceramic Chip Cap	220 pF	10V	805		
C100	Ceramic Cap	10 nF	250V	Radial 5mm	10nF 250V	
C101	Electrolytic 105°C	10 uF	25V	Radial 5mm	EKY-500ELL100ME11D	Nippon Chemi Con
C103	Ceramic Cap	10 nF	250V	Radial 5mm	10nF 250V	
C106,C109,C110	Electrolytic 105°C Low Z	1000 uF	16V	Radial 5mm D8mm	EKY-160ELL102MH20D	Nippon Chemi Con
C111	Electrolytic 105°C Low Z	330 uF	16V	Radial 5mm D8mm	EKY-160ELL331MHB5D	Nippon Chemi Con
C112	Ceramic Chip Cap	470 nF	10V	805		
C113,C114	Ceramic Chip Cap	100 nF	16V	805		
C115,C116	Electrolytic 105°C	10 uF	35V	Radial 5mm D5	EKY-500ELL100ME11D	Nippon Chemi Con
C117	Ceramic Chip Cap	270 pF	10V	805		
C118,C119	Ceramic Chip Cap	100 pF	10V	805		
C121	Ceramic Chip Cap	270 pF	25V	805		
C122,C123	Electrolytic 105°C Low Z	1000 uF	16V	Radial 5mm D8mm	EKY-160ELL102MH20D	Nippon Chemi Con
C126	Electrolytic 105°C Low Z	330 uF	16V	Radial 5mm D8mm	EKY-160ELL331MHB5D	Nippon Chemi Con

C127	CCS-Y1	1 nF	400V / 4KV	Radial 10mm	5SE102MT402A97E	SUCCESS
C130	Ceramic Chip Cap	470 nF	10V	805		
C137	Ceramic Chip Cap	10 nF	10V	805		
C138	Electrolytic 105°C Low Z	330 uF	16V	Radial 5mm D8mm	KY 16VB330 8*12	Nippon Chemi Con
C140	Ceramic Chip Cap	22 pF	10V	805		
C142	Electrolytic 105°C	220 uF	35V	Radial 5mm D8mm	EKY-350ELL221MH15D	Nippon Chemi Con
C143	Ceramic Chip Cap	4.7 nF	25V	805		
C300,C301	Ceramic Chip Cap	470 nF	16V	805		
C304,C305	Ceramic Chip Cap	1 uF	10V	805		
C306	CFS	100 nF	450V	Radial 15mm	MES104K450VDC	Joey Electronics
C307	Electrolytic 105°C	47 uF	16V	Radial 5mm D5	EKMG500ELL470MF11D	Nippon Chemi Con
C308	Ceramic Chip Cap	1 uF	16V	805		
C309,C310	Ceramic Cap	5 pF	2 kV	Radial 5mm	8NPO5R0D302A76E	SUCCESS
C311	Ceramic Chip Cap	4u7	10V	805		
C312	Ceramic Chip Cap	220 pF	10V	805		
C313,C314	Ceramic Chip Cap	5n6	16V	805		
C315	Ceramic Chip Cap	1 uF	10V	805		
C316,C317	Ceramic Chip Cap	1 nF	16V	805		
C318	Ceramic Chip Cap	10 nF	10V	805		
C319	Ceramic Chip Cap	100 nF	10V	805		
C320,C321	Ceramic Chip Cap	100 pF	10V	805		
C322	Ceramic Chip Cap	1 nF	10V	805		
C323	Ceramic Chip Cap	2n2	10V	805		
C324	Ceramic Chip Cap	47 pF	10V	805		
C325,C326	Ceramic Chip Cap	10 nF	10V	805		
C327	Ceramic Chip Cap	680 pF	10V	805		
C328	CFS	1 uF	450V	Radial 15mm	MES105K450VDC	Joey Electronics
C329,C330	Ceramic Cap	5 pF	2 kV	Radial 5mm	8NPO5R0D302A76E	SUCCESS
CN001	Connector	4333-W05ST	5A 250V	Radial 15mm with 2 ext. pins	4333-W05ST	LEAMAX Enterprise
CN300-CN305	HV Lamp Connector	SM02B-BHSS-1-TB	2pins	Radial 12.5mm	01040023028	SUNDA
CN306	Signal connector	4324-2S	Straight 2pins	Radial 2.5mm	4324-2S	LEAMAX Enterprise

CN309	Signal connector	4324-10S	Straight 10pins	Radial 2.5mm	4324-10S	LEAMAX Enterprise
CN311	Signal connector	4324-11S	Straight 11pins	Radial 2.5mm	4324-11S	LEAMAX Enterprise
D001	Diode	1N5406	3A-600V	DO-201 TOP Manual Axial 22.5mm 10mm High Preformed	1N5406	ON Semiconductor
D002	Diode	MUR550APF	5A-520V	DO-201 TOP Manual Axial 22.5mm 10mm High Preformed.	MUR550APF	ON Semiconductor
D003	Diode	MMSD4148	0.2A-100V	SOD-123	MMSD4148	ON Semiconductor
D100	Diode	BAV21	0.2A 250V	DO-35 Axial 12.5mm	BAV21	PANJIT
D101	Diode Ultra Fast	MUR160	1A 600V	DO-41 Axial 12.5mm	MUR160	ON Semiconductor
D104	Diode	MMSD4148	0.2A 100V	SOD-123	MMSD4148	ON Semiconductor
D105	Diode	BAV21	0.2A 250V	DO-35 Axial 12.5mm	BAV21	PANJIT
D107	Diode, Dual Schottky	MBR20100CTG	20A 100V	TO-220AB	MBR20100CTG	ON Semiconductor
D107A	Screw			M3*8		
D107B	Heat-sink			40mm		YUAN FENG Industrial Co,,LTD.
D107C	Insulator				SLTO-220	JUNHO
D108,D110	Diode	MMSD4148	0.2A 100V	SOD-123	MMSD4148	ON Semiconductor
D111	Diode, Dual Schottky	MBR20100CTG	20A 100V	TO-220AB	MBR20100CTG	ON Semiconductor
D111A	Screw			M3*8		
D111B	Heat-sink			40mm		YUAN FENG Industrial Co,,LTD.
D111C	Insulator				SLTO-220	JUNHO
D113,D121	Diode	MMSD4148	0.2A 100V	SOD-123	MMSD4148	ON Semiconductor
D122		0R / Jumper				
D124	Carbon Chip Resistor	0R		1206		
D300,D301	Diode	BAV21	0.2A 250V	DO-35 Axial 12.5mm	BAV21	PANJIT
D302	Dual Signal Diode	BAV70LT1	0.2A 75V	SOT-23	BAV70LT1	ON Semiconductor
D303,D304	Dual Schottky diode	BAT54SWT1	0.2A 30V	SOT323	BAT54SWT1	ON Semiconductor
D305	Dual Signal Diode	BAV70LT1	0.2A 75V	SOT-23	BAV70LT1	ON Semiconductor
D306,D307	Diode	BAV21	0.2A 250V	DO-35 Axial 12.5mm	BAV21	PANJIT
D308-D313	Dual Signal Diode	BAV70LT1	0.2A 75V	SOT-23	BAV70LT1	ON Semiconductor
D314,D315	Dual Schottky diode	BAT54SWT1	0.2A 30V	SOT323	BAT54SWT1	ON Semiconductor

F001	Fuse	4A	250V	Axial 5x20mm	UBM-A004	CONQUER
F100	LV Fuse resistance	0.47R 1/2W	250V	Radial 5mm D10	FKN 050 J R47 FK	Synton-Tech Corporation.
F300	HV Fuse resistance	0.47R 1W	450V	Radial 5mm D10	FRN 100S J R47 FK	Synton-Tech Corporation.
F301	LV Fuse resistance	0.47R 1/2W	250V	Radial 5mm D10	FKN 050 J R47 FK	Synton-Tech Corporation.
IC001	PFC Controller	NCP1606B		SOIC-8	NCP1606B	ON Semiconductor
IC100	QFTon Controller	NCP1351B		SOIC-8	NCP1351B	ON Semiconductor
IC101	Voltage Ref.	TL431ACLPRPG	1%	TO-92	TL431ACLPRPG	ON Semiconductor
IC300	Inverter Controller	LX6503-IDW		SOIC-16	LX6503-IDW	Microsemi
J001	Jumper			Axial 12.5mm		
J002	Jumper			Axial 12.5mm		
J100	Jumper			Axial 12.5mm		
J103	Jumper			Axial 12.5mm		
J104	Jumper			Axial 12.5mm		
L001	Diff. Mode Filter	130uH		TOP Manual	JLC2030	Shenzhen Jewel Electric.
L002	PFC Coil	TF2815 - 150uH		TOP Manual	JLC2832	Shenzhen Jewel Electric.
L005	Common Mode Filter	CFS24 - 2mH	2.5A	TOP Manual	JLB24103	Shenzhen Jewel Electric.
L101,L102	Inductance filter	10uH	5A	Radial 5mm	JLC0895	Shenzhen Jewel Electric.
M300.M301	Dual N+P MOS Driver	NTGD4167C	2A 30V	TSOP-6	NTGD4167C	ON Semiconductor
PC100,PC101	Opto-coupler	SFH817A		DIP-4	SFH817A	SHARP
Q001	Power MOS	STP11NK50ZFP	11A 500V	TO220FP	STP11NK50ZFP	STMicroelectronics
Q001A	Screw			M3*8		
Q001B	Heat-sink			70mm		YUAN FENG Industrial Co,,LTD.
Q002	PNP transistor	BC856ALT1		SOT-23	BC856ALT1	ON Semiconductor
Q103	Dual NPN	BC846BDW		SOT-363	BC846BDW	ON Semiconductor
Q106	Power MOS	STD3NK60ZT4	4A 600V	DPAK	STD3NK60ZT4	STMicroelectronics
Q107	PNP	BC856ALT1		SOT-23	BC856ALT1	ON Semiconductor
Q108,Q111,Q112	NPN	BC846ALT1		SOT-23	BC846ALT1	ON Semiconductor
Q113	NMOS	NTD14N03R	14A 30V	DPAK	NTD14N03R	ON Semiconductor
Q114	NMOS	NTD3055-094T4G	12A 60V	DPAK	NTD3055-094T4G	ON Semiconductor
Q300-Q303	Power MOS	STD3NK50ZT4	3A 500V	DPAK	STD3NK50ZT4	STMicroelectronics
Q304,Q305	Signal NMOS	NTA4153N-SC75	1A 20V	SC75	NTA4153N-SC75	ON Semiconductor
R002	Carbon Film Resistor	1M3 1%	1/4W	Axial 12.5mm		

R004	Carbon Chip Resistor	27K		805		
R005	Carbon Chip Resistor	68		805		
R006	Carbon Film Resistor	1M3 1%	1/4W	Axial 12.5mm		
R008	Carbon Chip Resistor	68		805		
R009	Carbon Chip Resistor	10K		805		
R010	Carbon Film Resistor	1M3 1%	1/4W	Axial 12.5mm		
R011	Carbon Chip Resistor	56K		805		
R012	Carbon Chip Resistor	220		805		
R013	Carbon Chip Resistor	24K9 1%		805		
R014	Wirewound Resistor	0.10 5%	2W	TOP Manual Axial 22.5mm		
R015-R020	Carbon Film Resistor	150K		805		
R024	Carbon Chip Resistor	68		805		
R025	Carbon Chip Resistor	470		805		
R026	Carbon Chip Resistor	680		805		
R100,R101,R102	Carbon Film Resistor	1M	1/4W	Axial 12.5mm		
R104	Metal Film Resistor	33K 5%	2W	TOP Manual Axial 22.5mm 10mm High Preformed.		
R108	Wirewound Resistor	0.47R 5%	2W	TOP Manual Axial 22.5mm		
R112	Carbon Chip Resistor	3K3		805		
R113	Carbon Film Resistor	7K5	1/4W	Axial 12.5mm		
R114	Carbon Chip Resistor	0R		805		
R116	Carbon Chip Resistor	100		805		
R117	Carbon Chip Resistor	47		805		
R118	Carbon Chip Resistor	10		805		
R119	Carbon Chip Resistor	10K		805		
R120	Carbon Chip Resistor	20K		805		
R121	Carbon Chip Resistor	2K7		805		
R122	Carbon Chip Resistor	4K7		805		
R124	Carbon Chip Resistor	470		805		
R125	Carbon Chip Resistor	1K		805		
R127	Carbon Film Resistor	2K2	1/4W	Axial 12.5mm		
R129	Carbon Chip Resistor	100K		805		

R130	Carbon Chip Resistor	150K		805		
R131	Carbon Chip Resistor	10K		805		
R134	Carbon Film Resistor	27	1/4W	Axial 12.5mm		
R136	Carbon Chip Resistor	47K		805		
R137	Carbon Chip Resistor	220		805		
R138	Carbon Chip Resistor	1K		805		
R142	Carbon Chip Resistor	16K2 1%		805		
R144	Carbon Chip Resistor	6K19 1%		805		
R147	Carbon Chip Resistor	100		805		
R148	Carbon Chip Resistor	4K7		805		
R149	Carbon Chip Resistor	0R		805		
R153	Carbon Chip Resistor	10K		805		
R154	Carbon Film Resistor	100K	1/4W	Axial 12.5mm		
R155	Carbon Chip Resistor	2K49 1%		805		
R157	Carbon Chip Resistor	1K		805		
R158,R159	Carbon Chip Resistor	2K2		805		
R161	Carbon Chip Resistor	100K		805		
R163	Carbon Chip Resistor	4K7		805		
R164	Carbon Chip Resistor	100K		805		
R165	Carbon Chip Resistor	470		805		
R166	Carbon Chip Resistor	4K7		805		
R167,R168	Carbon Chip Resistor	470		805		
R170	Carbon Chip Resistor	1K		805		
R172,R300	Carbon Chip Resistor	4K7		805		
R301	Carbon Chip Resistor	2k21 1%		805		
R302	Carbon Chip Resistor	4K7		805		
R303	Carbon Chip Resistor	2k21 1%		805		
R304,R305	Carbon Chip Resistor	56		805		
R306,R307	Carbon Chip Resistor	3K3		805		
R308,R309	Carbon Chip Resistor	422		805		
R310,R311	Carbon Chip Resistor	10K		805		
R312,R313	Carbon Chip Resistor	4K7		805		

R316,R317	Carbon Chip Resistor	3K3		805		
R318,R319	Carbon Chip Resistor	1K5		805		
R320,R321	Carbon Chip Resistor	10K		805		
R322,R323	Carbon Chip Resistor	100K		805		
R324,R325	Carbon Chip Resistor	4K7		805		
R326,R327	Carbon Chip Resistor	3K3		805		
R328,R329	Carbon Chip Resistor	4K7		805		
R330,R331	Carbon Chip Resistor	3K3		805		
R332	Carbon Chip Resistor	75K		805		
R333,R334	Carbon Chip Resistor	750K		805		
R335,R336	Carbon Chip Resistor	4K7		805		
R337	Carbon Chip Resistor	120		805		
R338,R339	Carbon Chip Resistor	150		805		
R340	Carbon Chip Resistor	120		805		
R341,R342	Carbon Chip Resistor	3K3		805		
R343-R345	Carbon Chip Resistor	10K		805		
R346-R348	Carbon Chip Resistor	4K7		805		
R349	Carbon Chip Resistor	1K0		805		
R350	Carbon Chip Resistor	3K3		805		
R351	Carbon Chip Resistor	2K0		805		
R352	Carbon Chip Resistor	3K3		805		
R353	Carbon Chip Resistor	10K		805		
R354	Carbon Chip Resistor	2K0		805		
R355	Carbon Chip Resistor	20K		805		
R356	Carbon Chip Resistor	10K		805		
R357	Carbon Chip Resistor	100K		805		
R358	Carbon Chip Resistor	18K		805		
R359	Carbon Chip Resistor	22K		805		
R360	Carbon Chip Resistor	33K		805		
R361,R362	Carbon Film Resistor	220	1/4W	Axial 12.5mm		
R363,R364	Carbon Chip Resistor	22K		805		
R365-R368	Carbon Chip Resistor	120		805		

RT001	Thermistor	2R5 3W		TOP Manual Rad 7.5mm	SCK 15 2R5 8 M S Y	Thinking Electronic
RV001	Varistor	TVR10471KSY	470V	TOP Manual Rad 7.5mm	TVR10471KSY	Thinking Electronic
T100	Switch Mode Transformer	Flyback EER28L		TOP Manual	BCK-28-1050	Shenzhen Jewel Electric.
T300-T302,T305-T308, T310-T314	Current Balance Transformer	PBT-07087-1322G		TOP Manual	PBT-07087-1322G	Taipei Multipower Products (TMP)
T303,T304	Drive Transformer	BCK-13-021TC		TOP Manual	BCK-13-021TC	Shenzhen Jewel Electric.
T309	Inverter. HV Transformer	PIT125050-3551 AG		TOP Manual	PIT125050-3551 AG	Taipei Multipower Products (TMP)
ZD001	Diode, Zener	1N4733A	5.1V 5%	DO-41 Axial 12.5mm	1N4733A	ON Semiconductor
ZD100	Diode, Zener	1N5929B	15V 5%	DO-41 Axial 12.5mm	1N5929B	ON Semiconductor
ZD101	Diode, Zener	1N4746A	22V 5%	DO-41 Axial 12.5mm	1N4746A	ON Semiconductor
ZD103	Diode, Zener	1N4733A	5.1V 5%	DO-41 Axial 12.5mm	1N4733A	ON Semiconductor

Notes: Resistor tolerances are +/- 5% unless noted otherwise

Capacitor tolerances are +/- 10% unless noted otherwise

Electrolytic capacitor tolerances are +/- 20% unless noted otherwise

NCP1351

- [Datasheet](#)
- [AND8288 NCP1351 Evaluation Board Documentation](#)
- [Modeling the NCP1351](#)

NCP1606/7

- [NCP1606 Data Sheet](#)
- [NCP1607 Data Sheet](#)
- [AND8123 Power Factor Correction Operating in Critical Conduction Mode](#)
- [AND8353 Implementing Cost Effective & Robust Power Factor Correction with NCP1607](#)
- [AND8154 Universal Adapter Power Supply with Active PFC](#)
- [AND8016 Design of Power Factor Correction Circuits](#)
- [PFC Handbook](#)

LX6503

- [Data Sheet](#)
- [Backlight Design for large LCD-TV Screens Article](#)

Magnetics Suppliers

- [TMP – HV Inverter Transformer and Balancers](#)
- [Jewel – Flyback Transformer and PFC Inductor](#)

References on Energy Standards

CSC (China)
- http://www.cecp.org.cn

EU Eco-label (Europe)
> http://ec.europa.eu/environment/ecolabel/product/pg_television_en.htm

EU Code of Conduct (Europe)
- http://www.eup-network.de/product-groups/

Group for Energy Efficient Appliances (Europe)
- http://www.efficient-appliances.org/Criteria.htm

Top Runner (Japan)
- http://www.eccj.or.jp/top_runner/index.html
- http://www.eccj.or.jp/top_runner/e_0710.html

Energy Saving Label (Korea)
- http://www.kemco.or.kr/

Energy Star
- http://www.energystar.gov/
- http://www.energystar.gov/index.cfm?fuseaction=find_a_product.showProductGroup&pgw_code=TV
- http://www.energystar.gov/index.cfm?c=tv_vcr.pr_crit_tv_vcr

Standby Considerations
- http://standby.lbl.gov

Schematics of Complete PCB with all Configuration Options

The following four pages contain the schematics for the complete PCB with all possible options (see Table 3) of the GreenPoint HV-LIPS design for details on the alternate configurations.
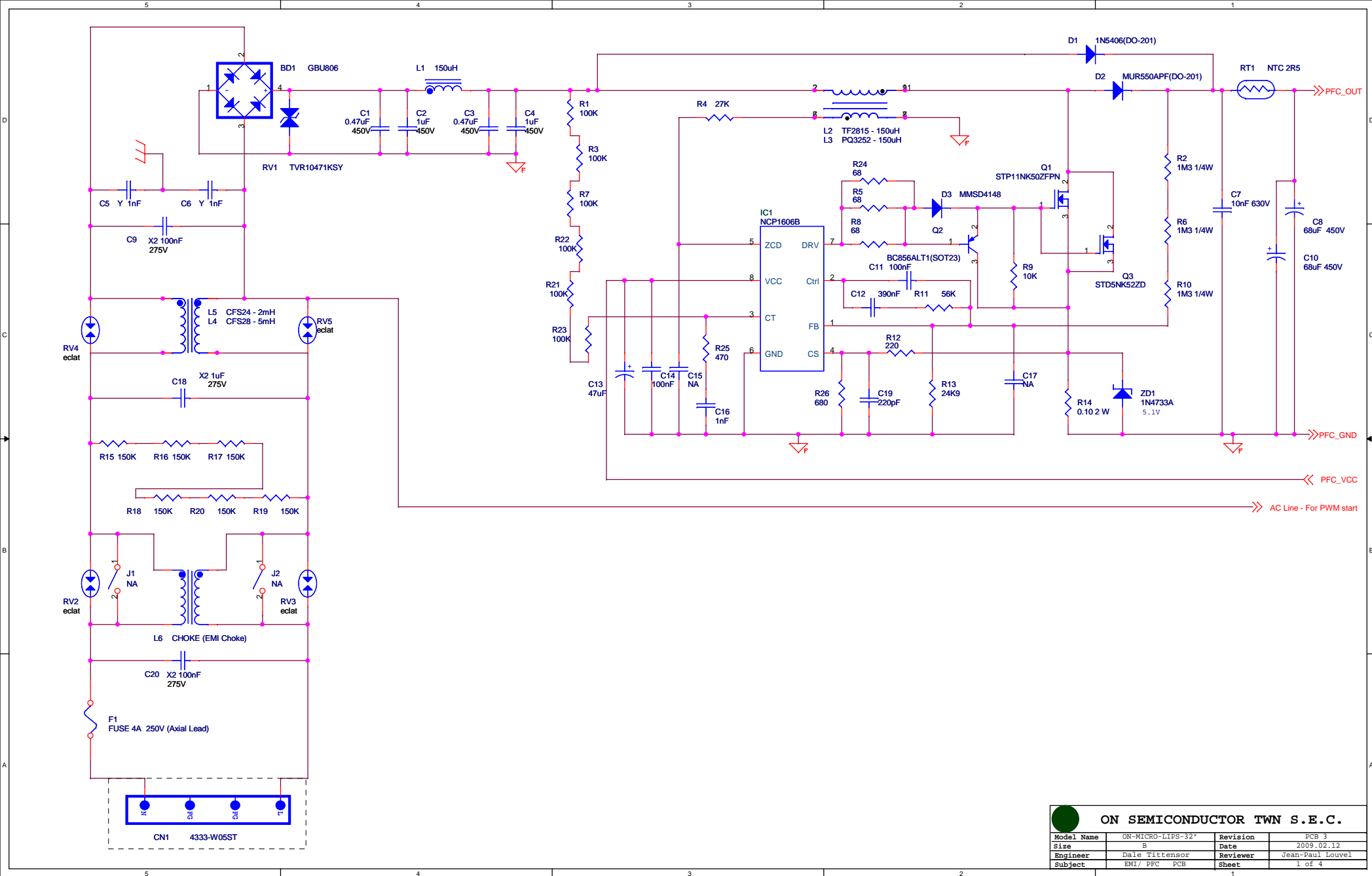
Schematic of Complete PCB with alternative configurations

ON SEMICONDUCTOR TWN S.E.C.		
Model Name	ON-MICRO-LIPS-32"	Revision	PCB 3
Size	B	Date	2009.02.12
Engineer	Dale Tittensor	Reviewer	Jean-Paul Louvel
Subject	EMI/ PFC PCB	Sheet	1 of 4

Schematic of Complete PCB with alternative configurations
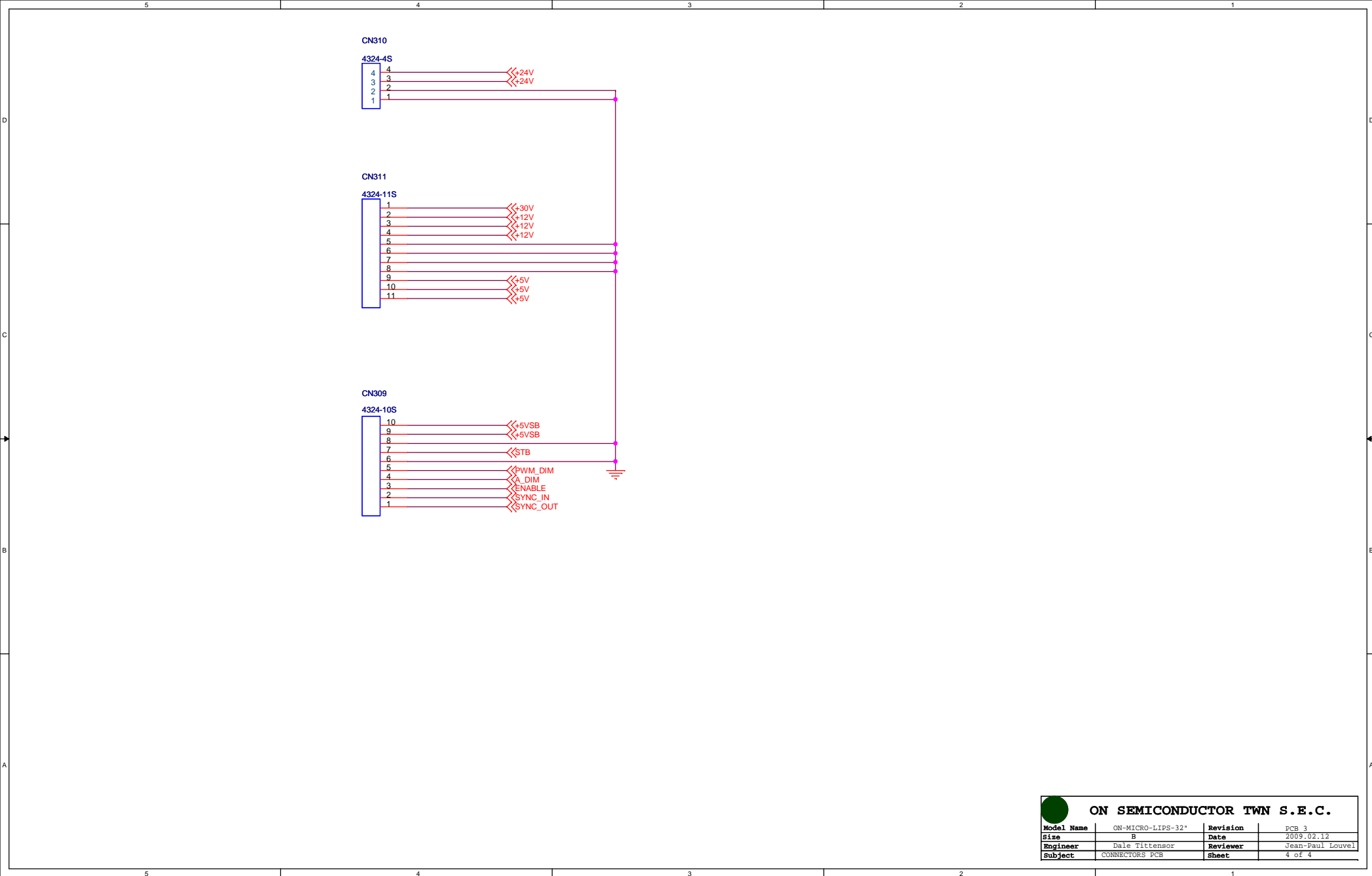
Model Name	ON-MICRO-LIPS-32"	Revision	PCB 3
Size	B	Date	2009.02.12
Engineer	Dale Tittensor	Reviewer	Jean-Paul Louvel
Subject	SMPS PCB	Sheet	2 of 4

ON SEMICONDUCTOR TWN S.E.C.

CN310

4324-4S

4	4 — +24V
3	3 — +24V
2	2
1	1

CN311

4324-11S

1	1 — +30V
2	2 — +12V
3	3 — +12V
4	4 — +12V
5	5
6	6
7	7
8	8
9	9 — +5V
10	10 — +5V
11	11 — +5V

CN309

4324-10S

10	10 — +5VSB
9	9 — +5VSB
8	8
7	7 — STB
6	6
5	5 — PWM_DIM
4	4 — A_DIM
3	3 — ENABLE
2	2 — SYNC_IN
1	1 — SYNC_OUT

ON SEMICONDUCTOR TWN S.E.C.

Model Name	ON-MICRO-LIPS-32"	Revision	PCB 3
Size	B	Date	2009.02.12
Engineer	Dale Tittensor	Reviewer	Jean-Paul Louvel
Subject	CONNECTORS PCB	Sheet	4 of 4

Schematic of Complete PCB with alternative configurations

Schematic of Complete PCB with alternative configurations

Note:
1. Input Voltage 400V.
2. Output 100W to 200W.
3. ENABLE active above 1.5V.
4. Analog dimming input (A_DIM) 1 to 4VDC, or equivalent PWM signal.
5. PWM dimming input (PWM_DIM) 1 to 4VDC, Controls duty cycle from 0 TO 100%,
   Above 4V goes into continuous operation.
6. T2 and T3 about EE15 size, 25:38+38.
7. T1 about 108:360

ON SEMICONDUCTOR TWN S.E.C.

Model Name	ON-MICRO-LIPS-32"	Revision	PCB 3
Size	B	Date	2009.02.12
Engineer	Dale Tittensor	Reviewer	Jean-Paul Louvel
Subject	INVERTER PCB	Sheet	3 of 4