

MB25
TFT TV
SERVICE MANUAL

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1. INTRODUCTION

17MB25 mainboard is based on MSTAR concept IC. This IC is capable of handling audio processing, video processing, scaling-display processing, 3D comb filter, OSD and text processing, 8 bit dual LVDS transmitter.

TV supports PAL, SECAM, NTSC colour standards and multiple transmission standards as B/G, D/K, I/I', and L/L' including German and NICAM stereo.

Sound system is able to supply 2x10W (10%THD) audio output power for stereo speakers.
Supported peripherals are:

The analog part of the moard can support DVD module which is connected to mainboard through a cable.
The USB feature is supported through digital part of the mainboard.

1 RF input VHF1, VHF3, UHF @ 75Ohm(Common)
1 Side AV (SVHS, CVBS, HP, R/L_Audio) (Common)
1 SCART socket(Common)
1 YPbPr (Common)
1 PC input(Optional)
2 HDMI (Common)
1 Stereo audio input for PC(Common)
1 Line out(Common)
1 S/PDIF output(Common)
1 Side S-Video(Optional)
1 Headphone(Common)
1 Common interface(Optional)
1 Digital USB(Opional)
1 RS232(Optional)

2. TUNER

A horizontal mounted and Digital Half-Nim tuner is used in the product, which covers 3 Bands(From 48MHz to 862MHz for COFDM, from 45.25MHz to 863.25MHz for CCIR CH). The tuning is available through the digitally controlled I2C bus (PLL). Below you will find info on the Tuner in use.

1.1 General description of TDTC-G101D:

The Tuner covers 3 Bands(from 48MHz to 862MHz for COFDM, from 45.25MHz to 863.25MHz for CCIR CH). Band selection and Tuning are performed digitally via the I2C bus.

1.2 Features of TDTC-G101D:

- Digital Half-NIM tuner for COFDM
- Covers 3 Bands(From 48MHz to 862MHz for COFDM,
- From 45.25MHz to 863.25MHz for CCIR CH)

- Including IF AGC with SAW Filter
- Bandwidth Switching (7/8 MHz) possible
- DC/DC Converter built in for Tuning Voltage
- Internal(or External) RF AGC, Antenna Power Optional

1.3 Pin Configuration

PIN NAME	PIN No.	PIN Description
Ant PWR	1	+5V (for Active Antenna), Optional
B1	2	+ 5V (for Loop through & DC-DC)
RF AGC	3	N.C
SCL	4	I²C Bus for TUNER PLL
SDA	5	I²C Bus for TUNER PLL
B2	6	+ 5V (for TU & IF AGC AMP)
Vtu T.P	7	N.C
AS	8	PLL IC Address selection
IF AGC Control	9	IF AGC Control
DIF2	10	Total IF Output2
DIF1	11	Total IF Output1
AIF	12	Tuner IF Output

3. AUDIO AMPLIFIER STAGE WITH TPA3101

3.1 General Description of TPA3101

The TPA3101D2 Rev.A evaluation module consists of a single 10-W, class-D, stereo audio power amplifier complete with a small number of external components mounted on a circuit board that can be used to directly drive a speaker with an external analog audio source as the input.

The gain of the amplifier is controlled by two gain select pins. The gain selections are 20, 26, 32, 36dB.
The outputs are fully protected against shorts to GND, Vcc and output to output shorts with an auto recovery feature and monitor output.

3.2 Features of TPA3101

- 10-W/ch into an 8-Ω Load From a 13-V Supply
- 9.2-W/ch into an 8-Ω Load From a 12-V Supply
- Operates from 10 V to 26 V
- 87% Efficient Class-D Operation Eliminates
- Need for Heat Sinks
- Four Selectable, Fixed Gain Settings

- Differential Inputs
- Thermal and Short-Circuit Protection With
- Auto Recovery Feature
- Clock Output for Synchronization With Multiple Class-D Devices
- Surface Mount 7 mm ´ 7 mm, 48-pin QFN Package
- Surface Mount 7 mm ´ 7 mm, 48-pin HTQFP Package

3.3 Pin Configuration of TPA3101

TERMINAL			I/O	DESCRIPTION
NAME	QFN NO.	HTQFP NO.		
$\overline{\text{SHUTDOWN}}$	44	44	I	Shutdown signal for IC (LOW = disabled, HIGH = operational). TTL logic levels with compliance to AVCC.
RINN	2	2	I	Negative audio input for right channel. Biased at VREG/2.
RINP	3	3	I	Positive audio input for right channel. Biased at VREG/2.
LINN	6	6	I	Negative audio input for left channel. Biased at VREG/2.
LINP	5	5	I	Positive audio input for left channel. Biased at VREG/2.
GAIN0	8	7, 8	I	Gain select least significant bit. TTL logic levels with compliance to VREG.
GAIN1	9	9	I	Gain select most significant bit. TTL logic levels with compliance to VREG.
GND		1, 12, 13, 24, 25, 36, 37		Connect to the thermal pad.
MUTE	45	45	I	Mute signal for quick disable/enable of outputs (HIGH = outputs high-Z, LOW = outputs enabled). TTL logic levels with compliance to AVCC.
FAULT	46	46	O	TTL compatible output. HIGH = short-circuit fault. LOW = no fault. Only reports short-circuit faults. Thermal faults are not reported on this terminal.
BSLP	18	18	I/O	Bootstrap I/O for left channel, positive high-side FET.
PVCCL	26, 27	26, 27		Power supply for left channel H-bridge, not internally connected to PVCCR or AVCC.
LOUTP	19, 20	19, 20	O	Class-D 1/2-H-bridge positive output for left channel.
PGNDL	28, 29	28, 29		Power ground for left channel H-bridge.
LOUTN	21, 22	21, 22	O	Class-D 1/2-H-bridge negative output for left channel.
BSLN	23	23	I/O	Bootstrap I/O for left channel, negative high-side FET.
VCLAMPL	30	30		Internally generated voltage supply for left channel bootstrap capacitor.
VCLAMPR	31	31		Internally generated voltage supply for right channel bootstrap capacitor.
BSRN	38	38	I/O	Bootstrap I/O for right channel, negative high-side FET.
ROUTN	39, 40	39, 40	O	Class-D 1/2-H-bridge negative output for right channel.
PGNDR	32, 33	32, 33		Power ground for right channel H-bridge.
ROUTP	41, 42	41, 42	O	Class-D 1/2-H-bridge positive output for right channel.
PVCCR	34, 35	34, 35		Power supply for right channel H-bridge, not connected to PVCCL or AVCC.
BSRP	43	43	I/O	Bootstrap I/O for right channel, positive high-side FET.
AGND	4, 17	4, 17		Analog ground for digital/analog cells in core.
ROSC	14	14	I/O	I/O for current setting resistor of ramp generator.
MSTR/$\overline{\text{SLV}}$	10	10	I	Master/Slave select for determining direction of SYNC terminal. HIGH=Master mode, SYNC terminal is an output; LOW = slave mode, SYNC terminal accepts a clock input. TTL logic levels with compliance to VREG.
SYNC	11	11	I/O	Clock input/output for synchronizing multiple class-D devices. Direction determined by MSTR/$\overline{\text{SLV}}$ terminal. Input signal not to exceed VREG.
VBYP	16	16	O	Reference for preamplifier. Nominally equal to 1.25 V. Also controls start-up time via external capacitor sizing.
VREG	15	15	O	4-V regulated output for use by internal cells, GAINx, MUTE, and MSTR/$\overline{\text{SLV}}$ pins only. Not specified for driving other external circuitry.
AVCC	48	47, 48		High-voltage analog power supply. Not internally connected to PVCCR or PVCCL.
NC	1, 7, 12, 13, 24, 25, 36, 37, 47			Not internally connected.
Thermal Pad	-	-	-	Connect to AGND and PGND – should be star point for both grounds. Internal resistive connection to AGND and PGND. Thermal vias on the PCB should connect this pad to a large copper area on an internal or bottom layer for the best thermal performance. *The Thermal Pad must be soldered to the PCB for mechanical reliability.*

4. MICROCONTROLLER (MSTAR)

4.1 Genaral Description

The MST6WB7GQ-3 is a high performance and fully integrated IC for multi-function LCD monitor/TV with resolutions up to full HD (1920x1080). It is configured with an integrated triple-ADC/PLL, an integrated DVI/HDCP/HDMI receiver, a multi-standard TV video and audio decoder, two video de-interlacers, two scaling engines, the MStarACE-3 color engine, an on-screen display controller, an 8-bit MCU and a built-in output panel interface. By use of external frame buffer, PIP/POP is provided for multimedia applications. Furthermore, 3-D video decoding and processing are fulfilled for high-quality TV applications. To further reduce system costs, the MST6WB7GQ-3 also integrates intelligent power management control capability for green-mode requirements and spread-spectrum support for EMI management.

4.2 Features

LCD TV controller with PIP/POP display functions

- Input supports up to UXGA & 1080P
- Panel supports up to full HD (1920x1080)
- TV decoder with 3-D comb filter
- Multi-standard TV sound demodulator and decoder
- 10-bit triple-ADC for TV and RGB/YPbPr
- 10-bit video data processing
- Integrated DVI/HDCP/HDMI compliant receiver
- High-quality dual scaling engines & dual 3-D video de-interlacers
- 3-D video noise reduction
- Full function PIP/PBP/POP
- MStarACE-3 picture/color processing engine
- Embedded On-Screen Display (OSD) controler engine
- Built-in MCU supports PWM & GPIO
- Built-in dual-link 8/10-bit LVDS transmitter
- 5-volt tolerant inputs
- Low EMI and power saving features
- 296-pin LQFP

NTSC/PAL/SECAM Video Decoder

- Supports NTSC M, NTSC-J, NTSC-4.43, PAL (B,D,G,H,M,N,I,Nc), and SECAM
- Automatic TV standard detection
- Motion adaptive 3-D comb filter for NTSC/PAL
- 8 configurable CVBS & Y/C S-video inputs
- Supports Teletext level-1.5, WSS, VPS, Closed-caption, and V-chip
- Macrovision detection
- CVBS video output

Video IF for Multi-Standard Analog TV

- Digital low IF architecture
- Stepped-gain PGA with 26 dB tuning range and 1 dB tuning resolution
- Maximum IF analog gain of 37dB in addition to digital gain
- Programmable TOP to accommodate different tuner gain to optimize noise and linearity performance

Multi-Standard TV Sound Decoder

- Supports BTSC/NICAM/A2/EIA-J demodulation and decoding
- FM stereo & SAP demodulation
- L/Rx4, mono, and SIF audio inputs
- L/Rx3 loudspeaker and line outputs
- Supports sub-woofer output
- Built-in audio output DAC's
- Audio processing for loudspeaker channel, including volume, balance, mute, tone, EQ, and virtual stereo/surround
- Optional advanced surround available (Dolby1, SRS2, BBE3… etc)

Digital Audio Interface

- I2S digital audio input & output
- S/PDIF digital audio input & output
- HDMI audio channel processing capability
- Programmable delay for audio/video synchronization

Analog RGB Compliant Input Ports

- Three analog ports support up to UXGA
- Supports HDTV RGB/YPbPr/YCbCr
- Supports Composite Sync and SOG (Sync-on-Green) separator
- Automatic color calibration

DVI/HDCP/HDMI Compliant Input Port

- Two HDMI input ports with built-in switch
- Supports TMDS clock up to 225MHz @ 1080P 60Hz with 12-bit deep-color resolution
- Single link on-chip DVI 1.0 compliant receiver
- High-bandwidth Digital Content Protection(HDCP) 1.1 compliant receiver

5. INTEGRATED DVB-T RECEIVER (CHEERTEK)

5.1 General Description

CT216T is a highly integrated single chip for DVB-T compliant STB solution. Compared with Cheertek's previous generations of STB receiver devices. CT216T further interates COFDM demodulator USB 2.0 HS host controller, memory card reader, 1/2-bit SPIFlash interface, audio DAC, PWM in/out and SAR-ADC functions. In additiont special enhangements are provided such as MPEG-4 video decoding, 16-bit OSD with anti-flickering,

HW JPEG decoding, flesh tone and black-white extensions, and improvement of small video quality.

CT216T includes COFDM demodulator transport stream de-multiplexer, DVB-CSA compliant de-scrambler, RISC MPUs, MPEG-1/2/4 AV decoder, digital TV encoder, audio DACs, USB 2.0 HS host controller, memory card reader, smart card reader, CI controller and other peripherals.

Cli216T is designed in focus on the market of single tuner input product which makes, it a cost effective solution. Supports include free to air, conditional access for SC (Smart card) and CI portable devices, PVR, LCD TV, and other DVB-T applications.

5.2 Features

COFDM Demodulator

- ETSI EN 300 744 DVB-T NorDig Unified 1.0.3, and D-book compliant
- Automatic spectral inversion, detection
- Integrated ADC
- Direct IF (36.167 MHz or 43.75 MHz) or low IF (4.57 MHz) supported
- Single IF AGC or dual RF/lF AGC controls with ΔΣ modulabon
- Impulsive noise cancellation
- Carrier acquisition range: ±400 kHz (extensible to ±600 kHz in 8MHz BW)
- Adjacent channel interference (ACI) filter,for supporting 6, 7, and 8MHz channels with one 8MHz analog filter
- Co-channel interterence (CCl) supression
- RF signal strength monitor

MPU

- Three 32-bit RISC MPU run up to 166MHz with total 448DMIPS
- 8KB I-Cache and 8KB D-Cache
- Two general purpose timers
- Watchdog timer
- DSU for source level debug

Memory

- 6-bit SDRAM controller supports up to 32MB (16MB for l28-pin)
- Unified memory architecture
- Parallel flash (216-pin only)
- 1/2-bit SPI flash

Transport De-multiplexing

- TS, PES, and ES demultiplexing
- OneTS path
- CI CAM interface (216-pin only)
- 32 general purpose PID filters
- 32 Section filters
- CRC-32 accelerator
- DVB-CSA de-scramblers

Video Decoding and Processing

- MPEG-2 MP@ML
- MPEG-4 SP&ASP
- PAL/NTSC format conversion
- 3:2 pull down
- Zoom in/out from 1/16X to 16X
- HW JPEG decode
- 4/8/16-bit OSD with anti-flickering
- On chip NTSC/PAL TV encoder
- CVBS, S-VHS, and component video
- VBI insertion for Teletext, CC and WSS
- ITU-R BT.601 and ITU-R BT.656 outputs
- Flesh tone extension
- Black/white extension,

Audio Decoding and Processing

- MPEG-1: layer 1/2/3
- MPEG-2: layer 1/2
- Decode MPEG-2 and MPEG-1 audio at sampling frequency of 16K, 22.05K, 24K, 32K, 44.1K, and 48KHz
- Decode CU-DA at sampling frequency of 44.1 KHz
- SPDIF out for AC-3 by-pass
- Embedded 2 channels audio DAC for L/R outputs
- Digital mute control and volume adjustment

OSD(On Screen Display)

- There are total 9 display planes: border; background. video. RS1 (Rectangle Strip 1), RS2, OSD, RS3, RS4, and cursor.
- 4/8l16-bit OSD with anti-flickering and anti-flutter
- Support alpha-blending per color
- Adjustable brightness control in window
- Bitmap OSD
- Support horizontal pixel duplication to enlarge bitmap automatically
- Support sub-region redraw to facilitate bitmap display.

Digitnal TV Encoder

- NTSC-M, PAL-B, D, G, H, I, Nc, M encoding
- Four video DACs to provide 6 configuration output: modes
- Support CVBS, S-VHS. and component video outs
- VBI insertion for Teletext, CC and WSS
- Color burst amplitude control
- Programmable sync. level
- On chip, color-bar generator

High Speed I/O

- USB 2.0 HS host controller

- Memory card reader with SD, MMC, and MS interfaces
- Compliant with SD spec. 1.1 and MMC spec. 4.0 with 1-bit & 4-bit modes.
- Compliant with Memory Stick Pro format spec. 1.02 and Memory stick format spec 1.43 with 1-bit and 4-bit modes.

Peripherals
- Up to 3 full duplex UART with 16-byte FIFO
- 2-wire serial (2WS) in master mode .. .
- Up to 2 IS0-7816 compliant SC (1 in 128-pin, can also be used as UART)
- 5 digits 7-Segrnent LED control
- 5x3 two-dimension key scan
- 2 SAR-ADC input
- 4 PWM input/output
- 1 HW IR command decode
- GPIO

Electrical and Physical Characteristics
- Capable of using single 27MHz clock input crystal
- 1.8V and 3.3V dual power supply
- Power standby mode
- PQFP-128 (CT216T-Z) or LQFP-216 (CT216T-R) package

6. 4MX16 BIT SYNCHRONOUS DRAM (SDRAM)

6.1 General Description

The EM638165 SDRAM is a high-speed CMOS synchronous DRAM containing 64 Mbits. It is internally configured as 4 Banks of 1M word x 16 DRAM with a synchronous interface (all signals are registered on the positive edge of the clock signal, CLK). Read and write accesses to the SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of a BankActivate command which is then followed by a Read or Write command. The EM638165 provides for programmable Read or Write burst lengths of 1, 2, 4, 8, or full page, with a burst termination option. An auto precharge function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst sequence. The refresh functions, either Auto or Self Refresh are easy to use. By having a programmable mode register, the system can choose the most suitable modes to maximize its performance. These devices are well suited for applications requiring high memory bandwidth and particularly well suited to high performance PC applications.

6.2 Features

- Fast access time from clock: 4.5/5/5.4 ns
- Fast clock rate: 200/166/143 MHz
- Fully synchronous operation
- Internal pipelined architecture
- 1M word x 16-bit x 4-bank
- Programmable Mode registers

- CAS Latency: 2, or 3
- Burst Length: 1, 2, 4, 8, or full page
- Burst Type: interleaved or linear burst
- Burst stop function
- Auto Refresh and Self Refresh
- 4096 refresh cycles/64ms
- CKE power down mode
- Single +3.3V ± 0.3V power supply
- Interface: LVTTL
- 54-pin 400 mil plastic TSOP II package
- Pb free and Halogen free
- 60-ball 6.4mm x 10.1mm VFBGA package
- Pb free

6.3 Pin Configuration

<table>
<tr><th>Symbol</th><th>Type</th><th>Description</th></tr>
<tr><td>CLK</td><td>Input</td><td>Clock: CLK is driven by the system clock. All SDRAM input signals are sampled on the positive edge of CLK. CLK also increments the internal burst counter and controls the output registers.</td></tr>
<tr><td>CKE</td><td>Input</td><td>Clock Enable: CKE activates (HIGH) and deactivates (LOW) the CLK signal. If CKE goes low synchronously with clock (set-up and hold time same as other inputs), the internal clock is suspended from the next clock cycle and the state of output and burst address is frozen as long as the CKE remains low. When all banks are in the idle state, deactivating the clock controls the entry to the Power Down and Self Refresh modes. CKE is synchronous except after the device enters Power Down and Self Refresh modes, where CKE becomes asynchronous until exiting the same mode. The input buffers, including CLK, are disabled during Power Down and Self Refresh modes, providing low standby power.</td></tr>
<tr><td>BA0,BA1</td><td>Input</td><td>Bank Activate: BA0, BA1 input select the bank for operation.
<table>
<tr><th>BA1</th><th>BA0</th><th>Select Bank</th></tr>
<tr><td>0</td><td>0</td><td>BANK #A</td></tr>
<tr><td>0</td><td>1</td><td>BANK #B</td></tr>
<tr><td>1</td><td>0</td><td>BANK #C</td></tr>
<tr><td>1</td><td>1</td><td>BANK #D</td></tr>
</table></td></tr>
<tr><td>A0-A11</td><td>Input</td><td>Address Inputs: A0-A11 are sampled during the BankActivate command (row address A0-A11) and Read/Write command (column address A0-A7 with A10 defining Auto Precharge) to select one location out of the 2M available in the respective bank. During a Precharge command, A10 is sampled to determine if all banks are to be precharged (A10 = HIGH). The address inputs also provide the op-code during a Mode Register Set command.</td></tr>
<tr><td>CS#</td><td>Input</td><td>Chip Select: CS# enables (sampled LOW) and disables (sampled HIGH) the command decoder. All commands are masked when CS# is sampled HIGH. CS# provides for external bank selection on systems with multiple banks. It is considered part of the command code.</td></tr>
<tr><td>RAS#</td><td>Input</td><td>Row Address Strobe: The RAS# signal defines the operation commands in conjunction with the CAS# and WE# signals and is latched at the positive edges of CLK. When RAS# and CS# are asserted "LOW" and CAS# is asserted "HIGH," either the BankActivate command or the Precharge command is selected by the WE# signal. When the WE# is asserted "HIGH," the BankActivate command is selected and the bank designated by BA is turned on to the active state. When the WE# is asserted "LOW," the Precharge command is selected and the bank designated by BA is switched to the idle state after the precharge operation.</td></tr>
<tr><td>CAS#</td><td>Input</td><td>Column Address Strobe: The CAS# signal defines the operation commands in conjunction with the RAS# and WE# signals and is latched at the positive edges of CLK. When RAS# is held "HIGH" and CS# is asserted "LOW," the column access is started by asserting CAS# "LOW." Then, the Read or Write command is selected by asserting WE# "LOW" or "HIGH."</td></tr>
<tr><td>WE#</td><td>Input</td><td>Write Enable: The WE# signal defines the operation commands in conjunction with the RAS# and CAS# signals and is latched at the positive edges of CLK. The WE# input is used to select the BankActivate or Precharge command and Read or Write command.</td></tr>
</table>

LDQM, UDQM	Input	**Data Input/Output Mask:** Controls output buffers in read mode and masks Input data in write mode.
DQ0-DQ15	Input / Output	**Data I/O:** The DQ0-15 input and output data are synchronized with the positive edges of CLK. The I/Os are maskable during Reads and Writes.
NC/RFU	-	**No Connect:** These pins should be left unconnected.
V_{DDQ}	Supply	**DQ Power:** Provide isolated power to DQs for improved noise immunity. (3.3V± 0.3V)
V_{SSQ}	Supply	**DQ Ground:** Provide isolated ground to DQs for improved noise immunity. (0 V)
V_{DD}	Supply	**Power Supply:** +3.3V ± 0.3V
V_{SS}	Supply	**Ground**

7. 512K CMOS SERIAL FLASH – MX25L512

7.1 General Description

The MX25L512 is a CMOS 524,288 bit serial Flash memory, which is configured as 65,536 x 8 internally. The MX25L512 feature a serial peripheral interface and software protocol allowing operation on a simple 3-wire bus. The three bus signals are a clock input (SCLK), a serial data input (SI), and a serial data output (SO). SPI access to the device is enabled by CS# input. The MX25L512 provide sequential read operation on whole chip. After program/erase command is issued, auto program/ erase algorithms which program/ erase and verify the specified page or sector/block locations will be executed. Program command is executed on page (256 bytes) basis, and erase command is executes on chip or sector (4K-bytes). To provide user with ease of interface, a status register is included to indicate the status of the chip. The status read
command can be issued to detect completion status of a program or erase operation via WIP bit. When the device is not in operation and CS# is high, it is put in standby mode and draws less than 10uA DC current. The MX25L512 utilize MXIC's proprietary memory cell, which reliably stores memory contents even after 100,000 program and erase cycles.

7.2 Features

General

- Serial Peripheral Interface (SPI) compatible -- Mode 0 and Mode 3
- 524,288 x 1 bit structure
- 16 Equal Sectors with 4K byte each
- Any Sector can be erased individually
- Single Power Supply Operation
- 2.7 to 3.6 volt for read, erase, and program operations
- Latch-up protected to 100mA from -1V to Vcc +1V
- Low Vcc write inhibit is from 1.5V to 2.5V

Performance

- High Performance
- Fast access time: 85MHz serial clock (15pF + 1TTL Load) and 66MHz serial clock (30pF + 1TTL Load)
- Fast program time: 1.4ms(typ.) and 5ms(max.)/page (256-byte per page)
- Fast erase time: 60ms(typ.) and 120ms(max.)/sector (4K-byte per sector) ; 1s(typ.) and 2s(max.)/chip(512Kb)
- Low Power Consumption
- Low active read current: 12mA(max.) at 85MHz, 8mA(max.) at 66MHz and 4mA(max.) at 33MHz
- Low active programming current: 15mA (max.)
- Low active erase current: 15mA (max.)
- Low standby current: 10uA (max.)
- Deep power-down mode 1uA (typical)
- Minimum 100,000 erase/program cycles

Software Features

- Input Data Format
- 1-byte Command code
- Block Lock protection
- The BP0~BP1 status bit defines the size of the area to be software protected against Program and Erase instructions.
- Auto Erase and Auto Program Algorithm
- Automatically erases and verifies data at selected sector
- Automatically programs and verifies data at selected page by an internal algorithm that automatically times the program pulse widths (Any page to be programed should have page in the erased state first)
- Status Register Feature
- Electronic Identification
- JEDEC 2-byte Device ID
- RES command, 1-byte Device ID

Hardware Features

- SCLK Input
- Serial clock input
- SI Input
- Serial Data Input
- SO Output
- Serial Data Output
- WP# pin
- Hardware write protection
- HOLD# pin pause the chip without diselecting the chip
- PACKAGE
- 8-pin SOP (150mil)
- All Pb-free devices are RoHS Compliant

8. 16MX16 BIT SYNCHRONOUS DRAM (SDRAM)

8.1 General Description

The EM63A165 SDRAM is a high-speed CMOS synchronous DRAM containing 256 Mbits. It is internally configured as 4 Banks of 2M word x 16 DRAM with a synchronous interface (all signals are registered on the positive edge of the clock signal, CLK). Read and write accesses to the SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of a BankActivate command which is then followed by a Read or Write command. The EM63A165 provides for programmable Read or Write burst lengths of 1, 2, 4, 8, or full page, with a burst termination option. An auto precharge function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst sequence. The refresh functions, either Auto or Self Refresh are easy to use. By having a programmable mode register, the system can choose the most suitable modes to maximize its performance. These devices are well suited for applications requiring high memory bandwidth and particularly well suited to high performance PC applications.

8.2 Features

Fast access time from clock: 5/5.4 ns
• Fast clock rate: 166/143 MHz
• Fully synchronous operation
• Internal pipelined architecture
• 4M word x 16-bit x 4-bank
• Programmable Mode registers
  - CAS Latency: 2, or 3
  - Burst Length: 1, 2, 4, 8, or full page
  - Burst Type: interleaved or linear burst
  - Burst stop function
• Auto Refresh and Self Refresh
• 8192 refresh cycles/64ms
• CKE power down mode
• Single +3.3V power supply
• Interface: LVTTL
• 54-pin 400 mil plastic TSOP II package
  - Pb free and Halogen free

9. SAW FILTER

9.1 IF Filter for Audio Applications – Epcos K9656M

9.1.1 Standarts

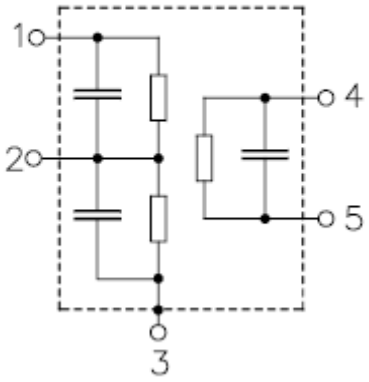
- B/G
- D/K
- I
- L/L’

9.1.2 Features

- TV IF audio filter with two channels
- Channel 1 (L') with one pass band for sound carriers at 40,40 MHz (L') and 39,75 MHz (L'- NICAM)
- Channel 2 (B/G,D/K,L,I) with one pass band for sound carriers between 32,35 MHz and 33,40 MHz

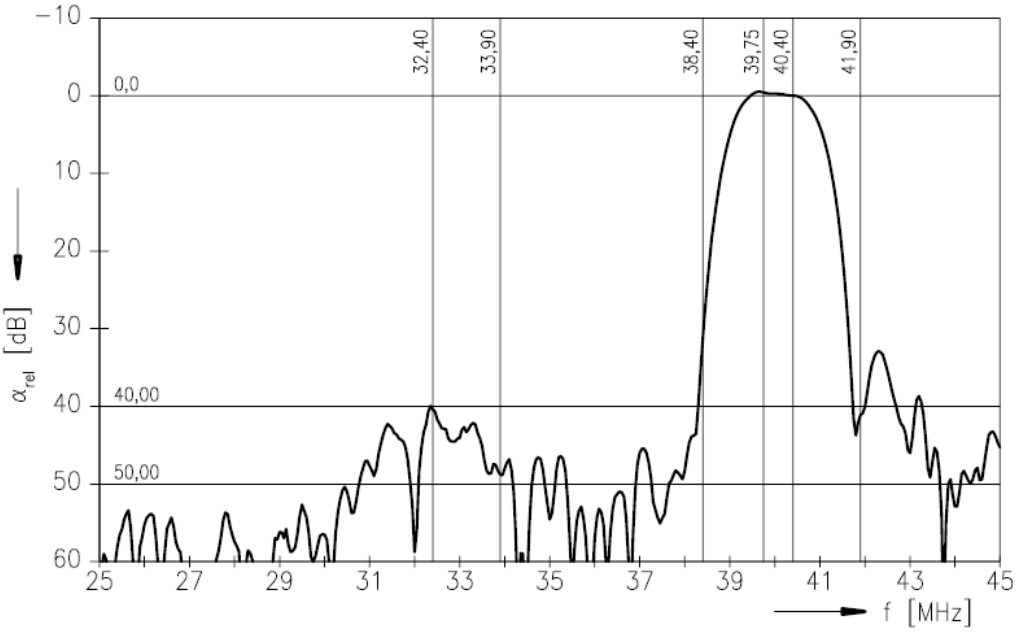
9.1.3 Pin Configuration

1 Input
2 Switching input
3 Chip carrier - ground
4 Output
5 Output

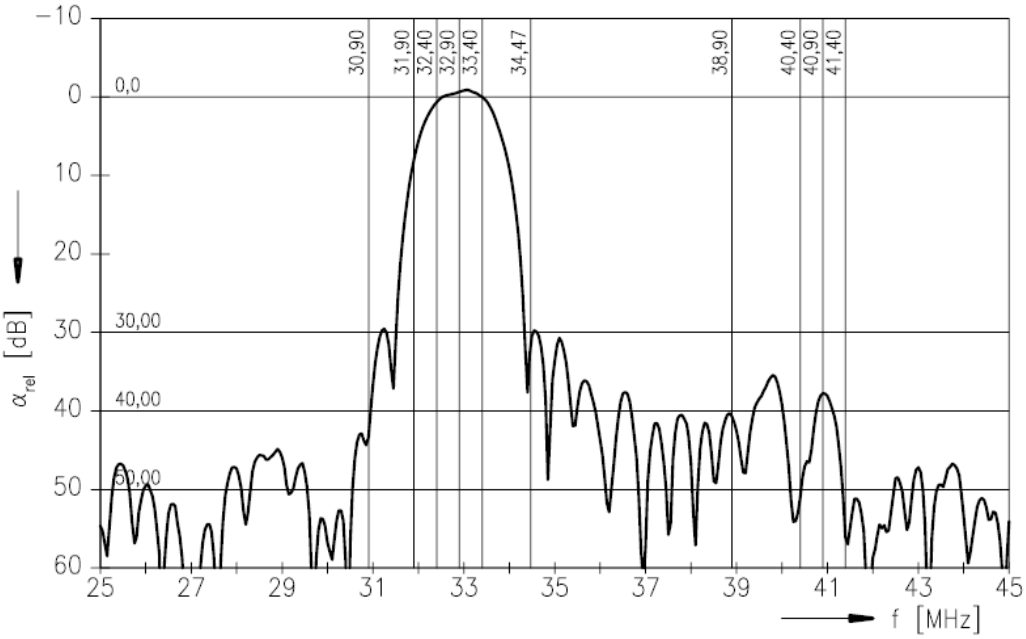


9.1.4 Frequency Response

Frequency Response of Channel 1:



Frequency Response of Channel 2:



9.2 IF Filter for Video Applications – Epcos K3958M

9.2.1 Standarts

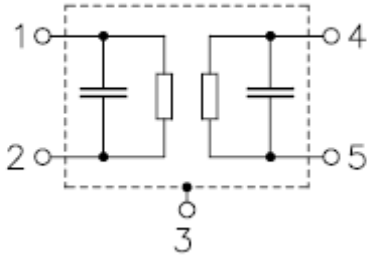
- B/G
- D/K
- I
- L/L'

9.2.2 Features

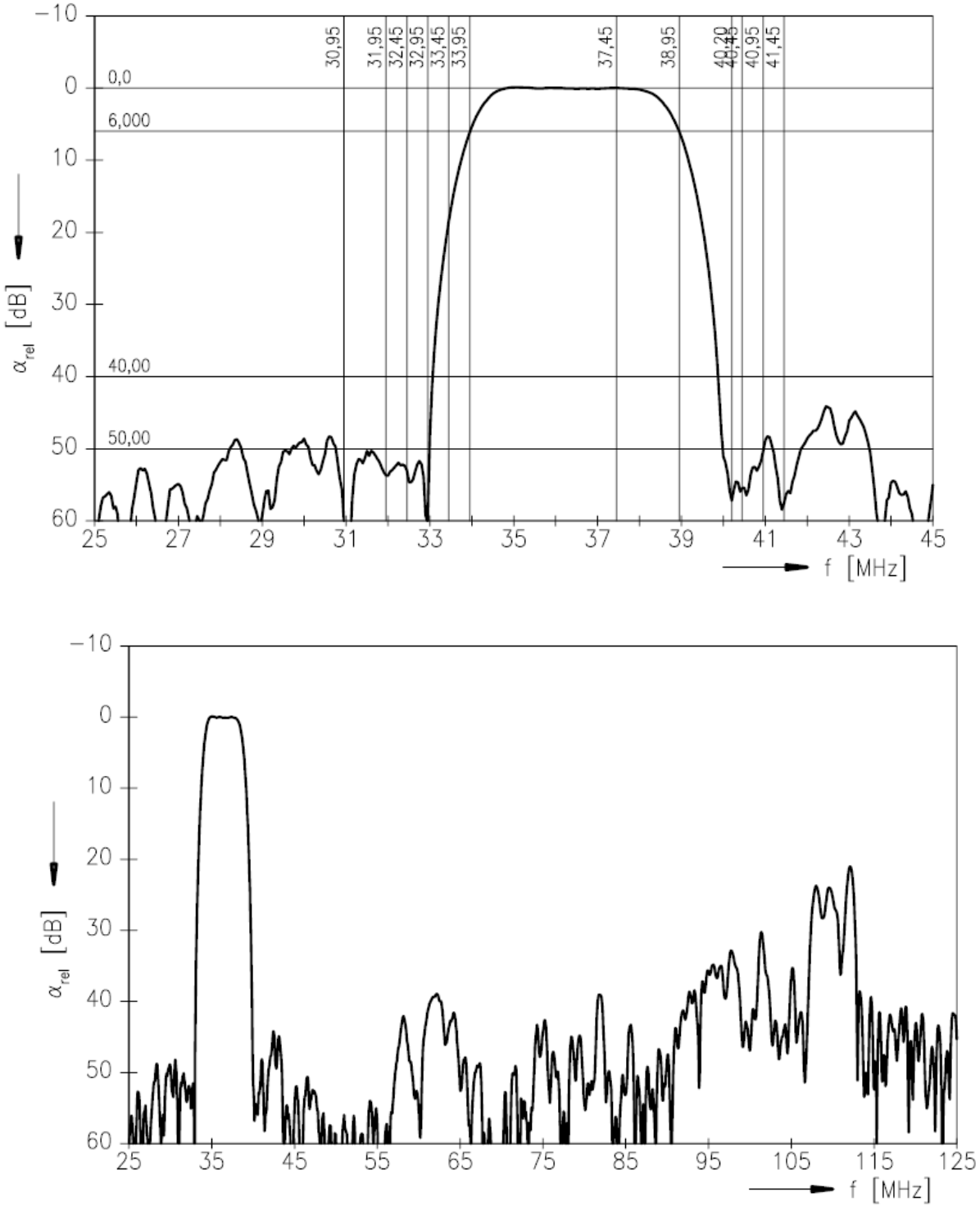
- TV IF filter with Nyquist slopes at 33.90 MHz and 38.90 MHz
- Constant group delay

9.2.3 Pin Configuration

1 Input
2 Input - ground
3 Chip - carrier ground
4 Output
5 Output



9.2.4 Frequency Response



10. POWER STAGE

The DC voltages required at various parts of the chassis and inverters are provided by an external power supply unit or produced on the chassis if an adapter is used for the supply. The 12V dc voltage is switched by IRF 7314 power mosfet in TV sets with mechanical switch to produce the required standby voltage. Also regulators and mosfets generate 1.8V, 3.3V and 5V and 1.26V voltages for other different parts of the chassis.

11. IC SPECIFICATIONS

11.1 32K Smart Serial EEPROM – 24C32

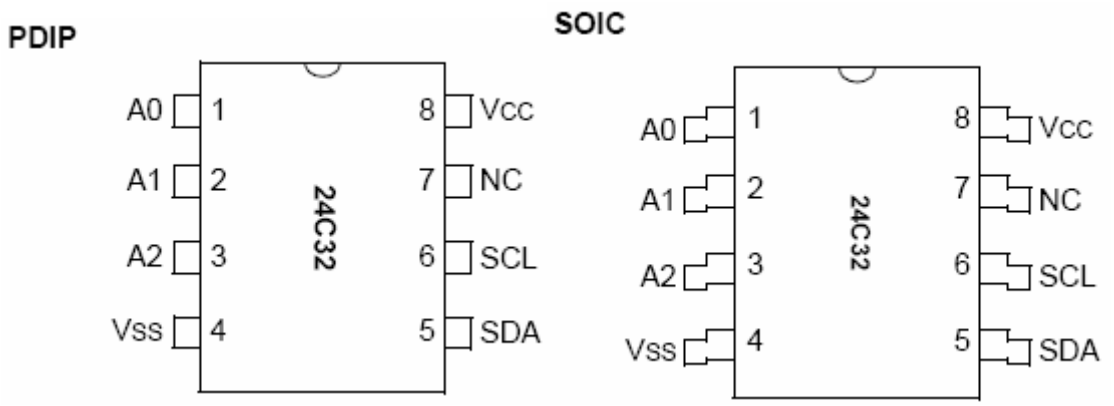
General Description

The Microchip Technology Inc. 24C32 is a 4K x 8 (32K bit) Serial Electrically Erasable PROM. This device has been developed for advanced, low power applications such as personal communications or data acquisition. The 24C32 features an input cache for fast write loads with a capacity of eight 8-byte pages, or 64 bytes. It also features a fixed 4K-bit block of ultra-high endurance memory for data that changes frequently. The 24C32 is capable of both random and sequential reads up to the 32K boundary. Functional address lines allow up to eight 24C32 devices on the same bus, for up to 256K bits address space. Advanced CMOS technology makes this device ideal for low-power non-volatile code and data applications. The 24C32 is available in the standard 8-pin plastic DIP and 8-pin surface mount SOIC package.

Features

- Voltage operating range: 4.5V to 5.5V
- Peak write current 3 mA at 5.5V
- Maximum read current 150 µA at 5.5V
- Standby current 1 µA typical
- Industry standard two-wire bus protocol, I2C compatible
- Including 100 kHz and 400 kHz modes
- Self-timed write cycle (including auto-erase)
- Power on/off data protection circuitry
- Endurance: 10,000,000 Erase/Write cycles guaranteed for High Endurance Block, 1,000,000 E/W cycles guaranteed for Standard Endurance Block
- 8 byte page, or byte modes available
- 1 page x 8 line input cache (64 bytes) for fast write loads
- Schmitt trigger, filtered inputs for noise suppression
- Output slope control to eliminate ground bounce
- 2 ms typical write cycle time, byte or page
- Up to 8 chips may be connected to the same bus for up to 256K bits total memory
- Electrostatic discharge protection > 4000V
- Data retention > 200 years
- 8-pin PDIP/SOIC packages
- Temperature ranges: Commercial (C): 0°C to +70°C, Industrial (I): -40°C to +85°C

Pin Configuration



Name	Function
A0,A1,A2	User Configurable Chip Selects
Vss	Ground
SDA	Serial Address/Data I/O
SCL	Serial Clock
Vcc	+4.5V to 5.5V Power Supply
NC	**No Internal Connection**

11.2 TL062

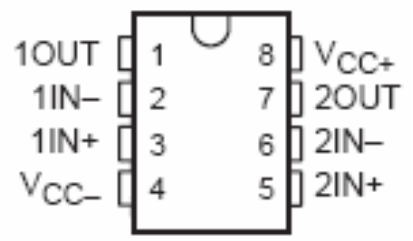
General Description

Low-power JFET-input operational amplifier

Features

- Very Low Power Consumption
- Typical Supply Current . . . 200 μA (Per Amplifier)
- Wide Common-Mode and Differential Voltage Ranges
- Low Input Bias and Offset Currents
- Common-Mode Input Voltage Range Includes VCC+
- Output Short-Circuit Protection
- High Input Impedance . . . JFET-Input Stage
- Internal Frequency Compensation
- Latch-Up-Free Operation
- High Slew Rate . . . 3.5 V/μs Typ

Pin Configuration



11.3 PI5V330

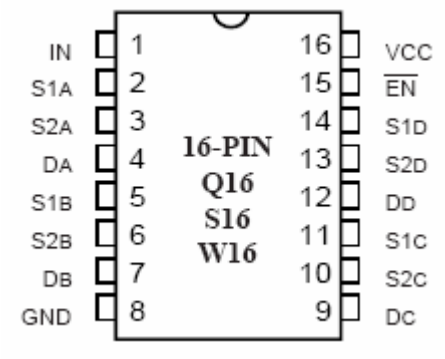
General Description

Pericom Semiconductor.s PI5V series of mixed signal video circuits are produced in the Company.s advanced CMOS low-power technology, achieving industry leading performance. The PI5V330 is a true bidirectional Quad 2-channel multiplexer/demultiplexer that is recommended for both RGB and composite video switching applications. The VideoSwitch. can be driven from a current output RAMDAC or voltage output composite video source. Low ON-resistance and wide bandwidth make it ideal for video and other applications. Also this device has exceptionally high current capability which is far greater than most analog switches offered today. A single 5V supply is all that is required for operation. The PI5V330 offers a high-performance, low-cost solution to switch between video sources. The application section describes the PI5V330 replacing the HC4053 multiplier and buffer/amplifier.

Features

- High-performance, low-cost solution to switch between video sources
- Wide bandwidth: 200 MHz
- Low ON-resistance: 3Ω
- Low crosstalk at 10 MHz: .58 dB
- Ultra-low quiescent power (0.1 µA typical)
- Single supply operation: +5.0V
- Fast switching: 10 ns
- High-current output: 100 mA
- Packages available:
- 16-pin 300-mil wide plastic SOIC (S)
- 16-pin 150-mil wide plastic SOIC (W)
- 16-pin 150-mil wide plastic QSOP (Q)

Pin Configuration



Pin Name	Description
$S1_A$, $S2_A$ $S1_B$, $S2_B$ $S1_C$, $S2_C$ $S1_D$, $S2_D$	Analog Video I/O
IN	Select Input
$\overline{EN}$	Enable
D_A, D_B, D_C, D_D	Analog Video I/O
GND	Ground
V_{CC}	Power

11.4 74HCT4053

General Description

The 74HC4053; 74HCT4053 is a high-speed Si-gate CMOS device and is pin compatible with the HEF4053B. It is specified in compliance with JEDEC standard no. 7A. The 74HC4053; 74HCT4053 is triple 2-channel analog multiplexer/demultiplexer with a common enable input (E). Each multiplexer/demultiplexer has two independent inputs/outputs (nY0 and nY1), a common input/output (nZ) and three digital select inputs (Sn). With E LOW, one of the two switches is selected (low-impedance ON-state) by S1 to S3. With E HIGH, all switches are in the high-impedance OFF-state, independent of S1 to S3. VCC and GND are the supply voltage pins for the digital control inputs (S1 to S3 and E). The VCC to GND ranges are 2.0 V to 10.0 V for 74HC4053 and 4.5 V to 5.5 V for 74HCT4053. The analog inputs/outputs (nY0 and nY1, and nZ) can swing between VCC as a positive limit and VEE as a negative limit. VCC - VEE may not exceed 10.0 V.
For operation as a digital multiplexer/demultiplexer, VEE is connected to GND (typically ground).

Features

- Low ON resistance:
- 80 W (typical) at VCC - VEE = 4.5 V
- 70 W (typical) at VCC - VEE = 6.0 V
- 60 W (typical) at VCC - VEE = 9.0 V
- Logic level translation:
- To enable 5 V logic to communicate with ±5 V analog signals
- Typical ‘break before make’ built in
- Complies with JEDEC standard no. 7A
- ESD protection: HBM EIA/JESD22-A114-C exceeds 2000 V, MM EIA/JESD22-A115-A exceeds 200 V
- Multiple package options
- Specified from -40 °C to +85 °C and from -40 °C to +125 °C

Pin Configuration

Symbol	Pin	Description
2Y1	1	2 independent input/output 1
2Y0	2	2 independent input/output 0
3Y1	3	3 independent input/output 1
3Z	4	3 common input/output
3Y0	5	3 independent input/output 0
$\overline{E}$	6	enable input (active LOW)
V_{EE}	7	negative supply voltage
GND	8	ground (0 V)
S3	9	select input 3
S2	10	select input 2
S1	11	select input 1
1Y0	12	1 independent input/output 0
1Y1	13	1 independent input/output 1
1Z	14	1 common input/output
2Z	15	2 common input/output
V_{CC}	16	supply voltage

11.5 FMS6145

General Description

The FMS6145 Low-Cost Video Filter (LCVF) is intended to replace passive LC fi lters and drivers with a low-cost integrated device. Five 4th-order fi lters provide improved image quality compared to typical 2nd or 3rd-order passive solutions. The FMS6145 may be directly driven by a DC-coupled DAC output or an AC-coupled signal. Internal diode clamps and bias circuitry may be used if AC-coupled inputs are required. The outputs can drive AC- or DC-coupled single (150Ω) or dual (75Ω) loads. DC coupling the outputs removes the need for output coupling capacitors. The input DC levels are offset approximately +280mV at the output.

Features

- Five 4th-order 8MHz (SD) fi lters
- Drives single,AC- or DC-coupled, video loads (2Vpp, 150Ω)
- Drives dual, AC- or DC-coupled, video loads (2Vpp, 75Ω)
- Transparent input clamping
- AC- or DC-coupled inputs
- AC- or DC-coupled outputs
- DC-coupled outputs eliminate AC-coupling capacitors
- 5V only
- Robust 8kV ESD protection
- Lead-free TSSOP-14 package

Pin Configuration

Pin #	Name	Type	Description
1	IN1	Input	Video input, channel 1
2	IN2	Input	Video input, channel 2
3	IN3	Input	Video input, channel 3
4	V_{CC}	Input	+5V supply, do not float
5	IN4	Input	Video input, channel 4
6	IN5	Input	Video input, channel 5
7, 8	NC		No Connect
9	OUT5	Output	Filtered video output, channel 5
10	OUT4	Output	Filtered video output, channel 4
11	GND	Output	Must be tied to ground, do not float
12	OUT3	Output	Filtered video output, channel 3
13	OUT2	Output	Filtered video output, channel 2
14	OUT1	Output	Filtered video output, channel 1

11.6 LM1117

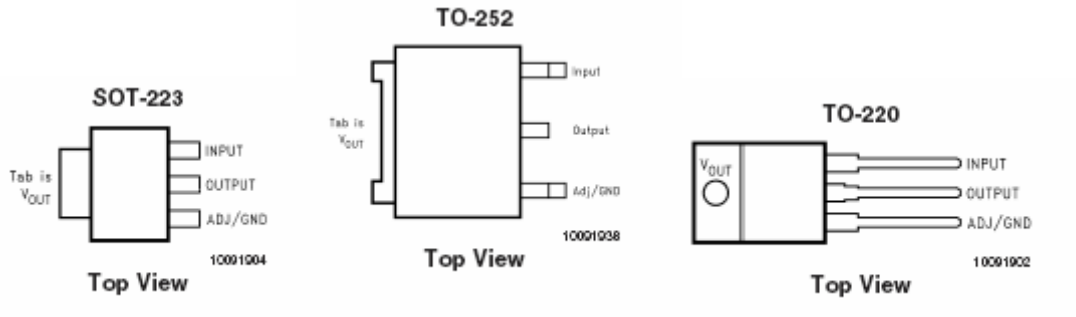
General Description

The LM1117 is a series of low dropout voltage regulators with a dropout of 1.2V at 800mA of load current. It has the same pin-out as National Semiconductor's industry standard LM317. The LM1117 is available in an adjustable version, which can set the output voltage from 1.25V to 13.8V with only two external resistors. In addition, it is also available in five fixed voltages, 1.8V, 2.5V, 2.85V, 3.3V, and 5V. The LM1117 offers current limiting and thermal shutdown. Its circuit includes a zener trimmed bandgap reference to as-sure output voltage accuracy to within ±1%. The LM1117 series is available in SOT- 223, TO-220, and TO-252 D-PAK packages. A minimum of 10μF tantalum capacitor is required at the output to improve the transient response and stability.

Features

- Available in 1.8V, 2.5V, 2.85V, 3.3V, 5V, and Adjustable Versions
- Space Saving SOT-223 Package
- Current Limiting and Thermal Protection
- Output Current 800mA
- Line Regulation 0.2% (Max)
- Load Regulation 0.4% (Max)
- Temperature Range
- LM1117 0°C to 125°C
- LM1117I -40°C to 125°C

Pin Configuration



11.7 ST24LC21

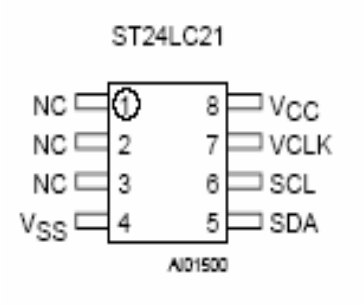
Description

The ST24LC21 is a 1K bit electrically erasable programmable memory (EEPROM), organized by 8 Bits.This device can operate in two modes: Transmit Only mode and I2C bidirectional mode. When powered, the device is in Transmit Only mode with EEPROM data clocked out from the rising edge of the signal applied on VCLK. The device will switch to the I2C bidirectional mode upon the falling edge of the signal applied on SCL pin. The ST24LC21 cannot switch from the I2C bidirectional mode to the Transmit Only mode (except when the power supply is removed). The device operates with a power supply value as low as 2.5V. Both Plastic Dual-in-Line and Plastic Small Outline packages are available.

Features

- 1 Mıllıon Erase/Wrıte Cycles
- 40 Years Data Retentıon
- 2.5v To 5.5v Sıngle Supply Voltage
- 400k Hz Compatıbılıty Over The Full
- Range Of Supply Voltage
- Two Wıre Serıal Interface I2c Bus
- Compatıble
- Page Wrıte (Up To 8 Bytes)
- Byte, Random And Sequentıal Read
- Modes
- Self Tımed Programmıng Cycle
- Automatıc Address Incrementıng
- Enhanced Esd/Latch Up
- Performances

Pin Configuration



SDA	Serial Data Address Input/Output
SCL	Serial Clock (I^2C mode)
V_{CC}	Supply Voltage
V_{SS}	Ground
VCLK	Clock Transmit only mode
WC	Write Control

11.8 24LC02

Description

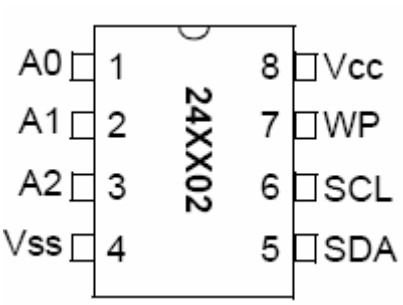
The Microchip Technology Inc. 24AA02/24LC02B (24XX02*) is a 2 Kbit Electrically Erasable PROM. The device is organized as one block of 256 x 8-bit memory with a 2-wire serial interface. Low-voltage design permits operation down to 1.8V, with standby and active currents of only 1 □A and 1 mA, respectively. The 24XX02 also has a page write capability for up to 8 bytes of data. The 24XX02 is available in the standard 8-pin PDIP, surface mount OIC, TSSOP and MSOP packages and is also available in the 5-lead SOT-23 package.

Features

• Single supply with operation down to 1.8V
• Low-power CMOS technology
- 1 mA active current typical
- 1μA standby current typical (I-temp)
• Organized as 1 block of 256 bytes (1 x 256 x 8)
• 2-wire serial interface bus, I2C™ compatible
• Schmitt Trigger inputs for noise suppression
• Output slope control to eliminate ground bounce
• 100 kHz (24AA02) and 400 kHz (24LC02B) compatibility
• Self-timed write cycle (including auto-erase)
• Page write buffer for up to 8 bytes
• 2 ms typical write cycle time for page write
• Hardware write-protect for entire memory
• Can be operated as a serial ROM
• Factory programming (QTP) available
• ESD protection > 4,000V
• 1,000,000 erase/write cycles
• Data retention > 200 years
• 8-lead PDIP, SOIC, TSSOP and MSOP packages
• 5-lead SOT-23 package
• Pb-free finish available
• Available for extended temperature ranges:

- Industrial (I): -40°C to +85°C
- Automotive (E): -40°C to +125°C

Pin Configuration



Name	Description
A0	Not Connected
A1	Not Connected
A2	Not Connected
Vss	Ground
SDA	Serial Address/Data I/O
SCL	Serial Clock
WP	Write-Protect Input
Vcc	+1.8V to 5.5V Power Supply

11.9 MAX810

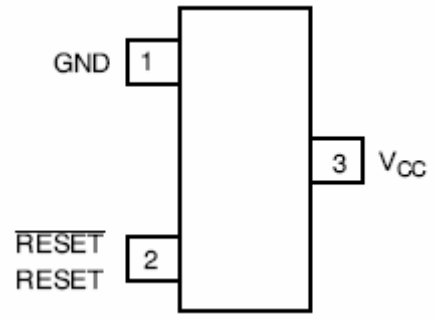
General Description

The MAX809 and MAX810 are cost-effective system supervisor circuits designed to monitor VCC in digital systems and provide a reset signal to the host processor when necessary. No external components are required. The reset output is driven active within 10 _sec of VCC falling through the reset voltage threshold. Reset is maintained active for a timeout period which is trimmed by the factory after VCC rises above the reset threshold. The MAX810 has an active-high RESET output while the MAX809 has an active-low RESET output. Both devices are available in SOT-23 and SC-70 packages. The MAX809/810 are optimized to reject fast transient glitches on the VCC line. Low supply current of 0.5 _A (VCC = 3.2 V) makes these devices suitable for battery powered applications.

Features

- Precision VCC Monitor for 1.5 V, 2.5 V, 3.0 V, 3.3 V, and 5.0 V Supplies
- Precision Monitoring Voltages from 1.2 V to 4.9 V Available in 100 mV Steps
- Four Guaranteed Minimum Power-On Reset Pulse Width Available (1 ms, 20 ms, 100 ms, and 140 ms)
- RESET Output Guaranteed to VCC = 1.0 V.
- Low Supply Current
- Compatible with Hot Plug Applications
- VCC Transient Immunity
- No External Components
- Wide Operating Temperature: -40°C to 105°C
- Pb-Free Packages are Available

Pin Configuration



11.10 TDA1308

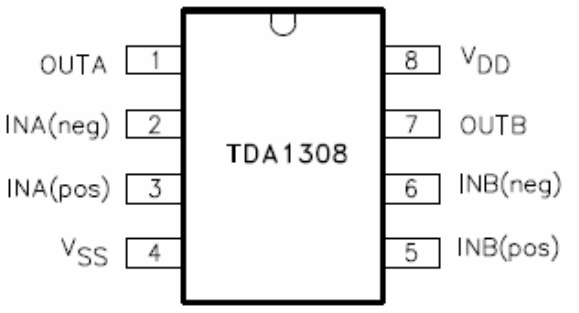
Description

The TDA1308 is an integrated class AB stereo headphone driver contained in an SO8 or a DIP8 plastic package. The device is fabricated in a 1 mm CMOS process and has been primarily developed for portable digital audio applications.

Features

- Operating temperature range: -40 to +85 C
- No switch ON/OFF clicks
- Short-circuit resistant
- signal-to-noise ratio: 110 dB
- total harmonic distortion: 0.001 %

Pin Configuration



SYMBOL	PIN	DESCRIPTION
OUTA	1	output A
INA(neg)	2	inverting input A
INA(pos)	3	non-inverting input A
V_{SS}	4	negative supply
INB(pos)	5	non-inverting input B
INB(neg)	6	inverting input B
OUTB	7	output B
V_{DD}	8	positive supply

11.11 MP1583

General Description

The MP1583 is a step-down regulator with a built in internal Power MOSFET. It achieves 3A continuous output current over a wide input supply range with excellent load and line regulation. Current mode operation provides fast transient response and eases loop stabilization. Fault condition protection includes cycle-by-cycle current limiting and thermal

shutdown. Adjustable soft-start reduces the stress on the input source at turn-on. In shutdown mode the regulator draws 20μA of supply current.
The MP1583 requires a minimum number of readily available external components to complete a 3A step down DC to DC converter solution.

Features

- 3A Output Current
- Programmable Soft-Start
- 100mΩ Internal Power MOSFET Switch
- Stable with Low ESR Output Ceramic Capacitors
- Up to 95% Efficiency
- 20μA Shutdown Mode
- Fixed 385KHz frequency
- Thermal Shutdown
- Cycle-by-Cycle Over Current Protection
- Wide 4.75 to 23V operating Input Range
- Output Adjustable From 1.22 to 21V
- Under Voltage Lockout
- Available in 8 pin SOIC Package
- 3A Evaluation Board Available

Pin Configuration

#	Name	Description
1	BS	High-Side Gate Drive Boost Input. BS supplies the drive for the high-side n-channel MOSFET switch. Connect a 4.7nF or greater capacitor from SW to BS to power the high side switch.
2	IN	Power Input. IN supplies the power to the IC, as well as the step-down converter switches. Drive IN with a 4.75V to 23V power source. Bypass IN to GND with a suitably large capacitor to eliminate noise on the input to the IC. See *Input Capacitor*
3	SW	Power Switching Output. SW is the switching node that supplies power to the output. Connect the output LC filter from SW to the output load. Note that a capacitor is required from SW to BS to power the high-side switch.
4	GND	Ground. (Note: Connect the exposed pad on backside to Pin 4).
5	FB	Feedback Input. FB senses the output voltage to regulate that voltage. Drive FB with a resistive voltage divider from the output voltage. The feedback threshold is 1.222V. See *Setting the Output Voltage*
6	COMP	Compensation Node. COMP is used to compensate the regulation control loop. Connect a series RC network from COMP to GND to compensate the regulation control loop. In some cases, an additional capacitor from COMP to GND is required. See *Compensation*
7	EN	Enable Input. EN is a digital input that turns the regulator on or off. Drive EN high to turn on the regulator, drive it low to turn it off. For automatic startup, leave EN unconnected.
8	SS	Soft Start Control Input. SS controls the soft start period. Connect a capacitor from SS to GND to set the soft-start period. A 0.1μF capacitor sets the soft-start period to 10ms. To disable the soft-start feature, leave SS unconnected.

11.12 MP2112

General Description

The MP2112 is a 1MHz constant frequency, current mode, PWM step-down converter. The device integrates a main switch and a synchronous rectifier for high efficiency without an external Schottky diode. It is ideal for powering portable equipment that powered by a single cell Lithium-Ion (Li+) battery. The MP2112 can supply 1A of load current from a 2.5V to 6V input voltage. The output voltage can be regulated as low as 0.6V. The MP2112 can also run at 100% duty cycle for low dropout applications.
The MP2112 is available in a space-saving 6-pin QFN package.

Features

- High Efficiency: Up to 95%
- 1MHz Constant Switching Frequency
- 1A Available Load Current
- 2.5V to 6V Input Voltage Range
- Output Voltage as Low as 0.6V
- 100% Duty Cycle in Dropout
- Current Mode Control
- Short Circuit Protection
- Thermal Fault Protection
- <0.1μA Shutdown Current
- Space Saving 3mm x 3mm QFN6 Package

Pin Configuration

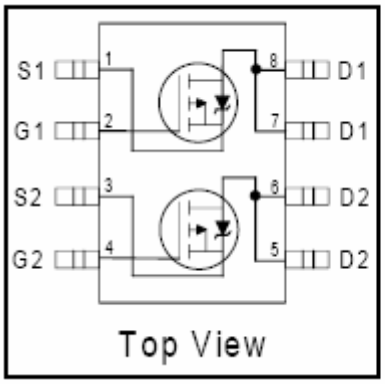
Pin #	Name	Description
1	FB	Feedback Input. Connect FB to the center point of the external resistor divider. The feedback threshold voltage is 0.6V.
2	GND	Ground.
3	SW	Power Switch Output. Inductor connection to drains of the internal PFET and NFET switches.
4	VINB	Supply Input-Power.
5	VINA	Supply Input-Analog.
6	EN	Enable Input.

11.13 IRF7314

General Description

Fifth Generation HEXFETs from International Rectifier utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET Power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications. The SO-8 has been modified through a customized leadframe for enhanced thermal characteristics and multiple-die capability making it ideal in a variety of power applications. With these improvements, multiple devices can be used in an application with dramatically reduced board space. The package is designed for vapor phase, infra red, or wave soldering techniques.

Pin Configuration



V_{DSS} = -20V

$R_{DS(on)}$ = 0.058Ω

12. SERVICE MENU SETTINGS

In order to reach service menu, First Press **"MENU"** Then press the remote control code, which is **"4725"**. In DTV mode, first press **"MENU**" and select **"TV SETUP"**. Then, press **"4725"**.

12.1. Video Setup

Panel Info <.....>

32_LC_SAC1

Blue Background <.....>

*If "Menu" selected, **"Blue Background"** item is seen in **"Feature"** menu.*

*If "Yes" selected, **"Blue Background"** is on and not seen in **"Feature"** menu*

Film Mode <.....>

*If "Yes" selected, **"Film Mode"** feature is active.*

Dynamic Contrast <.....>

*If "Yes" selected, **"Dynamic Contrast"** feature is active.*

Game Mode <.....>

*If "Yes" selected, **"Game Mode"** feature is active*

SRGB For PC <.....>

If "Yes" selected, PCs can use SRGB option.

Dynamic Noise Reduction<.....>

*If "Yes" selected, **"Dynamic Noise Reduction"** feature is active*

WSS Option<.....>

If "Yes" selected, WSS Option can be used

12.2. AudioSetup

BG<.....>

Europe

New Zelland
Australia
No

DK<.....>
I<.....>
L<.....>
Equalizer <.....>
*If "Yes" selected, **"Equalizer"** item is seen in **"Sound"** menu.*
Headphone <.....>
*If "Yes" selected, **"Headphone"** item is seen in **"Sound"** menu.*
Power On/Off Melody <.....>
If "Yes" selected, when power on/off conditions, the power on/off melody can be heard.
Dynamic Bass <.....>*Value between 0 to 12*
Effect<.....> *Value between 0 to 7*
Audio Delay ,offset <.....> *Value between 0 to 190*
Audio Setup Cont...2
Carrier mute<.....> *Value between 0 to 28*
Headphone Sound Select <.....>
Always Active Select
Always Inactive Select
Menu
Always Main Menu
Always PIP/PAP Window
Sound Mode Detect Time <.....> *Value between 0 to 255*
Noise Reduction Threshold <.....> *Value between 0 to 255*
Noise Reduction Time <.....> *Value between 0 to 15*
AVL Attack Time <.....> *Value between 0 to 255*
AVL Release Time <.....> *Value between 0 to 255*
Prescales (AVL On)
FM Prescale<.....> *Value between 0 to 255*
AM Prescale <.....> *Value between 0 to 255*
NICAM Prescale <.....> *Value between 0 to 255*
SCART Prescale <.....> *Value between 0 to 255*
FAV Prescale <.....> *Value between 0 to 255*
DTV Prescale <.....> *Value between 0 to 255*
HDMI Prescale <.....> *Value between 0 to 255*
YPbPr/PC Prescale <.....> *Value between 0 to 255*
An. USB Prescale <.....> *Value between 0 to 255*
Dig. USB Prescale <.....> *Value between 0 to 255*
Prescales (AVL Off)
FM Prescale<.....> *Value between 0 to 255*
AM Prescale <.....> *Value between 0 to 255*
NICAM Prescale <.....> *Value between 0 to 255*
SCART Prescale <.....> *Value between 0 to 255*
FAV Prescale <.....> *Value between 0 to 255*
DTV Prescale <.....> *Value between 0 to 255*
HDMI Prescale <.....> *Value between 0 to 255*
YPbPr/PC Prescale <.....> *Value between 0 to 255*

An. USB Prescale <.....> *Value between 0 to 255*
Dig. USB Prescale <.....> *Value between 0 to 255*

Clipping Levels (AVL On)

FM Clipping <.....> *Value between 0 to 255*
AM Clipping <.....> *Value between 0 to 255*
NICAM Clipping <.....> *Value between 0 to 255*
SCART Clipping <.....> *Value between 0 to 255*
FAV Clipping <.....> *Value between 0 to 255*
DTV Clipping <.....> *Value between 0 to 255*
HDMI Clipping <.....> *Value between 0 to 255*
YPbPr/PC Clipping <.....> *Value between 0 to 255*
An. USB Clipping <.....> *Value between 0 to 255*
Dig. USB Clipping <.....> *Value between 0 to 255*

Clipping Levels (AVL Off)

FM Clipping <.....> *Value between 0 to 255*
AM Clipping <.....> *Value between 0 to 255*
NICAM Clipping <.....> *Value between 0 to 255*
SCART Clipping <.....> *Value between 0 to 255*
FAV Clipping <.....> *Value between 0 to 255*
DTV Clipping <.....> *Value between 0 to 255*
HDMI Clipping <.....> *Value between 0 to 255*
YPbPr/PC Clipping <.....> *Value between 0 to 255*
An. USB Clipping <.....> *Value between 0 to 255*
Dig. USB Clipping <.....> *Value between 0 to 255*

12.3. Service Scan/Tuning Setup

First Search for L/L' <.....>
ATS Delay Time (ms) <.....> *Value between 0 to +200*
Main Tuner Setup

Tuner Type

LC_TDTC_GXX1D
Thomson DTT7543X
Philips TD1318AF-3
Samsung DTOs403LH172A
Generic (Analog Only)

Control Byte <.....> *Value between 0 to +255*
BSW1 <.....> *Value between 0 to +255*
BSW2 <.....> *Value between 0 to +255*
BSW3 <.....> *Value between 0 to +255*
Low-Mid – Low Byte <.....>
Low-Mid – High Byte <.....>
Mid-High – Low Byte <.....>
Mid-High – High Byte <.....>

S Band TOP <.....>
VIF TOP <.....> *Value between 0 to +15*
VIF TOP SECAM <.....> *Value between 0 to +15*
VIF TOP DK<.....> *Value between 0 to +15*
Synch Threshold<.....> *Value between 0 to +40*

16.4. Options

Options-1

Power Up

Standby

Last state

TV Open Mode

Source

1st TV

Last Tv

First APS <.....>

If "Yes" selected, first time TV opens by asking APS.

APS Volume <.....> *Value between 0 to +63*

Burn In Mode <.....>

If "Yes" selected, TV opens with Burn-In mode. This mode is used in manufacturing.

APS Test

Autostore <.....>

If "Yes" selected, Channel is automatically stored.

Unicode Enabled <.....>

If "Yes" selected,Unicode characters can be read in the USB Files.

Options-2

Source List menu <.....>

If "Yes" selected, Sorce List Menu appears on the screen when press "source" button.

RS232 for B2B <.....>

If "Yes" selected, Remote Control commandsthe TV via RS232 and vice versa.

RC Select <.....>

RC Group 1

RC Group 2

RC Group 3

RC Group 4

RC Group 5

RC Group 6

Double Digit Key <.....>

If "Yes" selected, Double Digit Button on RC activates.

Protection <.....>

If "Yes" selected,short circuit protection activates.

Led Type <.....>

1 Led 1 Color

1 Led 2 Color

2 Led 2 Color

1 Led 3 Color

2 Led 3 Color

200 Programme <.....>

If "Yes" selected, totaly 200 programmes can be used.

TouchPad <.....>

If "Yes" selected, TouchPad can be used.

Teletext Options

TXT Darkness <.....> *Value between 0 to +63*

TXT Type <.....>

- ***Fasttext&Toptext***
- ***No***
- ***Default***
- ***Fastext***
- ***Toptext***

TXT Language <.....>

- ***Menu***
- ***West***
- ***East***
- ***Cyrillic***
- ***Turk/Gre***
- ***Arabic***
- ***Persian***
- ***Auto***

No Txt Warning <.....>

If "Yes" selected, "No Txt Transmission" warning appears on the screen when pressing txt button from RC.

Txt Subtitle <.....>

If "Yes" selected, Teletext subtitles can be seen.

Optional Features

Default Zoom <.....>

- ***Menu***
- ***16:9***
- ***4:3***
- ***Panaromic***
- ***14:9 Zoom***

Menu Timeout <.....>

- ***Menu***
- ***15 Sec***
- ***30 Sec***
- ***60 Sec***
- ***No Time***

Backlight <.....>

If "Yes" selected, ***"Backlight"*** *feature is active.*

100 Step Slider <.....>

If "Yes" selected, 64 step sliders will become 100 step sliders.

Analog USB Enabled <.....>

If "Yes" selected, ***"Analog USB"*** *option is active.*

Menu Double Size <.....>

If "Yes" selected, menu sizes increases.

CEC Enable <.....>

If "Yes" selected, ***"CEC"*** *feature is active.*

Digital USB Hotplug <.....>

If "Yes" selected, ***"Digital USB Hotplug"*** *feature is active.*

PIP Options

Pip <.....>

AV PIP

No PIP

PC PIP

Hotel Options <.....>

Hotel TV <.....>

*If "Yes" selected, **"Hotel TV"** feature is active.*

IR Smartloader <.....>

*If "Yes" selected, **"IR Smartloader"** feature is active.*

16.5. External Source Settings

TV <.....>
DTV <.....>
Ext 2 <.....>
Ext 2 S <.....>
FAV <.....>
BAV <.....>
S-Video <.....>
HDMI 1 <.....>
HDMI 2 <.....>
HDMI 3 <.....>
HDMI 4 <.....>
YPbPr <.....>
PC <.....>

16.6. Preset

User Ad.j
ADC Adj.
Service Adj.
All Adj.
Init Factory Channels.

16.7. NVM Edit

NVM-edit addr. (hex)
NVM-edit data (hex)
NVM-data dec

16.8. Programming

HDMI DDC Update Mode <.....>
HDCP Key Update Mode <.....>
Software Bypass <.....>

If "On" selected, speaker effects are bypassed.

LVDS Clock Step <.....> *Value between 0 to +255*
Memory Clock Step <.....> *Value between 0 to +255*
DTV Download <.....>

If "On" selected, DTV software can be updated from SCART.

DSUB9 Download <.....>

If "On" selected, DTV software can be updated from DSUB9.

16.9. Diagnostic

Eeprom I2C
Tuner I2C
IF I2C
HDMI I2C
DTV RS232

16.10. Product Info

13. SOFTWARE UPDATE DESCRIPTION

13.1 17MB25 Analog Part Software Update With Bootloader Procedure

1.1 The File Types Used By The Bootloader

All file types that used by the bootloader software are listed below:

1. The Binary File : It has ".bin" extension and it is the tv application. Its size is 1920 Kb.

2. The Config Binary File : It has ".cin extension and it is the config of the tv application. Its size may be 64 Kb or a few times 64 Kb.

3. The Test Script File : It has ".txt" extension and it is the test script that is parsed and executed by the bootloader. It don't have to be any times of 64 Kb.

4. The Test Binary File : It has ".tin" extension and it is used and written by the test groups. It is run to understand the problem part of the hardware.

Alltough a file that is used by the bootloader can be had any one of these extensions, its name has to be "VESTEL_S" and it has to be located in the root directory of the usb device.

1.2 Usage of The Bootloader

1. The starting to pass through : The chassis is only powered up.
2. The starting to download something : When chassis is powered up the menu key has to be pushed.Before the chassis is powered up and if any usb device is plugged to the usb port, the programme is downloaded from usb firstly.

Any usb device is plugged to usb port , user must open hyperterminal in the pc and connect pc to chassis via Mstar debug tool and any one of scart,dsub9 or I2c connectors. Serial connection settings are listed below:

- Bit per second: 115200
- Data bits: 8

- Parity: None
- Stop bits: 1
- Flow control: None

In this case the bootloader sofware puts “C” character to uart. After repeating “C” characters are seen in the hyperterminal user can send any file to chassis by selecting Transfer -> Send File menu item and choosing “**1K Xmodem**” from protocol section.

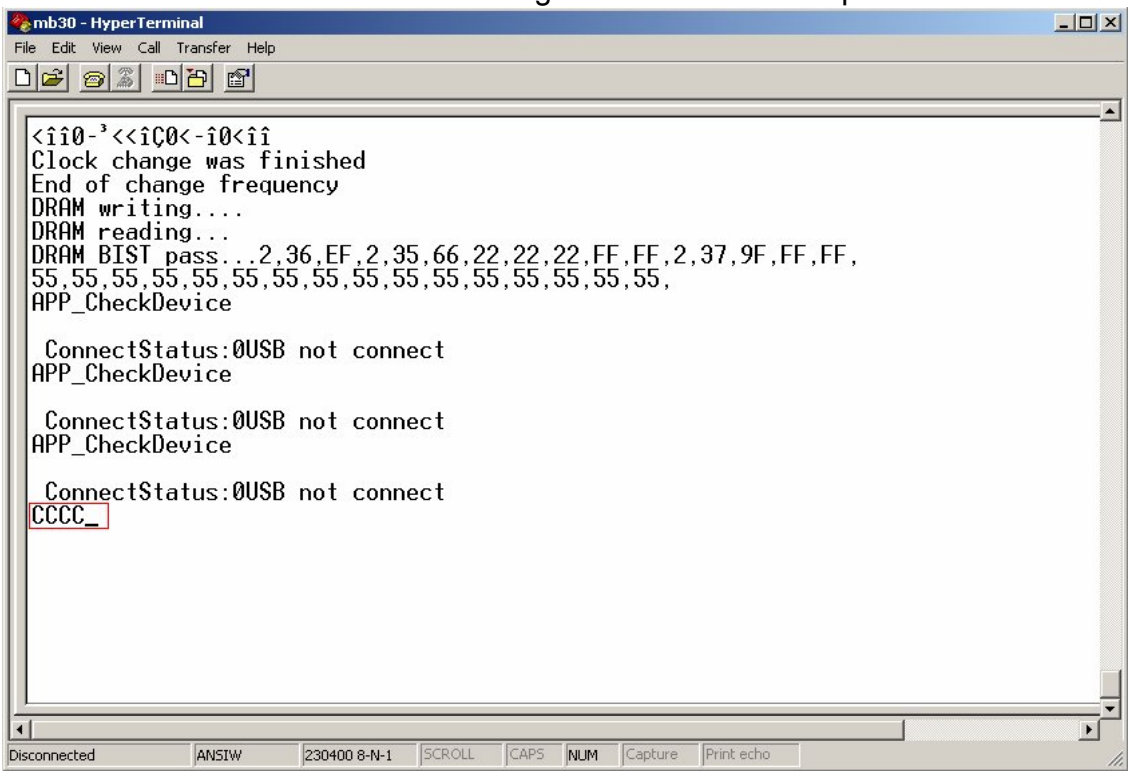


Figure 1. The Sample Output Before Sending The File

2. EEProm update

To Update eeprom content via uart scart,dsub9 or i2c with Mstar tool can used.
Serial connection settings are listed below:

- Bit per second: 9600
- Data bits: 8
- Parity: None
- Stop bits: 1
- Flow control: None

Programming menu item is choosed in the service menu and switch “HDCP Key Update Mode” from off to on.

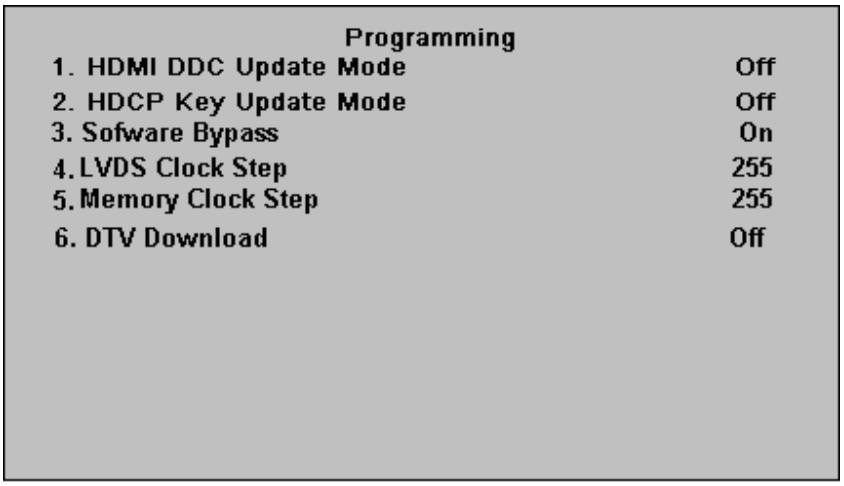


Figure 2. The Programming Service Menu

After then you must see Xmodem menu in the hyperterminal.To download hdcp key press k or to download eeprom content press w.

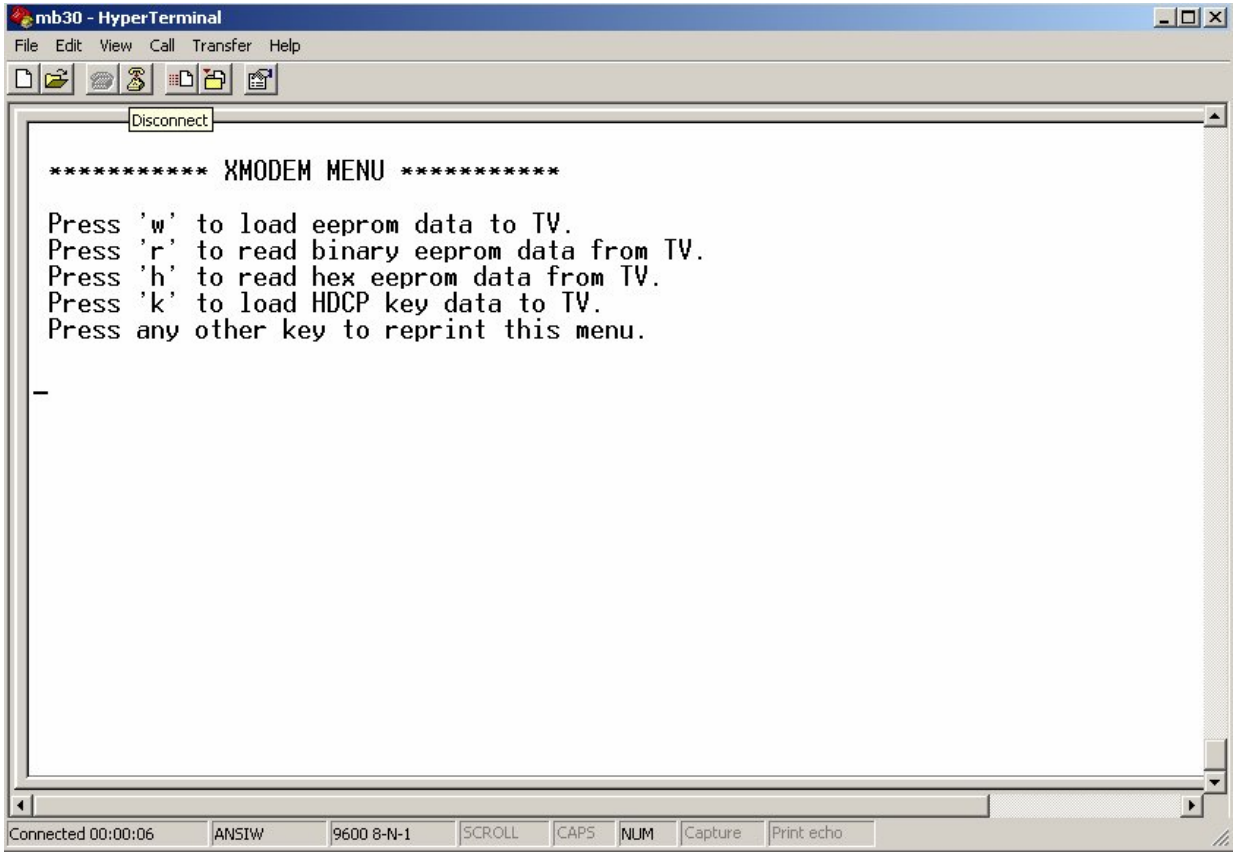


Figure 3. Xmodem Menu

If the repeated “C” characters are seen you can transfer file content via select Transfer->Send File and choose “**Xmodem”** protocol and click the “Send” button.

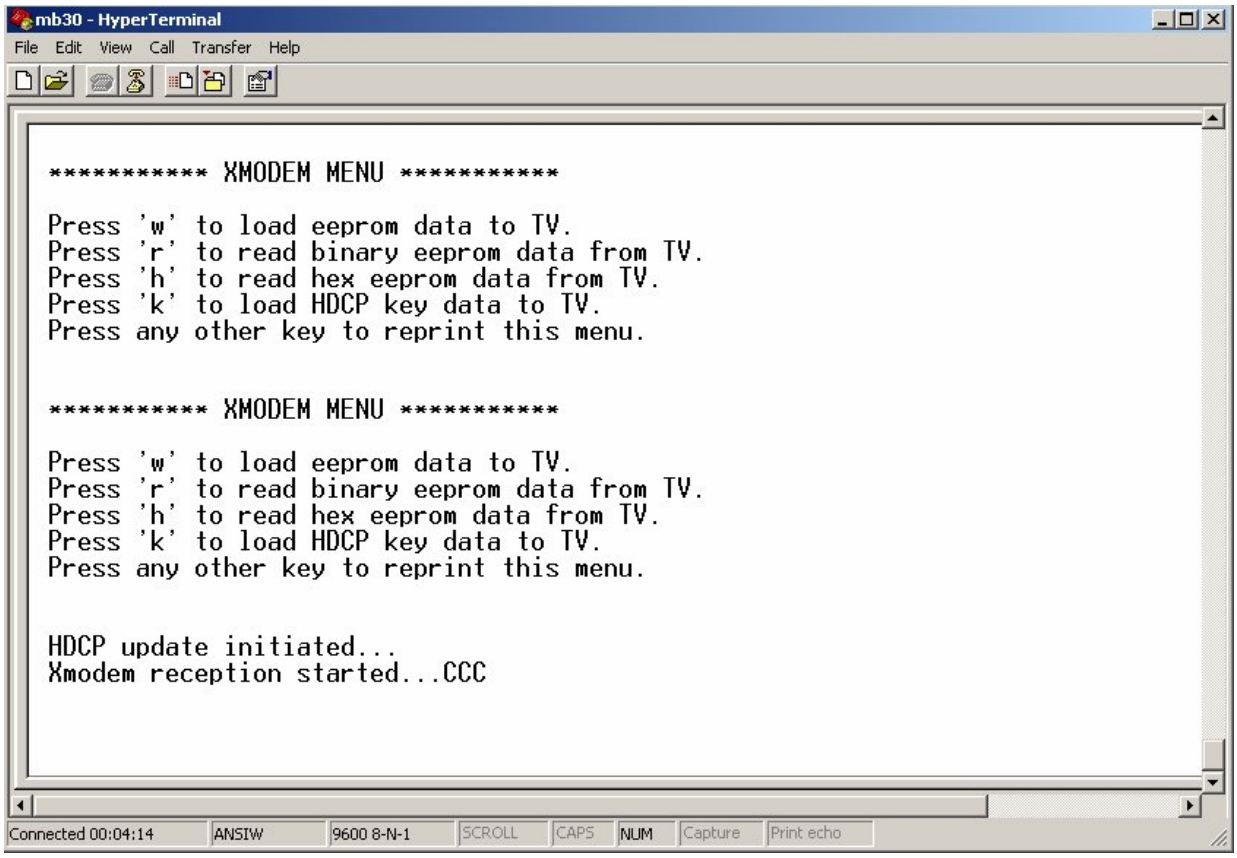


Figure 4. The Starting To Send

16.2 17MB25 HDCP key upload procedure.

1) Turn on TV set.
2) Open a COM connection using fallowing parameters and select ISP COM Port No

Baud Rate: 9600 bps
Data Bits: 8
Stop Bits: 1
Parity: None
Flow Control: None

3) Enter service menu by pressing “4” “7” “2” 5” consecutively while main menu is open
4) Select “9. Programming”
5) Select “HDMI HDCP Update Mode” yes.
6) On Hyper Terminal Window press “k”
7) Click on send file under Transfer Tab.
8) Select Xmodem and choose the HDCP key to be uploaded.
9) Press send button
10) Restart TV set

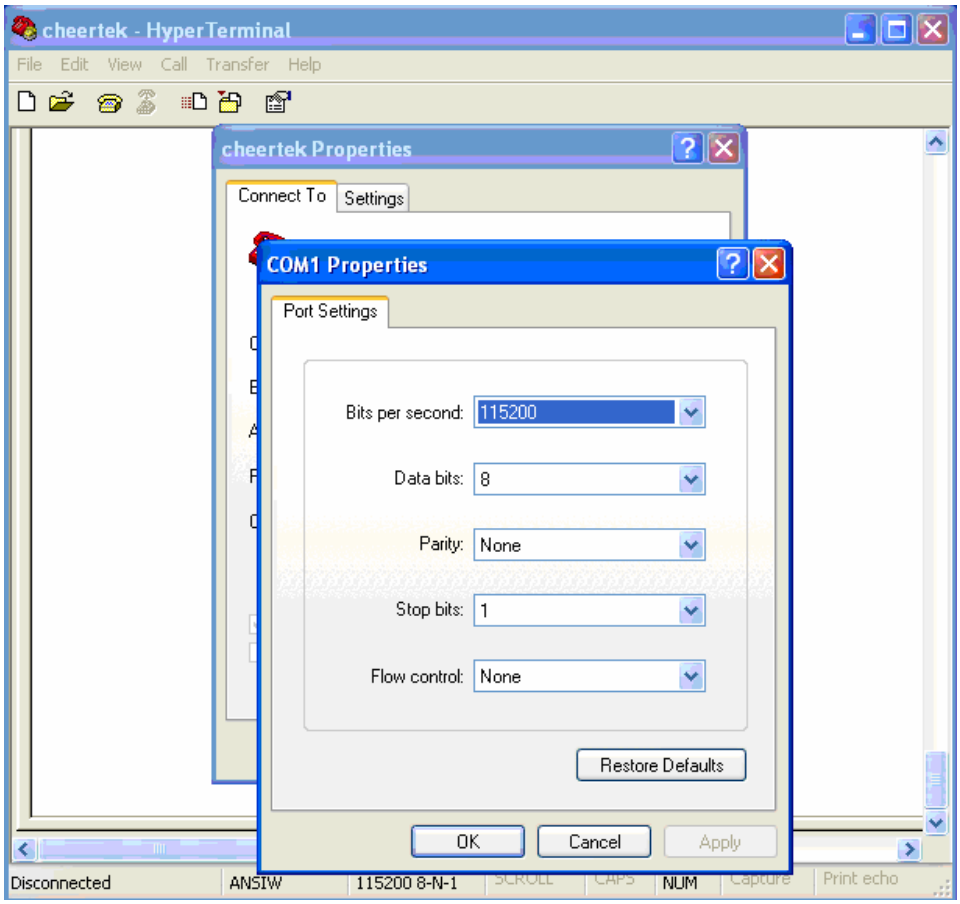
13.3 17MB25 Digital Software Update From SCART

Adjusting DTV Download Mode:

1. Power on the TV.
2. Exit the Stby Mode.
3. Enter the “Tv Menu”.
4. Enter “4725” for jumping to “Service Settings”.
5. Select “8. Programming” step.
6. Change “6. DTV Download” to “On”.
7. Switch to the Stby mode.

Adjusting HyperTerminal:

1. Connect the “MB25 SCART Interface” to SCART1 (bottom SCART plug).
2. Also connect the “MB25 SCART Interface” to PC.
3. Open “HyperTerminal”.
4. Determine the “COM” settings listed and showed below.
   - Bit per second: 115200
   - Data bits: 8
   - Parity: None
   - Stop bits: 1
   - Flow control: None

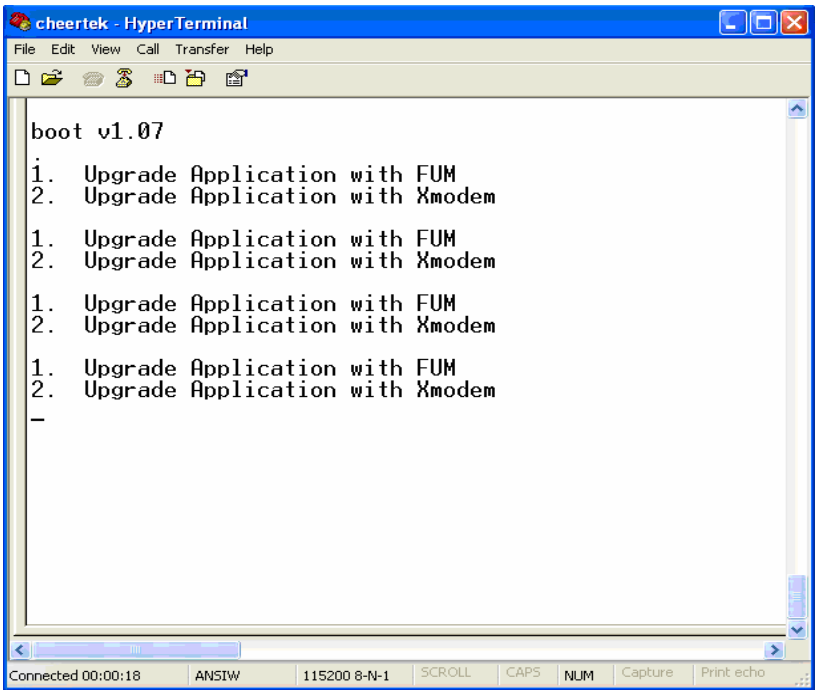


COM Properties Window

6. Click “OK”.

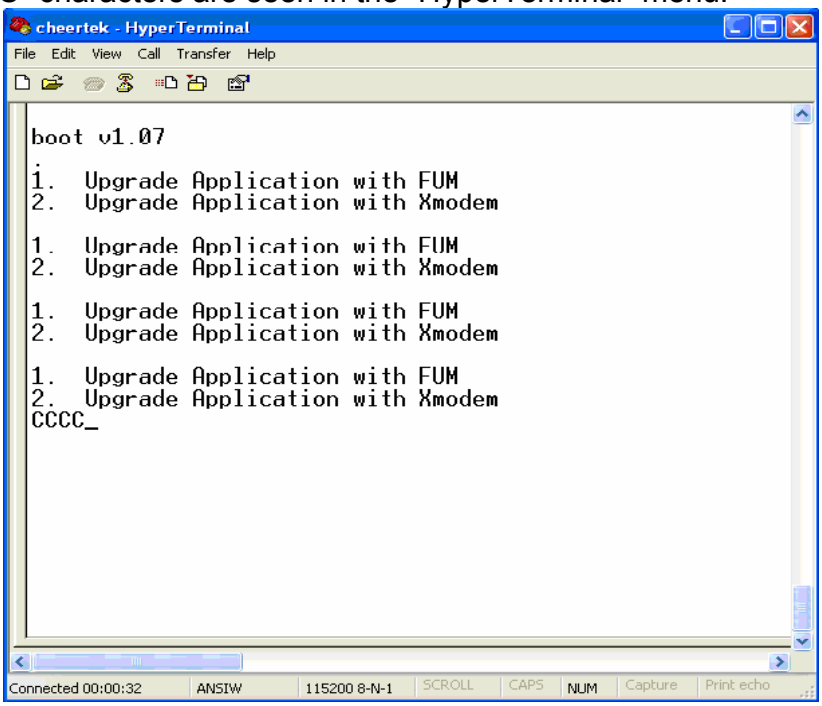
Software Updating Procedure

1. In the HyperTerminal Menu, click the “Connect” button.
2. Exit the Stby Mode.
3. The “Space” button on the keyboard must be pressed, when the following window can be seen.



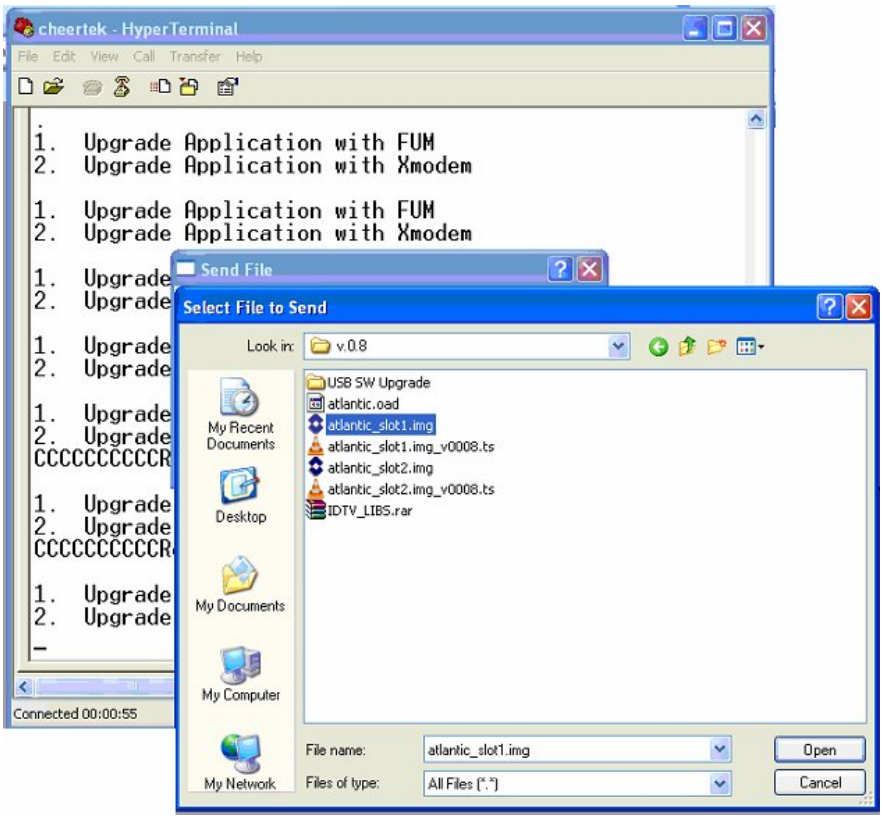
Selection Window

4. Press the “2” button on the keyboard for choosing “2. Upgrade Application with Xmodem”.
5. Repeating “C” characters are seen in the “HyperTerminal” menu.

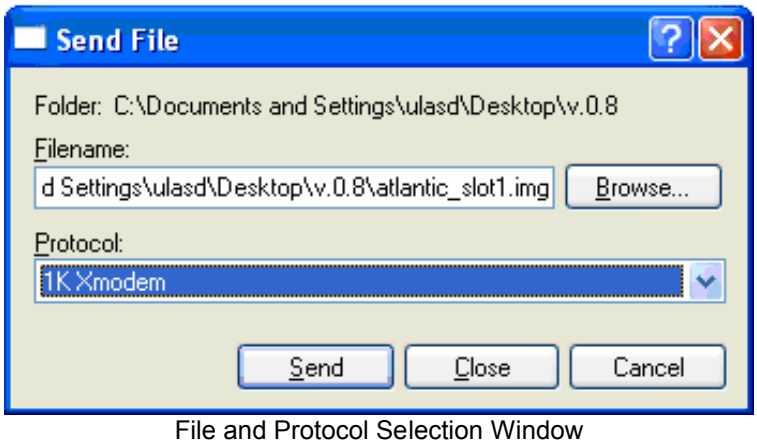


The Sample Output Before Sending The File

6. Click the “Send” button on the HyperTerminal
7. Select the “Filename **xxxx**_slot1.img” using “Browse”.
8. Choose the “1K Xmodem” from “Protocol” option.

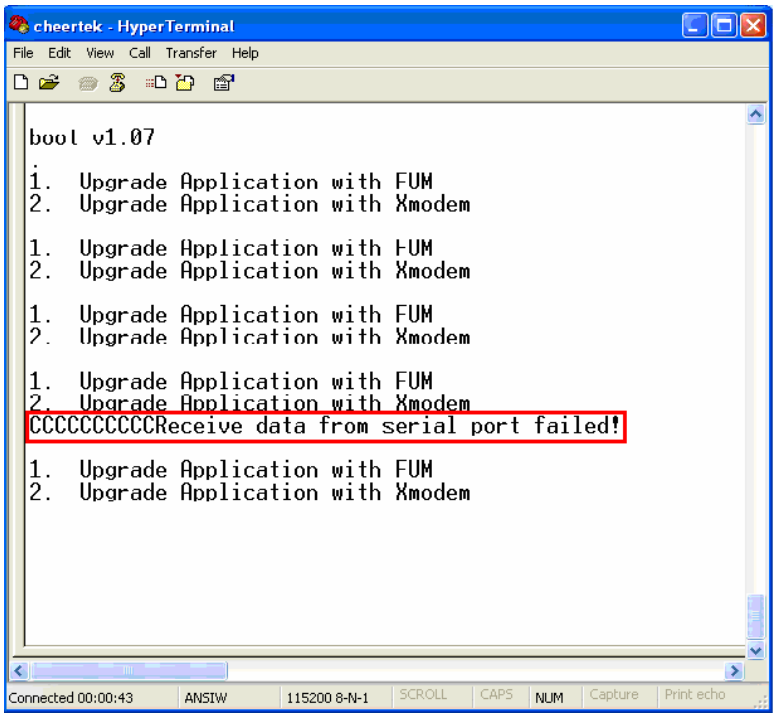


Selection of File



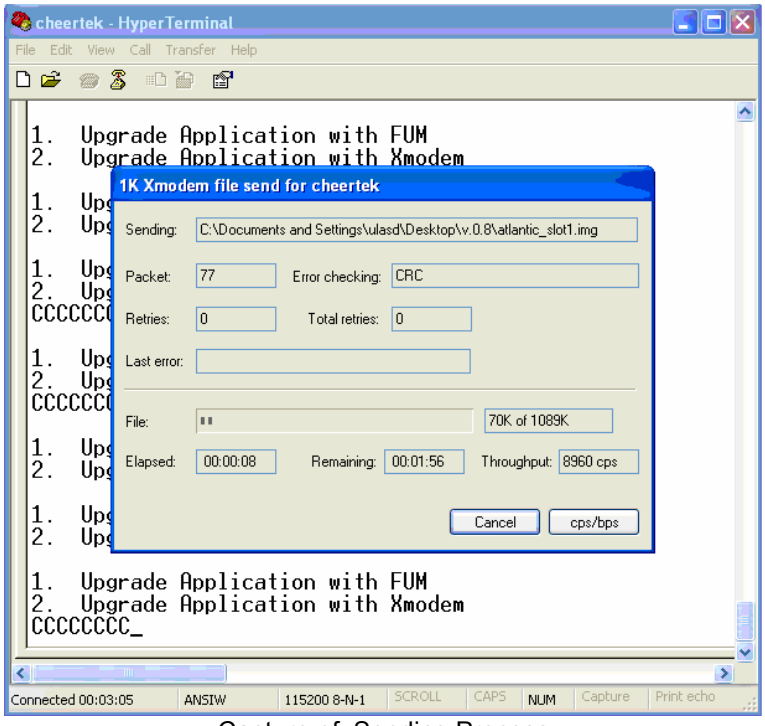
File and Protocol Selection Window

Note: In the Software updating Procedure section, when the first “C” character is seen, the filename selection process must be finished before 10 seconds. If the process can not be finished, the file sending operation will be cancelled. The following figure shows this situation.



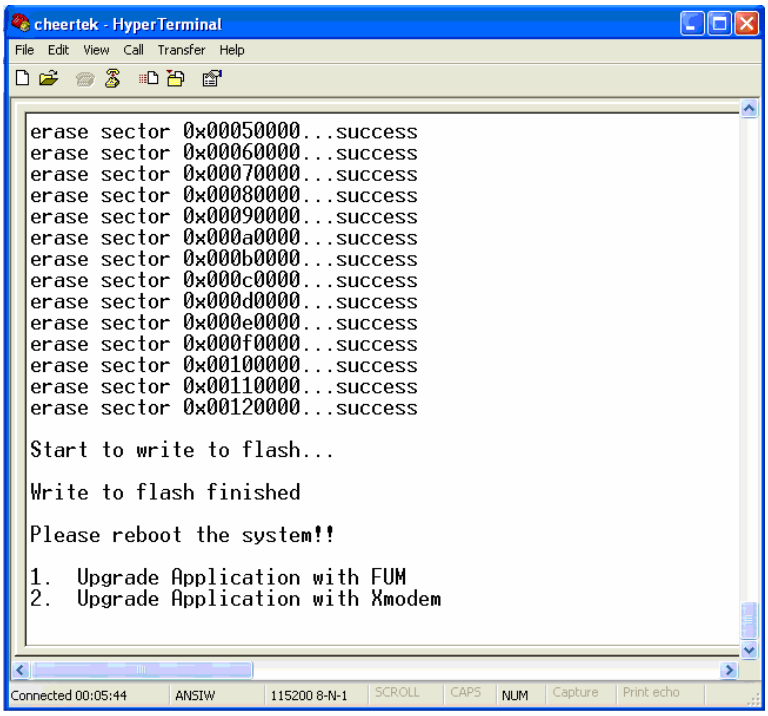
Capture of Receving Data Failing

9. When sending the file the following window must be seen.



Capture of Sending Process

10. After the sending process the following HyperTerminal window must be seen.

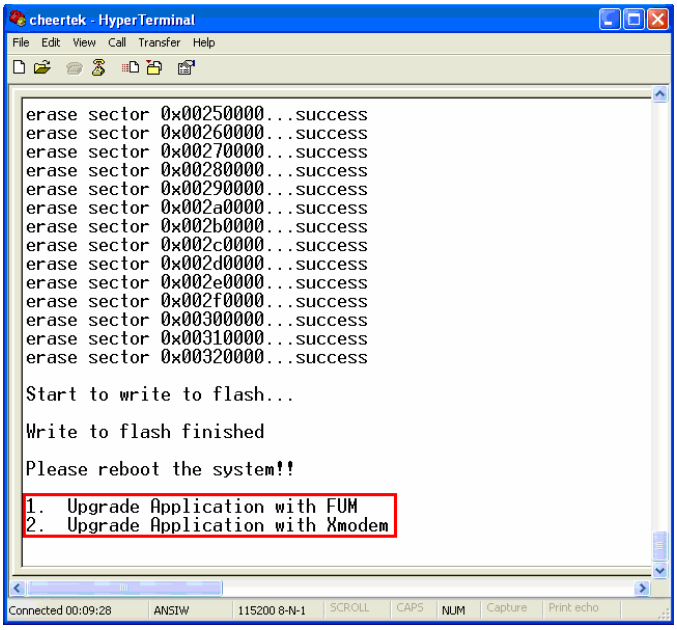


Capture of End of The Sending Process

11. For sending second program file, the Software Updating Procedure must be repeated from the step **X**. Select the “Filename **xxxx**_slot2.img” using “Browse”.
12. After sending the second program file, the Software Updating Procedure will be succesful.

Note: After the File Sending Process,

1. Upgrade Application with FUM
2. Upgrade Application with Xmodem, options must be seen.



End of The Sending Process

Checking Of The New Software

1. Turn off and on the TV.
2. Enter the “Setup” submenu in the “DTV Menu”.
3. Choose the “Configuration” option.
4. For controlling new software, check the “Receiver Upgrade” option.

13.4 17MB25 Digital Software Update From USB

Software upgrade is possible via USB disk by folowing the steps below.

1. Copy the bin file, including higher version than the software loaded in flash, into the USB flash memory root directory. This file should be named up.bin.
2. Insert the USB disk.
3. Digital module performs version and CRC check. If version and CRC check is successful, then a message prompt appears to notify user about new version. If the user confirms loading of new version, upgrade.bin file is written into flash unused slot.
4. Digital module disables the previous software in the flash and then a system reset is performed.
5. After the reset, digital module starts with new software.

Revert operation:

With revert operation, it is possible to *downgrade* the software.
Revert operation is very similar to upgrade process. In the revert operation, file name should be f_up.bin. Also user confirmation is not asked.

1. Copy the bin file into the USB flash memory root directory. This file should be named force_upgrade.bin.
2. Insert the USB disk.
3. A lower version than the software in flash can be loaded with revert operation. Digital module performs only CRC check. If CRC check is successful, then force_upgrade.bin file is written into flash unused slot.
4. Digital module disables the previous software in the flash.
5. A message prompt is displayed to notify user about end of revert process.
6. Power off/on is required to start digital module with the new software.

For controlling new software, check the “Receiver Upgrade” option.

New Zelland
Australia
No

DK<.....>
I<.....>
L<.....>
Equalizer <.....>
*If "Yes" selected, **"Equalizer"** item is seen in **"Sound"** menu.*
Headphone <.....>
*If "Yes" selected, **"Headphone"** item is seen in **"Sound"** menu.*
Power On/Off Melody <.....>
If "Yes" selected, when power on/off conditions, the power on/off melody can be heard.
Dynamic Bass <.....>*Value between 0 to 12*
Effect<.....> *Value between 0 to 7*
Audio Delay ,offset <.....> *Value between 0 to 190*
Audio Setup Cont...2
Carrier mute<.....> *Value between 0 to 28*
Headphone Sound Select <.....>
Always Active Select
Always Inactive Select
Menu
Always Main Menu
Always PIP/PAP Window
Sound Mode Detect Time <.....> *Value between 0 to 255*
Noise Reduction Threshold <.....> *Value between 0 to 255*
Noise Reduction Time <.....> *Value between 0 to 15*
AVL Attack Time <.....> *Value between 0 to 255*
AVL Release Time <.....> *Value between 0 to 255*
Prescales (AVL On)
FM Prescale<.....> *Value between 0 to 255*
AM Prescale <.....> *Value between 0 to 255*
NICAM Prescale <.....> *Value between 0 to 255*
SCART Prescale <.....> *Value between 0 to 255*
FAV Prescale <.....> *Value between 0 to 255*
DTV Prescale <.....> *Value between 0 to 255*
HDMI Prescale <.....> *Value between 0 to 255*
YPbPr/PC Prescale <.....> *Value between 0 to 255*
An. USB Prescale <.....> *Value between 0 to 255*
Dig. USB Prescale <.....> *Value between 0 to 255*
Prescales (AVL Off)
FM Prescale<.....> *Value between 0 to 255*
AM Prescale <.....> *Value between 0 to 255*
NICAM Prescale <.....> *Value between 0 to 255*
SCART Prescale <.....> *Value between 0 to 255*
FAV Prescale <.....> *Value between 0 to 255*
DTV Prescale <.....> *Value between 0 to 255*
HDMI Prescale <.....> *Value between 0 to 255*
YPbPr/PC Prescale <.....> *Value between 0 to 255*

An. USB Prescale <.....> *Value between 0 to 255*
Dig. USB Prescale <.....> *Value between 0 to 255*

Clipping Levels (AVL On)

FM Clipping <.....> *Value between 0 to 255*
AM Clipping <.....> *Value between 0 to 255*
NICAM Clipping <.....> *Value between 0 to 255*
SCART Clipping <.....> *Value between 0 to 255*
FAV Clipping <.....> *Value between 0 to 255*
DTV Clipping <.....> *Value between 0 to 255*
HDMI Clipping <.....> *Value between 0 to 255*
YPbPr/PC Clipping <.....> *Value between 0 to 255*
An. USB Clipping <.....> *Value between 0 to 255*
Dig. USB Clipping <.....> *Value between 0 to 255*

Clipping Levels (AVL Off)

FM Clipping <.....> *Value between 0 to 255*
AM Clipping <.....> *Value between 0 to 255*
NICAM Clipping <.....> *Value between 0 to 255*
SCART Clipping <.....> *Value between 0 to 255*
FAV Clipping <.....> *Value between 0 to 255*
DTV Clipping <.....> *Value between 0 to 255*
HDMI Clipping <.....> *Value between 0 to 255*
YPbPr/PC Clipping <.....> *Value between 0 to 255*
An. USB Clipping <.....> *Value between 0 to 255*
Dig. USB Clipping <.....> *Value between 0 to 255*

16.3. Service Scan/Tuning Setup

First Search for L/L' <.....>
ATS Delay Time (ms) <.....> *Value between 0 to +200*
Main Tuner Setup

Tuner Type

LC_TDTC_GXX1D
Thomson DTT7543X
Philips TD1318AF-3
Samsung DTOs403LH172A
Generic (Analog Only)

Control Byte <.....> *Value between 0 to +255*
BSW1 <.....> *Value between 0 to +255*
BSW2 <.....> *Value between 0 to +255*
BSW3 <.....> *Value between 0 to +255*
Low-Mid – Low Byte <.....>
Low-Mid – High Byte <.....>
Mid-High – Low Byte <.....>
Mid-High – High Byte <.....>

S Band TOP <.....>
VIF TOP <.....> *Value between 0 to +15*
VIF TOP SECAM <.....> *Value between 0 to +15*
VIF TOP DK<.....> *Value between 0 to +15*
Synch Threshold<.....> *Value between 0 to +40*

16.4. Options

Options-1

Power Up

Standby

Last state

TV Open Mode

Source

1st TV

Last Tv

First APS <.....>

If "Yes" selected, first time TV opens by asking APS.

APS Volume <.....> *Value between 0 to +63*

Burn In Mode <.....>

If "Yes" selected, TV opens with Burn-In mode. This mode is used in manufacturing.

APS Test

Autostore <.....>

If "Yes" selected, Channel is automatically stored.

Unicode Enabled <.....>

If "Yes" selected,Unicode characters can be read in the USB Files.

Options-2

Source List menu <.....>

If "Yes" selected, Sorce List Menu appears on the screen when press "source" button.

RS232 for B2B <.....>

If "Yes" selected, Remote Control commandsthe TV via RS232 and vice versa.

RC Select <.....>

RC Group 1

RC Group 2

RC Group 3

RC Group 4

RC Group 5

RC Group 6

Double Digit Key <.....>

If "Yes" selected, Double Digit Button on RC activates.

Protection <.....>

If "Yes" selected,short circuit protection activates.

Led Type <.....>

1 Led 1 Color

1 Led 2 Color

2 Led 2 Color

1 Led 3 Color

2 Led 3 Color

200 Programme <.....>

If "Yes" selected, totaly 200 programmes can be used.

TouchPad <.....>

If "Yes" selected, TouchPad can be used.

Teletext Options

TXT Darkness <.....> *Value between 0 to +63*

TXT Type <.....>

- ***Fasttext&Toptext***
- ***No***
- ***Default***
- ***Fastext***
- ***Toptext***

TXT Language <.....>

- ***Menu***
- ***West***
- ***East***
- ***Cyrillic***
- ***Turk/Gre***
- ***Arabic***
- ***Persian***
- ***Auto***

No Txt Warning <.....>

If "Yes" selected, "No Txt Transmission" warning appears on the screen when pressing txt button from RC.

Txt Subtitle <.....>

If "Yes" selected, Teletext subtitles can be seen.

Optional Features

Default Zoom <.....>

- ***Menu***
- ***16:9***
- ***4:3***
- ***Panaromic***
- ***14:9 Zoom***

Menu Timeout <.....>

- ***Menu***
- ***15 Sec***
- ***30 Sec***
- ***60 Sec***
- ***No Time***

Backlight <.....>

If "Yes" selected, ***"Backlight"*** *feature is active.*

100 Step Slider <.....>

If "Yes" selected, 64 step sliders will become 100 step sliders.

Analog USB Enabled <.....>

If "Yes" selected, ***"Analog USB"*** *option is active.*

Menu Double Size <.....>

If "Yes" selected, menu sizes increases.

CEC Enable <.....>

If "Yes" selected, ***"CEC"*** *feature is active.*

Digital USB Hotplug <.....>

If "Yes" selected, ***"Digital USB Hotplug"*** *feature is active.*

PIP Options

Pip <.....>

AV PIP

No PIP

PC PIP

Hotel Options <.....>

Hotel TV <.....>

*If "Yes" selected, **"Hotel TV"** feature is active.*

IR Smartloader <.....>

*If "Yes" selected, **"IR Smartloader"** feature is active.*

16.5. External Source Settings

TV <.....>
DTV <.....>
Ext 2 <.....>
Ext 2 S <.....>
FAV <.....>
BAV <.....>
S-Video <.....>
HDMI 1 <.....>
HDMI 2 <.....>
HDMI 3 <.....>
HDMI 4 <.....>
YPbPr <.....>
PC <.....>

16.6. Preset

User Ad.j
ADC Adj.
Service Adj.
All Adj.
Init Factory Channels.

16.7. NVM Edit

NVM-edit addr. (hex)
NVM-edit data (hex)
NVM-data dec

16.8. Programming

HDMI DDC Update Mode <.....>
HDCP Key Update Mode <.....>
Software Bypass <.....>

If "On" selected, speaker effects are bypassed.

LVDS Clock Step <.....> *Value between 0 to +255*
Memory Clock Step <.....> *Value between 0 to +255*
DTV Download <.....>

If "On" selected, DTV software can be updated from SCART.

DSUB9 Download <.....>

If "On" selected, DTV software can be updated from DSUB9.

16.9. Diagnostic

Eeprom I2C
Tuner I2C
IF I2C
HDMI I2C
DTV RS232

16.10. Product Info

17. SOFTWARE UPDATE DESCRIPTION

16.1 17MB25 Analog Part Software Update With Bootloader Procedure

1.1 The File Types Used By The Bootloader

All file types that used by the bootloader software are listed below:

1. The Binary File : It has ".bin" extension and it is the tv application. Its size is 1920 Kb.

2. The Config Binary File : It has ".cin extension and it is the config of the tv application. Its size may be 64 Kb or a few times 64 Kb.

3. The Test Script File : It has ".txt" extension and it is the test script that is parsed and executed by the bootloader. It don't have to be any times of 64 Kb.

4. The Test Binary File : It has ".tin" extension and it is used and written by the test groups. It is run to understand the problem part of the hardware.

Alltough a file that is used by the bootloader can be had any one of these extensions, its name has to be "VESTEL_S" and it has to be located in the root directory of the usb device.

1.2 Usage of The Bootloader

1. The starting to pass through : The chassis is only powered up.
2. The starting to download something : When chassis is powered up the menu key has to be pushed.Before the chassis is powered up and if any usb device is plugged to the usb port, the programme is downloaded from usb firstly.

Any usb device is plugged to usb port , user must open hyperterminal in the pc and connect pc to chassis via Mstar debug tool and any one of scart,dsub9 or I2c connectors. Serial connection settings are listed below:

- Bit per second: 115200
- Data bits: 8

- Parity: None
- Stop bits: 1
- Flow control: None

In this case the bootloader sofware puts “C” character to uart. After repeating “C” characters are seen in the hyperterminal user can send any file to chassis by selecting Transfer -> Send File menu item and choosing “**1K Xmodem**” from protocol section.

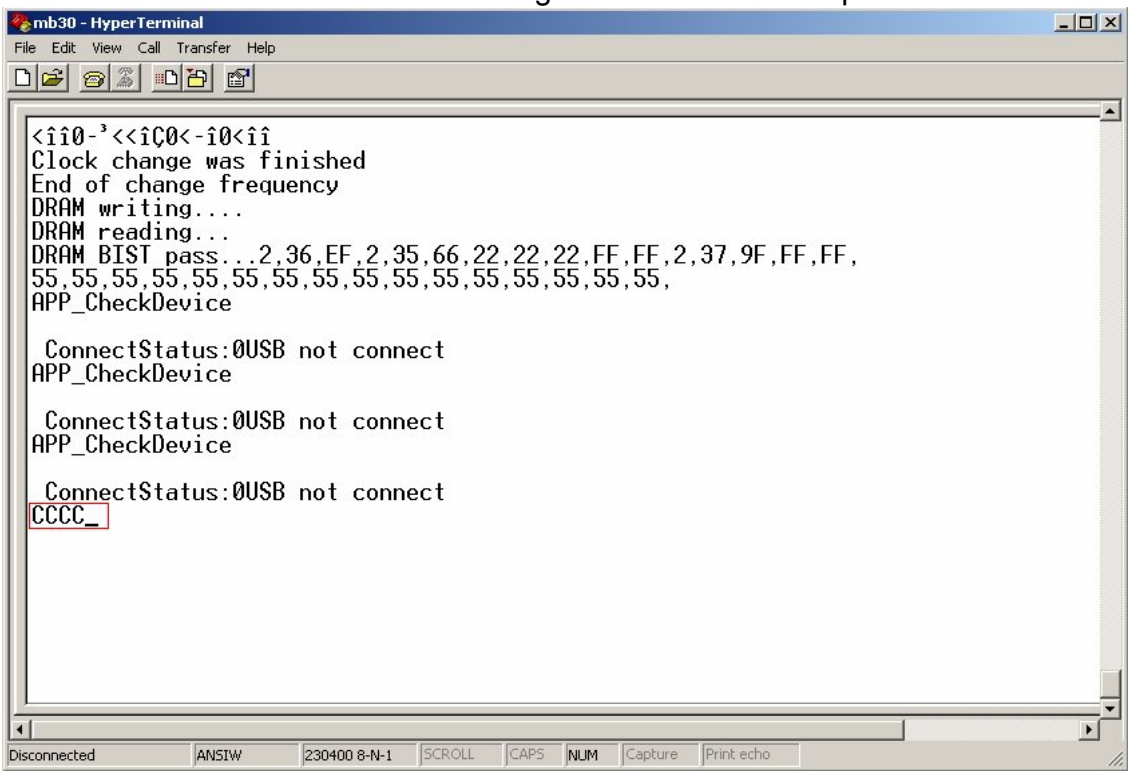


Figure 1. The Sample Output Before Sending The File

2. EEProm update

To Update eeprom content via uart scart,dsub9 or i2c with Mstar tool can used.
Serial connection settings are listed below:

- Bit per second: 9600
- Data bits: 8
- Parity: None
- Stop bits: 1
- Flow control: None

Programming menu item is choosed in the service menu and switch “HDCP Key Update Mode” from off to on.

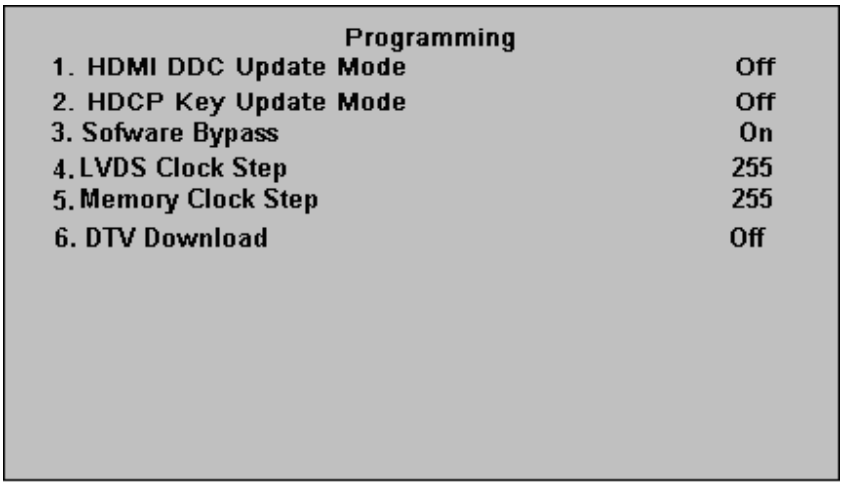


Figure 2. The Programming Service Menu

After then you must see Xmodem menu in the hyperterminal.To download hdcp key press k or to download eeprom content press w.

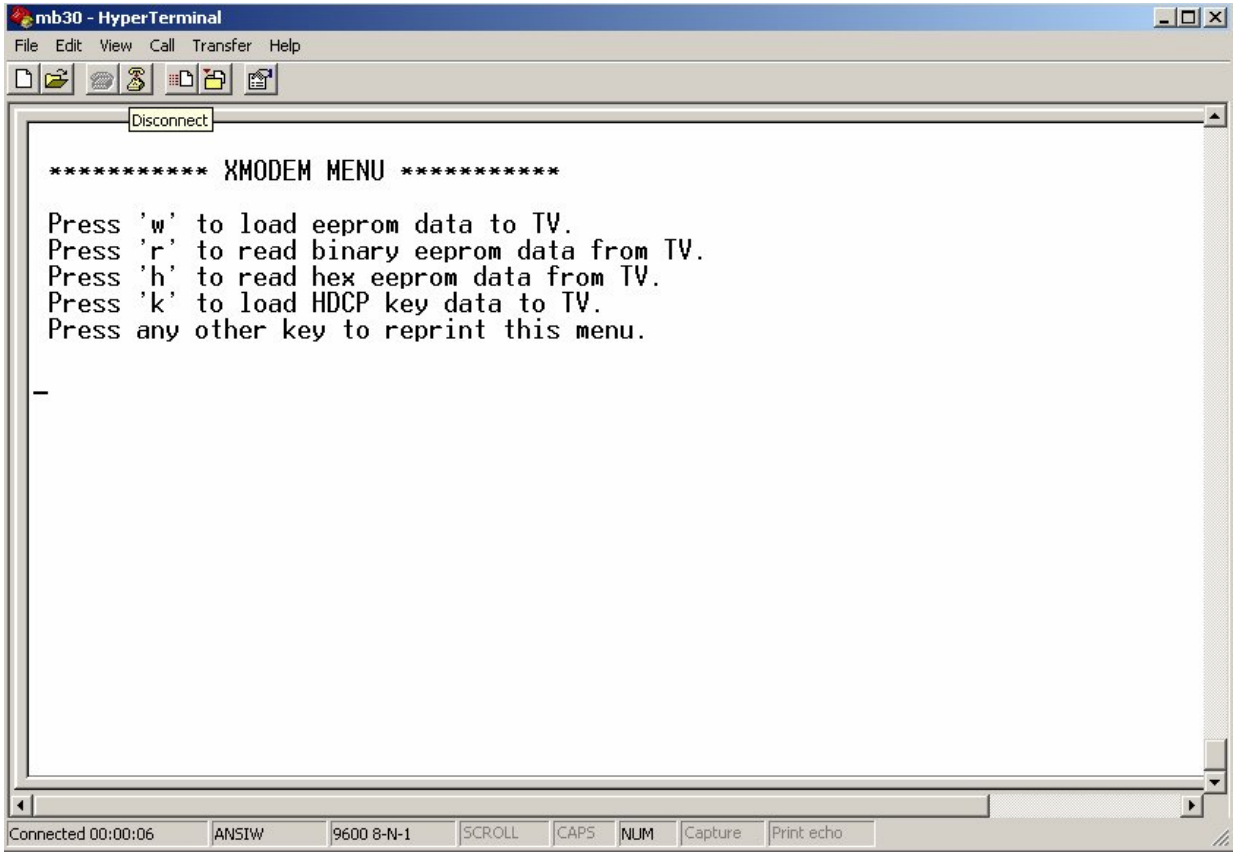


Figure 3. Xmodem Menu

If the repeated “C” characters are seen you can transfer file content via select Transfer->Send File and choose “**Xmodem”** protocol and click the “Send” button.

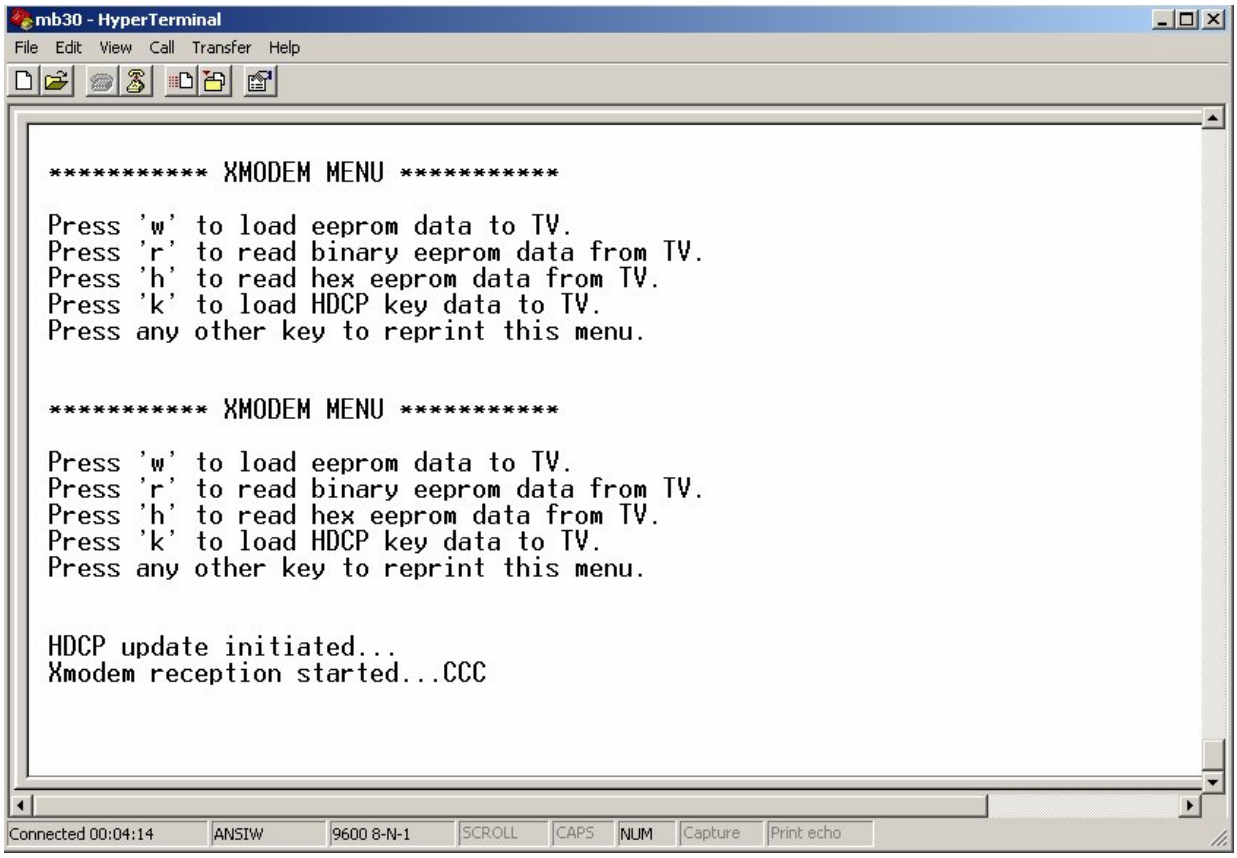


Figure 4. The Starting To Send

16.2 17MB25 HDCP key upload procedure.

1) Turn on TV set.
2) Open a COM connection using fallowing parameters and select ISP COM Port No

Baud Rate: 9600 bps
Data Bits: 8
Stop Bits: 1
Parity: None
Flow Control: None

3) Enter service menu by pressing “4” “7” “2” 5” consecutively while main menu is open
4) Select “9. Programming”
5) Select “HDMI HDCP Update Mode” yes.
6) On Hyper Terminal Window press “k”
7) Click on send file under Transfer Tab.
8) Select Xmodem and choose the HDCP key to be uploaded.
9) Press send button
10) Restart TV set

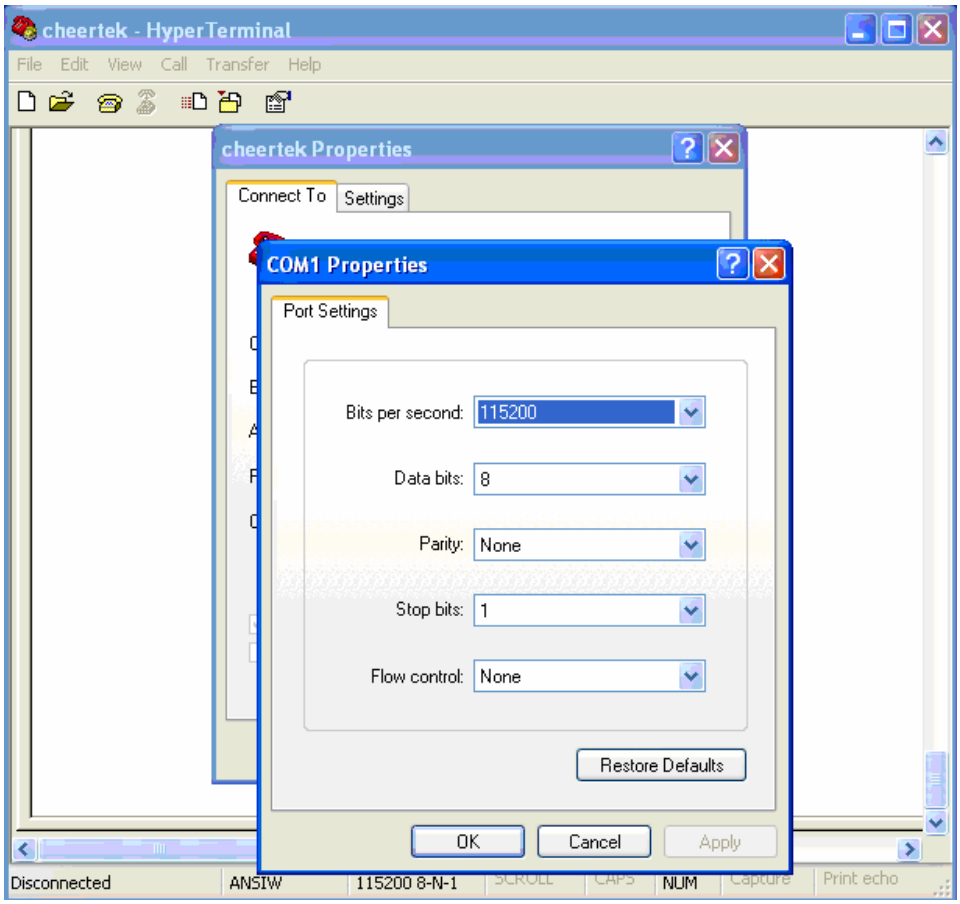
16.3 17MB25 Digital Software Update From SCART

Adjusting DTV Download Mode:

1. Power on the TV.
2. Exit the Stby Mode.
3. Enter the “Tv Menu”.
4. Enter “4725” for jumping to “Service Settings”.
5. Select “8. Programming” step.
6. Change “6. DTV Download” to “On”.
7. Switch to the Stby mode.

Adjusting HyperTerminal:

1. Connect the “MB25 SCART Interface” to SCART1 (bottom SCART plug).
2. Also connect the “MB25 SCART Interface” to PC.
3. Open “HyperTerminal”.
4. Determine the “COM” settings listed and showed below.
   - Bit per second: 115200
   - Data bits: 8
   - Parity: None
   - Stop bits: 1
   - Flow control: None

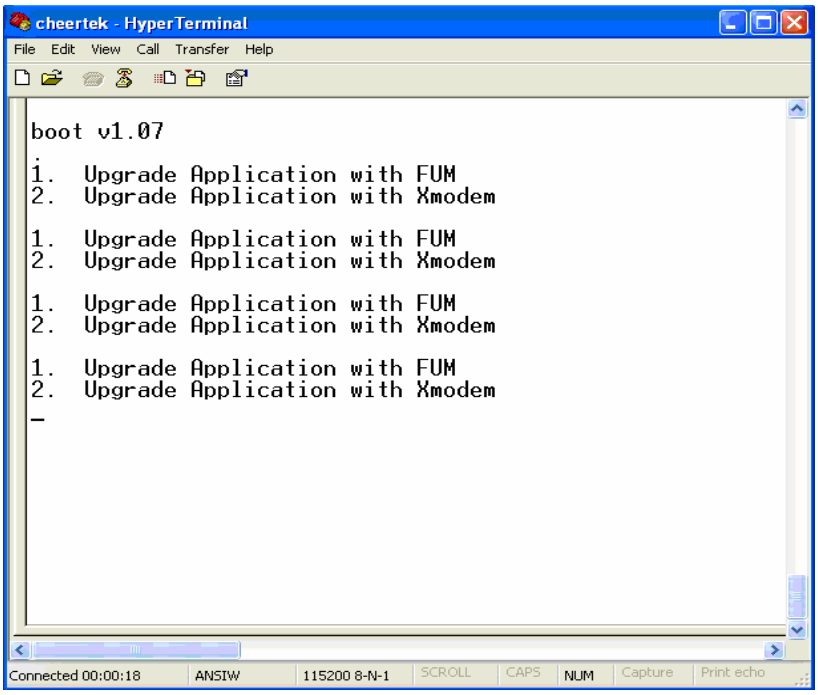


COM Properties Window

6. Click “OK”.

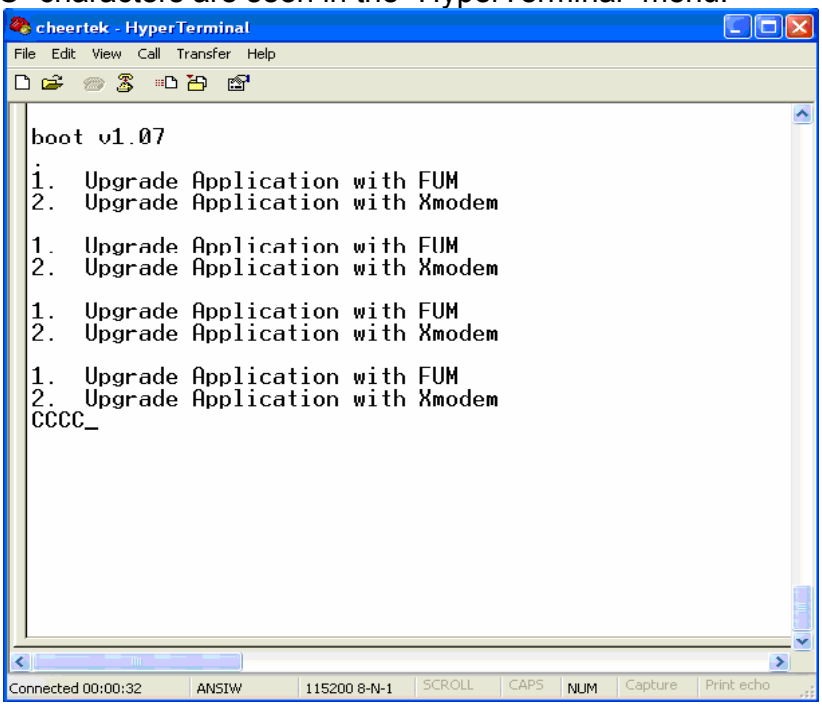
Software Updating Procedure

1. In the HyperTerminal Menu, click the “Connect” button.
2. Exit the Stby Mode.
3. The “Space” button on the keyboard must be pressed, when the following window can be seen.



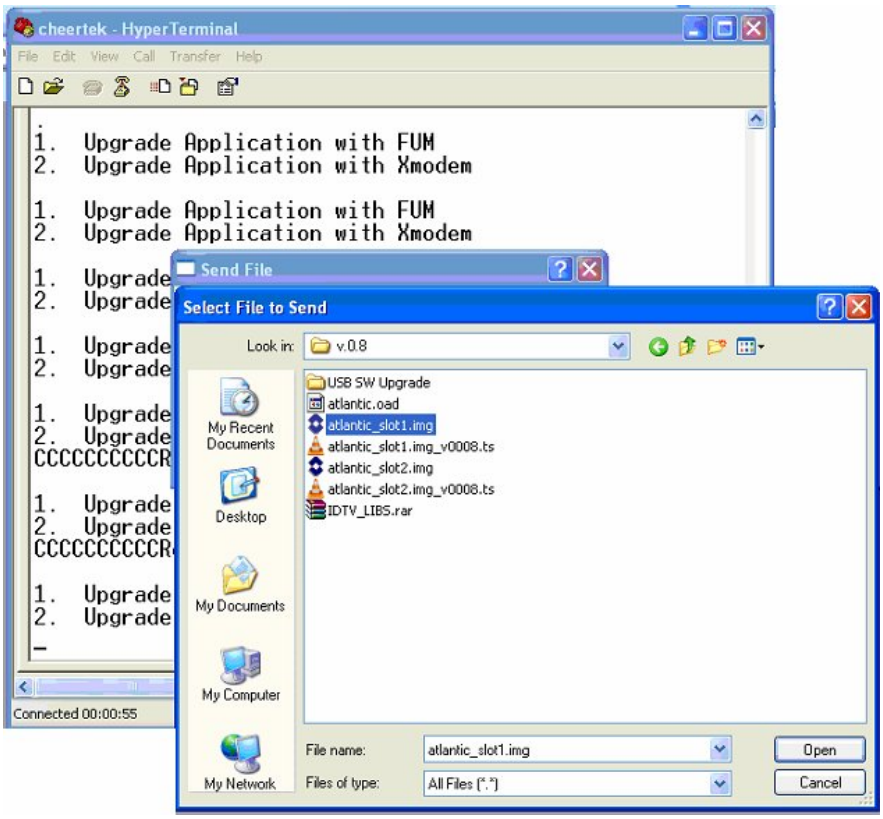
Selection Window

4. Press the “2” button on the keyboard for choosing “2. Upgrade Application with Xmodem”.
5. Repeating “C” characters are seen in the “HyperTerminal” menu.

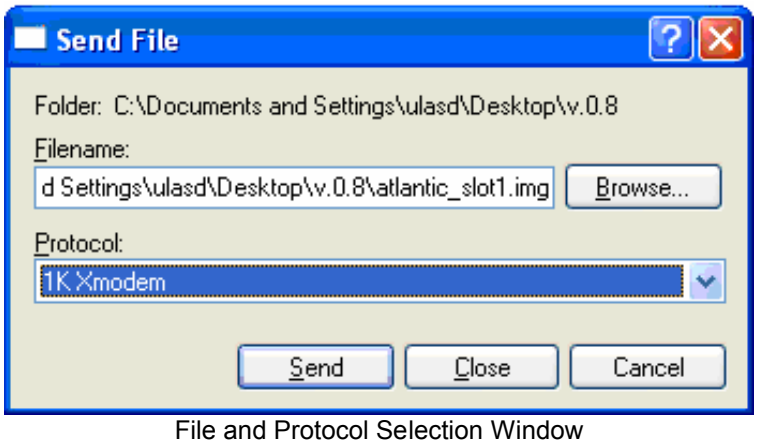


The Sample Output Before Sending The File

6. Click the “Send” button on the HyperTerminal
7. Select the “Filename **xxxx**_slot1.img” using “Browse”.
8. Choose the “1K Xmodem” from “Protocol” option.

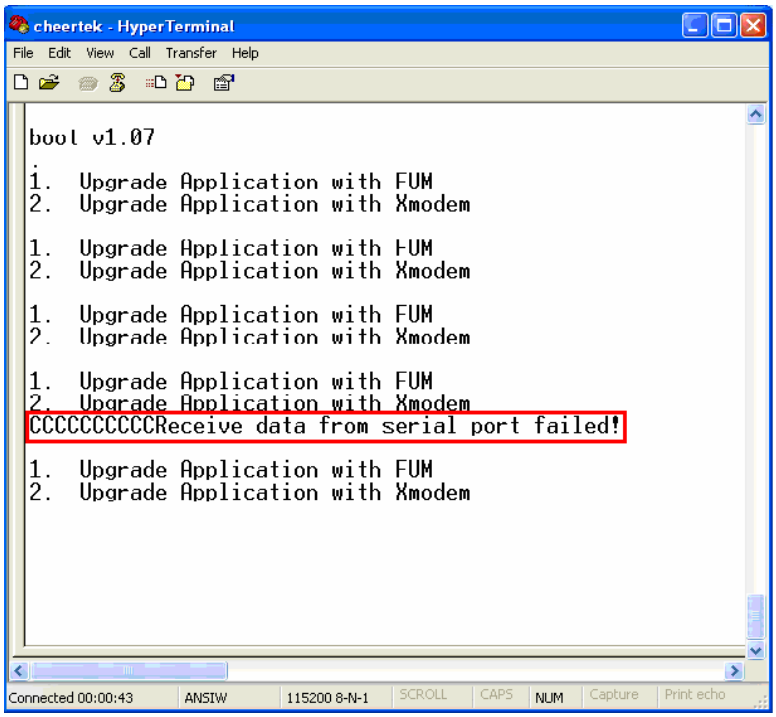


Selection of File



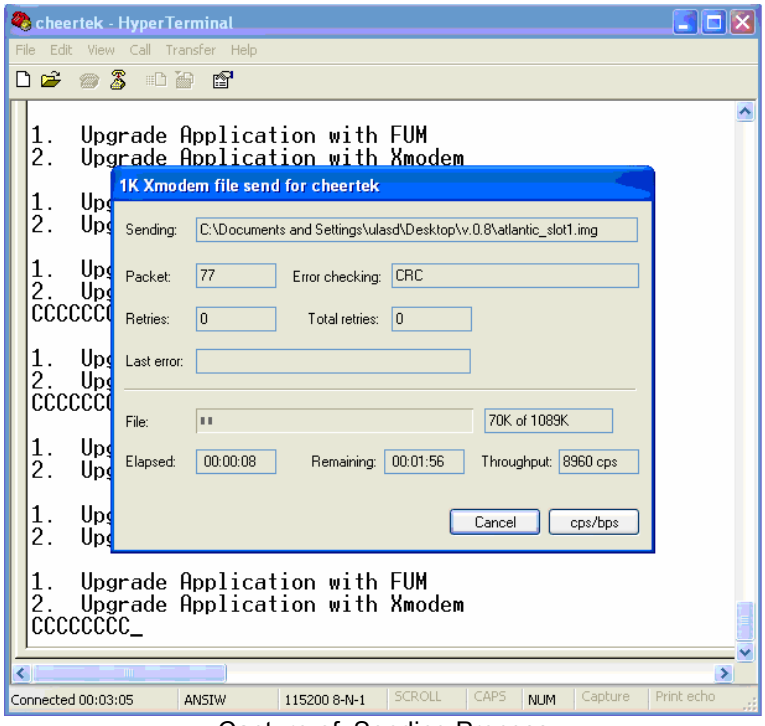
File and Protocol Selection Window

Note: In the Software updating Procedure section, when the first “C” character is seen, the filename selection process must be finished before 10 seconds. If the process can not be finished, the file sending operation will be cancelled. The following figure shows this situation.



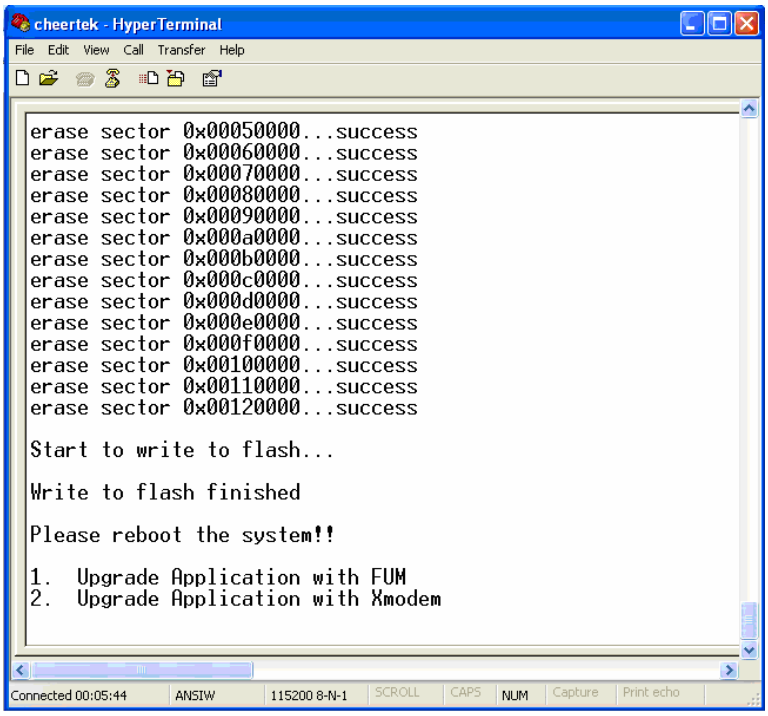
Capture of Receving Data Failing

9. When sending the file the following window must be seen.



Capture of Sending Process

10. After the sending process the following HyperTerminal window must be seen.

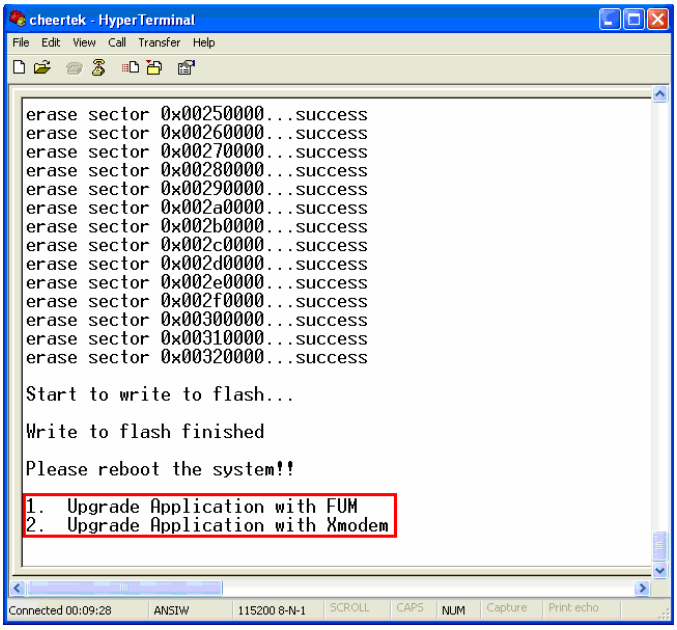


Capture of End of The Sending Process

11. For sending second program file, the Software Updating Procedure must be repeated from the step **X**. Select the “Filename **xxxx**_slot2.img” using “Browse”.
12. After sending the second program file, the Software Updating Procedure will be succesful.

Note: After the File Sending Process,

1. Upgrade Application with FUM
2. Upgrade Application with Xmodem, options must be seen.



End of The Sending Process

Checking Of The New Software

1. Turn off and on the TV.
2. Enter the “Setup” submenu in the “DTV Menu”.
3. Choose the “Configuration” option.
4. For controlling new software, check the “Receiver Upgrade” option.

16.4 17MB25 Digital Software Update From USB

Software upgrade is possible via USB disk by folowing the steps below.

1. Copy the bin file, including higher version than the software loaded in flash, into the USB flash memory root directory. This file should be named up.bin.
2. Insert the USB disk.
3. Digital module performs version and CRC check. If version and CRC check is successful, then a message prompt appears to notify user about new version. If the user confirms loading of new version, upgrade.bin file is written into flash unused slot.
4. Digital module disables the previous software in the flash and then a system reset is performed.
5. After the reset, digital module starts with new software.

Revert operation:

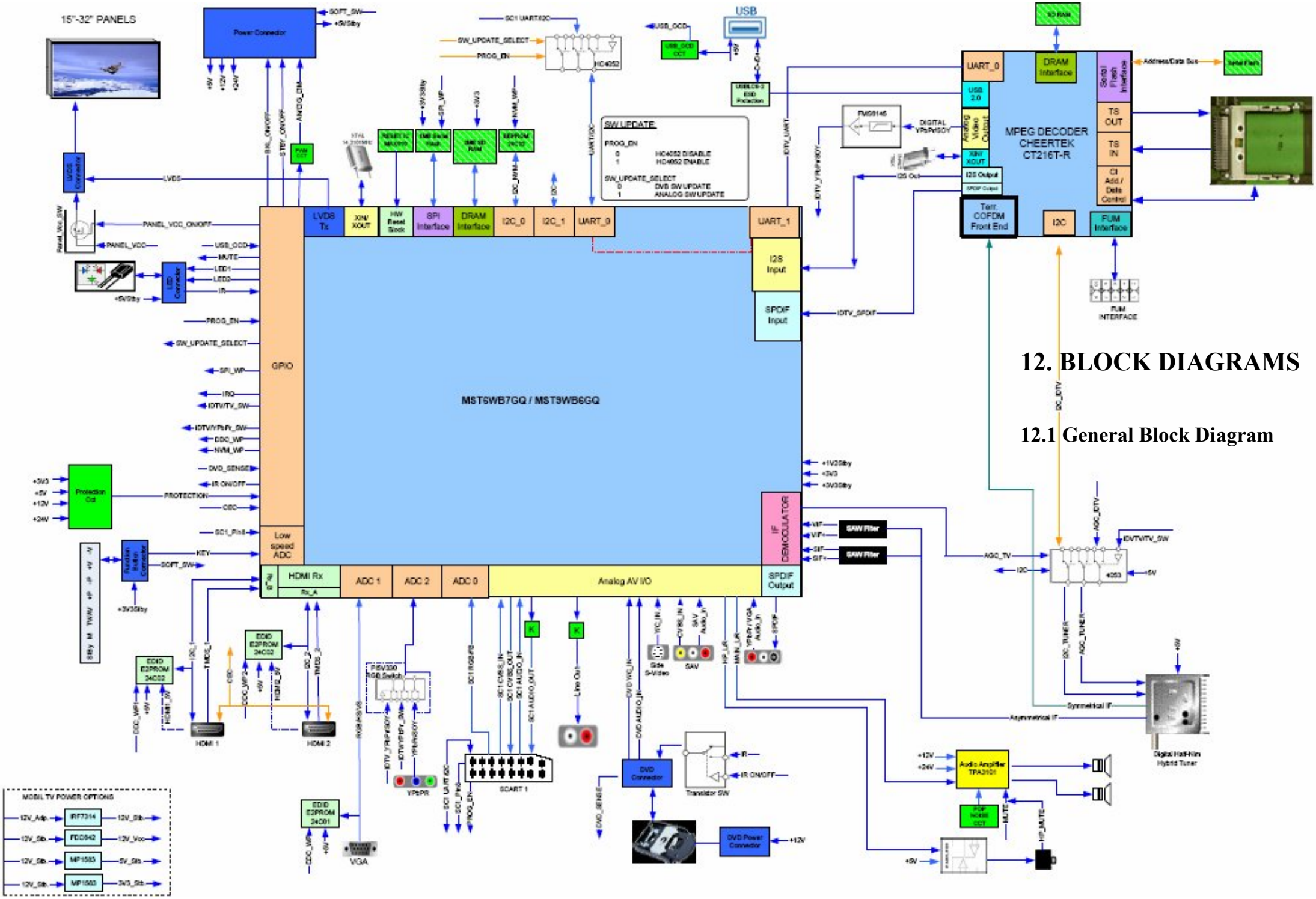
With revert operation, it is possible to *downgrade* the software.
Revert operation is very similar to upgrade process. In the revert operation, file name should be f_up.bin. Also user confirmation is not asked.

1. Copy the bin file into the USB flash memory root directory. This file should be named force_upgrade.bin.
2. Insert the USB disk.
3. A lower version than the software in flash can be loaded with revert operation. Digital module performs only CRC check. If CRC check is successful, then force_upgrade.bin file is written into flash unused slot.
4. Digital module disables the previous software in the flash.
5. A message prompt is displayed to notify user about end of revert process.
6. Power off/on is required to start digital module with the new software.

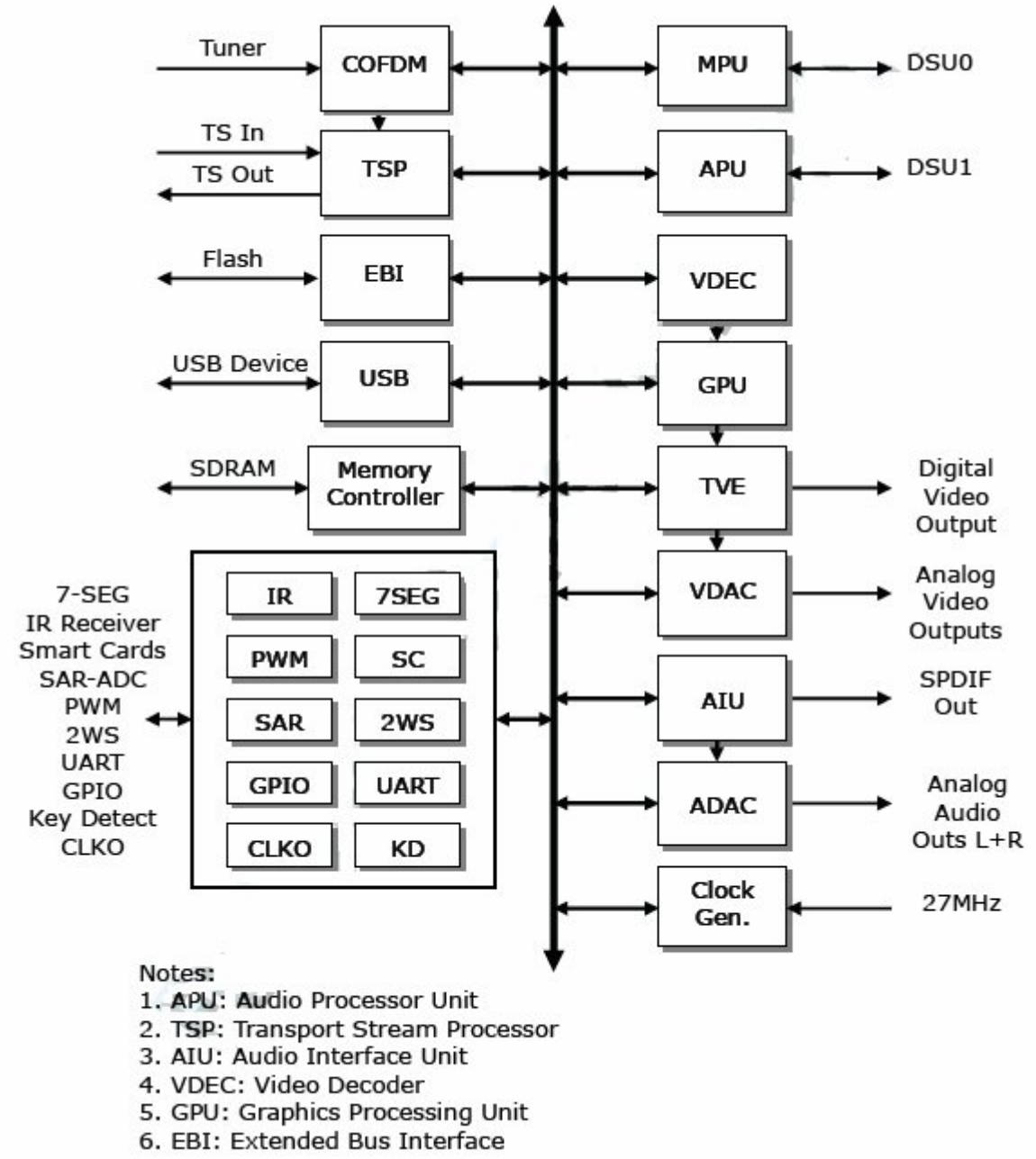
For controlling new software, check the “Receiver Upgrade” option.

12. BLOCK DIAGRAMS

12.1 General Block Diagram

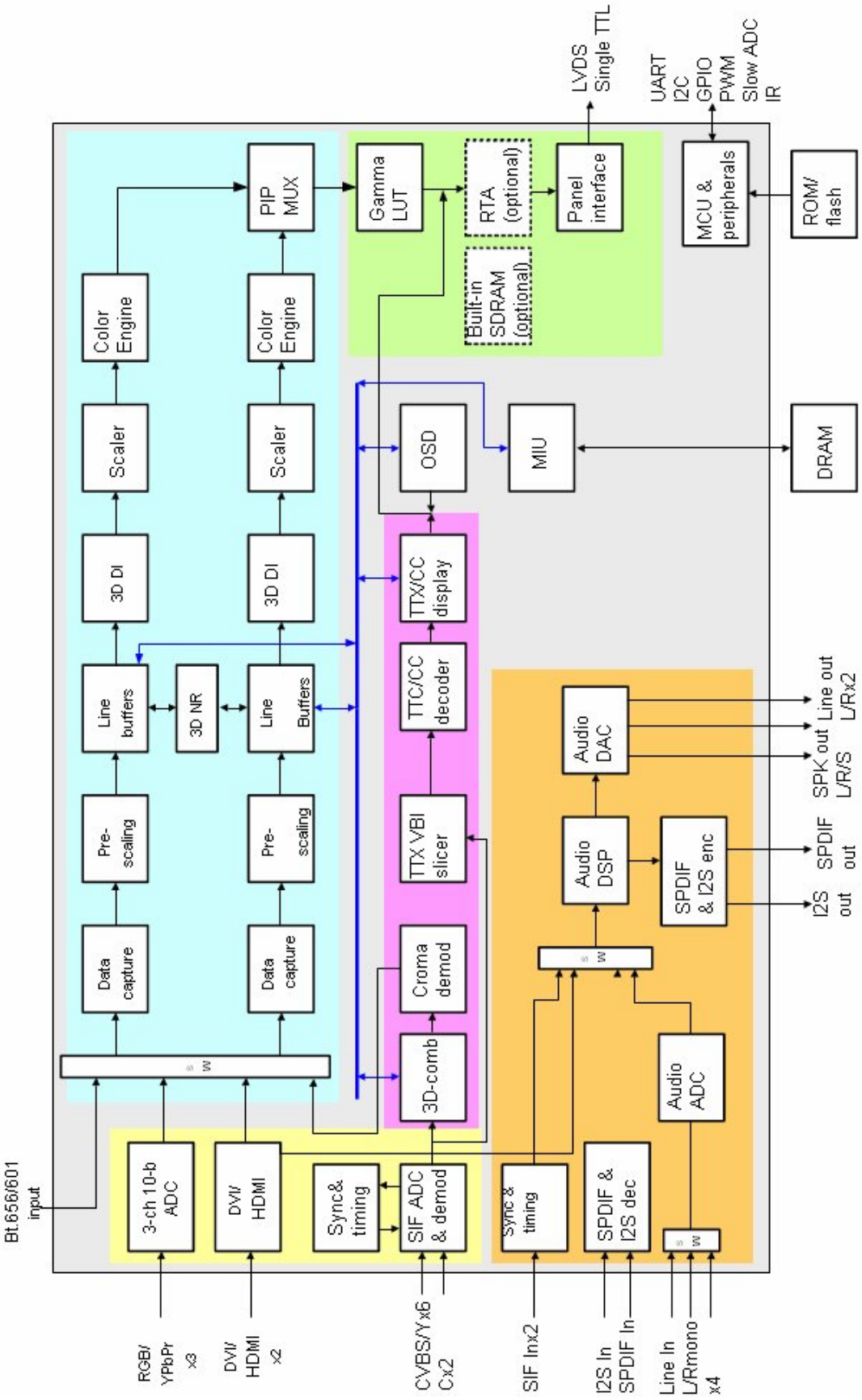


12.2 Integrated DVB-T Receiver Block Diagram



Notes:
1. APU: Audio Processor Unit
2. TSP: Transport Stream Processor
3. AIU: Audio Interface Unit
4. VDEC: Video Decoder
5. GPU: Graphics Processing Unit
6. EBI: Extended Bus Interface

12.3 MSTAR Block Diagram



LG

TU102 TDTC-G101D

AIF 12 — ANALOG_IF
DIF1 11 — DIGITAL_IF_N
DIF2 10 — DIGITAL_IF_P
IF_AGC 9 — IF_AGC_DVB_IN
AS 8 — ADDRESS_SEL_TUNER
NC 7
B2 6 — 5V_TUN
SDA 5 — SDA_TUNER
SCL 4 — SCL_TUNER
RF_AGC 3 — RF_AGC
B1 2 — 33V_TUNER
ANT_PWR 1 — ACT_ANT

Samsung/Thomson

TU101 DTOS403LH172A

IFOUT- 11
IFOUT+ 10 — DIGITAL_IF_P
VT 9 — 33V_TUNER
IF_AGC 8 — IF_AGC_DVB_IN
+5V 7 — 5V_TUN
AIF_OUT 6 — ANALOG_IF
SDA 5 — SDA_TUNER
SCL 4 — SCL_TUNER
SAS 3 — ADDRESS_SEL_TUNER
RF_AGC 2 — RF_AGC
BA 1 — ACT_ANT

L117 1u
C675 47p 50V
DIGITAL_IF_N
S104

ACTIVE ANTENNA

5V_TUN — R482 4R7 — 2R1 TH101
OVER_CUR_DETECT — R502 10k — F234 330R
R501 10k
R622 1k
Q102 FDN336P
BC848B Q115
R503 10k — ANT_CTRL
ACT_ANT — Tp151
C359 10u 10V
R504 10k

D121 1N4148
RF_AGC_A — R111 12k — T_AGC
C448 47u 16V N.C.

IF_AGC_DVB_IN — R505 10k — IF_AGC_DVB
10V 100n C136

This part must be placed near the tuner

SCL_TUNER — R126 47R — SCL_TUN
C586 47p 50V
SDA_TUNER — R127 47R — SDA_TUN
C587 47p 50V

TUNER SUPPLY OPSION

8V_VCC — F116 330R — C600 47u 16V
U123 LM1117 (IN, OUT, GND, VOUT)
R408 330R
R460 1k
C360 10u 10V
C134 100n 10V
Near Tuner supply pin
S105
5V_TUN

!!!En az 1.8 cm2 altta ve üstte soðutma alaný býrakýlmalý.

AGC AND I2C SWITCH PART

Connect if "33V Integrated Tuner" is used!

33V_TUNER — C532 1u 50V — R624 1k — 5V_TUN
S102
5V_VCC
C128 100n 10V

U115 74HCT4053

SCL_TUN_DVB — SCL — SCL_TUN
RF_AGC_DVB — RF_AGC_A — SDA_TUN_DVB — SDA — SDA_TUN
RF_AGC — S103 — S101
10V 100n C137 NEAR THE TUNER
R254 4k7 — 5V_VCC

Q116 BC848B — R595 22k — IDTV_SW

This part must be placed near the tuner

8V_VCC — R380 75R — C520 47u 16V
R252 4k7
C135 100n 10V
L114 1u
R735 680R
R483 1k2
R125 47R
ANALOG_IF — L111 1u — C545 10n 16V — R680 56R
Q144 BF799
R623 1k
R384 10R

5V_TUN — R473 6k8 — R231 3k3
C546 10n 16V
BA782 — D145
Z101 K9656M (IN1, IN2, OUT1, OUT2, GND)
SIFP
SIFM
R474 6k8
R594 22k
SIF_CTL — R209 100k — Q140 BSN20
R210 100k N.C.
C547 10n 16V
Z102 K3958M (IN1, IN2, OUT1, OUT2, GND)
L104 2u2 N.C.
VIFM
VIFP

WARNING!!! Saw filter outputs must be close the chip

WARNING!!! This part must be close to chip

C467 10u 10V — C132 100n 10V
C654 220u 6V3 — C133 220n 10V — C597 220p 50V — C598 100p 50V
3V3_STBY — F187 330R
C363 10u 10V — C131 100n 10V
3V3_VCC — F184 330R
C364 10u 10V — C130 100n 10V

U138 MST6WB7GQ-3

62 AVDD_MPLL
63 VR27 (4)
64 VR12
65 AVDD_RXS
66 GND_RXS
67 SIFP
68 SIFM
69 VIFM
70 VIFP
71 GND_RXV
72 AVDD_RXV
73 TAGC

C361 10u 10V — C129 100n 10V
3V3_VCC — F185 330R
5V_TUN — F186 330R
C510 100n 10V
4k7 R253
T_AGC

WARNING!!! This part must be close to chip

VESTEL	PROJECT NAME : 17MB25	A3
SCH NAME :ANALOG IF		SHEET:1 OF:11
DRAWN BY :ÖNDER GENÇ		4-28-2008_16:47

SCART1 INPUT

DVD CONNECTION

S-VIDEO INPUT

VGA INPUT

SIDE AV INPUT

YPBPR INPUT

LINE OUTPUT
SUBWOOFER OUTPUT

COAXIAL SPDIF OUTPUT
YPBPR/PC LINE INPUT

SPDIF OUTPUT INTERFACE

VESTEL	PROJECT NAME : 17MB25	A3
SCH NAME :A/V INTERFACE		SHEET:2 OF:11
DRAWN BY :ONDER GENC		4-28-2008_15:57

VIDEO TERMINATIONS AND DIFFERENTIAL TRACING
Place 75R termination resistors
close to Paulo reference GNDs

DVD_C_IN — R651 75R — R143 47R — 16V 47n C432 — C0
DVD_Y_IN — R650 75R — R142 47R — C434 47n 16V — Y0
S_VIDEO_C_IN — R653 75R — R145 47R — 16V 47n C423 — C1
S_VIDEO_Y_IN — R652 75R — R144 47R — C422 47n 16V — Y1
SC1_CVBS_IN — R654 75R — R146 47R — C424 47n 16V — CVBS1
R773 470R — C612 1n — SOGIN0
SAV_CVBS — R649 75R — R141 47R — C433 50V 47n 16V — CVBS2
DVB_CVBS — R664 75R — R140 47R — C435 47n 16V — CVBS3
SC1_B — R665 75R — R137 47R — C421 47n 16V — BIN0P
SC1_G — R667 75R — R138 47R — C418 47n 16V — GIN0P
SC1_R — R666 75R — R139 47R — C417 47n 16V — RIN0P
SW_PB — R656 75R — R149 47R — C428 47n 16V — BIN2P
SW_Y — R657 75R — R148 47R — C426 47n 16V — GIN2P
SW_PR — R655 75R — R147 47R — C427 47n 16V — RIN2P
VGA_B — R659 75R — R150 47R — C429 47n 16V — BIN1P
VGA_G — R658 75R — R151 47R — C431 47n 16V — GIN1P
VGA_R — R660 75R — R152 47R — C430 47n 16V — RIN1P
DVB_C_IN — R667 75R — R138 47R — C418 47n 16V — GIN0P
SC1_G — R666 75R — R139 47R — C417 47n 16V — RIN0P
SC1_R — R656 75R — R149 47R — C428 47n 16V — BIN2P
SW_PB — R648 47R — C426 47n 16V — GIN2P
SW_Y — R657 75R — R403 470R — C490 1n 50V — SOGIN2
SW_PR — R655 75R — R147 47R — C427 47n 16V — RIN2P
VGA_B — R659 75R — R150 47R — C429 47n 16V — BIN1P
VGA_G — R658 75R — R404 470R — C491 1n 50V — SOGIN1
VGA_R — R660 75R — R152 47R — C430 47n 16V — RIN1P

U138
MST6WB7GQ-3

VGA_HSNC	17	HSYNC1	AVDD_AU_1	74	AVDD_AU (C148 100n 10V, 10V 10u)
VGA_VSNC	18	VSYNC1	GND5	75	
C152 100n 10V	19	VCLAMP	AUVRM	76	10V 10u C369
C151 100n 10V	20	REFP	AUVRP	77	C368
C150 100n 10V	21	REFM	AUVAG	78	C344 1u 16V
BIN1P	22	BIN1P	AVDD_AU_2	79	AVDD_AU
SOGIN1	23	SOGIN1	LINE_IN_0L	80	LINE_IN_0L
GIN1P	24	GIN1P	LINE_IN_0R	81	LINE_IN_0R
RIN1P	25	RIN1P	LINE_IN_1L	82	LINE_IN_1L
R133 47R — C420 47n 16V	26	BIN0M	LINE_IN_1R	83	LINE_IN_1R
BIN0P	27	BIN0P	AUCOM	84	C149 100n 10V — S106
R134 47R — C419 47n 16V	28	GIN0M	LINE_IN_2L	85	LINE_IN_2L
GIN0P	29	GIN0P	LINE_IN_2R	86	LINE_IN_2R
SOGIN0	30	SOGIN0	LINE_IN_3L	87	LINE_IN_3L
RIN0P	31	RIN0P	LINE_IN_3R	88	LINE_IN_3R
AVDD_33 — C143 100n 10V	32	AVDD_33_3	LINE_IN_MONO	89	R686 33k
	33	GND3	LINE_OUT_3L	90	DSP_CH2_L
	34	HSYNC0	LINE_OUT_3R	91	DSP_CH2_R
SC1_FB — R687 33k	35	VSYNC0	LINE_OUT_2L	92	DSP_CH4_L
	36	VSYNC2	LINE_OUT_2R	93	DSP_CH4_R
BIN2P	37	BIN2P	LINE_OUT_1L	94	DSP_CH1_L
SOGIN2	38	SOGIN2	LINE_OUT_1R	95	DSP_CH1_R
GIN2P	39	GIN2P	LINE_OUT_0L	96	DSP_CH3_L
RIN2P	40	RIN2P	LINE_OUT_0R	97	DSP_CH3_R
C1	41	C1			
Y1	42	Y1			
C0	43	C0			
Y0	44	Y0			
CVBS3	45	CVBS3			
CVBS2	46	CVBS2			
CVBS1	47	CVBS1			
R132 47R — C425 47n 16V	48	VCOM1			
R512 10k	49	CVBS0			
R131 47R — C416 47n 16V	50	VCOM0			
AVDD_33 — C144 100n 10V	51	AVDD_33_4			
	52	CVBSOUT1			
	53	CVBSOUT0			
	54	GND4			

CVBS0_OUT — R351 100R

AVDD_AU DECOUPLING CAPACITORS
AVDD_AU — C142 100n 10V — pin79
C145 100n 10V — pin74
F120 330R — 3V3_VCC

SCART VIDEO OUTPUT AMPLIFIERS

5V_TUN — F119 330R — C326 1u 16V
Q146 BC858B — R402 470R — R674 39k
Q119 BC848B — C378 10u 10V — CVBS0_OUT
SC1_CVBS_OUT — R646 75R — R620 300R
R879 75R — R221 100R — R467 15k
GAIN_SW1 — R806 4k7 — Q154 2N7002

SC1_AUD_R_OUT — C375 10V 10u — R692 33k — C121 220p 50V — R678 82k
SC_1_R — C332 1u 16V — R739 20k
U118 TL062 (OUT1 VDD, IN1- OUT2, IN1+ IN2-, VSS IN2+)
V+ — C512 100n 16V — F217 600R — 8V_VCC
R691 33k — C374 10V 10u — SC1_AUD_L_OUT
C120 220p 50V — R677 82k
R738 20k — C335 1u 16V — SC1_L

LINE_R_OUT — C372 10V 10u — R155 47R — R690 33k
8V_VCC — F219 600R — C511 100n 16V
POP_MUTE — R522 10k — R802 3k3 — Q121 BC848B
C119 50V 220p — R676 82k
LINE_OUT_R — C331 1u 16V — R737 20k
U117 TL062 (OUT1 VDD, IN1- OUT2, IN1+ IN2-, VSS IN2+)
R689 33k — R153 47R — C371 10V 10u — LINE_L_OUT
Q120 BC848B — R521 10k — POP_MUTE — 3k3 R801
C118 50V 220p — R675 82k
R736 20k — C330 1u 16V — LINE_OUT_L

V+ — C327 1u 16V — C367 10u 10V — R684 33k — R685 33k — 8V_VCC

AUDIO INPUT VOLTAGE DIVISION AND DC BLOCK
Place close to Paulo

LINE_IN_0L — C340 1u 16V — R513 10k — R607 22k — SC1_AUD_L_IN
LINE_IN_0R — C341 1u 16V — R514 10k — C493 1n 50V — R606 22k — SC1_AUD_R_IN
LINE_IN_1L — C338 1u 16V — R515 10k — C492 1n 50V — R605 22k — DVD_AUD_L_IN
LINE_IN_1R — C339 1u 16V — R516 10k — C495 1n 50V — R603 22k — DVD_AUD_R_IN
LINE_IN_2L — C336 1u 16V — R517 10k — C494 1n 50V — R601 22k — YPBPR_AUD_L_IN
LINE_IN_2R — C337 1u 16V — R518 10k — C497 1n 50V — R600 22k — YPBPR_AUD_R_IN
LINE_IN_3L — C343 1u 16V — R519 10k — C496 1n 50V — R599 22k — SAV_AUD_L_IN
LINE_IN_3R — C342 1u 16V — R520 10k — C498 1n 50V — R598 22k — SAV_AUD_R_IN
C499 1n 50V

DVB/YPBPR SWITCH

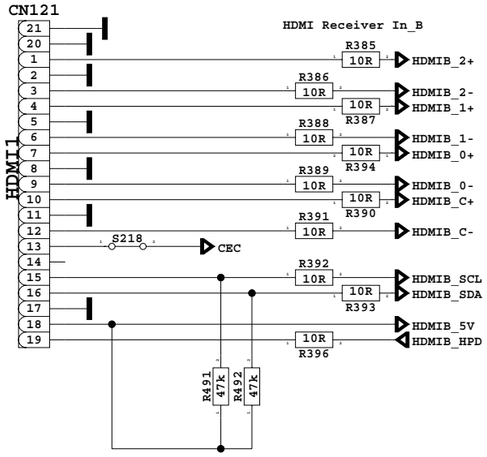
C443 27p 50V — DVB/YPBPR_SW — R627 1k
DVB_PR — R661 75R — S109 — S110 — RCA_PR
SW_PR — DVB_Y — C444 27p 50V — R662 75R — RCA_Y — S108 — S112 — SW_Y
U129 PI5V330 (IN, S1A, S2A, DA, S1B, S2B, DB, GND; VCC, EN, S1D, S2D, DD, S1C, S2C, DC)
10V 100n — C147 — F151 330R — 5V_VCC
C445 27p 50V — DVB_PB — R663 75R — SW_PB
RCA_PB — S107 — S111

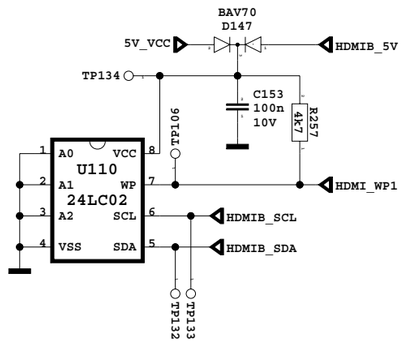
DSP_CH2_L — R228 100R — C555 10n 16V — R419 22k — HP_L
DSP_CH2_R — R229 100R — C554 10n 16V — R420 22k — HP_R
DSP_CH4_L — R224 100R — C550 10n 16V — R415 22k — LINE_OUT_L
DSP_CH4_R — R225 100R — C551 10n 16V — R416 22k — LINE_OUT_R
DSP_CH1_L — R227 100R — C553 10n 16V — R418 22k — MAIN_L
DSP_CH1_R — R226 100R — C552 10n 16V — R417 22k — MAIN_R
DSP_CH3_L — R223 100R — C549 10n 16V — R414 22k — SC1_L
DSP_CH3_R — R222 100R — C548 10n 16V — R413 22k — SC_1_R

AUDIO OUTPUT FILTERS
Place close to Paulo

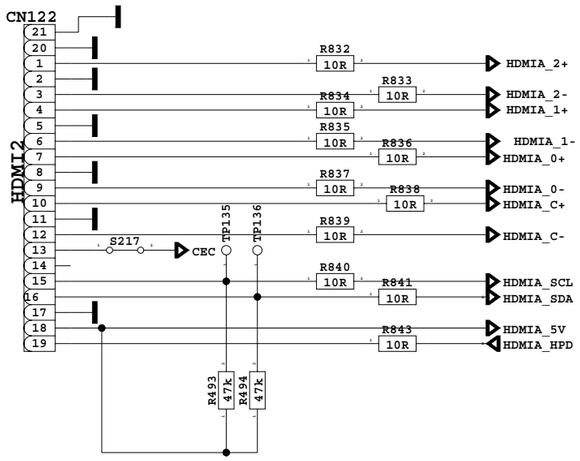
VESTEL	PROJECT NAME : 17MB25	A3
SCH NAME :A/V INTERFACE	SHEET:3	OF:11
DRAWN BY :ONDER GENC	4-28-2008_15:57	

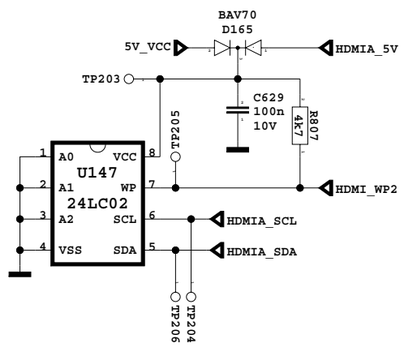
HDMI1

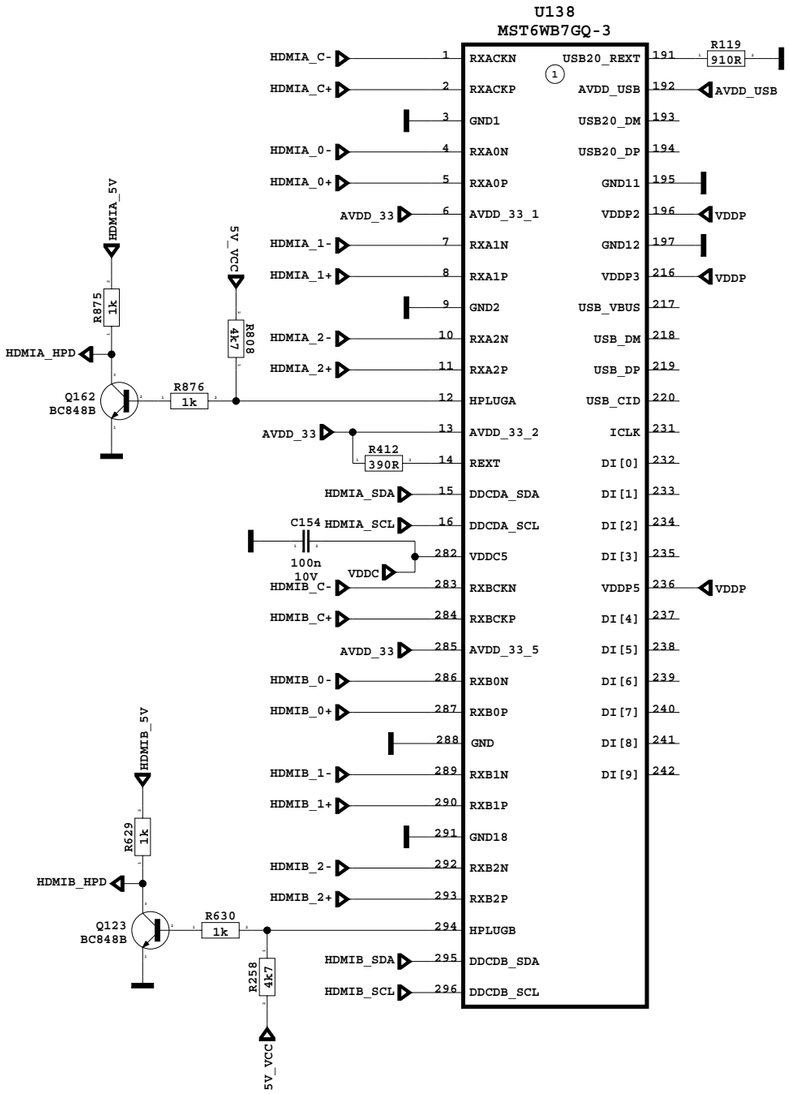


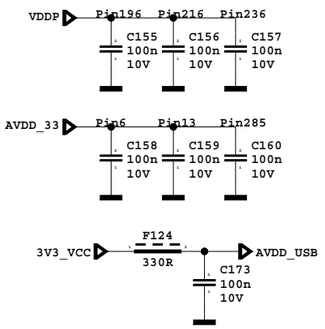


HDMI2

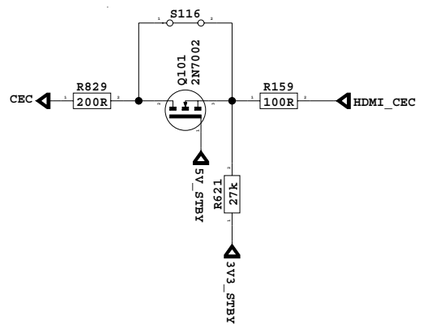






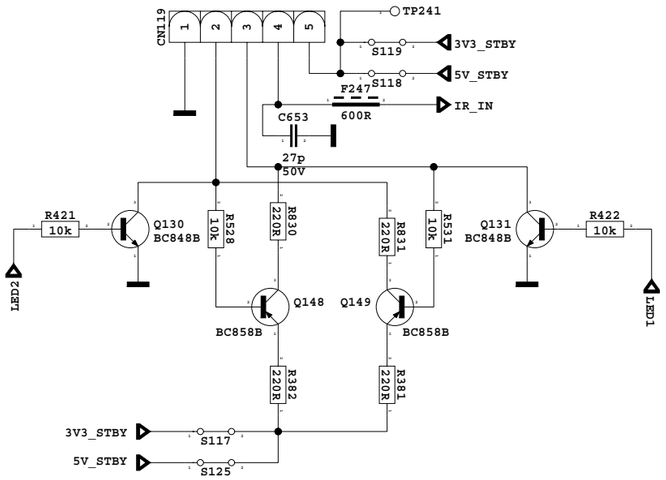


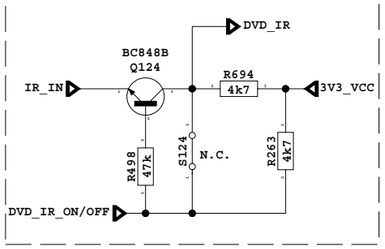
CEC CIRCUIT

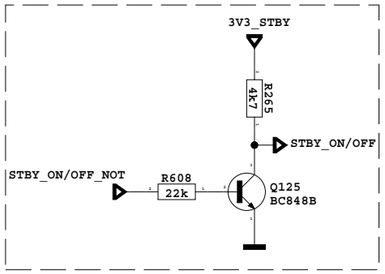


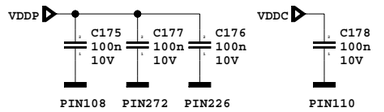
VESTEL	PROJECT NAME : 17MB25	A3
SCH NAME :HDMI&USB	SHEET:4	OF:11
DRAWN BY :S.SEBNEM TAS & ULAS DERELI	4-28-2008_15:57	

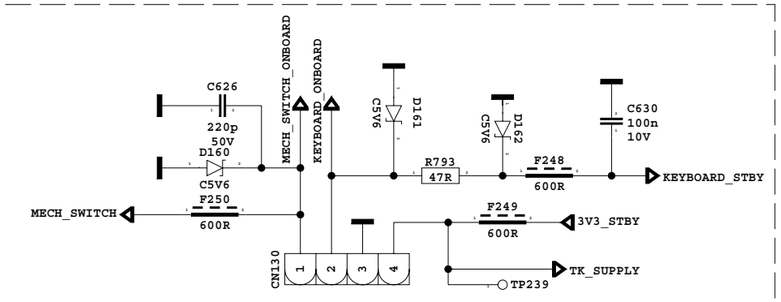
LED

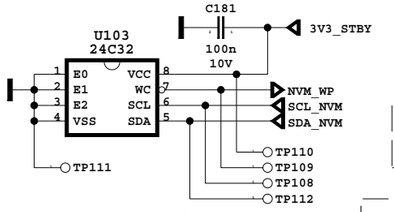


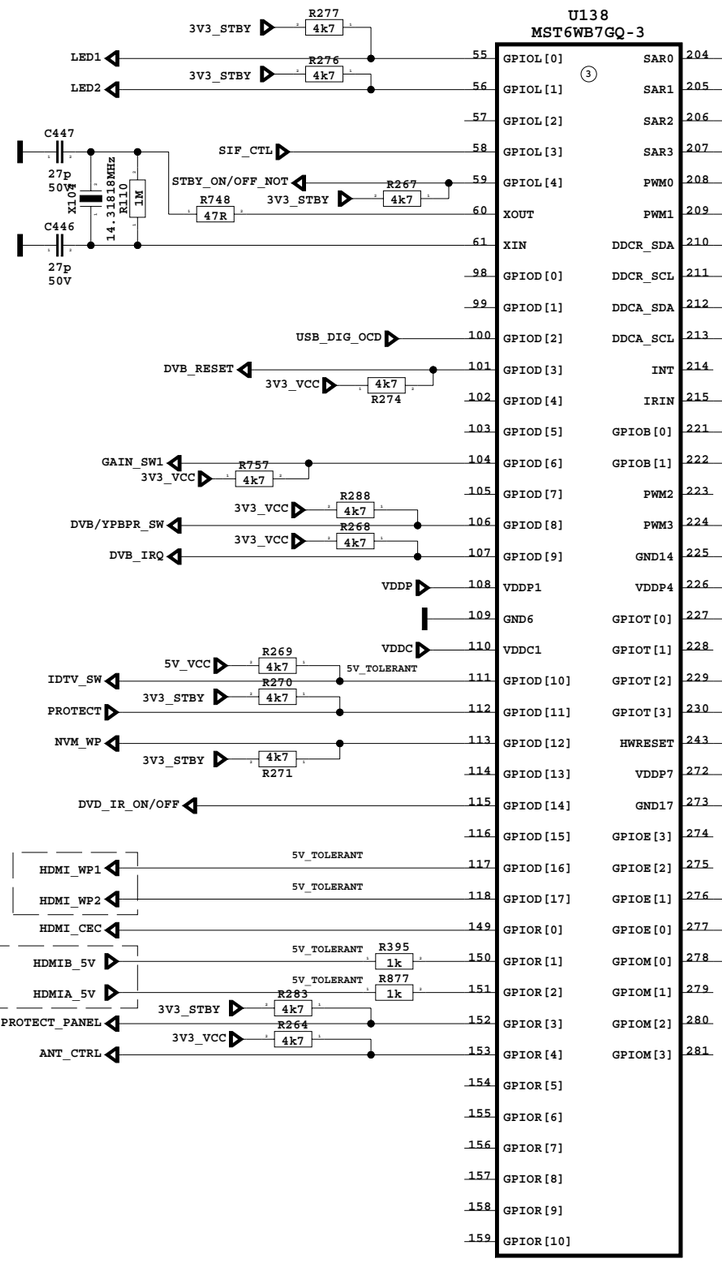




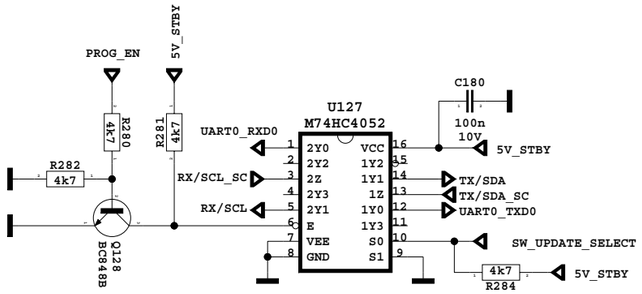


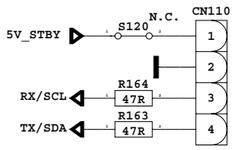






PROGRAMMING PART

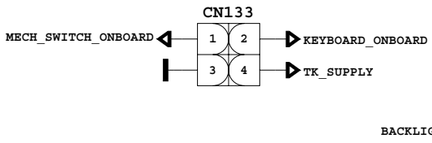


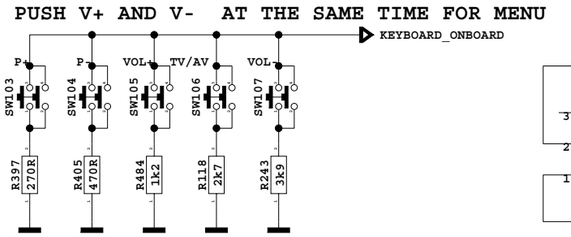


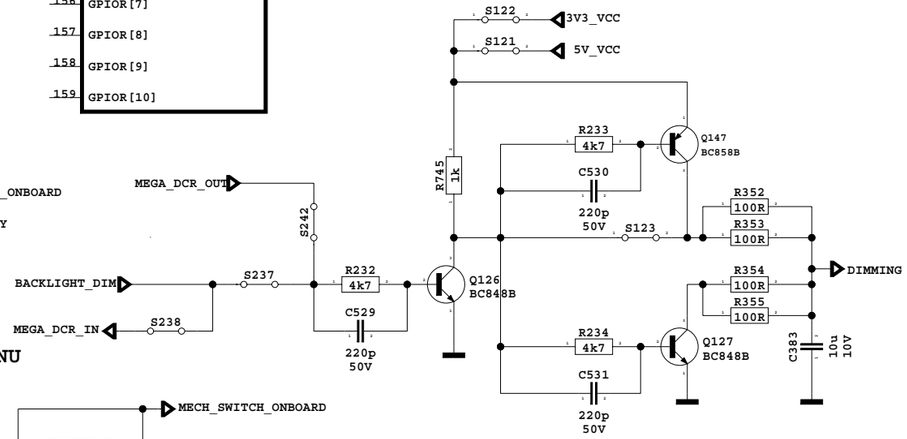
DEBUG SOCKET

PROG_EN	
0	HC4052 DISABLE
1	HC4052 ENABLE

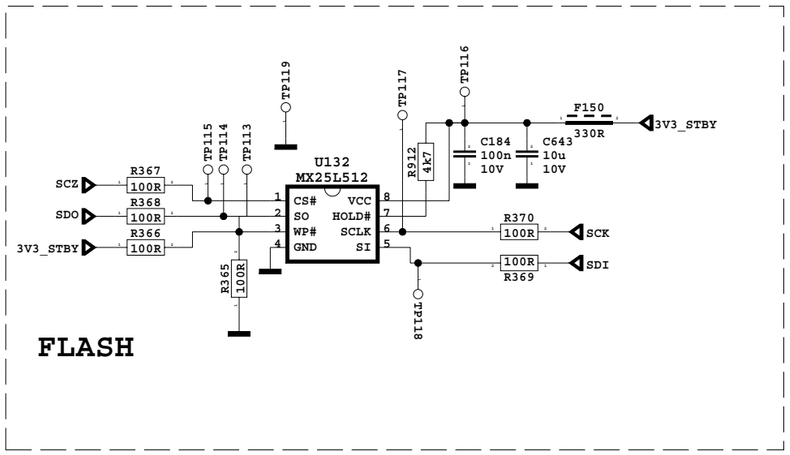
SW_UPDATE_SELECT	
0	DVB_SW_UPDATE
1	ANALOG_SW_UPDATE

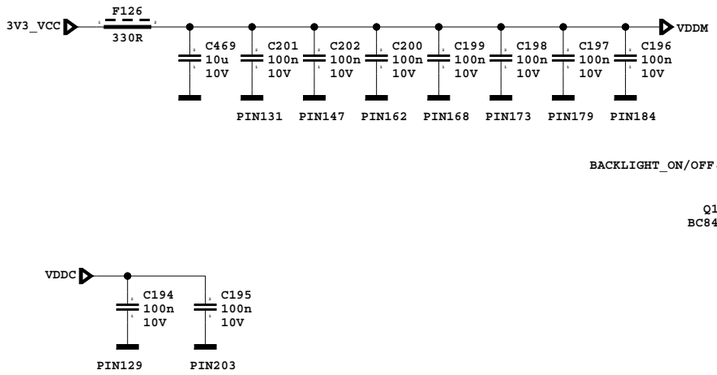


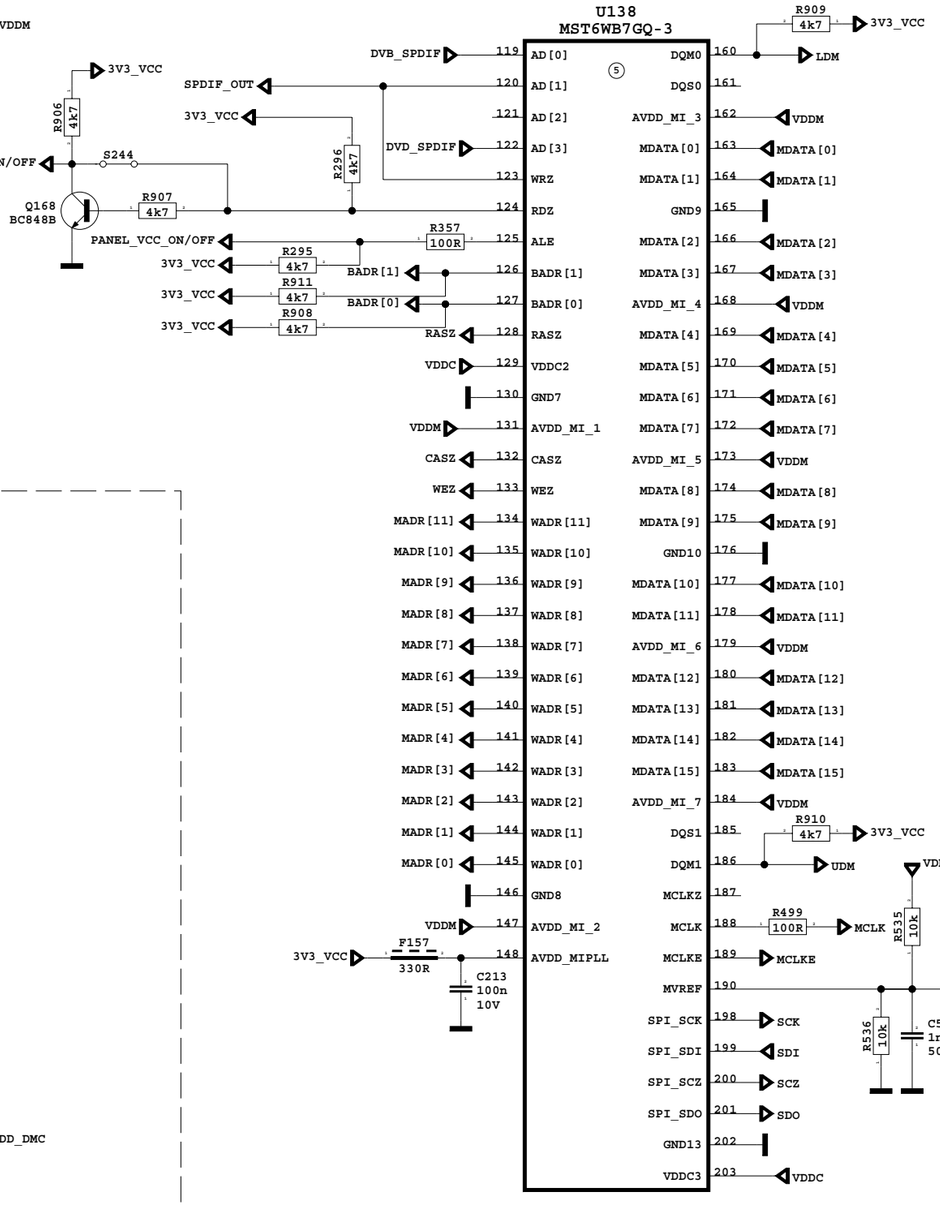




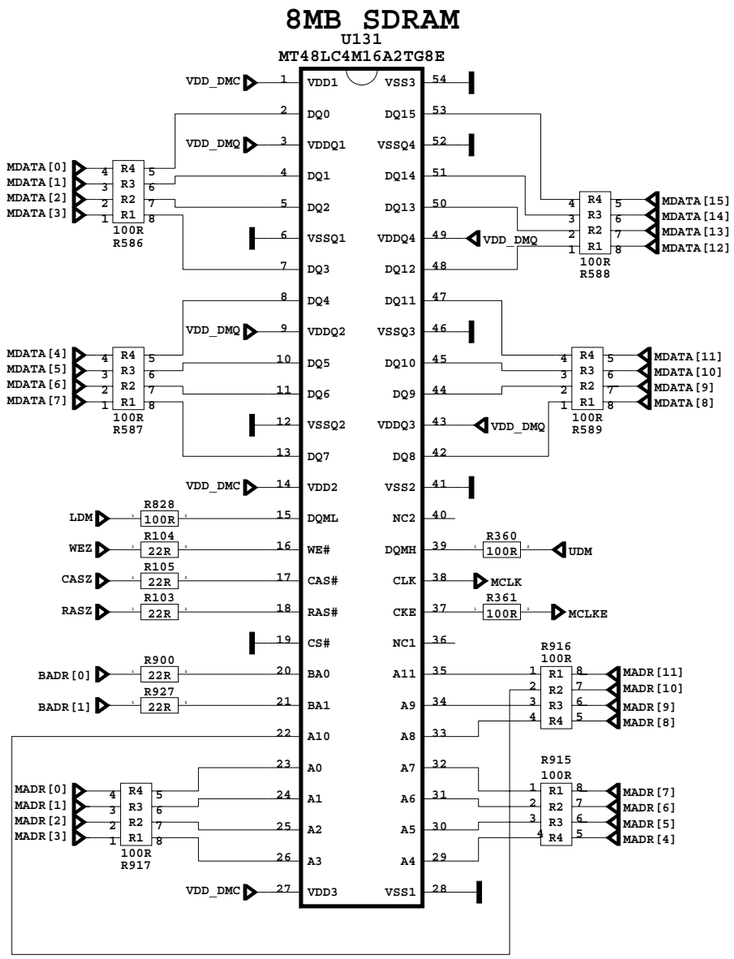
VESTEL	PROJECT NAME : 17MB25	A3
SCH NAME :CONTROLLER		SHEET:5 OF:11
DRAWN BY :ÖNDER GENÇ		4-28-2008_15:57







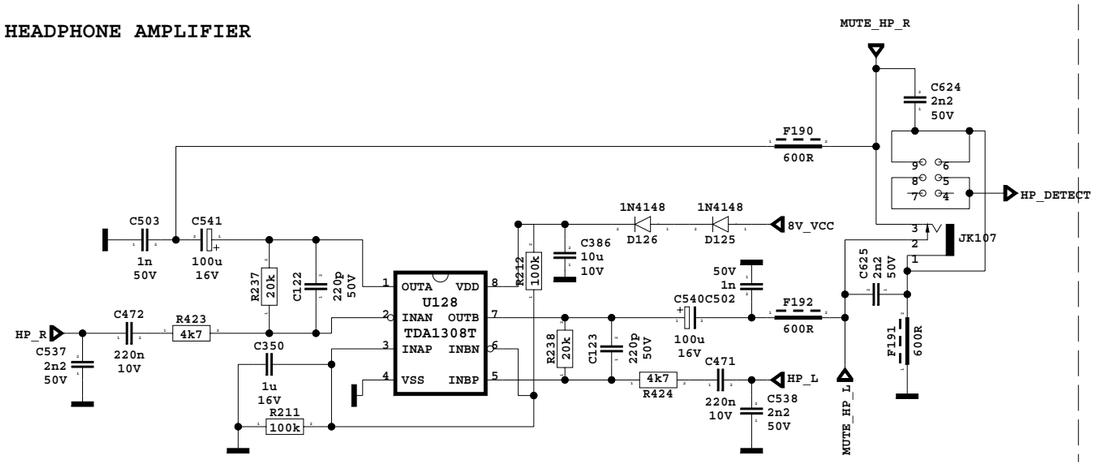
MEMORY



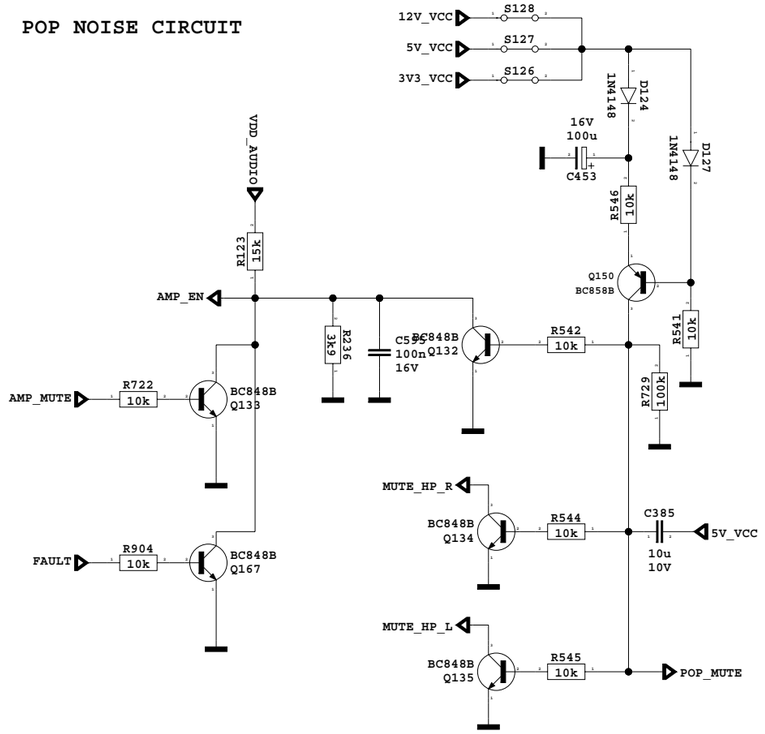
WARNING!!!DON'T USE VIA FOR MCLK AND DATA SIGNALS

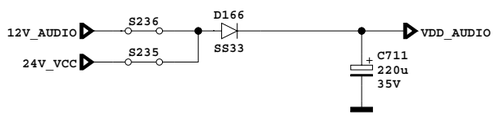
VESTEL	PROJECT NAME : 17MB25	A3
SCH NAME :MEMORY INTERFACE	SHEET:6	OF:11
DRAWN BY :ÖNDER GENÇ	4-28-2008_15:57	

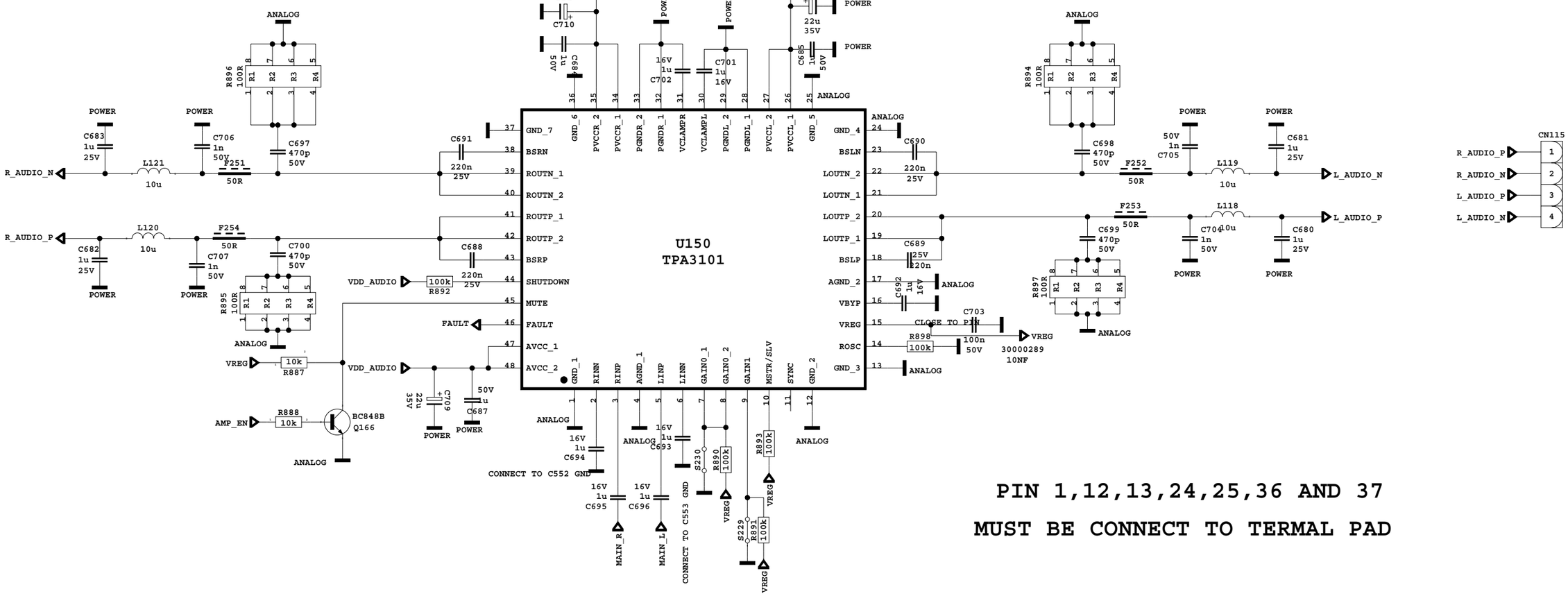
HEADPHONE AMPLIFIER



POP NOISE CIRCUIT





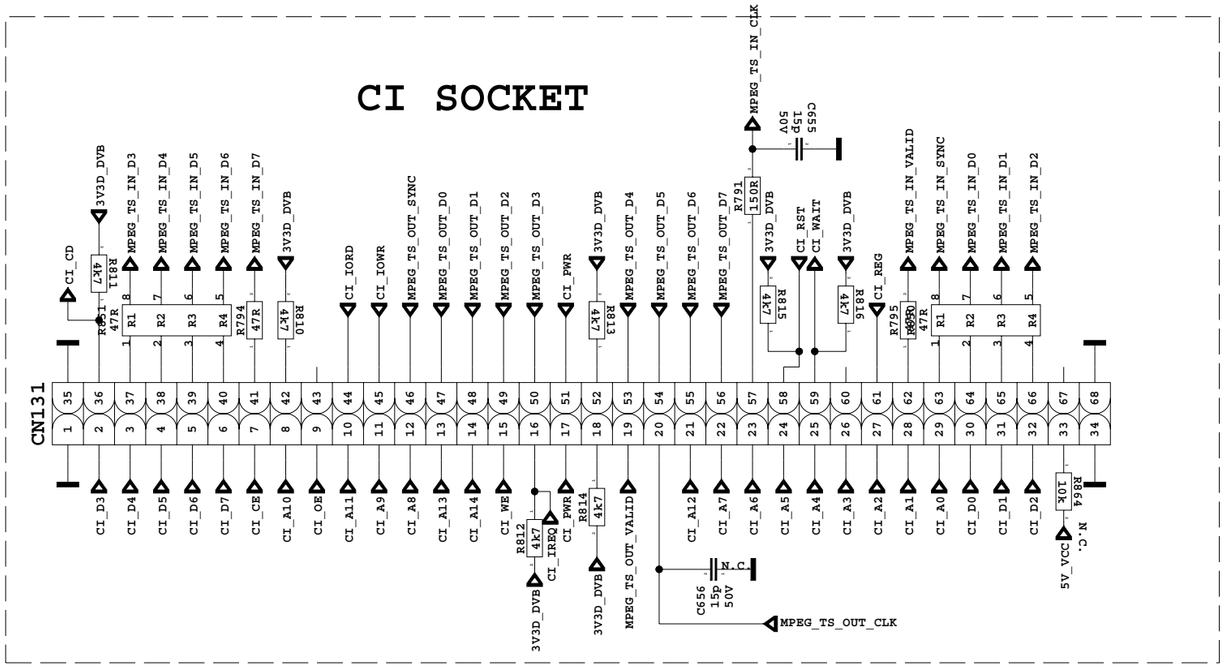


PIN 1,12,13,24,25,36 AND 37

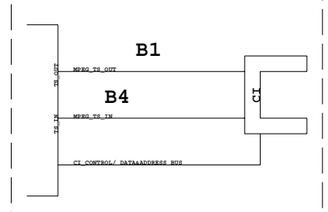
MUST BE CONNECT TO TERMAL PAD

VESTEL	PROJECT NAME : 17MB25	A3
SCH NAME :AUDIO		SHEET:7 OF:11
DRAWN BY :S.SEBNEM TAS		4-28-2008_15:57

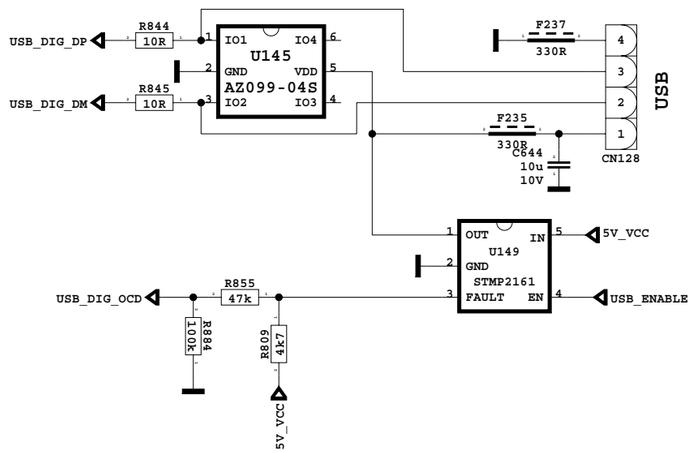
CI SOCKET



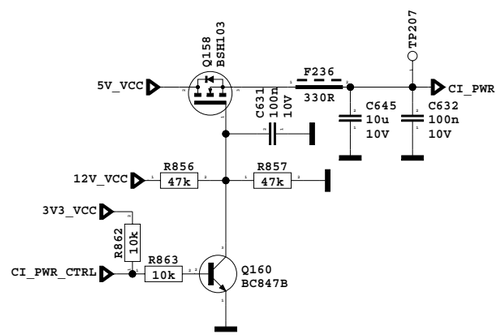
TS ROUTING



USB INTERFACE



CI 5V SWITCH CIRCUIT



VESTEL	PROJECT NAME : 17MB25	A3
SCH NAME :CI		SHEET:8 OF:11
DRAWN BY :MB35 HW GROUP		4-28-2008_15:57

CHEERTEK

MPEG DECODER

FUM Interface

CN109

MPEG_TS_OUT_D0
MPEG_TS_OUT_SYNC
FUM_EN
MPEG_TS_OUT_CLK
DSU_TXD0
DSU_RXD0
MPEG_TS_OUT_VALID

CI CONTROL SIGNALS

CI_REG
CI_IREQ
CI_IOWR
CI_IORD
CI_CE
CI_CD
CI_RST
CI_WAIT
CI_OE
CI_WE
CI_PWR_CTRL

DVB VIDEO FILTER&AMP

U139 FMS6145

ENC_CVBS
ENC_PR
ENC_PB
ENC_Y
DVB_CVBS
DVB_PR
DVB_PB
DVB_Y

Comm.Port

CVBS/YPbPr Video Outputs ==>

U134 MT48LC4M16A2TG8E SDRAM

MD0 MD1 MD2 MD3 MD4 MD5 MD6 MD7 MD8 MD9 MD10 MD11 MD12 MD13 MD14 MD15
MDQM MCLK_SDRAM MCKE MCS# MRAS MCAS MWE MBS0 MBS1 MA10 MA0 MA1 MA2 MA3 MA4 MA5 MA6 MA7 MA8 MA9 MA11 MA12

27MHz VCXO

X102 27MHz

RAM DATA BUS / RAM ADDRESS BUS

MD0 MD1 MD2 MD3 MD4 MD5 MD6 MD7 MDQM MD15 MD14 MD13 MD12 MD11 MD10 MD9 MD8
MCLK_SDRAM
MA12 MA11 MA9 MA8 MA7 MA6 MA5 MA4 MWE
MCAS MRAS MBS0 MBS1 MA10 MA0 MA1 MA2 MA3

CI ADDRESS BUS / CI DATA BUS

CI_A14 CI_A13 CI_A12 CI_A11 CI_A10 CI_A9 CI_A8 CI_A7 CI_A6 CI_A5 CI_A4 CI_A3 CI_A2 CI_A1 CI_A0
CI_D7 CI_D6 CI_D5 CI_D4 CI_D3 CI_D2 CI_D1 CI_D0

SERIAL FLASH

U114 MX25L512

SF_CS SF_DO SF_CLK SF_DIO

U104 CT216T-R

HAD0/GPOE0 HAD1/GPOE1 HAD2/GPOE2 HAD3/GPOE3 HAD4/GPOE4 HAD5/GPOE5 HAD6/GPOE6 HAD7/GPOF7
SF_CS#/FCS# SF_CLK/HA22/GPOD4 SF_DO/HA21/GPOD3 SF_DIO/HA20/GPOD2
GPIO29 GPIO28 GPIO23/CIREG GPIO8/CIOINT# GPIO9/CIIINT# GPIO31/CIOWR# GPIO30/CIORD# GPIO25/CIOCE# GPIO27/CIICE# GPIO24/CIOCD# GPIO26/CIICD# HWAIT/GPIO22 HRD#/CIOE#/GPIO21 HWR#/CIWE# HA15/GPIO15 HA16/CIIIORD#/GPIO16 HA17/CIIOR#/GPIO17 HALE/GPIO20 GPB9/HSYN/KEYDET1 GPB10/VSYN/KEYDET2 GPB8/DSB_DRVVBUS GPB4/DSB_DRVVBUS GPB3/DSPLYCM3 GPB2/DSPLYCM2 GPB1/RXI/DSPLYCM1 GPB0/TXI/DSPLYCM0 VDD33_4 GPB6/DSPLYCLK GPB5/DSPLYDAT GPB7/IR VDD18_3 GPA13/SC1CD GPC8/SC1RST GPC9/SC1PWR GPC7/RX2/SCIDAT GPC6/TX2/SC1CLK GPA3/SCOCD GPC4/SCORST GPC5/SCOPWR GPC3/UART1_TX/SCOCLK GPC2/UART1_RX/SCODAT GPB14/SD/MS_D3 GPB15/SD/MS_D2 GPB11/SD/MMC_CMD GPB12/SD/MMC_CLK GPC14/SD/MMC_DAT GPB13/SD/MMC_WP GPA10/SD/MMC_PWE GPC13/SD/MMC_INS GPC12/SD_PWR GPC11/SD/MS_D1 GPC10/SD/MS_D0 GPA9/SD/MMC_CD GPA8/SD/MMC_CMD GPC0/SD_CD# GPA2/CS2#/TX1/VSYN/PCMCLK GPA1/CS1#/RX1/HSYN/SD_CD# RESET# VDD33_2 GPD0/UART0_RX/GPD0 GPD1/UART0_TX/GPD1 GPD2/TSO_D0/PD0 GPD3/TSO_D1/PD1 GPD4/TSO_D2/PD2 GPD5/TSO_D3/PD3 GPD6/TSO_D4/PD4 GPD7/TSO_D5/PD5 GPD8/TSO_D6/PD6 GPD9/TSO_D7/PD7 GPD10/TSO_D2 GPD11/TSO_D3 GPD12/TSO_D4 GPD13/TSO_D5 GPD14/TSO_D6 GPD15/TSO_D7 TSI_VID/VSYN TSI_SYN/HSYN TSI_CLK/CLKO TSI_D0/PD0 TSI_D1/PD1 TSI_D2/PD2 TSI_D3/PD3 TSI_D4/PD4 TSI_D5/PD5 TSI_D6/PD6 TSI_D7/PD7 VDD33_2 GPD0/TSO_SYN GPD6/TSO_VID GPD7/TSO_CLK GPD5/TSO_D0 GPD8/TSO_D1 GPD9/TSO_D2 GPD10/TSO_D3 GPD11/TSO_D4 GPD12/TSO_D5 GPD13/TSO_D6 GPD14/TSO_D7 GPD15/TSO_D7 TSI_SYN/HSYN TSI_VID/V

17PW26 CONNECTOR

A/D DIMMING SELECTION

CN117

TP196 TP195

30V_VCC 24V_VCC 5V_VCC 3V3_VCC 12V_STBY 12V_AUDIO TP200 TP199 TP197 TP198 TP202 TP201

R339 4k7 R340 4k7 R341 4k7

6V3 100u C507 C506 6V3 100u

ADAPTER OPTIONS

JK103

FS102 7A/32VDC FS103 7A/32VDC

12V_PSU 12V_INV MECH_SWITCH

C659 220n 25V R874 22k C667 220n 25V R873 22k

Q155 IRF7314 R847 10R R846 10R

FS104 7A/32VDC

C642 10u 25V C660 220n 25V F241 60R D175 A81C

U137 MP1583

BS SS IN EN SW COMP GND FB

C358 10n 16V S211 C662 220n 25V C568 22u 25V C567 22u 16V

C519 100n 10V C599 5n6 50V C518 NC 100n 16V R244 3k9 R865 10k

R878 1k R790 30k TP157

D144 SS33 L106 15u C565 22u 16V C566 22u 16V

5V_STBY C668 220n 25V R880 33k R797 47R R881 33k

Q157 FDC642P TP210

MOSFET_CONTROL R818 4k7 C634 100n 10V Q164 BC848B

12V_STBY C669 220n 25V R882 33k R883 33k R798 47R

Q156 FDC642P TP209

MOSFET_CONTROL R817 4k7 C633 100n 10V Q163 BC848B

12V_AUDIO S245

ADAPTER AND IPS15 OPTIONS

U148 MP1583

BS SS IN EN SW COMP GND FB

12V_STBY S227 C666 220n 25V C671 22u C674 22u 16V

C670 10n 16V C635 100n 10V C677 5n6 50V C666 100n 16V NC R803 3k9 R866 10k R886 2k R854 15k TP211

D164 SS33 L116 15u C673 22u 16V C672 22u 16V NC 3V3_STBY

17PW26 OPTIONS

12V_STBY S222 3V3_STBY

3V3_STBY FS105 4A/24VDC C436 220n 25V R337 33k R796 47R R336 33k

Q105 FDC642P TP145 D174 C5V6

MOSFET_CONTROL R338 4k7 C310 100n 10V Q138 BC848B

PAULO DECOUPLING CAPACITORS

3V3_STBY F146 330R C408 10u 10V C307 100n 10V VDDP

1V26_STBY F147 330R C410 10u 10V C308 100n 10V VDDC

3V3_STBY F145 330R C409 10u 10V C306 100n 10V AVDD_33

17IPS17 CONNECTOR

CN126

5V_VCC 3V3_VCC 12V_STBY 5V_STBY 12V_AUDIO 12V_VCC

D156 C5V6 D157 C5V6 D120 C5V6

R345 4k7 DIMMING

R344 4k7 BACKLIGHT_ON/OFF

R343 4k7 STBY_ON/OFF

R342 4k7 STBY_ON/OFF_NOT

MECH_SWITCH

U122 LM1117

IN OUT GND VOUT

12V_VCC C470 47u 16V TP143 8V_VCC R411 2k C452 10u 25V R378 10k R476 1k

STBY_ON/OFF S241 STBY_ON/OFF_NOT S243 MOSFET_CONTROL

SHORT CCT PROTECTION

PROTECT_PANEL Q137 BC848B R708 33k PANEL_VCC 10k R571

R706 33k 8V_VCC 10k R569

D135 BAW56 D136 BAW56 D137 BAW56

3V3_STBY S240 5V_STBY S239

5V_TUN 3V3_VCC 5V_VCC

R565 10k R564 10k R563 10k R562 10k

TP150 PROTECT Q151 BC858B Q136 BC848B

R705 33k 12V_VCC 10k R568 R570 10k 33k 24V_VCC R707 33k 12V_AUDIO R709

PANEL SUPPLY SWITCH

3V3_VCC 5V_VCC 12V_VCC F169 60R F170 60R F171 60R F172 60R

C664 220n 25V C618 220n 25V R700 33k R205 47R R566 33k

C455 100u 25V TP149 PANEL_VCC R699 33k

Q104 FDC642P

PANEL_VCC_ON/OFF R575 10k C309 100n 10V Q139 BC848B

INVERTER SOCKET

BACKLIGHT_ON/OFF TP236 C636 100u 10V

DIMMING TP237 C637 100n 10V

TP238 12V_INV C661 220n 25V C641 10u 25V

CN127

17PW26 OPTIONS

3V3_STBY S210 C665 220n 25V C578 22u 16V C576 22u 16V

U144 MP2112

VINB SW VINA GND EN FB

L110 4u7 TP142 1V26_STBY C575 22u 16V C579 22u 16V NC

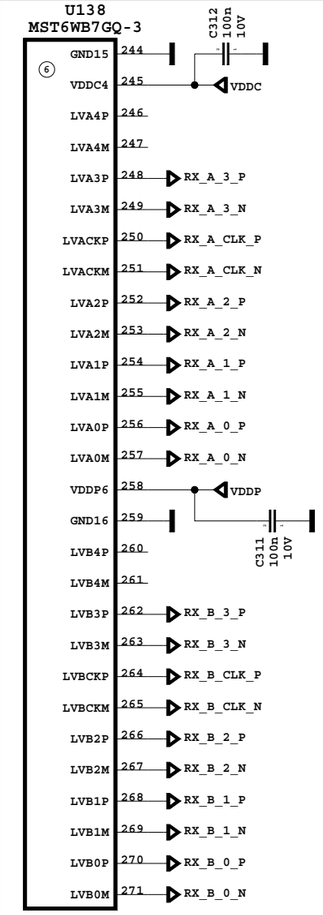
R702 33k C535 1n 50V R249 200k R124 160k 180K olacak S134

U121 LM1117

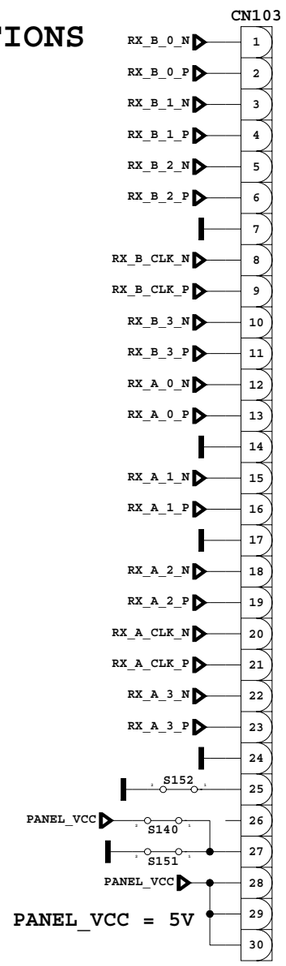
IN OUT GND VOUT

3V3_VCC F222 60R C506 10u 10V TP147 1V8_VCC R721 100R C543 100u 16V R410 47R S228

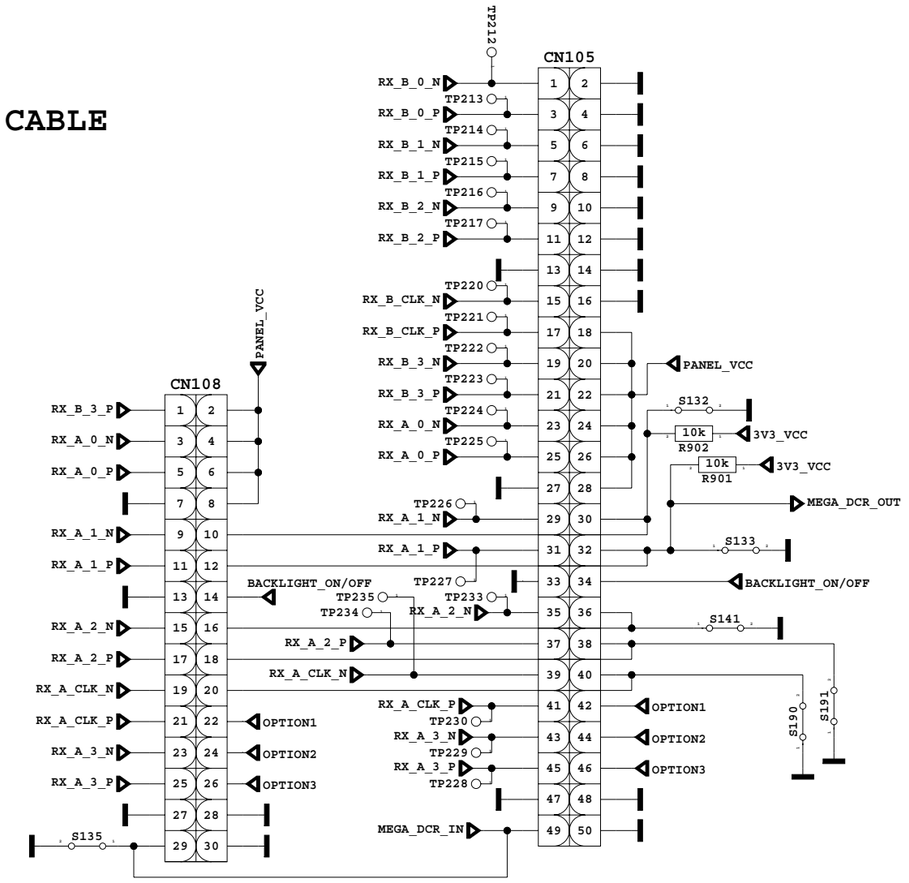
VESTEL	PROJECT NAME : 17MB25	A3
SCH NAME :MB25 POWER		SHEET:10 OF:11
DRAWN BY :ONDER GENC		4-28-2008_15:57



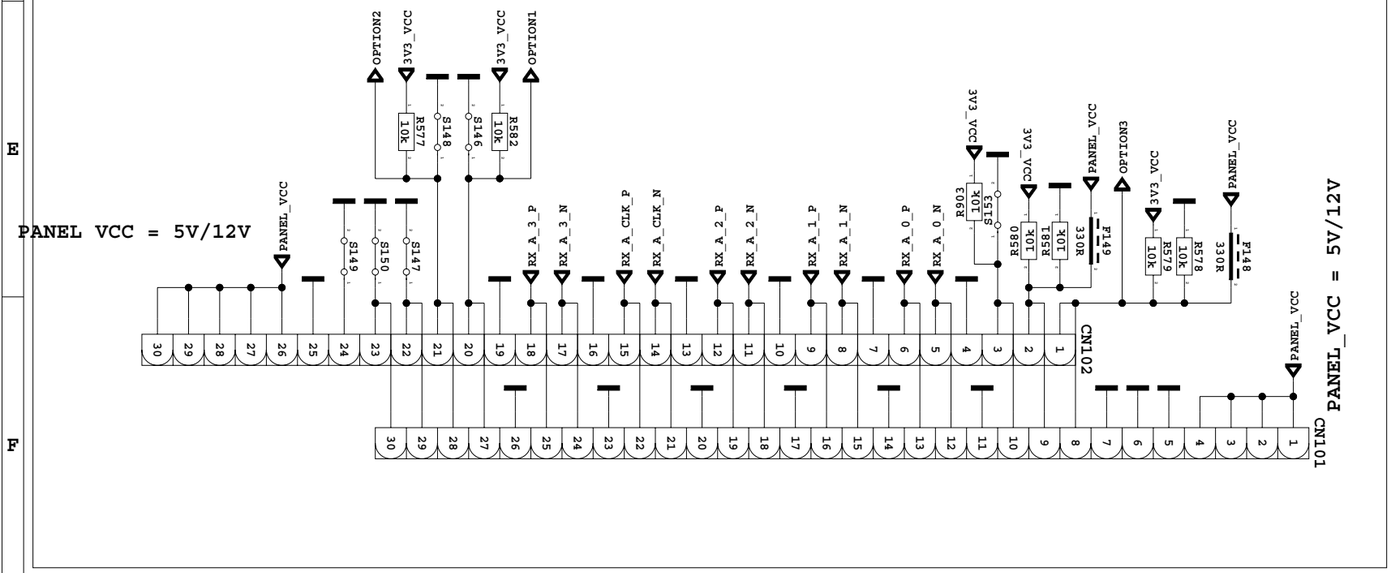
19" TO 22" FFC OPTIONS



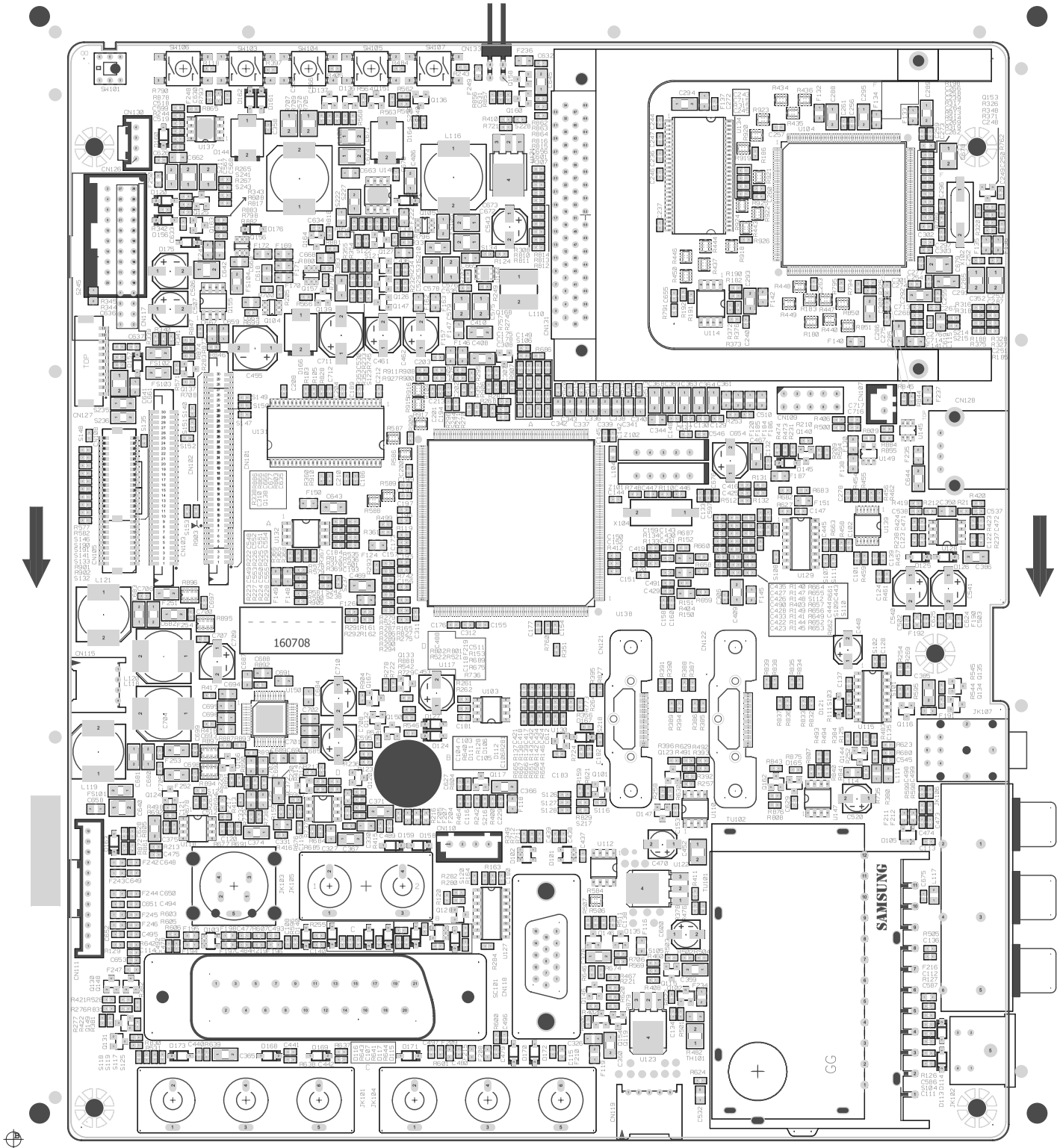
LVDS CABLE

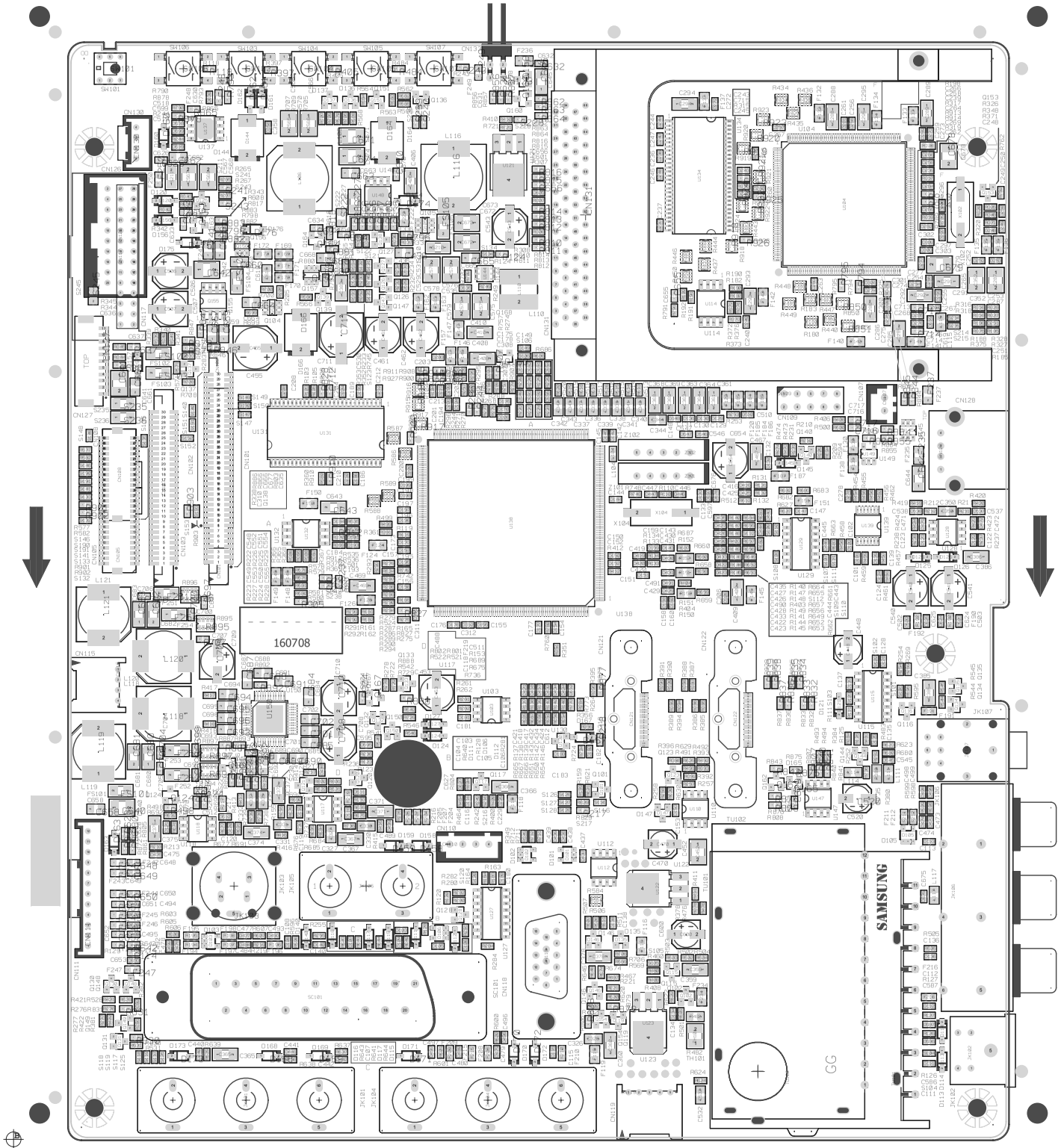


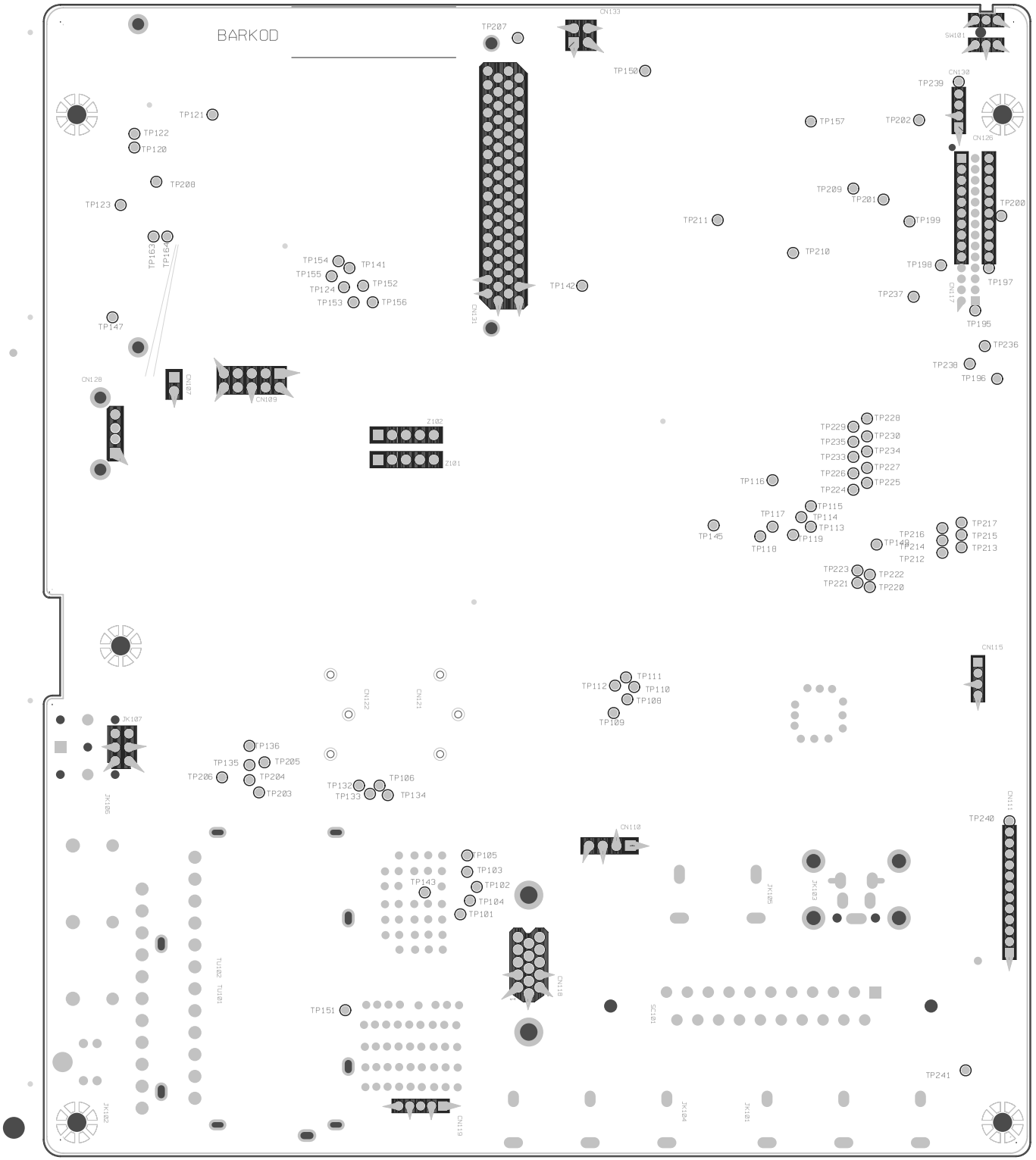
26" TO 32" FFC OPTIONS



VESTEL	PROJECT NAME : 17MB25	A3
SCH NAME :LVDS INTERFACE		SHEET:11 OF:11
DRAWN BY :ONDER GENC		4-28-2008_15:57


160708
SAMSUNG


160708
SAMSUNG


BARKOD
TP207
CN133
TP150
SW101
CN130
TP239
TP157
TP202
CN126
TP121
TP122
TP120
TP200
TP123
TP209
TP201
TP200
TP211
TP199
TP210
TP198
TP197
TP237
CN127
TP195
TP154
TP141
TP155
TP152
TP124
TP153
TP156
TP142
CN131
TP147
TP163
TP164
TP236
TP238
TP196
CN128
CN107
CN109
Z102
Z101
TP228
TP229
TP230
TP235
TP234
TP233
TP227
TP226
TP225
TP224
TP116
TP115
TP117
TP114
TP113
TP145
TP119
TP118
TP148
TP216
TP214
TP212
TP217
TP215
TP213
TP223
TP222
TP221
TP220
CN115
TP111
TP112
TP110
TP108
TP109
CN122
CN121
JK107
TP136
TP135
TP205
TP206
TP204
TP203
TP106
TP132
TP133
TP134
JK105
CN110
TP105
TP103
TP143
TP102
TP104
TP101
CN111
TP240
JK103
JK104
TU102
TU101
CN118
TP151
SC101
JK102
CN119
JK104
JK101
TP241