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## 1-TECHNICAL SPECIFICATIONS, CONNECTIONS and CHASSIS OVERVIEW

### 1.1. Technical Specifications

### 1.1.1 Reception

Tuning System
Color Systems
Sound Systems
A/V Connections
Channel Selections
IF Frequency

Aerial Input

### 1.1.2 Miscellaneous

Audio Output (RMS)
Mains Voltage
Mains Frequency
Ambient Temperature
Maximum Humidity
Power Consumption
Standby Power Consumption
: Digital Multimedia Tuner (PLL)
: PAL SECAM NTSC (Playback)
: B/G D/K L/L'
: SCART AND FRONT AV
: AIR, CABLE : The entire band via frequency search
: B/G, D/K, L : 38.9 MHz
L': 33.4 MHz
$\mathrm{I}: 39.5 \mathrm{MHz}$
: 75 OHM
: $2 \times 2 \mathrm{~W}$
: 220-240 V ( $\pm 10$ \%) (12 VDC 5A Adapter)
: 50/60 Hz ( $\pm 5$ \%)

30 W (for 15" LCD TV), 50 W (for 17" LCD TV) + Adapter power cons.
: <3 W
1.2 Connections


Rear Connections


Side Connection

## ASSEMBLING/DISASSEMBLING PROCEDURE

Disassembly procedure is explained as below. Before disassembling the TV set please read the safety instructions and warning parts of the service manual.

- Turn off LCD TV and plug off the adapter socket
- Remove the connector cover
- Remove screws (8 pieces) to dismount the back cover
- Remove connector between the Inverter PCB and main board.
- Remove headphone connector
- Remove speaker connectors
- Remove side AV connector
- Remove remote and keyboard connectors
- Remove connector between LCD panel and main board
- Remove screws on the main board (7 pieces)

Main board should be free for the fixing procedure. To remove Invertor PCB;

- Remove connectors (4 pieces) between LCD panel and invertor PCB.
- Remove the screws (4 pieces) on invertor PCB Invertor PCB should be free.
Slide out the boards (no screws, straps or other fixing).


## TFT LCD TECHNOLOGY

## Description

The LCD TV is a color active matrix TFT(Thin Film Transistor) liquid crystal display that uses amorphous silicon TFT switching devices. This model is composed of a TFT LCD panel, a driver circuit and a back-light system. The resolution of 15.0(17.0)-inch contains $1,024^{*} 768(1280 * 1024)$ pixel and can display more than 16 millions colors.

## Features

- High contrast radio, High aperture structure
- Wide viewing angle
- High-speed response
- Low power consumption
- CCFTs (Cold Cathode Fluorescent Tube)


## Structure \& Principle Operation of TFT LCD

TFT LCD (Thin Film Transistor Liquid Crystal Display) has

Please follow the assembly instructions explained below;

- Be sure that all cables are free. If necessary fix the cables firmly to avoid any kind of squeezing while placing the boards back.
- Place the board and fix it by screws
- Plug in the sockets coming from remote PCB,
- Plug in the sockets coming from speakers
- Plug in the socket coming from side AV
- Plug in the socket coming from side keyboard
- Plug in the socket coming from side headphone
- Plug in the socket between LCD panel and main board (20. pin should be free)
- Plug in the socket between inverter PCB and main board (assuming that inverter already placed) If inverter is not placed;
- Place the inverter PCB and fix it by screws, be careful about the direction of connector
- Plug in the sockets coming from LCD panel, two connectors at each short edge.
- Place the back cover back to its place (8 screws) and plug in the adepter
- Plug the mains in.
- Turn on the LCD TV.
a sandwich-like structure with liquid crystal filled between two glass plates.
TFT Glass has as many TFTs as the number of pixels displayed, while a Color Filter Glass has color filter, which generates color. Liquid crystals move according to the difference in voltage between the Color Filter Glass and the TFT Glass. The amount of light supplied by Back Light is determined by the amount of movement of the liquid crystals in such a way as to generate color.



## SOLDERING PROCESS

## 1) SMD Components (Surface Mounted Device)

## Desoldering:

Heat up the component from its terminals for 2 or 3 seconds with a soldering iron and afterwards take out the component carefully by means of the tweezers. Remove superfluous solder at the solder surfaces of the components place at pcb by means of desoldering strand or suction de-solder equipment. Never force the component for removing without heating the terminals sufficiently. Unsoldered components should not be used for once more.

## Soldering:

Place the component properly to its position by means of tweezers and solder one side of the component. Then check out the position of the component and be sure if it is soldered to the right place and then solder other side of the component. Terminals of the SMD components must not contact directly to the soldering
iron

## 2)PLCC Components

## Desoldering:

Heat up the terminals of PLCC component for 3 or 5 seconds by means of SMD soldering iron and PLCC desoldering pair (angle $90^{\circ} \mathrm{C}$, Leg: 24 mm ). Take out PLCC component carefully by slightly turning of desoldering tweezers.

## Soldering:

Remove superfluous solder at the solder surfaces of the components placed on pcb by means of de-soldering iron or suction de-solder equipment. Apply flux with low grease content. Place PLCC device on the soldering surface and take care for its correct placement. Secure diagonally by means of two soldering joints. Apply soldering paste along PLCC pins. Short circuits which may occure during soldering process have to be removed immediately with a soldering iron.

## SPECIFICATIONS OF THE CONNECTOR (EURO SCART)

I- Audio output 1. right channel 0.5 VRMS/<1 k 0
2- Audio input 1. right channel 0.5 VRMS (connected to No.6)
3- Audio output 2. left channel 0.5 VRMS (connected to No.1)
4- GND (audio)
5- GND
6- Audio input 2. left channel 0.5 VRMS/>10k 0
7- RGB input, blue (B)
8- Switch signal video (status)
9- GND
10- Reserved for clock signals (not connected)
11- RGB input, green (G)
12- Reserved for remote control (not connected)
13- GND
14- GND switch signal RGB
15- RGB input, red (R)


16- Switch signal RGB
17- GND (video)
18- GND
19- Video output 1 Vpp/75 ohm
20- Video input 1 Vpp/75 ohm
21-Shield





## KEYBOARD

All the keys on the keyboard are used same as the relevant keys on the RC. But navigation in menus is quite different. In order to open Main Menu from keyboard $\mathrm{V}+$ and V - keys must be pressed together. After displaying the menus $\mathrm{P}+$ and P keys will be used as Navigation Up and Navigation Down keys. There is no enter key on the keyboard so V+or V- will be used as Menu Right key if a submenu item is highlighted on the menu. These two keys will also be used as Navigation Left and Navigation Right keys in order to change any highlighted options right side value. To return previous menu V+ and Vkeys should be pressed together.

## 2- SAFETY INSTRUCTIONS AND WARNINGS

## SAFETY INSTRUCTIONS FOR SERVICE REPAIRS

1. Use only the original spare parts with the same specifications for replacement.
2. Safety components, indicated by the symbol, should be replaced by components identical to the original ones.
3. Main leads and connecting leads should be checked for external damage before connection. Insulation must be checked.
4. Parts contributing to the safety of the product must not be damaged or obviously unsuitable. This is valid especially for insulators and insulating parts.
5. Thermally loaded solder pads are to be sucked off and re-soldered.
6. Potentials as high as 1.1 KV are present when this receiver is operating
7. Servicing should not be attempted by anyone who is not thoroughly familiar with precautions necessary when working on high voltage equipment.
8. Keep wire away from the high voltage or high temperature components.
9. When replacing a wattage resistor, keep the resistor 10 mm away from the circuit board.

## HANDLING THE MOS CHIP COMPONENTS

MOS circuit requires special attention with regard to static charges. Static charges may occur with any highly insulated plastics and can be transferred to persons wearing clothes and shoes made of synthetic materials. Protective circuits on the inputs and outputs of MOS circuits give protection to a limited extend only due to time of reaction. Please observe the following instructions to protect the components against ESD.

1. Keep MOS components in conductive package until they are used. Most components must never be stored in styropor materials or plastic magazines.
2. Personnel must not touch the MOS components to avoid electrostatic discharging.
3. Hold the component by the body touching the terminals.
4. Use only grounded instruments for testing and processing purposes.
5. Remove or connect MOS Ics when operating voltage is disconnected.
6. Personnel in charge must make sure that they are connected with the same potential as the mass of the set by a wristband with resistance.

## 3- $\boldsymbol{I}^{2}$ BUS INTERCONNECTION DIAGRAM



## 4- MATRIX PANEL



## 5- TFT PANEL

| SVS DC |
| :---: |
| 21253139 |
| MICROCONTROLLER |
| 8 |
| TXT DECODER |
| ST92195 |


Optional

## 6- FAULT TRACING DIAGRAM-POWER BLOCK

First check the adapter for 12 V and power block for short circuits.


## 7- DVD MODULE (IF AVAILABLE)

Cason MTK loader embedded to chassis and command are delivered to DVD module IR command line connecting to DVD module. To enter service menu of the DVD loader one should press eject, setup, right arrow, left arrow, down arrow, up arrow, display button quickly and respectively. Technical details for the cason loader can be listed as follow.

### 7.1 SAFETY AND HANDLING PRECAUTIONS

1. DO NOT use and store the Loader in dusty, high temperature or high humidity environments.
2. To avoid damage to the Loader by electrostatic dischargers, measuring equipment and operators should be grounded during handling. The user of this unit takes all necessary precautions to avoid ESD (Electro-Static Discharge) failures during handling and assembly of this unit into the end product.
3. Contamination of the PCB might influence the performance. Avoid fingerprints and stains on the PCB and handle the Loader in a clean environment.
4. The mechanism of the Loader has been adjusted carefully during manufacturing. High shocks on this unit may damage and should be avoided.
5. Fast heating (e.g. by bringing the Loader unit from a cold place into a warm and humid room) can result in moisture condensing on the pickup lens, thus influencing the playability for a certain time. Before checking the performance the Loader unit should be stabilized for at least 4 hours.
6. DO NOT disamble the loader to avoid ESD failures and to prevent from contamination.

AC Source Supply:
The Voltage Fluctuation: 110/220 V $\pm 10 \%$ tolerance
The Impulse Noise $: 110 / 220 \mathrm{~V} \pm 10 \%$ tolerance

Applicable Discs Format

|  | Disc Type | Description |
| :---: | :---: | :---: |
| Disc Format | DVD-5 (Single Layer) <br> DVD-9 (Double Layer) <br> DVD-10 (Single Layer Double Side) <br> DVD-18 (Double Layer Double Side) | IS09660 <br> UDE <br> DVD BOOK |
|  | CD | IS09660 <br> RED BOOK (CD-DA) <br> WHITE BOOK (Video-CD) <br> BLUE BOOK (CD Extra) <br> YELLOW BOOK (CD-ROM) <br> ORANGE BOOK (CD-RW, R) |
| Disc Capacity | DVD-5 <br> DVD-9 <br> DVD-10 <br> DVD-18 | $\begin{aligned} & 4.7 \mathrm{~GB} \\ & 8.5 \mathrm{~GB} \\ & 9.4 \mathrm{~GB} \\ & 17 . \mathrm{GB} \end{aligned}$ |
|  | CD | 656 MB (Mode 1) <br> 748 MB (Mode 2) |
| Disc Diameter | DVD/CD | $12 \mathrm{~cm} / 8 \mathrm{~cm}$ |
| Disc Thickness | 1.2 mm |  |
| Disc center Aperture | 15 mm |  |
| Track Gap | 1.6 mm, CD | $0.74 \mu \mathrm{~m}$, DVD |

## Functions

Data Transfer Rate:
DVD 2600kB/sec (max)
CD $870 \mathrm{kB} / \mathrm{sec}$ (max)
Data Buffer Capacity
256KB (DVD/CD)
Error Rate
$10 e^{-15}$ MAX (DVD), $10 e^{-12}$ MAX (CD)
Reading Time
Starting procedure (Less than 15seconds)
Stopping procedure (Less than 2 Seconds)

## Laser Specifications

|  |  | DVD | CD |
| :--- | :--- | :--- | :--- |
| Laser wavelength | $650-665 \mathrm{~nm}$ | $790+20 \mathrm{~nm}$ |  |
| Laser power | 0.5 mW | 0.7 mW |  |
| Object <br> lens | Lens | Non-spherical lens |  |
| Length of Ray <br> Coil 0.6 mm 0.47 mm  <br>  Moving Range 1.71 mm 1.35 mm <br> Focus Astigmatism   <br> Searching Phase difference detection Three spot tracking  |  |  |  |

## Disc Loading Mode

Motor- driven front-loading tray
Disc Fixing
Beam magnetic fixation
Reliability
Mean Time Between Failure (MTBF): Not less than 2,000 hours
Mean Time To Repair (MTTR): 0.5 hours

## Working Environment

Temperature and Humidity
Operating temperature $\quad 5-$ to 45 -
Storage temperature - 20 - to 60 -
Operating temperature varying 11-/hour(max)
Storage temperature varying 20-/hour(max)
Operating humidity $10 \%$ to $70 \%$
Storage humidity 5\% to 80\%
Vibration
Reading data state
Playing CD audio state
Standby
$\begin{array}{lcl}0.2 \mathrm{~g} & 10-30 \mathrm{~Hz} \text { sine wave } \\ & 0.15 \mathrm{~g} & 10-30 \mathrm{~Hz} \text { random } \\ 2.4 \mathrm{~g} & 10-30 \mathrm{~Hz} \text { random }\end{array}$
Striking
Standby state $100 \mathrm{~kg} \quad 6 \mathrm{~ms}$ half sine-wave (in $\mathrm{X}, \mathrm{Y}$ and Z directions)
Noise
Not more than 45 dB in one meter away

## 8- SERVICE MENU ADJUSTMENT

Service menu adjustment is required when an empty NVM replaced or any option bit or geometry adjustment is requested. Option bytes are available and simple based on hardware dependencies. If panel replaced by new one adjustment is not necessary if the new panel is same brand and version. Otherwise some modifications is mandatory. Option list is as follow; TunerB1, TunerB2, Secam, DVD AV., PC AV., No. Sig. Tim, 17-15, Child lock.

- TunerB1 and TunerB2 are used for the defining tuner. Default tuner is Samsung TCPQ9091PD27D AFH or Samsung TCPQ9091PD27D(S) AMC with RT08 resistance.
- Both are defined by 00.
- If dvd is available then the DVD AV bit should be 1.
- If VGA connection is supported via hardware then the software adjusted according to this facility by this bit. Therefore is VGA connection is available then this bit should be set.
- No signal timer is customer depended bit. If bit is set then set activate no signal timer.
- $17-15$ bit used for defining the panel size. If 17 " panel then this bit should be 0 . Conversely if 15 " panel is used then this bit should be 1 .
- If child lock bit is enabled then child lock option will be available.

General Features Of 15 " TFT LCD Panel

| Active Screen Size | 15.0 inches diagonal |
| :--- | :--- |
| Outline Dimension | $304.1(\mathrm{H}) \times 228.1(\mathrm{~V}) \mathrm{mm}(\mathrm{Typ})$. |
| Pixel Pitch | $0.297 \mathrm{~mm} \times 0.297 \mathrm{~mm} \times$ RGB |
| Pixel Format | 1024 horiz. By 768 vert. Pixels RGB strip arrangement |
| Color Depth | 16.2 M colors |
| Luminance, White | $450 \mathrm{~cd} / \mathrm{m2}$ (Center 1 points typ.) |
| Viewing Angle(CR>10) | View Angle Free (R/L 130(Typ.), U/D 100(Typ.)) |
| Power Consumption | Total TBD Watt (Typ.) [LCM 4.14W / Inverter TBD W ] |
| Weight | TBD g (Typ.) |
| Display Operating Mode | Normally White |
| Surface Treatment | Haze 25\%, Hard-Coating (3H) |


| Active Screen Size | 17.1 inches(434.38mm) diagonal 15:9 |
| :--- | :--- |
| Outline Dimension | $400.0(\mathrm{H}) \times 258.0(\mathrm{~V}) \times 22.0(\mathrm{D}) \mathrm{mm}($ Typ. $)$ |
| Pixel Pitch | $0.291 \mathrm{~mm} \times 0.291 \mathrm{~mm}$ |
| Pixel Format | 1280 horiz. By 768 vert. Pixels RGB stripe arrangement |
| Color Depth | 8 -bits, 16,7M colors |
| Luminance, White | $450 \mathrm{~cd} / \mathrm{m} 2($ Center 1 point (Typ.)) |
| Viewing Angle (CR>10) | Viewing Angle Free [R/L 176Typ.), U/D 176(Typ.)] |
| Power Consumption | Total 30.4 Watt(Typ.), (2.2 Watt@VLCD,28.2 Watt@450cd/[LAMP=7mA]) |
| Weight | $2,200 \mathrm{~g}$ (Typ.) , 2,350 g (Max) |
| Display Operating Mode | Transmissive mode, normally black |
| Surface Treatment | Hard coating(3H) \& Anti-glare treatment of the front polarizer |

## ELECTRICAL CHARACTERISTICS FOR LF18C (refer to the test circuits, $\mathrm{Tj}=25 \mathrm{oC}$, $\mathrm{Ci}=0.1 \mathrm{mF}, \mathrm{Co}=\mathbf{2 . 2} \mathbf{~ m F}$ unless otherwise specified)

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Vo | Output Voltage | $\begin{aligned} & \mathrm{I} 0=50 \mathrm{~mA}, \mathrm{Vi}=3.5 \mathrm{~V} \\ & \mathrm{I} 0=50 \mathrm{~mA}, \mathrm{Vi}=3.5 \mathrm{~V}-25<\mathrm{Ta}<850 \mathrm{C} \end{aligned}$ | $\begin{aligned} & \hline 1.764 \\ & 1.728 \\ & \hline \end{aligned}$ | 1.8 | $\begin{array}{\|l\|} \hline 1.836 \\ 1.872 \end{array}$ | $\begin{aligned} & \hline \mathrm{V} \\ & \mathrm{~V} \end{aligned}$ |
| Vi | Operating Input Voltage | $10=500 \mathrm{~mA}$ | 3 |  | 16 | V |
| lout | Output Current Limit |  |  | 1 |  | A |
| Vo | Line Regulation | $\mathrm{Vi}=2.8$ to $16 \mathrm{~V}, 10=5 \mathrm{~mA}$ |  | 2 | 12 | mV |
| Vo | Load Regulation | $\mathrm{Vi}=3.3 \mathrm{~V} \mathrm{Io}=5$ to 500 mA |  | 2 | 10 | mV |
| ld | Quiescent Current | ON MODE |  |  |  |  |
|  |  | $\mathrm{Vi}=2.5$ to $16 \mathrm{~V} \mathrm{lo}=0 \mathrm{~mA}$ |  | 0.5 | 1 | mA |
|  |  | $\mathrm{Vi}=3.1$ to $16 \mathrm{~V} \mathrm{Io}=500 \mathrm{~mA}$ |  |  | 12 | mA |
|  |  | OFF MODE Vi $=6 \mathrm{~V}$ |  | 50 | 100 | mA |
| SVR | Supply Voltage Rejection | $10=5 \mathrm{~mA} \mathrm{Vi}=3.5 \mathrm{~V} \pm 1 \mathrm{~V}$ |  |  |  |  |
|  |  | $\mathrm{f}=120 \mathrm{~Hz}$ |  | 82 |  | dB |
|  |  | $\mathrm{f}=1 \mathrm{KHz}$ |  | 77 |  | dB |
|  |  | $\mathrm{f}=10 \mathrm{KHz}$ |  | 60 |  | dB |
| eN | Output Noise Voltage | $\mathrm{B}=10 \mathrm{~Hz}$ to 100 KHz |  | 50 |  | mV |
| Vd | Dropout Voltage | $10=200 \mathrm{~mA}$ |  | 0.7 |  | V |
| Vil | Control Input Logic Low | $=-40<\mathrm{Ta}<1250 \mathrm{C}$ |  |  | 0.8 | V |
| Vih | Control Input Logic High | $=-40<\mathrm{Ta}<1250 \mathrm{C}$ | 2 |  |  | V |
| li | Control Input Current | $\mathrm{Vi}=6 \mathrm{~V}, \mathrm{Vc}=6 \mathrm{~V}$ |  | 10 |  | mA |
| CO | Output Bypass Capacitance | $E S R=0.1$ to $10 \_\mathrm{lo}=0$ to 500 mA | 2 | 10 |  | mF |

ELECTRICAL CHARACTERISTICS FOR LF33AB (refer to the test circuits, $\mathrm{Tj}=25 \mathrm{oC}$, $\mathbf{C i}=0.1 \mathrm{mF}, \mathrm{Co}=2.2 \mathrm{mF}$ unless otherwise specified)

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Vo | Output Voltage | $10=50 \mathrm{~mA}, \mathrm{Vi}=5.3 \mathrm{~V}$ | 3.267 | 3.3 | 3.333 | V |
|  |  | $10=50 \mathrm{~mA}, \mathrm{Vi}=5.3 \mathrm{~V}-25<\mathrm{Ta}<850 \mathrm{C}$ | 3.234 |  | 3.366 | V |
| Vi | Operating Input Voltage | $10=500 \mathrm{~mA}$ |  |  | 16 | V |
| lo ut | Output Current Limit |  |  | 1 |  | A |
| DVo | Line Regulation | $\mathrm{Vi}=4.3$ to $16 \mathrm{~V}, \mathrm{lo}=5 \mathrm{~mA}$ |  | 3 | 16 | mV |
| DVo | Load Regulation | $\mathrm{Vi}=4.6 \mathrm{~V} \mathrm{Io}=5$ to 500 mA |  | 3 | 16 | mV |
| Id | Quiescent Current | ON MODE |  |  |  |  |
|  |  | $\mathrm{Vi}=4.3$ to $16 \mathrm{~V} \mathrm{Io}=0 \mathrm{~mA}$ |  | 0.5 | 1 | mA |
|  |  | $\mathrm{Vi}=4.6$ to $16 \mathrm{~V} \mathrm{Io}=500 \mathrm{~mA}$ |  |  | 12 | mA |
|  |  | OFF MODE Vi $=6 \mathrm{~V}$ |  | 50 | 100 | mA |
| SVR | Supply Voltage Rejection | $10=5 \mathrm{~mA} \mathrm{Vi}=5.3 \mathrm{~V} \pm 1 \mathrm{~V}$ |  |  |  |  |
|  |  | $\mathrm{f}=120 \mathrm{~Hz}$ |  | 80 |  | dB |
|  |  | $\mathrm{f}=1 \mathrm{KHz}$ |  | 75 |  | dB |
|  |  | $\mathrm{f}=10 \mathrm{KHz}$ |  | 65 |  | dB |
| eN | Output Noise Voltage | $\mathrm{B}=10 \mathrm{~Hz}$ to 100 KHz |  | 50 |  | mV |
| Vd | Dropout Voltage | $10=200 \mathrm{~mA}$ |  | 0.2 | 0.35 | V |
|  |  | $10=500 \mathrm{~mA}$ |  | 0.4 | 0.7 | V |
| Vil | Control Input Logic Low | $-40<\mathrm{Ta}<1250 \mathrm{C}$ |  |  | 0.8 | V |
| Vih | Control Input Logic High | $-40<\mathrm{Ta}<1250 \mathrm{C}$ | 2 |  |  | V |
| li | Control Input Current | $\mathrm{Vi}=6 \mathrm{~V}, \mathrm{Vc}=6 \mathrm{~V}$ |  | 10 |  | mA |
| CO | Output Bypass Capacitance | ESR $=0.1$ to $10 \mathrm{~W} \mathrm{Io}=0$ to 500 mA | 2 | 10 |  | mF |

9- AD9884A

## 100 MSPS/140 MSPS Analog Flat Panel Interface

## FEATURES

140 MSPS Maximum Conversion Rate
500 MHz Analog Bandwidth
0.5 V to 1.0 V Analog Input Range

400 ps p-p PLL Clock Jitter
Power-Down Mode
3.3 V Power Supply
2.5 V to 3.3 V Three-State CMOS Outputs

Demultiplexed Output Ports
Data Clock Output Provided
Low Power: 570 mW Typical
Internal PLL Generates CLOCK from HSYNC
Serial Port Interface
Fully Programmable
Supports Alternate Pixel Sampling for Higher-
Resolution Applications

## APPLICATIONS

RGB Graphics Processing
LCD Monitors and Projectors
Plasma Display Panels
Scan Converters

FUNCTIONAL BLOCK DIAGRAM


## GENERAL DESCRIPTION

The AD9884A is a complete 8 -bit 140 MSPS monolithic analog interface optimized for capturing RGB graphics signals from personal computers and workstations. Its 140 MSPS encode rate capability and full-power analog bandwidth of 500 MHz supports display resolutions of up to $1280 \cdot 1024$ (SXGA) at 75 Hz with sufficient input bandwidth to accurately acquire and digitize each pixel.
To minimize system cost and power dissipation, the AD9884A includes an internal 1.25 V reference, PLL to generate a pixel clock from HSYNC, and programmable gain, offset and clamp circuits. The user provides only a 3.3 V power supply, analog input, and HSYNC signals. Threestate CMOS outputs may be powered by a supply between 2.5 V and 3.3 V .

The AD9884A's on-chip PLL generates a pixel clock from the HSYNC input. Pixel clock output frequencies range from 20 MHz to 140 MHz . PLL clock jitter is typically 400 ps $p-p$ relative to the input reference. When the COAST signal is presented, the PLL maintains its output frequency in the
absence of HSYNC. A 32 -step sampling phase adjustment is provided. Data, HSYNC and Data Clock output phase relationships are always maintained. The PLL can be disabled and an external clock input provided as the pixel clock.
A clamp signal is generated internally or may be provided by the user through the CLAMP input pin. This device is fully programmable via a two-wire serial port.
Fabricated in an advanced CMOS process, the AD9884A is provided in a space-saving 128 -lead MQFP surface mount plastic package and is specified over a $0^{\circ} \mathrm{C}$ to $+70^{\circ} \mathrm{C}$ temperature range.

AD9884A-
VD = 3.3 V, VDD = 3.3 V, PVD = 3.3 V, ADC Clock Frequency = Maximum, PLL Clock SPECIFICATIONS

Frequency $=$ Maximum, Control Registers Programmed to Default State)


| Parameter | Temp | Test Level <br> Level | AD9884AKS-100 |  |  | AD9884AKS-140 |  |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | Min | Typ | Max | Min | Typ | Max |  |
| POWER SUPPLY |  |  |  |  |  |  |  |  |  |
| $V_{D}$ Supply Voltage | Full | IV | 3.0 | 3.3 | 3.6 | 3.0 | 3.3 | 3.6 | V |
| VDD Supply Voltage | Full | IV | 2.2 | 3.3 | 3.6 | 2.2 | 3.3 | 3.6 | V |
| PV ${ }_{\text {D }}$ Supply Voltage | Full | IV | 3.0 | 3.3 | 3.6 | 3.0 | 3.3 | 3.6 | V |
| ID Supply Current ( $\mathrm{V}_{\mathrm{D}}$ ) | $25^{\circ} \mathrm{C}$ | V |  | 125 |  |  | 135 |  | mA |
| IDD Supply Current (VDD) ${ }^{3}$ | $25^{\circ} \mathrm{C}$ | V |  | 33 |  |  | 47 |  | mA |
| IPVD Supply Current (PVD) | $25^{\circ} \mathrm{C}$ | V |  | 15 |  |  | 15 |  | mA |
| Total Power Dissipation | Full | VI |  | 570 | 675 |  | 650 | 775 | mW |
| Power-Down Supply Current | Full | VI |  | 2.0 | 25 |  | 2.0 | 25 | mA |
| Power-Down Dissipation | Full | VI |  | 6.6 | 82.5 |  | 6.6 | 82.5 | mW |
| DYNAMIC PERFORMANCE |  |  |  |  |  |  |  |  |  |
| Analog Bandwidth, Full Power | $25^{\circ} \mathrm{C}$ | V |  | 500 |  |  | 500 |  | MHz |
| Transient Response | $25^{\circ} \mathrm{C}$ | V |  | 2 |  |  | 2 |  | ns |
| Overvoltage Recovery Time | $25^{\circ} \mathrm{C}$ | V |  | 1.5 |  |  | 1.5 |  | ns |
| Signal-to-Noise Ratio (SNR) ${ }^{4}$ | $25^{\circ} \mathrm{C}$ | I | 44.0 | 46.5 |  | 43.5 | 46.2 |  | dB |
| (Without Harmonics) $\mathrm{fIN}=40.7 \mathrm{MHz}$ | Full | V |  | 46.0 |  |  | 45.0 |  | dB |
| Crosstalk | Full | V |  | 60 |  |  | 60 |  | dBc |
| THERMAL CHARACTERISTICS |  |  |  |  |  |  |  |  |  |
| $\varnothing_{\mathrm{JC}}$-Junction-to-Case <br> Thermal Resistance |  | V |  | 8.4 |  |  | 8.4 |  | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| $\varnothing$ JA-Junction-to-Ambient <br> Thermal Resistance |  | V |  | 35 |  |  | 35 |  | - ${ }^{\circ} / \mathrm{W}$ |

## NOTES

${ }^{1}$ VCORNGE $=01$, CURRENT $=001$, PLLDIV $=1693_{10}$.
${ }^{2}$ VCORNGE $=10$, CURRENT $=110$, PLLDIV $=160010$.
${ }^{3}$ DEMUX $=1$; DATACK and DATACK load $=15 \mathrm{pF}$; Data load $=5 \mathrm{pF}$.
${ }^{4}$ Using external pixel clock.
Specifications subject to change without notice. $\varnothing$


## 10- TDA7057AQ

## $2 \times 5$ W stereo BTL Audio Output Amplifier with DC Volume Control

## FEATURES

- DC volume control
- Few external components
- Mute mode
- Thermal protection
- Short-circuit proof
- No switch-on and switch-off clicks
- Good overall stability
- Low power consumption
- Low HF radiation
- ESD protected on all pins.


## GENERAL DESCRIPTION

The TDA7057AQ is astereo BTL output amplifier with DC volume control. The device is designed for use in TV and monitors, but are also suitable for battery-fed portable recorders and radios.

## Missing Current Limiter (MCL)

A MCL protection circuit is built-in. The MCL circuit is activated when the difference in current between the output terminal of each amplifier exceeds 100 mA (typical 300 mA ). This level of 100 mA allows for headphone applications (single-ended).

## QUICK REFERENCE DATA

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
| :--- | :--- | :--- | :--- | :--- | :--- | :---: |
| $V_{P}$ | supply voltage |  | 4.5 | - | 18 | V |
| $\mathrm{P}_{\text {out }}$ | output power | $\mathrm{V}_{\mathrm{p}}=12 \mathrm{~V} ; \mathrm{R}_{\mathrm{L}}=16 \Omega$ | 3.0 | 3.5 | - | W |
|  |  | $\mathrm{V}_{\mathrm{p}}=12 \mathrm{~V} ; \mathrm{R}_{\mathrm{L}}=8 \Omega$ | - | 5.3 | - | W |
| $\mathrm{G}_{\mathrm{V}}$ | voltage gain |  | 39.5 | 40.5 | 41.5 | dB |
| $\mathrm{G}_{\mathrm{C}}$ | gain control |  | 68.0 | 73.5 | - | dB |
| $\mathrm{I}_{\mathrm{q}(\text { tot })}$ | total quiescent current | $\mathrm{V}_{\mathrm{p}}=12 \mathrm{~V} ; \mathrm{R}_{\mathrm{L}}=\infty$ | - | 22 | 25 | mA |
| THD | total harmonic current | $\mathrm{P}_{\text {out }}=0.5 \mathrm{~W} \mathrm{~W}$ | - | 0.3 | 1 | $\%$ |


| TYPE | PACKAGE |  |  |  |  |
| :--- | :--- | :--- | :---: | :---: | :---: |
|  | NAME | DESCRIPTION |  |  | VERSION |
| TDA7057AQ | DBS13P | Plastic DIL-bent-SIL power package; 13 leads (lead length 12 mm ) | SOT141-6 |  |  |


| SYMBOL | PIN | DESCRIPTION |
| :--- | :---: | :--- |
| VC1 | 1 | DC volume contol 1 |
| n.c. | 2 | not connected |
| $\mathrm{V}_{I_{(1)}}$ | 3 | voltage input 1 |
| $\mathrm{V}_{\mathrm{P}}$ | 4 | positive supply voltage |
| $\mathrm{V}_{I_{(2)}}$ | 5 | voltage input 2 |
| SGND | 6 | signal ground |
| VC2 | 7 | DC volume contol 2 |
| OUT2+ | 8 | positeve output 2 |
| PGND2 | 9 | power ground 2 |
| OUT2- | 10 | negative output 2 |
| OUT1- | 11 | negative output 1 |
| PGND1 | 12 | powwer ground 1 |
| OUT1+ | 13 | positive output 1 |

$$
\begin{aligned}
& \text { Pin Configuration }
\end{aligned}
$$


(1) This capacitor can be omittedfifelter malloytic capacitor is connected close to pin 5 .
(2) $\mathrm{R}=16 \Omega$.

## FUNCTIONAL DESCRIPTION

The TDA7057AQ is a stereo output amplifiers with two DC volume control stages. The device is designed for TV and monitors, but also suitable for battery-fed portable recorders and radios.
In conventional DC volume control circuits the control or input stage is AC coupled to the output stage via external capacitors to keep the offset voltage low.
In the TDA7057AQ the two DC volume control stages are integrated into the input stages so that no coupling capacitors are required and a low offset voltage is still maintained. The minimum supply voltage also remains low.
The BTL principle offers the following advantages:

- Lower peak value of the supply current
- The frequency of the ripple on the supply voltage is twice the signal frequency.
Consequently, a reduced power supply with smaller capa
citors can be used which results in cost reductions.
For portable applications there is a trend to decrease the supply voltage, resulting in a reduction of output power at conventional output stages. Using the BTL principle increases the output power.
The maximum gain of the amplifier is fixed at 40.5 dB .
The DC volume control stages have a logarithmic control characteristic. Therefore, the total gain can be controlled from +40.5 dB to -33 dB . If the DC volume control voltage falls below 0.4 V , the device will switch to the mute mode. The amplifier is short-circuit protected to ground, Vp and across the load. A thermal protection circuit is also implemented. If the crystal temperature rises above 150 oC the gain will be reduced, thereby reducing the output power. Special attention is given to switch-on and switch-off clicks, low HF radiation and a good overall stability.


## ST92195B

## 32-64K ROM HCMOS MCU WITH ON-SCREEN-DISPLAY AND TELETEXT DATA SLICER

- Register File based 8/16 bit Core Architecture with RUN, WFI, SLOW and HALT modes
- $0^{\circ} \mathrm{C}$ to $+70^{\circ} \mathrm{C}$ operating temperature range
- Up to 24 MHz . operation @ $5 \mathrm{~V} \pm 10 \%$
- Min. instruction cycle time: 165ns at 24 MHz .
- 32, 48, 56 or 64 Kbytes ROM
- 256 bytes RAM of Register file (accumulators or index registers)
- 256 bytes of on-chip static RAM
- 2, 6 or 8 Kbytes of TDSRAM (Teletext and Display Storage RAM)
- 28 fully programmable I/O pins
- Serial Peripheral Interface
- Flexible Clock controller for OSD, Data Slicer and Core clocks running from a single low frequency external crystal.
- Enhanced display controller with 26 rows of 40/80 characters
- Serial and Parallel attributes
- $10 \times 10$ dot matrix, 512 ROM characters, definable by user
$-4 / 3$ and $16 / 9$ supported in $50 / 60 \mathrm{~Hz}$ and 100/ 120 Hz mode
- Rounding, fringe, double width, double height, scrolling, cursor, full background color, halfintensity color, translucency and half-tone modes
- Teletext unit, including Data Slicer, Acquisition Unit and up to 8 Kbytes RAM for data storage
- VPS and Wide Screen Signalling slicer (on some devices)
- Integrated Sync Extractor and Sync Controller
- 14-bit Voltage Synthesis for tuning reference voltage
- Up to 6 external interrupts plus one NonMaskable Interrupt
- $8 \times 8$-bit programmable PWM outputs with 5 V open-drain or push-pull capability
- 16-bit watchdog timer with 8-bit prescaler
- One 16-bit standard timer with 8-bit prescaler
- 4-channel A/D converter; 5-bit guaranteed


PSDIP56


TQFP64
See end of Datasheet for ordering information

- Rich instruction set and 14 addressing modes
- Versatile development tools, including Assembler, Linker, C-compiler, Archiver, Source Level Debugger and hardware emulators with Real-Time Operating System available from third parties
- Pin-compatible EPROM and OTP devices available


## Device Summary

| Device | Program Memory | TDS RAM | VPS/ <br> WSS | Package |
| :---: | :---: | :---: | :---: | :---: |
| ST92195B1 | 32K ROM | 2K | No | $\begin{gathered} \text { PSDIP56/ } \\ \text { TQFP64 } \end{gathered}$ |
| ST92195B2 | 32K ROM | 6K | No |  |
| ST92195B3 | 32K ROM | 6K | Yes |  |
| ST92195B4 | 48K ROM | 6K | Yes |  |
| ST92195B5 | 48K ROM | 8K | Yes |  |
| ST92195B6 | 56K ROM | 8K | Yes |  |
| ST92195B7 | 64K ROM | 8K | Yes |  |
| ST92T195B7 | 64K OTP | 8K | Yes |  |
| ST92E195B7 | 64K EPROM | 8K | Yes | $\begin{aligned} & \text { CSDIP56 } \\ & \text { /CQFP64 } \end{aligned}$ |


| Symbol | Parameter | Value |  | Unit |
| :--- | :--- | :---: | :---: | :---: |
|  |  | Min. | Max. |  |
| $\mathrm{T}_{\mathrm{A}}$ | Operating Temperature | 0 | 70 | ${ }^{\circ} \mathrm{C}$ |
| $\mathrm{V}_{\mathrm{DD}}$ | Supply Voltage | 4.5 | 5.5 | V |
| $\mathrm{~V}_{\mathrm{DDA}}$ | Analog Supply Voltage (PLL) | 4.5 | 5.5 | V |
| $\mathrm{f}_{\mathrm{OSCE}}$ | External Oscillator Frequency | 3.3 | 8.7 | MHz |
| $\mathrm{f}_{\mathrm{OSCl}}$ | Internal Clock Frequency (INTCLK) |  | 24 | MHz |

## ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
| :--- | :--- | :--- | :---: |
| $\mathrm{V}_{\mathrm{DD}}$ | Supply Voltage | $\mathrm{V}_{\mathrm{SS}}-0.3$ to $\mathrm{V}_{\mathrm{SS}}+7.0$ | V |
| $\mathrm{~V}_{\mathrm{SSA}}$ | Analog Ground | $\mathrm{V}_{\mathrm{SS}}-0.3$ to $\mathrm{V}_{\mathrm{SS}}+0.3$ | V |
| $\mathrm{~V}_{\mathrm{DDA}}$ | Analog Supply Voltage | $\mathrm{V}_{\mathrm{DD}}-0.3$ to $\mathrm{V}_{\mathrm{DD}}+0.3$ | V |
| $\mathrm{~V}_{\mathrm{I}}$ | Input Voltage | $\mathrm{V}_{\mathrm{SS}}-0.3$ to $\mathrm{V}_{\mathrm{DD}}+0.3$ | V |
| $\mathrm{~V}_{\mathrm{AI}}$ | Analog Input Voltage (A/D Converter) | $\mathrm{V}_{\mathrm{SS}}-0.3$ to $\mathrm{V}_{\mathrm{DD}}+0.3$ <br> $\mathrm{~V}_{\mathrm{SSA}}-0.3$ to $\mathrm{V}_{\mathrm{DDA}}+0.3$ | V |
| $\mathrm{~V}_{\mathrm{O}}$ | Output Voltage | $\mathrm{V}_{\mathrm{SS}}-0.3$ to $\mathrm{V}_{\mathrm{DD}}+0.3$ | V |
| $\mathrm{~T}_{\mathrm{STG}}$ | Storage Temperature | -55 to +150 | ${ }^{\circ} \mathrm{C}$ |
| $\mathrm{I}_{\text {INJ }}$ | Pin Injected Current <br> Maximum Accumulated Pin <br> Injected Current In Device | -5 to +5 | mA |

Note: Stress above those listed as "Absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS
( $\mathrm{V}_{\mathrm{DD}}=5 \mathrm{~V}+/-10 \% ; \mathrm{T}_{\mathrm{A}}=0$ to $70^{\circ} \mathrm{C}$; unless otherwise specified)

| Symbol | Parameter | Test Conditions | Value |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | Min. | Max. |  |
| $\mathrm{V}_{\text {IHCK }}$ | Clock In high level | External clock | $0.7 \mathrm{~V}_{\mathrm{DD}}$ |  | V |
| $\mathrm{V}_{\text {ILCK }}$ | Clock in low level | External clock |  | $0.3 \mathrm{~V}_{\mathrm{DD}}$ | V |
| $\mathrm{V}_{\mathrm{IH}}$ | Input high level | TTL | 2.0 |  | V |
| $\mathrm{V}_{\text {IL }}$ | Input low level | TTL |  | 0.8 | V |
| $\mathrm{V}_{\mathrm{IH}}$ | Input high level | CMOS | $0.8 \mathrm{~V}_{\mathrm{DD}}$ |  | V |
| $\mathrm{V}_{\text {IL }}$ | Input low level | CMOS |  | $0.2 \mathrm{~V}_{\mathrm{DD}}$ | V |
| $\mathrm{V}_{\text {IHRS }}$ | Reset in high level |  | $0.7 \mathrm{~V}_{\mathrm{DD}}$ |  | V |
| $\mathrm{V}_{\text {ILRS }}$ | Reset in low level |  |  | $0.3 \mathrm{~V}_{\mathrm{DD}}$ | V |
| $\mathrm{V}_{\text {HYRS }}$ | Reset in hysteresis |  | 0.3 |  | V |
| $\mathrm{V}_{\text {IHY }}$ | P2.(1:0) input hysteresis |  | 0.9 |  | V |
| $\mathrm{V}_{\text {IHVH }}$ | HSYNC/VSYNC input high level |  | $0.7 \mathrm{~V}_{\mathrm{DD}}$ |  | V |
| $\mathrm{V}_{\text {ILVH }}$ | HSYNC/VSYNC input low level |  |  | $0.3 \mathrm{~V}_{\mathrm{DD}}$ | V |
| $\mathrm{V}_{\text {HYHV }}$ | HSYNC/VSYNC input hysteresis |  | 0.5 |  | V |
| $\mathrm{V}_{\mathrm{OH}}$ | Output high level | Push-pull Ild=-0.8mA | $\mathrm{V}_{\mathrm{DD}}-0.8$ |  | V |
| $\mathrm{V}_{\mathrm{OL}}$ | Output low level | Push-pull Id=+1.6mA |  | 0.4 | V |
| $I_{\text {wPU }}$ | Weak pull-up current | bidir. state $\begin{aligned} & \mathrm{V}_{\mathrm{OL}}=3 \mathrm{~V} \\ & \mathrm{~V}_{\mathrm{OL}}=7 \mathrm{~V} \end{aligned}$ | 50 | 350 | $\mu \mathrm{A}$ |
| ILKIO | I/O pin input leakage current | $0<\mathrm{V}_{\text {IN }}<\mathrm{V}_{\text {DD }}$ | -10 | +10 | $\mu \mathrm{A}$ |
| ILKRS | Reset pin input | $0<\mathrm{V}_{\text {IN }}<\mathrm{V}_{\text {DD }}$ | -10 | +10 | $\mu \mathrm{A}$ |
| ILKAD | A/D pin input leakage current | alternate funct. op. drain | -10 | +10 | $\mu \mathrm{A}$ |
| $\mathrm{I}_{\text {LKOS }}$ | OSCIN pin input leakage current | $0<\mathrm{V}_{\text {IN }}<\mathrm{V}_{\text {DD }}$ | -10 | +10 | $\mu \mathrm{A}$ |

## LF00AB/C SERIES <br> VERY LOW DROP <br> VOLTAGE REGULATORS WITH INHIBIT

n VERY LOW DROPOUT VOLTAGE (0.45V)
n VERY LOW QUIESCENT CURRENT (TYP. 50 mA IN OFF MODE, 500mA IN ON MODE)
n OUTPUT CURRENT UP TO 500 mA
n LOGIC-CONTROLLEDELECTRONIC SHUTDOWN
n OUTPUT VOLTAGES OF 1.25;1.5; 1.8;2.5;
2.7; 3; 3.3; 3.5; 4; 4.5; 4.7; 5; 5.2; 5.5; 6; 8; 8.5; 9;12V
n INTERNAL CURRENT AND THERMAL LIMIT
n ONLY 2.2mF FOR STABILITY
n AVAILABLE IN $\pm 1 \%$ (AB)OR $\pm 2 \%$ (C)
SELECTIONAT $25^{\circ} \mathrm{C}$
n SUPPLY VOLTAGE REJECTION: 80dB (TYP.)
n TEMPERATURE RANGE:-40 TO $125^{\circ} \mathrm{C}$

## DESCRIPTION

The LF00 series are very Low Drop regulators available in PENTAWATT, TO-220, TO-220FP, DPAK and PPAK package and in a wide range of output voltages.
The very Low Drop voltage ( 0.45 V ) and the very low quiescent current make them particularly suitable for Low Noise, Low Power applications and specially in battery powered systems.
In the 5 pins configuration (PENTAWATT and PPAK) a Shutdown Logic Control function is

available (pin 2, TTL compatible). This means that when the device is used as a local regulator, it is possible to put a part of the board in standby, decreasing the total power consumption. In the three terminal configuration the device has the same electrical performance, but is fixed in the ON state. It requires only a 2.2 mF capacitor for stability allowing space and costsaving.

## SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
| :---: | :--- | :---: | :---: |
| $\mathrm{V}_{\mathrm{i}}$ | DC InputVoltage | -0.5 to $40(*)$ | V |
| $\mathrm{I}_{0}$ | Output Current | Internally limited |  |
| $\mathrm{P}_{\text {tot }}$ | Power Dissipation | Internally limited |  |
| $\mathrm{T}_{\text {stg }}$ | Storage Temperature Range | -40 to 150 | ${ }^{\circ} \mathrm{C}$ |
| $\mathrm{T}_{\text {op }}$ | Operating J unction Temperature Range | -40 to 125 | ${ }^{\circ} \mathrm{C}$ |

(*) For $18<\mathrm{V}_{\text {IN }}<40$ the regulator is in shut-down

THERMAL DATA

| Symbol | Parameter | PENTAWATT | TO-220 | TO-220FP | DPAK/PPAK | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $R_{\text {thj-case }}$ | Thermal Resistance J unction-case | 3 | 3 | 5 | 8 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| $R_{\text {thj-amb }}$ | Thermal Resistance J unction-ambient | 50 | 50 | 60 | 100 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |

CONNECTION DIAGRAM (top view)


PENTAWATT

$\qquad$

ORDERING NUMBERS

| Type | PENTAWATT | TO-220 | TO-220FP | DPAK | PPAK | Output Voltage |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| LF12C (*) | LF12CV5V | LF12CV | LF 12CP | LF 12CDT | LF 12CPT | 1.25 V |
| LF12AB (*) | LF 12ABV5V | LFF12ABV | LF 12ABP | LF 12ABDT | LF 12ABPT | 1.25 V |
| LF15C (*) | LF15CV5V | LF15CV | LF 15CP | LF 15CDT | LF 15CPT | 1.5 V |
| LF15AB (*) | LF15ABV5V | LF15ABV | LF 15ABP | LF 15ABDT | LF 15ABPT | 1.5 V |
| LF18C | LF18C5V | LF18CV | LF 18CP | LF 18CDT | LF 18CPT | 1.8 V |
| LF18AB | LF18AB5V | LF18ABV | LF 18ABP | LF 18ABDT | LF 18ABPT | 1.8 V |
| LF25C | LF25CV5V | LF25CV | LF 25CP | LF 25CDT | LF25CPT | 2.5 V |
| LF25AB | LF25ABV5V | LF25ABV | LF25ABP | LF 25ABDT | LF 25ABPT | 2.5 V |
| LF27C | LF27CV5V | LF27CV | LF27CP | LF 27CDT | LF27CPT | 2.7 V |
| LF27AB | LF27ABV5V | LF27ABV | LF27ABP | LF 27ABDT | LF27ABPT | 2.7 V |
| LF30C | LF30CV5V | LF30CV | LF30CP | LF 30CDT | LF 30CPT | 3 V |
| LF30AB | LF30ABV5V | LF30ABV | LF 30ABP | LF 30ABDT | LF30ABPT | 3 V |
| LF33C | LF33CV5V | LF33CV | LF33CP | LF 33CDT | LF33CPT | 3.3 V |
| LF33AB | LF33ABV5V | LF33ABV | LF33ABP | LF 33ABDT | LF33ABPT | 3.3 V |
| LF35C | LF35CV5V | LF35CV | LF35CP | LF 35CDT | LF35CPT | 3.5 V |
| LF35AB | LF35ABV5V | LF35ABV | LF35ABP | LF 35ABDT | LF35ABPT | 3.5 V |
| LF 40C | LF40CV5V | LF40CV | LF 40CP | LF 40CDT | LF 40CPT | 4 V |
| LF40AB | LF40ABV5V | LF $40 A B V$ | LF 40ABP | LF 40ABDT | LF 40ABPT | 4 V |
| LF45C (*) | LF45CV5V | LF45CV | LF45CP | LF 45CDT | LF45CPT | 4.5 V |
| LF45AB (*) | LF45ABV5V | LF45ABV | LF45ABP | LF 45ABDT | LF 45ABPT | 4.5 V |
| LF47C | LF47CV5V | LF47CV | LF47CP | LF 47CDT | LF47CPT | 4.75 V |
| LF47AB | LF47ABV5V | LF 47ABV | LF 47ABP | LF 47ABDT | LF 47ABPT | 4.75 V |
| LF50C | LF50CV5V | LF50CV | LF50CP | LF 50CDT | LF50CPT | 5 V |
| LF50AB | LF50ABV5V | LF50ABV | LF50ABP | LF 50ABDT | LF50ABPT | 5 V |
| LF52C | LF52CV5V | LF52CV | LF52CP | LF 52CDT | LF52CPT | 5.2 V |
| LF52AB | LF52ABV5V | LF52ABV | LF52ABP | LF 52ABDT | LF52ABPT | 5.2 V |
| LF55C | LF55CV5V | LF55CV | LF55CP | LF 55CDT | LF55CPT | 5.5 V |
| LF55AB | LF55ABV5V | LF55ABV | LF55ABP | LF 55ABDT | LF55ABPT | 5.5 V |
| LF60C | LF60CV5V | LF60CV | LF60CP | LF 60CDT | LF60CPT | 6 V |
| LF60AB | LF60ABV5V | LF60ABV | LF60ABP | LF 60ABDT | LF60ABPT | 6 V |
| LF80C | LF80CV5V | LF80CV | LF80CP | LF 80CDT | LF80CPT | 8 V |
| LF80AB | LF80ABV5V | LF80ABV | LF80ABP | LF 80ABDT | LF80ABPT | 8 V |
| LF85C | LF85CV5V | LF85CV | LF 85CP | LF 85CDT | LF85CPT | 8.5 V |
| LF85AB | LF85ABV5V | LF85ABV | LF85ABP | LF 85ABDT | LF85ABPT | 8.5 V |
| LF90C | LF90CV5V | LF90CV | LF90CP | LF 90CDT | LF90CPT | 9 V |
| LF90AB | LF90ABV5V | LF90ABV | LF90ABP | LF90ABDT | LF90ABPT | 9 V |
| LF120C | LF120CV5V | LF 120CV | LF 120CP | LF 120CDT | LF 120CPT | 12 V |
| LF 120AB | LF 120ABV5V | LF 120ABV | LF 120ABP | LF 120ABDT | LF 120ABPT | 12 V |

TESTCIRCUITS


ELECTRICAL CHARACTERISTICS FOR LF12AB（refer to the test circuits， $\mathrm{T}_{\mathrm{j}}=25^{\circ} \mathrm{C}$ ，
$\mathrm{C}_{\mathrm{i}}=0.1 \mu \mathrm{~F}, \mathrm{C}_{0}=2.2 \mu \mathrm{~F}$ unless otherwise specified）

| Symbol | Parameter | Test Conditions | Min． | Typ． | Max． | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| V。 | Output Voltage | $\begin{aligned} & \mathrm{I}_{\mathrm{o}}=50 \mathrm{~mA}, \mathrm{~V}_{\mathrm{i}}=3.3 \mathrm{~V} \\ & \mathrm{I}_{\mathrm{o}}=50 \mathrm{~mA}, \mathrm{~V}_{\mathrm{i}}=3.3 \mathrm{~V}-25<\mathrm{T}_{\mathrm{a}}<85^{\circ} \mathrm{C} \end{aligned}$ | $\begin{aligned} & 1.238 \\ & 1.225 \end{aligned}$ | 1.25 | $\begin{aligned} & 1.263 \\ & 1.275 \end{aligned}$ | $\begin{aligned} & \hline \mathrm{V} \\ & \mathrm{~V} \end{aligned}$ |
| $\mathrm{V}_{\mathrm{i}}$ | Operating Input Voltage | $\mathrm{I}_{0}=500 \mathrm{~mA}$ | 2.5 |  | 16 | V |
| Iout | Output Current Limit |  |  | 1 |  | A |
| $\Delta \mathrm{V}$ 。 | Line Regulation | $\mathrm{V}_{\mathrm{i}}=2.5$ to $16 \mathrm{~V}, \mathrm{I}_{0}=5 \mathrm{~mA}$ |  | 2 | 10 | mV |
| $\Delta \mathrm{V}_{0}$ | Load Regulation | $\mathrm{V}_{\mathrm{i}}=2.8 \mathrm{~V} \quad \mathrm{I}_{0}=5$ to 500 mA |  | 2 | 10 | mV |
| $I_{d}$ | Quiescent Current | ON MODE $\begin{array}{ll} V_{i}=2.5 \text { to } 16 \mathrm{~V} & \mathrm{I}_{0}=0 \mathrm{~mA} \\ \mathrm{~V}_{\mathrm{i}}=2.6 \text { to } 16 \mathrm{~V} & \mathrm{I}_{0}=500 \mathrm{~mA} \\ \hline \end{array}$ |  | 0.5 | $\begin{gathered} 1 \\ 12 \end{gathered}$ | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~mA} \end{aligned}$ |
|  |  | OFF MODE $\mathrm{V}_{\mathrm{i}}=6 \mathrm{~V}$ |  | 50 | 100 | $\mu \mathrm{A}$ |
| SVR | Supply Voltage Rejection | $\begin{aligned} & I_{0}=5 \mathrm{~mA} \quad \mathrm{~V}_{\mathrm{i}}=3.5 \mathrm{~V} \pm 1 \mathrm{~V} \\ & \mathrm{f}=120 \mathrm{~Hz} \\ & \mathrm{f}=1 \mathrm{KHz} \\ & \mathrm{f}=10 \mathrm{KHz} \end{aligned}$ |  | $\begin{aligned} & 82 \\ & 77 \\ & 65 \end{aligned}$ |  | $\begin{aligned} & d B \\ & d B \\ & d B \end{aligned}$ |
| eN | Output Noise Voltage | $\mathrm{B}=10 \mathrm{~Hz}$ to 100 KHz |  | 50 |  | $\mu \mathrm{V}$ |
| $\mathrm{V}_{\mathrm{d}}$ | Dropout Voltage | $\mathrm{I}_{0}=200 \mathrm{~mA}$ |  | 1.25 |  | V |
| $\mathrm{V}_{\text {il }}$ | Control Input Logic Low | $-40<\mathrm{T}_{\mathrm{a}}<125^{\circ}$ |  |  |  |  |
| $\mathrm{V}_{\text {ih }}$ | Control Input Logic High | $-40<\mathrm{T}_{\mathrm{a}}<125^{\circ} \mathrm{C}$ | 2 |  |  | V |
| I | Control Input Current | $\mathrm{V}_{\mathrm{i}}=6 \mathrm{~V}, \quad \mathrm{~V}_{\mathrm{c}}=6 \mathrm{~V}$ |  | 10 |  | $\mu \mathrm{A}$ |
| $\mathrm{C}_{0}$ | Output Bypass Capacitance | ESR $=0.1$ to $10 \Omega \quad \mathrm{I}_{0}=0$ to 500 mA | 2 | 10 |  | $\mu \mathrm{F}$ |

ELECTRICAL CHARACTERISTICS FOR LF12C（refer to the test circuits， $\mathrm{T}_{\mathrm{j}}=25^{\circ} \mathrm{C}$ ，
$\mathrm{C}_{\mathrm{i}}=0.1 \mu \mathrm{~F}, \mathrm{C}_{0}=2.2 \mu \mathrm{~F}$ unless otherwise specified）

| Symbol | Parameter | Test Conditions | Min． | Typ． | Max． | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| V。 | Output Voltage | $\begin{aligned} & \mathrm{I}_{\mathrm{o}}=50 \mathrm{~mA}, \mathrm{~V}_{\mathrm{i}}=3.3 \mathrm{~V} \\ & \mathrm{I}_{\mathrm{O}}=50 \mathrm{~mA}, \mathrm{~V}_{\mathrm{i}}=3.3 \mathrm{~V}-25<\mathrm{T}_{\mathrm{a}}<85^{\circ} \mathrm{C} \end{aligned}$ | $\begin{gathered} 1.225 \\ 1.2 \end{gathered}$ | 1.25 | $\begin{gathered} 1.275 \\ 1.3 \end{gathered}$ | $\begin{aligned} & \hline \mathrm{V} \\ & \mathrm{~V} \end{aligned}$ |
| $V_{i}$ | Operating Input Voltage | $\mathrm{I}_{0}=500 \mathrm{~mA}$ | 2.5 |  | 16 | V |
| Iout | Output Current Limit |  |  | 1 |  | A |
| $\Delta \mathrm{V}$ 。 | Line Regulation | $\mathrm{V}_{\mathrm{i}}=2.5$ to $16 \mathrm{~V}, \mathrm{I}_{0}=5 \mathrm{~mA}$ |  | 2 | 10 | mV |
| $\Delta \mathrm{V}_{0}$ | Load Regulation | $\mathrm{V}_{\mathrm{i}}=2.8 \mathrm{~V} \quad \mathrm{I}_{0}=5$ to 500 mA |  | 2 | 10 | mV |
| $I_{\text {d }}$ | Quiescent Current | ON MODE $\begin{array}{ll} \mathrm{V}_{\mathrm{i}}=2.5 \text { to } 16 \mathrm{~V} & \mathrm{I}_{0}=0 \mathrm{~mA} \\ \mathrm{~V}_{\mathrm{i}}=2.6 \text { to } 16 \mathrm{~V} & \mathrm{I}_{0}=500 \mathrm{~mA} \\ \hline \end{array}$ |  | 0.5 | $\begin{gathered} 1 \\ 12 \\ \hline \end{gathered}$ | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~mA} \end{aligned}$ |
|  |  | OFF MODE $\mathrm{V}_{\mathrm{i}}=6 \mathrm{~V}$ |  | 50 | 100 | $\mu \mathrm{A}$ |
| SVR | Supply Voltage Rejection | $\begin{aligned} & I_{0}=5 \mathrm{~mA} \quad V_{i}=3.5 \mathrm{~V} \pm 1 \mathrm{~V} \\ & f=120 \mathrm{~Hz} \\ & \mathrm{f}=1 \mathrm{KHz} \\ & \mathrm{f}=10 \mathrm{KHz} \end{aligned}$ |  | $\begin{aligned} & 82 \\ & 77 \\ & 65 \end{aligned}$ |  | $\begin{aligned} & \mathrm{dB} \\ & \mathrm{~dB} \\ & \mathrm{~dB} \end{aligned}$ |
| eN | Output Noise Voltage | $\mathrm{B}=10 \mathrm{~Hz}$ to 100 KHz |  | 50 |  | $\mu \mathrm{V}$ |
| $\mathrm{V}_{\mathrm{d}}$ | Dropout Voltage | $\mathrm{I}_{0}=200 \mathrm{~mA}$ |  | 1.25 |  | V |
| $\mathrm{V}_{\text {il }}$ | Control Input Logic Low | $-40<\mathrm{T}_{\mathrm{a}}<125^{\circ}$ |  |  |  |  |
| $\mathrm{V}_{\text {ih }}$ | Control Input Logic High | $-40<\mathrm{T}_{\mathrm{a}}<125^{\circ} \mathrm{C}$ | 2 |  |  | V |
| $\mathrm{I}_{\mathrm{i}}$ | Control Input Current | $\mathrm{V}_{\mathrm{i}}=6 \mathrm{~V}, \mathrm{~V}_{\mathrm{c}}=6 \mathrm{~V}$ |  | 10 |  | $\mu \mathrm{A}$ |
| Co | Output Bypass Capacitance | ESR $=0.1$ to $10 \Omega \mathrm{I}_{0}=0$ to 500 mA | 2 | 10 |  | $\mu \mathrm{F}$ |

## 13- BAS 70... / BAS 170W

## Silicon Schottky Diode

General-purpose diode for high-speed switching
Circuit protection
Voltage clamping
High-level detecting and mixing



BAS70-06
BAS70-06W

BAS70



BAS70-07 BAS70-07W

BAS70-04 BAS70-04T BAS70-04W


BAS70-04S
BAS70-05
BAS70-05W


| Type | Package | Configuration | $\mathrm{L}_{\mathrm{s}}(\mathrm{nH})$ | Marking |
| :--- | :--- | :--- | :---: | :--- |
| BAS170W | SOD323 | single | 1.8 | 7 |
| BAS70 | SOT23 | single | 1.8 | 73 s |
| BAS70-02L* | TSLP-2-1 | single, leadless | 0.4 | F |
| BAS70-02W | SCD80 | single | 0.6 | 73 |
| BAS70-04 | SOT23 | series | 1.8 | 74 s |
| BAS70-04S | SOT363 | dual series | 1.6 | 74 s |
| BAS70-04T | SC75 | series | 1.6 | 74 s |
| BAS70-04W | SOT323 | series | 1.4 | 74 s |
| BAS70-05 | SOT23 | common cathode | 1.8 | 75 s |
| BAS70-05W | SOT323 | common cathode | 1.4 | 75 s |
| BAS70-06 | SOT23 | common anode | 1.8 | 76 s |
| BAS70-06W | SOT323 | common anode | 1.4 | 76 s |
| BAS70-07 | SOT143 | parallel pair | 2 | 77 s |
| BAS70-07W | SOT343 | parallel pair | 1.8 | 77 s |

[^0]Maximum Ratings at $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$, unless otherwise specified

| Parameter | Symbol | Value | Unit |
| :---: | :---: | :---: | :---: |
| Diode reverse voltage | $\mathrm{V}_{\mathrm{R}}$ | 70 | V |
| Forward current | $\mathrm{I}_{\mathrm{F}}$ | 70 | mA |
| Surge forward current <br> t 10ms | $\mathrm{I}_{\text {FSM }}$ | 100 |  |
| Total power dissipation <br> BAS70, BAS70-07, Ts $72{ }^{\circ} \mathrm{C}$ <br> BAS70-02L, $T_{S} 117^{\circ} \mathrm{C}$ <br> BAS70-02W, $\mathrm{T}_{\mathrm{S}} 107^{\circ} \mathrm{C}$ <br> BAS70-04, BAS70-06, $T_{S} \quad 48^{\circ} \mathrm{C}$ <br> BAS70-04S/W/-06W, BAS170W, TS $97{ }^{\circ} \mathrm{C}$ <br> BAS70-04T, $\mathrm{T}_{S} \quad 91^{\circ} \mathrm{C}$ <br> BAS70-05, $T_{S} \quad 22^{\circ} \mathrm{C}$ <br> BAS70-05W, Ts $90^{\circ} \mathrm{C}$ <br> BAS70-07W, $T_{S} \quad 114{ }^{\circ} \mathrm{C}$ | $\mathrm{P}_{\text {tot }}$ | $\begin{aligned} & 250 \\ & 250 \\ & 250 \\ & 250 \\ & 250 \\ & 250 \\ & 250 \\ & 250 \\ & 250 \end{aligned}$ | mW |
| Junction temperature | T. | 150 | ${ }^{\circ} \mathrm{C}$ |
| Operating temperature range | $\mathrm{T}_{\text {op }}$ | -55 ... 125 |  |
| Storage temperature | $\mathrm{T}_{\text {stg }}$ | -55 ... 150 |  |

Thermal Resistance

| Parameter | Symbol | Value | Unit |
| :--- | :--- | :--- | :--- |
| Junction - soldering point ${ }^{1)}$ | $\mathrm{R}_{\text {thJS }}$ |  | K/W |
| BAS70, BAS70-07 |  | 310 |  |
| BAS70-02L |  | 130 |  |
| BAS70-02W |  | 170 |  |
| BAS70-04, BAS70-06 | 410 |  |  |
| BAS70-04S/W, BAS70-06W |  | 210 |  |
| BAS70-04T |  | 235 |  |
| BAS70-05 |  | 510 |  |
| BAS70-05W |  | 240 |  |
| BAS70-07W |  | 145 |  |
| BAS170W |  | 190 |  |

${ }^{1}$ For calculation of $\mathrm{R}_{\mathrm{thJA}}$ please refer to Application Note Thermal Resistance

Electrical Characteristics at $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$, unless otherwise specified

| Parameter | Symbol | Values |  |  | Unit |
| :--- | :---: | :---: | :---: | :---: | :---: |
|  |  | min. | typ. | max. |  |
| DC Characteristics | $\mathrm{V}_{(\mathrm{BR})}$ | 70 | - | - | V |
| Breakdown voltage |  |  |  |  |  |
| $\mathrm{I}_{(\mathrm{BR})}=10 \mu \mathrm{~A}$ | $\mathrm{I}_{\mathrm{R}}$ | - | - | 0.1 | $\mu \mathrm{~A}$ |
| Reverse current |  |  |  |  |  |
| $\mathrm{V}_{\mathrm{R}}=50 \mathrm{~V}$ | $\mathrm{~V}_{\mathrm{F}}$ |  |  |  | mV |
| Forward voltage |  | 300 | 375 | 410 |  |
| $\mathrm{I}_{\mathrm{F}}=1 \mathrm{~mA}$ |  | 600 | 705 | 750 |  |
| $\mathrm{I}_{\mathrm{F}}=10 \mathrm{~mA}$ |  | 750 | 880 | 1000 |  |
| $\mathrm{I}_{\mathrm{F}}=15 \mathrm{~mA}$ | $\mathrm{~V}_{\mathrm{F}}$ | - | - | 20 |  |
| Forward voltage matching1) |  |  |  |  |  |

AC Characteristics

| Diode capacitance | $\mathrm{C}_{\mathrm{T}}$ | - | 1.5 | 2 | pF |
| :--- | :--- | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\mathrm{R}}=0, \mathrm{f}=1 \mathrm{MHz}$ |  |  |  |  |  |$\quad \mathrm{rf}$

[^1]
## DPS9450

## 1. Introduction

The DPS 9450A is a single-chip digital display processor and scaler specially designed for TV applications with LCD or PDP displays. The DPS 9450A is a new family component of the Micronas MEGAVISION ${ }^{\circledR}$ IC set manufactured in a deep submicron CMOS technology. The device comprises a $\mathrm{YC}_{\mathrm{r}} \mathrm{C}_{b} / R G B$ interface with fast-blank capability (SCART) including A/D converter, ITU-601/656 digital input, scaling units including panorama mode, embedded SRAM for up- and downscaling, deinterlacer, picture improvements like luminance transition improvements, chrominance transition improvements, dynamic contrast improvement, black level expander, peaking, digital OSD input, as well as a generator for LCD panel control signals.

### 1.1. Features

## Video Inputs

- Digital input for 50/60 interlace or 50/60 progressive signals in ITU-656 (8-bit) or ITU-601 (16-bit)
- 38 -bit $\mathrm{YC}_{\mathrm{r}} \mathrm{C}_{\mathrm{b}} / R G B$ input (depends on I/O config.)
- Two analog RGB/YC $C_{b}$ inputs (for teletext, graphic, 480p (EIA-770.2, 1080i/720p reduced resolution):
- Four built-in ADCs (8-bit) for RGB and Fastblank with max. 81 MHz sampling rate
- Separate HS and VS (2 ) inputs (external sync separation required)


## Sync Processing

- H and V-sync outputs to synchronize the external analog RGB/YUV source in soft mix mode (see display modes)
- H- and V-sync outputs to synchronize an external OSD source


## High-Performance Video Processing

- Full 4:4:4 processing
- RGB-to- $\mathrm{YC}_{\mathrm{r}} \mathrm{C}_{\mathrm{b}}$ conversion
- Brightness, Contrast, Saturation for analog component input
- Dynamic contrast improvement (DCI)
- Black level expander (BLE)
- Luma and chroma transition improvement
- Dynamic peaking
- Brightness, Contrast, Saturation, Tint
- Programmable $\mathrm{YC}_{r} \mathrm{C}_{b}$-to-RGB matrix
- Programmable characteristic on R,G,B for gamma correction, Blue stretch, White drive
- Dithering for 8- to 6-bit digital outputs


## Display Modes

- Digital mode: video from the digital input only
- Analog mode: video/graphic/teletext from the ana$\log R G B / Y C_{r} C_{b}$ input only
- Soft mix mode: soft mixing of the video and component input (component source works as slave and is synchronized with the digital video input)
In each display mode, additional OSD can be mixed.


## Display Format Processing

- Prescaling of the input signal:

Horizontal scaling factor: 1.0 ... 1/64

- Upscaling of the output signal:

Horizontal scaling factor: 1... 4
(5-zone panorama generator)

- Vertical scaling factor: 0.5 ... 4
- Deinterlacing with line-doubling or upscaling


## OSD

- Digital RGB input (6- or 12-bit / pixel)
- 64-entry CLUT with 12-bit colors
- Picture frame and test pattern generation
- Half-contrast switch (0, 25\%, 50\%, 100\%)


## Display Resolutions

- 640480 (VGA; 4:3 panel)
- 852480 (W-VGA; 16:9 panel)
- 800600 (SVGA)
- 1024768 (XGA)
- 1365768 (W-XGA)


## Output Interface

- 18 or 24 -bit RGB output
- 2 18- or 24 -bit RGB output: dual pixel mode (depending on I/O configuration)
- programmable panel control signals


## Miscellaneous

- up to 2 PWM outputs
- up to 8 general purpose I/Os (depending on I/O configuration)
- $\mathrm{I}^{2} \mathrm{C}$ interface ( 400 kHz )
- $1.8 \mathrm{~V} \pm 5 \%$ and $3.3 \mathrm{~V} \pm 5 \%$ supply voltages
- PMQFP144 package

|  | Input: <br> Digital <br> ITU656 | Input: <br> Digital <br> RGB | Input: <br> Analog <br> RGB | Input: <br> Digital <br> OSD | Output: <br> single bus <br> dig. RGB | Output: <br> dual bus <br> dig. RGB |
| :--- | :--- | :--- | :--- | :--- | :--- | :--- |
| Default (VGAINOUT) | $8 / 16$-bit |  | RGB1/2 | $6 / 12$-bit | $18 / 24$-bit |  |
| Config1 (XGAINOUT) |  | 24 -bit | RGB1/2 |  |  | 218 -bit |
| Config2 (XGAIN) | 8 -bit | 24 -bit | RGB1/2 | 6 -bit | $18 / 24$-bit |  |
| Config3 (XGAIN/TU) | $8 / 16$-bit |  | RGB1/2 | 6 -bit |  | 218 -bit |
| Config4 (XGAOUT) | 8 -bit |  | RGB1/2 | 6 -bit | $18 / 24$-bit | 224 -bit |

## Electrical Characteristics

## Absolute Maximum Ratings

All voltages listed are referenced to ground ( $0 \mathrm{~V}, \mathrm{~V}_{\mathrm{SS}}$ ) except where noted.

| Symbol | Parameter | Limit Values |  | Unit | Remark |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Max |  |  |
| $\mathrm{T}_{\text {A }}$ | Ambient Operating Temperature | 0 | 65 | ${ }^{\circ} \mathrm{C}$ |  |
| $\mathrm{T}_{\text {S }}$ | Storage Temperature | 40 | 125 | ${ }^{\circ} \mathrm{C}$ |  |
| $\mathrm{V}_{\mathrm{DD} 1}$ | Supply Voltages 1 | 0.3 | 2 | V | VDD_CORE, VDDAFBL, VDDARGB, VDDPLL |
| $\mathrm{V}_{\mathrm{DD} 2}$ | Supply Voltages2 | 0.3 | 3.6 | V | VDD_PAD, VDD33FBL, VDD33RGB |
| $V_{1}$ | Input Voltage | 0.3 | $\mathrm{V}_{\mathrm{DD} 2}+0.3$ | V | not valid for $\mathrm{V}_{\mathrm{DD} 1}$ supply pins |
| $\mathrm{V}_{0}$ | Output Voltage | 0.3 | $\mathrm{V}_{\mathrm{DD2} 2}+0.3$ | V | not valid for $\mathrm{V}_{\mathrm{DD} 1}$ supply pins |

Stresses beyond those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only. Functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions/Characteristics" of this specification is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

# 15- DS90C385/DS90C365 <br> +3.3V Programmable LVDS Transmitter 24-Bit Flat Panel Display (FPD) Link-85MHz, +3.3V Programmable LVDS Transmitter 18-Bit Flat Panel Display (FPD) Link-85MHz. 

## General Description

The DS90C385 transmitter converts 28 bits of LVCMOS/ LVTTL data into four LVDS (Low Voltage Differential Signaling) data streams. A phase-locked transmit clock is transmitted in parallel with the data streams over a fifth LVDS link. Every cycle of the transmit clock 28 bits of input data are sampled and transmitted. At a transmit clock frequency of 85 $\mathrm{MHz}, 24$ bits of RGB data and 3 bits of LCD timing and control data (FPLINE, FPFRAME, DRDY) are transmitted at a rate of 595 Mbps per LVDS data channel. Using a 85 MHz clock, the data throughput is 297.5 Mbytes $/ \mathrm{sec}$. Also available is the DS90C365 that converts 21 bits of LVCMOS/ LVTTL data into three LVDS (Low Voltage Differential Signaling) data streams. Both transmitters can be programmed for Rising edge strobe or Falling edge strobe through a dedicated pin. A Rising edge or Falling edge strobe transmitter will interoperate with a Falling edge strobe Receiver (DS90CF386/DS90CF366) without any translation logic.
The DS90C385 is also offered in a 64 ball, 0.8 mm fine pitch ball grid array (FBGA) package which provides a 44 \% reduction in PCB footprint compared to the TSSOP package.

Block Diagrams


10086801
Order Number DS90C385MTD or DS90C385SLC See NS Package Number MTD56 or SLC64A

This chipset is an ideal means to solve EMI and cable size problems associated with wide, high-speed TTL interfaces.

## Features

n 20 to 85 MHz shift clock support
n Best-in-Class Set \& Hold Times on TxINPUTs
n Tx power consumption <130 mW (typ) @85MHz Grayscale
n Tx Power-down mode $<200 \mu \mathrm{~W}$ (max)
n Supports VGA, SVGA, XGA and Dual Pixel SXGA.
n Narrow bus reduces cable size and cost
n Up to 2.38 Gbps throughput
n Up to 297.5 Megabytes/sec bandwidth
n 345 mV (typ) swing LVDS devices for low EMI
n PLL requires no external components
n Compatible with TIA/EIA-644 LVDS standard
n Low profile 56 -lead or 48-lead TSSOP package
n DS90C385 also available in a 64 ball, 0.8 mm fine pitch ball grid array (FBGA) package

## Block Diagrams



Order Number DS90C365MTD
See NS Package Number MTD48

[^2]```
Absolute Maximum Ratings (Note 1)
If Military/Aerospace specified devices are required,
please contact the National Semiconductor Sales Office/
Distributors for availability and specifications.
```



| DS90C385SLC | 2.0 W |
| :---: | :---: |
| Package Derating: |  |
| DS90C385MTD | $12.5 \mathrm{~mW} /{ }^{\circ} \mathrm{C}$ above $+25^{\circ} \mathrm{C}$ |
| Package Derating: |  |
| DS90C365MTD | $16 \mathrm{~mW} /{ }^{\circ} \mathrm{C}$ above $+25^{\circ} \mathrm{C}$ |
| DS90C385SLC | $10.2 \mathrm{~mW} / \mathrm{C}$ above $+25^{\circ} \mathrm{C}$ |
| ESD Rating |  |
| (HBM, 1.5k $\Omega$, 100pF) | $>7 \mathrm{kV}$ |
| (EIAJ, 0 ת, 200 pF ) | > 500 V |
| Latch Up Tolerance @ $25^{\circ} \mathrm{C}$ | $> \pm 300 \mathrm{~mA}$ |

## Recommended Operating

Conditions

|  |  |  | Min Nom Max Units |  |  |  |
| :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- |
|  |  |  | 3.0 | 3.3 | 3.6 | V |
| Supply Voltage ( V | cc $)$ |  |  |  |  |  |

## Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified.

| Symbol | Parameter |  | Conditions |  | Min | Typ | Max | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| LVCMOS/LVTTL DC SPECIFICATIONS |  |  |  |  |  |  |  |  |
| $\mathrm{V}_{\text {IH }}$ | High Level Input Voltage |  |  |  | 2.0 |  | $1 / \mathrm{cc}$ | V |
| $\mathrm{V}_{\text {IL }}$ | Low Level Input Voltage |  |  |  | GND |  | 0.8 | V |
| $\mathrm{V}_{\mathrm{CL}}$ | Input Clamp Voltage |  | $\mathrm{CL}=18 \mathrm{~mA}$ |  |  | 0.79 | 1.5 | V |
| $\mathrm{I}_{\text {IN }}$ | Input Current | $\mathrm{V}_{\text {IN }}=0.4 \mathrm{~V}, 2.5 \mathrm{~V}$ or $\mathrm{V}_{\text {cc }}$ |  |  |  | +1.8 | +10 | $\mu \mathrm{A}$ |
|  |  |  | $\mathrm{V}_{\text {IN }}=$ GND |  | 10 | 0 |  | $\mu \mathrm{A}$ |
| LVDS DC SPECIFICATIONS |  |  |  |  |  |  |  |  |
| $\mathrm{V}_{\text {OD }}$ | Differential Output Voltage | R | $\llcorner=100 \Omega$ |  | 250 | 345 | 450 | mV |
| $\Delta \mathrm{V}_{\text {OD }}$ | Change in V od between complimentary output states |  |  |  |  |  | 35 | mV |
| $\mathrm{V}_{\text {os }}$ | Offset Voltage (Note 4) |  |  |  | 1.125 | 1.25 | 1.375 | V |
| $\Delta \mathrm{V}_{\text {os }}$ | Change in V os between complimentary output states |  |  |  |  |  | 35 | mV |
| $\mathrm{I}_{0}$ | Output Short Circuit Current | V | Out $=0 \mathrm{~V}, \mathrm{R}_{\mathrm{L}}=100 \Omega$ |  |  | 3.5 | 5 | mA |
| $\mathrm{I}_{0 z}$ | Output TRI-STATE © Current |  | Power Down $=0 \mathrm{~V}$,$\mathrm{V}_{\text {OUT }}=0 \mathrm{~V} \text { or } \mathrm{V}_{\mathrm{cc}}$ |  |  | $\pm 1$ | $\pm 10$ | $\mu \mathrm{A}$ |
| TRANSMITTER SUPPLY CURRENT |  |  |  |  |  |  |  |  |
| ICCTW | Transmitter Supply Current <br> Worst Case <br> DS90C385 |  | $\begin{aligned} & \mathrm{R}_{\mathrm{L}}=100 \Omega \text {, } \\ & \mathrm{C}_{\mathrm{L}}=5 \mathrm{pF}, \\ & \text { Worst Case Pattern } \\ & \text { (Figures 1, } 4 \text { ) } \end{aligned}$ | $\mathrm{f}=32.5 \mathrm{MHz}$ |  | 31 | 45 | mA |
|  |  |  |  | $\mathrm{f}=40 \mathrm{MHz}$ |  | 32 | 50 | mA |
|  |  |  |  | $\mathrm{f}=65 \mathrm{MHz}$ |  | 37 | 55 | mA |
|  |  |  |  | $\mathrm{f}=85 \mathrm{MHz}$ |  | 42 | 60 | mA |
| ICCTG | $\begin{aligned} & \text { Transmitter Supply Current } \\ & 16 \text { Grayscale } \\ & \text { DS90C385 } \end{aligned}$ |  | $\begin{aligned} & \hline \mathrm{R}_{\mathrm{L}}=100 \Omega, \\ & \mathrm{C}_{\mathrm{L}}=5 \mathrm{pF}, \\ & 16 \text { Grayscale Pattern } \\ & \text { (Figures 2, 4 ) } \end{aligned}$ | $\mathrm{f}=32.5 \mathrm{MHz}$ |  | 29 | 38 | mA |
|  |  |  |  | $\mathrm{f}=40 \mathrm{MHz}$ |  | 30 | 40 | mA |
|  |  |  |  | $\mathrm{f}=65 \mathrm{MHz}$ |  | 35 | 45 | mA |
|  |  |  |  | $\mathrm{f}=85 \mathrm{MHz}$ |  | 39 | 50 | mA |

4

## Electrical Characteristics

(Continued)
Over recommended operating supply and temperature ranges unless otherwise specified.

| Symbol | Parameter | Conditions |  | Typ | Max | Units |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| TRANSMITTER SUPPLY CURRENT |  |  |  |  |  |  |  |
| ICCTW | Transmitter Supply Current <br> Worst Case <br> DS90C365 | $\begin{array}{\|l} \hline \mathrm{R}_{\mathrm{L}}=100 \Omega, \\ C_{\mathrm{L}}=5 \mathrm{pF}, \\ \text { Worst Case Pattern } \\ \text { (Figures 1, 4 ) } \end{array}$ | $\mathrm{f}=32.5 \mathrm{MHz}$ |  | 28 | 42 | mA |
|  |  |  | $\mathrm{f}=40 \mathrm{MHz}$ |  | 29 | 47 | mA |
|  |  |  | $\mathrm{f}=65 \mathrm{MHz}$ |  | 34 | 52 | mA |
|  |  |  | $\mathrm{f}=85 \mathrm{MHz}$ |  | 39 | 57 | mA |
| ICCTG | $\begin{aligned} & \text { Transmitter Supply Current } \\ & 16 \text { Grayscale } \\ & \text { DS90C365 } \end{aligned}$ | $\begin{aligned} & \hline \mathrm{R}_{\mathrm{L}}=100 \Omega, \\ & \mathrm{C}_{\mathrm{L}}=5 \mathrm{pF}, \\ & 16 \text { Grayscale Pattern } \\ & \text { (Figures 3, 4 ) } \end{aligned}$ | $\mathrm{f}=32.5 \mathrm{MHz}$ |  | 26 | 35 | mA |
|  |  |  | $\mathrm{f}=40 \mathrm{MHz}$ |  | 27 | 37 | mA |
|  |  |  | $\mathrm{f}=65 \mathrm{MHz}$ |  | 32 | 42 | mA |
|  |  |  | $\mathrm{f}=85 \mathrm{MHz}$ |  | 36 | 47 | mA |
| ICCTZ | Transmitter Supply Current Power Down | Power Down = Low <br> Driver Outputs in TRI-STATE under <br> Power Down Mode |  |  | 10 | 55 | $\mu \mathrm{A}$ |

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The tables of "Electrical Characteristics" specify conditions for device operation.
Note 2: Typical values are given for $\mathrm{V} \quad \mathrm{CC}=3.3 \mathrm{~V}$ and $\mathrm{T}_{\mathrm{A}}=+25 \mathrm{C}$.
Note 3: Current into device pins is defined as positive. Current out of device pins is defined as negative. Voltages are referenced to ground unless otherwise specified (except $V$ OD and $\Delta \mathrm{V}_{O D}$ ).
Note 4: $V_{0 S}$ previously referred as $V$ CM .

## SERIAL 16K (2K x 8) EEPROM

- 1 MILLION ERASE/WRITE CYCLES, with 40 YEARS DATA RETENTION
- SINGLE SUPPLY VOLTAGE:
- 4.5V to 5.5 V for ST24×16 versions
- 2.5V to 5.5 V for ST25x16 versions
- HARDWARE WRITE CONTROL VERSIONS: ST24W16 and ST25W16
- TWO WIRE SERIAL INTERFACE, FULLY I ${ }^{2} \mathrm{C}$ BUS COMPATIBLE
- BYTE and MULTIBYTE WRITE (up to 8 BYTES) for the ST24C16
- PAGE WRITE (up to 16 BYTES)
- BYTE, RANDOM and SEQUENTIAL READ MODES
- SELF TIMED PROGRAMING CYCLE
- AUTOMATIC ADDRESS INCREMENTING
- ENHANCED ESD/LATCH UP PERFORMANCES


## DESCRIPTION

This specification covers a range of 16 K bits $\mathrm{I}^{2} \mathrm{C}$ bus EEPROM products, the ST24/25C16 and the ST24/25W16. In the text, products are referred to as ST24/25x16 where "x" is: "C" for Standard version and "W" for hardware Write Control version.
The ST24/25×16 are 16K bit electrically erasable programmable memories (EEPROM), organized as 8 blocks of $256 \times 8$ bits. These are manufactured in SGS-THOMSON's Hi-Endurance Advanced CMOS technology which guarantees an endur-

## Signal Names

| PRE | Write Protect Enable |
| :--- | :--- |
| PB0, PB1 | Protect Block Select |
| SDA | Serial Data Address Input/Output |
| SCL | Serial Clock |
| MODE | Multybyte/Page Write Mode <br> (C version) |
| $\overline{\text { WC }}$ | Write Control (W version) |
| VCC $^{\text {WSS }}$ | Supply Voltage |
| VSS | Ground |



Figure 1. Logic Diagram


Note: $\overline{\mathrm{WC}}$ signal is only available for ST24/25W16 products.

Input Parameters ${ }^{(1)}\left(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}, \mathrm{f}=100 \mathrm{kHz}\right)$

| Symbol | Parameter | Test Condition | Min | Max | Unit |
| :---: | :--- | :--- | :---: | :---: | :---: |
| $\mathrm{C}_{\mathrm{IN}}$ | Input Capacitance (SDA) |  |  | 8 | pF |
| $\mathrm{C}_{\mathrm{IN}}$ | Input Capacitance (other pins) |  |  | 6 | pF |
| $Z_{W C L}$ | $\overline{W C}$ Input Impedance (ST24/25W16) | $\mathrm{V}_{\mathrm{IN}} \leq 0.3 \mathrm{~V}_{\mathrm{CC}}$ | 5 | 20 | $\mathrm{k} \Omega$ |
| $Z_{\mathrm{WCH}}$ | $\overline{W C}$ Input Impedance (ST24/25W16) | $\mathrm{V}_{\mathrm{IN}} \geq 0.7 \mathrm{~V}_{\mathrm{CC}}$ | 500 |  | $\mathrm{k} \Omega$ |
| $\mathrm{t}_{\mathrm{WP}}$ | Low-pass filter input time constant <br> (SDA and SCL) |  |  | 100 | ns |

Note: 1. Sampled only, not 100\% tested.

AC Characteristics
( $\mathrm{T}_{\mathrm{A}}=0$ to $70^{\circ} \mathrm{C}$ or -40 to $85^{\circ} \mathrm{C}$; $\mathrm{V}_{\mathrm{CC}}=4.5 \mathrm{~V}$ to 5.5 V or 2.5 V to 5.5 V )

| Symbol | Alt | Parameter | Min | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{t}_{\mathbf{C H} 1 \mathrm{CH} 2}$ | $t_{R}$ | Clock Rise Time |  | 1 | $\mu \mathrm{S}$ |
| tCL1CL2 | $t_{\text {F }}$ | Clock Fall Time |  | 300 | ns |
| tDH1DH2 | tR | Input Rise Time |  | 1 | $\mu \mathrm{s}$ |
| tDL1DL1 | $t_{\text {F }}$ | Input Fall Time |  | 300 | ns |
| $\mathrm{tchDX}^{(1)}$ | tsu:STA | Clock High to Input Transition | 4.7 |  | $\mu \mathrm{S}$ |
| $\mathrm{t}_{\text {CHCL }}$ | $t_{\text {tigh }}$ | Clock Pulse Width High | 4 |  | $\mu \mathrm{s}$ |
| $t_{\text {DLCL }}$ | $t_{\text {HD: STA }}$ | Input Low to Clock Low (START) | 4 |  | $\mu \mathrm{s}$ |
| tcldx | thd:DAT | Clock Low to Input Transition | 0 |  | $\mu \mathrm{s}$ |
| tclch | tıow | Clock Pulse Width Low | 4.7 |  | $\mu \mathrm{s}$ |
| toxcx | tsu:DAT | Input Transition to Clock Transition | 250 |  | ns |
| tchDH | tsu:Sto | Clock High to Input High (STOP) | 4.7 |  | $\mu \mathrm{s}$ |
| tDHDL | $t_{\text {BUF }}$ | Input High to Input Low (Bus Free) | 4.7 |  | $\mu \mathrm{s}$ |
| $\mathrm{tcLQV}^{(2)}$ | $t_{\text {AA }}$ | Clock Low to Next Data Out Valid | 0.3 | 3.5 | $\mu \mathrm{s}$ |
| $t_{\text {clQx }}$ | $t_{\text {DH }}$ | Data Out Hold Time | 300 |  | ns |
| $\mathrm{f}_{\mathrm{C}}$ | $\mathrm{f}_{\text {SCL }}$ | Clock Frequency |  | 100 | kHz |
| tw ${ }^{(3)}$ | twr | Write Time |  | 10 | ms |

Notes: 1. For a reSTART condition, or following a write cycle.
2. The minimum value delays the falling/rising edge of SDA away from $S C L=1$ in order to avoid unwanted START and/or STOP conditions.
3. In the Multibyte Write mode only, if accessed bytes are on two consecutive 8 bytes rows ( 5 address MSB are not constant) the maximum programming time is doubled to 20 ms .

## DC Characteristics

( $\mathrm{T}_{\mathrm{A}}=0$ to $70^{\circ} \mathrm{C}$ or -40 to $85^{\circ} \mathrm{C}$; $\mathrm{V} \mathrm{CC}=4.5 \mathrm{~V}$ to 5.5 V or 2.5 V to 5.5 V )

| Symbol | Parameter | Test Condition | Min | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| l L | Input Leakage Current | $\mathrm{O} \leq \mathrm{V}_{\text {IN }} \leq \mathrm{V}_{\text {CC }}$ |  | $\pm 2$ | $\mu \mathrm{A}$ |
| ILO | Output Leakage Current | $\begin{gathered} 0 \mathrm{~V} \leq \mathrm{V}_{\text {OUT }} \leq \mathrm{V}_{\text {CC }} \\ \text { SDA in Hi-Z } \end{gathered}$ |  | $\pm 2$ | $\mu \mathrm{A}$ |
| Icc | Supply Current (ST24 series) | $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{f}_{\mathrm{C}}=100 \mathrm{kHz}$ <br> (Rise/Fall time < 10ns) |  | 2 | mA |
|  | Supply Current (ST25 series) | $\mathrm{V}_{\mathrm{CC}}=2.5 \mathrm{~V}, \mathrm{f}_{\mathrm{C}}=100 \mathrm{kHz}$ |  | 1 | mA |
| Iccı | Supply Current (Standby) (ST24 series) | $\begin{gathered} V_{\mathrm{IN}}=V_{\mathrm{SS}} \text { or } \mathrm{V}_{\mathrm{CC}}, \\ V_{\mathrm{CC}}=5 \mathrm{~V} \end{gathered}$ |  | 100 | A |
|  |  | $\begin{gathered} V_{I N}=V_{S S} \text { or } V_{C C}, \\ V_{C C}=5 V, f_{C}=100 \mathrm{kHz} \end{gathered}$ |  | 300 | A |
| Icc2 | Supply Current (Standby) (ST25 series) | $\begin{gathered} \mathrm{V}_{\mathrm{IN}}=\mathrm{V}_{\mathrm{SS}} \text { or } \mathrm{V}_{\mathrm{CC}}, \\ \mathrm{~V}_{\mathrm{CC}}=2.5 \mathrm{~V} \end{gathered}$ |  | 5 | $\mu \mathrm{A}$ |
|  |  | $\mathrm{V}_{\text {IN }}=\mathrm{V}_{\text {SS }}$ or $\mathrm{V}_{\mathrm{CC}}$, $\mathrm{V}_{\mathrm{CC}}=2.5 \mathrm{~V}, \mathrm{f}_{\mathrm{C}}=100 \mathrm{kHz}$ |  | 50 | $\mu \mathrm{A}$ |
| VIL | Input Low Voltage (SCL, SDA) |  | -0.3 | 0.3 Vcc | V |
| $\mathrm{V}_{\mathrm{IH}}$ | Input High Voltage (SCL, SDA) |  | 0.7 VCC | $\mathrm{V}_{\mathrm{CC}}+1$ | V |
| VIL | Input Low Voltage <br> (PBO - PB1, PRE, MODE, $\overline{\mathrm{WC}}$ ) |  | -0.3 | 0.5 | V |
| $\mathrm{V}_{\mathrm{IH}}$ | Input High Voltage <br> (PB0 - PB1, PRE, MODE, $\overline{\mathrm{WC}}$ ) |  | $\mathrm{V}_{\mathrm{cc}}-0.5$ | $\mathrm{V}_{\mathrm{cc}}+1$ | V |
| Vol | Output Low Voltage (ST24 series) | $\mathrm{loL}=3 \mathrm{~mA}, \mathrm{~V}_{\mathrm{CC}}=5 \mathrm{~V}$ |  | 0.4 | V |
|  | Output Low Voltage (ST25 series) | $\mathrm{loL}=2.1 \mathrm{~mA}, \mathrm{~V}_{\mathrm{CC}}=2.5 \mathrm{~V}$ |  | 0.4 | V |

## ST24LC21B, ST24LW21 ST24FC21, ST24FC21B, ST24FW21

## 1 Kbit (x8) Dual Mode Serial EEPROM for VESA PLUG \& PLAY

- 1 MILLION ERASE/WRITE CYCLES
- 40 YEARS DATA RETENTION

■ 3.6 V to 5.5 V or 2.5 V to 5.5 V SINGLE SUPPLY VOLTAGE

- HARDWARE WRITE CONTROL (ST24LW21 and ST24FW21)
- TTL SCHMITT-TRIGGER on VCLK INPUT
- 100k / 400k Hz COMPATIBILITY with the ${ }^{2} \mathrm{C}$ BUS BIT TRANSFER RANGE
- TWO WIRE SERIAL INTERFACE I ${ }^{2} \mathrm{C}$ BUS COMPATIBLE
- I ${ }^{2}$ C PAGE WRITE (up to 8 Bytes)
- ${ }^{2} \mathrm{C}$ BYTE, RANDOM and SEQUENTIAL READ MODES
- SELF TIMED PROGRAMMING CYCLE
- AUTOMATIC ADDRESS INCREMENTING
- ENHANCED ESD/LATCH UP PERFORMANCES
- ERROR RECOVERY MECHANISM (ST24FC21 and ST24FW21) VESA 2 COMPATIBLE


## DESCRIPTION

The ST24LC21B, ST24LW21, ST24FC21, ST24FC21B and ST24FW21 are 1K bit electrically erasable programmable memory (EEPROM), organized in $128 \times 8$ bits. In the text, products are referred as ST24xy21, where "x" is either "L" for VESA 1 or "F" for VESA 2 compatible memories and where "y" indicates the Write Control pin connection: "C" means WC on pin 7 and "W" means WC on pin 3.

Table 1. Signal Names

| SDA | Serial Data Address Input/Output |
| :--- | :--- |
| SCL | Serial Clock ( ${ }^{2}$ C mode) |
| VCC | Supply Voltage |
| VSS | Ground |
| VCLK | Clock Transmit only mode |
| WC | Write Control |



Figure 1. Logic Diagram


Note: WC signal is only available for ST24LW21 and ST24FW21 products.

Figure 2A. DIP Pin Connections

| ST24LC21B |
| :---: |
|  |  |
|  |  |

Warning: NC = Not Connected.

Figure 2C. DIP Pin Connections

| $\begin{aligned} & \text { ST24FC21 } \\ & \text { ST24FC21B } \end{aligned}$ |
| :---: |
|  |
| A101744 |

Warning: NC = Not Connected. DU = Don't Use, must be left open or connected to $V_{C C}$ or $V_{S s}$.

Figure 2E. DIP Pin Connections

| ST24FW21 ST24LW21 |
| :---: |
|  |
| A101746 |

Warning: NC = Not Connected.

Figure 2B. SO Pin Connections


Warning: NC = Not Connected.

Figure 2D. SO Pin Connections


Warning: NC = Not Connected. DU = Don't Use, must be left open or connected to $\mathrm{V}_{\mathrm{Cc}}$ or $\mathrm{V}_{\text {SS }}$.

Figure 2F. SO Pin Connections


Warning: NC = Not Connected.

Table 2. Absolute Maximum Ratings ${ }^{(1)}$

| Symbol | Parameter |  |  | Value | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{T}_{\mathrm{A}}$ | Ambient Operating Temperature |  |  | -40 to 85 | ${ }^{\circ} \mathrm{C}$ |
| TstG | Storage Temperature |  |  | -65 to 150 | ${ }^{\circ} \mathrm{C}$ |
| TLEAD | Lead Temperature, Soldering | (SO8 package) (PSDIP8 package) | $\begin{aligned} & 40 \mathrm{sec} \\ & 10 \mathrm{sec} \end{aligned}$ | $\begin{aligned} & 215 \\ & 260 \end{aligned}$ | ${ }^{\circ} \mathrm{C}$ |
| $\mathrm{V}_{10}$ | Input or Output Voltages |  |  | -0.3 to 6.5 | V |
| $\mathrm{V}_{\mathrm{CC}}$ | Supply Voltage |  |  | -0.3 to 6.5 | V |
| $V_{\text {ESD }}$ | Electrostatic Discharge Voltage (Human Body model) ${ }^{(2)}$ |  |  | 4000 | V |
|  | Electrostatic Discharge Voltage (Machine model) ${ }^{(3)}$ |  |  | 500 | V |

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of thedevice at these or any other conditions above those indicated in the Operating sections of this specification is not mplied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.
2. MIL-STD-883C, 3015.7 (100pF, 1500 |).
3. EIAJ IC-121 (Condition C) (200pF, 0 ) .

Table 3A. Device Select Code (ST24LC21B, ST24LW21, ST24FC21 and ST24FW21)

|  | Device Code |  |  |  | Chip Enable |  |  | R $\bar{W}$ |
| :--- | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Bit | b 7 | b 6 | b 5 | b 4 | b 3 | b 2 | b 1 | b 0 |
| Device Select | 1 | 0 | 1 | 0 | X | X | X | $\mathrm{R} \bar{W}$ |

Note: The MSB b7 is sent first.
$\mathrm{X}=0$ or 1 .

Table 3B. Device Select Code (ST24FC21B)

|  | Device Code |  |  |  | Chip Enable |  |  | RW |
| :--- | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Bit | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
| Device Select | 1 | 0 | 1 | 0 | 0 | 0 | 0 | $R-$ |

Note: The MSB b7 is sent first.
$X=0$ or 1 .

## DESCRIPTION (cont'd)

The ST24xy21 can operate in two modes: Trans-mit-Only mode and $I^{2} \mathrm{C}$ bidirectional mode. When powered, the device is in Transmit-Only mode with EEPROM data clocked out from the rising edge of the signal applied on VCLK.
The device will switch to the $\mathrm{I}^{2} \mathrm{C}$ bidirectional mode upon the falling edge of the signal applied on SCL pin. When in $\mathrm{I}^{2} \mathrm{C}$ mode, the ST24LC21B (or the ST24LW21) cannot switch back to the Transmit Only mode (except when the power supply is removed). For the ST24FC21, ST24FC21B (or the ST24FW21), after the falling edge of SCL, the memory enter in a transition state which allowed to
switch back to the Transmit-Only mode if no valid $I^{2} \mathrm{C}$ activity is observed. Both Plastic Dual-in-Line and Plastic Small Outline packages are available.

## Transmit Only Mode

After a Power-up, the ST24xy21 is in the Transmit Only mode. A proper initialization sequence (see Figure 3) must supply nine clock pulses on the VCLK pin (in order to internally synchronize the device). During this initialization sequence, the SDA pin is in high impedance. On the rising edge of the tenth pulse applied on VCLK pin, the device will output the first bit of byte located at address 00h (most significant bit first).

## LM2596

SIMPLE SWITCHER ${ }^{\circledR}$ Power Converter 150 kHz 3A Step-Down Voltage Regulator

## General Description

The LM2596 series of regulators are monolithic integrated circuits that provide all the active functions for a step-down (buck) switching regulator, capable of driving a 3A load with excellent line and load regulation. These devices are available in fixed output voltages of $3.3 \mathrm{~V}, 5 \mathrm{~V}, 12 \mathrm{~V}$, and an adjustable output version.
Requiring a minimum number of external components, these regulators are simple to use and include internal frequency compensationt, and a fixed-frequency oscillator.
The LM2596 series operates at a switching frequency of 150 kHz thus allowing smaller sized filter components than what would be needed with lower frequency switching regulators. Available in a standard 5-lead TO-220 package with several different lead bend options, and a 5-lead TO-263 surface mount package.
A standard series of inductors are available from several different manufacturers optimized for use with the LM2596 series. This feature greatly simplifies the design of switch-mode power supplies.
Other features include a guaranteed $\pm 4 \%$ tolerance on output voltage under specified input voltage and output load conditions, and $\pm 15 \%$ on the oscillator frequency. External shutdown is included, featuring typically $80 \mu \mathrm{~A}$ standby current. Self protection features include a two stage frequency reducing current limit for the output switch and an over temperature shutdown for complete protection under fault conditions.

## Features

n3.3V, 5V, 12V, and adjustable output versions
nAdjustable version output voltage range, 1.2 V to 37 V
$\pm 4 \%$ max over line and load conditions
nAvailable in TO-220 and TO-263 packages
nGuaranteed 3A output load current
nlnput voltage range up to 40 V
nRequires only 4 external components
nExcellent line and load regulation specifications
n 150 kHz fixed frequency internal oscillator
nTTL shutdown capability
nLow power standby mode, I Q typically $80 \mu \mathrm{~A}$
nHigh efficiency
nUses readily available standard inductors
nThermal shutdown and current limit protection

## Applications

nSimple high-efficiency step-down (buck) regulator
nOn -card switching regulators
nPositive to negative converter
Note: †Patent Number 5,382,918.

Specifications with standard type face are for $\mathrm{T}_{J}=25^{\circ} \mathrm{C}$, and those with boldface type apply over full Operating Temperature Range

| Symbol | Parameter | Conditions | LM2596-5.0 |  | Units (Limits) |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | $\begin{aligned} & \text { Typ } \\ & \text { (Note 3) } \end{aligned}$ | Limit <br> (Note 4) |  |
| SYSTEM PARAMETERS (Note 5) Test Circuit Figure 1 |  |  |  |  |  |
| $\mathrm{V}_{\text {OUT }}$ | Output Voltage | $7 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 40 \mathrm{~V}, 0.2 \mathrm{~A} \leq \mathrm{I}_{\text {LOAD }} \leq 3 \mathrm{~A}$ | 5.0 | $\begin{aligned} & 4.800 / 4.750 \\ & 5.200 / 5.250 \end{aligned}$ | $\begin{aligned} & V{ }_{V(\min )} V \\ & V(\max ) \end{aligned}$ |
| $\eta$ | Efficiency | $\mathrm{V}_{\text {IN }}=12 \mathrm{~V}, \mathrm{I}_{\text {LOAD }}=3 \mathrm{~A}$ | 80 |  | \% |

## ANALOG MULTIPLEXERS-DEMULTIPLEXERS

## 4051B - SINGLE 8-CHANNEL

4052B - DIFFERENTIAL 4-CHANNEL
4053B - TRIPLE 2-CHANNEL

- QUIESCENT CURRENT SPECIFIED TO 20V FOR HCC DEVICE
- LOW "ON" RESISTANCE : $125 \Omega$ (typ.) OVER 15 V p.p. SIGNAL-INPUT RANGE FOR VDD $V_{E E}=15 \mathrm{~V}$
- HIGH "OFF" RESISTANCE : CHANNEL LEAK$A G E \pm 100 p A$ (typ.) $V_{D D}-V_{E E}=18 \mathrm{~V}$
- BINARY ADDRESS DECODING ON CHIP
- VERY LOW QUIESCENT POWER DISSIPATION UNDER ALL DIGITAL CONTROL INPUT AND SUPPLY CONDITIONS : $0.2 \mu \mathrm{~W}$ (typ.), $V_{D D}-V_{S S}=V_{D D}-V_{E E}=10 \mathrm{~V}$
MATCHED SWITCH CHARACTERISTICS : RON $=5 \Omega$ (typ.) for $V_{D D}-V_{E E}=15 \mathrm{~V}$
- WIDE RANGE OF DIGITALAND ANALOG SIGNAL LEVELS : DIGITAL 3 TO 20V, ANALOG TO 20 V p.p.
- 5V, 10 V , AND 15V PARAMETRIC RATINGS
- INPUT CURRENT OF 100mA AT 18V AND 25)C FOR HCC DEVICE
- 100\% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDECTENTATIVE STANDARD ${ }^{\circ}$ 13A, "STANDARD SPECIFICATIONS FOR DESCRIPTION OF "B" SERIES CMOS DEVICES"



## DESCRIPTION

The HCC 4051B, 4052B and 4053B (extended temperature range) and HCF4051B, 4052B and 4053B (intermediate temperature range) are monolithic integrated circuits, available in 16 -lead dual in-line plastic or ceramic package and plastic micropackage. HCC/HCF4051B, HCC/HCF4052B, and HCC/HCF4053B analog multiplexers/demultiplexers are digitally controlled analog switches having low ON impedanœ and very low OFF leakage

PIN CONNECTIONS

current. These multiplexer circuits dissipate extremely low quiescent power over the full $\mathrm{V}_{\mathrm{DD}}-\mathrm{V}_{\mathrm{SS}}$ and $\mathrm{V}_{\mathrm{DD}}$ - $\mathrm{V}_{\mathrm{EE}}$ supply-voltage ranges, independent of the logic state of the control signals. When a-logic " 1 " is present at the inhibit input terminal all channel are off. The HCC/HCF4051B is a single 8-channel multiplexer having three binary control inputs, A, B, and $C$, and an inhibit input. The three binary signals select 1 of 8 channels to be turned on, and connect one of the 8 inputs to the output. The HCC/HCF4052B is a differential 4-channel multi-
plexer having two binary control inputs, $A$ and $B$, and an inhibit input. The two binary input signals select 1 of 4 pairs of channels to be turned on and connect the analog inputs to the outputs. The HCC/HCF4053B is a triple 2-channel multiplexer having three separate digital control inputs, $\mathrm{A}, \mathrm{B}$, and C , and an inhibit input. Each control input selects one of a pair of channels which are connected in a singlepole double-throw configuration.

FUNCTIONAL DIAGRAMS AND TRUTH TABLES


FUNCTIONAL DIAGRAMS AND TRUTH TABLES (continued)


ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
| :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\mathrm{DD}}{ }^{*}$ | Supply Voltage : HCC Types <br> HCF Types | $\begin{aligned} & -0.5 \text { to }+20 \\ & -0.5 \text { to }+18 \\ & \hline \end{aligned}$ | $\begin{aligned} & \hline \mathrm{V} \\ & \mathrm{~V} \end{aligned}$ |
| $\mathrm{V}_{\mathrm{i}}$ | Input Voltage | -0.5 to $\mathrm{V}_{\mathrm{DD}}+0.5$ | V |
| $I_{1}$ | DC Input Current (any one input) | $\pm 10$ | mA |
| $\mathrm{P}_{\text {tot }}$ | Total Power Dissipation (per package) Dissipation per Output Transistor for $\mathrm{T}_{\mathrm{op}}=$ Full Package-temperature Range | $\begin{aligned} & 200 \\ & 100 \\ & \hline \end{aligned}$ | mW <br> mW |
| $\mathrm{T}_{\text {op }}$ | Operating Temperature : HCC Types <br> HCF Types | $\begin{aligned} & -55 \text { to }+125 \\ & -40 \text { to }+85 \end{aligned}$ | $\begin{aligned} & \mathrm{\imath C} \\ & \mathrm{nc} \end{aligned}$ |
| $\mathrm{T}_{\text {stg }}$ | Storage Temperature | -65 to + 150 | 1 C |

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for external periods may affect device reliability.

* All voltage values are referred to $\mathrm{V}_{\text {ss }}$ pin voltage.


## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Value | Unit |
| :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\mathrm{DD}}$ | Supply Voltage : HCC Types |  |  |
| HCF Types |  |  |  |

STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

( $\propto$ ) Determined by minimum feasible leakage measurement for automatic testing.
(*) TLow $=-551 \mathrm{C}$ for HCC device : - 40 1C for HCF device.
(*) $\mathrm{T}_{\text {High }}=+125 \mathrm{hC}$ for HCC device : + 85ㄷC for HCF device.

DYNAMIC ELECTRICAL CHARACTERISTICS
( $\mathrm{T}_{\mathrm{amb}}=251 \mathrm{C}, \mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}$ all input square wave rise and fall time $=20 \mathrm{~ns}$ )

( $\infty$ Peak to peak voltage symmetrical about $V_{D D}-V_{E E}$
(*) Both ends of channel.

## MSP34X0G

## Release Note:

The hardware and software description in this document is valid for the MSP 34x0G version B8 and following versions.

## Introduction

The MSP $34 \times 0$ G family of single-chip Multistandard Sound Processors covers the sound processing of all analog TV-Standards worldwide, as well as the NICAM digital sound standards. The full TV sound processing, starting with analog sound IF signal-in, down to processed analog AF-out, is performed on a single chip. Figure $1-1$ shows a simplified functional block diagram of the MSP $34 \times 0 \mathrm{G}$.

This new generation of TV sound processing ICs now includes versions for processing the multichannel television sound (MTS) signal conforming to the standard recommended by the Broadcast Television Systems Committee (BTSC). The DBX noise reduction, or alternatively, Micronas Noise Reduction (MNR) is performed alignment free.

Other processed standards are the Japanese FM-FM multiplex standard (EIA-J) and the FM Stereo Radio standard.

Current ICs have to perform adjustment procedures in order to achieve good stereo separation for BTSC and EIA-J. The MSP $34 \times 0 \mathrm{G}$ has optimum stereo performance without any adjustments.

All MSP $34 \times x$ versions are pin compatible to the MSP $34 x x$ D. Only minor modifications are necessary to adapt a MSP $34 \times x$ D controlling software to the MSP $34 \times x$. The MSP $34 \times 0$ G further simplifies controlling software. Standard selection requires a single $1^{2} \mathrm{C}$ transmission only.

The MSP $34 \times 0$ G has built-in automatic functions: The IC is able to detect the actual sound standard automatically (Automatic Standard Detection). Furthermore, pilot levels and identification signals can be evaluated internally with subsequent switching between mono/ stereo/bilingual; no $\mathrm{I}^{2} \mathrm{C}$ interaction is necessary (Automatic Sound Selection).

The MSP $34 \times 0 \mathrm{G}$ can handle very high FM deviations even in conjunction with NICAM processing. This is especially important for the introduction of NICAM in China.

The ICs are produced in submicron CMOS technology. The MSP $34 \times 0$ is available in the following packages: PLCC68 (not intended for new design), PSDIP64, PSDIP52, PQFP80, and PLQFP64.


Fig. 1-1: Simplified functional block diagram of the MSP

## Electrical Characteristics

## Absolute Maximum Ratings

| Symbol | Parameter | Pin Name | Min. | Max. | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{T}_{\mathrm{A}}$ | Ambient Operating Temperature |  | 0 | 70 | 1C |
| $\mathrm{T}_{\text {S }}$ | Storage Temperature |  | 40 | 125 | nc |
| $\mathrm{V}_{\text {SUP1 }}$ | First Supply Voltage | AHVSUP | 0.3 | 9.0 | V |
| $V_{\text {SUP2 }}$ | Second Supply Voltage | DVSUP | 0.3 | 6.0 | V |
| $\mathrm{V}_{\text {SUP } 3}$ | Third Supply Voltage | AVSUP | 0.3 | 6.0 | V |
| $\mathrm{dV}_{\text {SUP23 }}$ | Voltage between AVSUP and DVSUP | AVSUP, DVSUP | 0.5 | 0.5 | V |
| $\mathrm{P}_{\text {TOT }}$ | Power Dissipation <br> PLCC68 <br> PSDIP64 <br> PSDIP52 <br> PQFP80 <br> PLQFP64 | AHVSUP, DVSUP, AVSUP |  | $\begin{array}{r} 1200 \\ 1300 \\ 1200 \\ 1000 \\ 960 \end{array}$ | mW <br> mW <br> mW <br> mW <br> mW |
| $\mathrm{V}_{\text {Idig }}$ | Input Voltage, all Digital Inputs |  | 0.3 | $\mathrm{V}_{\text {SUP } 2}+0.3$ | V |
| $\mathrm{I}_{\text {dig }}$ | Input Current, all Digital Pins |  | 20 | +20 | $\mathrm{mA}^{1)}$ |
| $\mathrm{V}_{\text {lana }}$ | Input Voltage, all Analog Inputs | $\begin{aligned} & \text { SCn_IN_s, }{ }^{2)} \\ & \text { MONO_IN } \end{aligned}$ | 0.3 | $\mathrm{V}_{\text {SUP } 1}+0.3$ | V |
| $\mathrm{I}_{\text {lana }}$ | Input Current, all Analog Inputs | $\begin{aligned} & \text { SCn_IN_s, }{ }^{2)} \\ & \text { MONO_IN } \end{aligned}$ | 5 | +5 | $m A^{1)}$ |
| $\mathrm{I}_{\text {Oana }}$ | Output Current, all SCART Outputs | SCn_OUT_s ${ }^{2}$ | ${ }^{3)}$, 4) | ${ }^{3)}$, 4) |  |
| loana | Output Current, all Analog Outputs except SCART Outputs | DACp_s ${ }^{2}$ | 3) | 3) |  |
| $\mathrm{I}_{\text {Cana }}$ | Output Current, other pins connected to capacitors | $\begin{aligned} & \text { CAPL_p,2) } \\ & \text { AGNDC } \end{aligned}$ | 3) | 3) |  |
| ${ }^{\text {1) }}$ positive value means current flowing into the circuit <br> 2) " $n$ " means " 1 ", " 2 ", " 3 ", or " 4 ", " $s$ " means " $L$ " or " $R$ ", " $p$ " means " $M$ " or " $A$ " <br> ${ }^{3)}$ The analog outputs are short-circuit proof with respect to First Supply Voltage and ground. <br> ${ }^{4)}$ Total chip power dissipation must not exceed absolute maximum rating. |  |  |  |  |  |

Stresses beyond those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only. Functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions/Characteristics" of this specification is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

## 21- DVD BOARD



## 22-DVD OUT PCB



## 23- LED 01



LED01

## 24-PC BOARD

HUO1


```
A B B C C P
```

D E







## 26- PUSH SET




[^0]:    * Preliminary

[^1]:    $1 V_{F}$ is the difference between lowest and highest $V_{F}$ in a multiple diode component.

[^2]:    TRI-STATE ${ }^{\text {© }}$ is a registered trademark of National Semiconductor Corporation

