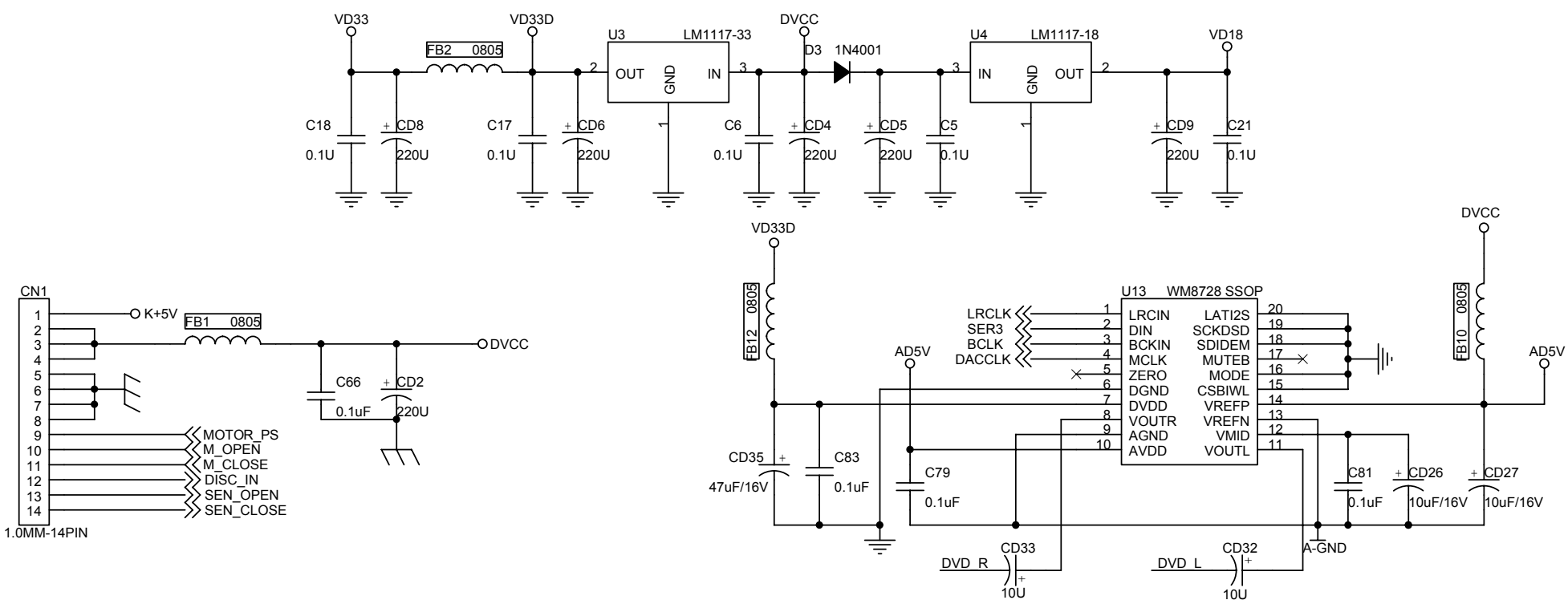
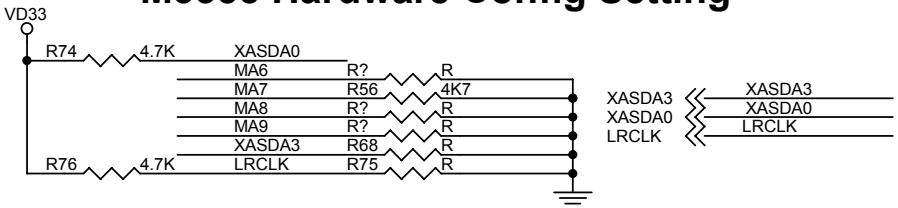


M3355 Hardware Config Setting



1. DMFSEL[1:0] :Sdram Clock select 108M, 121.5M,128.25M,135Mhz MA[8:7]
   00:Select 108Mhz
   01:Select 128.25Mhz
   10:Select 135Mhz
   11:Select 121.5Mhz(Default)
2. EJTAGDBG :1:Use EJTAG debug and or use RS232 PMON to control CPU to debug, MA[9]
   1:Use EJTAG debug, but still keep CTXD pin, CRXD is from XGPIO[5](Default)
   0:Use RS232 to debug or down load, No need EJTAG. CRXD is from XTDI.
3. VGAENJ : default 1, 0 to enable VGA pin HSYNC/VSYNC from pin Servo Flag XFLAG [1:0], XASDA3
   0:VGA is enable, VSYNC from XFLAG[1], HSYNC from XFLAG[0].
   1:VGA is disable.(Default)
4. ROM8EN : 1, MA[6]
   1: 8 bits rom data bus
   0:16 bits rom data bus
5. UPDBGOUT : 1, XBCLK is normal digital output or internal PLL clock output, XASDA0
   1:XASDA3 is normal digital audio output.
   0:XASDA3 is output XTOCK, this is internal PLL clock output.
6. TM_HWCFGA :1 XLRCLK for CPUCLK_SEL
   1:108 MHZ
   0:121 MHZ