Design Example Report

Title	***27 W Power Supply Using TOP266EG***
Specification	90 VAC – 265 VAC Input; 5 V, 2.5 A and 14.5 V, 1 A Outputs
Application	LCD Monitor
Author	Applications Engineering Department
Document Number	DER-235
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Revision	1.0

Summary and Features

- Very low standby consumption
  - <100 mW Input power with 4 mA load on 5 V output
    - 90 mW at 240 VAC input
    - 95 mW at 265 VAC Input
- Very low no-load input power
  - No-load Input power of 60 mW at 230 VAC input
- High full-load efficiency
- Greater than 80.5% efficiency at 90 VAC / 60 Hz
- Less than 55°C plastic temperature of TOPSwitch device at 90 VAC / 60 Hz, 25°C room temperature
  - Easily meets industry thermal requirement of <90°C at 50°C ambient
- Greater than 6 dB margin on conducted EMI
- Hysteretic output overvoltage protection
- Hysteretic output short circuit protection
- Hysteretic thermal overload protection with large hysteresis

PATENT INFORMATION
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Important Note:
Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.

1 Introduction

This document is an engineering report describing a 5 V / 2.5 A, 14.5 V / 1 A power supply utilizing a TOP266EG. The TOP266EG is part of the TOPSwitch-JX IC family from Power Integrations.

The document contains the power supply specification, schematic, bill of materials, transformer documentation, printed circuit layout, and performance data.

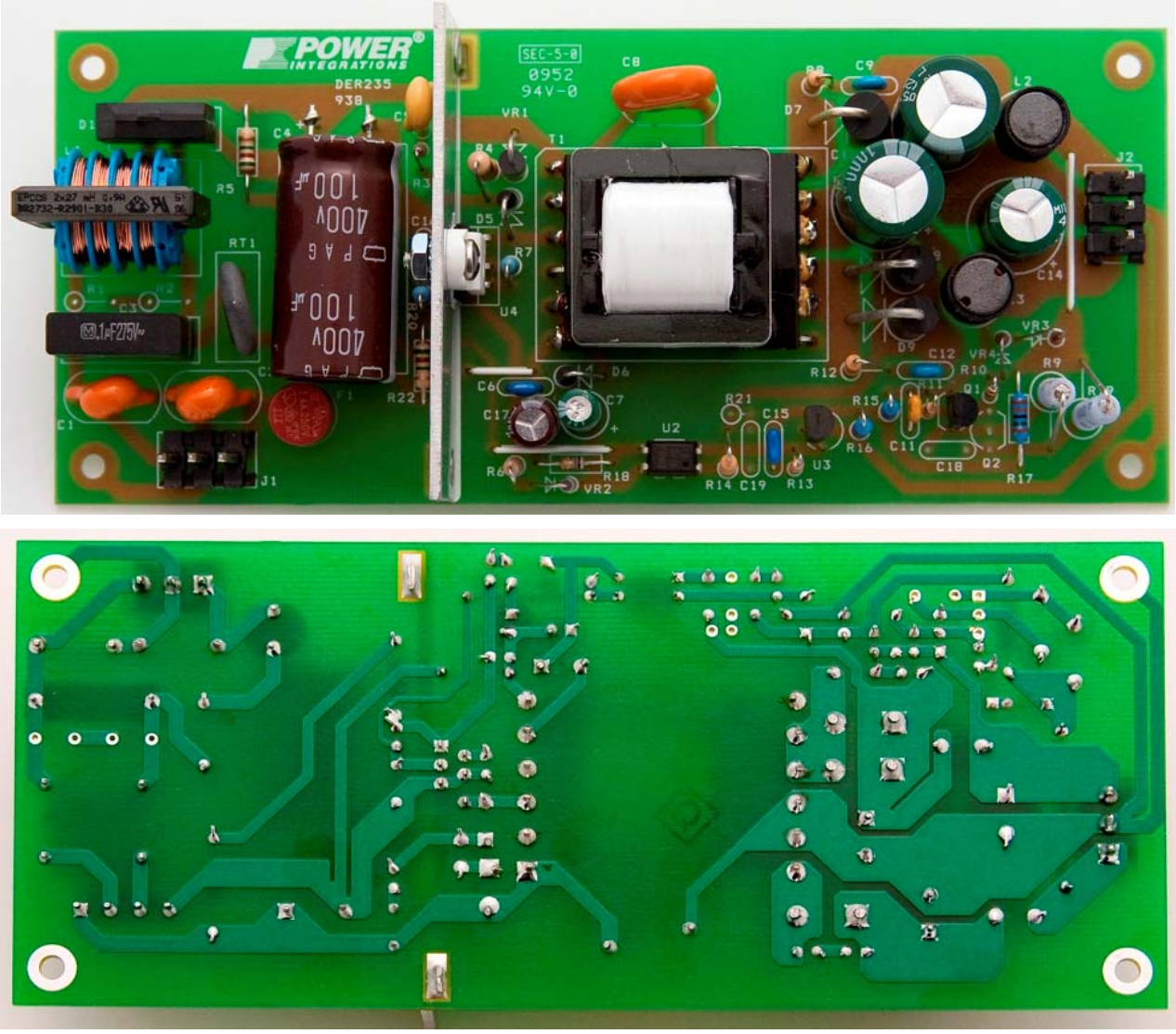


Figure 1 – Populated Board.

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2 Power Supply Specification

The table below represents the minimum acceptable performance of the design. Actual performance is listed in the results section.

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	V_{IN}	90		265	VAC	3 Wire – with P.E.
Frequency	f_{LINE}	47	50/60	64	Hz	
No-load Input Power (264 VAC)				<0.1	W	With 4mA load on 5V output
Output						
Output Voltage 1	V_{OUT1}	4.75	5	5.25	V	± 5%
Output Ripple Voltage 1	$V_{RIPPLE1}$			50	mV	
Output Current 1	I_{OUT1}	0		2.5	A	
Output Voltage 2	V_{OUT2}	12.3	14.5	16.7	V	± 15%
Output Ripple Voltage 2	$V_{RIPPLE2}$			500	mV	20 MHz bandwidth
Output Current 2	I_{OUT2}	0		1	A	
Total Output Power						
Continuous Output Power	P_{OUT}			27	W	
Efficiency						
Full Load (90VAC)	η	80			%	Measured at P_{OUT} 25 °C
Environmental						
Conducted EMI		Meets CISPR22B / EN55022B				
Safety		Designed to meet IEC950, UL1950 Class II				
Ambient Temperature	T_{AMB}	0		50	°C	Free convection, sea level

3 Schematic

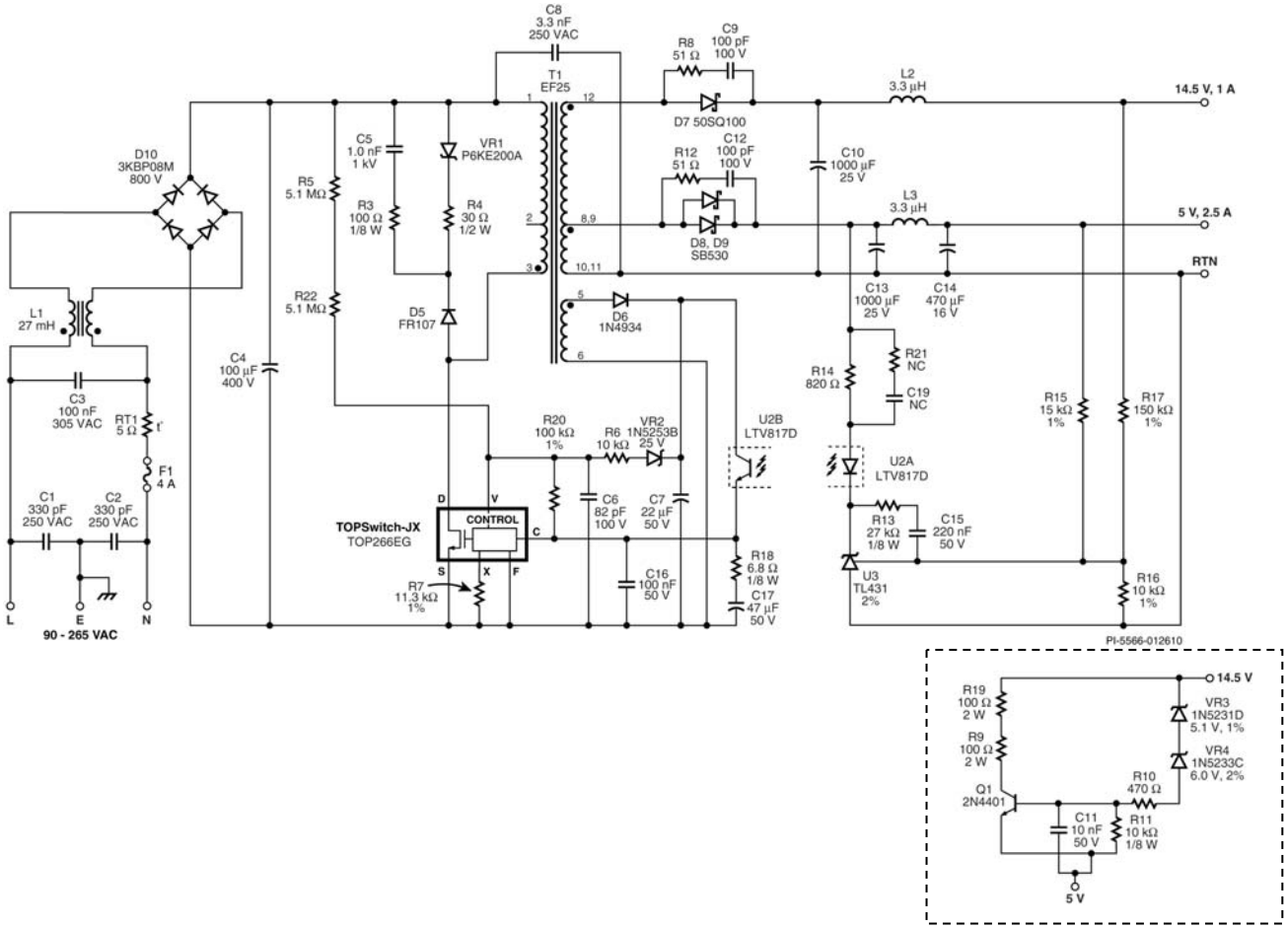


Figure 2 – Schematic (including optional active pre-load to improve output cross regulation).

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4 Circuit Description

The power supply employs a TOPSwitch-JX TOP266EG device (U1) with an integrated high voltage MOSFET and a controller in a flyback configuration.

4.1 Input EMI Filtering and Rectification

Capacitors C1, C2 and C3 together with common mode choke L1 forms an EMI filter that attenuates both common mode and differential mode conducted EMI. Diode Bridge D10 rectifies the AC input. A 3 A rated bridge was selected for D10 to improve low line, full load efficiency.

4.2 TOPSwitch-JX Primary

The TOP266EG device (U1) integrates an oscillator, a switch controller, startup and protection circuitry, and a power MOSFET, all on one monolithic IC. One side of the power transformer (T1) primary winding is connected to the positive side of the bulk capacitors C4, and the other side are connected to the DRAIN pin of U1. When the MOSFET turns off, the leakage inductance of the transformer induces a voltage spike on the drain node. The amplitude of that spike is limited by a clamp network that consists of D5, R4, VR1, R3 and C5. The majority of the dissipation occurs in VR1 and R4 with the series combination of R3 and C5 (in parallel with R4 and VR1) share some of the dissipation and reduce high frequency ringing. Resistor R4 determines the proportion of dissipation between the two networks. This arrangement was selected to reduce clamp losses under light and no-load conditions.

The line under-undervoltage threshold of 95 V_{DC} is determined by the current supplied via resistors R5, R22 and R20 and the V pin current threshold of 25 μA. The addition of R20 reduces the dissipation of R5 and R22, improving no-load input power. This also effectively disabled the line OV shutdown (threshold is >800 V_{DC}) but the design easily passed differential surge levels above the 1 kV. The value of R20 was selected to ensure that the V pin current is above the UV threshold when the CONTROL pin is at 4.8 V during auto-restart. This ensures correct auto-restart timing. Resistor R6 and Zener diode VR2 are used for output overvoltage protection, for example during an open loop fault, triggering non-latching shut-down when the V pin current exceeds 112 μA.

Note for this power level the TOP265 is also suitable providing a slight reduction in efficiency and rise in device temperature is acceptable.

4.3 Output Rectification

Diodes D8 and D9 rectify the 5 V secondary winding output of T1. The output voltage is filtered by C13, L3, and C14. Resistor R12 and capacitor C12 snubs the voltage spike caused by the commutation of D8 and D9. Diode D7 rectifies the 14.5 V secondary winding output of T1. The output voltage is filtered by C10 and L2. Resistor R8 and capacitor C9 absorb the noise caused by the commutation of D7. Dual axial diodes were used for D8 and D9 for both low cost but maintaining high efficiency compared to a single TO220 higher current diode with an external heatsink. The two axial diodes are co-

located and share the same copper area on the cathode side to ensure thermal tracking. The resultant current sharing was excellent as can be seen in the thermal image where the diodes are operating at the same temperature indicting similar diode currents.

A low voltage rating (30 V) was achievable for D8 and D9 due to the flexibility of a higher turns ratio (higher VOR) due to the 725 V rating of the MOSFET in U1. This further improved efficiency as the V_F of a 30 V diode is lower than the >50 V diode typically required for designs where the MOSFET rating is 600 V or 650 V.

4.4 Output Feedback

The output voltage regulation is set by voltage dividers formed by R15, R17 and R16 and the shunt regulator U3. Resistor R13 and capacitor are compensation elements around error amplifier U3. A high CTR opto-coupler was selected for U2 to minimize the secondary side feedback (opto) current and thereby reduce no-load and standby input power. To reduce the feedback losses on the primary side the number of bias winding turns on the transformer and the value of C7 was optimized to give a minimum voltage of 9 V at high line under standby loading conditions (voltage monitored across C7 with an oscilloscope to ensure lowest voltage ≥8.5 V).

An active pre-load (shunt-regulator) was included to prevent an unloaded 14.5 V output rising outside of specification while the 5 V is loaded. This circuit is formed by VR3, VR4, R10, R11, C11, Q1, R9 and R19. When the difference between the 5 V and 14.5 V outputs exceeds the voltage defined by VR3, VR4 and the V_{BE} of Q1, Q1 is biased on and current is shunted from the 14.5 V output into the 5 V output via R9 and R19. If the 14.5 V output always has a minimum load then this circuit can be omitted.

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5 PCB Layout

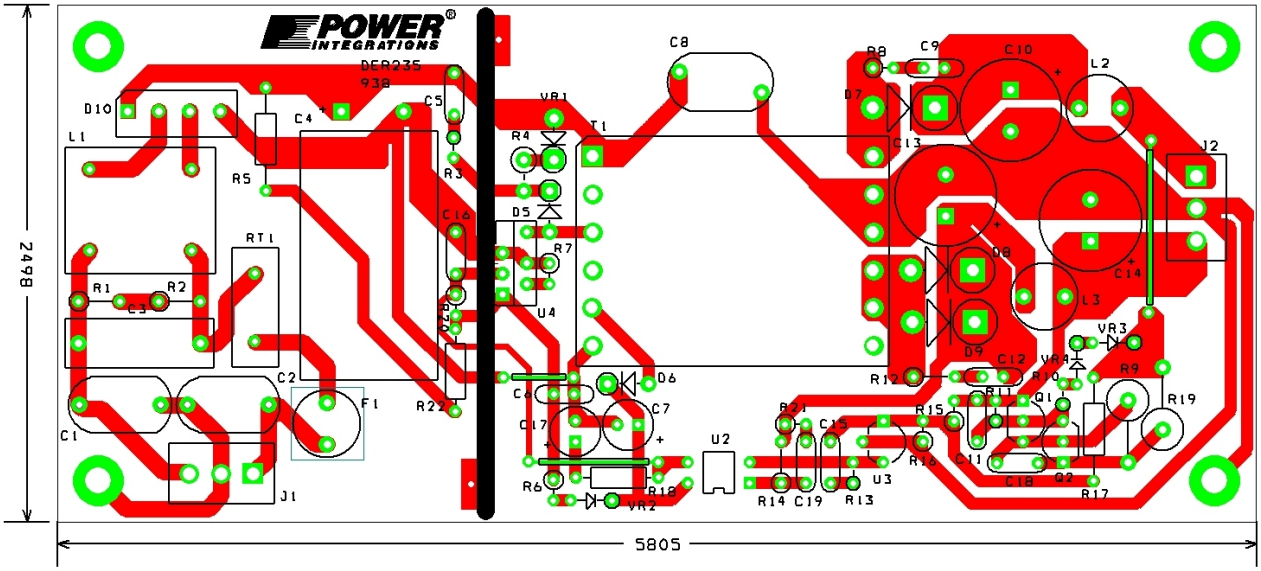


Figure 3 – PCB Layout.

6 Bill of Materials

Item	Qty	Ref Des	Description	Mfg Part Number	Manufacturer
1	2	C1 C2	330 pF, 250 VAC, Film, X1Y1	CD70-B2GA221KYAS	TDK
2	1	C3	100 nF, 275VAC, Film, X2	F1772-410-2000	Vishay/Roederstein
3	1	C4	100 µF, 400 V, Electrolytic, Low ESR, (16 x 30)	EPAG401ELL101ML30S	Nippon Chemi-Con
4	1	C5	0.001 µF, 1 kV, Disc Ceramic	562R10TSD10	Vishay
5	1	C6	82 pF, 100 V, Ceramic, COG	B37979N1820J000	Epcos
6	1	C7	22 µF, 50 V, Electrolytic, Very Low ESR, 340 mΩ, (5 x 11)	EKZE500ELL220ME11D	Nippon Chemi-Con
7	1	C8	3.3 nF, Ceramic, Y1	440LD33-R	Vishay
8	2	C9 C12	100 pF, 100 V, Ceramic, COG	B37979N1101J000	Epcos
9	2	C10 C13	1000 µF, 25 V, Electrolytic, Very Low ESR, 21 mΩ, (12.5 x 20)	EKZE250ELL102MK20S	Nippon Chemi-Con
10	1	C11	100 nF, 50 V, Ceramic, Z5U, .2Lead Space	C317C104M5U5TA	Kemet
11	1	C14	470 µF, 16 V, Electrolytic, Very Low ESR, 53 mΩ, (10 x 12.5)	EKZE160ELL471MJC5S	Nippon Chemi-Con
12	1	C15	220 nF, 50 V, Ceramic, X7R	B37987F5224K000	Epcos
13	1	C16	100 nF, 50 V, Ceramic, X7R	RPER71H104K2K1A03B	Murata
14	1	C17	47 µF, 50 V, Electrolytic, Gen. Purpose, (6.3 x 11)	EKMG500ELL470MF11D	Nippon Chemi-Con
15	1	C19	Not installed		
16	1	D5	1000 V, 1 A, Fast Recovery Diode, DO-41	FR107-T-F	Diodes Inc.
17	1	D6	100 V, 1 A, Fast Recovery, 200 ns, DO-41	1N4934	Vishay
18	1	D7	100 V, 5 A, Schottky, DO-201AR	VS-50SQ100	Vishay
19	2	D8 D9	30 V, 5 A, Schottky, DO-201AD	SB530	Vishay
20	1	D10	800 V, 3 A, Bridge Rectifier, Glass Passivated	3KBP08M-E4/51	Vishay
21	1	F1	4 A, 250V, Slow, TR5	3721400041	Wickman
22	2	J1 J2	3 Position (1 x 3) header, 0.156 pitch, Vertical	26-48-1031	Molex
23	1	L1	27 mH, 0.9 A, Common Mode Choke	B82732-R2901-B30	Epcos
24	2	L2 L3	3.3 µH, 5.7 A	ELC08D3R3E	Panasonic
25	4	MTG HOLE	Mounting Hole No 4		
26	1	Q1	NPN, Small Signal BJT, 40 V, 0.6 A, TO-92	2N4401BU	Fairchild Semiconductor
27	1	R3	100 Ω, 5%, 1/8 W, Carbon Film	CFR-12JB-100R	Yageo
28	1	R4	30 Ω, 5%, 1/2 W, Carbon Film	CFR-50JB-30R	Yageo
29	2	R5 R22	5.1 MΩ, 5%, 1/4 W, Carbon Film	CFR-25JB-5M1	Yageo
30	1	R6	10 kΩ, 5%, 1/4 W, Carbon Film	CFR-25JB-10K	Yageo
31	1	R7	11.3 kΩ, 1%, 1/4 W, Metal Film	MFR-25FBF-11K3	Yageo
32	2	R8 R12	51 Ω, 5%, 1/4 W, Carbon Film	CFR-25JB-51R	Yageo
33	2	R9 R19	100 Ω, 5%, 2 W, Metal Oxide	RSF200JB-100R	Yageo
34	1	R10	470 Ω, 5%, 1/8 W, Carbon Film	CFR-12JB-470R	Yageo
35	1	R11	10 kΩ, 5%, 1/8 W, Carbon Film	CFR-12JB-10K	Yageo
36	1	R13	27 kΩ, 5%, 1/8 W, Carbon Film	CFR-12JB-27K	Yageo
37	1	R14	820 Ω, 5%, 1/4 W, Carbon Film	CFR-25JB-820R	Yageo
38	1	R15	15 kΩ, 1%, 1/4 W, Metal Film	MFR-25FBF-15K0	Yageo
39	1	R16	10 kΩ, 1%, 1/4 W, Metal Film	ERO-S2PHF1002	Panasonic
40	1	R17	150 kΩ, 1%, 1/4 W, Metal Film	MFR-25FBF-150K	Yageo
41	1	R18	6.8 Ω, 5%, 1/8 W, Carbon Film	CFR-12JB-6R8	Yageo
42	1	R20	100 k, 1%, 1/4 W, Metal Film	MFR-25FBF-100K	Yageo
43	1	R21	Not installed		
44	1	RT1	NTC Thermistor, 5 Ohms, 2.8 A	CL160	Thermometrics
45	1	T1	Bobbin, EF25, Horizontal, 12 pins	YC2504	Ying Chin
46	2	TERMINAL EYELET	Terminal, Eyelet, Tin Plated Brass, Zierick PN 190	190	Zierick

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47	1	U1	TOPSwitch-JX, TOP266EG, eSIP-7C	TOP266EG	Power Integrations
48	1	U2	Opto coupler, 35 V, CTR 300-600%, 4-DIP	LTV-817D	Liteon
49	1	U3	2.495 V Shunt Regulator IC, 2%, 0 to 70C, TO-92	TL431CLPG	On Semiconductor
50	1	VR1	200 V, 5 W, 5%, TVS, DO204AC (DO-15)	P6KE200ARLG	OnSemi
51	1	VR2	25 V, 5%, 500 mW, DO-35	1N5253B	Microsemi
52	1	VR3	5.1 V, 1%, 500 mW, DO-35	1N5231D	Microsemi
53	1	VR4	6.0 V, 2%, 500 mW, DO-35	1N5233C	Microsemi

7 Transformer Specification

7.1 Electrical Diagram

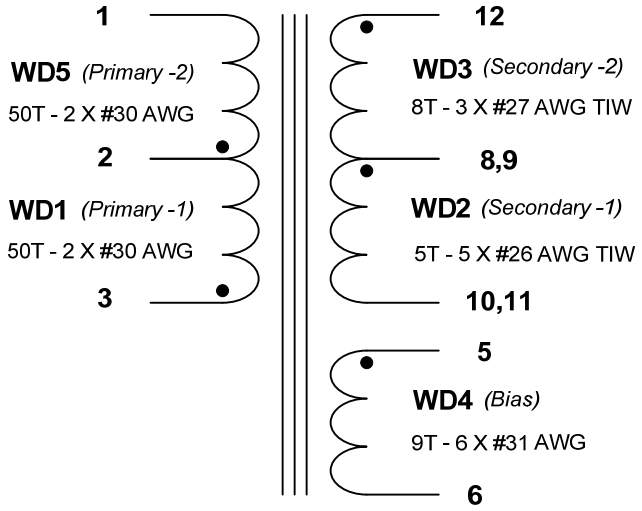


Figure 4 – Transformer Electrical Diagram.

7.2 Electrical Specifications

Electrical Strength	1 second, 60 Hz, from pins 1-6 to pins 7-12	3000 VAC
Primary Inductance	Pins 1-3, all other windings open, measured at 100 kHz, 0.4 VRMS	677 µH, ± 5%
Resonant Frequency	Pins 1-3, all other windings open	400 kHz (Min.)
Primary Leakage Inductance	Pins 1-3, with pins 8, 9, 10, 11, 12 shorted, measured at 100 kHz, 0.4 VRMS	25 µH (Max.)

7.3 Materials

Item	Description
[1]	Core: EF25, NC-2H (Nicera) or equivalent, gapped for ALG of 57 nH/t²
[2]	Bobbin: Generic, 6 primary + 6 seconday
[3]	Barrier tape: Polyester film (1 mil base thickness), 15.60 mm wide
[4]	Varnish
[5]	Magnet wire: #30 AWG, solderable double coated
[6]	Magnet wire: #31 AWG, solderable double coated
[7]	Triple Insulated Wire: #26 AWG
[8]	Triple Insulated Wire: #27 AWG

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7.4 Transformer Build Diagram

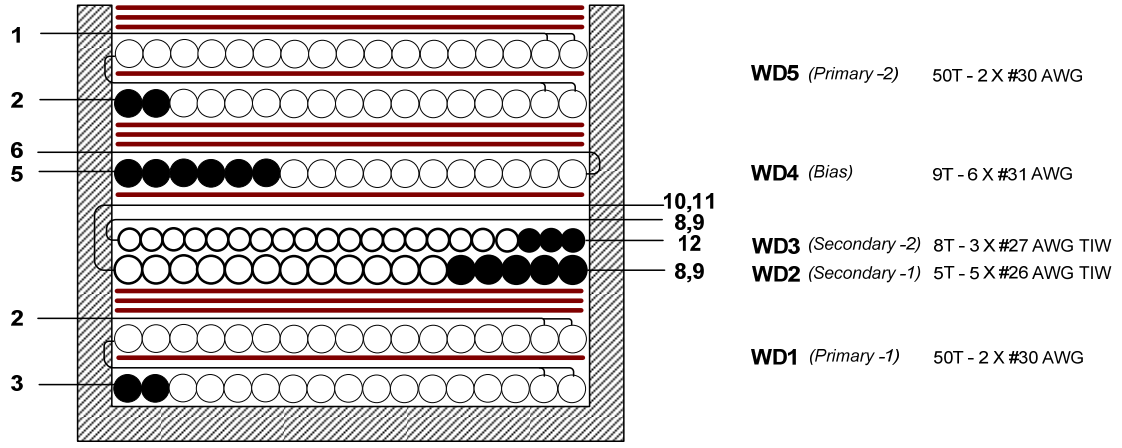


Figure 5 – Transformer Build Diagram.

7.5 Transformer Construction

WD1 1st Half of Primary	Start on pin(s) 3, wind 25 turns (x 2 filar) of item [5] in 1 layer(s) from left to right. Return the wire to left side. Use 1 layer of tape item [3]. Wind 25 turns (x 2 filar) of item [5] in 1 layer(s) from left to right. Return the wire to left side and finish this winding on pin(s) 2.
Basic Insulation	Use 3 layer of tape, item [3], for insulation.
WD2 Secondary Winding 5 V	Start on pins 8 and 9 wind 5 turns (x 5 filar) of item [7] from right to left. Wind in same rotational direction as primary winding. Spread the winding evenly across entire bobbin. Set the wire temporarily at primary side.
WD3 Secondary Winding 14.5 V	Start on pin 12 wind 8 turns (x 3 filar) of item [8] from right to left. Wind in same rotational direction as primary winding. Spread the winding evenly across entire bobbin. Bring to wire back to secondary side and finish at pins 8 and 9. Bring the wire for WD2 back to secondary side and finish at pins 10 and 11.
Basic Insulation	Use 1 layer of tape, item [3], for insulation.
WD4 Bias	Start on pin(s) 5 and wind 9 turns (x 6 filar) of item [6]. Spread the winding evenly across entire bobbin. Finish this winding on pin(s) 6.
Basic Insulation	Use 3 layers of item [4] for basic insulation.
WD6 2nd Half of Primary	Start on pin(s) 2, wind 25 turns (x 2 filar) of item [5] in 1 layer(s) from left to right. Return the wire to left side. Use 1 layer of tape item [3]. Wind 25 turns (x 2 filar) of item [5] in 1 layer(s) from left to right. Return the wire to left side and finish this winding on pin(s) 1.
Outer Wrap	Wrap windings with 3 layers of tape [item [4].
Core Preparation	Prepare the core to get the correct primary inductance.
Final Assembly	Assemble and secure core halves with tape.
Varnishing	Dip varnish the transformer in item [4].

8 Transformer Design Spreadsheet

ACDC_TOPSwitchJX_120709; Rev.1.1; Copyright Power Integrations 2009	INPUT	INFO	OUTPUT	UNIT	TOP_JX_120709: TOPSwitch-JX Continuous/Discontinuous Flyback Transformer Design Spreadsheet
ENTER APPLICATION VARIABLES					
VACMIN	90			Volts	Minimum AC Input Voltage
VACMAX	265			Volts	Maximum AC Input Voltage
fL	50			Hertz	AC Mains Frequency
VO	5.00			Volts	Output Voltage (main)
PO_AVG	27.00			Watts	Average Output Power
PO_PEAK			27.00	Watts	Peak Output Power
Heatsink Type	**External**		External		Heatsink Type
Enclosure	**Open Frame**				Open Frame enclosure assume sufficienct airflow while adapter means a sealed enclosure.
n	0.80			%/100	Efficiency Estimate
Z	0.50				Loss Allocation Factor
VB	9	*Info*		Volts	Ensure proper operation at no load.
tC	3.00			ms	Bridge Rectifier Conduction Time Estimate
CIN	100.0		100	uFarads	Input Filter Capacitor
ENTER TOPSWITCH-JX VARIABLES					
TOPSwitch-JX	**TOP266E**			Universal / Peak	115 Doubled/230V
Chosen Device		*TOP266E*	Power Out	86 W / 86 W	119W
KI	0.55				External Ilimit reduction factor (KI=1.0 for default ILIMIT, KI <1.0 for lower ILIMIT)
ILIMITMIN_EXT			1.304	Amps	Use 1% resistor in setting external ILIMIT
ILIMITMAX_EXT			1.500	Amps	Use 1% resistor in setting external ILIMIT
Frequency (F)=132kHz, (H)=66kHz	**F**		F		Select 'H' for Half frequency - 66kHz, or 'F' for Full frequency - 132kHz
fS			132000	Hertz	TOPSwitch-JX Switching Frequency: Choose between 132 kHz and 66 kHz
fSmin			119000	Hertz	TOPSwitch-JX Minimum Switching Frequency
fSmax			145000	Hertz	TOPSwitch-JX Maximum Switching Frequency
High Line Operating Mode			FF		Full Frequency, Jitter enabled
VOR	110.00			Volts	Reflected Output Voltage
VDS			10	Volts	TOPSwitch on-state Drain to Source Voltage
VD	0.50			Volts	Output Winding Diode Forward Voltage Drop
VDB	0.70			Volts	Bias Winding Diode Forward Voltage Drop
KP	0.72				Ripple to Peak Current Ratio (0.3 < KRP < 1.0 : 1.0< KDP<6.0)

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PROTECTION FEATURES					
LINE SENSING					V pin functionality
VUV_STARTUP			101	Volts	Minimum DC Bus Voltage at which the power supply will start-up
VOV_SHUTDOWN			490	Volts	Typical DC Bus Voltage at which power supply will shut-down (Max)
RLS			4.4	M-ohms	Use two standard, 2.2 M-Ohm, 5% resistors in series for line sense functionality.
OUTPUT OVERVOLTAGE					
VZ			16	Volts	Zener Diode rated voltage for Output Overvoltage shutdown protection
RZ			5.1	k-ohms	Output OVP resistor. For latching shutdown use 20 ohm resistor instead
OVERLOAD POWER LIMITING					X pin functionality
Overload Current Ratio at VMAX			1.2		Enter the desired margin to current limit at VMAX. A value of 1.2 indicates that the current limit should be 20% higher than peak primary current at VMAX
Overload Current Ratio at VMIN		*Info*	1.38		Your margin to current limit at low line is high. Reduce KI to 0.48 (if possible).
ILIMIT_EXT_VMIN			0.93	A	Peak primary Current at VMIN
ILIMIT_EXT_VMAX			0.81	A	Peak Primary Current at VMAX
RIL			11.38	k-ohms	Current limit/Power Limiting resistor.
RPL			N/A	M-ohms	Resistor not required. Use RIL resistor only
ENTER TRANSFORMER CORE/CONSTRUCTION VARIABLES					
Core Type	**EF25**		EF25		Core Type
Core		*EF25*		*P/N:*	PC40EF25-Z
Bobbin		*EF25_BOBBIN*		*P/N:*	*
AE			0.518	cm^2	Core Effective Cross Sectional Area
LE			5.78	cm	Core Effective Path Length
AL			2000	nH/T^2	Ungapped Core Effective Inductance
BW			15.6	mm	Bobbin Physical Winding Width
M	0.00			mm	Safety Margin Width (Half the Primary to Secondary Creepage Distance)
L	2.00				Number of Primary Layers
NS	5		5		Number of Secondary Turns
DC INPUT VOLTAGE PARAMETERS					
VMIN			107	Volts	Minimum DC Input Voltage
VMAX			375	Volts	Maximum DC Input Voltage
CURRENT WAVEFORM SHAPE PARAMETERS					
DMAX			0.53		Maximum Duty Cycle (calculated at PO_PEAK)
IAVG			0.32	Amps	Average Primary Current (calculated at average output power)

IP			0.93	Amps	Peak Primary Current (calculated at Peak output power)
IR			0.67	Amps	Primary Ripple Current (calculated at average output power)
IRMS			0.45	Amps	Primary RMS Current (calculated at average output power)
TRANSFORMER PRIMARY DESIGN PARAMETERS					
LP			677	uHenries	Primary Inductance
LP Tolerance	5		5		Tolerance of Primary Inductance
NP			100		Primary Winding Number of Turns
NB			9		Bias Winding Number of Turns
ALG			68	nH/T^2	Gapped Core Effective Inductance
BM			1211	Gauss	Maximum Flux Density at PO, VMIN (BM<3000)
BP			2059	Gauss	Peak Flux Density (BP<4200) at ILIMITMAX and LP_MAX. Note: Recommended values for adapters and external power supplies <=3600 Gauss
BAC			436	Gauss	AC Flux Density for Core Loss Curves (0.5 X Peak to Peak)
ur			1776		Relative Permeability of Ungapped Core
LG			0.93	mm	Gap Length (Lg > 0.1 mm)
BWE			31.2	mm	Effective Bobbin Width
OD			0.31	mm	Maximum Primary Wire Diameter including insulation
INS			0.05	mm	Estimated Total Insulation Thickness (= 2 * film thickness)
DIA			0.26	mm	Bare conductor diameter
AWG			30	AWG	Primary Wire Gauge (Rounded to next smaller standard AWG value)
CM			102	Cmils	Bare conductor effective area in circular mils
CMA			224	Cmils/Amp	Primary Winding Current Capacity (200 < CMA < 500)
Primary Current Density (J)			8.97	Amps/mm^2	Primary Winding Current density (3.8 < J < 9.75)
TRANSFORMER SECONDARY DESIGN PARAMETERS (SINGLE OUTPUT EQUIVALENT)					
Lumped parameters					
ISP			18.54	Amps	Peak Secondary Current
ISRMS			8.54	Amps	Secondary RMS Current
IO_PEAK			5.40	Amps	Secondary Peak Output Current
IO			5.40	Amps	Average Power Supply Output Current
IRIPPLE			6.62	Amps	Output Capacitor RMS Ripple Current
CMS			1708	Cmils	Secondary Bare Conductor minimum circular mils
AWGS			17	AWG	Secondary Wire Gauge (Rounded up to next larger standard AWG value)
DIAS			1.15	mm	Secondary Minimum Bare Conductor Diameter

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ODS			3.12	mm	Secondary Maximum Outside Diameter for Triple Insulated Wire
INSS			0.98	mm	Maximum Secondary Insulation Wall Thickness
VOLTAGE STRESS PARAMETERS					
VDRAIN			593	Volts	Maximum Drain Voltage Estimate (Includes Effect of Leakage Inductance)
PIVS			24	Volts	Output Rectifier Maximum Peak Inverse Voltage
PIVB			42	Volts	Bias Rectifier Maximum Peak Inverse Voltage
TRANSFORMER SECONDARY DESIGN PARAMETERS (MULTIPLE OUTPUTS)					
1st output					
VO1			5	Volts	Output Voltage
IO1_AVG	2.50		2.50	Amps	Average DC Output Current
PO1_AVG			12.50	Watts	Average Output Power
VD1			0.5	Volts	Output Diode Forward Voltage Drop
NS1			5.00		Output Winding Number of Turns
ISRMS1			3.955	Amps	Output Winding RMS Current
IRIPPLE1			3.06	Amps	Output Capacitor RMS Ripple Current
PIVS1			24	Volts	Output Rectifier Maximum Peak Inverse Voltage
CMS1			791	Cmils	Output Winding Bare Conductor minimum circular mils
AWGS1			21	AWG	Wire Gauge (Rounded up to next larger standard AWG value)
DIAS1			0.73	mm	Minimum Bare Conductor Diameter
ODS1			3.12	mm	Maximum Outside Diameter for Triple Insulated Wire
2nd output					
VO2	14.50			Volts	Output Voltage
IO2_AVG	1.00			Amps	Average DC Output Current
PO2_AVG			14.50	Watts	Average Output Power
VD2	0.50		0.5	Volts	Output Diode Forward Voltage Drop
NS2			13.64		Output Winding Number of Turns
ISRMS2			1.582	Amps	Output Winding RMS Current
IRIPPLE2			1.23	Amps	Output Capacitor RMS Ripple Current
PIVS2			66	Volts	Output Rectifier Maximum Peak Inverse Voltage
CMS2			316	Cmils	Output Winding Bare Conductor minimum circular mils
AWGS2			25	AWG	Wire Gauge (Rounded up to next larger standard AWG value)
DIAS2			0.46	mm	Minimum Bare Conductor Diameter
ODS2			1.14	mm	Maximum Outside Diameter for Triple Insulated Wire
3rd output					
VO3				Volts	Output Voltage

IO3_AVG				Amps	Average DC Output Current
PO3_AVG			0.00	Watts	Average Output Power
VD3			0.7	Volts	Output Diode Forward Voltage Drop
NS3			0.64		Output Winding Number of Turns
ISRMS3			0.000	Amps	Output Winding RMS Current
IRIPPLE3			0.00	Amps	Output Capacitor RMS Ripple Current
PIVS3			2	Volts	Output Rectifier Maximum Peak Inverse Voltage
CMS3			0	Cmils	Output Winding Bare Conductor minimum circular mils
AWGS3			N/A	AWG	Wire Gauge (Rounded up to next larger standard AWG value)
DIAS3			N/A	mm	Minimum Bare Conductor Diameter
ODS3			N/A	mm	Maximum Outside Diameter for Triple Insulated Wire
Total Continuous Output Power			27	Watts	Total Continuous Output Power
Negative Output			N/A		If negative output exists enter Output number; eg: If VO2 is negative output, enter 2

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9 Performance Data

All measurements performed at room temperature. Unless otherwise specified, all testing performed with a line frequency of 50 Hz except for 90 VAC and 115 VAC where 60 Hz was used.

9.1 Full Load Efficiency

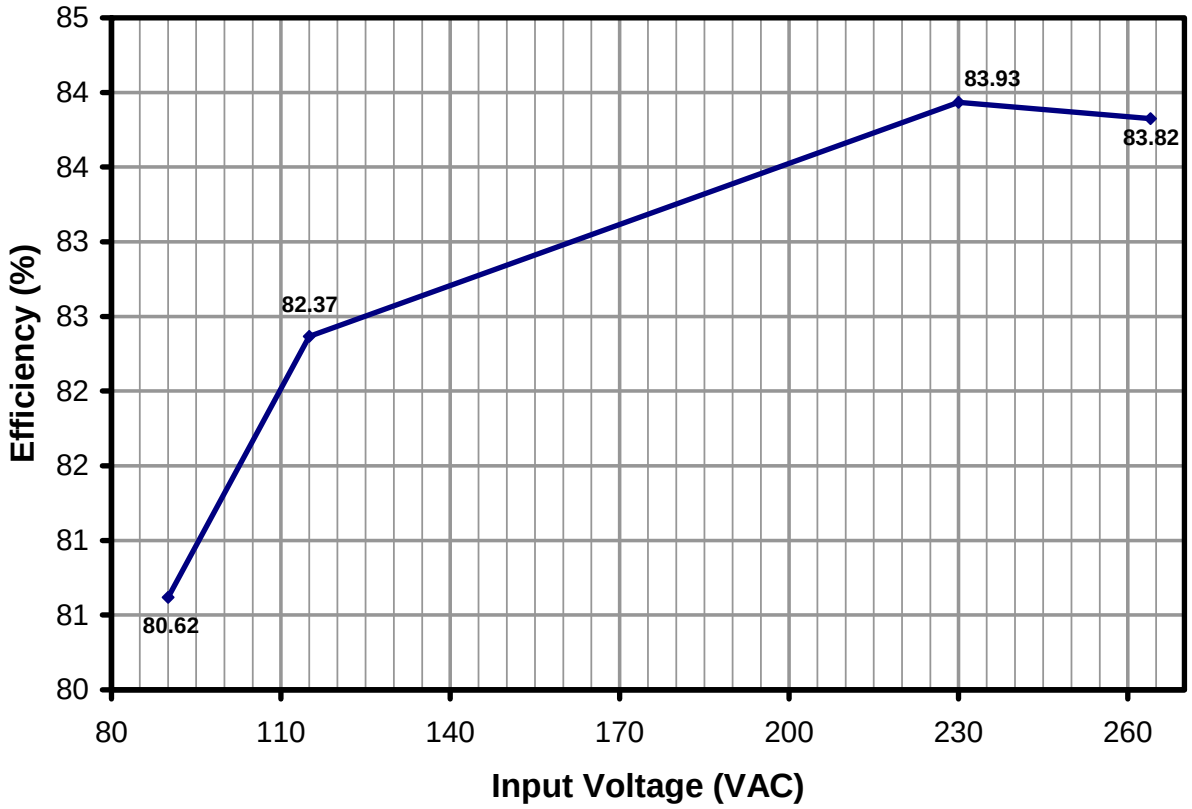


Figure 6 – Efficiency vs. Input Voltage, 60 Hz, Full Load, Room Temperature.

9.2 Input Power with 2.6 mA, 3 mA and 4 mA Load at 5 V Output

Measured with 14.5 V output unloaded.

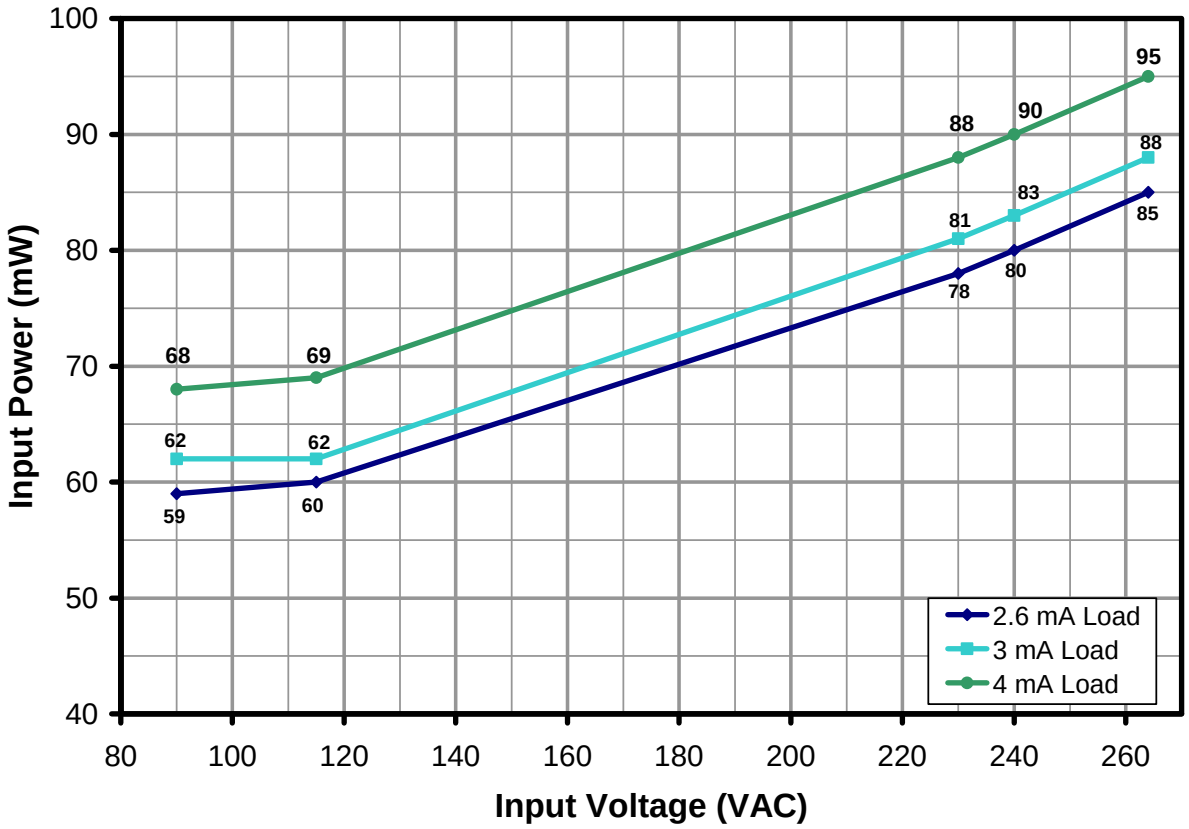


Figure 7 – Input Power with 2.6 mA, 3 mA and 4 mA. Load at 5 V. Output vs. Line Voltage and Temperature.

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9.3 No-load Input Power

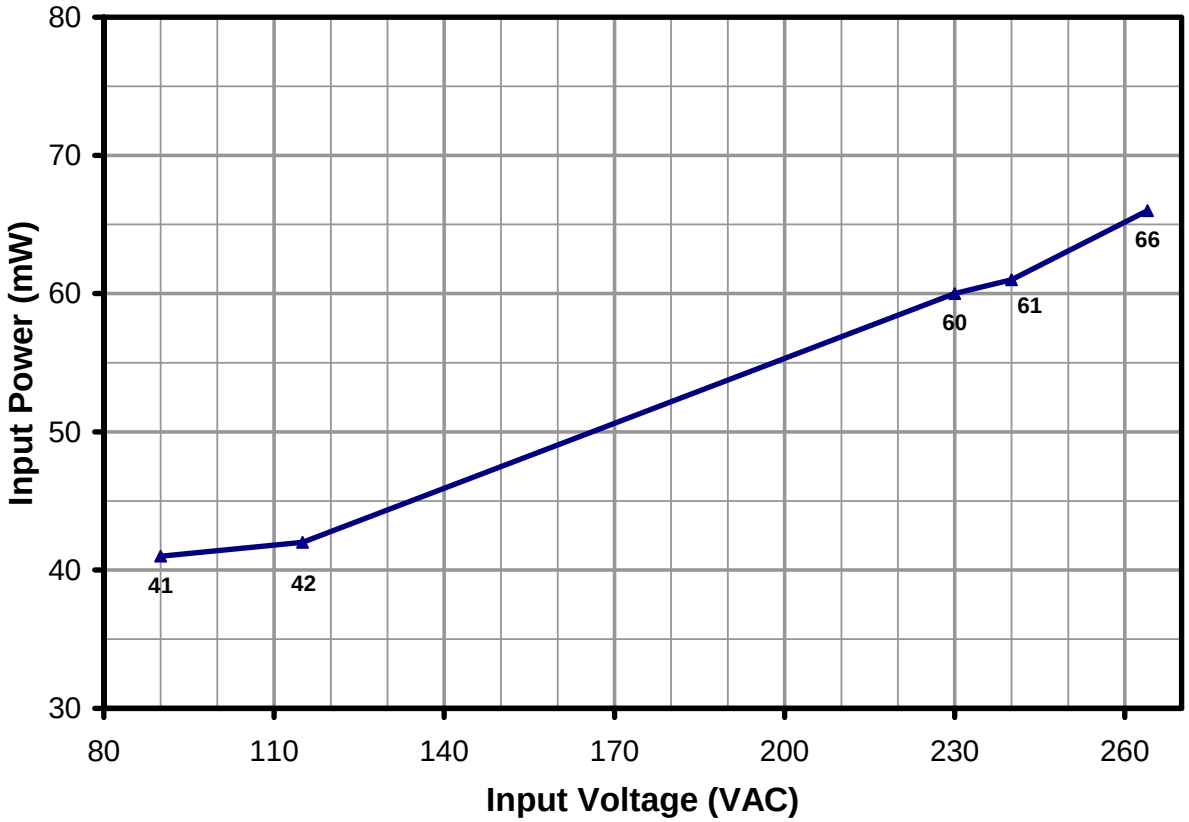


Figure 8 – No-load Input Power vs. Line Voltage.

9.4 Regulation

9.4.1 Load

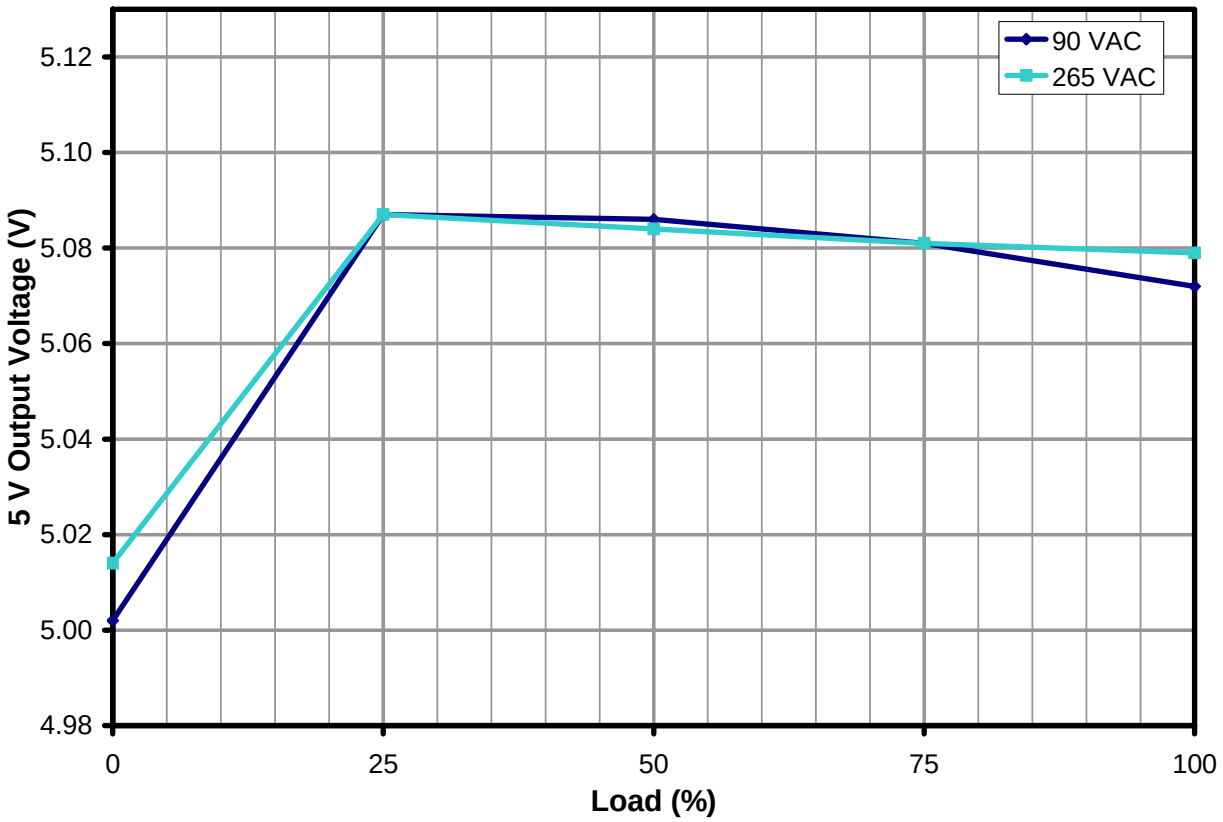


Figure 9 – 5 V Output Load Regulation, Room Temperature.

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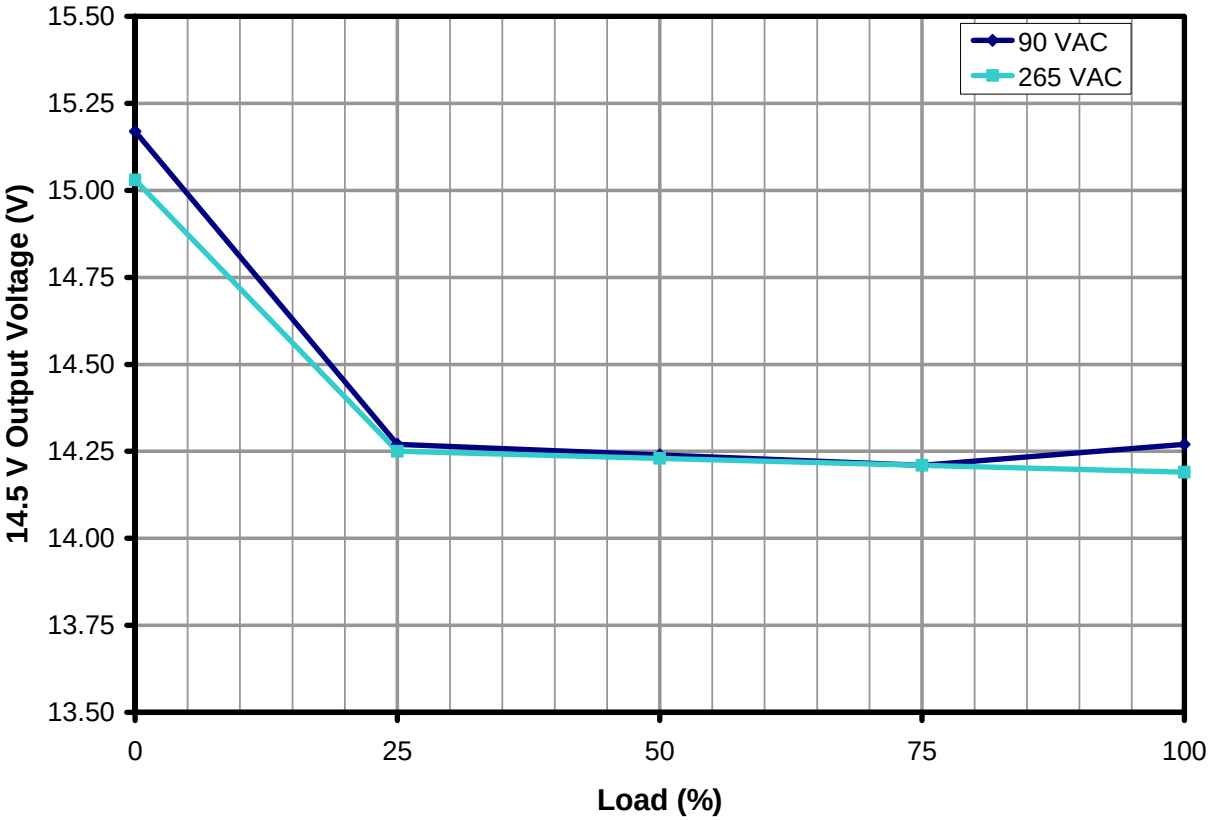


Figure 10 – 14.5 V Output Load Regulation, Room Temperature.

9.4.2 Line

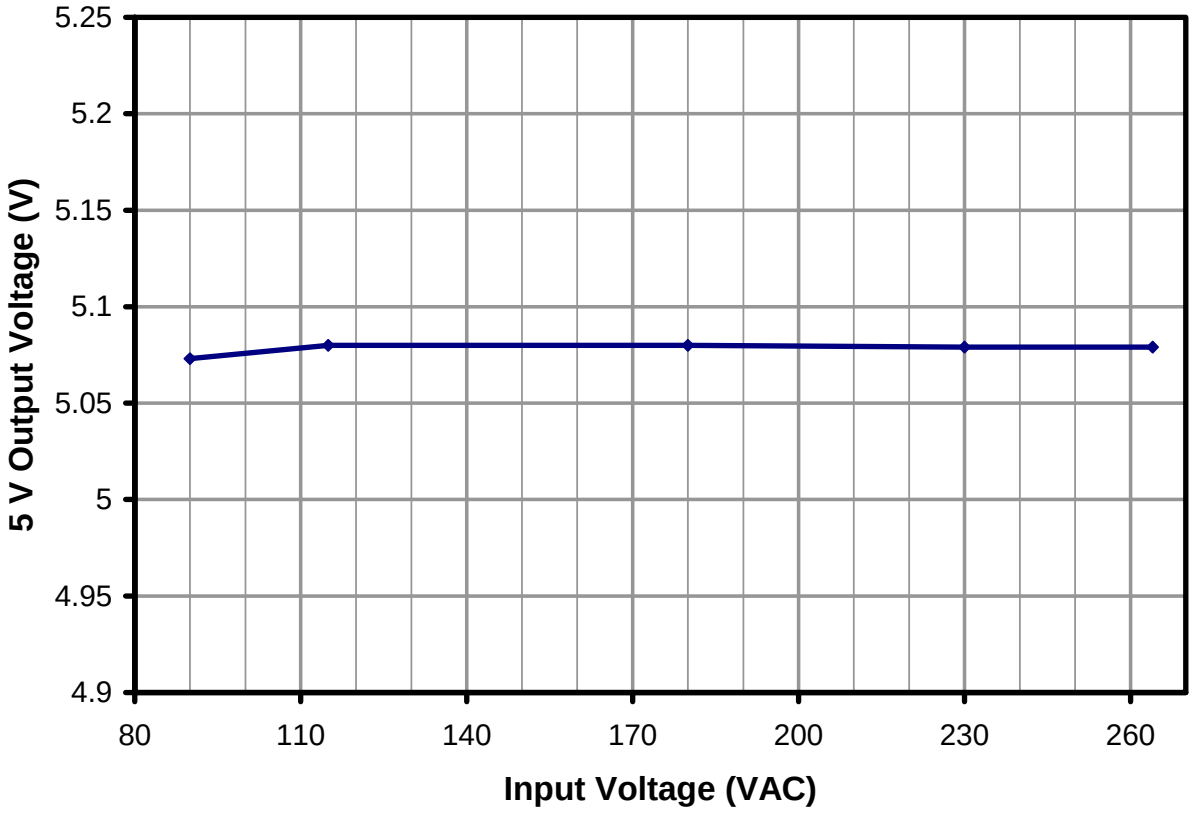


Figure 11 – 5 V Output Line Regulation, Room Temperature, Full Load.

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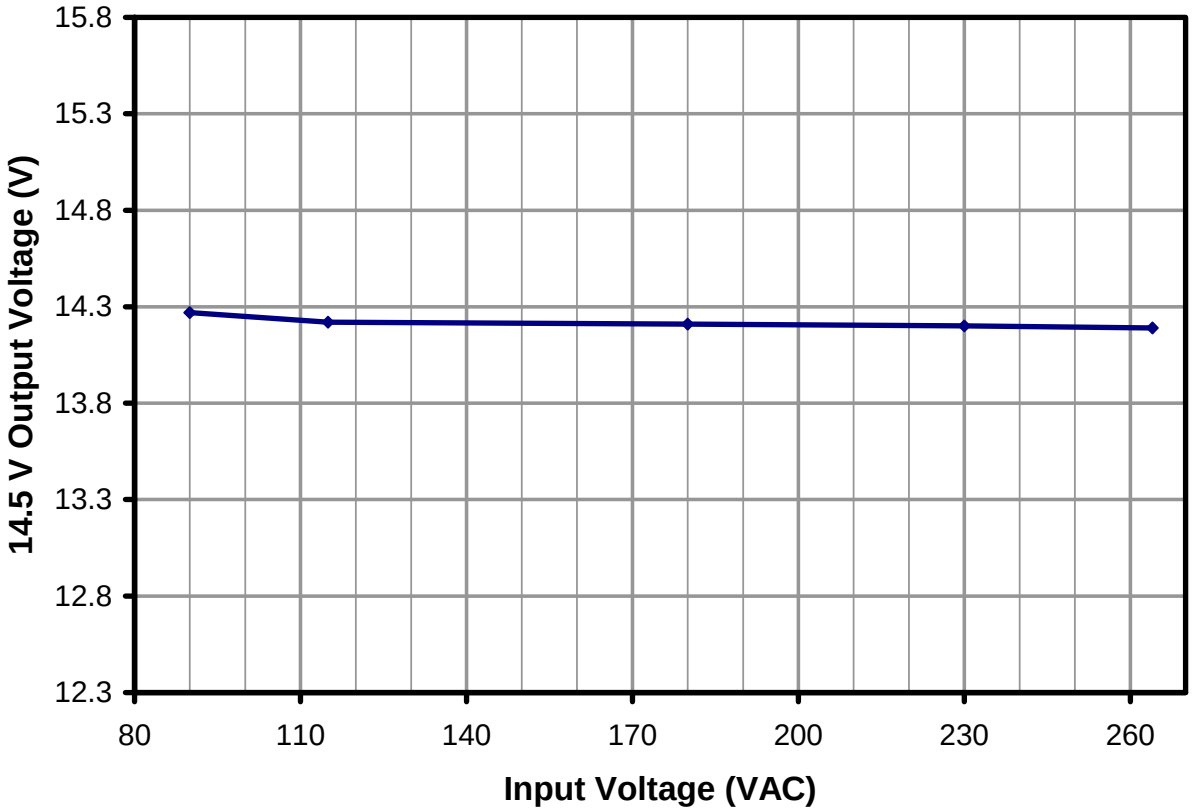


Figure 12 – 14.5 V Output Line Regulation, Room Temperature, Full Load.

9.4.3 Cross Regulation

	90 VAC		265 VAC	
	5 V OUT (V)	**14.5 V OUT (V)**	**5 V OUT (V)**	**14.5 V OUT (V)**
14.5 V / 1 A, 5 V / 2.5 A	5.07	14.27	5.08	14.19
14.5 V / 0 A, 5 V / 0 A	5.00	15.17	5.01	15.03
14.5 V / 0.1 A, 5 V / 2.5 A	4.96	15.47	4.96	15.50
14.5 V / 1 A, 5 V / 0.1 A	5.18	13.29	5.19	13.13

10 Thermal Performance

The unit was running for two hours to thermally stabilize prior to the measurement. The unit was loaded at maximum load of 27 W at room temperature on the bench open frame.

Note the tracking of the temperatures of D8 and D9 in bottom right hand corner of the thermal image indicating good current sharing.

Item	Temperature (°C)
	90 VAC / 60 Hz
Ambient	25
Common Mode Choke (L1)	61
Bridge (D10)	60
Transformer (T1) Core	56
Transformer Winding (T1)	64
***PI Device* (U1)**	55
Rectifier for 5V (D8)	67
Rectifier for 14.5V (D7)	59
Thermistor (RT1)	75

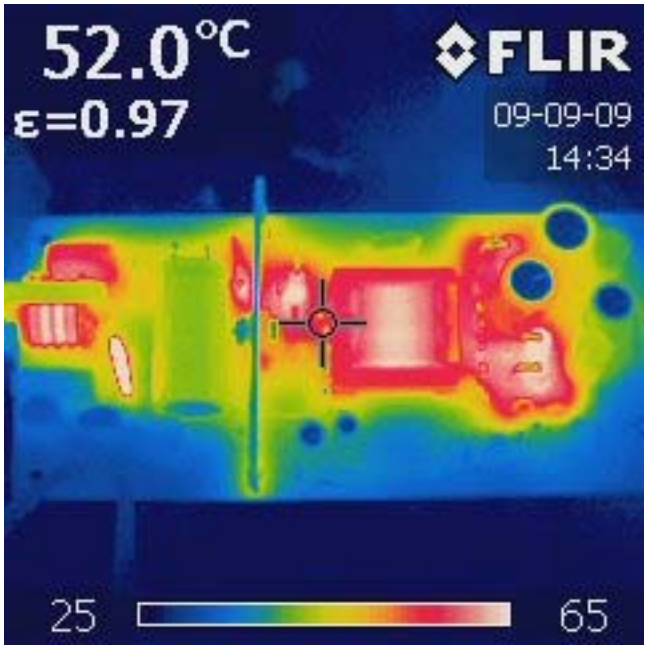


Figure 13 – Infra-Red Image of the Component Side after Two Hours Operation Full Load, 90 VAC, 60 Hz and Room Temperature Open Frame.

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11 Waveforms

11.1 Drain Voltage and Current, Normal Operation

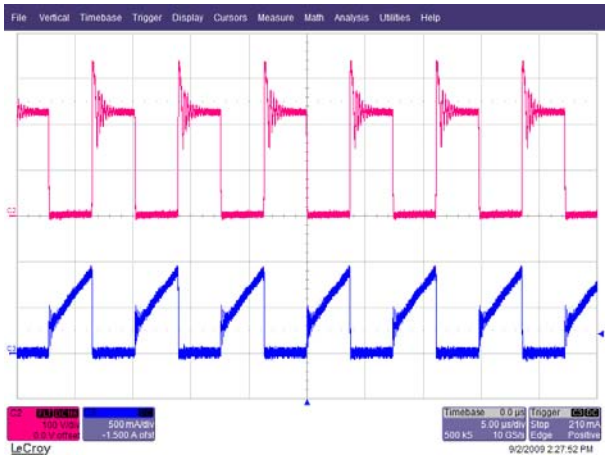


Figure 14 – 90 VAC, Full Load.
Upper: V_{DRAIN}, 100 V / div.
Lower: I_{DRAIN}, 0.5 A, 5 µs / div.

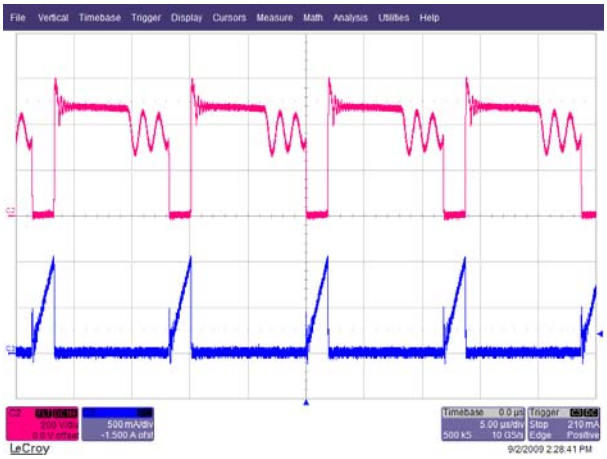


Figure 15 – 265 VAC, Full Load.
Upper: V_{DRAIN}, 200 V / div.
Lower: I_{DRAIN}, 0.5 A, 5 µs / div.

11.2 Output Voltage Start-up Profile



Figure 16 – Start-up Profile, 90 VAC.
Upper: $V_{5\,V}$, 2 V / div.
Lower: $V_{14.5\,V}$, 5 V, 20 ms / div.



Figure 17 – Start-up Profile, 265 VAC.
Upper: $V_{5\,V}$, 2 V / div.
Lower: $V_{14.5\,V}$, 5 V, 20 ms / div.

11.3 Drain Voltage and Current Start-up Profile

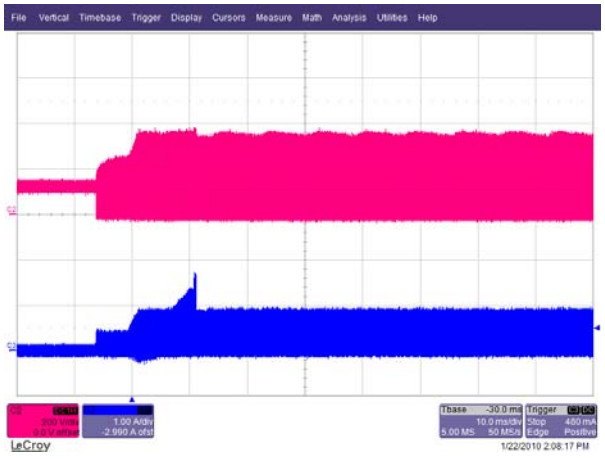


Figure 18 – 90 VAC Input and Full Load.
Upper: V_{DRAIN}, 200 V / div.
Lower: I_{DRAIN}, 0.5 A ,10 ms / div.



Figure 19 – 265 VAC Input and Full Load.
Upper: V_{DRAIN}, 200 V / div.
Lower: I_{DRAIN}, 0.5 A ,10 ms / div.

11.4 Load Transient Response (75% to 100% Load Step)

In the figures shown below, signal averaging was used to better enable viewing the load transient response. The oscilloscope was triggered using the load current step as a trigger source. Since the output switching and line frequency occur essentially at random with respect to the load transient, contributions to the output ripple from these sources will average out, leaving the contribution only from the load step response.

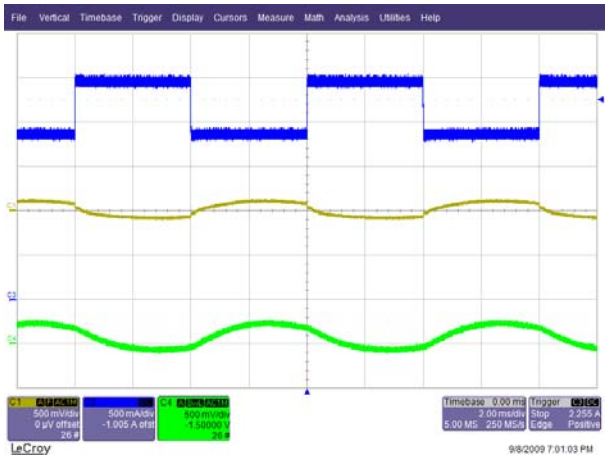


Figure 20 – Transient Response, 90 VAC,
75-100-75% Load Step at 5 V Output.
Top: Output Current, 500 mA / div.
Middle: 5 V Output, 500 mV / div.
Bottom: 14.5 V Output.
500 mV, 2 ms / div.

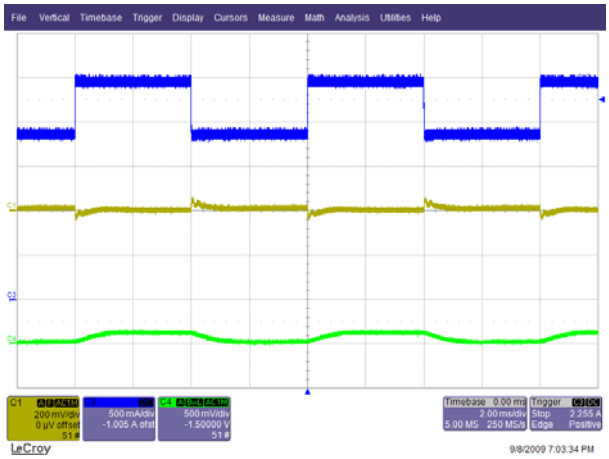


Figure 21 – Transient Response, 265 VAC,
75-100-75% Load Step at 5 V Output.
Top: Output Current, 500 mA / div.
Middle: 5 V Output, 200 mV / div.
Bottom: 14.5 V Output.
500 mV, 2 ms / div.

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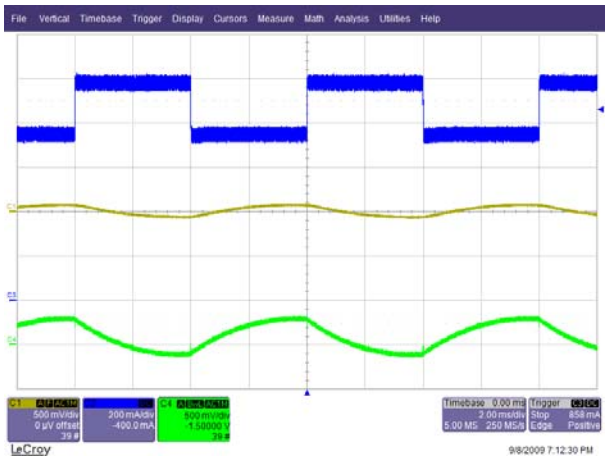


Figure 22 – Transient Response, 90 VAC, 75-100-75% Load Step at 14.5 V Output.
Top: Output Current, 200 mA / div.
Middle: 5 V Output, 500 mV / div.
Bottom: 14.5 V Output,
500 mV, 2 ms / div.

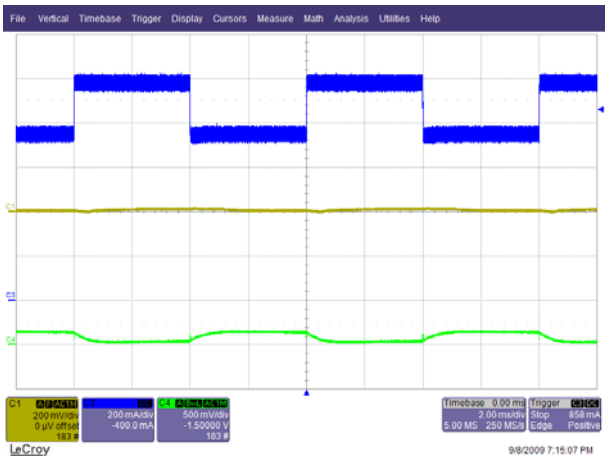


Figure 23 – Transient Response, 265 VAC, 75-100-75% Load Step at 14.5 V Output.
Top: Output Current, 200 mA / div.
Middle: 5 V Output, 200 mV / div.
Bottom: 14.5 V Output.
500 mV, 2 ms / div.

11.5 Output Overvoltage Protection

An output over voltage condition was simulated by shorting LED of the optocoupler (U2), with the output fully loaded. The resultant output oscillograph (below) shows the operation of the primary side OV shutdown via VR2 into the V pin.

The behavior can be changed from non-latching to latching by reducing the value of R6 to 22 Ohms.



Figure 24 – Output Overvoltage Protection, 90 VAC.
Top: 14.5 V Output Voltage, 5 V / div.
Bottom: 5 V Output Voltage, 2 V / div., 500 ms / div.

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11.6 Output Ripple Measurements

11.6.1 Ripple Measurement Technique

For DC output ripple measurements, a modified oscilloscope test probe must be utilized in order to reduce spurious signals due to pickup. Details of the probe modification are provided in the figures below.

The 4987BA probe adapter is affixed with two capacitors tied in parallel across the probe tip. The capacitors include one (1) 0.1 μF/50 V ceramic type and one (1) 1.0 μF/50 V aluminum electrolytic. The aluminum electrolytic type capacitor is polarized, so proper polarity across DC outputs must be maintained (see below).

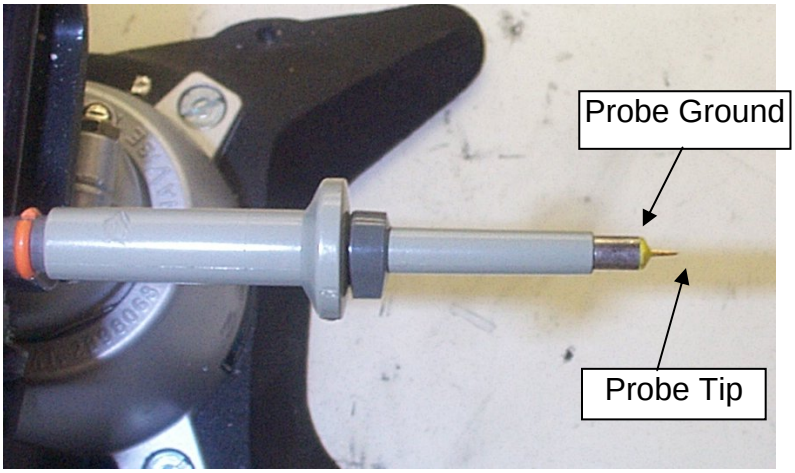


Figure 25 – Oscilloscope Probe Prepared for Ripple Measurement. (End Cap and Ground Lead Removed)

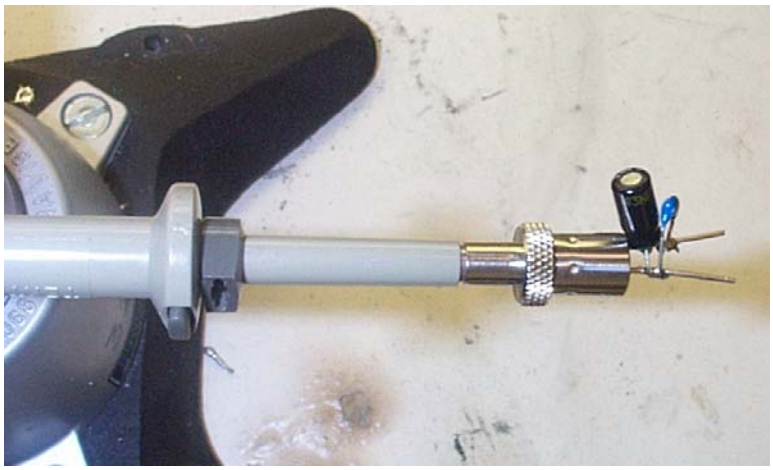


Figure 26 – Oscilloscope Probe with Probe Master (**www.probemaster.com**) 4987A BNC Adapter.
(Modified with wires for ripple measurement, and two parallel decoupling capacitors added)

11.6.2 Measurement Results

Note: Measurements of ripple were made with the V pin of U1 connected to SOURCE pin. This was done to correctly simulate the performance of the final version of U1 which has an optimized V pin characteristic compared to the device used on this board.

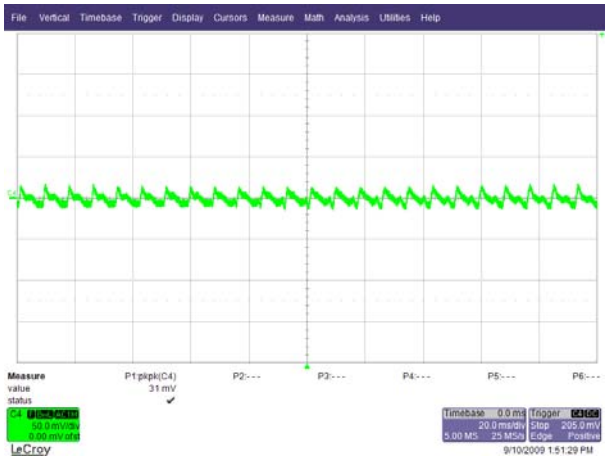


Figure 27 – 5 V Output Ripple [31 mV_{P-P}],
90 VAC, 60 Hz, Full Load.
50 mV, 20 ms / div.

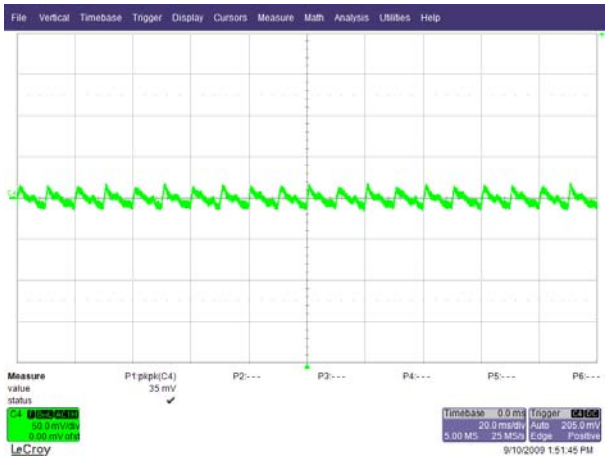


Figure 28 – 5 V Output Ripple [35 mV_{P-P}],
115 VAC, 50 Hz, Full Load.
50 mV, 20 ms / div.



Figure 29 – 5 V Output Ripple [10.9 mV_{P-P}],
265 VAC, 50 Hz, Full Load.
10 mV, 5 ms / div.

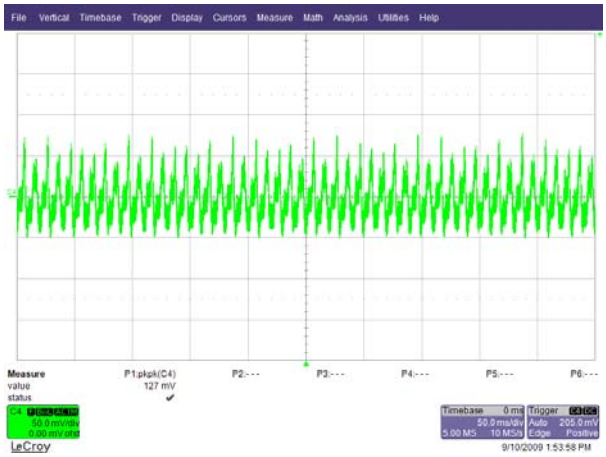


Figure 30 – 14.5 V Output Ripple, [127 mV_{P-P}]
90 VAC, 50 Hz, Full Load.
50 mV, 50 ms / div.

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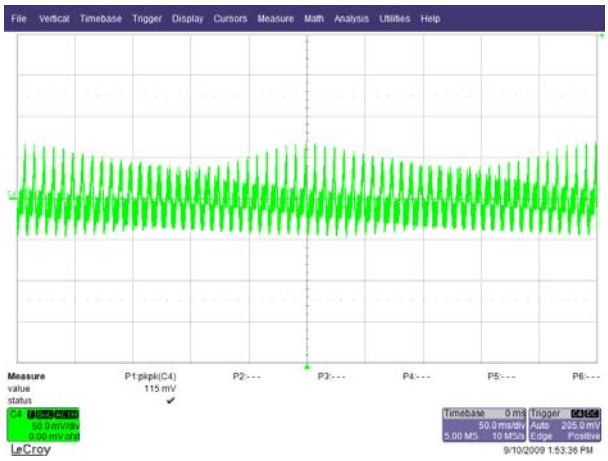


Figure 31 – 14.5 V Output Ripple, [115 mV_{P-P}]
115 VAC, 60 Hz, Full Load.
50 mV, 50 ms / div

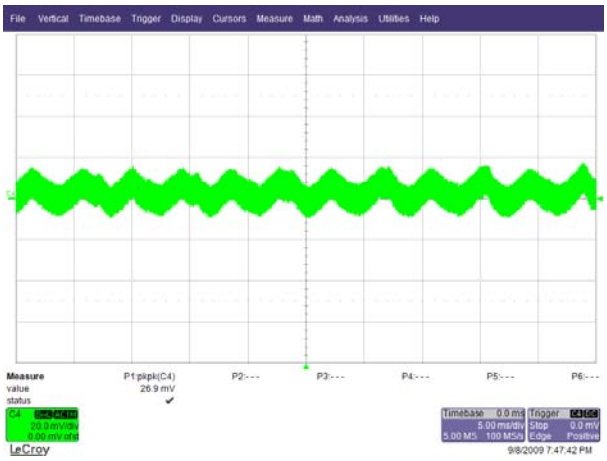


Figure 32 – 14.5 V Output Ripple, [26.9 mV_{P-P}]
265 VAC, 50 Hz, Full Load.
20 mV, 5 ms / div.

12 Conducted EMI

Conducted EMI was measured with the board mounted above a grounded metal plate, both with the output return floating and connected to earth ground. The results below represent worst case results..

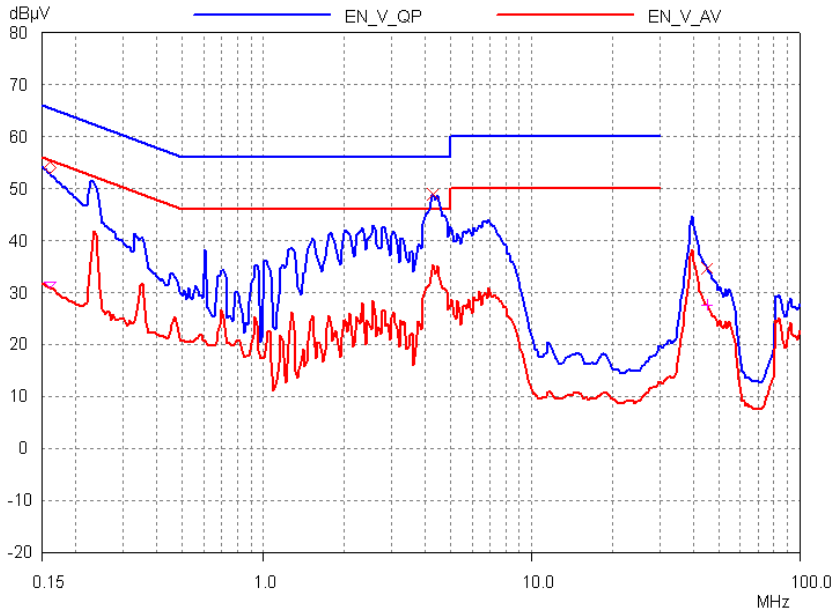


Figure 33 – Conducted EMI, Full Load, 115 VAC, 60 Hz.

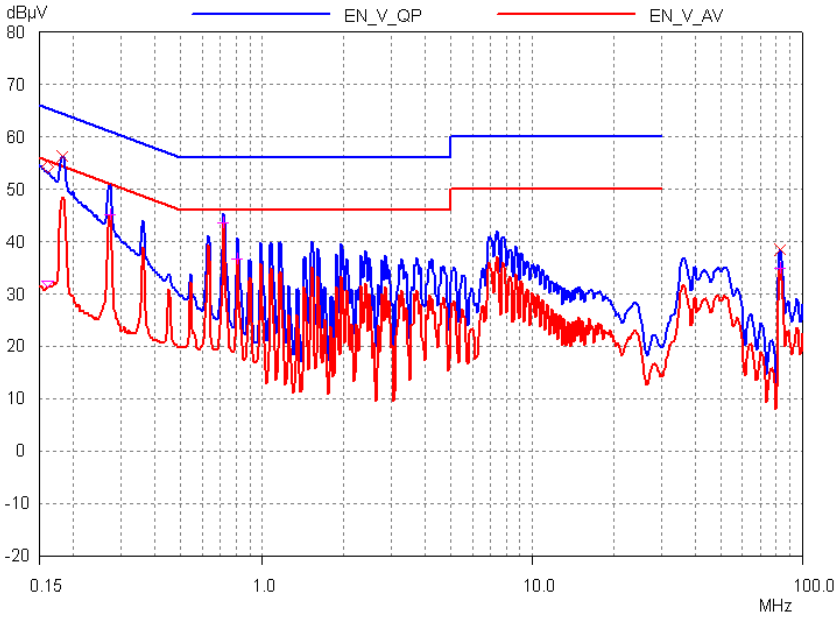


Figure 34 – Conducted EMI, Full Load, 230 VAC, 60 Hz.

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13 Revision History

Date	Author	Revision	Description & changes	Reviewed
08-Jan-10	JY	1.0	First Release	ME, PV

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