NCP1402

200 mA, PFM Step-Up Micropower Switching Regulator

The NCP1402 series are monolithic micropower step−up DC to DC converter that are specially designed for powering portable equipment from one or two cell battery packs.These devices are designed to startup with a cell voltage of 0.8 V and operate down to less than 0.3 V. With only three external components, this series allow a simple means to implement highly efficient converters that are capable of up to 200 mA of output current at V_{in} = 2.0 V, V_{OUT} = 3.0 V.

Each device consists of an on−chip PFM (Pulse Frequency Modulation) oscillator, PFM controller, PFM comparator, soft−start, voltage reference, feedback resistors, driver, and power MOSFET switch with current limit protection. Additionally, a chip enable feature is provided to power down the converter for extended battery life.

The NCP1402 device series are available in the Thin SOT−23−5 package with five standard regulated output voltages. Additional voltages that range from 1.8 V to 5.0 V in 100 mV steps can be manufactured.

Features

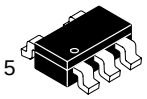
- Pb−Free Packages are Available
- Extremely Low Startup Voltage of 0.8 V
- Operation Down to Less than 0.3 V
- High Efficiency 85% (V_{in} = 2.0 V, V_{OUT} = 3.0 V, 70 mA)
- Low Operating Current of 30 μA (V_{OUT} = 1.9 V)
- Output Voltage Accuracy ± 2.5%
- Low Converter Ripple with Typical 30 mV
- Only Three External Components Are Required
- Chip Enable Power Down Capability for Extended Battery Life
- Micro Miniature Thin SOT−23−5 Packages

Typical Applications

- Cellular Telephones
- Pagers
- Personal Digital Assistants (PDA)
- Electronic Games
- Portable Audio (MP3)
- Camcorders
- Digital Cameras
- Handheld Instruments

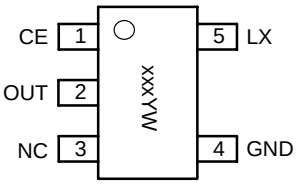
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http://onsemi.com



SOT23−5
(TSOP−5, SC59−5)
SN SUFFIX
CASE 483

PIN CONNECTIONS AND MARKING DIAGRAM



xxx = Marking
Y = Year
W = Work Week

(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information in the ordering information section on page 3 of this data sheet.

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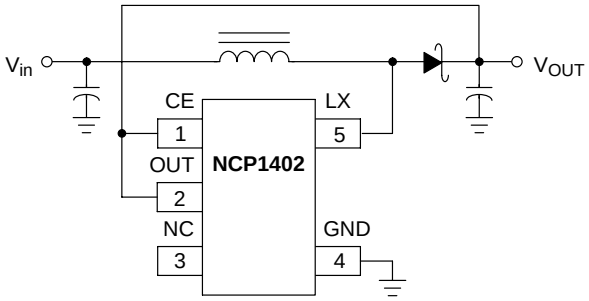


Figure 1. Typical Step−Up Converter Application

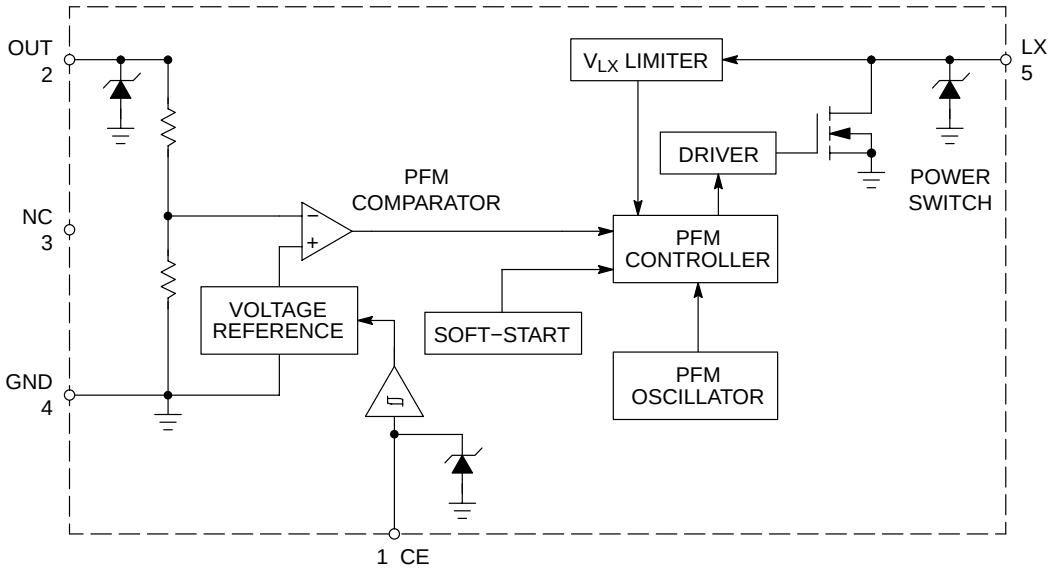


Figure 2. Representative Block Diagram

PIN FUNCTION DESCRIPTIONS

Pin #	Symbol	Pin Description
1	CE	Chip Enable pin (1) The chip is enabled if a voltage which is equal to or greater than 0.9 V is applied (2) The chip is disabled if a voltage which is less than 0.3 V is applied (3) The chip will be enabled if it is left floating
2	OUT	Output voltage monitor pin, also the power supply pin of the device
3	NC	No internal connection to this pin
4	GND	Ground pin
5	LX	External inductor connection pin to power switch drain

ORDERING INFORMATION

Device	Output Voltage	Device Marking	Package	Shipping†
NCP1402SN19T1	1.9 V	DAU	SOT23−5	3000 Units Per Reel
NCP1402SN27T1	2.7 V	DAE		
NCP1402SN30T1	3.0 V	DAF		
NCP1402SN33T1	3.3 V	DAG		
NCP1402SN33T1G	3.3 V	DAG	SOT23−5 (Pb−Free)	
NCP1402SN40T1	4.0 V	DCR	SOT23−5	
NCP1402SN50T1	5.0 V	DAH		
NCP1402SN50T1G	5.0 V	DAH	SOT23−5 (Pb−Free)	

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NOTE: The ordering information lists five standard output voltage device options. Additional device with output voltage ranging from 1.8 V to 5.0 V in 100 mV increments can be manufactured. Contact your ON Semiconductor representative for availability.

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage (Pin 2)	V_{OUT}	6.0	V
Input/Output Pins LX (Pin 5) LX Peak Sink Current	 V_{LX} I_{LX}	 −0.3 to 6.0 400	 V mA
CE (Pin 1) Input Voltage Range Input Current Range	 V_{CE} I_{CE}	 −0.3 to 6.0 −150 to 150	 V mA
Thermal Resistance, Junction−to−Air	$R_{\theta JA}$	250	°C/W
Operating Ambient Temperature Range (Note 2)	T_A	−40 to +85	°C
Operating Junction Temperature Range	T_J	−40 to +125	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

NOTES:

1. This device series contains ESD protection and exceeds the following tests:
   Human Body Model (HBM) ±2.0 kV per JEDEC standard: JESD22−A114.
   Machine Model (MM) ±200 V per JEDEC standard: JESD22−A115.
2. The maximum package power dissipation limit must not be exceeded.
$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$
3. Latchup Current Maximum Rating: ±150 mA per JEDEC standard: JESD78.
4. Moisture Sensitivity Level: MSL 1 per IPC/JEDEC standard: J−STD−020A.

ELECTRICAL CHARACTERISTICS (For all values T_A = 25°C, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OSCILLATOR					
Switch On Time (current limit not asserted)	t_{on}	3.6	5.5	7.6	μs
Switch Minimum Off Time	t_{off}	1.0	1.45	1.9	μs
Maximum Duty Cycle	D_{MAX}	70	78	85	%
Minimum Startup Voltage (I_O = 0 mA)	V_{start}	−	0.8	0.95	V
Minimum Startup Voltage Temperature Coefficient (T_A = −40°C to 85°C)	ΔV_{start}	−	−1.6	−	mV/°C
Minimum Operation Hold Voltage (I_O = 0 mA)	V_{hold}	0.3	−	−	V
Soft−Start Time (V_{OUT} > 0.8 V)	t_{SS}	0.3	2.0	−	ms
LX (PIN 5)					
Internal Switching N−Channel FET Drain Voltage	V_{LX}	−	−	6.0	V
LX Pin On−State Sink Current (V_{LX} = 0.4 V) Device Suffix:	I_{LX}				mA
19T1		110	145	−	
27T1		130	180	−	
30T1		130	190	−	
33T1		130	200	−	
40T1		130	210	−	
50T1		130	215	−	
Voltage Limit	V_{LXLIM}	0.45	0.65	0.9	V
Off−State Leakage Current (V_{LX} = 6.0 V, T_A = −40°C to 85°C)	I_{LKG}	−	0.5	1.0	μA
CE (PIN 1)					
CE Input Voltage (V_{OUT} = V_{SET} x 0.96)					V
High State, Device Enabled	$V_{CE(high)}$	0.9	−	−	
Low State, Device Disabled	$V_{CE(low)}$	−	−	0.3	
CE Input Current (Note 6)					μA
High State, Device Enabled (V_{OUT} = V_{CE} = 6.0 V)	$I_{CE(high)}$	−0.5	0	0.5	
Low State, Device Disabled (V_{OUT} = 6.0 V, V_{CE} = 0 V)	$I_{CE(low)}$	−0.5	0.15	0.5	
TOTAL DEVICE					
Output Voltage Device Suffix:	V_{OUT}				V
19T1		1.853	1.9	1.948	
27T1		2.632	2.7	2.768	
30T1		2.925	3.0	3.075	
33T1		3.218	3.3	3.383	
40T1		3.900	4.0	4.100	
50T1		4.875	5.0	5.125	
Output Voltage Temperature Coefficient (T_A = −40°C to +85°C) Device Suffix:	ΔV_{OUT}				ppm/°C
19T1		−	150	−	
27T1		−	150	−	
30T1		−	150	−	
33T1		−	150	−	
40T1		−	150	−	
50T1		−	150	−	
Operating Current 2 (V_{OUT} = V_{CE} = V_{SET} +0.5 V, Note 5)	I_{DD2}	−	13	15	μA
Off−State Current (V_{OUT} = 5.0 V, V_{CE} = 0 V, T_A = −40°C to +85°C, Note 6)	I_{OFF}	−	0.6	1.0	μA
Operating Current 1 (V_{OUT} = V_{CE} = V_{SET} x 0.96) Device Suffix:	I_{DD1}				μA
19T1		−	30	50	
27T1		−	39	60	
30T1		−	42	60	
33T1		−	45	60	
40T1		−	55	100	
50T1		−	70	100	

5. V_{SET} means setting of output voltage.
6. CE pin is integrated with an internal 10 MΩ pullup resistor.

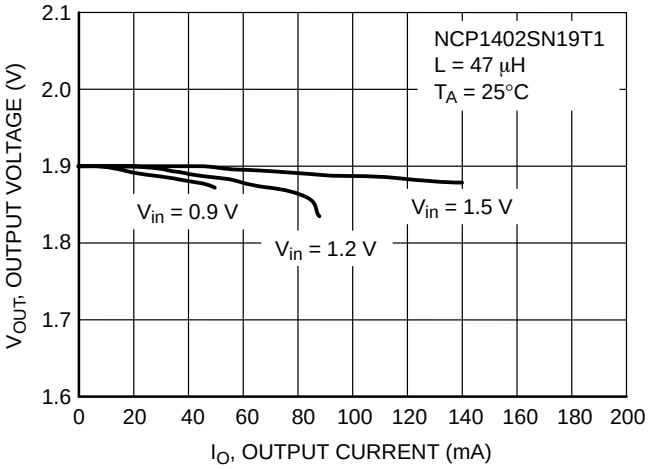


Figure 3. NCP1402SN19T1 Output Voltage vs. Output Current

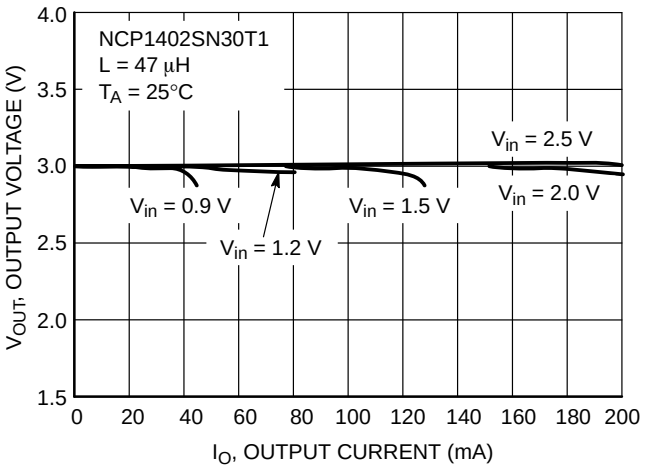


Figure 4. NCP1402SN30T1 Output Voltage vs. Output Current

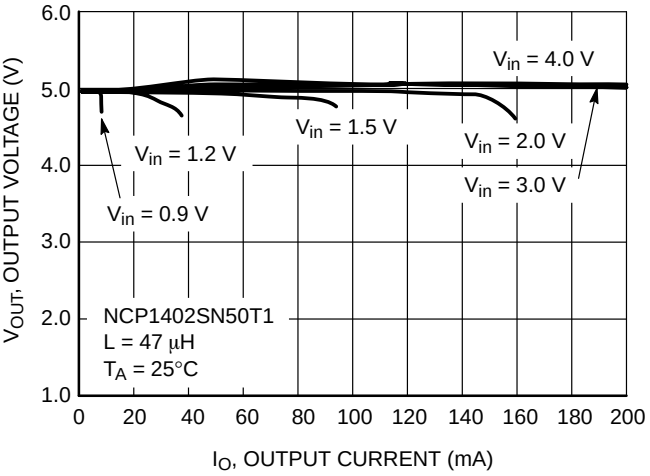


Figure 5. NCP1402SN50T1 Output Voltage vs. Output Current

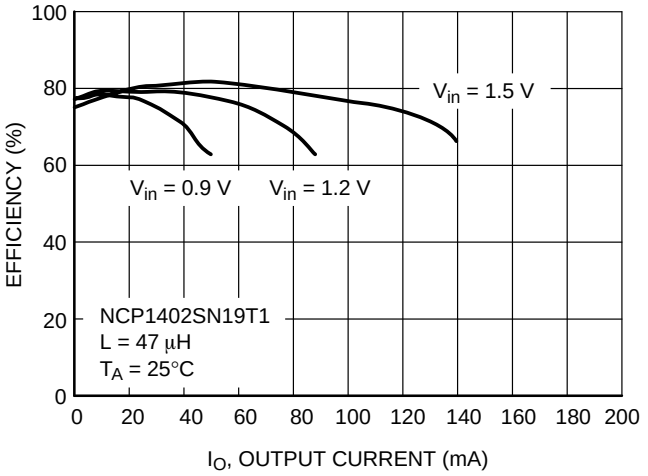


Figure 6. NCP1402SN19T1 Efficiency vs. Output Current

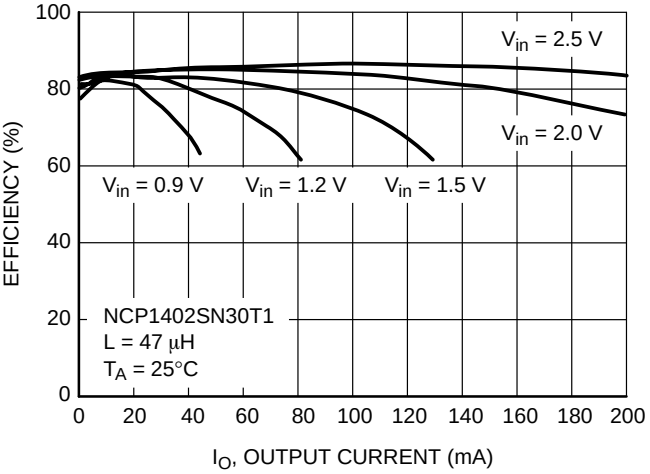


Figure 7. NCP1402SN30T1 Efficiency vs. Output Current

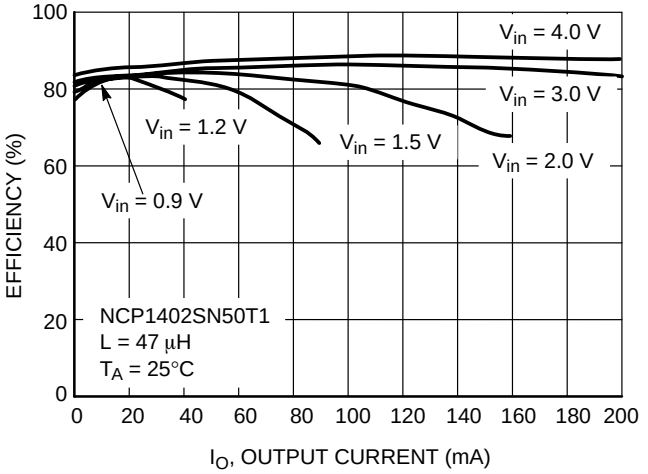


Figure 8. NCP1402SN50T1 Efficiency vs. Output Current

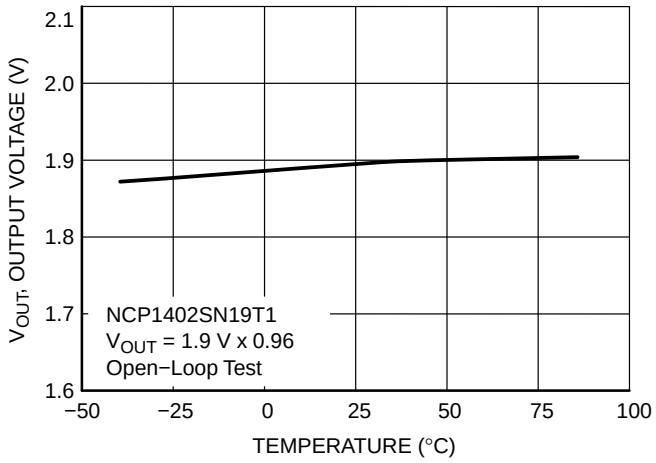


Figure 9. NCP1402SN19T1 Output Voltage vs. Temperature

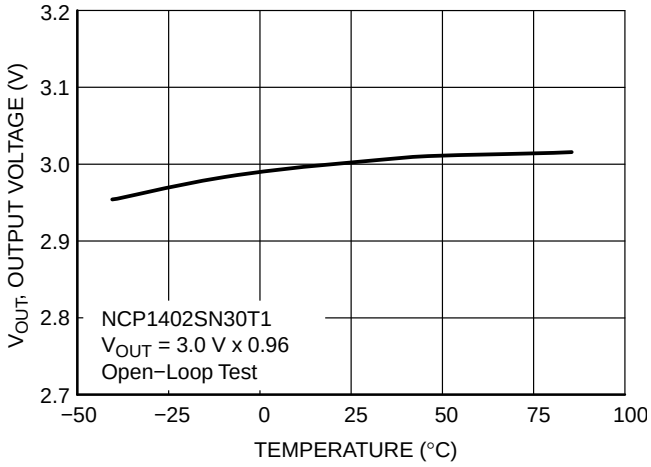


Figure 10. NCP1402SN30T1 Output Voltage vs. Temperature

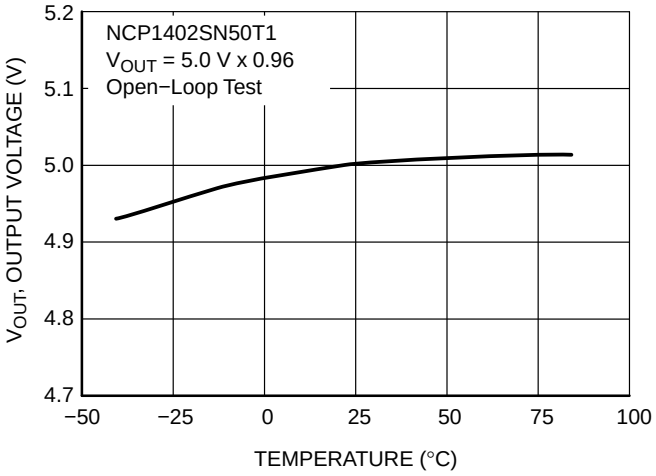


Figure 11. NCP1402SN50T1 Output Voltage vs. Temperature

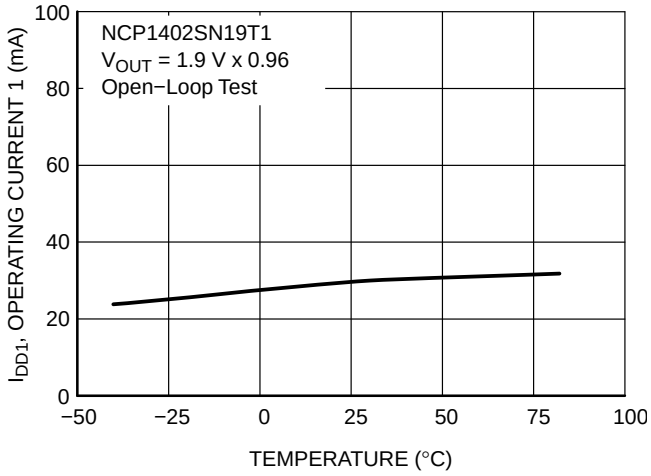


Figure 12. NCP1402SN19T1 Operating Current 1 vs. Temperature

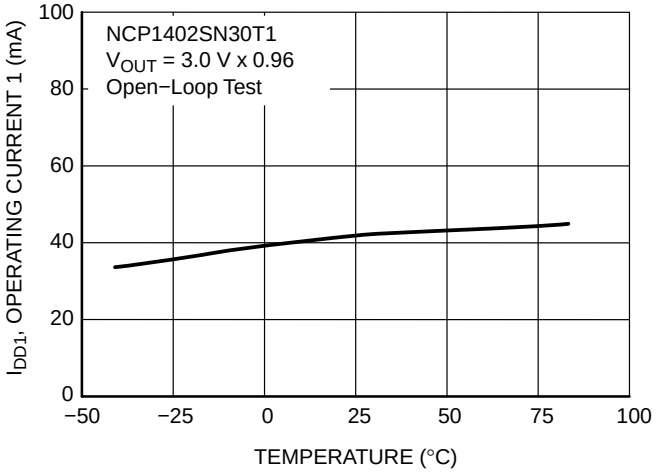


Figure 13. NCP1402SN30T1 Operating Current 1 vs. Temperature

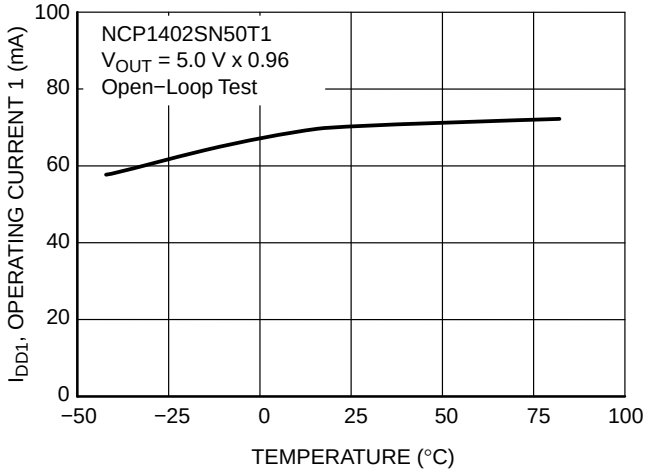


Figure 14. NCP1402SN50T1 Operating Current 1 vs. Temperature

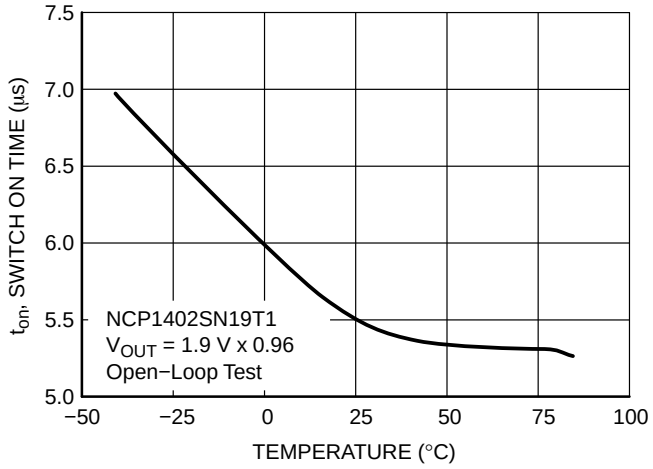


Figure 15. NCP1402SN19T1 Switch On Time vs. Temperature

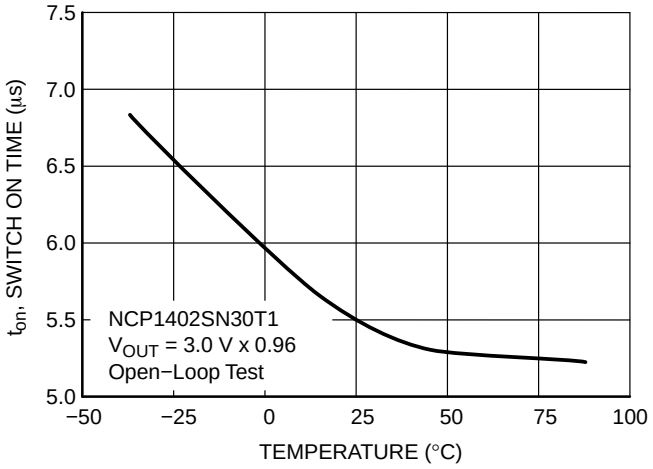


Figure 16. NCP1402SN30T1 Switch On Time vs. Temperature

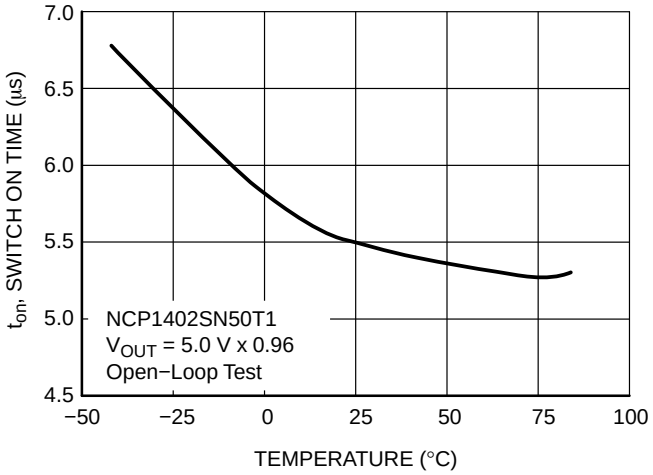


Figure 17. NCP1402SN50T1 Switch On Time vs. Temperature

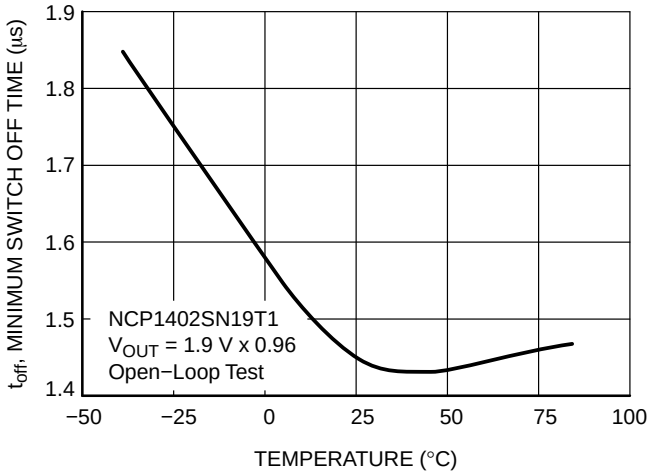


Figure 18. NCP1402SN19T1 Minimum Switch Off Time vs. Temperature

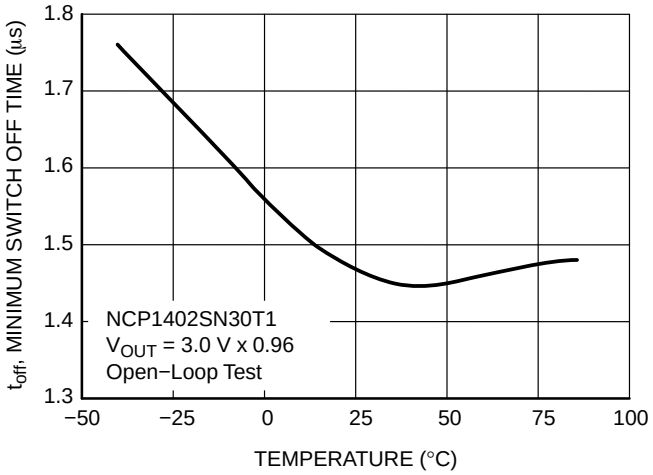


Figure 19. NCP1402SN30T1 Minimum Switch Off Time vs. Temperature

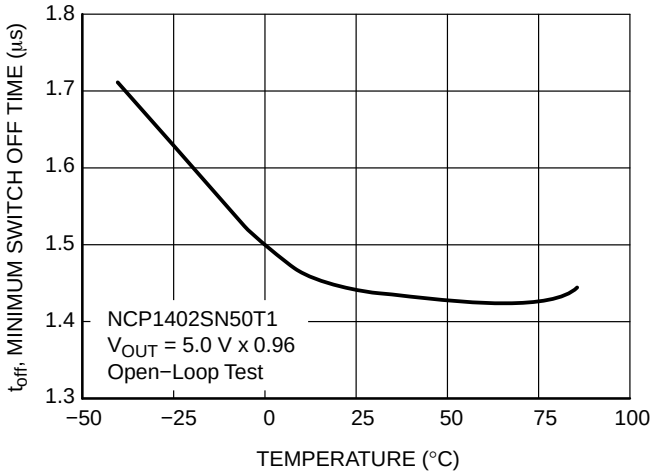


Figure 20. NCP1402SN50T1 Minimum Switch Off Time vs. Temperature

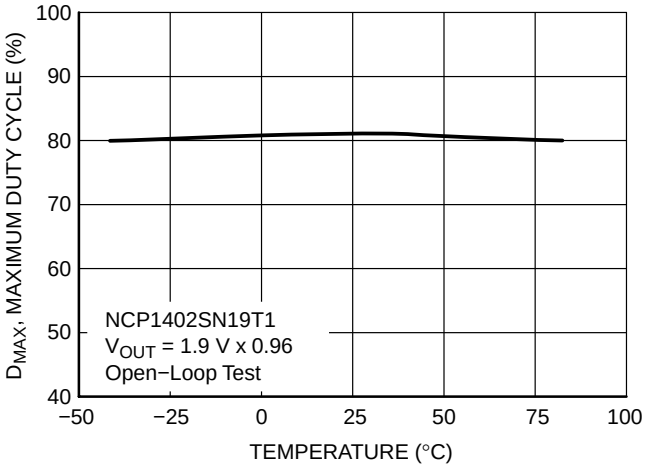


Figure 21. NCP1402SN19T1 Maximum Duty Cycle vs. Temperature

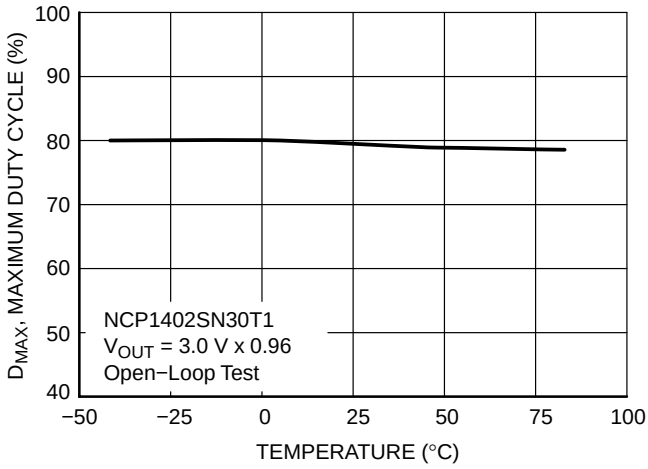


Figure 22. NCP1402SN30T1 Maximum Duty Cycle vs. Temperature

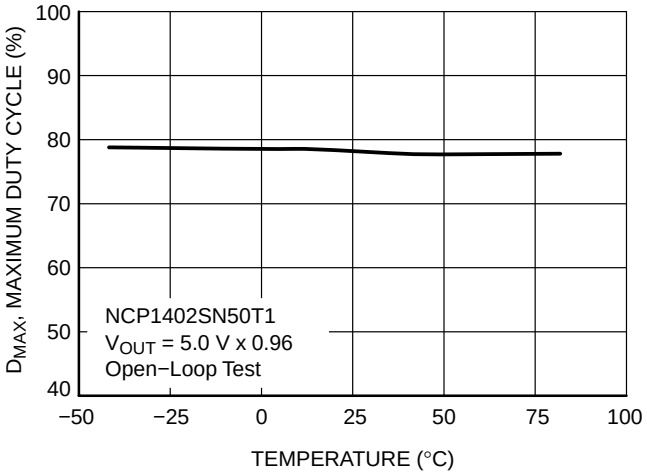


Figure 23. NCP1402SN50T1 Maximum Duty Cycle vs. Temperature

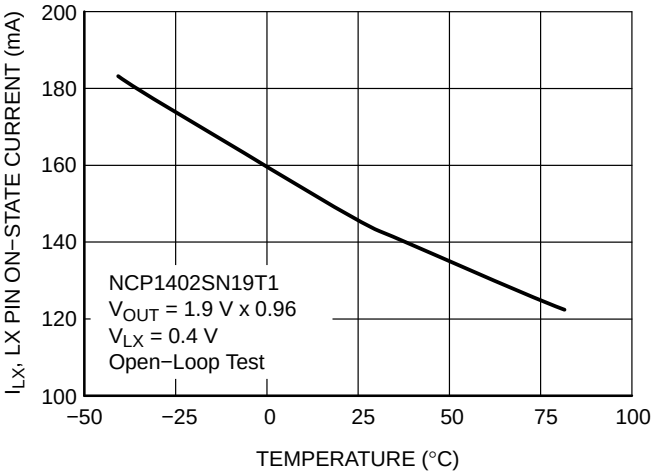


Figure 24. NCP1402SN19T1 LX Pin On−State Current vs. Temperature

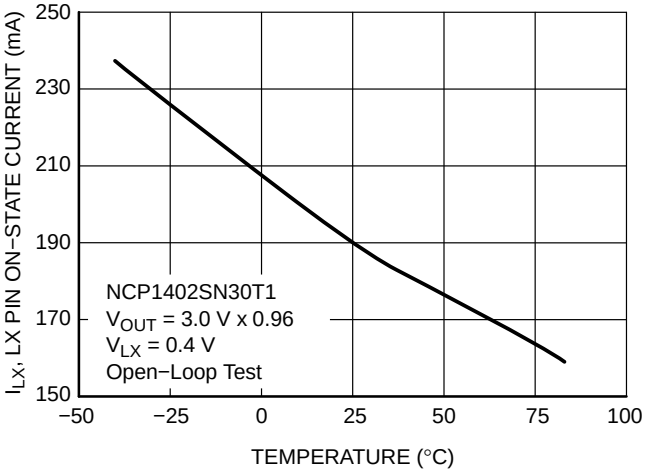


Figure 25. NCP1402SN30T1 LX Pin On−State Current vs. Temperature

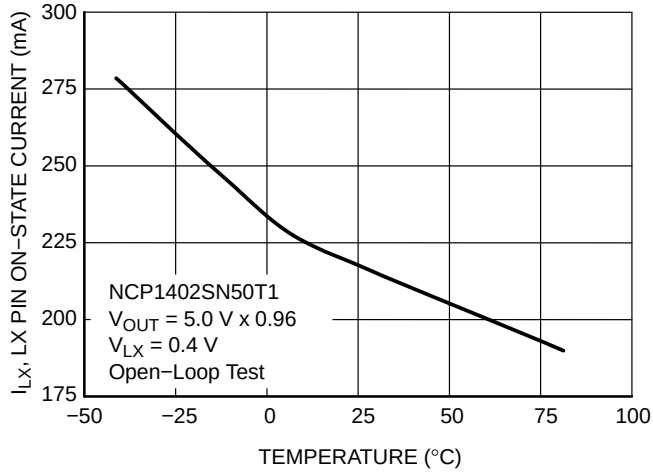


Figure 26. NCP1402SN50T1 LX Pin On−State Current vs. Temperature

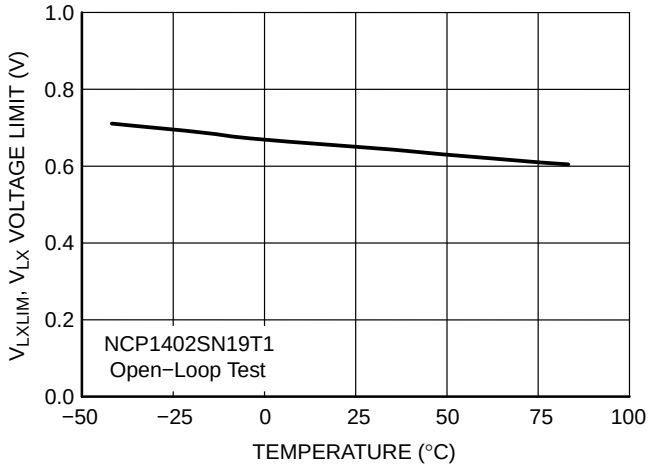


Figure 27. NCP1402SN19T1 V_{LX} Voltage Limit vs. Temperature

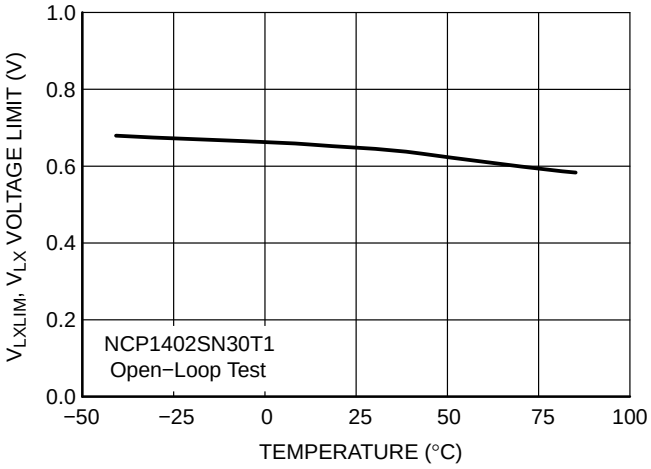


Figure 28. NCP1402SN30T1 V_{LX} Voltage Limit vs. Temperature

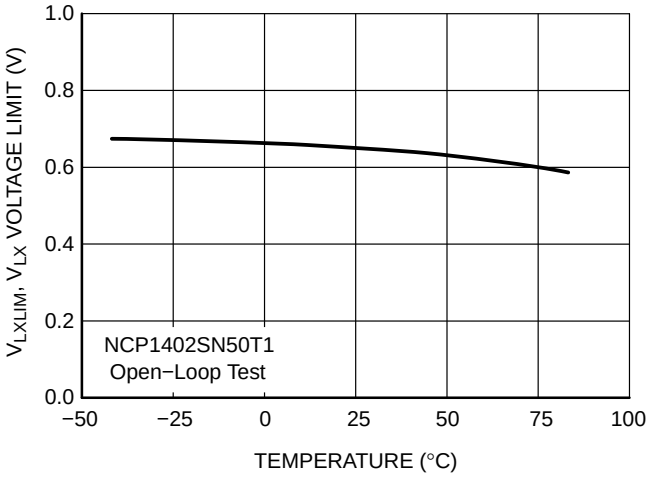


Figure 29. NCP1402SN50T1 V_{LX} Voltage Limit vs. Temperature

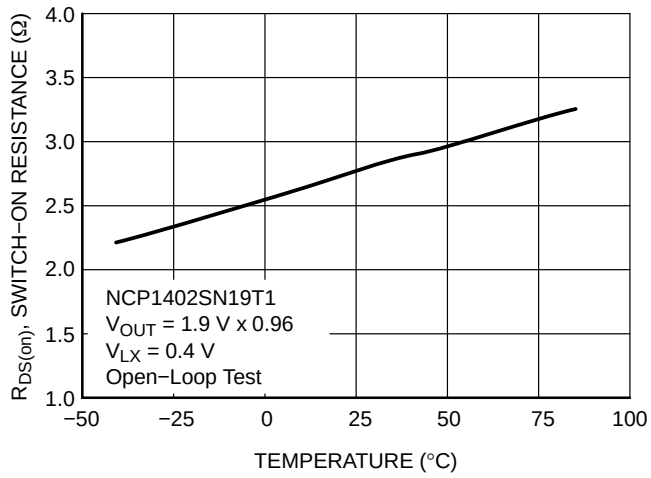


Figure 30. NCP1402SN19T1 Switch−on Resistance vs. Temperature

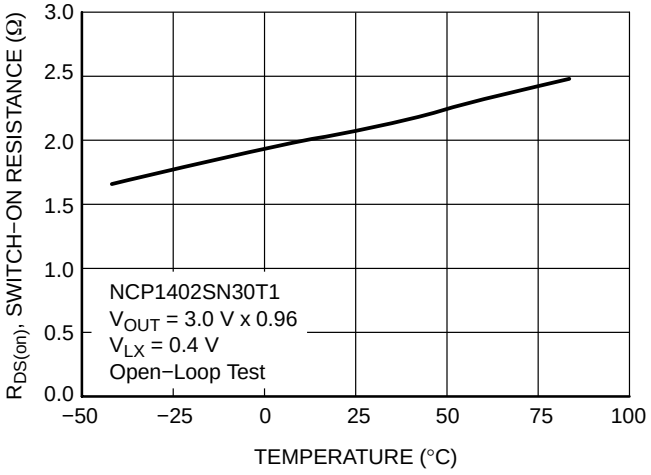


Figure 31. NCP1402SN30T1 Switch−on Resistance vs. Temperature

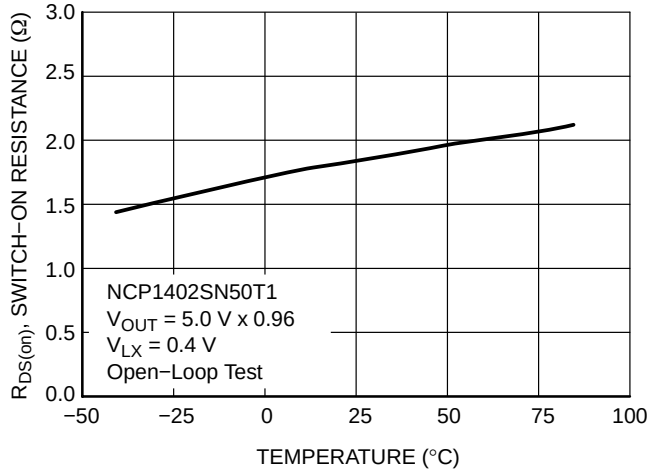


Figure 32. NCP1402SN50T1 Switch−on Resistance vs. Temperature

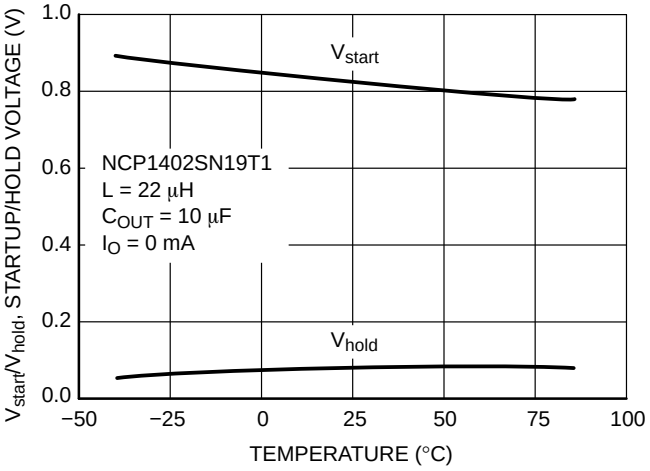


Figure 33. NCP1402SN19T1 Startup/Hold Voltage vs. Temperature

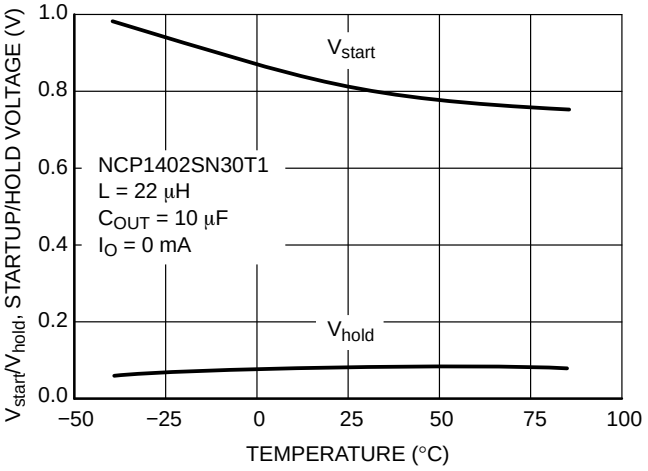


Figure 34. NCP1402SN30T1 Startup/Hold Voltage vs. Temperature

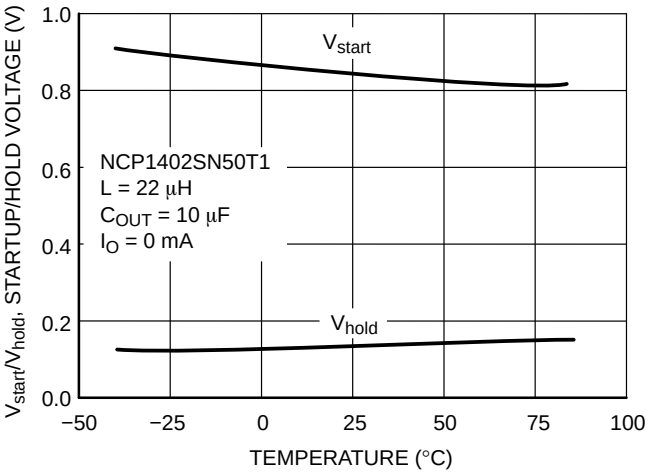


Figure 35. NCP1402SN50T1 Startup/Hold Voltage vs. Temperature

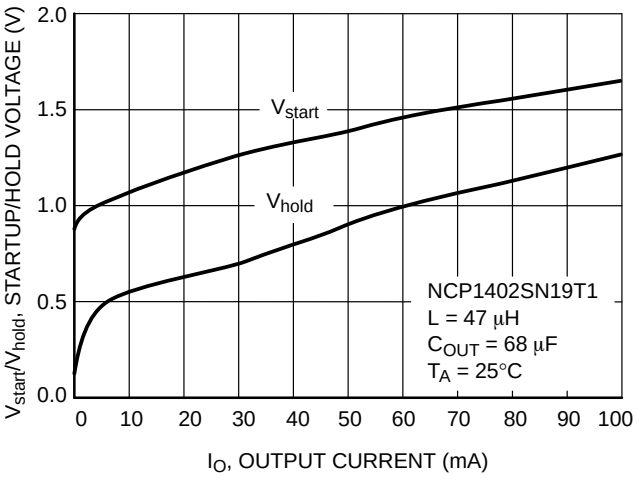


Figure 36. NCP1402SN19T1 Startup/Hold Voltage vs. Output Current

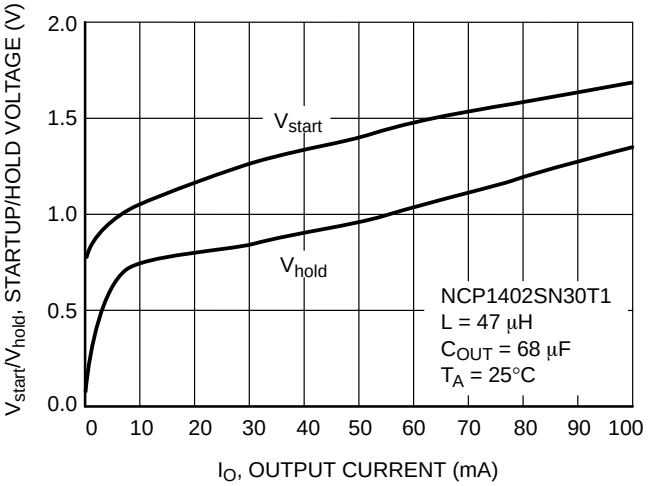


Figure 37. NCP1402SN30T1 Startup/Hold Voltage vs. Output Current

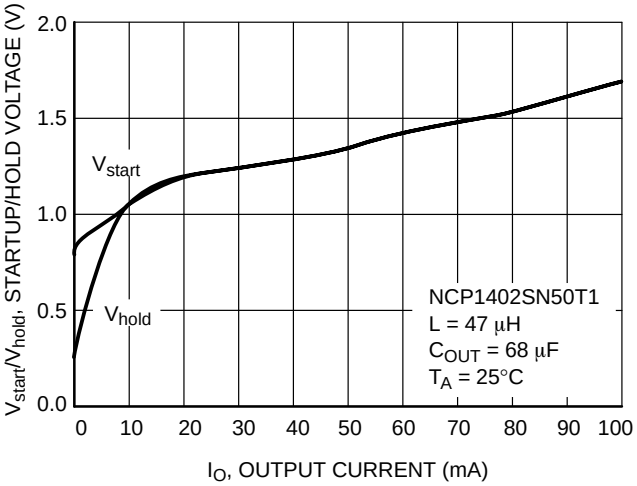
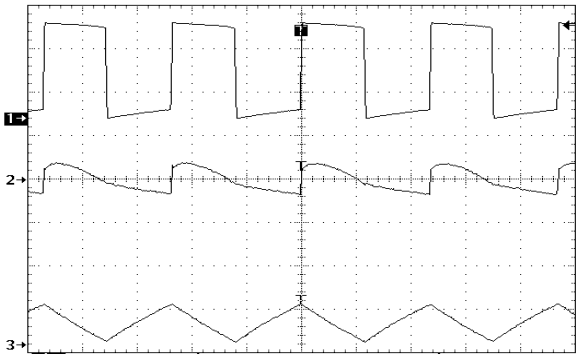


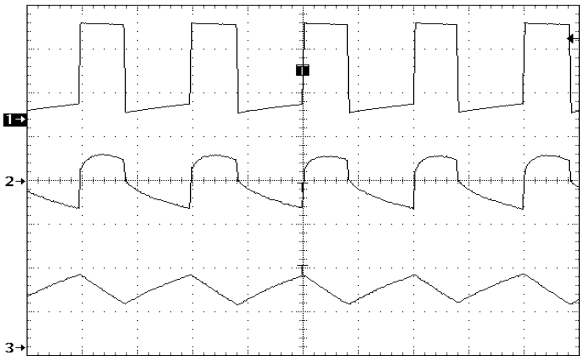
Figure 38. NCP1402SN50T1 Startup/Hold Voltage vs. Output Current



5 μs/div

V_{OUT} = 1.9 V, V_{in} = 1.2 V, I_O = 30 mA, L = 47 μH, C_{OUT} = 68 μF
1. V_{LX}, 1.0 V/div
2. V_{OUT}, 20 mV/div, AC coupled
3. I_L, 100 mA/div

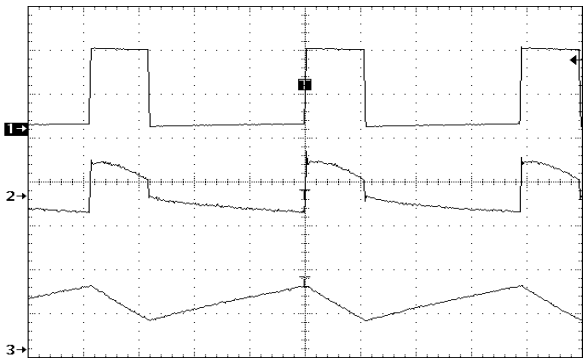
Figure 39. NCP1402SN19T1 Operating Waveforms (Medium Load)



5 μs/div

V_{OUT} = 1.9 V, V_{in} = 1.2 V, I_O = 70 mA, L = 47 μH, C_{OUT} = 68 μF
1. V_{LX}, 1.0 V/div
2. V_{OUT}, 20 mV/div, AC coupled
3. I_L, 100 mA/div

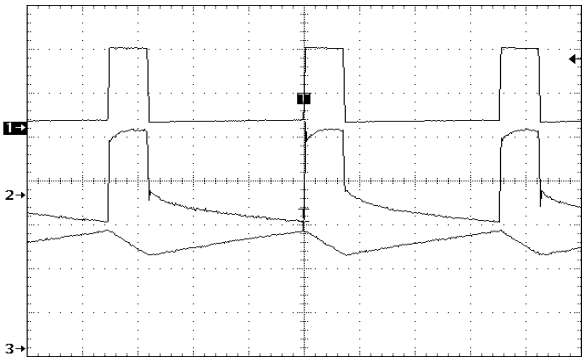
Figure 40. NCP1402SN19T1 Operating Waveforms (Heavy Load)



2 μs/div

V_{OUT} = 3.0 V, V_{in} = 1.2 V, I_O = 30 mA, L = 47 μH, C_{OUT} = 68 μF
1. V_{LX}, 2.0 V/div
2. V_{OUT}, 20 mV/div, AC coupled
3. I_L, 100 mA/div

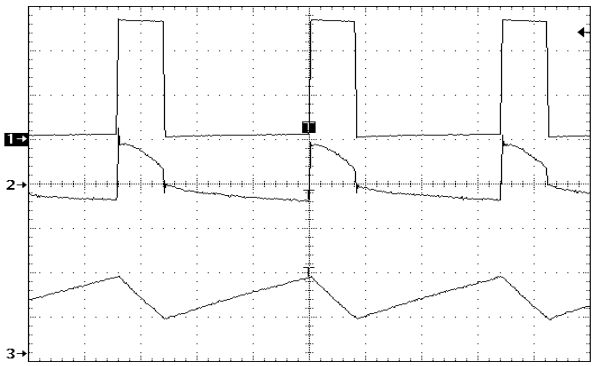
Figure 41. NCP1402SN30T1 Operating Waveforms (Medium Load)



2 μs/div

V_{OUT} = 3.0 V, V_{in} = 1.2 V, I_O = 70 mA, L = 47 μH, C_{OUT} = 68 μF
1. V_{LX}, 2.0 V/div
2. V_{OUT}, 20 mV/div, AC coupled
3. I_L, 100 mA/div

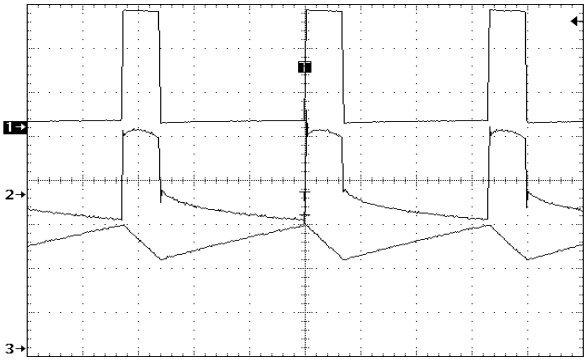
Figure 42. NCP1402SN30T1 Operating Waveforms (Heavy Load)



2 μs/div

V_{OUT} = 5.0 V, V_{in} = 1.5 V, I_O = 30 mA, L = 47 μH, C_{OUT} = 68 μF
1. V_{LX}, 2.0 V/div
2. V_{OUT}, 20 mV/div, AC coupled
3. I_L, 100 mA/div

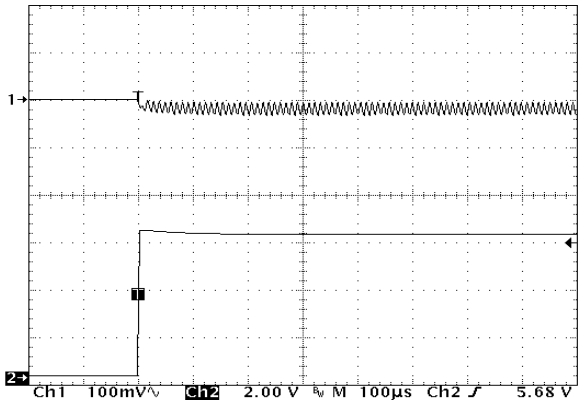
Figure 43. NCP1402SN50T1 Operating Waveforms (Medium Load)



2 μs/div

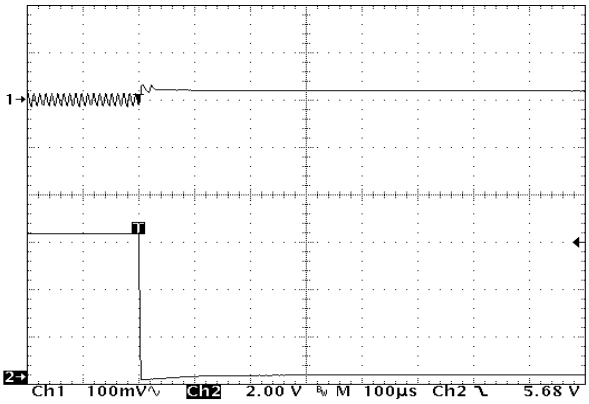
V_{OUT} = 5.0 V, V_{in} = 1.5 V, I_O = 60 mA, L = 47 μH, C_{OUT} = 68 μF
1. V_{LX}, 2.0 V/div
2. V_{OUT}, 20 mV/div, AC coupled
3. I_L, 100 mA/div

Figure 44. NCP1402SN50T1 Operating Waveforms (Heavy Load)



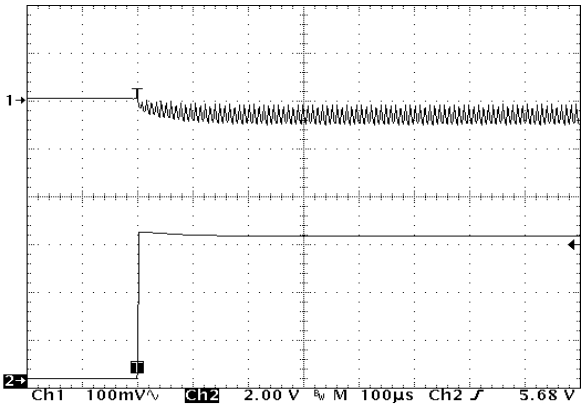
V_{in} = 1.2 V, L = 47 µH, C_{OUT} = 68 µF
1. V_{OUT} = 1.9 V (AC coupled), 100 mV/div
2. I_O = 0.1 mA to 80 mA

Figure 45. NCP1402SN19T1 Load Transient Response



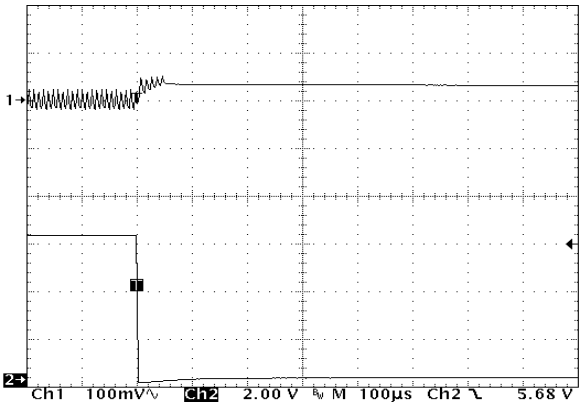
V_{in} = 1.2 V, L = 47 µH, C_{OUT} = 68 µF
1. V_{OUT} = 1.9 V (AC coupled), 100 mV/div
2. I_O = 80 mA to 0.1 mA

Figure 46. NCP1402SN19T1 Load Transient Response



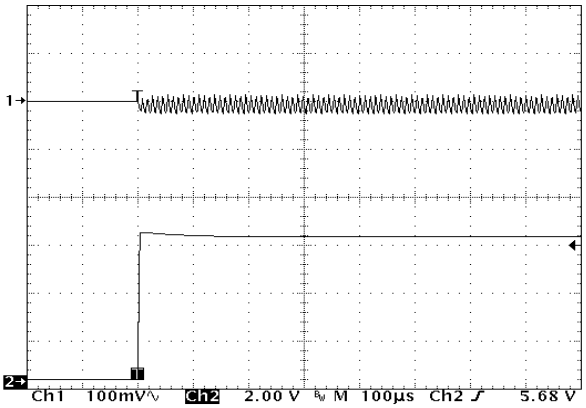
V_{in} = 1.5 V, L = 47 µH, C_{OUT} = 68 µF
1. V_{OUT} = 3.0 V (AC coupled), 100 mV/div
2. I_O = 0.1 mA to 80 mA

Figure 47. NCP1402SN30T1 Load Transient Response



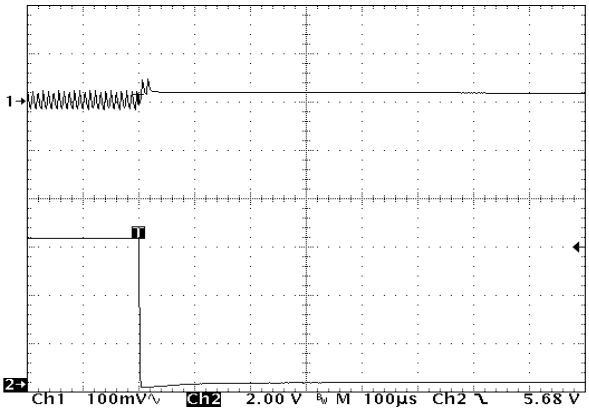
V_{in} = 1.5 V, L = 47 µH, C_{OUT} = 68 µF
1. V_{OUT} = 3.0 V (AC coupled), 100 mV/div
2. I_O = 80 mA to 0.1 mA

Figure 48. NCP1402SN30T1 Load Transient Response



V_{in} = 2.4 V, L = 47 µH, C_{OUT} = 68 µF
1. V_{OUT} = 5.0 V (AC coupled), 100 mV/div
2. I_O = 0.1 mA to 80 mA

Figure 49. NCP1402SN50T1 Load Transient Response



V_{in} = 2.4 V, L = 47 µH, C_{OUT} = 68 µF
1. V_{OUT} = 5.0 V (AC coupled), 100 mV/div
2. I_O = 80 mA to 0.1 mA

Figure 50. NCP1402SN50T1 Load Transient Response

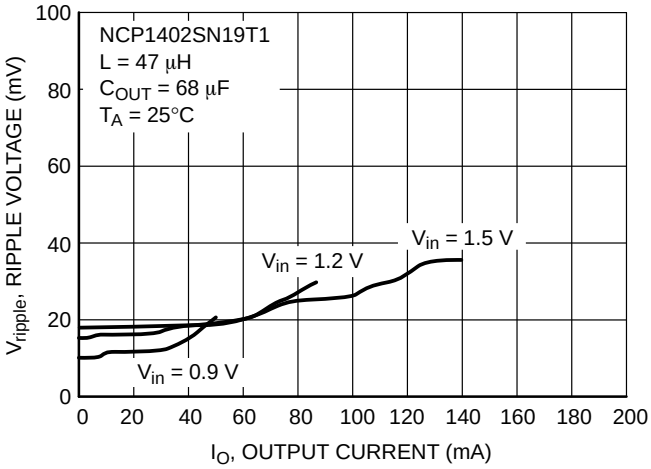


Figure 51. NCP1402SN19T1 Ripple Voltage vs. Output Current

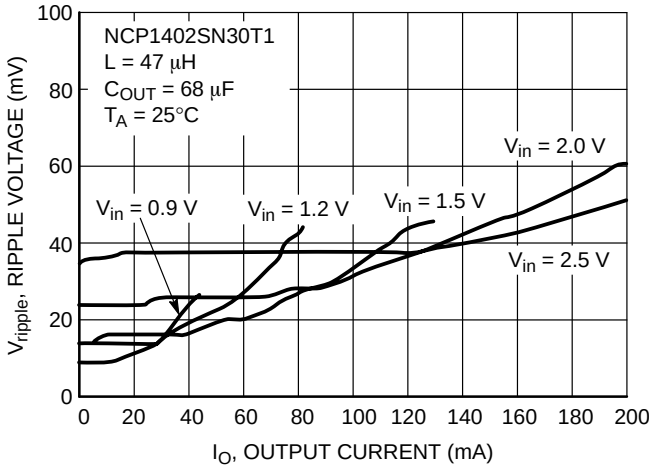


Figure 52. NCP1402SN30T1 Ripple Voltage vs. Output Current

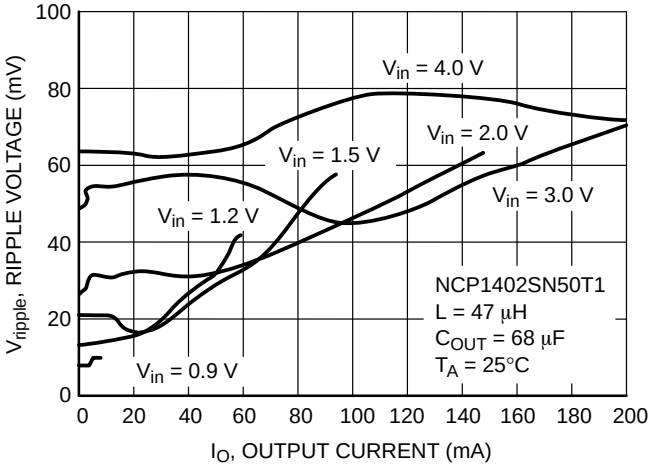


Figure 53. NCP1402SN50T1 Ripple Voltage vs. Output Current

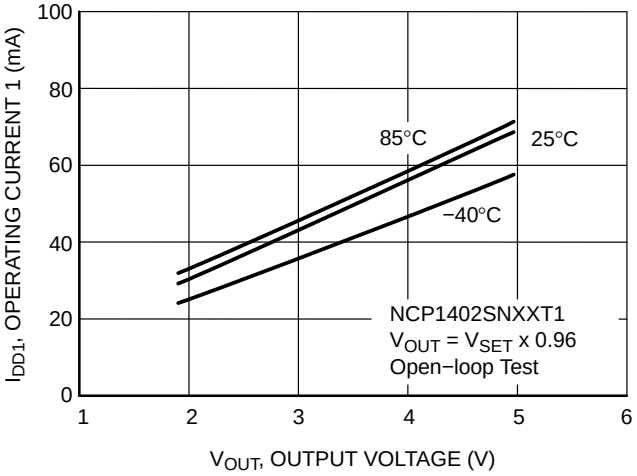


Figure 54. NCP1402SNXXT1 Operating Current 1 vs. Output Voltage

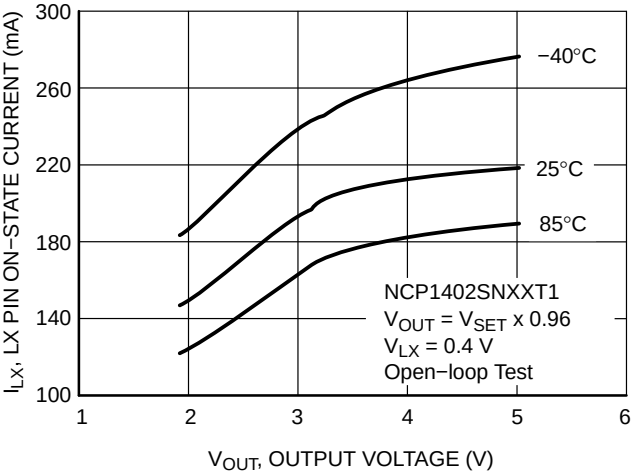


Figure 55. NCP1402SNXXT1 Pin On−state Current vs. Output Voltage

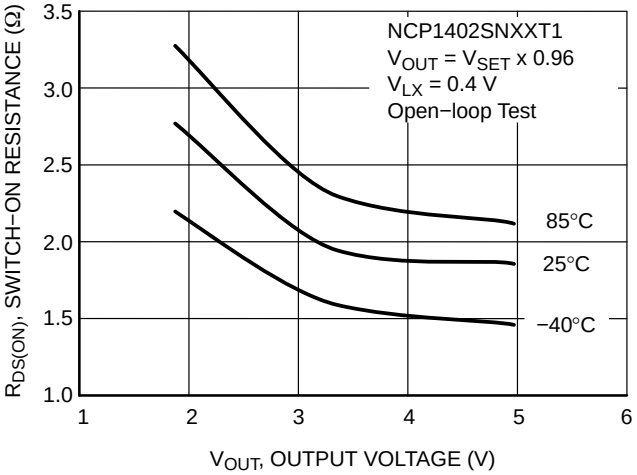


Figure 56. NCP1402SNXXT1 Switch−On Resistance vs. Output Voltage

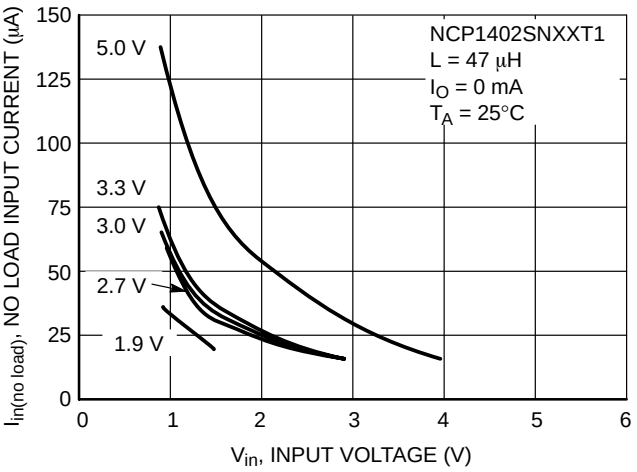


Figure 57. NCP1402SNXXT1 No Load Input Current vs. Input Voltage

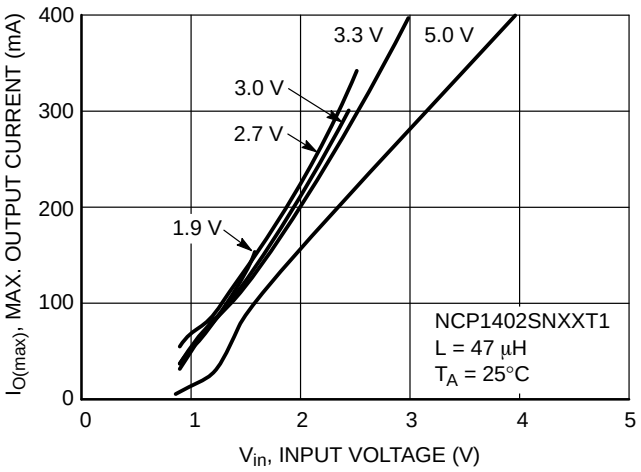


Figure 58. NCP1402SNXXT1 Maximum Output Current vs. Input Voltage

DETAILED OPERATING DESCRIPTION

Operation

The NCP1402 series are monolithic power switching regulators optimized for applications where power drain must be minimized. These devices operate as variable frequency, voltage mode boost regulators and designed to operate in continuous conduction mode. Potential applications include low powered consumer products and battery powered portable products.

The NCP1402 series are low noise variable frequency voltage−mode DC−DC converters, and consist of Soft−Start circuit, feedback resistor, reference voltage, oscillator, PFM comparator, PFM control circuit, current limit circuit and power switch. Due to the on−chip feedback resistor network, the system designer can get the regulated output voltage from 1.8 V to 5 V with a small number of external components. The operating current is typically 30 μA (V_{OUT} = 1.9 V), and can be further reduced to about 0.6 μA when the chip is disabled (V_{CE} < 0.3 V).

The NCP1402 operation can be best understood by examining the block diagram in Figure 2. PFM comparator monitors the output voltage via the feedback resistor. When the feedback voltage is higher than the reference voltage, the power switch is turned off. As the feedback voltage is lower than reference voltage and the power switch has been off for at least a period of minimum off−time decided by PFM oscillator, the power switch is then cycled on for a period of on−time also decided by PFM oscillator, or until current limit signal is asserted. When the power switch is on, current ramps up in the inductor, storing energy in the magnetic field. When the power switch is off, the energy in the magnetic field is transferred to output filter capacitor and the load. The output filter capacitor stores the charge while the inductor current is high, then holds up the output voltage until next switching cycle.

Soft−Start

There is a Soft−Start circuit in NCP1402. When power is applied to the device, the Soft−Start circuit pumps up the output voltage to approximately 1.5 V at a fixed duty cycle, the level at which the converter can operate normally. What is more, the startup capability with heavy loads is also improved.

Regulated Converter Voltage (V_{OUT})

The V_{OUT} is set by an internal feedback resistor network. This is trimmed to a selected voltage from 1.8 to 5.0 V range in 100 mV steps with an accuracy of ±2.5%.

Current Limit

The NCP1402 series utilizes cycle−by−cycle current limiting as a means of protecting the output switch MOSFET from overstress and preventing the small value inductor from saturation. Current limiting is implemented by monitoring the output MOSFET current build−up during conduction, and upon sensing an overcurrent conduction immediately turning off the switch for the duration of the oscillator cycle.

The voltage across the output MOSFET is monitored and compared against a reference by the VLX limiter. When the threshold is reached, a signal is sent to the PFM controller block to terminate the power switch conduction. The current limit threshold is typically set at 350 mA.

Enable / Disable Operation

The NCP1402 series offer IC shut−down mode by chip enable pin (CE pin) to reduce current consumption. An internal pullup resistor tied the CE pin to OUT pin by default i.e. user can float the pin CE for permanent “On”. When voltage at pin CE is equal or greater than 0.9 V, the chip will be enabled, which means the regulator is in normal operation. When voltage at pin CE is less than 0.3 V, the chip is disabled, which means IC is shutdown.

Important: DO NOT apply a voltage between 0.3 V and 0.9 V to pin CE as this is the CE pin’s hyteresis voltage range. Clearly defined output states can only be obtained by applying voltage out of this range.

APPLICATIONS CIRCUIT INFORMATION

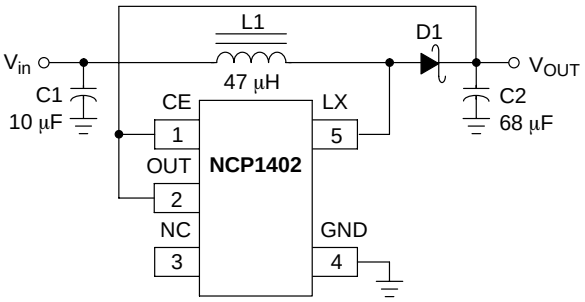


Figure 59. Typical Application Circuit

Step−up Converter Design Equations

NCP1402 step−up DC−DC converter designed to operate in continuous conduction mode can be defined by:

Calculation	Equation
L	$\leq M\left(\frac{V_{in}^2}{V_{OUT}\, I_{Omax}}\right)$
I_{PK}	$\frac{(V_{in} - V_S)t_{on}}{L} + I_{min}$
I_{min}	$\frac{(t_{on} + t_{off})I_O}{t_{off}} - \frac{(V_{in} - V_S)t_{on}}{2L}$
t_{off}	$\frac{(V_{in} - V_S)t_{on}}{(V_{OUT} + V_F - V_{in})}$
ΔQ	$(I_L - I_O)t_{off}$
V_{ripple}	$\approx \frac{\Delta Q}{C_{OUT}} + (I_L - I_O)ESR$

*NOTES:
- I_{PK} − Peak inductor current
- I_{min} − Minimum inductor current
- I_O − Desired dc output current
- I_{Omax} − Desired maximum dc output current
- I_L − Average inductor current
- V_{in} − Nominal operating dc input voltage
- V_{OUT} − Desired dc output voltage
- V_F − Diode forward voltage
- V_S − Saturation voltage of the internal FET switch
- ΔQ − Charge stores in the C_{OUT} during charging up
- V_{ripple} − Output ripple voltage
- ESR − Equivalent series resistance of the output capacitor
- M − An empirical factor, when $V_{OUT} \geq 3.0$ V, $M = 8 \times 10^{-6}$, otherwise $M = 5.3 \times 10^{-6}$.

EXTERNAL COMPONENT SELECTION

Inductor

The NCP1402 is designed to work well with a 47 μH inductor in most applications. 47 μH is a sufficiently low value to allow the use of a small surface mount coil, but large enough to maintain low ripple. Low inductance values supply higher output current, but also increase the ripple and reduce efficiency. Note that values below 27 μH is not recommended due to NCP1402 switch limitations. Higher inductor values reduce ripple and improve efficiency, but also limit output current.

The inductor should have small DCR, usually less than 1 Ω to minimize loss. It is necessary to choose an inductor with saturation current greater than the peak current which the inductor will encounter in the application.

Diode

The diode is the main source of loss in DC−DC converters. The most importance parameters which affect their efficiency are the forward voltage drop, V_F, and the reverse recovery time, t_{rr}. The forward voltage drop creates a loss just by having a voltage across the device while a current flowing through it. The reverse recovery time generates a loss when the diode is reverse biased, and the current appears to actually flow backwards through the diode due to the minority carriers being swept from the P−N junction. A Schottky diode with the following characteristics is recommended:

Small forward voltage, $V_F < 0.3$ V
Small reverse leakage current
Fast reverse recovery time/ switching speed
Rated current larger than peak inductor current, $I_{rated} > I_{PK}$
Reverse voltage larger than output voltage, $V_{reverse} > V_{OUT}$

Input Capacitor

The input capacitor can stabilize the input voltage and minimize peak current ripple from the source. The value of the capacitor depends on the impedance of the input source used. Small Equivalent Series Resistance (ESR) Tantalum or ceramic capacitor with value of 10 μF should be suitable.

Output Capacitor

The output capacitor is used for sustaining the output voltage when the internal MOSFET is switched on and smoothing the ripple voltage. Low ESR capacitor should be used to reduce output ripple voltage. In general, a 47 uF to 68 uF low ESR (0.15 Ω to 0.30 Ω) Tantalum capacitor should be appropriate. For applications where space is a critical factor, two parallel 22 uF low profile SMD ceramic capacitors can be used.

An evaluation board of NCP1402 has been made in the size of 23 mm x 20 mm only, as shown in Figures 60 and 61. Please contact your ON Semiconductor representative for availability. The evaluation board schematic diagram, the artwork and the silkscreen of the surface mount PCB are shown below:

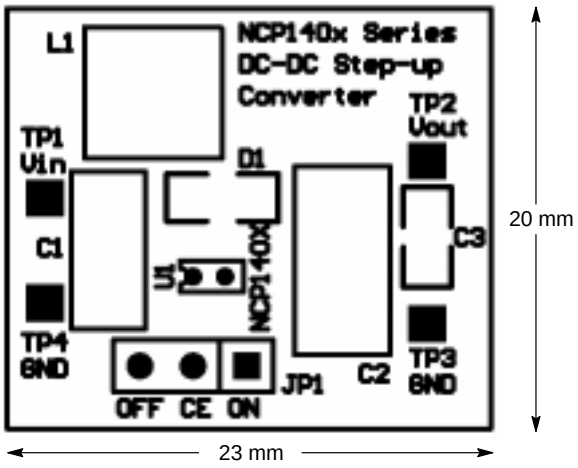


Figure 60. NCP1402 PFM Step−Up DC−DC Converter Evaluation Board Silkscreen

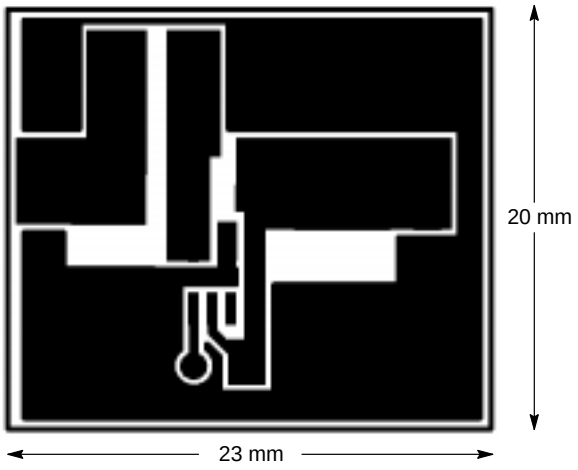


Figure 61. NCP1402 PFM Step−Up DC−DC Converter Evaluation Board Artwork (Component Side)

Components Supplier

Parts	Supplier	Part Number	Description	Phone
Inductor, L1	Sumida Electric Co. Ltd.	CD54−470L	Inductor 47 μH / 0.72 A	(852)−2880−6688
Schottky Diode, D1	ON Semiconductor Corp.	MBR0520LT1	Schottky Power Rectifier	(852)−2689−0088
Output Capacitor, C2	KEMET Electronics Corp.	T494D686K010AS	Low ESR Tantalum Capacitor 68 μF / 10 V	(852)−2305−1168
Input Capacitor, C1	KEMET Electronics Corp.	T491C106K016AS	Low Profile Tantalum Capacitor 10 μF / 16 V	(852)−2305−1168

PCB Layout Hints

Grounding

One point grounding should be used for the output power return ground, the input power return ground, and the device switch ground to reduce noise as shown in Figure 62, e.g.: C2 GND, C1 GND, and U1 GND are connected at one point in the evaluation board. The input ground and output ground traces must be thick enough for current to flow through and for reducing ground bounce.

Power Signal Traces

Low resistance conducting paths should be used for the power carrying traces to reduce power loss so as to improve efficiency (short and thick traces for connecting the inductor L can also reduce stray inductance), e.g.: short and thick traces listed below are used in the evaluation board:

1. Trace from TP1 to L1
2. Trace from L1 to Lx pin of U1
3. Trace from L1 to anode pin of D1
4. Trace from cathode pin of D1 to TP2

Output Capacitor

The output capacitor should be placed close to the output terminals to obtain better smoothing effect on the output ripple.

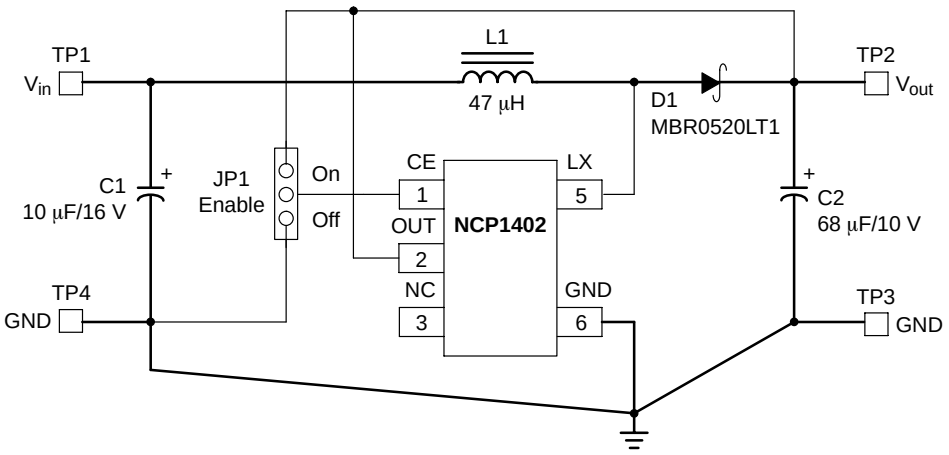
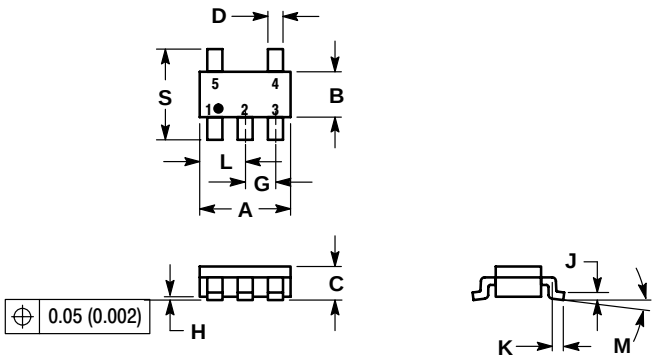


Figure 62. NCP1402 Evaluation Board Schematic Diagram

PACKAGE DIMENSIONS

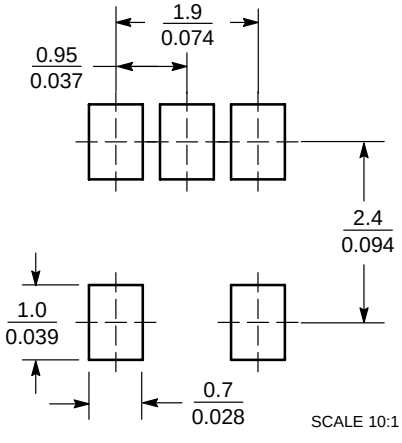
SOT23−5
(TSOP−5, SC59−5)
SN SUFFIX
CASE 483−02
ISSUE C



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. A AND B DIMENSIONS DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	2.90	3.10	0.1142	0.1220
B	1.30	1.70	0.0512	0.0669
C	0.90	1.10	0.0354	0.0433
D	0.25	0.50	0.0098	0.0197
G	0.85	1.05	0.0335	0.0413
H	0.013	0.100	0.0005	0.0040
J	0.10	0.26	0.0040	0.0102
K	0.20	0.60	0.0079	0.0236
L	1.25	1.55	0.0493	0.0610
M	0	10	0	10
S	2.50	3.00	0.0985	0.1181

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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