Compact LCD Bias IC With High Speed Amplifiers for TV-LCD Panels

FEATURES

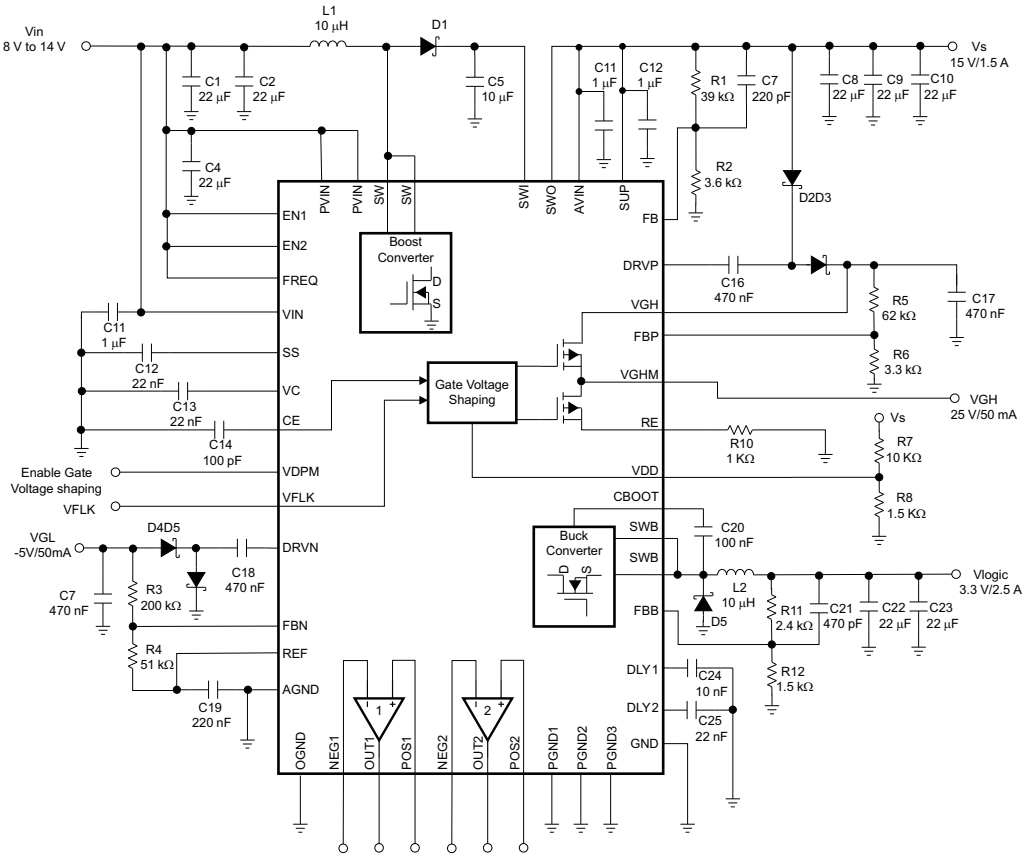
- 8-V to 14.4-V Input Voltage Range
- 500 kHz / 750 kHz Fixed Switching Frequency
- Boost Output Voltage up to 19 V
  - 1%-Accurate Boost With 2.8-A Switch Current Overvoltage Protection
- Input-to-Output Isolation Switch for Vs Short-Circuit protection for Boost
- 2.5-A Step-Down Converter
- Regulated Positive Charge-Pump Driver VGH
- Regulated Negative Charge-Pump Driver VGL
- Gate Voltage Shaping for VGH
- Soft Start for all Converters
- Two Integrated High-Speed Opamps
  - 50-MHz, 3-dB Bandwidth
  - Slew Rate 55 V / µs
  - 215-mA Short-Circuit Current
- 48 Pin 7x7 mm QFN Package

APPLICATIONS

- LCD TV
- LCD Monitor

DESCRIPTION

The TPS65162 is a compact LCD bias IC with two high-speed operational amplifiers for the V_{com} supply. The high current capability of the device is ideal for large LCD-monitor and LCD-TV applications.



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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

DESCRIPTION (CONTINUED)

The TPS65162 generates all four voltage rails for a TFT LCD (Vs, Vlogic, VGH and VGL) and includes two op-amps to generate the VCOM supply rail. An input-to-output isolation switch is integrated into the device, providing short-circuit protection for the boost converter. A current-limit function is implemented in the input-to-output isolation switch to allow soft turn-on during start-up. The device also features gate voltage shaping for improved TFT-LCD picture quality. The device consists of a boost converter to provide the source voltage Vs, and a step-down converter to provide the logic voltage for the system. A positive and a negative charge-pump driver provide adjustable regulated output voltages VGH and VGL to bias the TFT. Both boost and buck converter, as well as the charge-pump drivers, operate with a fixed switching frequency of 500 kHz or 750 kHz, selectable by the FREQ pin. The device includes adjustable power-on sequencing. The safety features of the device are overvoltage protection for boost converter, short-circuit protection for Vs, Vlogic and VGH, and thermal shutdown.

ORDERING INFORMATION(1)

T_A	ORDERING	QFN PACKAGE	PACKAGE MARKING
–40°C to 85°C	TPS65162RGZR	48 pin QFN	TPS65162

(1) The RGZ package is available taped and reeled and shipped in quantities of 2500 devices per reel.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

			VALUE	UNIT
	Input voltage range VIN, PVIN(2)		–0.3 to 16.8	V
	Voltage range at EN1, EN2, FREQ, VDPM, VFLK		– 0.3 to 16.8	V
V_I	Voltage on pin	AVIN, SUP	25	V
		VGH, VGHM, RE	35	V
		SW, SWI, SWO	25	V
		SWB	20	V
	Continuous total power dissipation		See Dissipation Rating Table	
T_J	Operating junction temperature range		–40 to 150	°C
T_A	Operating ambient temperature range		–65 to 85	°C
T_{stg}	Storage temperature range		–65 to 150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

DISSIPATION RATINGS(1)

PACKAGE	$R_{\theta JA}$	$T_A \le 25°C$ POWER RATING	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
48 pin QFN	30°C/W	3.33 W	1.83 W	1.33 W

(1) Exposed thermal die is soldered to the PCB using thermal vias. Refer to Texas Instruments Application report (SLUA271) QFN/SON PCB Attachment.

RECOMMENDED OPERATING CONDITIONS

		MIN	TYP	MAX	UNIT
VIN, PVIN	Input voltage range	8		14.4	V
T_A	Operating ambient temperature	–40		85	°C
T_J	Operating junction temperature	–40		125	°C

ELECTRICAL CHARACTERISTICS

Vin=12 V, EN1=EN2=FREQ=high, Vs=15 V, Vlogic=3.3 V ,T_A = –40°C to 85°C, typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
V_I	Input voltage range		8		14.4	V
I_{SD}	Shutdown current into VIN	EN1=EN2=GND		0.03	1	µA
	Shutdown current into PVIN	EN1=EN2=GND		0.01	1	
I_{QIN}	Quiescent current into VIN			1.7	4	mA
I_{SUP}	Shutdown current into SUP	EN1=EN2=GND		0.01	1	µA
I_{AVIN}	Shutdown current into AVIN	EN1=EN2=GND		50	220	µA
	Quiescent current into AVIN			8	10	mA
V_{UVLO}	Undervoltage lockout threshold	Vin falling		7.6	7.95	V
V_{REF}	Reference voltage		1.253	1.265	1.277	V
	Thermal shutdown	Temperature rising		160		°C
	Thermal shutdown hysteresis			10		°C
LOGIC SIGNALS EN1, EN2, FREQ, VFLK, VDPM						
V_{IH}	High level input voltage EN1, EN2, VDPM, FREQ		2.0			V
V_{IL}	Low level input voltage EN1, EN2, VDPM, FREQ				0.8	V
V_{IH}	High level input voltage VFLK		1.7			V
V_{IL}	lOW level input voltage VFLK				0.4	V
I_I	Input leakage current	EN1=EN2=FREQ=VFLK=VDPM=GND or VIN		0.01	0.1	µA
CONTROL AND SOFT START DLY1, DLY2, SS						
I_{chrg}	DLY1, DLY2 charge current	$V_{threshold}$ = 1.280 V	3.5	5	6	µA
I_{SS}	SS charge current		6	9.2	12	
V_{thr}	Delay threshold			1.280		V
INTERNAL OSCILLATOR						
fosc	Oscillator frequency	FREQ = high	600	750	900	kHz
		FREQ = low	400	500	600	
BOOST CONVERTER (Vs)						
V_S	Output voltage range				19	V
V_{FB}	Feedback regulation voltage		1.255	1.268	1.280	V
I_{FB}	Feedback input bias current			10	100	nA
$R_{DS(on)}$	N-MOSFET on-resistance (Q1)	Vs = 15 V, $I_{(SW)}$ = 500 mA		130	200	mΩ
	P-MOSFET on-resistance (Q2)	Vs = 15 V,$I_{(SW)}$ = 200 mA		9	15	Ω
I_{MAX}	Maximum P-MOSFET peak switch current				1	A
I_{LIM}	N-MOSFET switch current limit (Q1)		2.8	3.6	4.2	A
Ileak	Switch leakage current	$V_{(SW)}$ = 15 V		1	10	µA
Vswovp	Switch overvoltage protection	Vout rising	19.5	20	21	V
	Line Regulation	8V≤Vin≤14V, Iout = 2mA		0.007		%/V
	Load Regulation	2mA≤Iout≤1.5A		0.03		%/A
ISOLATION SWITCH						
RDSon	Isolation switch RDSon	I_{SW} = 1 A, Vs = 15 V		200		mΩ
I	Switch current				2	A
I_{SC}	Short circuit current limit	SWI = 12V, SWO = 0V		350		mA

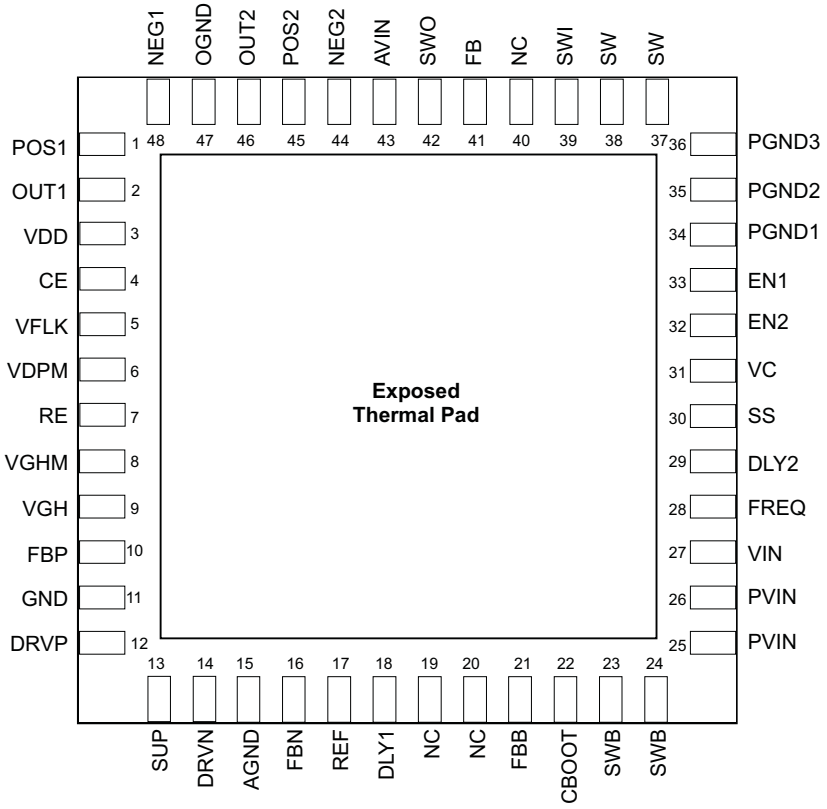
ELECTRICAL CHARACTERISTICS (continued)

Vin=12 V, EN1=EN2=FREQ=high, Vs=15 V, Vlogic=3.3 V ,T_A = –40°C to 85°C, typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
GATE VOLTAGE SHAPING VGHM						
V_{HVIN}	Input voltage				35	V
RDSon	VGH to VGHM RDSon (Q1)	VFLK = high, I = 20 mA		10	15	Ω
	VGHM to RE RDSon	VFLK = LOW, I = 20 mA		60	100	
I_{CE}	CE capacitor charge current	V_{CE} = 1.265 V	44	57	65	µA
V_{CE}	CE threshold voltage			1.284		V
G_{VDD}	VDD voltage gain	V_{VDD} = 1 V		5		V/V
STEP-DOWN CONVERTER (Vlogic)						
Vlogic	Output voltage range		1.5		5	V
V_{FB}	Feedback regulation voltage		1.240	1.265	1.290	V
I_{FB}	Feedback input bias current			10	100	nA
$R_{DS(on)}$	N-MOSFET on-resistance (Q1)	PVIN = 12 V, $I_{(SW)}$ = 500 mA		180	320	mΩ
I_{LIM}	N-MOSFET switch current limit (Q1)		2.8	3.6	4.2	A
Ileak	Switch leakage current	$V_{(SW)}$ = 0 V		1	10	µA
	Line regulation	8V≤Vin≤14V, Iout = 2mA		0.006		%/V
	Load regulation	2mA≤Iout≤2.5A		0.06		%/A
NEGATIVE CHARGE PUMP VGL						
VGL	Output voltage range				-2	V
V_{FB}	Feedback regulation voltage		–48	0	48	mV
I_{FB}	Feedback input bias current			10	100	nA
$R_{DS(on)}$	Q4 P-Channel switch RDSon	I_O = 20 mA		4	8	Ω
V_{DropN}	Current source voltage drop(1)	$I_{(DRVN)}$ = 50 mA, $V_{(FBN)}$ = $V_{(FBNnominal)}$– 5%		115	200	mV
		$I_{(DRVN)}$ = 100 mA, $V_{(FBN)}$ = $V_{(FBNnominal)}$– 5%		230	400	
	Load regulation	1 mA ≤ I_O ≤ 100 mA, VGL = –5 V		0.01		%/mA
POSITIVE CHARGE PUMP OUTPUT VGH						
VGH	Output voltage range				34	V
V_{FB}	Feedback regulation voltage		1.228	1.265	1.302	V
I_{FB}	Feedback input bias current			10	100	nA
RDSon	Q3 N-Channel switch RDSon	I_{OUT} = 20 mA		1.0	1.8	Ω
V_{DropP}	Current source voltage drop (V_{sup}–V_{DRP})(1)	I_{DRP} = 50 mA, V_{FBP} = $V_{FBPnominal}$– 5%		430	680	mV
		I_{DRP} = 100 mA, V_{FBP} = $V_{FBPnominal}$– 5%		950	1600	
	Load regulation	1 mA ≤ Iout ≤ 50 mA, VGH = 27 V		0.073		%/mA
OPERATIONAL AMPLIFIERS 1, 2						
Vos	Input offset voltage	V_{CM} = Vs/2	–15		18	mV
I_B	Input bias current	V_{CM} = Vs/2		0.05	3	µA
V_{CM}	Common Mode Input Voltage Range		0		Vs	V
CMRR	Common Mode Rejection Ratio	V_{CM} = 7.5 V	70			dB
A_{VOL}	Open Loop Gain	0.5 V ≤ V_{OUT}≤ 14.5 V, No load	50			dB
V_{OL}	Output Voltage Swing Low	I_{OUT} = 10 mA		60	200	mV
V_{OH}	Output Voltage Swing High	I_{OUT} = 10 mA	Vs-200	Vs-100		mV
I_{sc}	Short Circuit Current		120	215		mA
I_o	Output Current	V_{OUT} = 7.5 V , Input offset voltage 10 mV	90	170		mA
PSRR	Power Supply Rejection Ratio			80		dB
SR	Slew Rate	A_V = 1, VIN = 2 Vpp		55		V/µs
BW	– 3db Bandwidth	A_V = 1, V_{OUT} = 60 mVpp		50		MHz
GBWP	Gain Bandwidth Product			36		MHz

(1) The maximum charge pump output current is typically one-half the drive current of the internal current source.

PIN ASSIGNMENT
Top View



NOTE: The thermally-enhanced PowerPAD is connected to PGND1 (Device power Ground). NC pin is internally not connected.

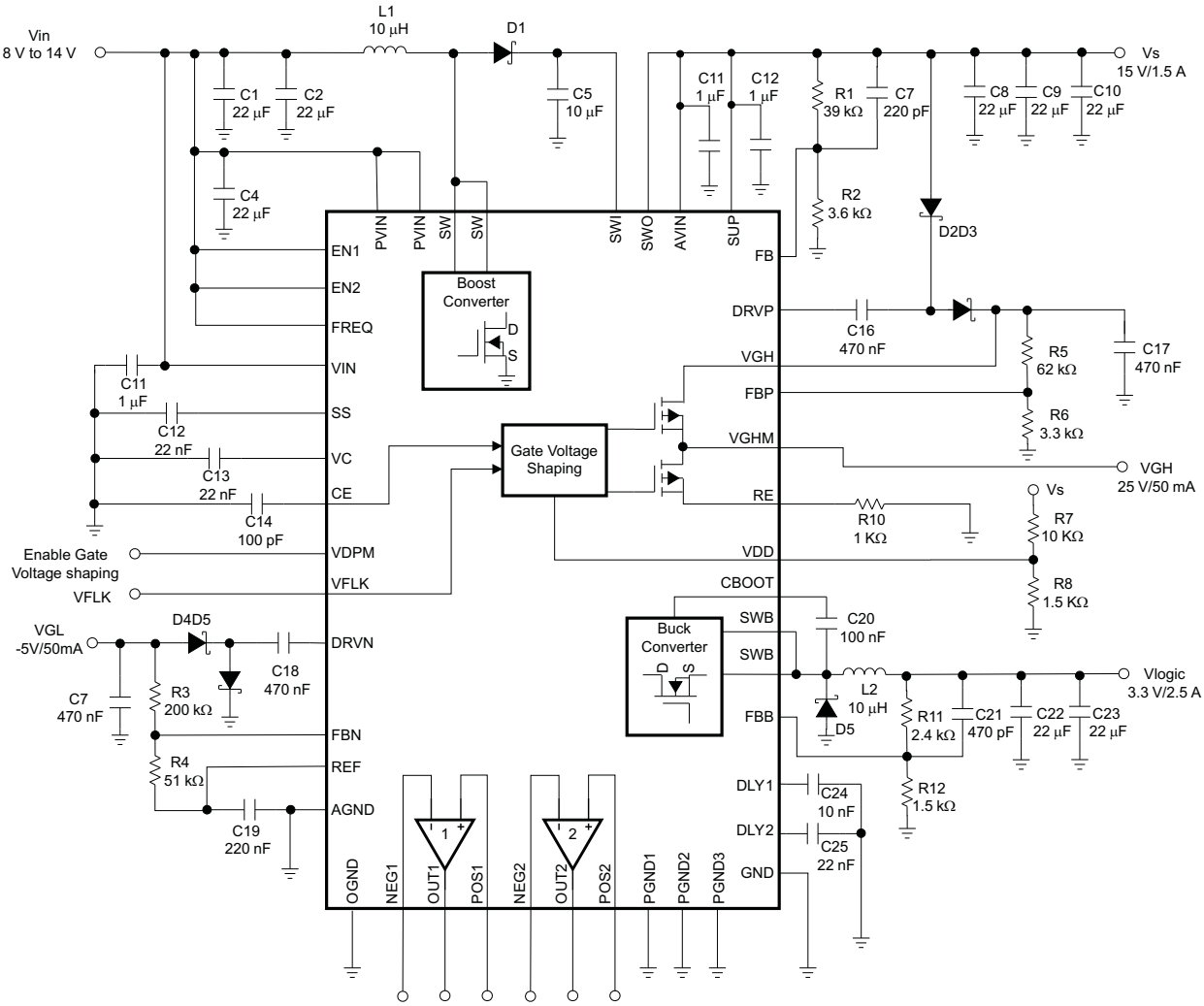
TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
POS1	1	I	Non inverting input of Operational Amplifier 1
OUT1	2	O	Output of Operational Amplifier 1.
VDD	3	I	Threshold voltage of gate voltage shaping. The five times of voltage applied to this pin set the threshold discharge voltage for the gate voltage shaping function
CE	4	I	Delay of gate voltage shaping. Sets the delay between the falling edge of VFLK to the falling edge of VGHM
VFLK	5	I	Control of gate voltage shaping.
VDPM	6	I	Enable of gate voltage shaping block.
RE	7	O	Slope adjustment of gate voltage shaping. Connecting a resistor to this pin allows to adjust the slop of gate voltage shaping.
VGHM	8	O	Output of the gate voltage shaping block.
VGH	9	I	High voltage for gate voltage shaping block. Connect the output of the positive charge pump to this pin.
FBP	10	I	Feedback of the positive charge pump.
GND	11		Ground for positive and negative charge pump.
DRVP	12	O	Drive pin of the positive charge pump.
SUP	13	I	Supply pin of the positive charge pump
DRVN	14	O	Drive pin of the negative charge pump
AGND	15		Analog ground
FBN	16	I	Feedback of the negative charge pump.

TERMINAL FUNCTIONS (continued)

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
REF	17	O	Internal reference output. Connect 220-nF capacitor directly from this pin to AGND to minimize possible noise coupling into the reference of the IC.
DLY1	18	O	Connecting a capacitor from this pin to GND allows setting the delay time between the step down converter and negative charge pump VGL
NC	19, 20, 40		Not connected.
FBB	21	I	Feedback of the buck converter.
CBOOT	22	I	N-channel MOSFET gate drive voltage for the buck converter. Connect a capacitor from this pin to SWB.
SWB	23, 24	O	Switch pin of the buck converter
PVIN	25, 26	I	Power input for the buck converter.
VIN	27	I	Analog input voltage of the device. This pin should be bypassed with a 1-µF capacitor for good filtering.
FREQ	28	I	Frequency selection pin. With FREQ=high, the device operates with 750 kHz. With FREQ=low, the device operates with 500kHz.
DLY2	29	O	Connecting a capacitor from this pin to GND allows setting the delay time between the step down converter and positive charge pump VGH.
SS	30	O	soft-start of the boost converter. Connect a capacitor from this pin to GND.
VC	31	O	Compensation pin of the boost converter.
EN2	32	I	Enable pin of the boost converter block.
EN1	33	I	Enable pin of the buck converter and negative charge pump. When this pin is pulled high, the buck converter starts up, and after a delay time set by DLY1, the negative charge pump starts up. A logic high enables the device and a logic low shut down the device.
PGND1	34		Power ground.
PGND2	35		Ground for boost converter.
PGND3	36		
SW	37, 38	I	Switch pin of the boost converter
SWI	39	I	Input of the isolation switch. The SWI pin is connected to internal overvoltage protection comparator.
FB	41	I	Feedback of the boost converter generating Vs
SWO	42	O	Output of the isolation switch
AVIN	43	I	Power input voltage pin for Operational Amplifier. Bypass this pin with a 1-µF bypass capacitor
NEG2	44	I	Inverting input of Operational Amplifier 2
POS2	45	I	Non inverting input of Operational Amplifier 2
OUT2	46	O	Output of Operational Amplifier 2
OGND	47		Ground for Operational Amplifier.
NEG1	48	I	Inverting input of Operational Amplifier 1

FUNCTIONAL BLOCK DIAGRAM



TYPICAL CHARACTERISTICS

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η	Efficiency	vs Load current	Figure 1
	Soft start		Figure 2
	PWM operation	at nominal load current	Figure 3
	PWM operation	at light load current	Figure 4
	Load transient response		Figure 5
	Short-circuit protection		Figure 6
	Overvoltage protection		Figure 7
Step-Down Converter (Vlogic)			
η	Efficiency	vs Load current	Figure 8
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	PWM operation	at light load current	Figure 10
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	Load transient response		Figure 12
System Performance			
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	Powerup sequencing	EN2 enabled separately	Figure 14
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	VGL	vs VGL Load current	Figure 16
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	Slew rate, opamp		Figure 18

BOOST CONVERTER (Vs)

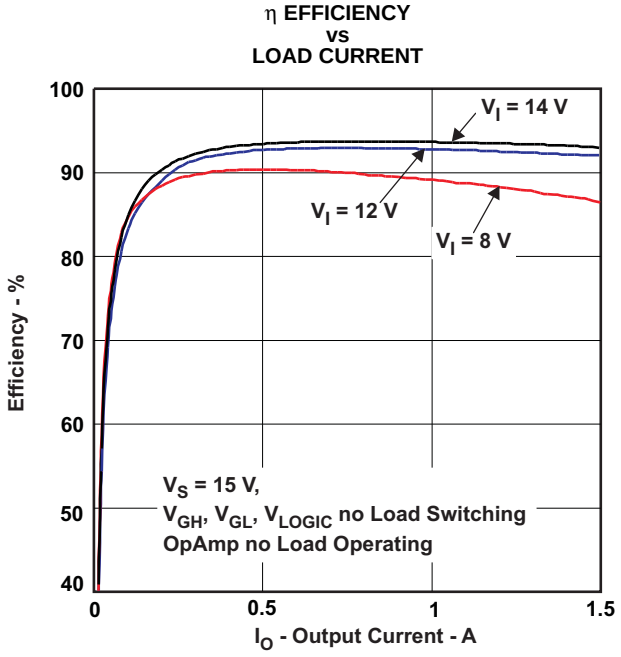


Figure 1.

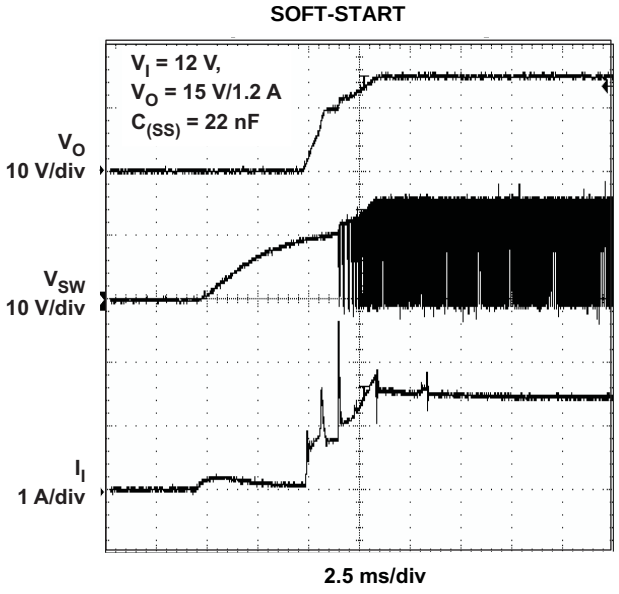


Figure 2.

PWM OPERATION AT NOMINAL LOAD CURRENT

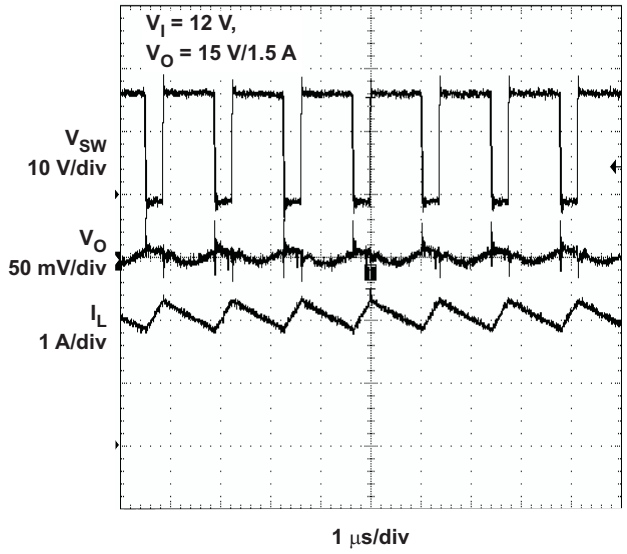


Figure 3.

PWM OPERATION, LIGHT LOAD CURRENT

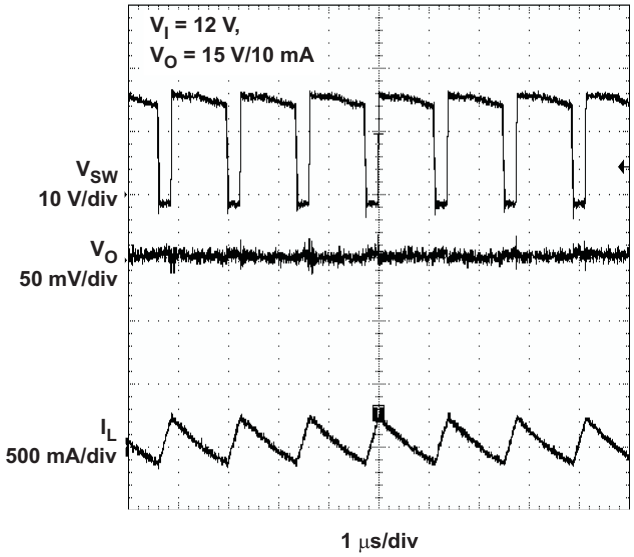


Figure 4.

LOAD TRANSIENT RESPONSE

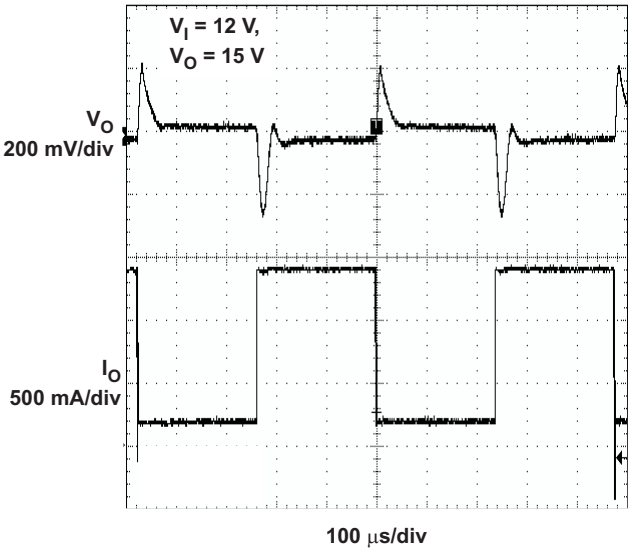


Figure 5.

SHORT CIRCUIT PROTECTION

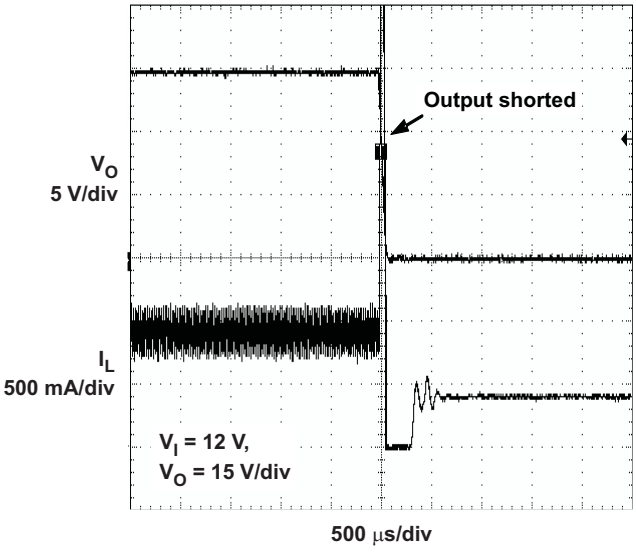


Figure 6.

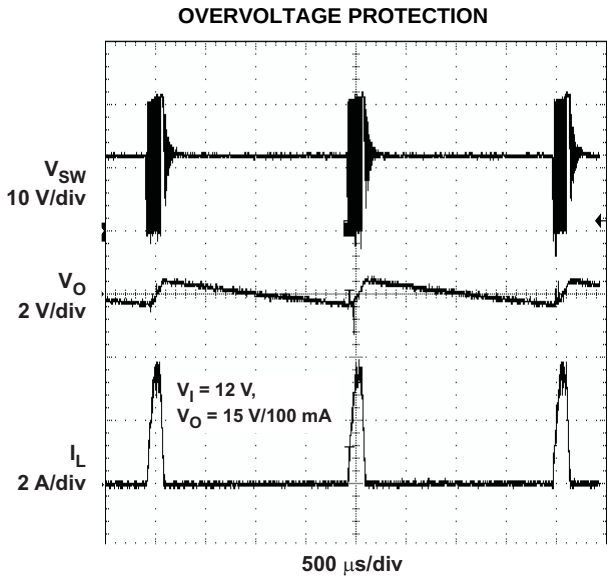


Figure 7.

STEP-DOWN CONVERTER (Vlogic)

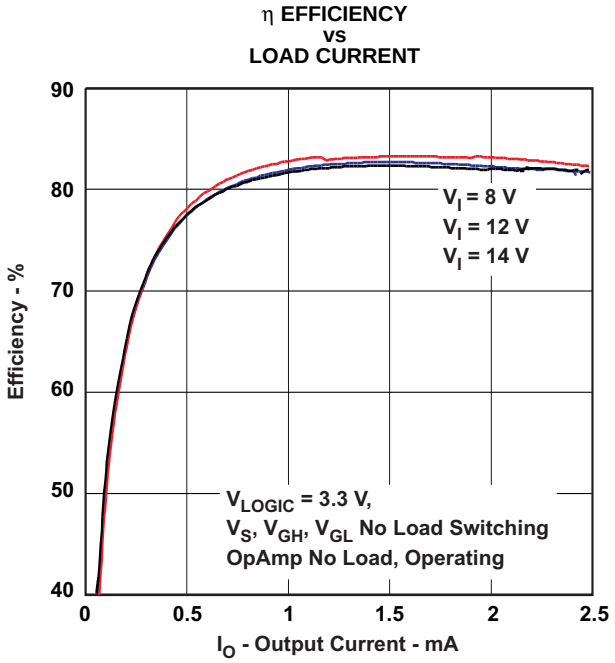


Figure 8.

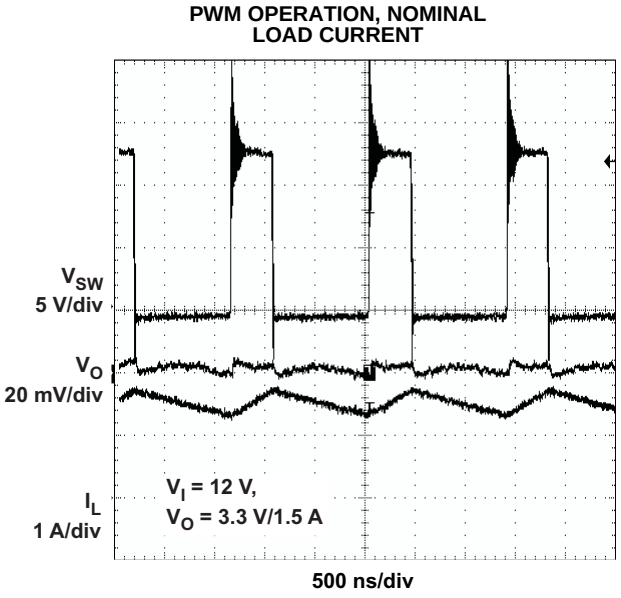


Figure 9.

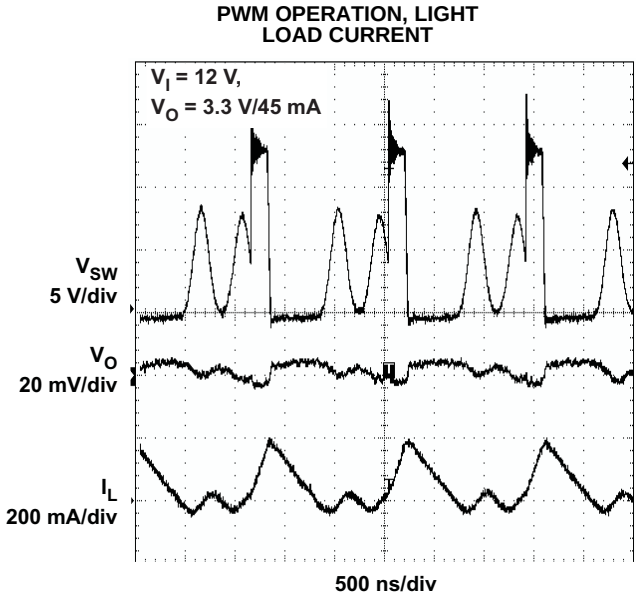


Figure 10.

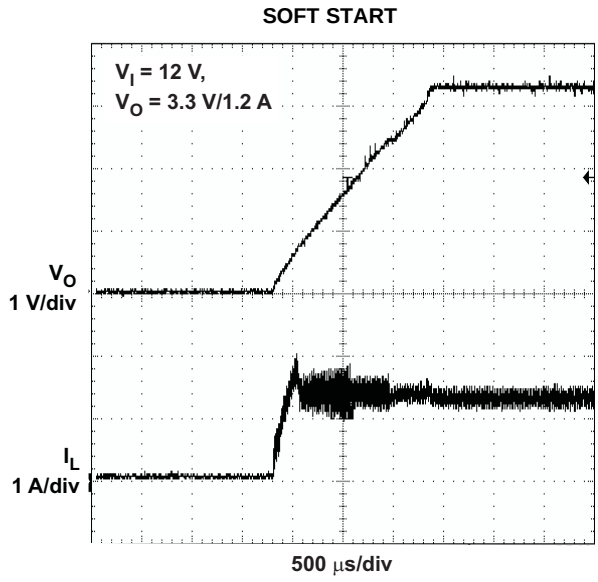


Figure 11.

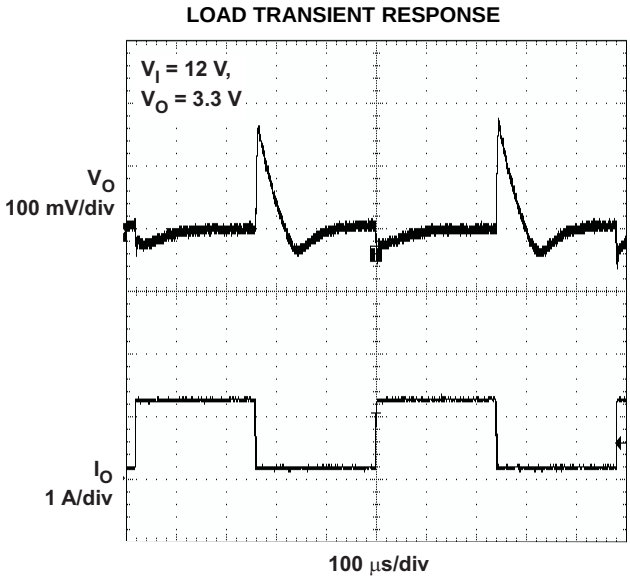


Figure 12.

SYSTEM PERFORMANCE

POWERUP SEQUENCING
vs
EN2 CONNECTED TO VIN

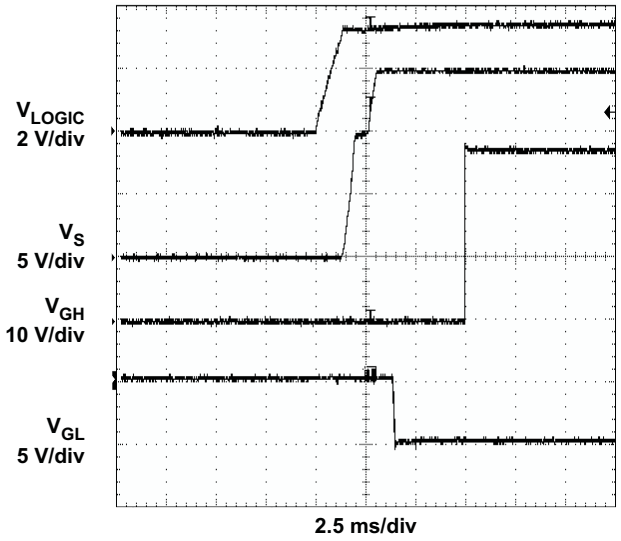


Figure 13.

POWERUP SEQUENCING
vs
EN2 ENABLED SEPARATELY

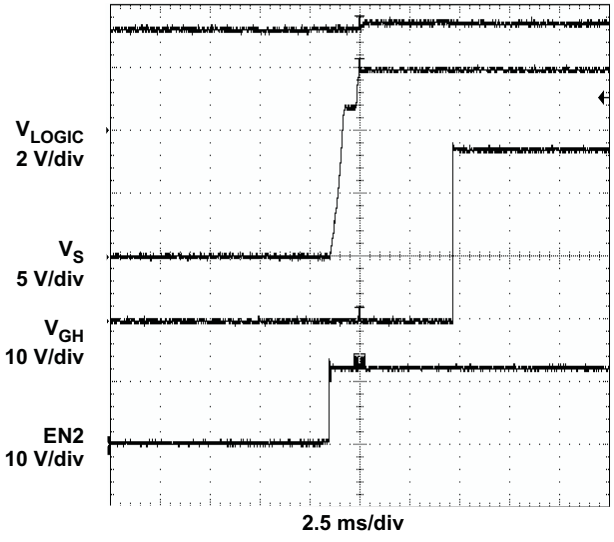


Figure 14.

GATE VOLTAGE SHAPING

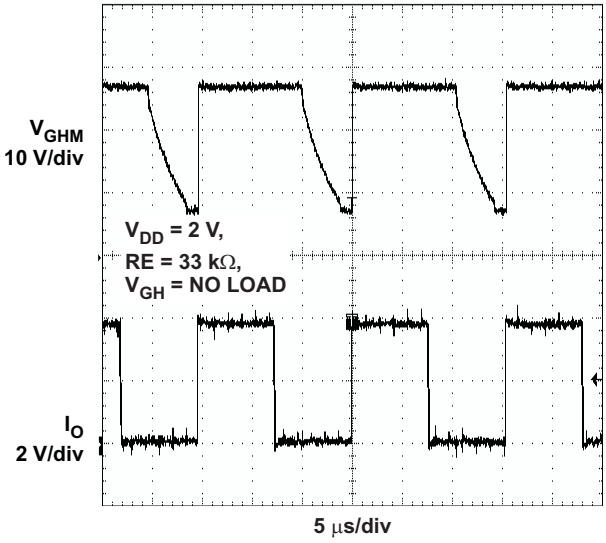


Figure 15.

NEGATIVE CHARGE PUMP DRIVER

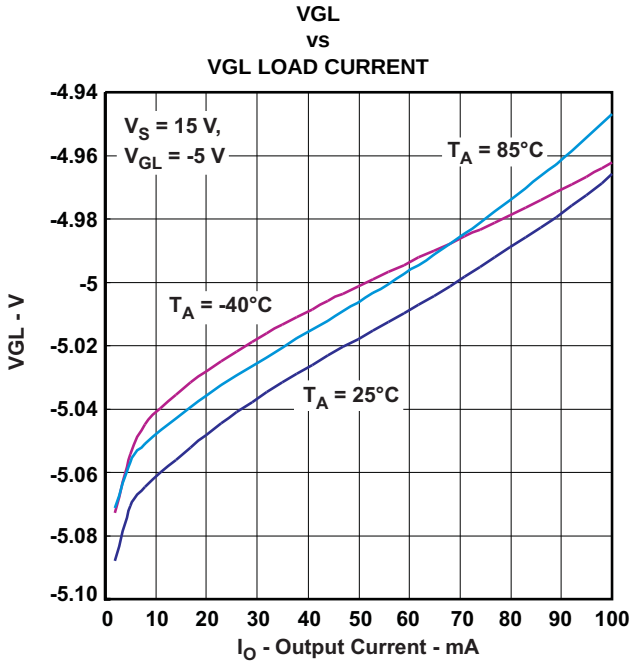


Figure 16.

VCOM BUFFERS

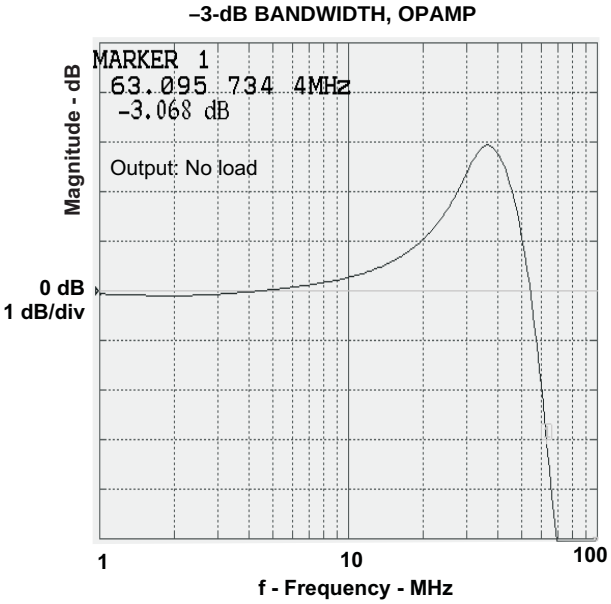


Figure 17.

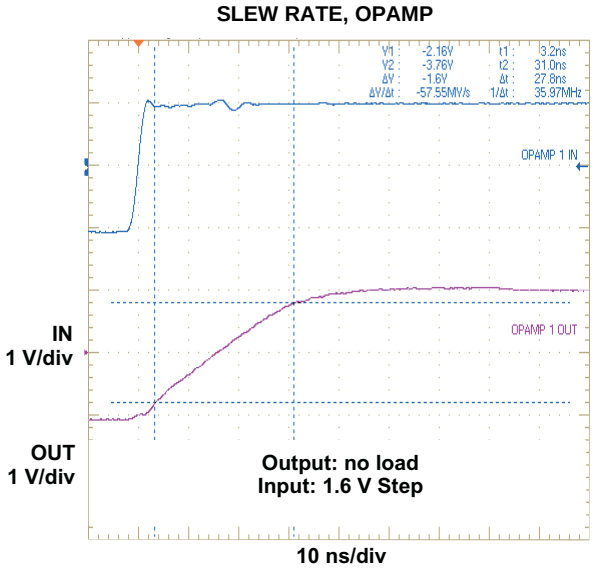


Figure 18.

APPLICATION INFORMATION

THERMAL SHUTDOWN

The thermal-shutdown feature prevents damage from excessive heat and power dissipation. Typically, the thermal-shutdown threshold is 160°C. When the temperature drops below the thermal shutdown threshold, the device restarts again automatically.

UNDERVOLTAGE LOCKOUT

To avoid device malfunction at low input voltages, an undervoltage lockout is included, which shuts down the device at voltages lower than 7.6 V.

REFERENCE OUTPUT, REF

The device provides a reference output that is used to regulate the negative charge pump. In order to have a stable reference voltage, a 220-nF bypass capacitor is required, connected directly from REF to AGND. The reference output has a current capability of 30 µA which should not be exceeded. Because of this, the feedback resistor from FBN to REF should not be smaller than 40 kΩ.

START-UP SEQUENCING

The start-up sequencing can be set by adjusting the capacitors connected to DLY1 and DLY2, and is controlled by the signals EN1 and EN2. Pulling EN1 high enables the step-down converter. After the step down converter has reached its power-good threshold, the other sequence timings are started. DLY1 sets the delay time between the step-down converter and the negative charge-pump driver. This delay starts when the power-good threshold of the step-down converter is reached. A high level on EN2 enables the boost converter. The boost converter starts when the power-good threshold of the step down converter is reached and EN2 is pulled high. DLY2 sets the delay time for the positive charge pump. This delay time starts when the power good threshold of the step down converter is reached. After the delay time has expired, the positive charge pump and op-amps start up. As the positive charge pump power-good threshold is reached, then the GPM block is enabled if VDPM is high as well. See Figure 19.

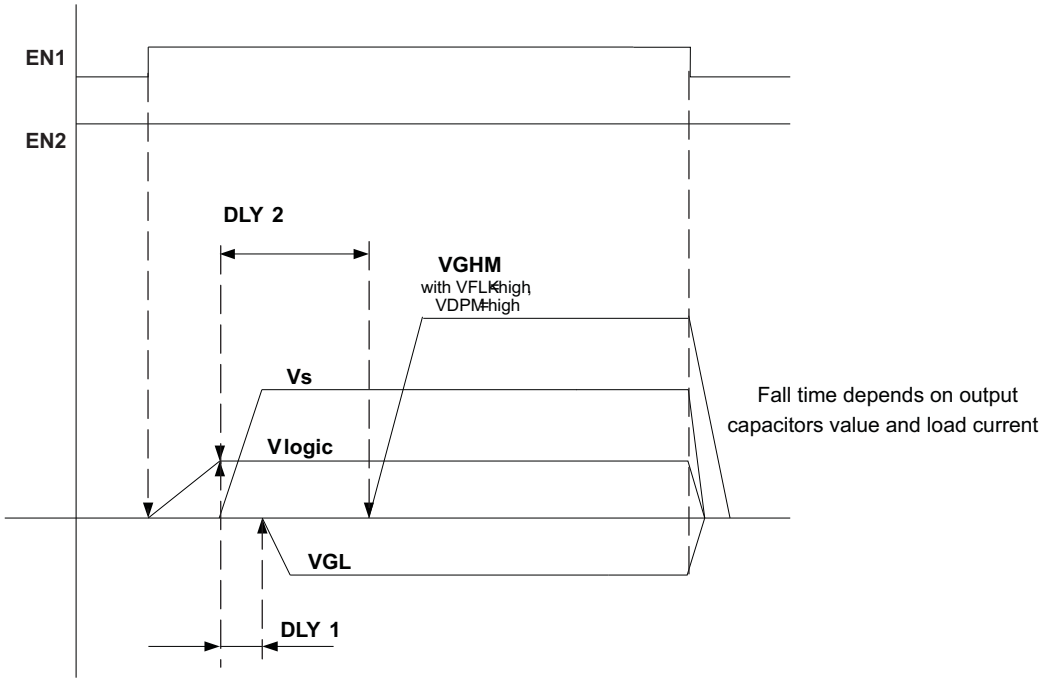


Figure 19. Power-On Sequencing With EN2 Always High (EN2=VIN)

APPLICATION INFORMATION (continued)

If EN2 goes high after the step down converter is already enabled, then the delay DLY2 starts when EN2 goes high. See Figure 20.

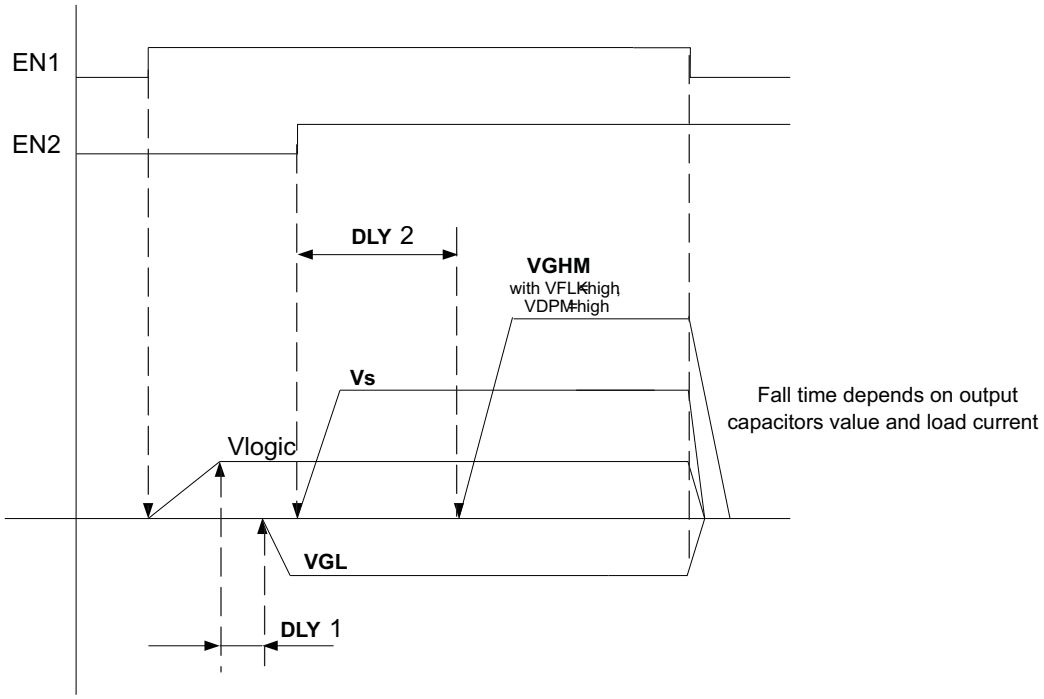


Figure 20. Power-on Sequencing Using EN1 and EN2

SETTING THE DELAY TIMES DLY1, DLY2

Connecting an external capacitor to the DLY1 and DLY2 pin sets the delay time. If no delay time is required these pins can be left open. To set the delay time the external capacitor connected to DLY1 and DLY2 is charged with a constant current source of typically 5 µA. The delay time is terminated when the capacitor voltage has reached the internal reference voltage of V_{REF}=1.280 V. The external delay capacitor is calculated using Equation 1:

$$C_{dly} = \frac{5\,\mu A \times t_d}{V_{REF}} = \frac{5\,\mu A \times t_d}{1.280\,V} \quad (1)$$

where t_d = Desired delay time

Example for setting a delay time of 5.3 ms:

$$C_{dly} = \frac{5\ \mu A \times 5.3\ ms}{1.280\ V} = 20.7\ nF \approx 22\ nF \quad (2)$$

APPLICATION INFORMATION (continued)

BOOST CONVERTER

The TPS65162 boost converter block is shown in Figure 21. The boost converter operates with PWM (Pulse Width Modulation) at a fixed switching frequency of 500 kHz or 750 kHz, selected by the FREQ pin. The converter uses an unique fast-response, voltage-mode controller scheme with input-voltage feedforward. This achieves excellent line and load regulation (0.03%/A load regulation typical), and allows the use of small external components. To add more flexibility to the selection of external component values, the device uses external loop compensation. Although the boost converter looks like a non-synchronous boost converter topology operating in discontinuous-conduction mode under a light load, the TPS65162 remains in continuous-conduction mode even under light load currents. (Figure 4) This is achieved with a novel architecture using an external Schottky diode with an integrated MOSFET in parallel connected between the SW pin and the SUP pin. This MOSFET allows the current to go below ground, which is the case under light load conditions. For this use, a small integrated P-Channel MOSFET (Q2) with typically 9 Ω RDSon is sufficient. When the inductor current is positive, the external Schottky diode, with the lower forward voltage, carries the current. This causes the converter to operate with a fixed frequency in continuous-conduction mode over the entire load-current range. This avoids ringing on the switch pin as seen with a standard non-synchronous boost converter, and allows a simpler compensation circuit for the boost converter.

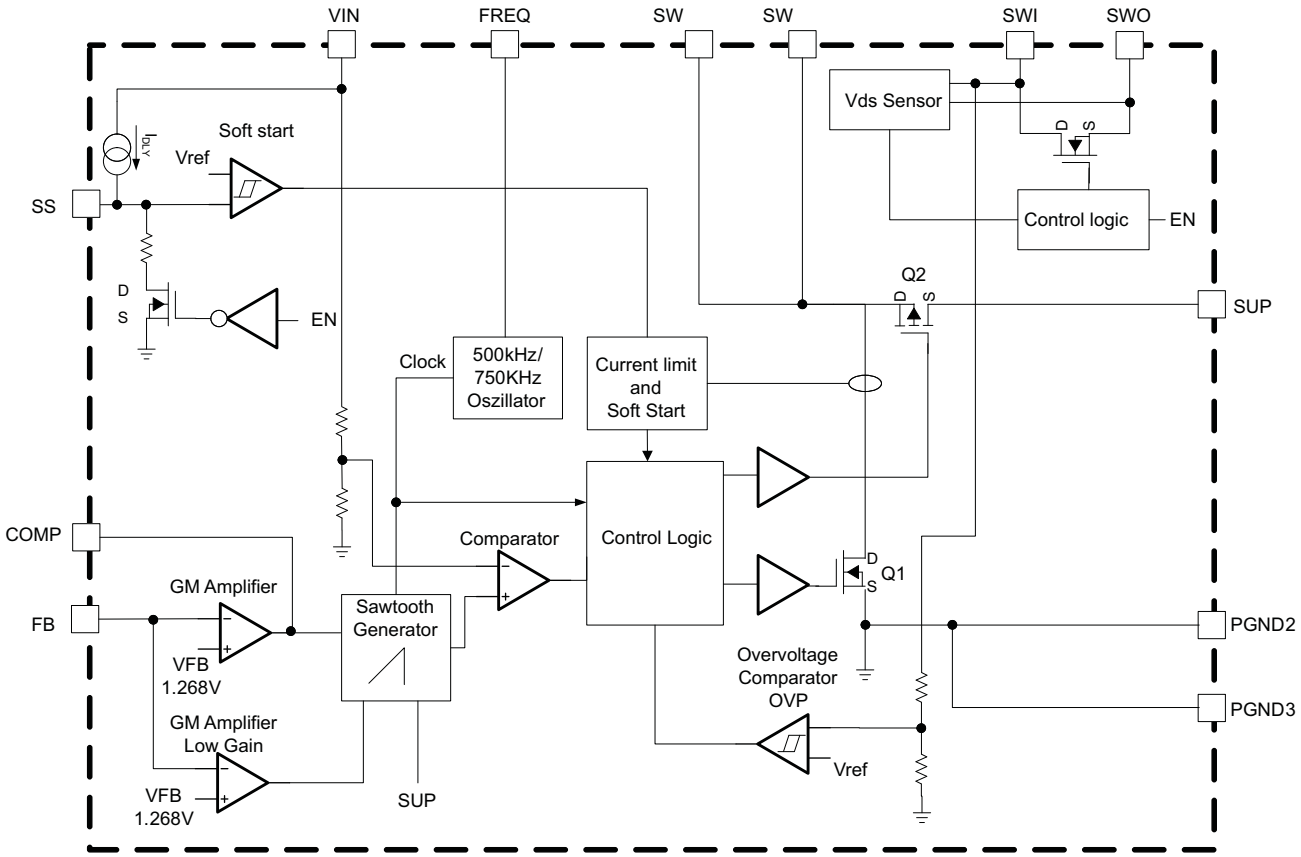


Figure 21. Boost Converter Block TPS65162

APPLICATION INFORMATION (continued)

Soft Start

To minimize inrush current during startup, the boost converter has an adjustable soft-start, and the input-to-output isolation switch has current-limit control. The current limit of the input-to-output isolation switch is slowly ramped up for a soft turn-on. The VDS sensor of the input-to-output isolation switch monitors the voltage difference between SWI and SWO, and controls the current through the isolation switch. With VDS = 12 V, the current-limit threshold through the isolation switch is typically 330 mA. This current-limit threshold will linearly increase by factor of two till VDS reaches 3 V; current limiting is disabled when VDS is below 3 V. The boost converter is enabled when VDS is below 0.5 V. An external capacitor connected to the soft-start pin, SS, is used to slowly ramp up the internal switch current limit of the boost converter. The capacitor connected to the SS pin is charged with a constant current that increases the voltage on the SS pin. The internal current limit is proportional to the voltage on the SS pin. When the threshold voltage of the internal-switch soft-start comparator is reached, the full current limit is released. The larger the soft-start capacitor value, the longer the soft-start time. A 22-nF capacitor is usually sufficient for typical applications.

Overvoltage Protection

The boost converter has an overvoltage-protection circuit to prevent the switch voltage from exceeding the absolute-maximum switch voltage rating in the event of a system fault. The device protects itself if the feedback pin is connected to ground or floated, and clamps the voltage of the output of the boost converter to 20 V. To implement the overvoltage protection, the overvoltage comparator shown in Figure 21 monitors the output voltage via the SWI pin. As soon as the output voltage exceeds the overvoltage threshold (typically 20 V), the device stops switching until the output voltage drops below the comparator threshold again. The typical waveform when the device is in overvoltage protection is shown in Figure 7.

Short CIrcuit Protection

The boost converter has a short-circuit protection circuit to prevent the inductor or rectifier diode from overheating when the output is shorted. The VDS sensor in the input-to-output isolation switch monitors the voltage difference between SWI and SWO. If the boost output is shorted, and the voltage difference between SWI and SWO exceeds the threshold (typically 1.4 V in full operation), then the boost converter shuts down, and the input-to-output isolation switch limits VS current.

Input Capacitor Selection (VIN, SUP)

Low ESR ceramic capacitors are recommended for good input-voltage filtering. The TPS65162 has an analog input (VIN) as well as a power supply input (SUP) powering all the internal rails. A 1-µF bypass capacitor is required as close as possible from VIN to GND, and from SUP to GND. Depending on the overall load current, two or three 22-µF input capacitors are required. For better input-voltage filtering, the input capacitor values can be increased. Refer to Table 1 and the *Typical Applications* schematic for input capacitor recommendations.

Table 1. Input Capacitor Selection

CAPACITOR	COMPONENT SUPPLIER	COMMENTS
22 µF / 16 V	Taiyo Yuden EMK316BJ226ML	Pin VIN, PVIN
2 ×10 µF / 25 V	Taiyo Yuden TMK316BJ106KL	Pin VIN, PVIN (Alternative)
1 µF / 35 V	Taiyo Yuden GMK107BJ105KA	Pin SUP, AVIN, VIN
1 µF / 25 V	Taiyo Yuden TMK107BJ105KA	Pin SUP, AVIN, VIN

Frequency Select Pin, FREQ

The frequency-select pin FREQ selects the switching frequency of the entire device to 500 kHz (FREQ=low) or 750 kHz (FREQ=high). A lower switching frequency gives a higher efficiency with a slightly reduced load-transient regulation.

Boost Converter Design Procedure

The first step in the design procedure is to verify whether the maximum possible output current of the boost converter supports the specific application requirements. To simplify the calculation, the fastest approach is to estimate the converter efficiency, by taking the efficiency numbers from the provided efficiency curves, or to use a worst-case assumption for the expected efficiency, e.g., 80%. With the efficiency number it is possible to calculate the steady-state values of the application.

1. Converter Duty Cycle: $$D = 1 - \frac{Vin \times \eta}{Vout}$$

2. Maximum output current: $$Iout = \left(Isw - \frac{Vin \times D}{2 \times fs \times L}\right) \times (1 - D)$$

3. Peak switch current: $$I_{swpeak} = \frac{Vin \times D}{2 \times fs \times L} + \frac{I_{out}}{1 - D}$$

With Isw = converter switch current (minimum switch current limit = 2.8 A)

fs = converter switching frequency (typical 500kHz or 750 kHz)

L = Selected inductor value

η = Estimated converter efficiency (use the number from the efficiency curves or 0.8 as an estimation)

The peak switch current is the steady-state peak switch current that the integrated switch, inductor and external Schottky diode must be able to handle. The calculation must be done for the minimum input voltage where the peak switch current is highest.

Inductor Selection

The TPS65162 typically operates with a 10-µH inductor. The main parameter for inductor selection is the inductor saturation current, which should be higher than the peak switch current, as calculated above, with additional margin to handle heavy load transients. An alternative more conservative approach is to choose an inductor with a saturation current at least as high as the typical switch current limit of 3.6 A. The second important parameter is the inductor DC resistance. Usually, the lower the DC resistance, the higher the efficiency of the converter. The choice of inductor can affect converter efficiency by as much as 10%. Example inductors are shown in Table 2.

Table 2. Inductor Selection (Boost Converter)

INDUCTOR VALUE	COMPONENT SUPPLIER	DIMENSIONS in mm	Isat/DCR
10 µH	Coilcraft DO3316P-103	12.95 × 9.4 × 5.51	3.9 A / 38 mΩ
10 µH	Sumida CDRH8D43-100	8.3 × 8.3 × 4.5	4.0 A / 29 mΩ
10 µH	Wuerth Elektronik 744066100	10 × 10 × 3.8	4.0 A / 25 mΩ

Output Capacitor

For best output-voltage filtering, a low-ESR output capacitor is recommended. Ceramic capacitors have a low ESR value and work best with the TPS65162. One 10-µF ceramic output capacitor before the input-to-output isolation switch, SWI, and six 10-µF or three 22-µF ceramic output capacitors in parallel after the input-to-output isolation switch, SWO, are sufficient for most applications. To improve the load transient regulation, add more capacitors after the input-to-output isolation switch. Refer to Table 3 for the selection of the output capacitor.

Table 3. Output Capacitor Selection

CAPACITOR	COMPONENT SUPPLIER	COMMENTS
10 µF/25 V	Taiyo Yuden TMK316BJ106KL	
22 µF/25 V	TDK C4532X7R1E226M	Alternative solution

Rectifier Diode Selection

To achieve high efficiency, a Schottky diode should be used. The reverse voltage rating should be higher than the maximum output voltage of the converter. The current rating for the Schottky diode is calculated as the off time of the converter times the typical switch current of the TPS65162:

$$I_{avg} = (1-D)\cdot I_{SW} = \frac{V_{in}}{V_{out}} \times 3.6\,A \quad (3)$$

where I_{SW}=typical switch current of the TPS65162 (3.6 A)

A Schottky diode with 2-A maximum average rectified forward current rating is sufficient for most applications. The Schottky rectifier must have adequate power dissipation. The dissipated power is the average rectified forward current times the diode forward voltage.

$$P_D = I_{avg}\cdot V_F = I_{SW}\cdot(1-D)\cdot V_F \quad (4)$$

where I_{SW}=typical switch current of the TPS65162 (3.6 A)

Table 4. Rectifier Diode Selection (Boost Converter)

Iavg	Vr	$V_{forward}$	$R_{\theta JA}$	SIZE	COMPONENT SUPPLIER
3 A	20 V	0.36 at 3 A	46°C/W	SMC	MBRS320, International Rectifier
2 A	20 V	0.44 V at 2 A	75°C/W	SMB	SL22, Vishay Semiconductor
2 A	20 V	0.5 at 2 A	75°C/W	SMB	SS22, Fairchild Semiconductor

Setting the Output Voltage and Selecting the Feedforward Capacitor

The output voltage is set by the external resistor divider and is calculated as:

$$V_{out} = 1.268\ V \times \left(1 + \frac{R1}{R2}\right) \quad (5)$$

Across the upper resistor a bypass capacitor is required to speed up the circuit during load transients. The capacitor is caluculated as:

$$C_{ff} = \frac{1}{2\cdot\pi\cdot f_z \cdot R1} \quad (6)$$

Depending on the inductor value, the zero frequency needs to be set. f_z is 19 kHz for a 10 µH inductor, and 9 kHz for a 22 µH inductor. A value coming closest to the calculated value should be used.

Compensation (VC)

The regulator loop can be compensated by adjusting the external components connected to the VC pin. The VC pin is the output of the internal transconductance error amplifier. A single capacitor connected to this pin sets the low frequency gain. A 22-nF capacitor is usually sufficient for most applications.

POSITIVE CHARGE PUMP

The positive charge pump provides a regulated output voltage set by the external resistor divider. The TPS65162 positive charge pump block is shown in Figure 22.

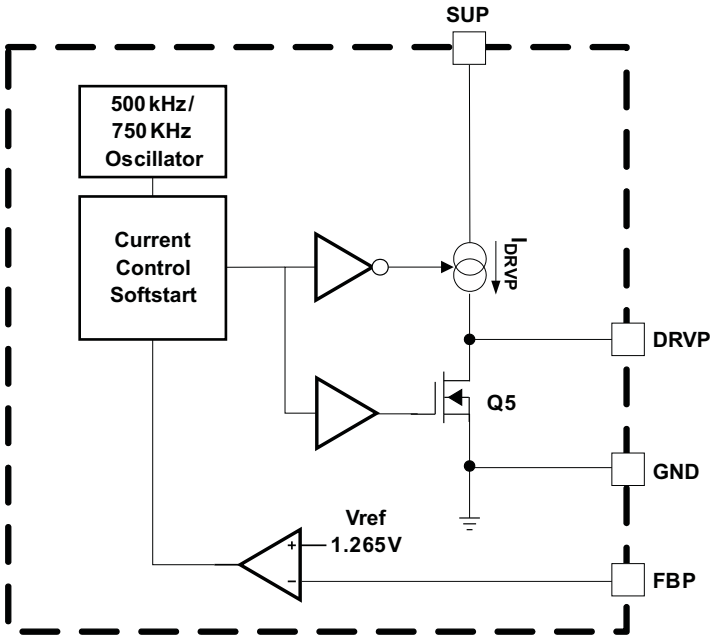


Figure 22. Positive Charge Pump Block TPS65162

Since the flying capacitor-voltage sits on top of the drive-pin voltage, the maximum output voltage is $V_{SUP}+V_S-V_{drop}$. V_{drop} is the voltage drop across the external diodes and internal charge pump MOSFETs. If higher output voltages are required, another charge pump stage can be added to the output.

Setting the output voltage:

$$V_{out} = V_{REF} \times \left(1 + \frac{R5}{R6}\right) = 1.265\ V \times \left(1 + \frac{R5}{R6}\right) \quad (7)$$

To minimize noise and leakage current sensitivity, we recommend a value of approximately 20 kΩ for the lower feedback divider resistor R6.

NEGATIVE CHARGE PUMP

The negative charge pump provides a regulated output voltage set by the external resistor divider. The TPS65162 negative charge pump block is shown in Figure 23. The negative charge pump operates very similar to the positive charge pump, with the difference that it runs from the input voltage VIN. The maximum negative output voltage is VGL=(–VIN)+V_{drop}. V_{drop} is the voltage drop across the external diodes and internal charge-pump MOSFETs.

The output voltage is calculated by:

$$V_{out} = -V_{REF} \times \frac{R3}{R4} = -1.265\ V \times \frac{R3}{R4} \quad (8)$$

Since the reference-output driver current should not exceed 30uA (typical), the lower feedback resistor value R4 should be in a range of 40 kΩ to 120 kΩ. Overall feedback resistance should be in the range from 500 kΩ to 1 MΩ. The negative charge pump requires two external Schottky diodes. The peak current rating of the Schottky diode must be twice the load current of the output. For a 20-mA output current, the dual Schottky diode BAV99 is a good choice.

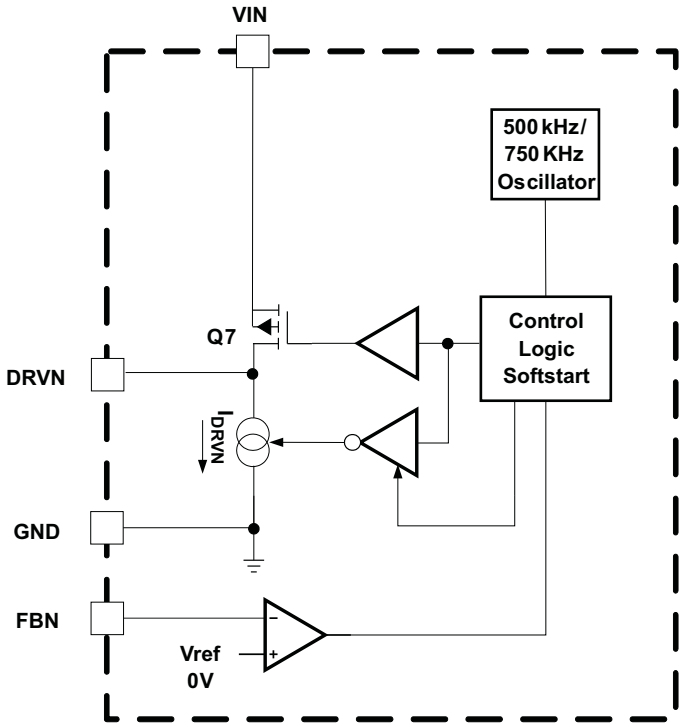


Figure 23. Negative Charge Pump Block TPS65162

GATE VOLTAGE SHAPING

The gate voltage shaping reduces the flickering effect of an LCD panel, and isolates VGHM from the source voltage VGH. For correct operation of this block, it is not recommend to connect an output capacitor to VGHM. To reduce the voltage ripple on VGHM, add more capacitors on VGH. The TPS65162 gate voltage shaping block is shown in Figure 24. The corresponding timing diagram is shown in Figure 26. The gate voltage shaping block responds to VFLK under the following conditions:

- The device is enabled with VDPM = high
- The input voltage is above the undervoltage lockout
- The positive charge pump is in regulation

When VGH is pulled below its power-good level, Q1 and Q2 are turned off and VGHM is discharged via the 1-kΩ resistor over Q3. With VFLK = high, Q1 and Q4 are turned on and Q2 is turned off. VGH is present at VGHM when Q1 is on, and at the same time, the capacitor connected to the CE pin is discharged by Q4 to

GND. When VFLK is taken low, Q4 is turned off, and the capacitor connected to the CE pin is charged by a constant current source, typically 60 μA. When the capacitor voltage reaches the internal reference voltage of 1.284 V and VFLK is low, Q1 is turned off and Q2 is turned on. With Q2 on, VGHM is discharged by the resistor connected to the RE pin. Once VGHM is discharged to five times VDD, Q2 is turned off and VGHM is high impedance. In the application of not using this function, connect VDPM, VFLK with high.

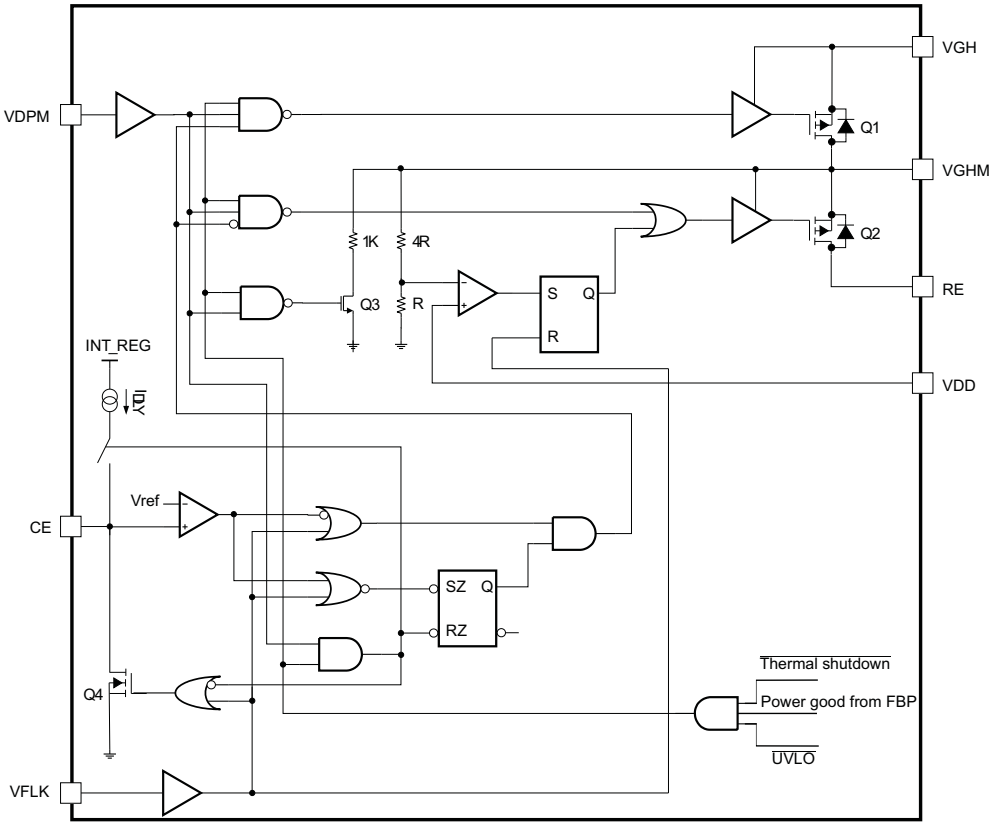


Figure 24. Gate Voltage Shaping Block TPS65162

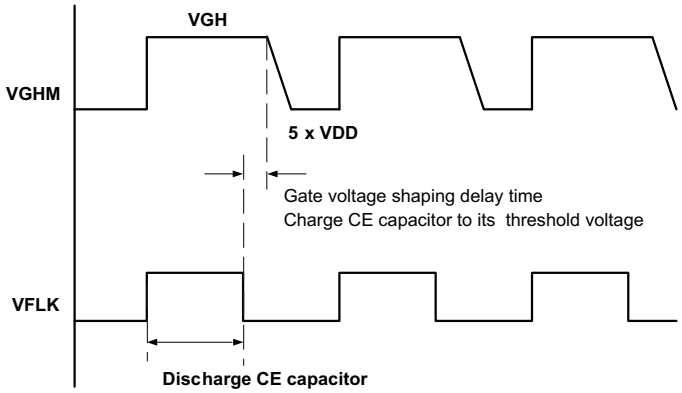


Figure 25. Gate Voltage Shaping Block TPS65162

STEP-DOWN CONVERTER

The TPS65162 step down converter block is shown in Figure 26. The non-synchronous step down converter operates at a fixed switching frequency using a fast response voltage mode topology with input voltage feedforward. This topology allows simple internal compensation and it is designed to operate with ceramic output capacitors. The converter drives an internal 2.8 A N-Channel MOSFET switch. The MOSFET driver is referenced to the switch pin SWB. The N-Channel MOSFET requires a gate drive voltage higher than the switch pin to turn the N-Channel MOSFET on. This is accomplished by a boost strap gate drive circuit running of the step down converter switch pin. When the switch pin SWB is at ground the boot strap capacitor is charged to 8 V. This way the N-Channel Gate drive voltage is typically around 8 V.

Soft Start

To avoid high inrush current during startup, an internal soft-start is implemented. When the step down converter is enabled over EN1, its reference voltage slowly rises from zero to its power good threshold of typically 90% of Vref. When the reference voltage reaches this power good threshold, the Error amplifier is released to its normal operation with its normal duty cycle. To further limit the inrush current during soft-start the converter frequency is set to 1/4 of the switching frequency fs and 1/2 of fs by the comparator that monitors the feedback voltage. refer to the internal block diagram. The typical soft-start is typically completed within 1ms.

Short Circuit Protection

To limit the short circuit current, the device has a cycle-by-cycle current limit. To prevent the short-circuit current from rising above the internal current limit when the output is shorted to GND, the switching frequency is reduced as well. This is implemented by two comparators monitoring the feedback voltage. The step-down converter switching frequency is reduced to 1/2 of $f$fs when the feedback is below 0.9 V, and 1/4 of the switching frequency when the feedback voltage is below 0.6 V.

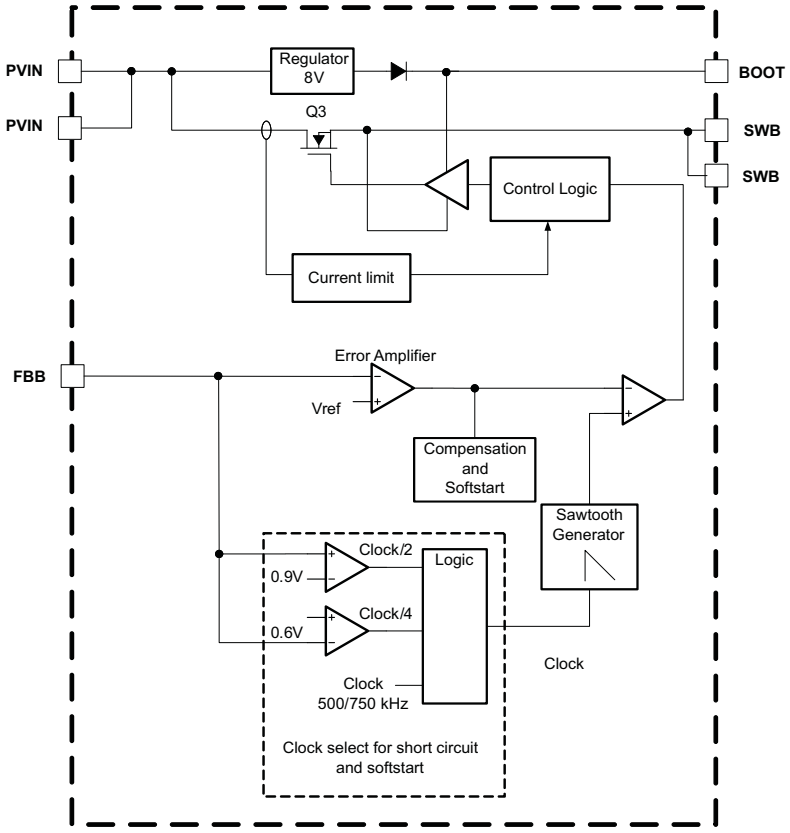


Figure 26. Step Down Converter Block TPS65162

Setting the Output Voltage

The step-down converter uses an external voltage divider to set the output voltage. The output voltage is calculated as:

$$V_{out} = 1.265\ V \times \left(1 + \frac{R5}{R6}\right) \quad (9)$$

At load currents <1 mA, the device operates in discontinuous conduction mode. When the load current is reduced to zero the output voltage rises slightly above the nominal output voltage. At zero load current, the device skips clock cycles, but does not completely stop switching, thus the output voltage sits slightly above the nominal output voltage. Therefore, the lower feedback resistor is selected to be around 1.2 kΩ to maintain around 1 mA minimum load current.

Selecting the Feedforward Capacitor

The feedforward capacitor across the upper feedback resistor divider forms a zero around 135 kHz, and is calculated as:

$$C_z = \frac{1}{2 \times \pi \times 135kHz \times R5} = \frac{1}{2 \times \pi \times 135kHz \times 2.5k\Omega} = 471.6\ pF \approx 470\ pF \quad (10)$$

Usually the standard capacitor value closest to the calculated value is selected.

Inductor Selection

The TPS65162 step-down converter typically operates with a 10-µH inductor. For high efficiency, the inductor should have a low DC resistance to minimize conduction loss. This must be considered when selecting the appropriate inductor. In order to avoid inductor saturation, the inductor should be rated at least for the maximum output current of the converter plus the inductor ripple current that will be calculated by:

$$\Delta I_L = Vout \times \frac{1 - \frac{Vout}{Vin}}{L \times f} \qquad I_{Lmax} = I_{outmax} + \frac{\Delta I_L}{2} \quad (11)$$

where

f = Switching Frequency (750 kHz, 500 kHz minimal)
L = Inductor Value (typically 10 µH)
ΔI_L= Peak to Peak inductor ripple current
I_{Lmax} = Maximum Inductor current

The highest inductor current occurs at maximum Vin. A more conservative approach is to select the inductor current rating just for the typical switch-current limit of 3.5 A.

Table 5. Inductor Selection

INDUCTOR VALUE	COMPONENT SUPPLIER	DIMENSIONS in mm	Isat/DCR
10 µH	Coilcraft DO3316P-103	12.95 × 9.4 × 5.51	3.9 A/38 mΩ
10 µH	Sumida CDRH8D43-100	8.3 × 8.3 × 4.5	4.0 A/29 mΩ
10 µH	Wuerth Elektronik 744066100	10 × 10 × 3.8	4.0 A/25 mΩ

Rectifier Diode Selection

To achieve high efficiency, a Schottky diode should be used. The reverse voltage rating should be higher than the maximum output voltage of the step-down converter. The averaged rectified forward current for which the Schottky diode should be rated is calculated as the off time of the step-down converter times the minimum switch current of the TPS65162:

$$D = \frac{V_{OUT}}{V_{IN}} \quad (12)$$

$$I_{avg} = (1-D)\cdot I_{SW} = (1-\frac{V_{OUT}}{V_{IN}})\cdot 2.8\,A \quad (13)$$

where Isw = minimum switch current of the TPS65162 (2.8 A)

Usually a Schottky diode with 2 A maximum average rectified forward current rating is sufficient for most of the applications. Secondly the Schottky rectifier has to be able to dissipate the power. The dissipated power is the average rectified forward current times the diode forward voltage.

$P_D = I_{avg} \times V_F = Isw \times (1 - D) \times V_F$ with I_{SW} = minimum switch current of the TPS65162 (2.8 A)

Table 6. Rectifier Diode Selection (Step-Down Converter)

CURRENT RATING Iavg	Vr	$V_{forward}$	$R_{\theta JA}$	SIZE	COMPONENT SUPPLIER
3 A	20 V	0.36 V at 3 A	46°C/W	SMC	MBRS320, International Rectifier
2 A	20 V	0.44 V at 2 A	75°C/W	SMB	SL22, Vishay Semiconductor
2 A	20 V	0.5 V at 2 A	75°C/W	SMB	SS22, Fairchild Semiconductor

Output Capacitor Selection

The device is designed to work with ceramic output capacitors. Two 22-µF output capacitors are sufficient for most of the applications. Larger output capacitance improves the load transient response.

Table 7. Output Capacitor Selection Step-Down Converter

CAPACITOR	COMPONENT SUPPLIER	COMMENT
22 µF/6.3 V	Taiyo Yuden JMK212BJ226MG	

OPERATIONAL AMPLIFIER 1 AND 2

The TPS65162 has two integrated operational amplifiers. The operational amplifiers can be used as a gamma-correction buffer or as a VCOM buffer.

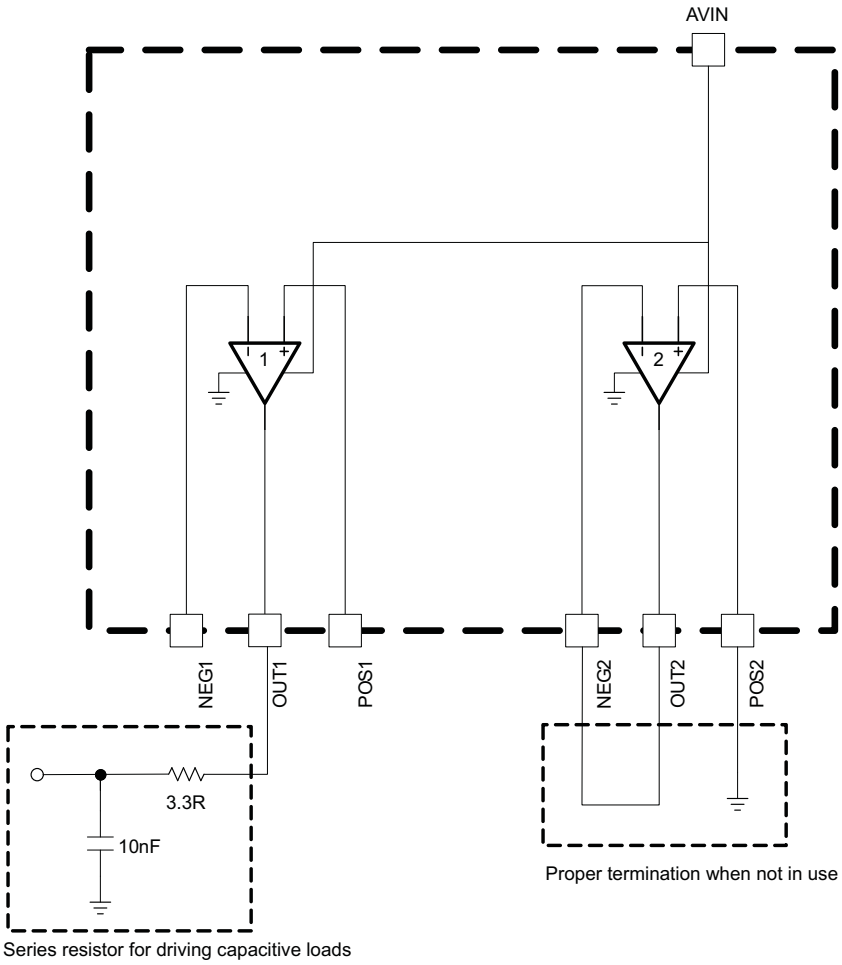


Figure 27. Operational Amplifier Block TPS65162

The power supply pin for the opamps is the AVIN pin connected to the boost converter Vs. To achieve good performance and minimize the output noise, a 1-µF bypass capacitor is required directly from the AVIN pin to ground. The opamps are not designed to drive capacitive loads, therefore it is not recommended to connect a capacitor directly to the output of the opamps. If capacitive loads are driven, use a series resistor at the output to provide stable operation. With a 3.3-Ω series resistor, a capacitive load of 10 nF can be driven, which is usually sufficient for typical LCD applications.

Operational Amplifier Termination

For some applications, not all of the amplifiers are used. To minimize device quiescent current the terminals should be terminated. The negative terminal is connected to the output of the operational amplifier and positive terminal is connected to GND and the output is left open. This termination minimizes device quiescent current and maintains correct functionality of the device.

PCB LAYOUT DESIGN GUIDELINES

1. Place the power components outlined in bold first on the PCB.
2. Rout the traces outlined in bold with wide PCB traces.
3. Place a 1-µF bypass capacitor directly from the SUP pin to GND and from AVIN to GND.

4. Use a short and wide trace to connect the SUP pin to the output of the boost converter Vs.
5. Place the 220-nF reference capacitor directly from REF to GND close to the IC pins.
6. The feedback resistor for the negative charge pump between FBN and REF should be >40 kΩ.
7. Use short traces for the charge-pump drive pin (DRVN) of VGL because the traces carry switching waveforms.
8. Solder the PowerPad™ of the QFN package to GND, and use thermal vias to lower the thermal resistance.
9. For more layout recommendations, refer to the TPS65162 evaluation module (EVM)

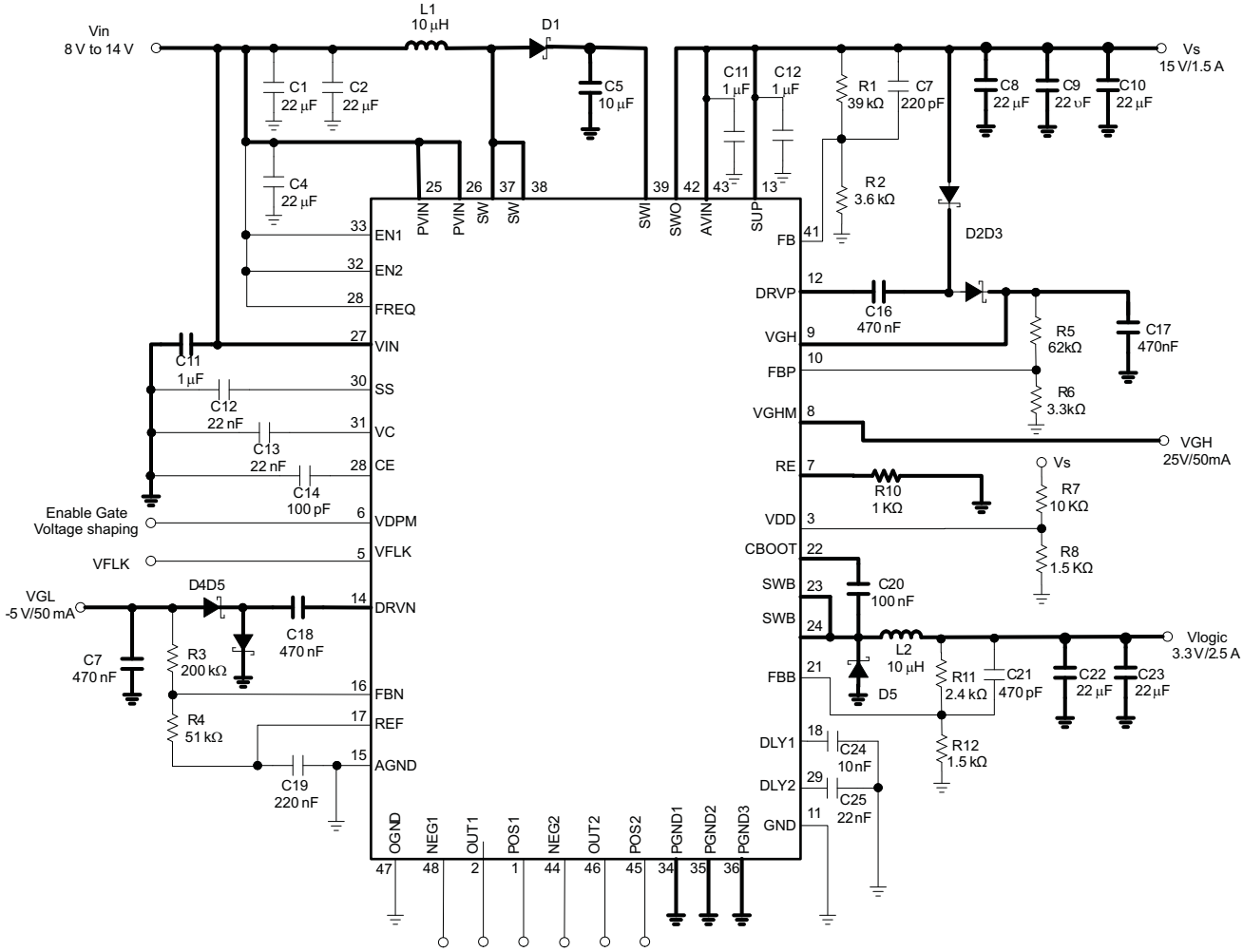
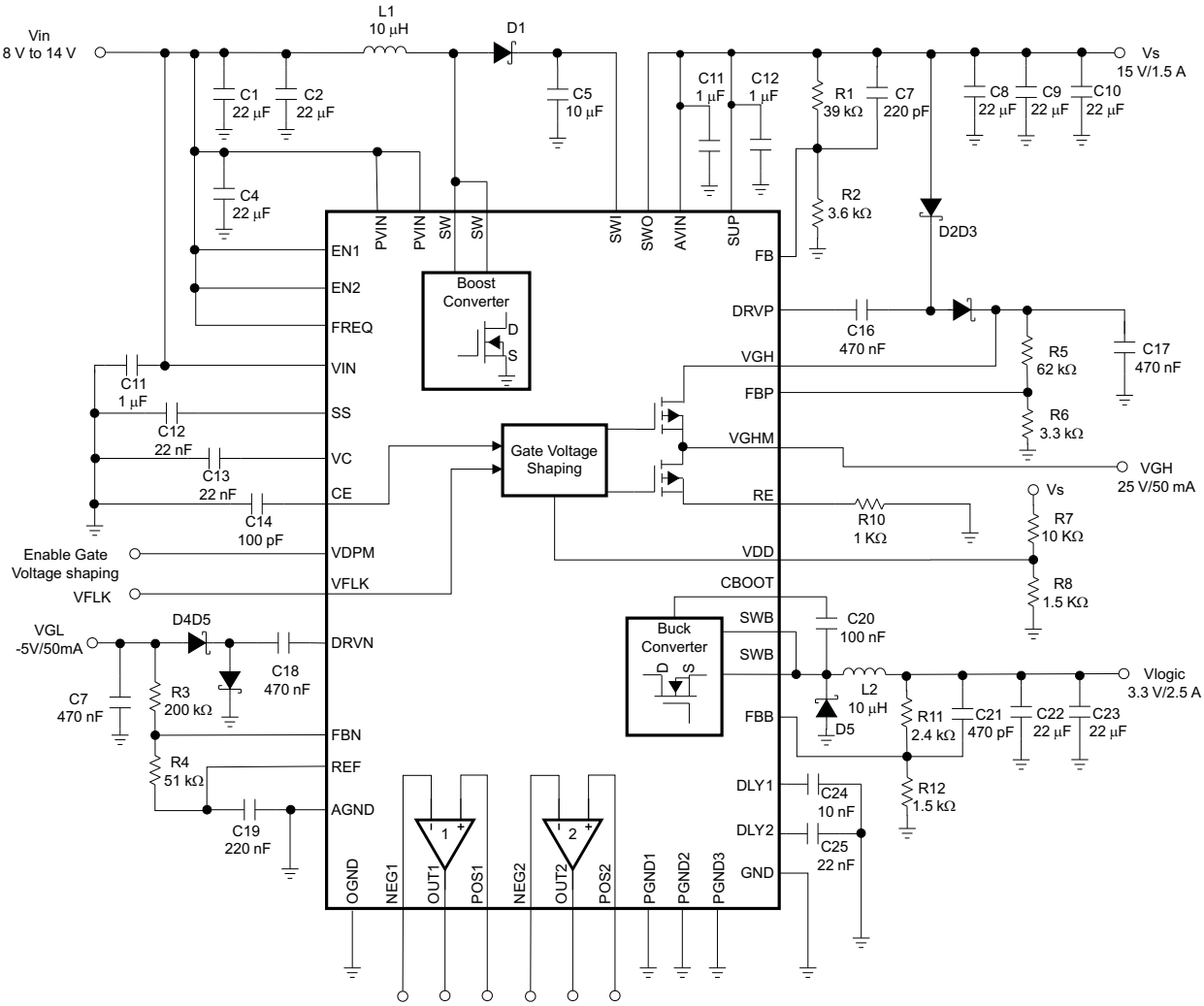
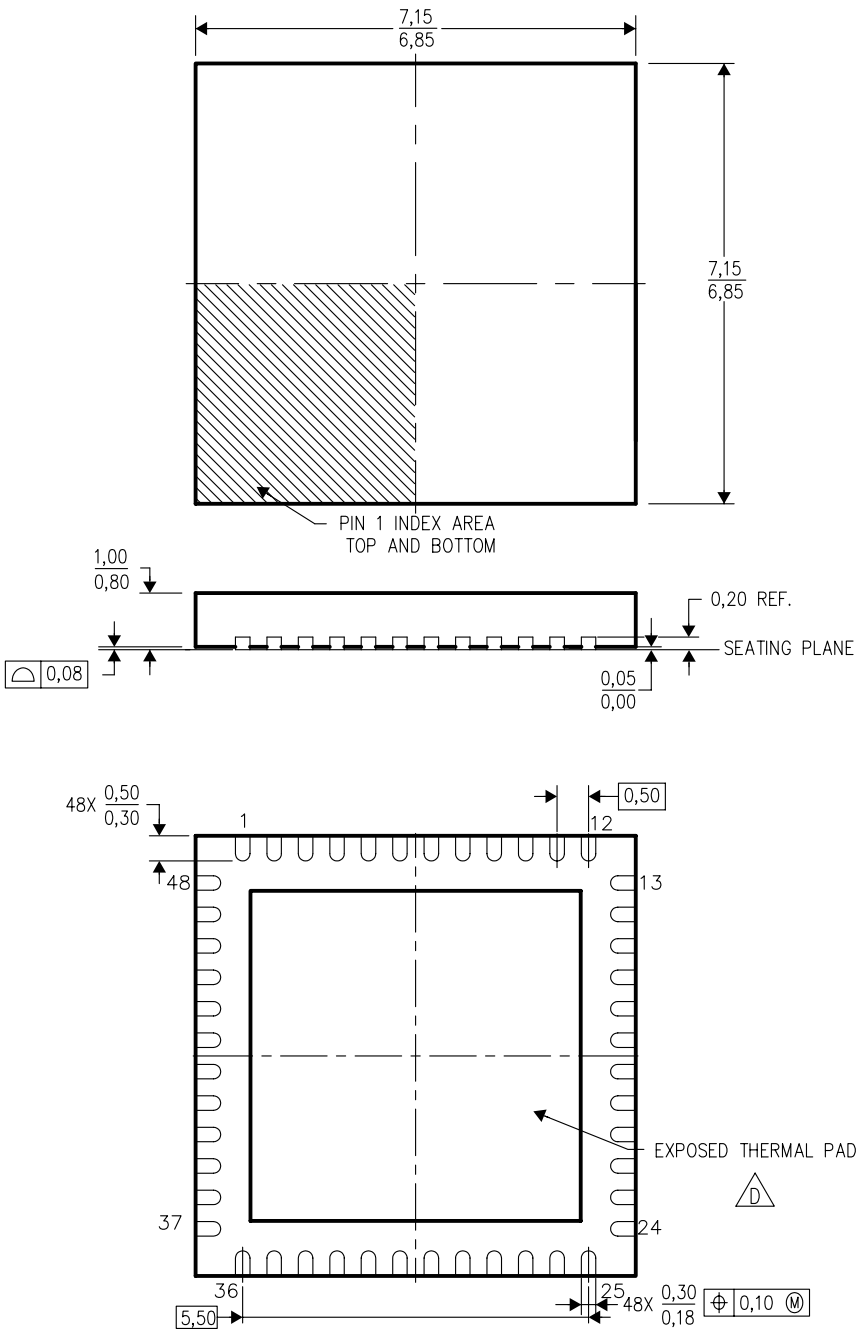


Figure 28. PCB Layout Recommendation TPS65162

TYPICAL APPLICATION



RGZ (S–PQFP–N48) PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MO–220.

THERMAL PAD MECHANICAL DATA

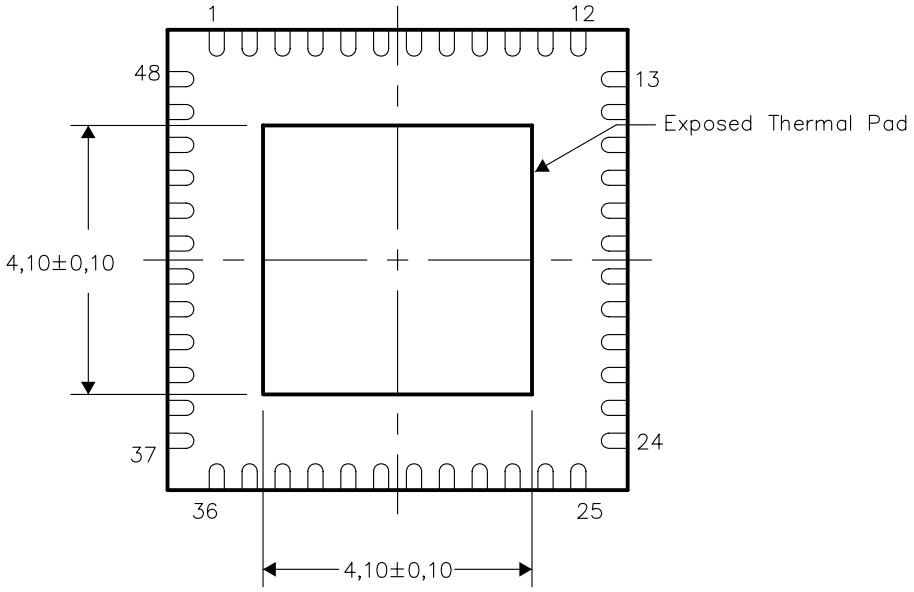
RGZ (S–PQFP–N48)

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to a ground or power plane (whichever is applicable), or alternatively, a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, Quad Flatpack No–Lead Logic Packages, Texas Instruments Literature No. SCBA017. This document is available at www.ti.com.

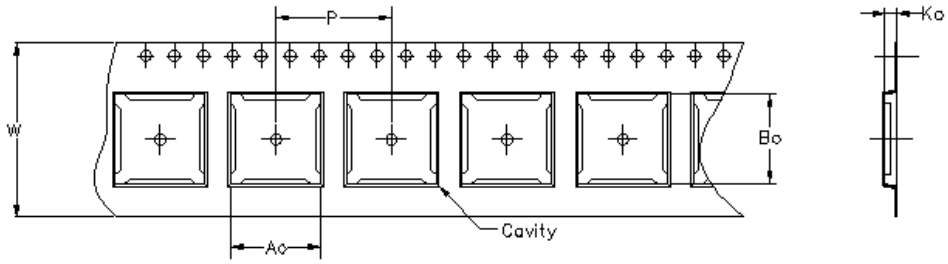
The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

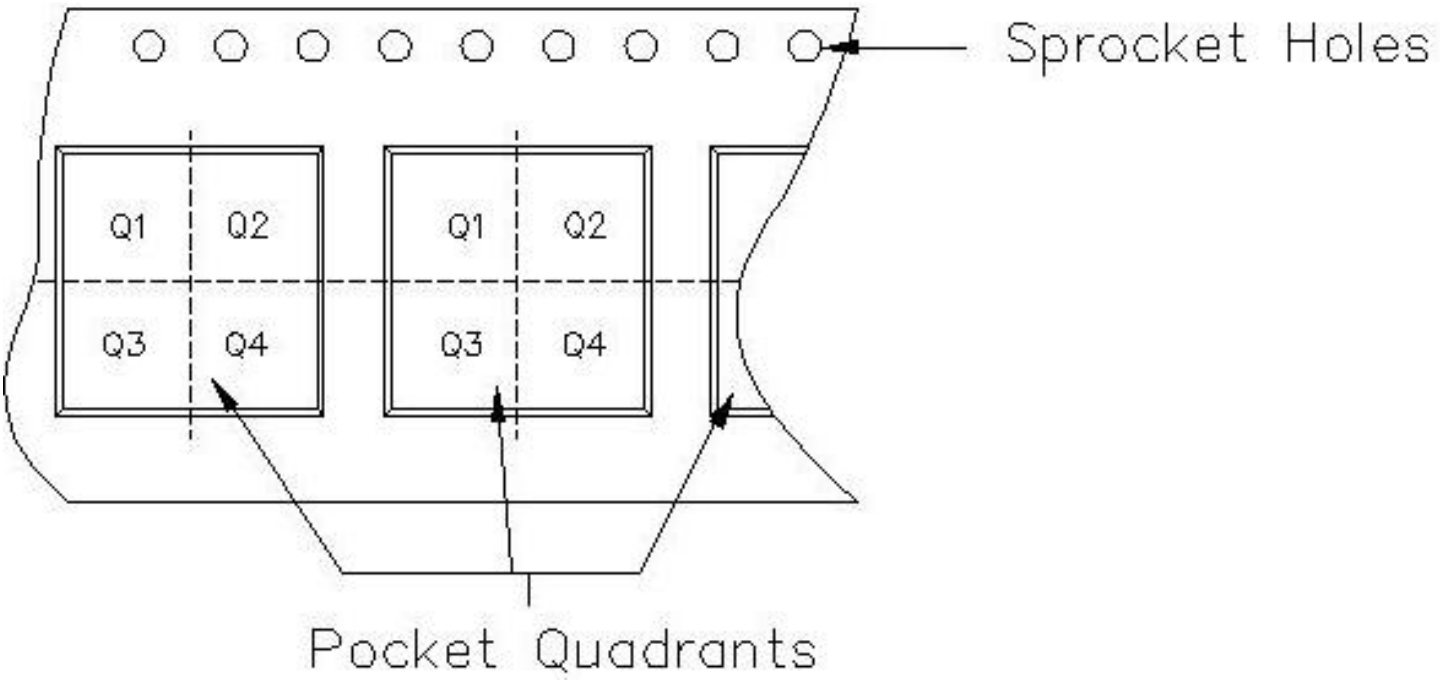
NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions



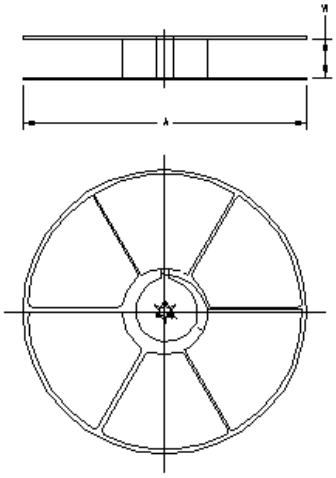
Carrier tape design is defined largely by the component lentgh, width, and thickness.

Ao = Dimension designed to accommodate the component width.
Bo = Dimension designed to accommodate the component length.
Ko = Dimension designed to accommodate the component thickness.
W = Overall width of the carrier tape.
P = Pitch between successive cavity centers.



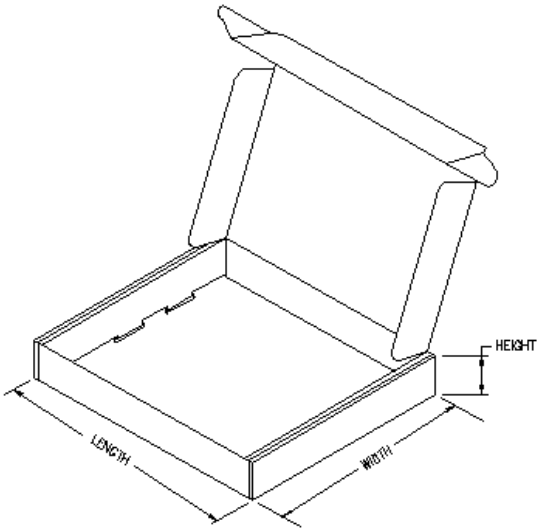
TAPE AND REEL INFORMATION

Device	Package	Pins	Site	Reel Diameter (mm)	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS65162RGZR	RGZ	48	FRB	330	16	7.3	7.3	1.5	12	16	Q2

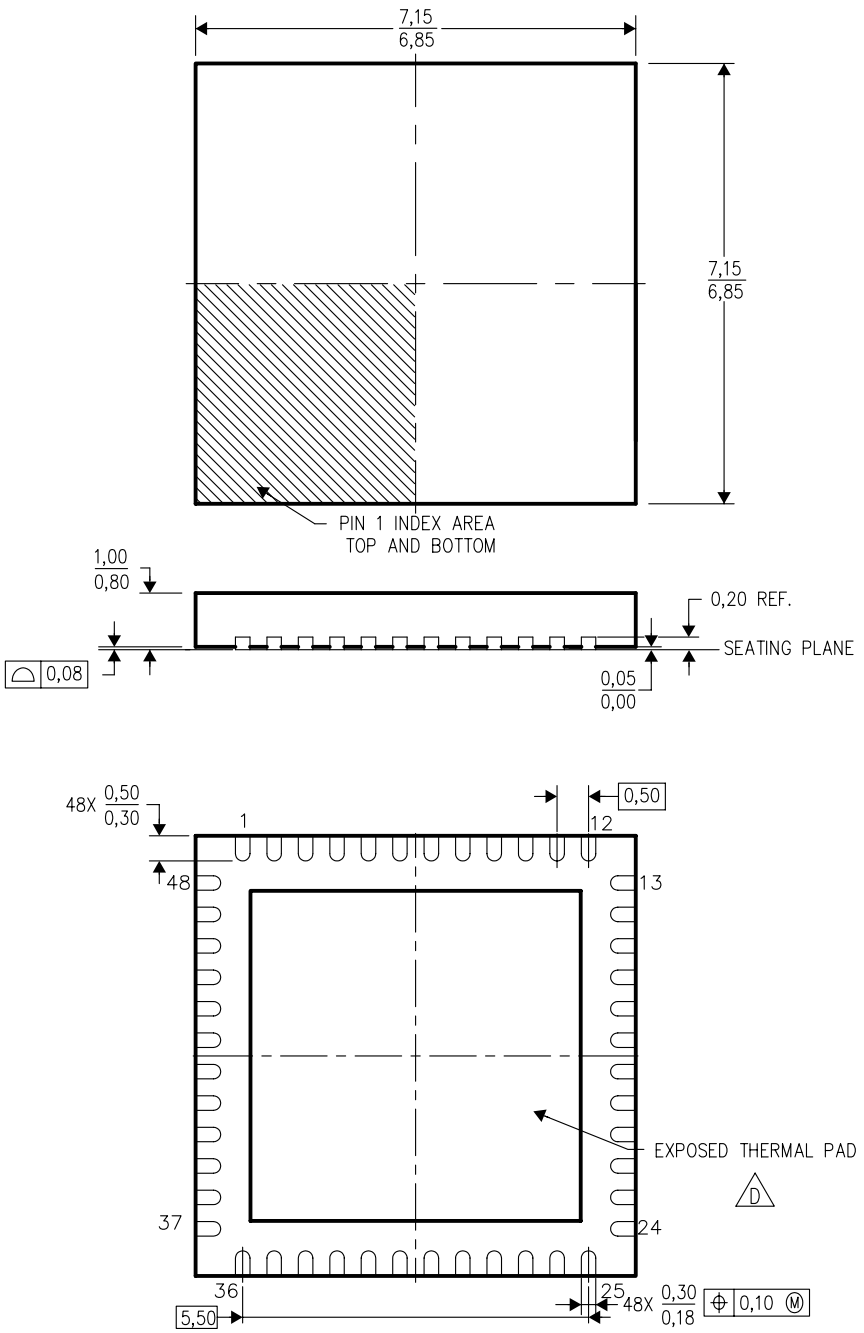


TAPE AND REEL BOX INFORMATION

Device	Package	Pins	Site	Length (mm)	Width (mm)	Height (mm)
TPS65162RGZR	RGZ	48	FRB	342.9	336.6	28.58



RGZ (S–PQFP–N48) PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MO–220.

THERMAL PAD MECHANICAL DATA

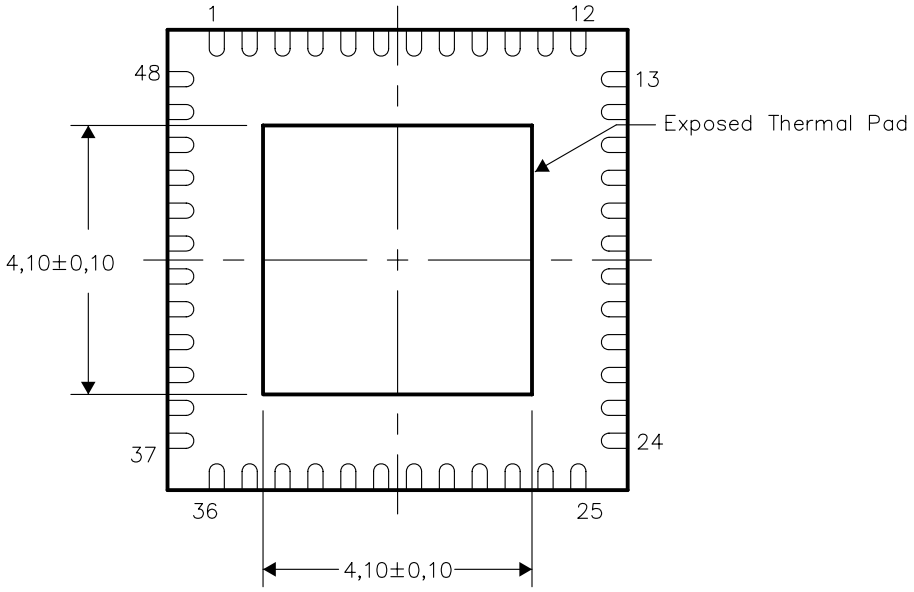
RGZ (S–PQFP–N48)

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to a ground or power plane (whichever is applicable), or alternatively, a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, Quad Flatpack No–Lead Logic Packages, Texas Instruments Literature No. SCBA017. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

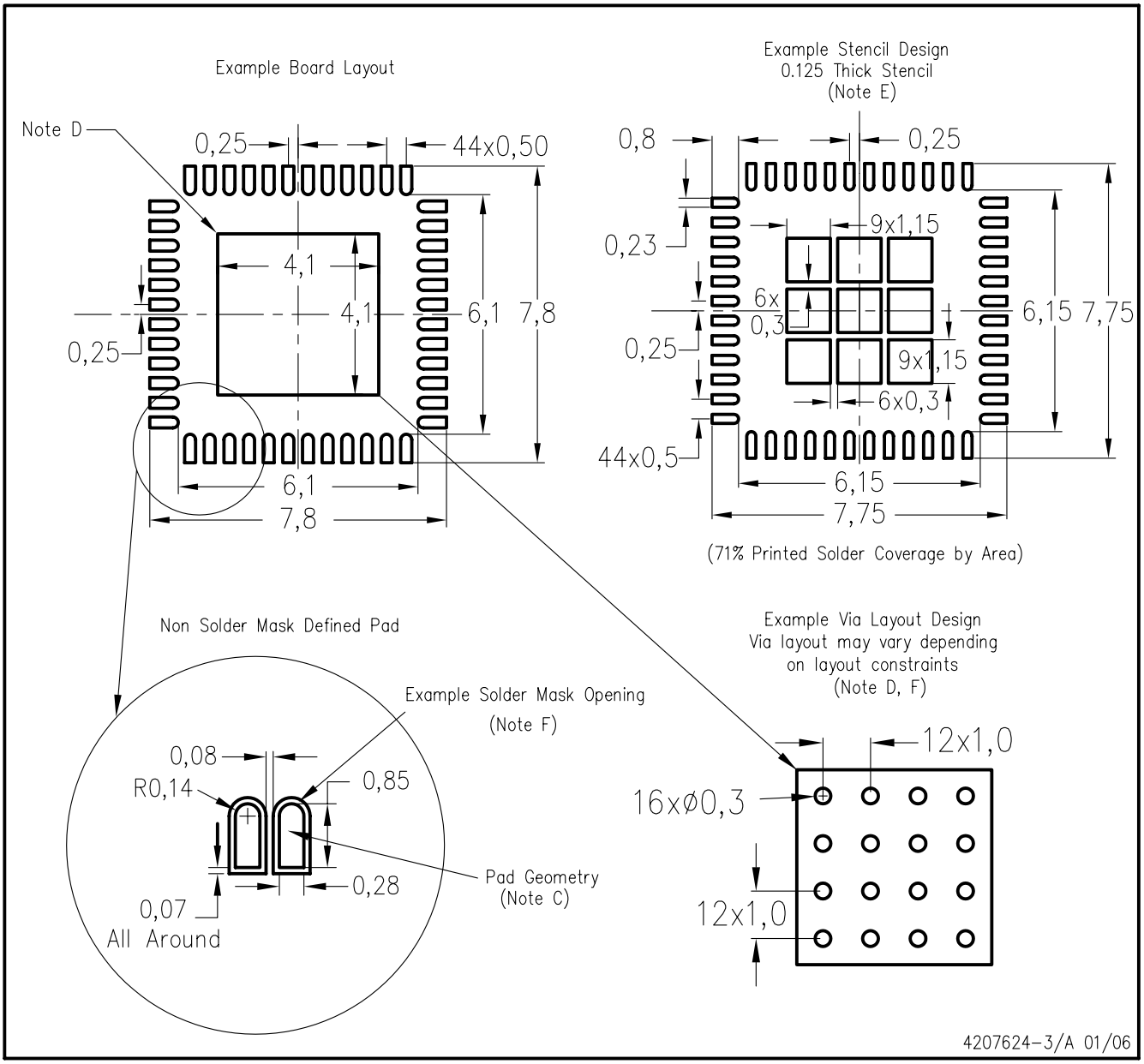


Bottom View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

RGZ (S–PQFP–N48)



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SCBA017, SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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