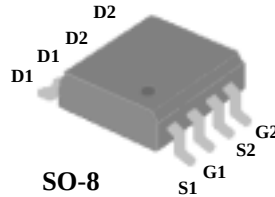


N AND P-CHANNEL ENHANCEMENT MODE POWER MOSFET

PRODUCT SUMMARY

Simple Drive Requirement
Low On-resistance
Fast Switching

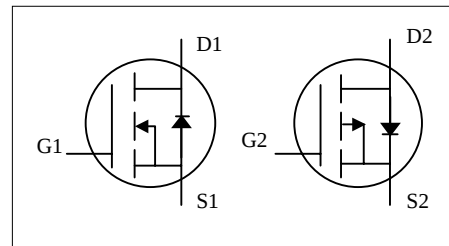


N-CH	BV_{DSS}	30V
	$R_{DS(ON)}$	50m Ω
	I_D	5A
P-CH	BV_{DSS}	-30V
	$R_{DS(ON)}$	70m Ω
	I_D	-4A

DESCRIPTION

The advanced power MOSFETs from Silicon Standard Corp. provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The SO-8 package is universally preferred for all commercial-industrial surface mount applications and suited for low voltage applications such as DC/DC converters.



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Rating		Units
		N-channel	P-channel	
V_{DS}	Drain-Source Voltage	30	-30	V
V_{GS}	Gate-Source Voltage	± 20	± 20	V
$I_D @ T_A = 25^\circ C$	Continuous Drain Current ³	5	-4	A
$I_D @ T_A = 70^\circ C$	Continuous Drain Current ³	4	-3.2	A
I_{DM}	Pulsed Drain Current ¹	20	-20	A
$P_D @ T_A = 25^\circ C$	Total Power Dissipation	2.0		W
	Linear Derating Factor	0.016		W/ $^\circ C$
T_{STG}	Storage Temperature Range	-55 to 150		$^\circ C$
T_J	Operating Junction Temperature Range	-55 to 150		$^\circ C$

THERMAL DATA

Symbol	Parameter	Value	Unit
$R_{thj-amb}$	Thermal Resistance Junction-ambient ³	Max. 62.5	$^\circ C/W$

N-CH ELECTRICAL CHARACTERISTICS

@T_j=25°C (unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250uA	30	-	-	V
$\Delta BV_{DSS} / \Delta T_j$	Breakdown Voltage Temperature Coefficient	Reference to 25°C, I _D =1mA	-	0.037	-	V/°C
R _{DS(ON)}	Static Drain-Source On-Resistance ²	V _{GS} =10V, I _D =5A	-	-	50	mΩ
		V _{GS} =4.5V, I _D =4.2A	-	-	70	mΩ
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250uA	1	-	3	V
g _{fs}	Forward Transconductance	V _{DS} =10V, I _D =5A	-	8	-	S
I _{DSS}	Drain-Source Leakage Current (T _j =25°C)	V _{DS} =30V, V _{GS} =0V	-	-	1	uA
	Drain-Source Leakage Current (T _j =70°C)	V _{DS} =24V, V _{GS} =0V	-	-	25	uA
I _{GSS}	Gate-Source Leakage	V _{GS} =±20V	-	-	±100	nA
Q _g	Total Gate Charge ²	I _D =5A	-	10.2	-	nC
Q _{gs}	Gate-Source Charge	V _{DS} =10V	-	1.2	-	nC
Q _{gd}	Gate-Drain ("Miller") Charge	V _{GS} =10V	-	3.4	-	nC
t _{d(on)}	Turn-on Delay Time ²	V _{DS} =10V	-	6	-	ns
t _r	Rise Time	I _D =1A	-	9	-	ns
t _{d(off)}	Turn-off Delay Time	R _G =6Ω, V _{GS} =10V	-	15	-	ns
t _f	Fall Time	R _D =10Ω	-	5.5	-	ns
C _{iss}	Input Capacitance	V _{GS} =0V	-	240	-	pF
C _{oss}	Output Capacitance	V _{DS} =25V	-	145	-	pF
C _{rss}	Reverse Transfer Capacitance	f=1.0MHz	-	55	-	pF

SOURCE-DRAIN DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
I _S	Continuous Source Current (Body Diode)	V _D =V _G =0V, V _S =1.2V	-	-	1.7	A
V _{SD}	Forward On Voltage ²	T _j =25°C, I _S =1.7A, V _{GS} =0V	-	-	1.2	V

P-CH ELECTRICAL CHARACTERISTICS

@T_j=25°C (unless otherwise specified)

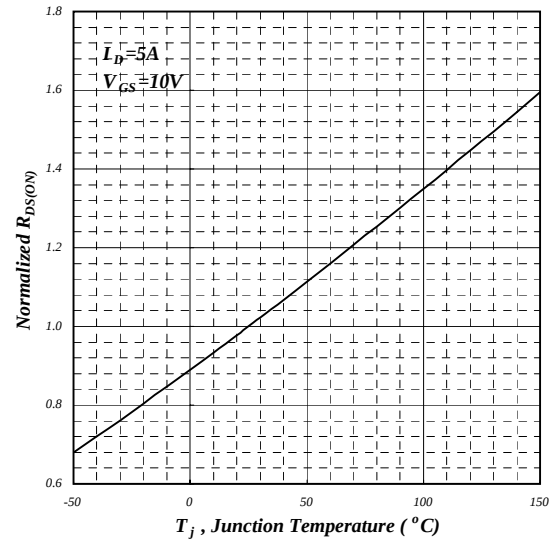
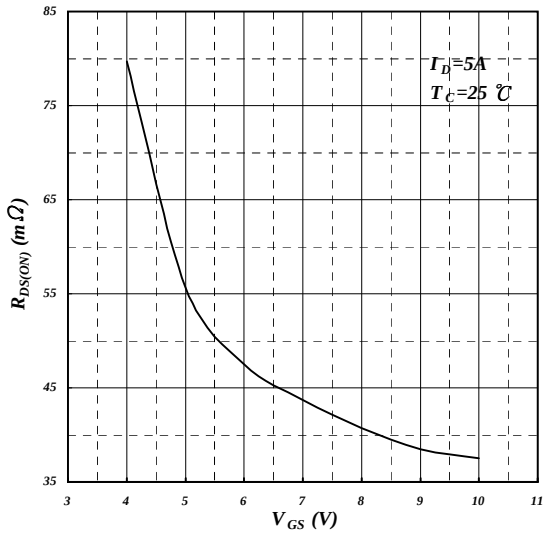
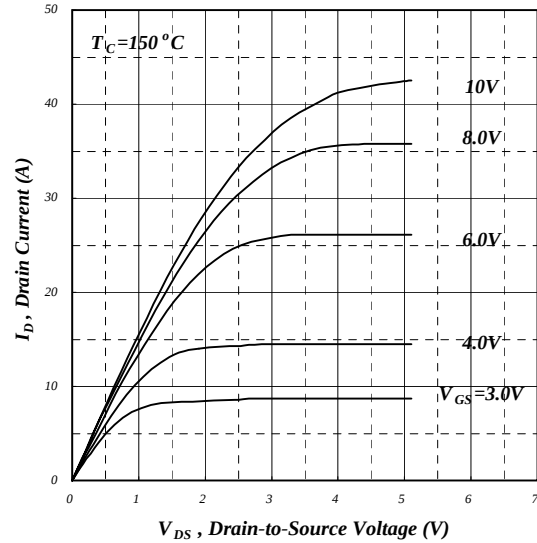
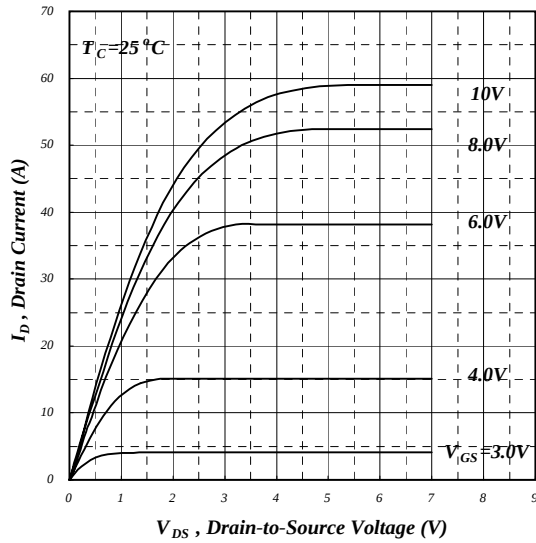
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250uA	-30	-	-	V
ΔBV _{DSS} /ΔT _j	Breakdown Voltage Temperature Coefficient	Reference to 25°C, I _D =-1mA	-	-0.028	-	V/°C
R _{DS(ON)}	Static Drain-Source On-Resistance ²	V _{GS} =-10V, I _D =-4A	-	-	70	mΩ
		V _{GS} =-4.5V, I _D =-3A	-	-	90	mΩ
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =-250uA	-1	-	-3	V
g _{fs}	Forward Transconductance	V _{DS} =-10V, I _D =-4A	-	5	-	S
I _{DSS}	Drain-Source Leakage Current (T=25°C)	V _{DS} =-30V, V _{GS} =0V	-	-	-1	uA
	Drain-Source Leakage Current (T=70°C)	V _{DS} =-24V, V _{GS} =0V	-	-	-25	uA
I _{GSS}	Gate-Source Leakage	V _{GS} = ± 20V	-	-	±100	nA
Q _g	Total Gate Charge ²	I _D =-4A	-	18.3	-	nC
Q _{gs}	Gate-Source Charge	V _{DS} =-10V	-	3.6	-	nC
Q _{gd}	Gate-Drain ("Miller") Charge	V _{GS} =-10V	-	1.5	-	nC
t _{d(on)}	Turn-on Delay Time ²	V _{DS} =-10V	-	8	-	ns
t _r	Rise Time	I _D =-1A	-	9	-	ns
t _{d(off)}	Turn-off Delay Time	R _G =6Ω, V _{GS} =-10V	-	21	-	ns
t _f	Fall Time	R _D =10Ω	-	10	-	ns
C _{iss}	Input Capacitance	V _{GS} =0V	-	760	-	pF
C _{oss}	Output Capacitance	V _{DS} =-25V	-	345	-	pF
C _{rss}	Reverse Transfer Capacitance	f=1.0MHz	-	90	-	pF

SOURCE-DRAIN DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
I _S	Continuous Source Current (Body Diode)	V _D =V _G =0V, V _S =-1.2V	-	-	-1.7	A
V _{SD}	Forward On Voltage ²	T _j =25°C, I _S =-1.7A, V _{GS} =0V	-	-	-1.2	V

Notes:

- 1.Pulse width limited by Max. junction temperature.
- 2.Pulse width ≤300us, duty cycle ≤2%.
- 3.Surface mounted on 1 in² copper pad of FR4 board ; 135°C/W when mounted on Min. copper pad.

N-Channel


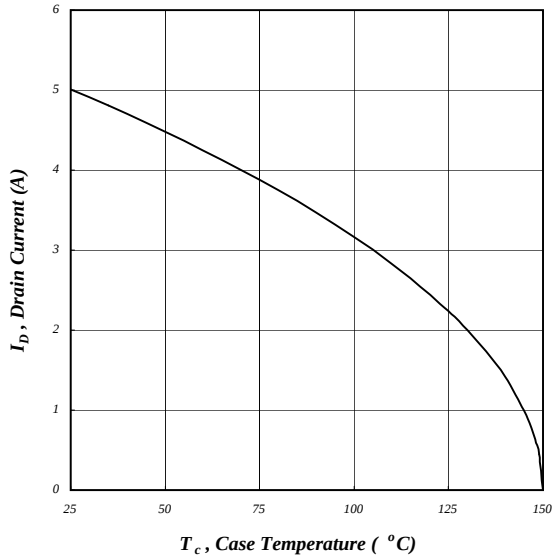
N-Channel


Fig 5. Maximum Drain Current v.s. Case Temperature

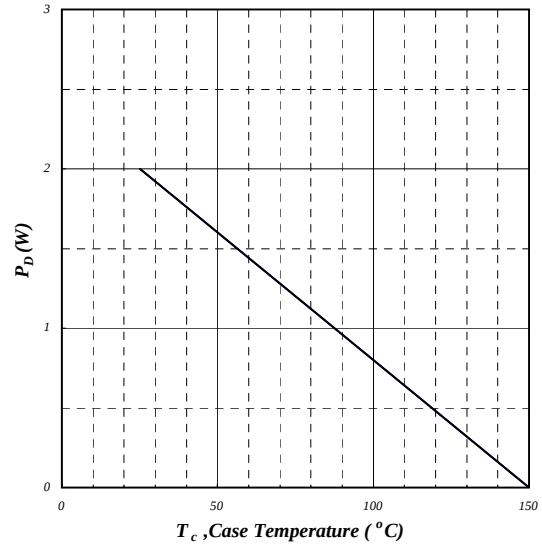


Fig 6. Typical Power Dissipation

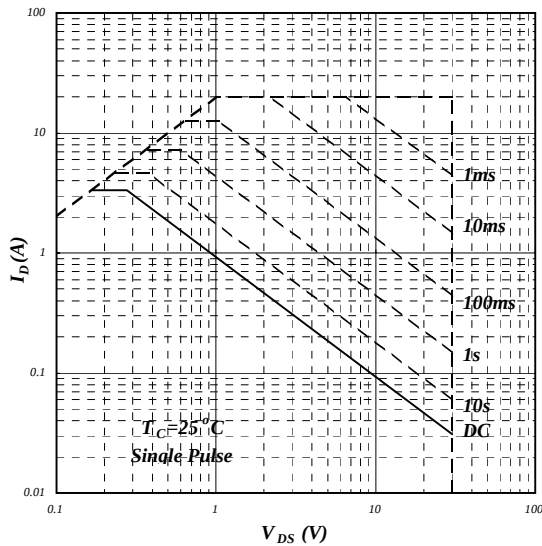


Fig 7. Maximum Safe Operating Area

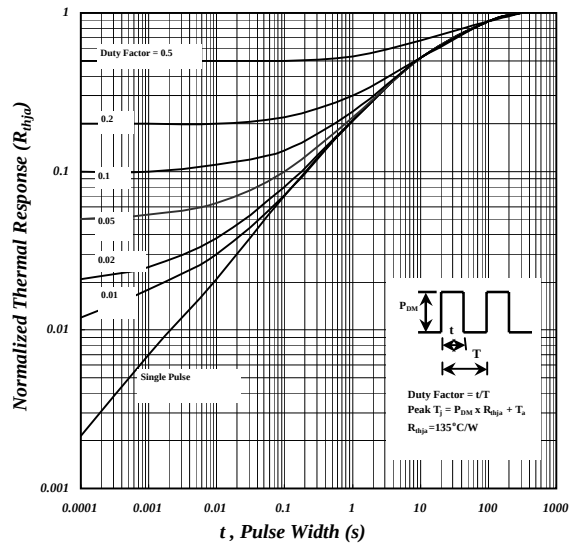
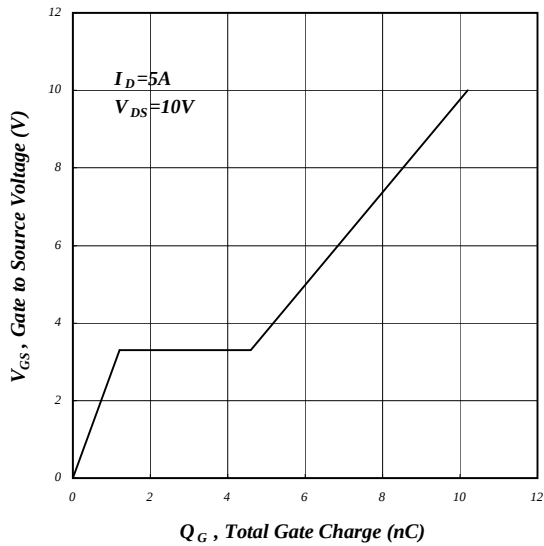
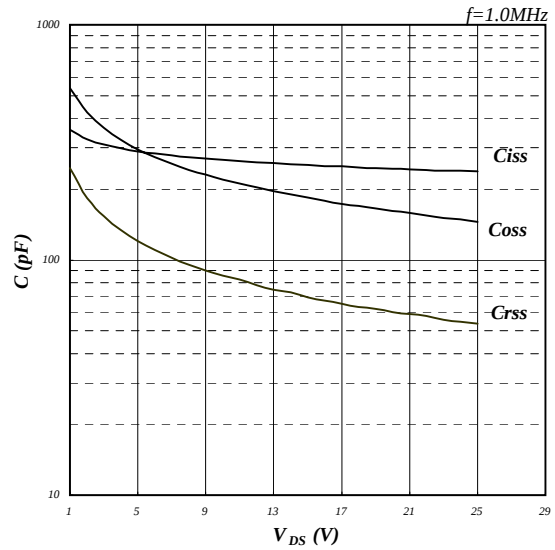
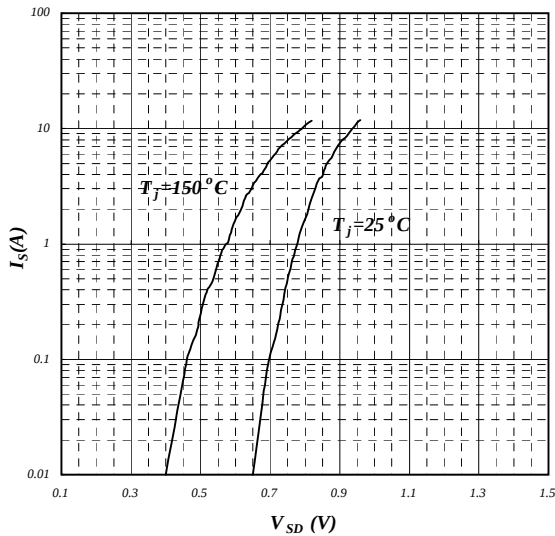
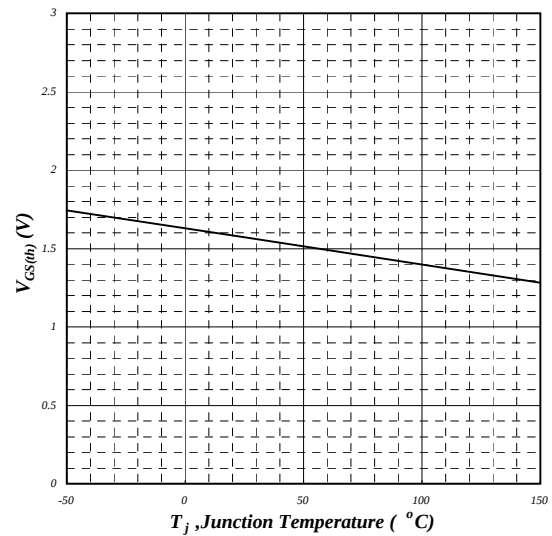


Fig 8. Effective Transient Thermal Impedance

N-Channel

Fig 9. Gate Charge Characteristics

Fig 10. Typical Capacitance Characteristics

Fig 11. Forward Characteristic of Reverse Diode

Fig 12. Gate Threshold Voltage v.s. Junction Temperature

N-Channel

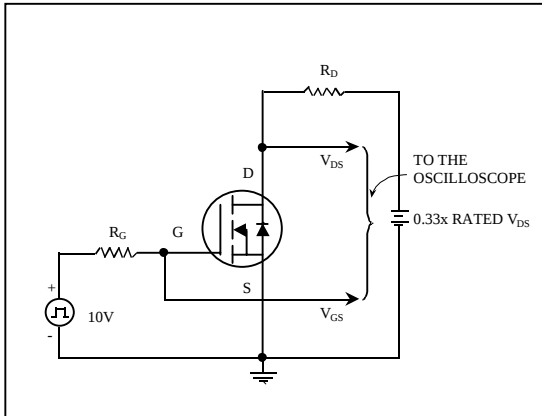


Fig 13. Switching Time Circuit

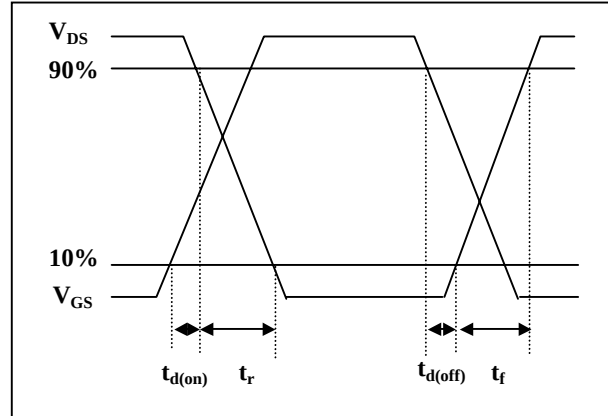


Fig 14. Switching Time Waveform

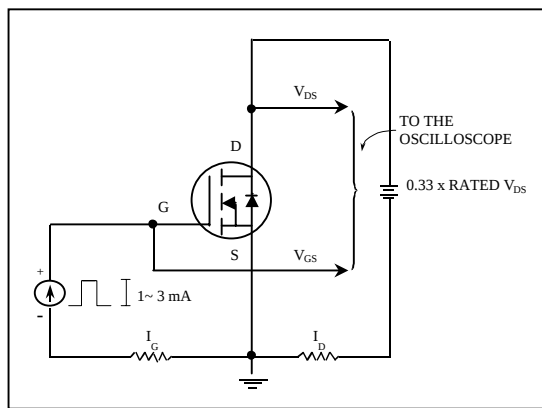


Fig 15. Gate Charge Circuit

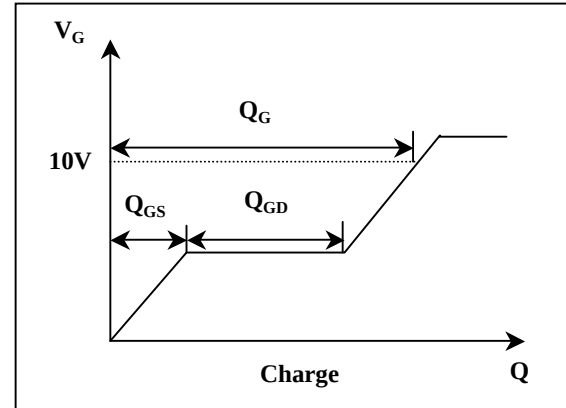
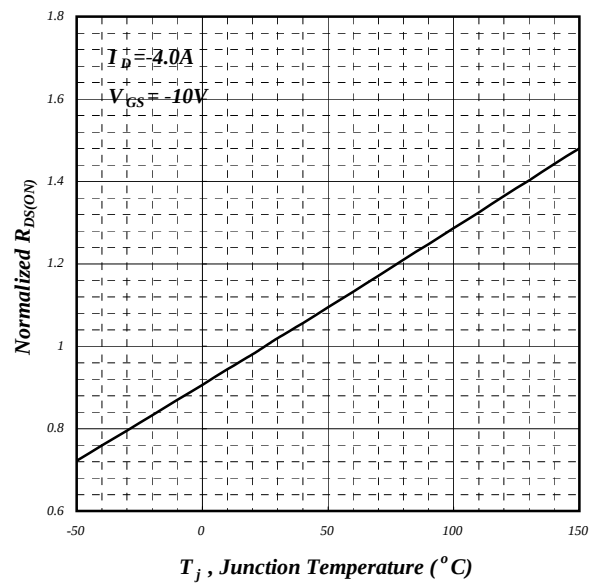
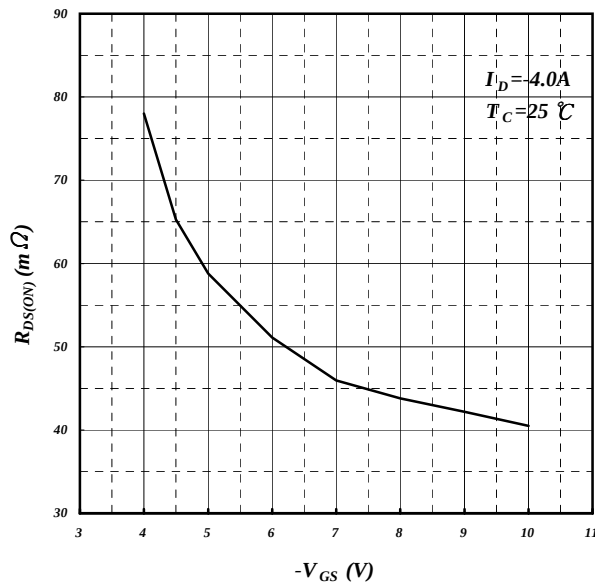
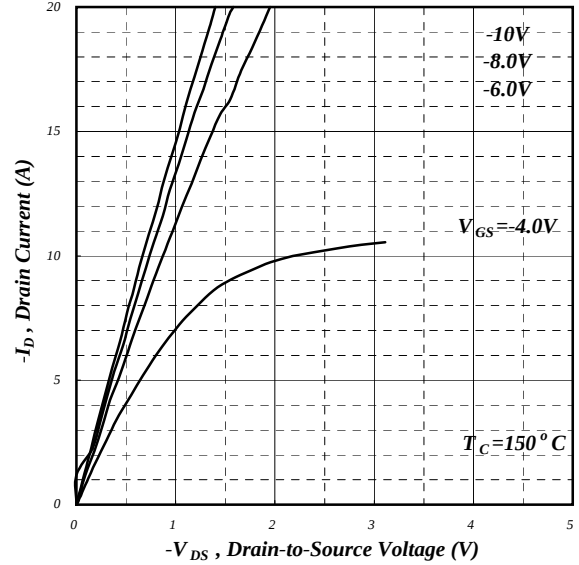
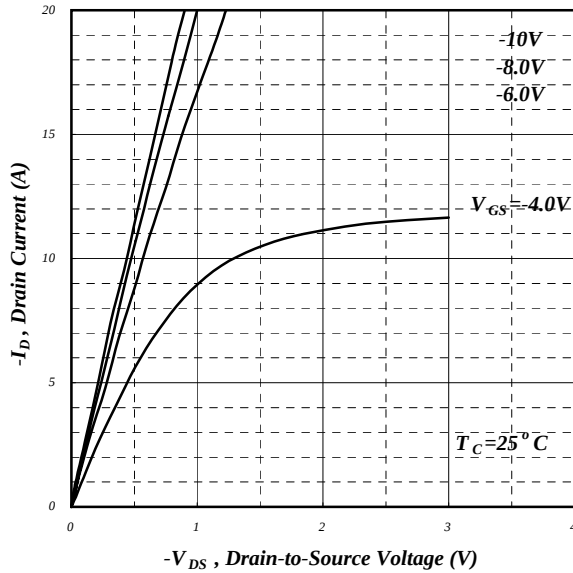


Fig 16. Gate Charge Waveform

P-Channel



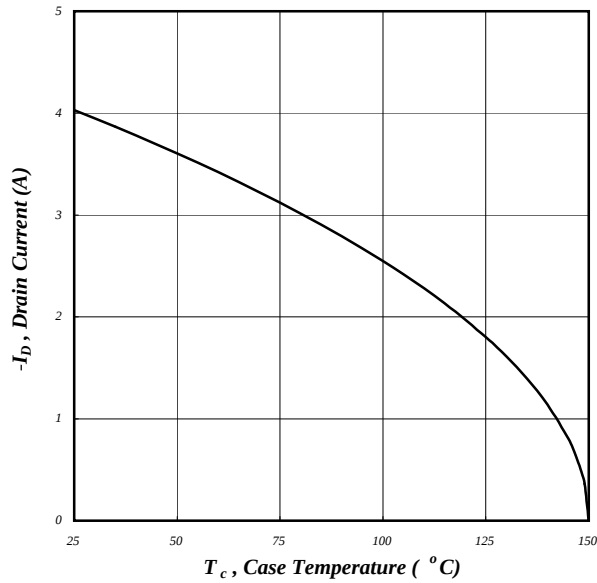
P-Channel


Fig 5. Maximum Drain Current v.s. Case Temperature

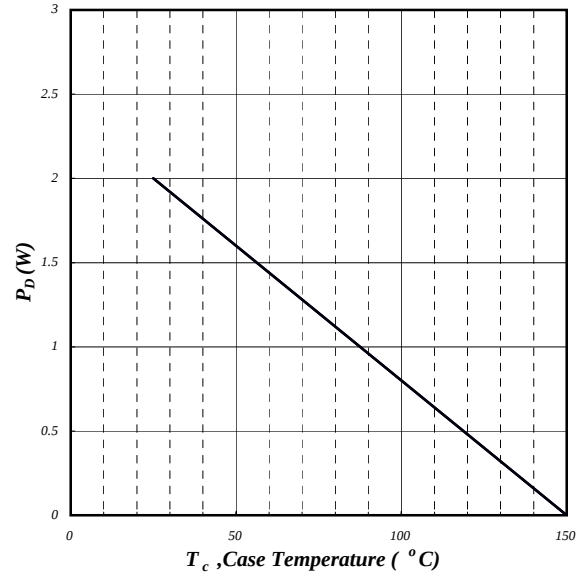


Fig 6. Typical Power Dissipation

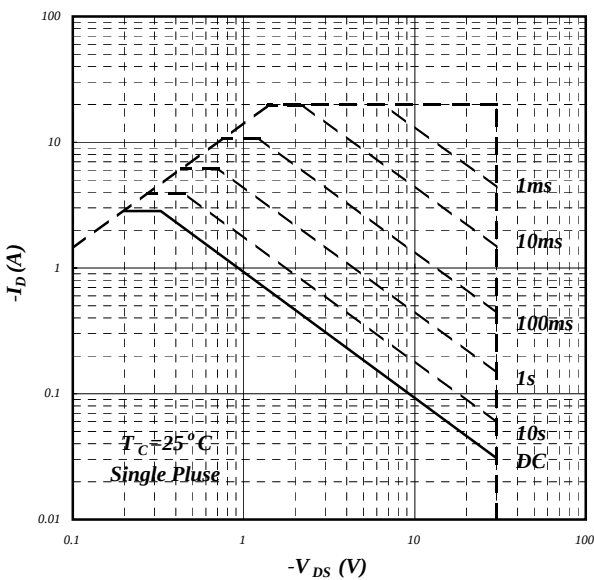


Fig 7. Maximum Safe Operating Area

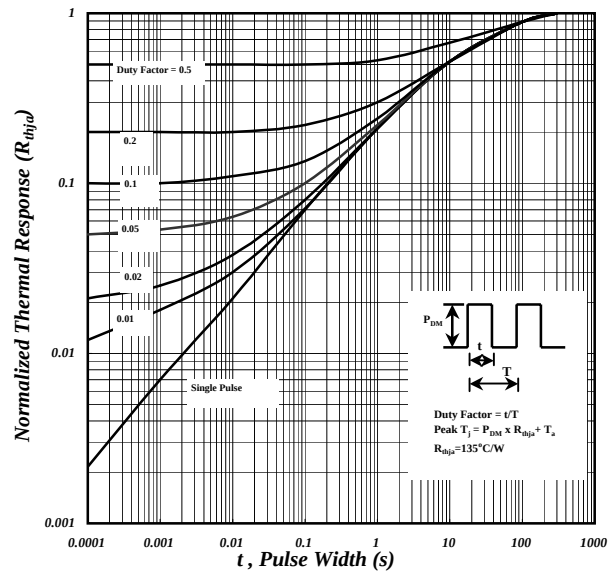


Fig 8. Effective Transient Thermal Impedance

P-Channel

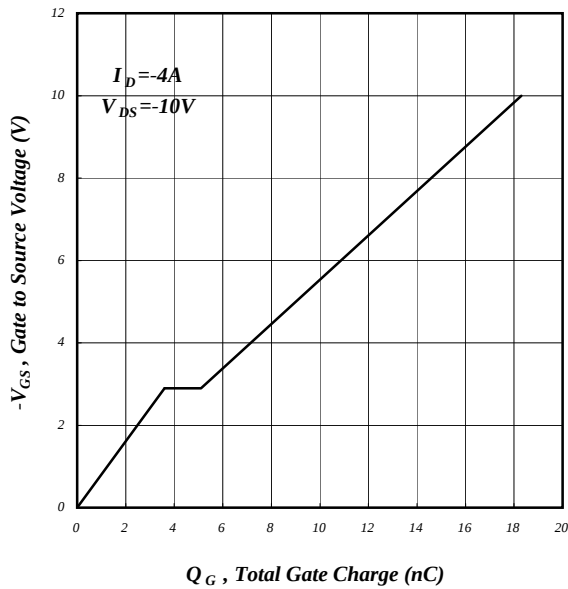


Fig 9. Gate Charge Characteristics

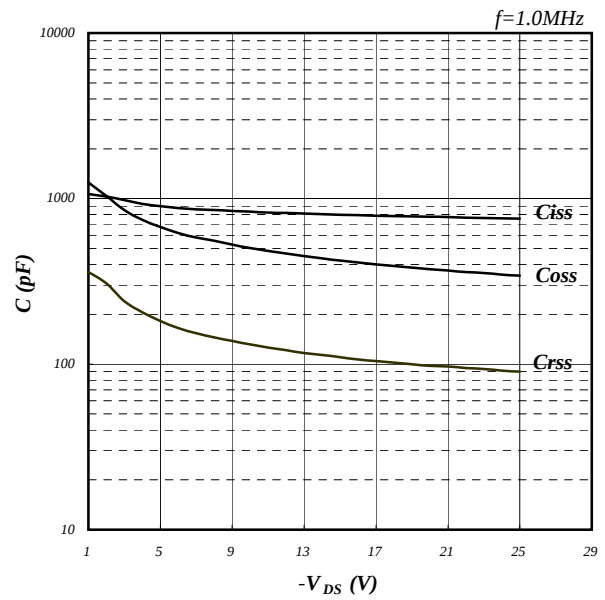


Fig 10. Typical Capacitance Characteristics

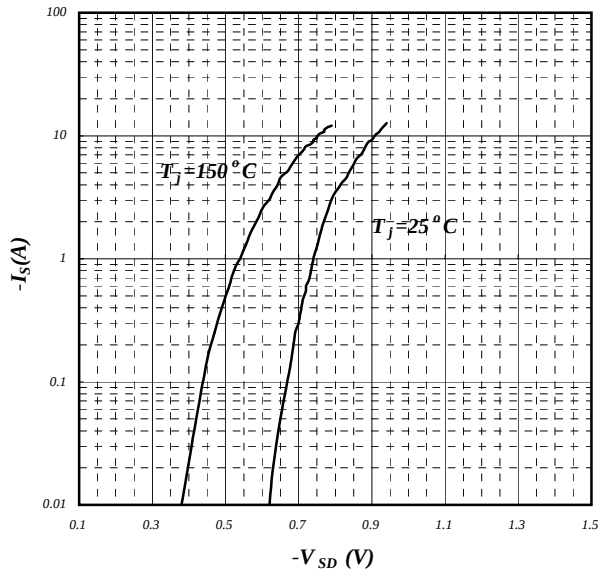


Fig 11. Forward Characteristic of Reverse Diode

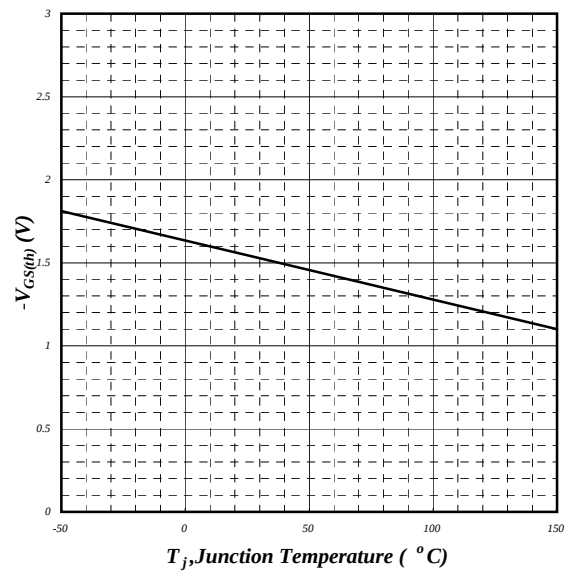


Fig 12. Gate Threshold Voltage v.s. Junction Temperature

P-Channel

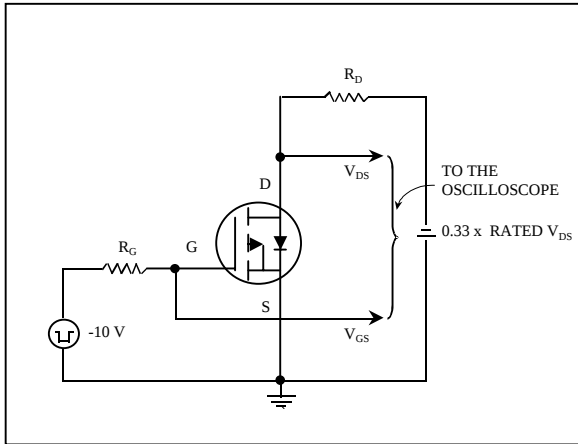


Fig 13. Switching Time Circuit

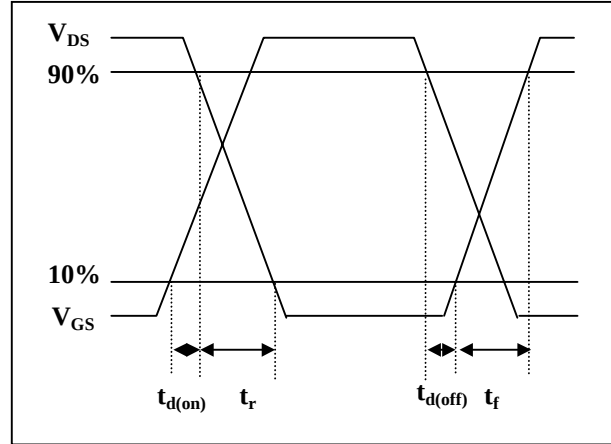


Fig 14. Switching Time Waveform

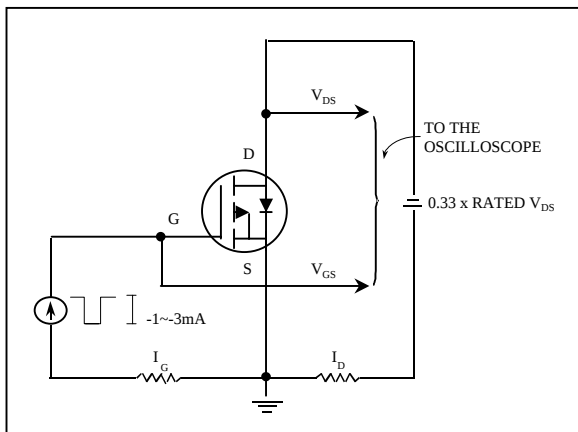


Fig 15. Gate Charge Circuit

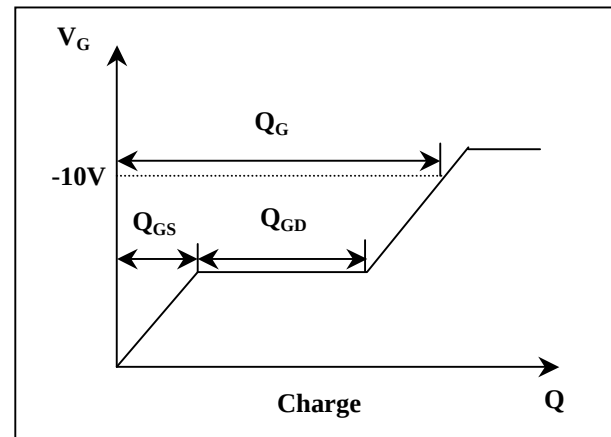


Fig 16. Gate Charge Waveform

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