TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

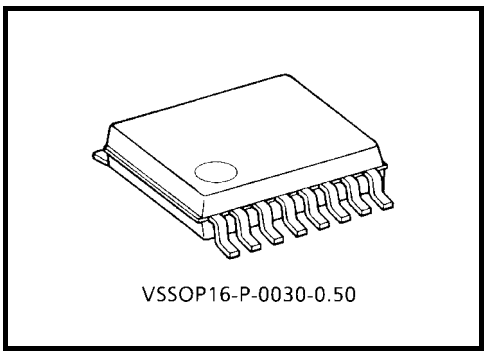
# TC7MBL3257AFK

## Quad 1-of-2 Multiplexer/Demultiplexer

The TC7MBL3257AFK is high-speed CMOS quad 1-2 multiplexer/demultiplexer. The low on resistance of the switch allows connections to be made with minimal propagation delay time.

This device consists of four individual two-inputs multiplexer/demultiplexer with common select input (S) and output enable ($\overline{OE}$). The A inputs is connected to the B1 or B2 outputs determined by the combination both the select input (S) and output enable ($\overline{OE}$). When the output enable ($\overline{OE}$) input is held "H" level, the switches are open with regardless the state of select inputs and a high-impedance state exists between the switches.

All inputs are equipped with protection circuits against static discharge.

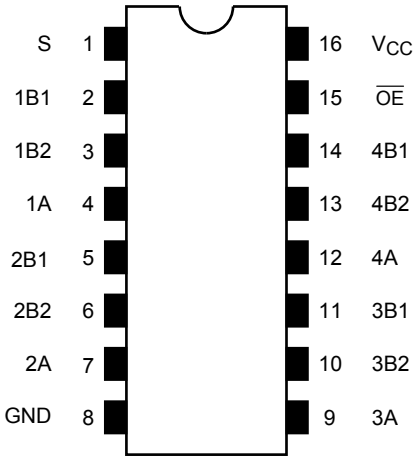



Weight: 0.02 g (typ.)

### Features

- Operating voltage: $V_{CC}$ = 2.0~3.6 V
- High speed: $t_{pd}$ = 0.31ns (max.) @ $V_{CC}$ =3.0V
- Low on resistance: $R_{ON}$ = 5 Ω (typ.) @ $V_{CC}$ =3.0V
- ESD performance: Machine model ≥ ±200 V
  Human body model ≥ ±2000 V
- Package: VSSOP (US16)
- Pin compatible with the 74xx257 type.

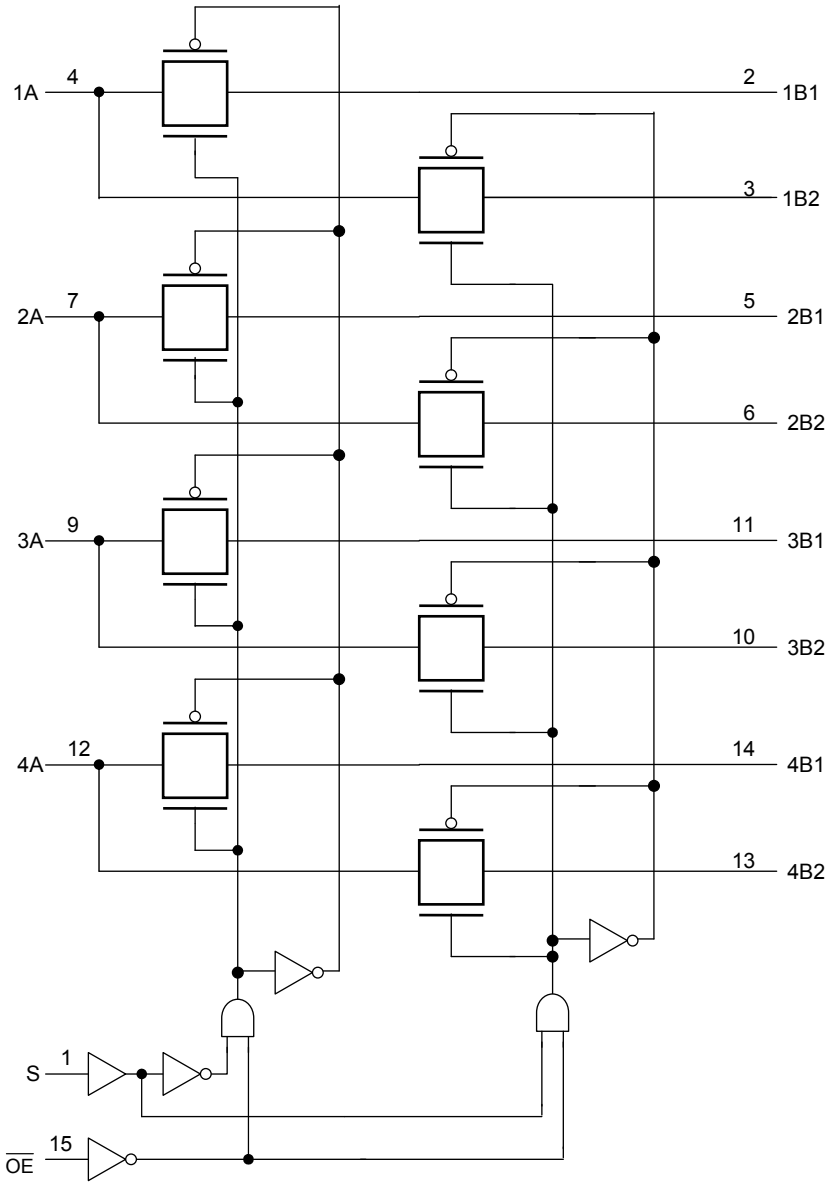
### Pin Assignment (top view)



## Truth Table

| Inputs | | Function |
|---|---|---|
| $\overline{OE}$ | S | |
| L | L | A port = B1 port |
| L | H | A port = B2 port |
| H | X | Disconnect |

## System Diagram



## Absolute Maximum Ratings (Note)

| Characteristics | Symbol | Rating | Unit |
|---|---|---|---|
| Power supply range | $V_{CC}$ | −0.5~4.6 | V |
| DC input voltage | $V_{IN}$ | −0.5~4.6 | V |
| DC switch voltage | $V_S$ | −0.5~Vcc+0.5 | V |
| Input diode current | $I_{IK}$ | −50 | mA |
| Continuous channel current | $I_S$ | 128 | mA |
| Power dissipation | $P_D$ | 180 | mW |
| DC $V_{CC}$/GND current | $I_{CC}/I_{GND}$ | ±100 | mA |
| Storage temperature | $T_{stg}$ | −65~150 | °C |

Note: Exceeding any of the absolute maximum ratings, even briefly, may lead to deterioration in IC performance or even destruction.
Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

## Operating Ranges (Note)

| Characteristics | Symbol | Rating | Unit |
|---|---|---|---|
| Supply voltage | $V_{CC}$ | 2.0~3.6 | V |
| Input voltage | $V_{IN}$ | 0~3.6 | V |
| Switch voltage | $V_S$ | 0~Vcc | V |
| Operating temperature | $T_{opr}$ | −40~85 | °C |
| Input rise and fall time | dt/dv | 0~10 | ns/V |

Note: The operating ranges must be maintained to ensure the normal operation of the device.
Unused inputs must be tied to either $V_{CC}$ or GND.

## Electrical Characteristics

## DC Characteristics (Ta = −40~85°C)

| Characteristics | | Symbol | Test Condition | $V_{CC}$ (V) | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|---|---|---|
| Input voltage | “H” level | $V_{IH}$ | — | 2.0 to 3.6 | 0.7 × $V_{CC}$ | — | — | V |
| | “L” level | $V_{IL}$ | — | 2.0 to 3.6 | — | — | 0.3 × $V_{CC}$ | |
| Input leakage current ( $\overline{OE}$ , S) | | $I_{IN}$ | $V_{IN}$ = 0~3.6 V | 2.0 to 3.6 | — | — | ±1.0 | μA |
| Power off leakage current | | $I_{OFF}$ | $\overline{OE}$ = 0~3.6 V | 0 | — | — | ±1.0 | μA |
| Off-state leakage current (switch off) | | $I_{SZ}$ | A, B = 0~$V_{CC}$, $\overline{OE}$ = $V_{CC}$ | 2.0 to 3.6 | — | — | ±1.0 | μA |
| ON resistance (Note 2) | | $R_{ON}$ | $V_{IS}$ = 0 V, $I_{IS}$ = 30 mA (Note 1) | 3.0 | — | 5 | 7 | Ω |
| | | | $V_{IS}$ = 3.0 V, $I_{IS}$ = 30 mA (Note 1) | 3.0 | — | 5 | 9 | |
| | | | $V_{IS}$ = 2.4 V, $I_{IS}$ = 15 mA (Note 1) | 3.0 | — | 6 | 15 | |
| | | | $V_{IS}$ = 0 V, $I_{IS}$ = 24 mA (Note 1) | 2.3 | — | 6 | 10 | |
| | | | $V_{IS}$ = 2.3 V, $I_{IS}$ = 24 mA (Note 1) | 2.3 | — | 6 | 15 | |
| Increase in $I_{CC}$ per input | | $I_{CC}$ | $V_{IN}$ = $V_{CC}$ or GND, $I_{OUT}$ = 0 | 3.6 | — | — | 10 | μA |

Note 1: All typical values are at Ta = 25°C.

Note 2: Measured by the voltage drop between A and B pins at the indicated current through the switch.
ON resistance is determined by the lower of the voltages on the two (A or B) pins.

## AC Characteristics (Ta = −40~85°C)

| Characteristics | Symbol | Test Condition | $V_{CC}$ (V) | Min | Max | Unit |
|---|---|---|---|---|---|---|
| Propagation delay time (bus to bus) | $t_{pLH}$ / $t_{pHL}$ | Figure 1, Figure 2 (Note) | 3.3 ± 0.3 | — | 0.31 | ns |
| | | | 2.5 ± 0.2 | — | 0.52 | |
| Propagation delay time (S to bus) | $t_{pLH}$ / $t_{pHL}$ | Figure 1, Figure 2 | 3.3 ± 0.3 | — | 11.0 | ns |
| | | | 2.5 ± 0.2 | — | 17.0 | |
| Output enable time ($\overline{OE}$ to bus) | $t_{pZL}$ / $t_{pZH}$ | Figure 1, Figure 3 | 3.3 ± 0.3 | — | 11.0 | ns |
| | | | 2.5 ± 0.2 | — | 17.0 | |
| Output enable time (S to bus) | $t_{pZL}$ / $t_{pZH}$ | Figure 1, Figure 3 | 3.3 ± 0.3 | — | 20.0 | ns |
| | | | 2.5 ± 0.2 | — | 22.0 | |
| Output disable time ($\overline{OE}$ to bus) | $t_{pLZ}$ / $t_{pHZ}$ | Figure 1, Figure 3 | 3.3 ± 0.3 | — | 20.0 | ns |
| | | | 2.5 ± 0.2 | — | 22.0 | |
| Output disable time (S to bus) | $t_{pLZ}$ / $t_{pHZ}$ | Figure 1, Figure 3 | 3.3 ± 0.3 | — | 20.0 | ns |
| | | | 2.5 ± 0.2 | — | 22.0 | |

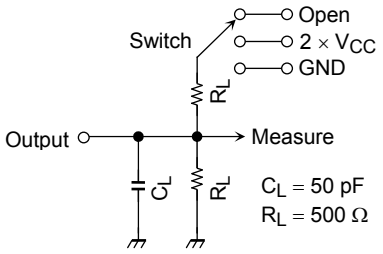
Note: This parameter is guaranteed by design but is not tested. The bus switch contributes no propagation delay other than the RC delay of the typical on resistance of the switch and the 50 pF load capacitance, when driven by an ideal voltage the source (zero output impedance).

## Capacitive Characteristics (Ta = 25°C)

| Characteristics | Symbol | Test Condition | $V_{CC}$ (V) | Typ. | Unit |
|---|---|---|---|---|---|
| Control pin input capacitance ($\overline{OE}$, S) | $C_{IN}$ | (Note) | 3.0 | 3 | pF |
| Switch terminal capacitance (B1~2) | $C_{I/O}$ | $\overline{OE}$ = $V_{CC}$ (Note) | 3.0 | 15 | pF |
| Switch terminal capacitance (A) | $C_{I/O}$ | $\overline{OE}$ = $V_{CC}$ (Note) | 3.0 | 26 | pF |

Note: This parameter is guaranteed by design.

## AC Test Circuit




| Parameter | Switch |
|---|---|
| $t_{pLH}$, $t_{pHL}$ | Open |
| $t_{pLZ}$, $t_{pZL}$ | 2 × $V_{CC}$ |
| $t_{pHZ}$, $t_{pZH}$ | GND |

**Figure 1**

## AC Waveform

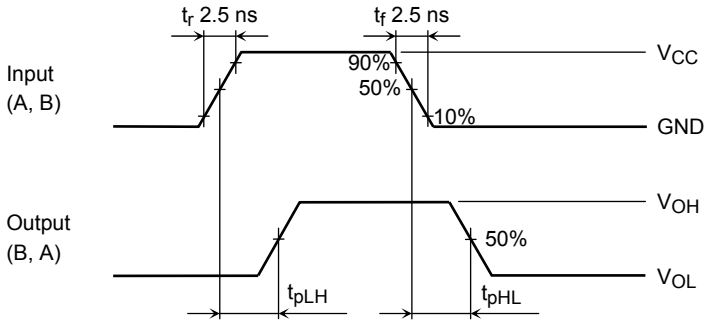



**Figure 2 $t_{pLH}$, $t_{pHL}$**

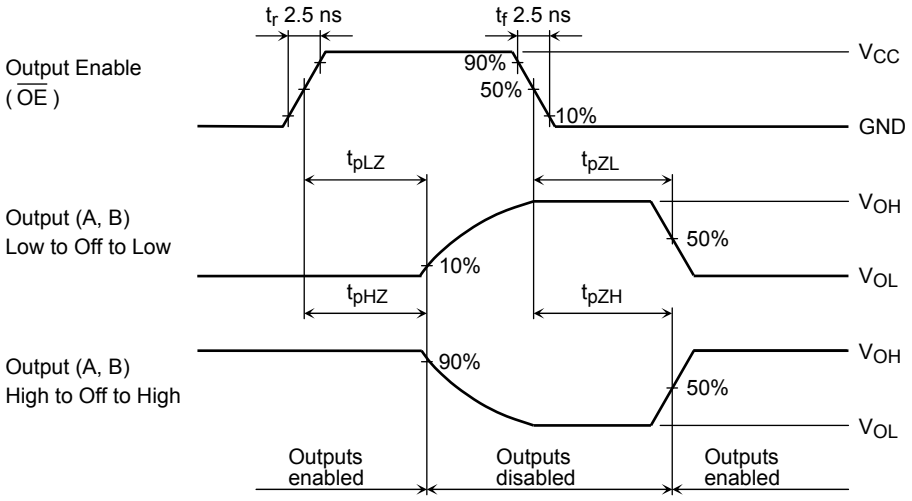
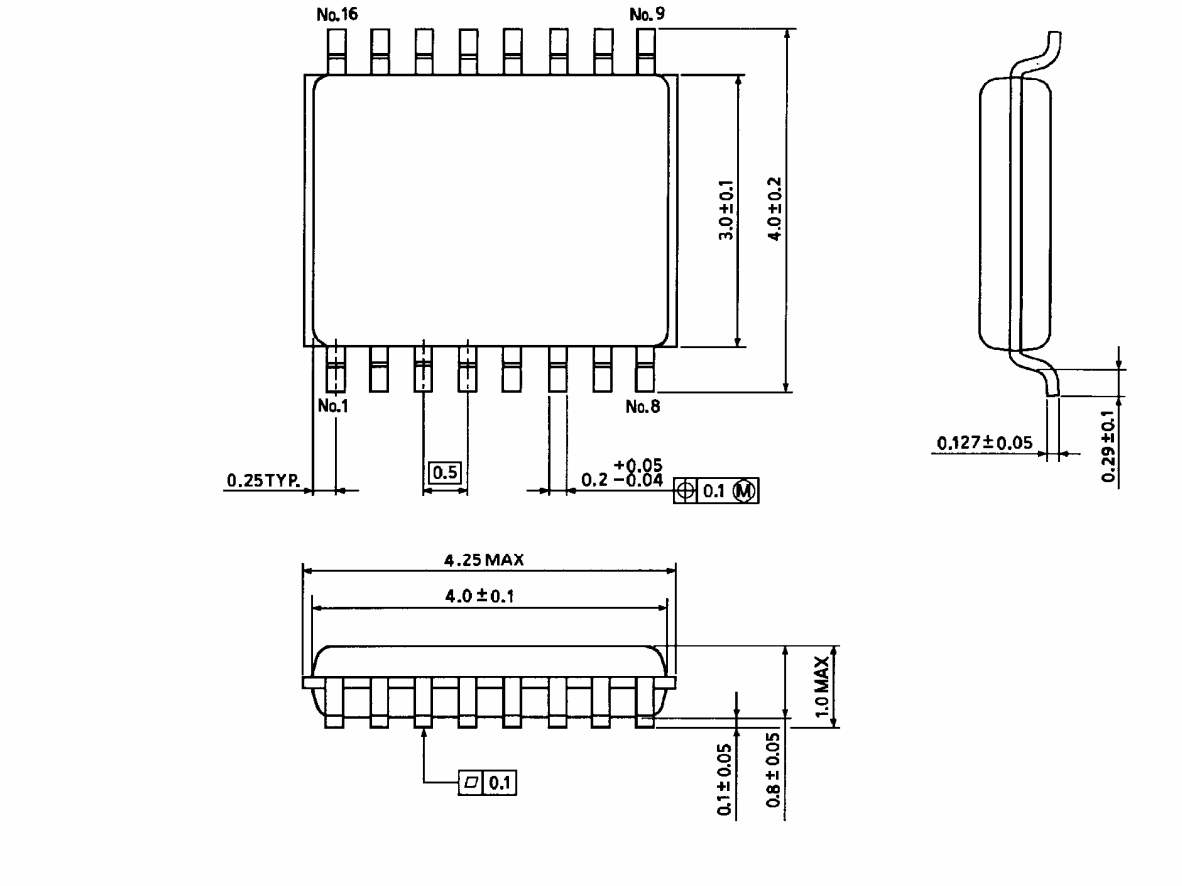



**Figure 3 $t_{pLZ}$, $t_{pHZ}$, $t_{pZL}$, $t_{pZH}$**

## Package Dimensions

VSSOP16-P-0030-0.50 Unit : mm




Weight: 0.02 g (typ.)

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20070701-EN GENERAL

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