NIPPON PRECISION CIRCUITS INC.

SM5302A

3-channel Video Buffer with Built-in wideband LPF

OVERVIEW

The SM5302A is a 3-channel video buffer with built-in 5th-order lowpass filters. The lowpass filter cutoff frequency range can be linearly controlled from 4.8MHz to 43MHz[*1]. The lowpass filter supports 480i to 1080i format, video signal equipment analog input/outputs. For video input systems, the device functions as a next-stage ADC system anti-aliasing filter. For video output systems, the filter removes video DAC aliasing and external noise and can drive a maximum of two 75Ω terminated loads. The cutoff frequency, signal input type, and output gain switching can be controlled using an I^2C[*2] control bus, and the I^2C slave address can be set by ADS (3-state input) to allow a maximum of three devices to be used simultaneously.

*1. When the resistor connected to ISET (R_{ISET}) is 1.8kΩ.
*2. I^2C BUS is a registered trademark of Philips Electronics N.V.

FEATURES

- Supply voltages
  - Analog: 4.75 to 5.25V
  - Digital: 3.0 to 5.5V
- Lowpass filter with linearly adjustable cutoff frequency (256 values)
  - Cutoff frequency range: 4.8MHz to 43MHz (R_{ISET} = 1.8kΩ)
- Filter bypass mode function for display specifications up to SXGA resolution
  - Passband: 80MHz (typ)
- Half fc mode switch function (CH-2, CH-3) suitable for digital component signals
- 2-system input multiplexer function (switchable using I^2C or MUXSEL input)
- Video input pins can be independently set to sync-tip clamp/bias/direct inputs
- Maximum two 75Ω terminated load drive capability
- Output gain switching: 0dB/6dB
- Disable function
  - ≤ 300µA current consumption when disabled
- Output sag compensation circuit built-in
- I^2C interface control
  - Slave address: 90h, 92h, or 94h (up to three devices can be used simultaneously, selected by ADS input)
  - Data transfer rate: Fast mode (up to 400kbit/s)
- Operating ambient temperature range: 0 to 70°C
- Package: 28-pin HSOP

APPLICATIONS

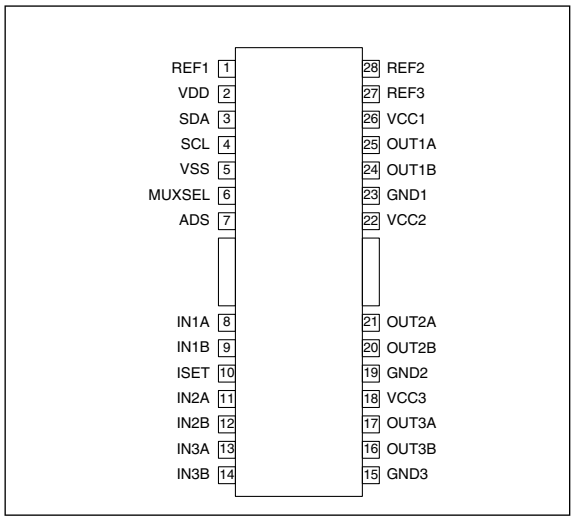
- HDTVs
- LCD TVs
- PDPs
- Projectors

ORDERING INFORMATION

Device	Package
SM5302AS	28-pin HSOP

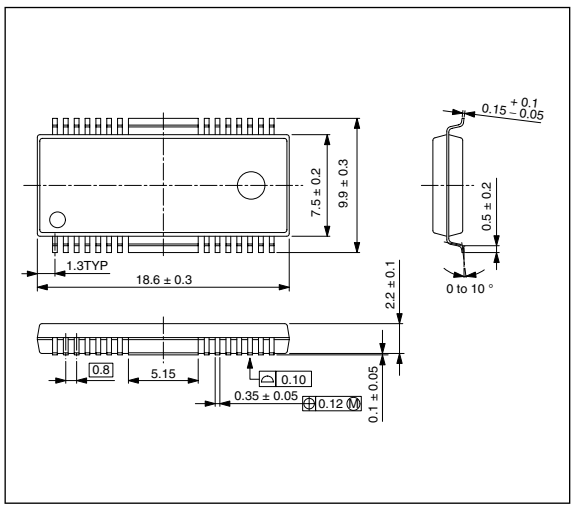
PINOUT

(Top view)

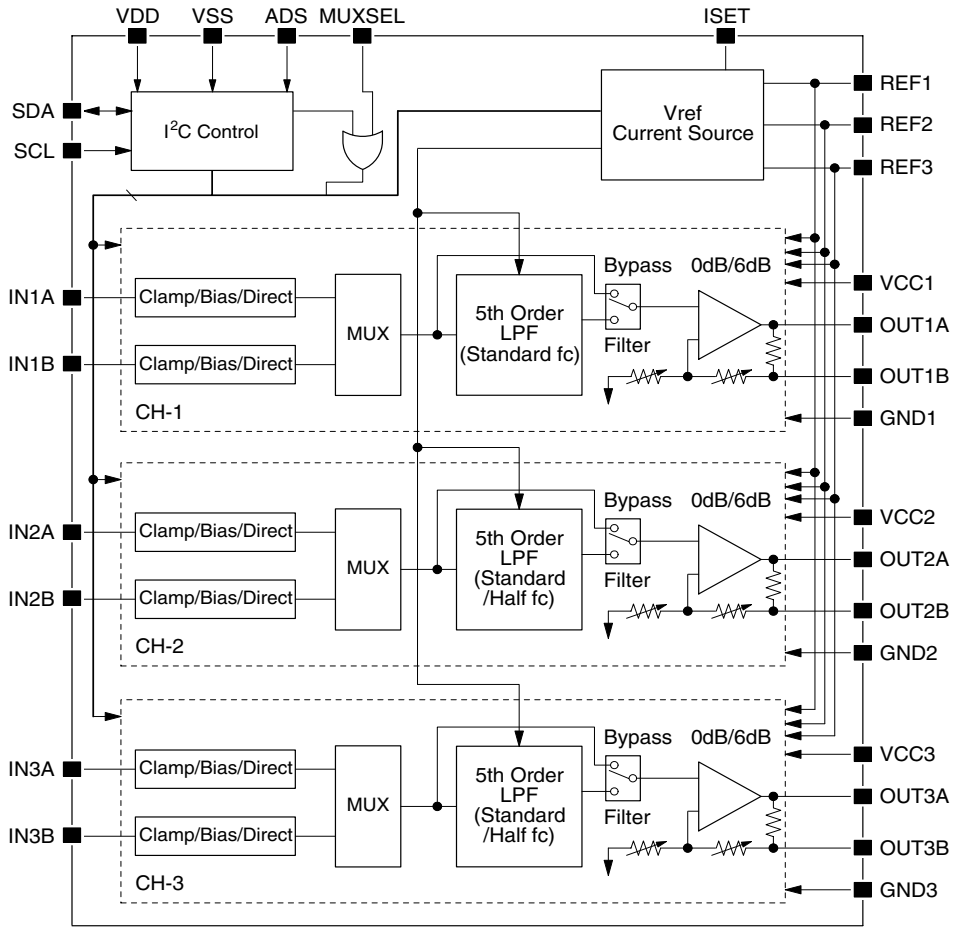


PACKAGE DIMENSIONS

(Unit: mm)



BLOCK DIAGRAM



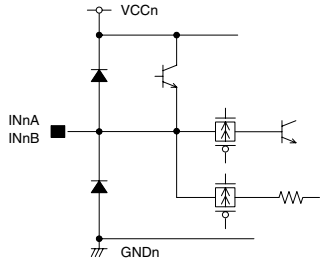
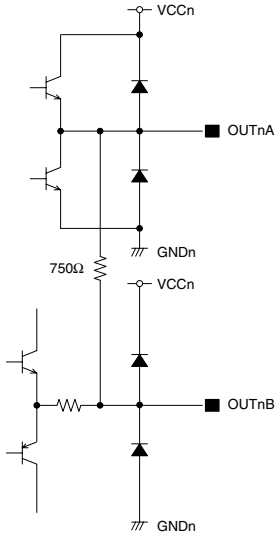
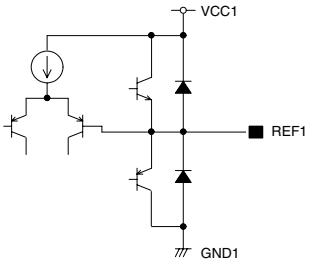
Note. The recommended value of the external resistor connected to ISET is 1.8kΩ.

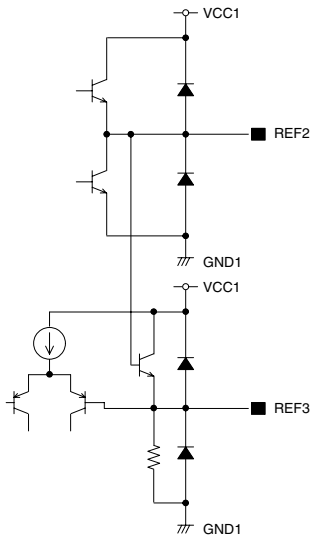
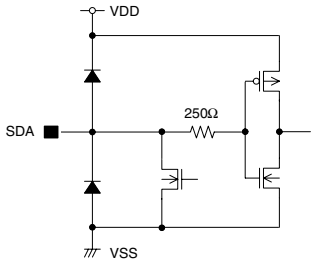
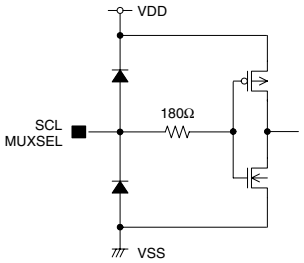
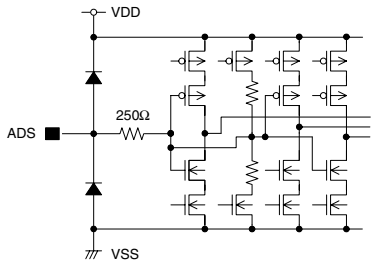
PIN DESCRIPTION

Number	Name	I/O*1	A/D*2	Description
1	REF1	O	A	Internal reference voltage 1
2	VDD	–	D	Digital supply (3.0 to 5.5V)
3	SDA	I/O	D	I^2C data signal input/output
4	SCL	I	D	I^2C clock signal input
5	VSS	–	D	Digital ground
6	MUXSEL	I	D	Input multiplexer switch control
7	ADS	I	D	I^2C slave address select (3-state input)
8	IN1A	I	A	Video signal input (CH-1, input A)
9	IN1B	I	A	Video signal input (CH-1, input B)
10	ISET	–	A	Internal current-setting resistor (R_{ISET}) connection (standard 1.8kΩ)
11	IN2A	I	A	Video signal input (CH-2, input A)
12	IN2B	I	A	Video signal input (CH-2, input B)
13	IN3A	I	A	Video signal input (CH-3, input A)
14	IN3B	I	A	Video signal input (CH-3, input B)
15	GND3	–	A	Analog ground (CH-3)
16	OUT3B	O	A	Video signal output (CH-3, for sag compensation)
17	OUT3A	O	A	Video signal output (CH-3)
18	VCC3	–	A	Analog supply (CH-3) (4.75 to 5.25V)
19	GND2	–	A	Analog ground (CH-2)
20	OUT2B	O	A	Video signal output (CH-2, for sag compensation)
21	OUT2A	O	A	Video signal output (CH-2)
22	VCC2	–	A	Analog supply (CH-2) (4.75 to 5.25V)
23	GND1	–	A	Analog ground (CH-1, Vref)
24	OUT1B	O	A	Video signal output (CH-1, for sag compensation)
25	OUT1A	O	A	Video signal output (CH-1)
26	VCC1	–	A	Analog supply (CH-1, Vref) (4.75 to 5.25V)
27	REF3	O	A	Internal reference voltage 3
28	REF2	O	A	Internal reference voltage 2

*1. I: input, O: output
*2. A: analog, D: digital

PIN EQUIVALENT CIRCUITS

Number	Name	I/O	Equivalent circuit
8 9 11 12 13 14	IN1A IN1B IN2A IN2B IN3A IN3B	I	
25 26 21 20 17 16	OUT1A OUT1B OUT2A OUT2B OUT3A OUT3B	O	
1	REF1	O	

Number	Name	I/O	Equivalent circuit
28 27	REF2 REF3	O	
3	SDA	I/O	
4 6	SCL MUXSEL	I	
7	ADS	I	

Note. Resistance values indicate design values.

SPECIFICATIONS

Absolute Maximum Ratings

V_{SS} = GND1 = GND2 = GND3 = 0V, VCC1 = VCC2 = VCC3 = VDD = V_{CC}

Parameter	Symbol	Condition	Rating	Unit
Supply voltage	V_{CC}	VCC1, VCC2, VCC3, VDD	– 0.3 to 7.0	V
Input voltage	V_{IN}	MUXSEL, ADS, SDA, SCL, INnA, INnB (n = 1, 2, 3)	GND – 0.3 to V_{CC} + 0.3	V
Storage temperature range	T_{STG}		– 55 to + 125	°C
Power dissipation	P_D	θja = 60°C/W Note. θja is the measured quantity under the mounted condition which NPC specified.	1.0	W
Junction temperature	T_J		125	°C

Recommended Operating Conditions

Parameter	Symbol	Condition	Rating	Unit
Supply voltage 1	V_{CC}	VCC1, VCC2, VCC3	4.75 to 5.25	V
Supply voltage difference	ΔV_{CC}	VCC1 – VCC2, VCC1 – VCC3, VCC2 – VCC3	± 0.1	V
Supply voltage 2	V_{DD}	VDD	3.0 to 5.5	V
Operating ambient temperature	Ta		0 to 70	°C

Note. VCC1 to VCC3 should be applied simultaneously.

Electrical Characteristics

DC Characteristics

V_{CC} = 5.0V, V_{DD} = 3.0 to 5.5V, Ta = 25°C, fin = 100kHz, V_{IN} = 1.0Vp-p, R_{ISET} = 1.8kΩ, R_L = 75Ω, CH-1 set to clamp input, CH-2 and CH-3 set to bias input, FCDATA = 227, unless otherwise noted.

Parameter	Symbol	Condition	Rating			Unit	Test level
			min	typ	max		
Current consumption 1*1	I_{CC1}	Filter mode, FCDATA = 255	–	130	155	mA	I
Current consumption 2*1	I_{CC2}	Filter bypass mode	–	85	110	mA	I
Current consumption 3*1	I_{CC3}	Power-down mode, 3-address mode	–	–	300	μA	I
Current consumption 4*1	I_{CC4}	Power-down mode , 2-address mode	–	–	250	μA	I
HIGH-level input voltage	V_{IH1}	SDA, SCL, MUXSEL, Ta = 0 to 70°C	0.7 V_{DD}	–	–	V	I
LOW-level Input voltage	V_{IL1}	SDA, SCL, MUXSEL, Ta = 0 to 70°C	–	–	0.3 V_{DD}	V	I
ADS HIGH-level input voltage	V_{IH2}	ADS, Ta = 0 to 70°C	0.8 V_{DD}	–	–	V	I
ADS LOW-level input voltage	V_{IL2}	ADS, Ta = 0 to 70°C	–	–	0.2 V_{DD}	V	I
ADS open-circuit input voltage	V_{OPEN}	ADS, Ta = 0 to 70°C	$V_{DD}/2$ – 0.2	–	$V_{DD}/2$ + 0.2	V	I
LOW-level input leakage current	I_{LL}	SDA, SCL, MUXSEL, V_{IN} = 0V	–	–	1.0	μA	I
HIGH-level input leakage current	I_{LH}	SDA, SCL, MUXSEL, V_{IN} = V_{DD}	–	–	1.0	μA	I
SDA output voltage	V_{OL}	Sink current = 3mA SDA = LOW output	0	–	0.4	V	I

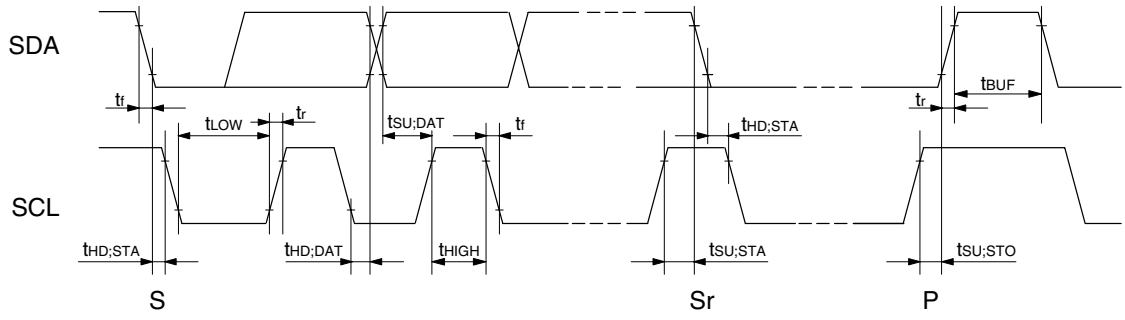
*1. Sum of VCC1 + VCC2 + VCC3 + VDD. No input signals.

AC Characteristics (I^2C)

V_{CC} = 5.0V, V_{DD} = 3.0 to 5.5V, Ta = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Rating			Unit	Test level
			min	typ	max		
SCL clock frequency	f_{SCL}		0	–	400	kHz	II
SCL hold time (start condition)	$t_{HD;STA}$		0.6	–	–	µs	II
SCL clock LOW-level pulsewidth	t_{LOW}		1.3	–	–	µs	II
SCL clock HIGH-level pulsewidth	t_{HIGH}		0.6	–	–	µs	II
SCL setup time (start condition)	$t_{SU;STA}$		0.6	–	–	µs	II
SDA data hold time	$t_{HD;DAT}$		0.15*1	–	0.9	µs	II
SDA data setup time	$t_{SU;DAT}$		100	–	–	ns	II
SDA, SCL rise time	t_r		–	–	300	ns	II
SDA, SCL fall time	t_f		–	–	300	ns	II
SCL setup time (stop condition)	$t_{SU;STO}$		0.6	–	–	µs	II
SDA, SCL input capacitance	C_i		–	–	10	pF	II

*1. This value is not conforming to the I^2C BUS specification established by Philips Corporation.



Analog Characteristics

Analog input characteristics

V_{CC} = 5.0V, V_{DD} = 3.0 to 5.5V, Ta = 25°C, fin = 100kHz, V_{IN} = 1.0Vp-p, R_{ISET} = 1.8kΩ, R_L = 75Ω, CH-1 set to clamp input, CH-2 and CH-3 set to bias input, FCDATA = 227, unless otherwise noted. Internal mode settings are shown in table 1 in "Mode Condition Settings".

Parameter	Symbol	Condition	Rating			Unit	Test level
			min	typ	max		
Clamp voltage	V_{CLMP}	Clamp input	1.8	2.0	2.2	V	I
Bias voltage	V_{BIAS}	Bias input	2.2	2.4	2.6	V	I
Input resistance	R_{BIAS}	Bias input	–	20	–	kΩ	II
Filter mode maximum input voltage	V_{AI1}	Mode: b0 (bias, 0dB), THD < 1.0%	1.4	–	–	Vp-p	I
	V_{AI2}	Mode: b6 (bias, 6dB), THD < 1.0%	1.4	–	–	Vp-p	I
	V_{AI3}	Mode: c0 (clamp, 0dB), THD < 1.0%	1.4	–	–	Vp-p	I
	V_{AI4}	Mode: c6 (clamp, 6dB), THD < 1.5%	1.0	–	–	Vp-p	I
Bias mode maximum input voltage	V_{AI5}	Mode: f0 (bias, 0dB), THD < 1.0%	1.4	–	–	Vp-p	I
	V_{AI6}	Mode: f6 (bias, 6dB), THD < 1.5%	1.2	–	–	Vp-p	I
	V_{AI7}	Mode: g0 (clamp, 0dB), THD < 1.0%	1.4	–	–	Vp-p	I
	V_{AI8}	Mode: g6 (clamp, 6dB), THD < 1.5%	1.0	–	–	Vp-p	I
Direct mode input DC voltage range	V_{IDC1}	Mode: h0 , THD < 1.5%, V_{IN} < 1.4Vp-p	1.5	–	3.5	V	I
	V_{IDC2}	Mode: h6, THD < 1.5%, V_{IN} < 1.2Vp-p	1.7	–	3.0	V	I
	V_{IDC3}	Mode: j0 , THD < 1.5%, V_{IN} < 1.4Vp-p	1.1	–	3.3	V	I
	V_{IDC4}	Mode: j6, THD < 1.5%, V_{IN} < 1.2Vp-p	1.4	–	2.9	V	I

Filter mode and bypass mode frequency characteristics

V_{CC} = 5.0V, V_{DD} = 3.0 to 5.5V, Ta = 25°C, fin = 100kHz, V_{IN} = 1.0Vp-p, R_{ISET} = 1.8kΩ, R_L = 75Ω, CH-1 set to clamp input, CH-2 and CH-3 set to bias input, FCDATA = 227, unless otherwise noted.

Parameter	Symbol	Condition	Rating			Unit	Test level
			min	typ	max		
Cutoff frequency	F_{C1}	FCDATA = 0	–	4.74	–	MHz	II
	F_{C2}	FCDATA = 10	5.98	6.79	7.60	MHz	I
	F_{C3}	FCDATA = 227	32.5	36.89	41.3	MHz	I
	F_{C4}	FCDATA = 255	–	43.73	–	MHz	II
Half fc mode cutoff frequency ratio	R_{half1}	Half fc mode, FCDATA = 10	44	49	54	%	I
	R_{half2}	Half fc mode, FCDATA = 227	49	54	59	%	I
4fc attenuation	G_{SB}	fin ≥ 4fc, attenuation from fin = 100kHz	–	50	–	dB	II
Filter bypass mode passband	F_{BP}	V_{IN} = 0.7Vp-p, Gain = – 1dB	68	80	–	MHz	I

Analog output characteristics

V_{CC} = 5.0V, V_{DD} = 3.0 to 5.5V, Ta = 25°C, fin = 100kHz, V_{IN} = 1.0Vp-p, R_{ISET} = 1.8kΩ, R_L = 75Ω, CH-1 set to clamp input, CH-2 and CH-3 set to bias input, FCDATA = 227, unless otherwise noted. Internal mode settings are shown in table 1 in "Mode Condition Settings".

Parameter	Symbol	Condition	Rating			Unit	Test level
			min	typ	max		
Filter mode output gain	A_{VF1}	Gain = 0dB	– 0.5	0	0.5	dB	I
	A_{VF2}	Gain = 6dB	5.5	6.0	6.5	dB	I
Filter bypass mode output gain	A_{VB1}	Gain = 0dB	– 0.5	0	0.5	dB	I
	A_{VB2}	Gain = 6dB	5.5	6.0	6.5	dB	I
Filter bypass mode gain error	dA_{VBP}	Gain error between filter mode and bypass mode	–	± 0.2	–	dB	I
Channel to channel gain error	dA_{VCH}		–	–	± 0.2	dB	I
Maximum output voltage	V_{out1}	Mode: b0, c0 (0dB), THD < 1.0%	1.4	–	–	Vp-p	I
	V_{out2}	Mode: b6, c6 (6dB), THD < 1.5%	2.4	–	–	Vp-p	I
Output distortion	T_{HDB1}	Mode: b0, fin = 1kHz, V_{IN} = 1.4Vp-p	–	0.2	1.0	%	I
	T_{HDB2}	Mode: b6, fin = 1kHz, V_{IN} = 1.2Vp-p	–	0.2	1.0	%	I
	T_{HDC1}	Mode: c0, fin = 1kHz, V_{IN} = 1.4Vp-p	–	0.2	1.0	%	I
	T_{HDC2}	Mode: c6, fin = 1kHz, V_{IN} = 1.0Vp-p	–	0.5	1.5	%	I
Channel to channel crosstalk	X_{TLK1}	0.5Vp-p input, fin = 1MHz, between 2 channels	–	– 71	–	dB	II
MUX input to input crosstalk	X_{TLK2}	0.5Vp-p input, fin = 1MHz, between INnA-INnB, 6dB	–	– 50	–	dB	II
Drive load resistance	R_L	1 load = 150Ω	–	–	2	load	I
I^2C response time	T_{IC}	Response time from ACK bit output when changing I^2C settings	–	–	1	µs	II
MUXSEL switch response time	T_{MS}	Response time at L → H, H → L	–	–	1	µs	II

Reference Voltage Characteristics (REF)

V_{CC} = 5.0V, V_{DD} = 3.0 to 5.5V, Ta = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Rating			Unit	Test level
			min	typ	max		
REF output voltage	V_{R1}	REF1	–	2.45	–	V	II
	V_{R2}	REF2	–	2.65	–	V	II
	V_{R3}	REF3	–	1.90	–	V	II

Test level

I : 100% of products tested at Ta = + 25°C.

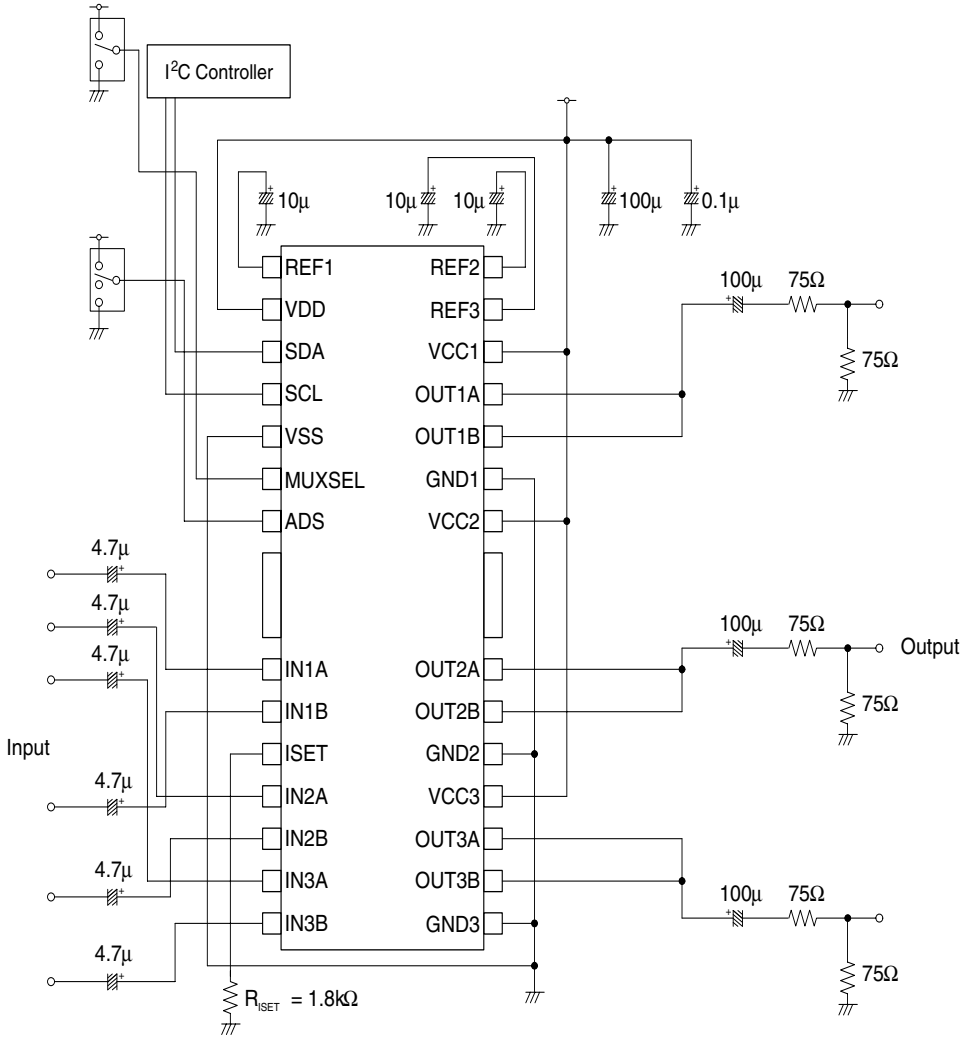
II : Guaranteed as result of design and characteristics evaluation.

Mode Condition Settings

Table 1. Mode settings

Mode setting	Input type			Output gain	fc mode	Filter/Bypass mode
	CH-1	CH-2	CH-3			
a0	Clamp	Bias	Bias	0dB	Standard	Filter
a6				6dB		
b0	Bias			0dB		
b6				6dB		
c0	Clamp			0dB		
c6				6dB		
d0	Bias			0dB	Half	
d6				6dB		
e0	Clamp			0dB		
e6				6dB		
f0	Bias			0dB	–	Bypass
f6				6dB		
g0	Clamp			0dB		
g6				6dB		
h0	Direct			0dB	Standard	Filter
h6				6dB		
i0				0dB	Half	
i6				6dB		
j0				0dB	–	Bypass
j6				6dB		

Evaluation Circuit Diagram



Note. This is the electrical characteristics evaluation circuit only, then it is not a recommended application circuit.

FUNCTIONAL DESCRIPTION

I²C BUS Control

The SM5302A uses an I²C BUS interface to set the following functions.

1) Cutoff frequency
2) Output gain
3) fc mode switching (1/2 cutoff frequency switching)
4) Filter mode/filter bypass mode switching
5) Input multiplexer selection
6) Input type switching (sync-tip clamp, bias, direct)
7) Disable function
8) Maximum number of slave addresses

It supports fast-mode data transfer rate (up to 400kbit/s).
Note that the SM5302A does not have a read function (IC is write only).

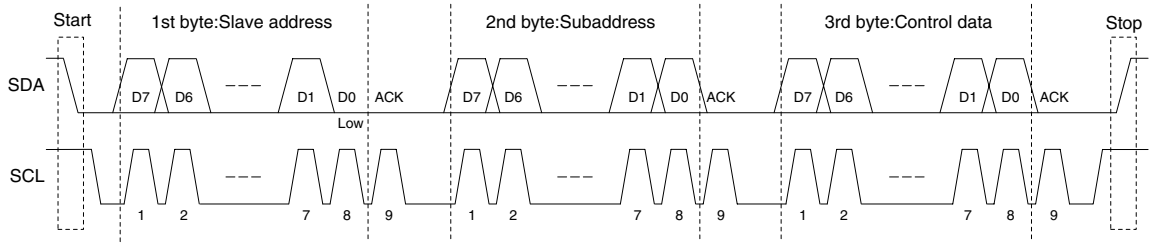
Basic cycle

I²C start/stop condition

The basic access cycle comprises the following elements.

1) Start condition
2) 1st byte: Slave address
3) 2nd byte: Subaddress
4) 3rd byte: Control data
5) Stop condition

If the input data does not match the slave address or the subaddress is incorrect, the corresponding ACK (acknowledge) bit is not output LOW. However, the ACK bit is output after 3rd byte irrespective of the byte data. Also note that the IC does not have a subaddress auto-increment function, hence each subaddress access requires all the basic cycle steps 1 to 5.



1st byte: slave address

The ADS pin can set one of three slave addresses. Note that D0 must be “0 (Write)”.

ADS	1st byte: slave address								
	HEX	D7	D6	D5	D4	D3	D2	D1	D0
L	90h	1	0	0	1	0	0	0	0 (W)
H	92h	1	0	0	1	0	0	1	0 (W)
Open*1	94h	1	0	0	1	0	1	0	0 (W)

*1. When ADS is open (94h), I^2C control may not be able to set the address. See “P16. (8) Maximum number of slave addresses.”

2nd byte: subaddress

The 2nd byte sets the subaddress, selecting one of three registers.

Register name	2nd byte: subaddress								
	HEX	D7	D6	D5	D4	D3	D2	D1	D0
FCSET	01h	0	0	0	0	0	0	0	1
CONDITION1	02h	0	0	0	0	0	0	1	0
CONDITION2	03h	0	0	0	0	0	0	1	1

3rd byte: control data

The 3rd byte control data sets the register flags corresponding to the subaddress selected by 2nd byte. The flags assigned are shown in the following table.

Register name	3rd byte: control data							
	D7	D6	D5	D4	D3	D2	D1	D0
FCSET	FCM	FC6	FC5	FC4	FC3	FC2	FC1	FC0
CONDITION1	CB5	CB4	CB3	CB2	CB1	CB0	–	GS
CONDITION2	PD	MUX	HALF	BYPASS	–	NCA	–	–

Flag settings

(1) Cutoff frequency

Register name: FCSET

Flag names: FCM, FC [6:0]

The FCSET register setting sets the cutoff frequency using one of two tuning adjustment functions, thus a total of 256 values are possible. The cutoff frequency is determined by the following equations. The values are shown in "Lowpass Filter".

- FCDATA = 0 to 127 : $fc = k11 \times FCDATA^2 + k12 \times FCDATA + k13$ [MHz]
- FCDATA = 128 to 255: $fc = k21 \times FCDATA^2 + k22 \times FCDATA + k23$ [MHz]

The coefficients when R_{ISET} = 1.8kΩ are:

- k11 = – 1.95e – 4, k12 = 2.07e – 1, k13 = 4.74
- k21 = – 3.92e – 4, k22 = 4.33e – 1, k23 = – 41.2

FCDATA	FCSET	Flag name								Cutoff frequency [MHz]	Default
		FCM	FC6	FC5	FC4	FC3	FC2	FC1	FC0		
0	00h	0	0	0	0	0	0	0	0	4.74	○
1	01h	0	0	0	0	0	0	0	1	4.95	
2	02h	0	0	0	0	0	0	1	0	5.15	
:											
125	7Dh	0	1	1	1	1	1	0	1	27.57	
126	7Eh	0	1	1	1	1	1	1	0	27.73	
127	7Fh	0	1	1	1	1	1	1	1	27.88	
128	80h	1	0	0	0	0	0	0	0	7.80	
129	81h	1	0	0	0	0	0	0	1	8.13	
130	82h	1	0	0	0	0	0	1	0	8.47	
:											
253	FDh	1	1	1	1	1	1	0	1	43.26	
254	FEh	1	1	1	1	1	1	1	0	43.49	
255	FFh	1	1	1	1	1	1	1	1	43.73	

(2) Input type switching (sync-tip clamp, bias, direct)

Register name: CONDITION1

Flag names: CB [5:4], CB [3:2], CB [1:0]

These flags set the input type of CH-1, CH-2, and CH-3 to one of three types: sync-tip clamp input, bias input, or direct input.

Channel	Flag name		Input type	Default
CH-1 CH-2 CH-3	CB5 CB3 CB1	CB4 CB2 CB0		
	L	L	Sync-tip clamp input	○
	L	H	Bias input	
	H	Don't care	Direct input*1	

*1. An input coupling capacitor should not be connected when direct input is selected.

(3) Output gain

Register name: CONDITION1

Flag name: GS

Flag name	Output gain	Default
GS		
L	0dB	○
H	6dB	

(4) Disable mode select

Register name: CONDITION2

Flag name: PD

This flag enables/disables the analog block. When the analog block is disabled, the output pins are high impedance.

Flag name	Mode	Default
PD		
L	Enable (normal operation)	○
H	Disable (no operation)	

(5) Input multiplexer selection

Register name: CONDITION2

Flag name: MUX

This flag selects the A or B input for all three channels (IN1×, IN2×, IN3×). Note that this flag is significant only when the MUXSEL input is LOW. See “Input Multiplexer Switching (MUXSEL)”.

Flag name	Input selection*1	Default
MUX		
L	INnA	○
H	INnB	

*1. n = 1, 2, 3

(6) fc mode switching (1/2 cutoff frequency switching)

Register name: CONDITION2

Flag name: HALF

This flag switches the cutoff frequency of CH-2 and CH-3 to divide the value set by the FCSET register into halves. Note that the CH-1 cutoff frequency cannot be switched. This mode is suitable for systems where the sampling frequency varies due to Y, Cr, and Cb requirements, such as digital component signals or digital HDTV signals.

Flag name	fc mode	Default
HALF		
L	Standard fc mode (CH-1, CH-2, CH-3 cutoff frequency is identical)	○
H	Half fc mode (CH-2, CH-3 cutoff frequency is 1/2 that of CH-1)	

(7) Filter bypass mode

Register name: CONDITION2

Flag name: BYPASS

This flag allows the lowpass filter to be bypassed. The output gain can be switched, even in filter bypass mode. The input type, multiplexer function, and output gain can all be set just as in filter mode. However, the cutoff frequency and fc mode settings have no effect on the outputs.

Flag name	Filter	Default
BYPASS		
L	Filter mode (signals pass through lowpass filter)	○
H	Filter bypass mode (signals bypass lowpass filter)	

(8) Maximum number of slave addresses

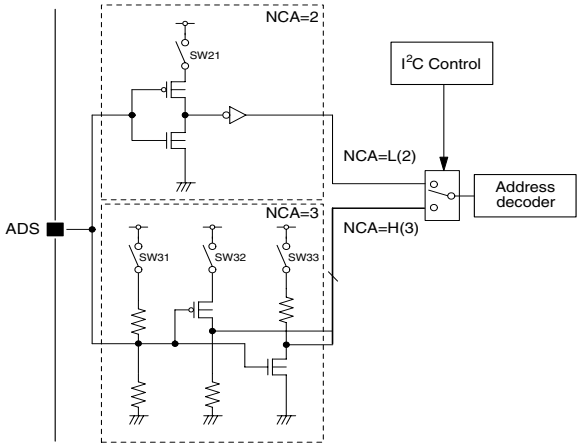
Register name: CONDITION2

Flag name: NCA

The NCA flag sets the maximum number of slave addresses to either 2 or 3. The NCA setting modifies the ADS input pin equivalent circuit as shown below.
When NCA = LOW (max = 2), switches SW31 to SW33 are OFF, reducing the current consumed in comparison to when NCA = HIGH (max = 3). Note that only 2 ADS input levels (LOW or HIGH) are valid.
When NCA = HIGH (max = 3), switches SW31 to SW33 are ON and hence current is consumed regardless of whether the ADS input is LOW, HIGH, or Open. However, note that 3 ADS input levels are valid.

Note. The default value for NCA is HIGH (max = 3). If NCA is once set to LOW (max = 2) for a device addressed by the setting when ADS is Open, that device is subsequently no longer accessible.

Flag name	Maximum number of slave address	Default	ADS level	Slave address	ADS pin current flow
NCA					
L	2 (2-address mode)		LOW HIGH Open	1001000 1001001 Invalid	No
H	3 (3-address mode)	○	LOW HIGH Open	1001000 1001001 1001010	Yes



Lowpass Filter

The IC has built-in 5th-order lowpass filters with variable cutoff frequency. The frequency range is determined by the resistor (R_{ISET}) connected between ISET and GND, and the cutoff frequency is set by register FCDATA data. The cutoff frequency vs. FCDATA values are listed in table 2, and shown graphically in figure 1.

Table 2. Cutoff frequency vs. FCDATA (R_{ISET} = 1.8kΩ)

FCDATA	FCSET (hex)	Cutoff freq. [MHz]	FCDATA	FCSET (hex)	Cutoff freq. [MHz]	FCDATA	FCSET (hex)	Cutoff freq. [MHz]	FCDATA	FCSET (hex)	Cutoff freq. [MHz]
0	00	4.74	64	40	17.19	128	80	7.80	192	C0	27.49
1	01	4.95	65	41	17.37	129	81	8.13	193	C1	27.77
2	02	5.15	66	42	17.55	130	82	8.47	194	C2	28.05
3	03	5.36	67	43	17.73	131	83	8.80	195	C3	28.33
4	04	5.56	68	44	17.91	132	84	9.13	196	C4	28.61
5	05	5.77	69	45	18.09	133	85	9.45	197	C5	28.89
6	06	5.97	70	46	18.27	134	86	9.78	198	C6	29.17
7	07	6.18	71	47	18.45	135	87	10.11	199	C7	29.44
8	08	6.38	72	48	18.63	136	88	10.44	200	C8	29.72
9	09	6.59	73	49	18.81	137	89	10.76	201	C9	30.00
10	0A	6.79	74	4A	18.99	138	8A	11.09	202	CA	30.27
11	0B	6.99	75	4B	19.17	139	8B	11.41	203	CB	30.55
12	0C	7.20	76	4C	19.35	140	8C	11.74	204	CC	30.82
13	0D	7.40	77	4D	19.52	141	8D	12.06	205	CD	31.09
14	0E	7.60	78	4E	19.70	142	8E	12.38	206	CE	31.36
15	0F	7.80	79	4F	19.88	143	8F	12.70	207	CF	31.63
16	10	8.00	80	50	20.05	144	90	13.02	208	D0	31.90
17	11	8.20	81	51	20.23	145	91	13.34	209	D1	32.17
18	12	8.40	82	52	20.40	146	92	13.66	210	D2	32.44
19	13	8.60	83	53	20.58	147	93	13.98	211	D3	32.71
20	14	8.80	84	54	20.75	148	94	14.30	212	D4	32.98
21	15	9.00	85	55	20.93	149	95	14.61	213	D5	33.24
22	16	9.20	86	56	21.10	150	96	14.93	214	D6	33.51
23	17	9.40	87	57	21.27	151	97	15.25	215	D7	33.77
24	18	9.60	88	58	21.45	152	98	15.56	216	D8	34.04
25	19	9.79	89	59	21.62	153	99	15.87	217	D9	34.30
26	1A	9.99	90	5A	21.79	154	9A	16.19	218	DA	34.56
27	1B	10.19	91	5B	21.96	155	9B	16.50	219	DB	34.83
28	1C	10.38	92	5C	22.13	156	9C	16.81	220	DC	35.09
29	1D	10.58	93	5D	22.30	157	9D	17.12	221	DD	35.35
30	1E	10.77	94	5E	22.47	158	9E	17.43	222	DE	35.61
31	1F	10.97	95	5F	22.65	159	9F	17.74	223	DF	35.87
32	20	11.16	96	60	22.81	160	A0	18.04	224	E0	36.12
33	21	11.36	97	61	22.98	161	A1	18.35	225	E1	36.38
34	22	11.55	98	62	23.15	162	A2	18.66	226	E2	36.64
35	23	11.75	99	63	23.32	163	A3	18.96	227	E3	36.89
36	24	11.94	100	64	23.49	164	A4	19.27	228	E4	37.15
37	25	12.13	101	65	23.66	165	A5	19.57	229	E5	37.40
38	26	12.32	102	66	23.83	166	A6	19.88	230	E6	37.65
39	27	12.52	103	67	23.99	167	A7	20.18	231	E7	37.91
40	28	12.71	104	68	24.16	168	A8	20.48	232	E8	38.16
41	29	12.90	105	69	24.33	169	A9	20.78	233	E9	38.41
42	2A	13.09	106	6A	24.49	170	AA	21.08	234	EA	38.66
43	2B	13.28	107	6B	24.66	171	AB	21.38	235	EB	38.91
44	2C	13.47	108	6C	24.82	172	AC	21.68	236	EC	39.16
45	2D	13.66	109	6D	24.99	173	AD	21.98	237	ED	39.40
46	2E	13.85	110	6E	25.15	174	AE	22.27	238	EE	39.65
47	2F	14.04	111	6F	25.31	175	AF	22.57	239	EF	39.90
48	30	14.23	112	70	25.48	176	B0	22.87	240	F0	40.14
49	31	14.41	113	71	25.64	177	B1	23.16	241	F1	40.39
50	32	14.60	114	72	25.80	178	B2	23.45	242	F2	40.63
51	33	14.79	115	73	25.97	179	B3	23.75	243	F3	40.87
52	34	14.98	116	74	26.13	180	B4	24.04	244	F4	41.11
53	35	15.16	117	75	26.29	181	B5	24.33	245	F5	41.36
54	36	15.35	118	76	26.45	182	B6	24.62	246	F6	41.60
55	37	15.54	119	77	26.61	183	B7	24.91	247	F7	41.84
56	38	15.72	120	78	26.77	184	B8	25.20	248	F8	42.07
57	39	15.91	121	79	26.93	185	B9	25.49	249	F9	42.31
58	3A	16.09	122	7A	27.09	186	BA	25.78	250	FA	42.55
59	3B	16.27	123	7B	27.25	187	BB	26.06	251	FB	42.79
60	3C	16.46	124	7C	27.41	188	BC	26.35	252	FC	43.02
61	3D	16.64	125	7D	27.57	189	BD	26.63	253	FD	43.26
62	3E	16.82	126	7E	27.73	190	BE	26.92	254	FE	43.49
63	3F	17.01	127	7F	27.88	191	BF	27.20	255	FF	43.73

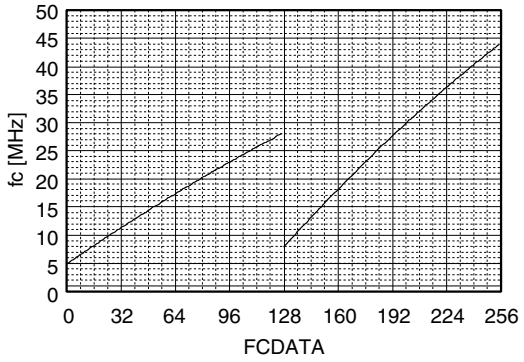


Figure 1. Cutoff frequency vs. FCDATA (R_{ISET} = 1.8kΩ)

R_{ISET}

R_{ISET} controls the internal current source, and its connection is essential. The recommended value is 1.8kΩ. In disable mode and filter bypass mode, the ISET pin is high impedance, and no current flows into R_{ISET}.

Note. A value other than 1.8kΩ will change the current consumption, so caution should be taken to ensure the power dissipation does not exceed the absolute maximum rating for the package.

Half fc Mode

In half fc mode, the CH-2 and CH-3 cutoff frequency is 1/2 that of the CH-1 cutoff frequency setting. Half fc mode is useful for systems where the sampling frequency varies due to luminance (Y) and color difference signal (Cr, Cb) requirements as in digital component signals. Note in figure 2 that the cutoff frequency ratio for a given cutoff frequency setting (FCDATA) is not constant.

Group Delay Characteristics

The group delay varies with the cutoff frequency setting, as shown in figure 3. Note also that in half fc mode, the group delay between CH-1 and CH-2/CH-3 varies.

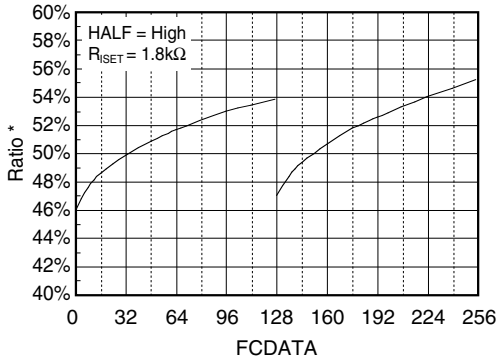


Figure 2. Cutoff frequency ratio (half fc mode)

* Ratio of CH-2 and CH-3 cutoff frequency at half fc mode based on CH-1 cutoff frequency.

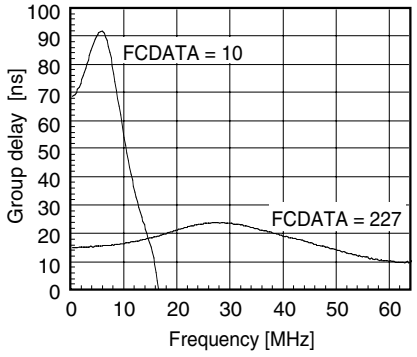


Figure 3. Group delay characteristics

Filter Bypass Mode

In filter bypass mode, the lowpass filter is bypassed and the signal is input to the output buffer stage. The input type, multiplexer function, and output gain are set just as for filter mode. The cutoff frequency setting and fc mode setting have no effect on the outputs. In this mode, the passband frequency is 80MHz (typ), which can support SXGA-class signals.

Input Multiplexer Switching (MUXSEL)

The input multiplexer setting can also be set using the MUXSEL input. When set using the I^2C BUS, a certain amount of communication time is required, but the setting can be made using the MUXSEL input with arbitrary timing for high-speed switching.

MUXSEL pin	MUX flag	Multiplexer selection*1
L	L	INnA
L	H	INnB
H	L	INnB
H	H	INnB

*1. n = 1, 2, 3

Power-ON Reset

When power is applied, an internal power-ON reset circuit operates initializing the internal register flags to their default settings. At power-ON, all supplies should be applied simultaneously.

Sag Compensation Circuit

A sag compensation circuit is built-in between the OUTnA and OUTnB pins. In circuits where the load resistance is small and the capacitance required is large, using the sag compensation circuit allows the total capacitance and mounting area to be reduced. If the sag compensation circuit is not used, output OUTnA should be connected to OUTnB. The electrical characteristics are not guaranteed if OUTnB is left open circuit.

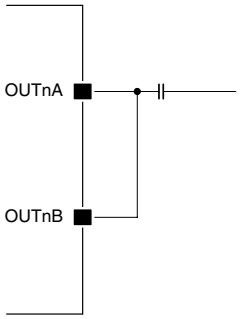


Figure 4. Connection without sag compensation circuit

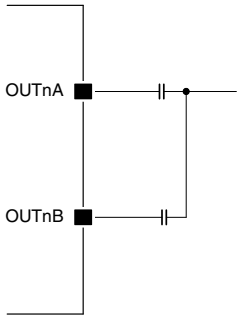


Figure 5. Connection with sag compensation circuit

Reference Voltage (REF)

The REFn pins (n = 1, 2, 3) are internal reference voltage outputs. A 10 µF capacitor connected to ground is recommended for stability. REF1, REF2, and REF3 are independent reference voltage outputs, and have no correspondence with channels CH-1, CH-2, and CH-3. In disable mode, they are high impedance outputs.

USAGE PRECAUTIONS

Slave Address (94h) Setting

When slave address 94h is used, the ADS input must be left open circuit. In this case, an external resistor should be connected as shown in figure 6 to reduce the risk of malfunction due to large external spikes or other noise. The recommended value is 10kΩ.

Oscillation Prevention Capacitor Connection

If the sag compensation circuit is used with 2 output capacitors connected, the capacitors should be mounted within approximately 8cm of the IC pins. If the distance exceeds 8cm, they may cause an oscillation. A 15pF oscillation prevention capacitor should be connected between OUTnA and OUTnB. If the sag compensation circuit is not used, OUTnA is connected to OUTnB. As there is only 1 output capacitor, an oscillation prevention capacitor is not required.

Unused Analog Inputs

It is recommended that unused analog inputs should be connected to ground through a capacitor as shown in figure 8.

Direct Input Mode

In direct input mode, the signal is connected to the input without an input capacitor. However, the input DC voltage range varies with the mode setting, hence the signal must be appropriately biased for the corresponding mode. The recommended LOW-level voltage (V_L) and HIGH-level voltage (V_H) for each mode is shown in table 3 (see figure 9, V_{CC} = 5V). If the input voltage exceeds these limits, harmonic distortion may occur in the output signal. Note that even if these limits are exceeded, device breakdown will not occur if still within the absolute maximum ratings.

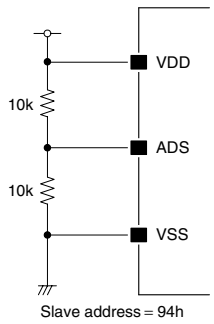


Figure 6. Slave address 94h setting

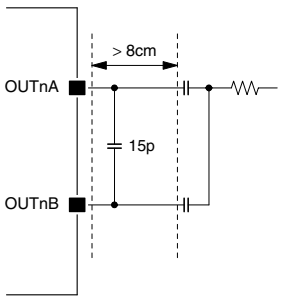


Figure 7. Oscillation prevention capacitor connection

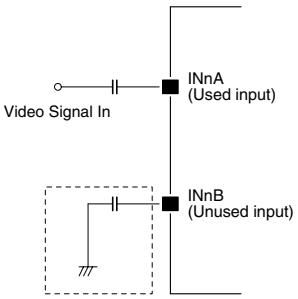


Figure 8. Unused analog inputs

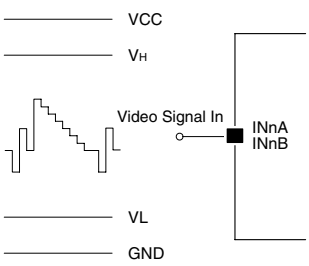


Figure 9. Direct input mode

Table 3. Direct mode recommended input DC voltage range (V_{CC} = 5V)

Mode setting	Gain	fc mode	Filter/Bypass mode	Sag compensation circuit*1	Channel	V_L [V]	V_H [V]
h0	0dB	Standard	Filter	Used	CH-1	1.5	3.5
					CH-2, CH-3		
				Not used	CH-1	1.3	3.7
					CH-2, CH-3		
i0		Half		Used	CH-1	1.5	3.5
					CH-2, CH-3	1.6	3.6
				Not used	CH-1	1.3	3.7
					CH-2, CH-3	1.5	3.7
j0		–	Bypass	Used	CH-1	1.0	3.3
					CH-2, CH-3		
				Not used	CH-1	1.1	3.6
					CH-2, CH-3		
h6	6dB	Standard	Filter	Used	CH-1	1.7	3.0
					CH-2, CH-3		
				Not used	CH-1	1.6	3.1
					CH-2, CH-3		
i6		Half		Used	CH-1	1.7	3.0
					CH-2, CH-3	1.8	2.95
				Not used	CH-1	1.6	3.1
					CH-2, CH-3	1.7	3.0
j6		–	Bypass	Used	CH-1	1.4	2.9
					CH-2, CH-3		
				Not used	CH-1	1.4	2.9
					CH-2, CH-3		

*1. Refer to figure 4 or 5 in “Sag Compensation Circuit”.

TYPICAL CHARACTERISTICS

V_{CC} = 5.0V, V_{DD} = 5.0V, Ta = 25°C, V_{IN} = 1.0Vp-p, R_{ISET} = 1.8kΩ, R_L = 75Ω, unless otherwise noted.

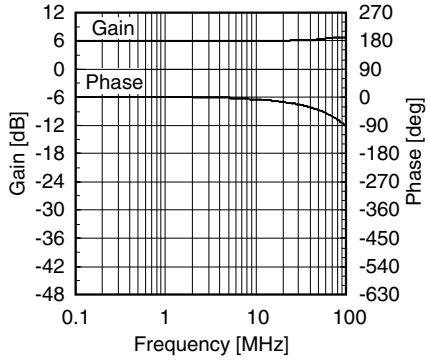


Figure 10. Gain and Phase characteristics (6dB, filter bypass mode)

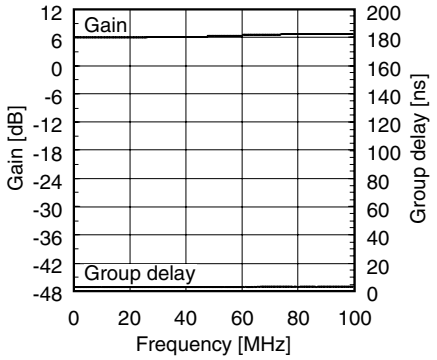


Figure 11. Gain and Group delay characteristics (6dB, filter bypass mode)

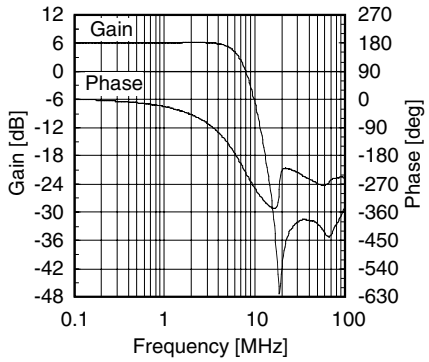


Figure 12. Gain and Phase characteristics (6dB, standard fc mode, FCDATA = 10)

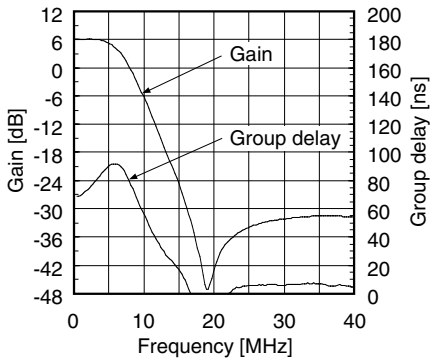


Figure 13. Gain and Group delay characteristics (6dB, standard fc mode, FCDATA = 10)

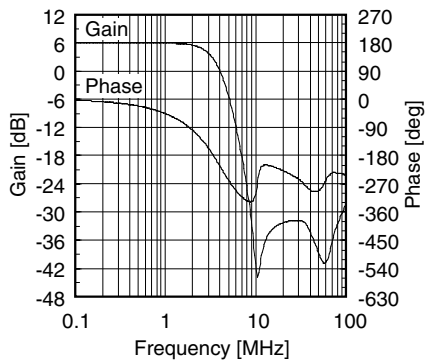


Figure 14. Gain and Phase Characteristics (6dB, half fc mode, FCDATA = 10)

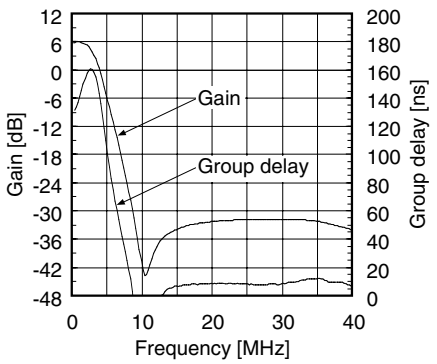


Figure 15. Gain and Group delay characteristics (6dB, half fc mode, FCDATA = 10)

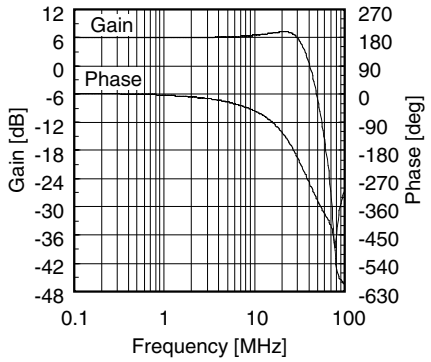


Figure 16. Gain and Phase characteristics (6dB, standard fc mode, FCDATA = 227)

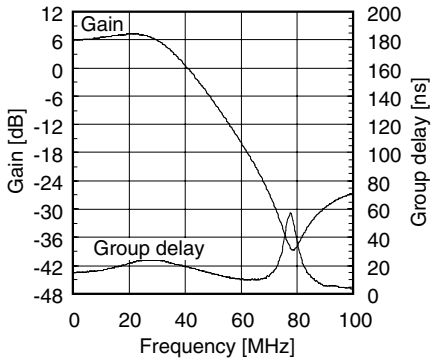


Figure 17. Gain and Group delay characteristics (6dB, standard fc mode, FCDATA = 227)

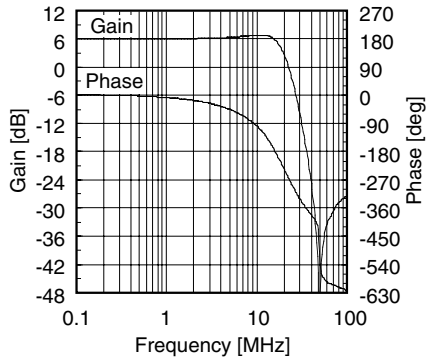


Figure 18. Gain and Phase characteristics (6dB, half fc mode, FCDATA = 227)

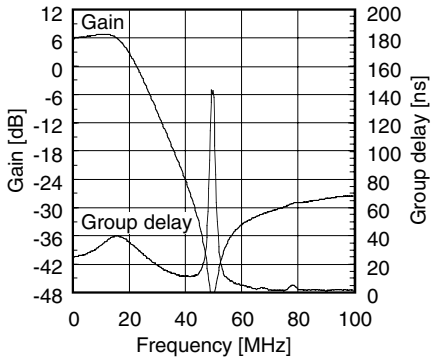


Figure 19. Gain and Group delay characteristics (6dB, half fc mode, FCDATA = 227)

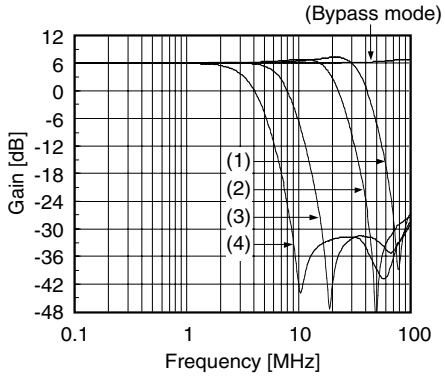


Figure 20. Gain vs. FCDATA, fc mode (6dB)

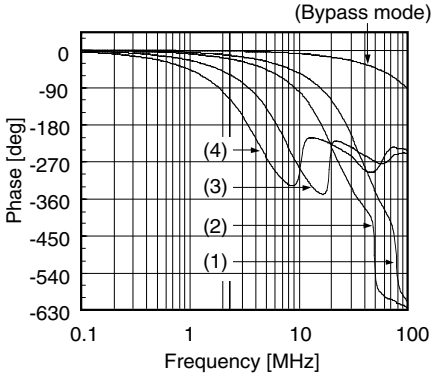


Figure 21. Phase vs. FCDATA, fc mode (6dB)

	FCDATA	fc mode
(1)	227	standard
(2)	227	half
(3)	10	standard
(4)	10	half

	FCDATA	fc mode
(1)	227	standard
(2)	227	half
(3)	10	standard
(4)	10	half

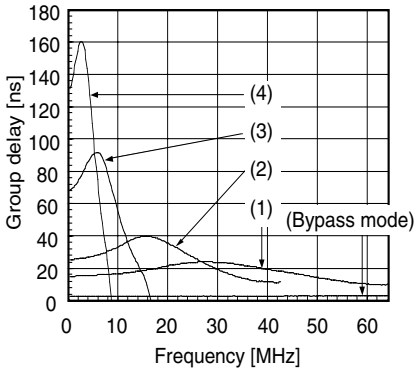


Figure 22. Group delay vs. FCDATA, fc mode (6dB)

	FCDATA	fc mode
(1)	227	standard
(2)	227	half
(3)	10	standard
(4)	10	half

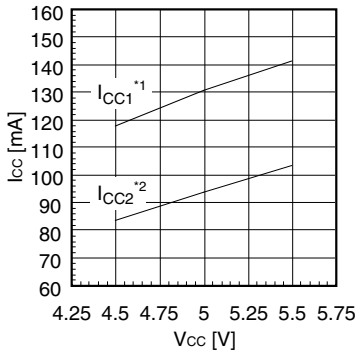


Figure 23. I_{CC1} vs. V_{CC} (6dB, FCDATA = 255)
*1. filter mode, FCDATA = 255
*2. filter bypass mode

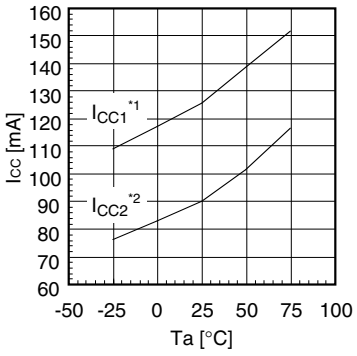


Figure 24. I_{CC1} vs. Ta (6dB, FCDATA = 255)
*1. filter mode, FCDATA = 255
*2. filter bypass mode

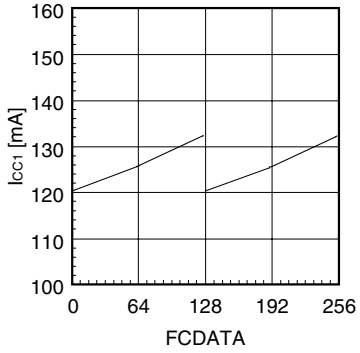


Figure 25. I_{CC1} vs. FCDATA (6dB)

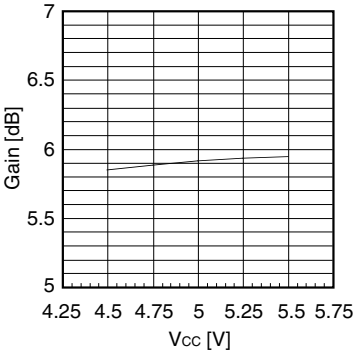


Figure 26. Gain vs. V_{CC} (6dB)

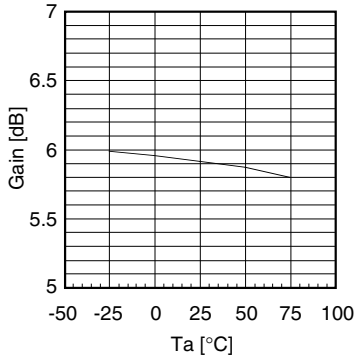


Figure 27. Gain vs. Ta (6dB)

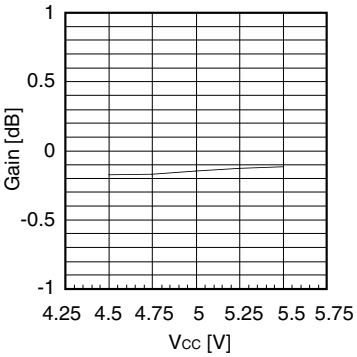


Figure 28. Gain vs. V_{CC} (0dB)

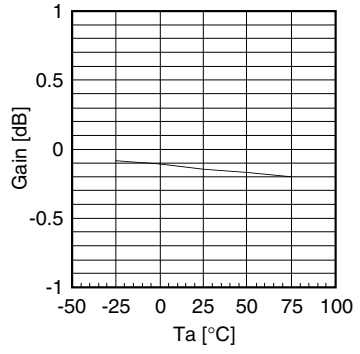


Figure 29. Gain vs. Ta (0dB)

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