SIEMENS

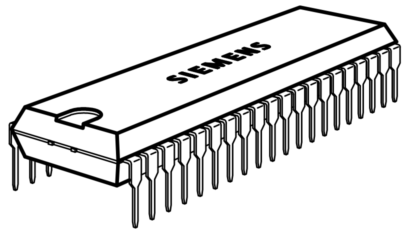
TV-Stereo Processor

TDA 6812-5

Preliminary Data **Bipolar IC**

Features

- High quality stereo signal processing
- High S/N ratio
- I^2C Bus
- Clipping detector and clock generator
- NICAM or AM sound inputs
- Volume control
- Universal audio interface for DOLBY, EQUALIZER, SURROUND SOUND features
- Multiplex 3-SCART connections
- Independent headphones



P-DIP-40-2

Type	Ordering Code	Package
TDA 6812-5	Q67000-A5127	P-DIP-40-2

TDA 6812-5 is a complete system for stereo TV-sound, controlled on an I^2C Bus. The device is made up of three functional blocks.

1. **Stereo Processing with High Quality** (better than DIN 45500; suitable for NICAM and CD for G-standard with I2C-controlled crosstalk compensation; selectable gain 0/6 dB
   a) Three stereo AF-inputs
   b) Random switching of all inputs to all outputs
   c) Stereo SCART-interface
   d) Stereo loudspeaker signal section with volume precontrol, treble/bass control, enlargement of quasi-stereo/stereo sound base, separate L/R-volume control, equalizer interface after tone control
   e) Stereo headphones signal section with Ch1/Ch2 and volume control

2. **TV-Identification-Signal Decoder**
   a) Active pilot-tone filter
   b) Phase-independent rectifier with very narrow bandwidth for identification-signal decoding
   c) Digital integrator for noise rejection
   d) Multiplexer for cyclic scanning for stereo or dual-sound identification
   e) Externally synchronized PLL for reference-signal generation: synchronization with line sync pulse or 62.5-kHz clock, integrated crystal oscillator and 4-MHz crystal, or with external 4-MHz timing signal

3. Control

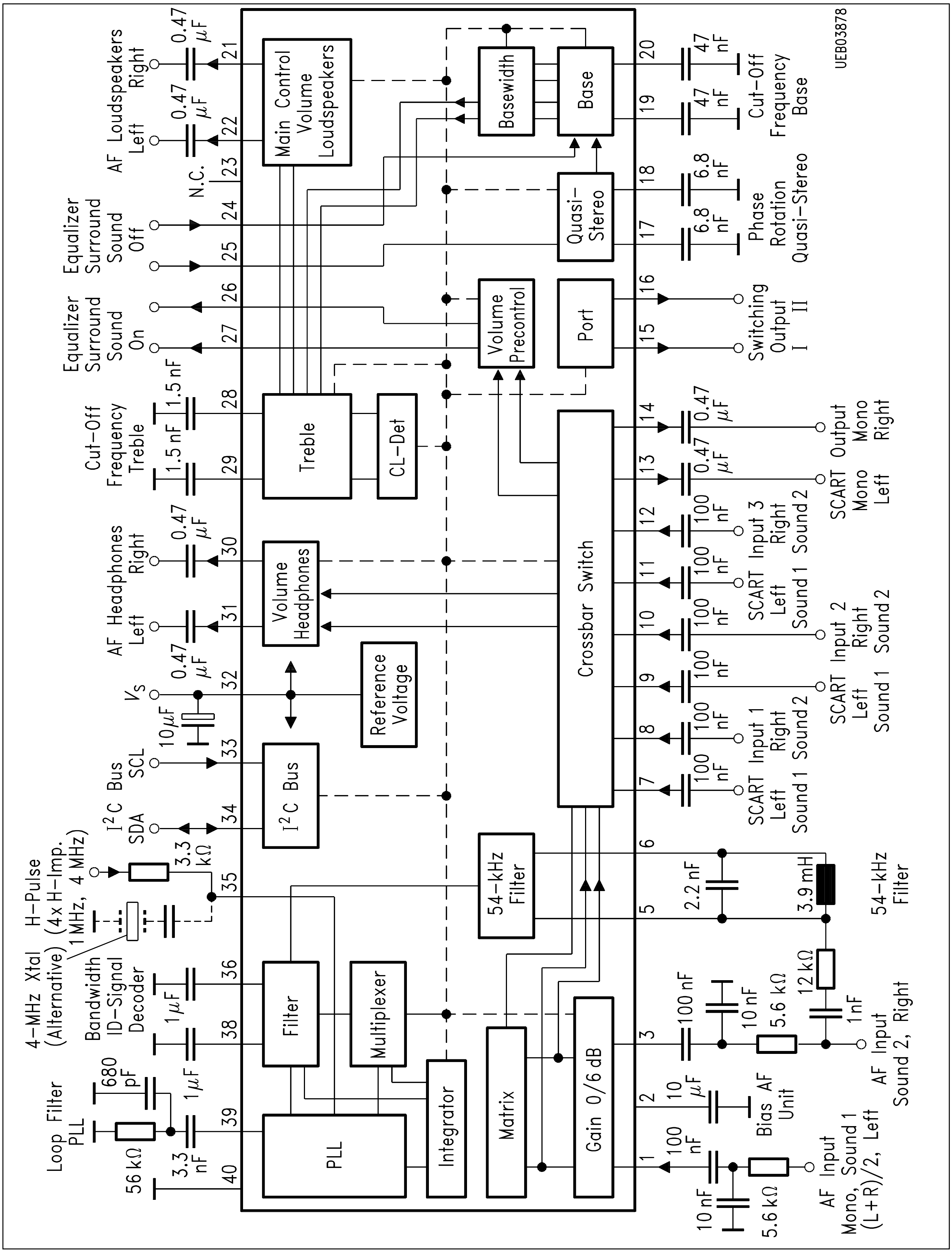
a) I²C Bus interface with listen/talk function
b) Control of entire audio processing
c) Reading of clipping detector
d) Control of identification-signal decoder
e) Reading of identification-signal decoder
f) Test modes

Pin Functions

Pin No.	Function
1	AF-input mono, left, sound 1 (adjustable)
2	Bias AF-operating point
3	AF-input, right, sound 2
4	N.C.
5	54-kHz input
6	54-kHz filter
7	SCART-input 1, left
8	SCART-input 1, right
9	SCART-input 2, left
10	SCART-input 2, right
11	SCART-input 3, left
12	SCART-input 3, right
13	AF-output SCART (mono, sound 1, left)
14	AF-output SCART (mono, sound 2, right)
15	Output port 1 (open collector)
16	Output port 2 (open collector)
17	Phase shifter quasi-stereo
18	Phase shifter quasi-stereo
19	Cut-off frequency bass (sound base), left
20	Cut-off frequency bass (sound base), right
21	AF-output, loudspeaker, right
22	AF-output, loudspeaker, left
23	N.C.
24	AF-input, volume control, right

Pin Functions (cont'd)

Pin No.	Function
25	AF-input, volume control, left
26	AF-output, equalizer, right
27	AF-output, equalizer, left
28	Cut-off frequency treble, left
29	Cut-off frequency treble, right
30	AF-output, headphones, right
31	AF-output, headphones, left
32	+ V_S (supply voltage)
33	I^2C Bus SCL
34	I^2C Bus SDA
35	Input line sync pulse (4 x H-pulse), crystal oscillator
36	Identification-signal decoder filter
37	N.C.
38	Identification-signal decoder, filter
39	Identification-signal decoder, PLL-filter
40	Ground



Block Diagram

Circuit Description

Signal Section

The dematrixing and switching of multichannel TV-sound signals are performed in the matrix and switch section by the dual-carrier method. Crosstalk compensation is on the sound 1 input. The compensation stage has a range of ± 3 dB with a smallest increment of 0.2 dB, and gain can also be switched between 0 and 6 dB. In addition to the two inputs for the demodulated sound carriers, there are three dual-channel SCART-inputs. The two matrix AF-inputs can be bypassed internally so that decoded stereo signals of other systems (NICAM) can also be processed. The switch section terminates in the SCART-output and signal paths for the loudspeaker and headphones outputs. AF-inputs can be randomly switched to AF-outputs (8-6 matrix).

In the loudpeaker signal path there is an inital volume control with a range of 0/– 15 dB and an increment of 1.25 dB. In conjunction with the main volume control that follows the tone control, very high overdriving immunity is ensured. The switchable quasi-stereo section that follows produces a stereo listening effect for mono signals through a 180 ^{o}C phase shift at mid-range frequencies (approx. 1 kHz) in one channel. The following bass control has an increment of 3 dB in its setting range of + 15/– 12 dB. The cut-off frequency for each channel is set by an external capacitor. The circuit for enlarging the stereo sound base can be cut in for stereo signals to make the aural impression even more stereo-like by frequency-dependent antiphase crosstalk of 55 %. This works with the same cut-off frequency as the bass control, but the function is largely independent. The treble control, whose cut-off frequency is also set by an external capacitor, likewise has an increment of 3 dB in a setting range of ± 12 dB. The main value control with maximum gain of 10 dB, which can be adjusted separately for L and R, terminates the loudspeaker signal path. 57 steps with an increment of 1.25 dB mean a setting range of 71.25 dB. Functions like balance or loudness are implemented by software setting of the appropriate tone and volume controls. In the tone-control section there is a clipping detector that can be read on the I^2C Bus and enables automatic volume correction by the controller. After each reading the clipping bit is reset, which enables a renewed check for clipping with each I^2C Bus read operation.

The headphones signal path includes a volume control with joint L/R-setting. 32 increments of 2 dB produce a range of 62 dB (31 x 2 dB = 62 dB).

Identification-Signal Decoder

The input of the identification-signal decoder consists of an operational amplifier for selectivity of the pilot tone and its sidebands with an external LC-circuit. The signal is fed to a phase-independent active bandpass filter of very narrow bandwidth (externally adjustable) that detects the presence of the lower sideband of the pilot carrier modulated with the identification signal. The center frequency of the filter is switched back and forth between dual and stereo by a multiplexer (software-controlled timing). The multiplexer halts when a sideband is detected. This first "detected" criterion is freed from noise by a digital integrator followed by a comparator and can then be read on the I^2C Bus (talker) as stereo or dual mode. The µC controls the signal paths. All necesssary timing signals are derived from a fast settling PLL synchronized by a reference frequency. This reference must be sufficiently identical to the horizontal frequency, **but no phase locking is necessary**. This means that it is possible to use the crystal-controlled frequency of 62.5 kHz that is often found in PLL-tuning systems. As further alternatives there is an integrated crystal oscillator that requires a 4-MHz crystal, or it is possible to use a clock frequency of 1 or 4 MHz.

Control Section

All functions are controlled by an I^2C Bus interface which can be both a listener and a talker. The currently valid data are stored in a latch block. The telegram structure is as follows:

start condition - chip address - any number of bytes - stop condition

The following conditions apply to the data bytes:

Before the actual data byte (with setting information) a subaddress byte **must always be** transmitted, which the I^2C Bus still interprets as a data byte.

Example: Headphones (HP) volume is to be increased in several steps.

Right	Wrong
Start condition Chip address 84 (Hex) Subaddress volume HP 03 (Hex) Volume Step 8 08 (Hex) Subaddress volume HP 03 (Hex) Volume step 9 09 (Hex) Subaddress volume HP 03 (Hex) Volume Step 10 0A (Hex) Stop condition	Start condition Chip address 84 (Hex) Subaddress volume HP 03 (Hex) Volume Step 8 08 (Hex) Volume step 9 09 (Hex) Volume Step 10 0A (Hex) Stop condition

Different subaddresses can be used within a telegram, ie without a new start condition. But the change between listener and talker must always be made by stop condition - start condition - chip address. A start condition and a chip address (talk) must always be transmitted before reading. This loads the data that are to be read out on the I^2C Bus interface for transfer to the µC.

Chip Address

MSB	•	•	•	•	•	•	LSB
1	0	0	0	0	1	0	R/W

R/W = 0 → Read (Listen)

R/W = 1 → Write (Talk)

Subaddress Bytes

	MSB	•	•	•	•	•	•	LSB
Volume precontrol	X	X	X	X	0	0	0	0
Volume left speaker	X	X	X	X	0	0	0	1
Volume right speaker	X	X	X	X	0	0	1	0
Volume headphones	X	X	X	X	0	0	1	1
Treble/bass	X	X	X	X	0	1	0	0
Switching byte I	X	X	X	X	0	1	1	0
Switching byte II	X	X	X	X	0	1	1	1
Switching byte III	X	X	X	X	1	0	0	0
Switching byte IV	X	X	X	X	1	0	0	1
Crosstalk compensation	X	X	X	X	0	1	0	1

Setting Bytes
a) Volume Precontrol

	MSB	•	•	•	•	•	•	LSB
Maximum volume	X	H	Q	0	0	0	0	X
Max. – 1	X	H	Q	0	0	0	1	X
Min. + 1	X	H	Q	1	0	1	1	X
Minimum volume	X	H	Q	1	1	0	0	X
Power ON	0	0	0	0	0	0	0	1

H = 0 Identification-signal decoder synchronization with f_H = 15.625 kHz; power ON
H = 1 Identification-signal decoder synchronization with 4 x f_H (must be 1 for operation with crystal or 4-MHz reference frequency)
Q = 0 PLL synchronization with line sync pulse; power ON
Q = 1 PLL synchronization with crystal oscillator (the bit for H must also be set to 1)

b) L/R-Loudspeaker Volume

	MSB	•	•	•	•	•	•	LSB
Maximum volume	X	X	1	1	1	1	1	1
Max. – 1	X	X	1	1	1	1	1	0
Max. – 15	X	X	1	1	0	0	0	0
Max. – 55	X	X	0	0	1	0	0	0
Power ON	0	0	0	0	0	0	0	1

c) Headphones Volume

	MSB	•	•	•	•	•	•	LSB
Maximum volume	T2	T1	T0	1	1	1	1	1
Max. – 1	T2	T1	T0	1	1	1	1	0
Max. – 15	T2	T1	T0	1	0	0	0	0
Max. – 31	T2	T1	T0	0	0	0	0	X
Power ON	0	0	0	0	0	0	0	1

T0, T1 and T2 are test bits and must be set to 0 for normal operation.

d) Crosstalk Compensation Matrix (sound 1)

	MSB	•	•	•	•	•	•	LSB
Maximum gain	X	X	X	1	1	1	1	1
Max. – 1	X	X	X	1	1	1	1	0
Gain 0 dB	X	X	X	1	0	0	0	0
Minimum gain	X	X	X	0	0	0	0	1
Minimum gain	X	X	X	0	0	0	0	X
Power ON	X	X	X	0	0	0	0	1

e) Treble / Bass

	MSB	•	•	•	•	•	•	LSB
Linear	1	0	0	0	1	0	0	0
Max. treble, lin. bass	1	1	0	0	1	0	0	0
Max. treble, lin. bass	1	1	X	X	1	0	0	0
Min. treble, lin. bass	0	1	0	0	1	0	0	0
Min. treble, lin. bass	0	0	X	X	1	0	0	0
Lin. treble, max. bass	1	0	0	0	1	1	0	1
Lin. treble, max. bass	1	0	0	0	1	1	X	1
Lin. treble, max. bass	1	0	0	0	1	1	1	X
Lin. treble, min. bass	1	0	0	0	0	1	0	0
Lin. treble, min. bass	1	0	0	0	0	0	X	X
Max. treble, max. bass	1	1	X	X	1	1	X	1
Min. treble, min. bass	0	0	X	X	0	0	X	X
Power ON	0	0	0	0	0	0	0	1
	MSB treble			LSB treble	MSB bass			LSB bass

f) Switching Bytes I, II, III

Switching Byte I	SCART-output
Switching byte II	Headphones output
Switching byte III	Loudspeaker output

MSB	•	•	•	•	•	•	LSB	
L3 0	L2 0	L1 0	L0 0	R3 0	R2 0	R1 0	R0 1	Power ON

L0 thru L3 left output, R0 thru 3 right output.

L3	**L2**	**L1**	**L0**	**Selected Input**
0	0	0	0	MUTE
0	0	0	1	AF-input left, mono, sound 1
0	0	1	0	AF-input right, sound 2
0	0	1	1	AF-input left, dematrixed
0	1	0	0	SCART 1 left
0	1	0	1	SCART 1 right
0	1	1	0	SCART 2 left
0	1	1	1	SCART 2 right
1	0	0	0	SCART 3 left
1	0	0	1	SCART 3 right

Assignment R3 thru R0 is identical to L3 thru L0.

g) Switching Byte IV

MSB	•	•	•	•	•	•	LSB
MPX0	MPX1	QSt	BE	Mono	P1	P2	Matrix

MPX0	MPX1	MPX-Period		Recommended $C_{36,38}$	Perm. Xtal Tolerances
0	0	2 s	Power-ON	1 µF	± 20 ppm
0	1	4 s		2.2 µF	± 10 ppm
1	0	8 s		4.7 µF	± 5 ppm

Settings specially recommended for crystal operation				
0	0	2 s	470 nF	± 40 ppm
0	1	4 s	330 nF	± 70 ppm

MXP-period = 2 s means that identification-signal decoder searches 1 s for dual and 1 s for stereo. It is basically permissible, for the given $C_{36,38}$, to make the MPX period longer, but not shorter.

QSt	=	0	Quasi-stereo OFF; power ON
QSt	=	1	Quasi-stereo ON
BE	=	0	Stereo base enlargement OFF; power ON
BE	=	1	Stereo base enlargement ON
Mono	=	0	Identification-signal decoder set to stereo and held; power ON
Mono	=	1	Normal operation of identification-signal decoder
P1	=	0	Port 1 (open collector) low (low-impedance); power ON
P1	=	1	Port 1 high (high impedance)
P2	=	0	Port 2 (open collector) low (low-impedance); power ON
P2	=	1	Port 2 high (high impedance)
Matrix	=	0	Gain matrix 0 dB
Matrix	=	1	Gain matrix 6 dB; power ON

h) Talk Mode

MSB	•	•	•	•	•	•	LSB
St	D	T3	T4	T5	CL	X	X
0	0	Decoder detects mono					
1	0	Decoder detects stereo					
0	1	Decoder detects dual					
1	1	Suppressed internally					

CL = 1 Loudspeaker signal path at clipping limit
(CL is automatically reset after each reading operation)

T3 thru T5 are test bits.

Absolute Maximum Ratings

T_A = 0 to 70 °C; all voltages relatives to V_{SS}

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Supply voltage	V_{21}	0	14	V	
Max. DC-voltage	V_1	0	V_{32}	V	
Max. DC-voltage	V_2	0	V_{32}	V	
Max. DC-voltage	V_3	0	V_{32}	V	
Max. DC-voltage	V_5	0	V_{32}	V	
Max. DC-voltage	V_7	0	V_{32}	V	
Max. DC-voltage	V_8	0	V_{32}	V	
Max. DC-voltage	V_9	0	V_{32}	V	
Max. DC-voltage	V_{10}	0	V_{32}	V	
Max. DC-voltage	V_{11}	0	V_{32}	V	
Max. DC-voltage	V_{12}	0	V_{32}	V	
Max. DC-voltage	V_{15}	0	V_{32}	V	
Max. DC-voltage	V_{16}	0	V_{32}	V	
Max. DC-voltage	V_{17}	0	V_{32}	V	
Max. DC-voltage	V_{18}	0	V_{32}	V	
Max. DC-voltage	V_{19}	0	V_{32}	V	
Max. DC-voltage	V_{20}	0	V_{32}	V	
Max. DC-voltage	V_{24}	0	V_{32}	V	
Max. DC-voltage	V_{25}	0	V_{32}	V	
Max. DC-voltage	V_{28}	0	V_{32}	V	
Max. DC-voltage	V_{29}	0	V_{32}	V	
Max. DC-voltage	V_{33}	0	V_{32}	V	
Max. DC-voltage	V_{34}	0	V_{32}	V	
Max. DC-voltage	V_{36}	0	V_{32}	V	
Max. DC-voltage	V_{38}	0	V_{32}	V	
Max. DC-current	I_6	0	2	mA	
Max. DC-current	I_{13}	0	2	mA	
Max. DC-current	I_{14}	0	2	mA	
Max. DC-current	I_{21}	0	2	mA	
Max. DC-current	I_{22}	0	2	mA	
Max. DC-current	I_{26}	0	2	mA	
Max. DC-current	I_{27}	0	2	mA	
Max. DC-current	I_{30}	0	2	mA	
Max. DC-current	I_{31}	0	2	mA	
Max. DC-current	I_{35}	0	2	mA	
Max. DC-current	I_{39}	0	2	mA	
ESD-voltage	V_{ESD}	– 2	2	kV	HBM (R = 1.5 kΩ, C = 100 pF)

Absolute Maximum Ratings (cont'd)

T_A = 0 to 70 °C; all voltages relatives to V_{SS}

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
ESD-voltage	$V_{ESD7-14}$	– 6	6	kV	HBM (R = 1.5 kΩ, C = 100 pF)
Junction temperature	T_j		150	°C	
Storage temperature	T_{stg}	– 40	125	°C	
Thermal resistance system ambient	$R_{th\ SA}$		38	K/W	

Operating Range

Parameter	Symbol	min.	max.	Unit	Remarks
Supply voltage	V_{32}	10	13.2	V	
Ambient temperature	T_A	0	70	°C	
Input frequency range	f_I	0.01	20	kHz	

Characterstics

V_S = 12 V; T_A = 25 °C; AF-reference level 0 dB = 250 mVrms unless otherwise defined; in accordance with test circuit 1.

I²C Bus preset:
Start - 84 - 01,3F - 02,3F - 00,00-03,1F - 04,88 - 05,10 - 06,12-07,12-08,12-09,00-Stop
Chip address - *Vol* $_{LSl}$ *63 - Vol* $_{LSr}$ *63 - Vol* $_{Pre}$ *0 - Vol* $_{HP}$ *31 - Tone lin - Gain 0 dB - Switch byte I, II, II, IV*

The basic setting for each item in the specifications is always preset; the test conditions only state settings that differ. Details in *italics* are for explanation of the hex codes, for switching bits only set bits or functions are given.5

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Current consumption	I_{32}		58	85	mA	

Signal Section

Parameter	Symbol	min.	typ.	max.	Unit	Test Condition
Max. gain	V_{22-1}	– 2	0	2	dB	
Max. gain	V_{21-3}	– 2	0	2	dB	
Max. gain	V_{27-1}	– 2	0	2	dB	
Max. gain	V_{26-3}	– 2	0	2	dB	
Max. gain	V_{31-1}	– 2	0	2	dB	
Max. gain	V_{30-3}	– 2	0	2	dB	
Gain	V_{13-1}	– 2	0	2	dB	
Gain	V_{14-3}	– 2	0	2	dB	
Max. gain	V_{22-3}	– 2	0	2	dB	08,32; *Stereo;* V_1 = 0
Max. gain	V_{21-3}	– 2	0	2	dB	08,32; *Stereo;* V_1 = 0
Max. gain	V_{27-3}	– 2	0	2	dB	08,32; *Stereo;* V_1 = 0
Max. gain	V_{26-3}	– 2	0	2	dB	08,32; *Stereo;* V_1 = 0
Max. gain	V_{31-3}	– 2	0	2	dB	07,32; *Stereo;* V_1 = 0
Max. gain	V_{30-3}	– 2	0	2	dB	07,32; *Stereo;* V_1 = 0
Max. gain	V_{22-1}	4	6	8	dB	08,32; *Stereo;* V_3 = 0
Max. gain	V_{27-1}	4	6	8	dB	08,32; *Stereo;* V_3 = 0
Max. gain	V_{31-1}	4	6	8	dB	07,32; *Stereo;* V_3 = 0
Gain	V_{13-3}	– 2	0	2	dB	06,32; *Stereo*; V_1 = 0
Gain	V_{13-1}	4	6	8	dB	06,32; *Stereo*; V_3 = 0
Max. gain	V_{22-1}	4	6	8	dB	09,01; *6 dB*
Max. gain	V_{21-3}	4	6	8	dB	09,01; *6 dB*
Max. gain	V_{27-1}	4	6	8	dB	09,01; *6 dB*
Max. gain	V_{26-3}	4	6	8	dB	09,01; *6 dB*
Max. gain	V_{31-1}	4	6	8	dB	09,01; *6 dB*
Max. gain	V_{30-3}	4	6	8	dB	09,01; *6 dB*

Characteristics (cont'd)

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Gain Gain	$V_{13\text{-}3}$ $V_{14\text{-}3}$	4 4	6 6	8 8	dB dB	09,01; *6 dB* 09,01; *6 dB*
Max. gain	$V_{22\text{-}3}$	4	6	8	dB	08,32-09,01; $V_1 = 0$ *Stereo; 6 dB*
Max. gain	$V_{21\text{-}3}$	4	6	8	dB	08,32-09,01; $V_1 = 0$ *Stereo; 6 dB*
Max. gain	$V_{27\text{-}3}$	4	6	8	dB	08,32-09,01; $V_1 = 0$ *Stereo; 6 dB*
Max. gain	$V_{26\text{-}3}$	4	6	8	dB	08,32-09,01; $V_1 = 0$ *Stereo; 6 dB*
Max. gain	$V_{31\text{-}3}$	4	6	8	dB	07,32-09,01; $V_1 = 0$ *Stereo; 6 dB*
Max. gain	$V_{30\text{-}3}$	4	6	8	dB	07,32-09,01; $V_1 = 0$ *Stereo; 6 dB*
Max. gain	$V_{22\text{-}1}$	10	12	14	dB	08,32-09,01; $V_3 = 0$ *Stereo; 6 dB*
Max. gain	$V_{27\text{-}1}$	10	12	14	dB	08,32-09,01; $V_3 = 0$ *Stereo; 6 dB*
Max. gain	$V_{31\text{-}1}$	10	12	14	dB	07,32-09,01; $V_3 = 0$ *Stereo; 6 dB*
Gain	$V_{13\text{-}3}$	4	6	8	dB	06,32-09,01; $V_1 = 0$ *Stereo; 6 dB*
Gain	$V_{13\text{-}1}$	10	12	14	dB	06,32-09,01; $V_3 = 0$ *Stereo; 6 dB*
Max. gain	$V_{22\text{-}7}$	– 2	0	2	dB	08,45; *SCART*
Max. gain	$V_{21\text{-}8}$	– 2	0	2	dB	08,45; *SCART*
Max. gain	$V_{27\text{-}7}$	– 2	0	2	dB	08,45; *SCART*
Max. gain	$V_{26\text{-}8}$	– 2	0	2	dB	08,45; *SCART*
Max. gain	$V_{31\text{-}7}$	– 2	0	2	dB	07,45; *SCART*
Max. gain	$V_{30\text{-}8}$	– 2	0	2	dB	07,45; *SCART*
Gain	$V_{13\text{-}7}$	– 2	0	2	dB	06,45; *SCART*
Gain	$V_{14\text{-}8}$	– 2	0	2	dB	06,45; *SCART*
Same values apply for pins 9 thru 12						
Min. gain main control	$V_{22\text{-}1}$		– 70	– 65	dB	01,08-02,08 *Vol* $_{LSl}$ *8-Vol* $_{LSr}$ *8*
Min. gain main control	$V_{21\text{-}3}$		– 70	– 65	dB	01,08-02,08 *Vol* $_{LSl}$ *8-Vol* $_{LSr}$ *8*
Min. gain precontrol	$V_{22\text{-}1}$	– 17	– 15	– 13	dB	01,08-02,08 *Vol* $_{Pre}$ *24*
Min. gain precontrol	$V_{21\text{-}3}$	– 17	– 15	– 13	dB	01,08-02,08 *Vol* $_{Pre}$ *24*

Characteristics (cont'd)

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Same values apply for pins 7 thru 12						
Min. gain Min. gain	$V_{31\text{-}1}$ $V_{30\text{-}3}$		– 62 – 62	– 57 – 57	dB dB	03,01; *Vol* $_{HP}$ *1* 03,01; *Vol* $_{HP}$ *1*
Same values apply for pins 7 thru 12						
Flutter and wow	$\Delta V_{21\text{-}22}$			± 2	dB	01,3F-01,24 02,3F-02,24 *Vol* $_{LSl}$ *63-36-Vol* $_{LSr}$ *63-36*
Flutter and wow	$\Delta V_{30\text{-}31}$			± 2	dB	03,1F-03,13 *Vol* $_{HP}$ *31-19*
Increment Vol $_{22}$	ΔV_{22}	0	1.25	2.5	dB	01,X-01, (X ± 1) *Vol* $_{LSl}$ *X-Vol* $_{LSl}$ *(X ± 1)*
Increment Vol $_{21}$	ΔV_{21}	0	1.25	2.5	dB	01,X-01, (X ± 1) *Vol* $_{LSr}$ *X-Vol* $_{LSr}$ *(X ± 1)*
Increment Vol $_{22}$	ΔV_{22}	0	1.25	2.5	dB	01,X-01, (X ± 1) *Vol* $_{Pre}$ *X-Vol* $_{Pre}$ *(X ± 1)*
Increment Vol $_{21}$	ΔV_{21}	0	1.25	2.5	dB	01,X-01, (X ± 1) *Vol* $_{Pre}$ *X-Vol* $_{Pre}$ *(X ± 1)*
Increment Vol $_{30}$	ΔV_{30}	0	2	4	dB	01,X-01, (X ± 1) *Vol* $_{HP}$ *X-Vol* $_{HP}$ *(X ± 1)*
Increment Vol $_{31}$	ΔV_{31}	0	2	4	dB	03,X-03, (X ± 1) *Vol* $_{HP}$ *X-Vol* $_{HP}$ *(X ± 1)*
Matrix adjustment	$V_{22\text{-}1}$	2.5	3	3.5	dB	05,1F; *Gain max*
Matrix adjustment	$V_{31\text{-}1}$	2.5	3	3.5	dB	05,1F; *Gain max*
Matrix adjustment	$V_{13\text{-}1}$	2.5	3	3.5	dB	05,1F; *Gain max*
Matrix adjustment	$V_{22\text{-}1}$	– 3.5	– 3	– 2.5	dB	05,01; *Gain max*
Matrix adjustment	$V_{31\text{-}1}$	– 3.5	– 3	– 2.5	dB	05,01; *Gain max*
Matrix adjustment	$V_{13\text{-}1}$	– 3.5	– 3	– 2.5	dB	05,01; *Gain max*
Adj. increment	ΔV_{22}	0.1	0.2	0.3	dB	05,X-05, (X ± 1) *Gain X-Gain (X ± 1)*
Adj. increment	ΔV_{31}	0.1	0.2	0.3	dB	05,X-05, (X ± 1) *Gain X-Gain (X ± 1)*
Adj. increment	ΔV_{13}	0.1	0.2	0.3	dB	05,X-05, (X ± 1) *Gain X-Gain (X ± 1)*

Characteristics (cont'd)

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Bass boost	$V_{31\text{-}1}$	13	15		dB	04,8F; f_{I} = 40 Hz *Bass max, Treble lin*
Bass boost	$V_{21\text{-}3}$	13	15		dB	04,8F; f_{I} = 40 Hz *Bass max, Treble lin*
Bass cutoff	$V_{31\text{-}1}$		– 12		dB	04,80; f_{I} = 40 Hz *Bass max, Treble lin*
Bass cutoff	$V_{21\text{-}3}$		– 12		dB	04,80; f_{I} = 40 Hz *Bass max, Treble lin*
Increment bass	ΔV_{21}	1	3	5	dB	04,8X-04.8 (X ± 1) *Bass X-Bass (X ± 1)*
Increment bass	ΔV_{22}	1	3	5	dB	04,8X-04.8 (X ± 1) *Bass X-Bass (X ± 1)*
Treble boost	$V_{22\text{-}1}$	10	12		dB	04,8F; f_{I} = 15 kHz *Treble max, Bass lin*
Treble boost	$V_{21\text{-}3}$	10	12		dB	04,8F; f_{I} = 15 kHz *Treble max, Bass lin*
Treble cut-off	$V_{22\text{-}1}$		– 12		dB	04,8F; f_{I} = 15 kHz *Treble max, Bass lin*
Treble cut-off	$V_{21\text{-}3}$		– 12		dB	04,8F; f_{I} = 15 kHz *Treble max, Bass lin*
Increment treble	ΔV_{21}	1	3	5	dB	04,8X-04, (X ± 1) 8 *Treble X-Treble (X ± 1)*
Increment treble	ΔV_{22}	1	3	5	dB	04,8X-04, (X ± 1) 8 *Treble X-Treble (X ± 1)*
Sound linearity	ΔV_{21}			± 2	dB	04,88; f_{I} = 40 Hz – 15 kHz *Treble, Bass lin*
Sound linearity	ΔV_{22}			± 2	dB	04,88; f_{I} = 40 Hz – 15 kHz *Treble, Bass lin*
Response threshold of clipping detector	V_1		580		mVrms	04,8F; f_{I} = 40 Hz *Treble lin, Bass max* 01,2F-02,2F *Vol* $_{\mathrm{LSl}}$ *47-Vol* $_{\mathrm{LSr}}$ *47*
Same values apply for pins 3 and 7 thru 12						
Channel separation	$\Delta V_{21\text{-}22}$	50			dB	V_3 or V_1 = 600 mVrms
Channel separation	$\Delta V_{30\text{-}31}$	50			dB	V_3 or V_1 = 600 mVrms
Channel separation	$\Delta V_{13\text{-}14}$	50			dB	V_3 or V_1 = 600 mVrms

Characteristics (cont'd)

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Crosstalk attenuation	$\alpha_{IN/OW}$	60			dB	V_{IW} = 0; $V_{IN1,3}$ = 600 mVrms; V_{IN7-12} = 2 Vrms
Muting	α_{1-22}	80			dB	08,0X; V_1 = 600 mVrms *MUTE L*
Muting	α_{3-21}	80			dB	08,0X; V_3 = 600 mVrms *MUTE R*
Muting	α_{1-27}	80			dB	08,0X; V_1 = 600 mVrms *MUTE L*
Muting	α_{3-26}	80			dB	08,0X; V_3 = 600 mVrms *MUTE R*
Muting	α_{1-31}	80			dB	07,0X; V_1 = 600 mVrms *MUTE L*
Muting	α_{3-30}	80			dB	07,0X; V_3 = 600 mVrms *MUTE R*
Muting	α_{3-14}	80			dB	06,0X; V_3 = 600 mVrms *MUTE R*
Muting	α_{1-13}	80			dB	06,0X; V_1 = 600 mVrms *MUTE L*
Same values apply for pins 7 thru 12; V_{7-12} = 2 Vrms						
Max. input voltage	V_3*	600			mVrms	$V_{21} \leq 1$ %
Max. input voltage	V_1	600			mVrms	$V_{22} \leq 1$ %
Max. input voltage	V_1	300			mVrms	$V_{22} \leq 1$ %; *stereo*
Max. input voltage	V_3*	300			mVrms	$V_{21} \leq 1$ %; 09,01; *6 dB*
Max. input voltage	V_1	300			mVrms	$V_{22} \leq 1$ %; 09,01; *6 dB*
Max. input voltage	V_1	150			mVrms	$V_{22} \leq 1$ %; 09,01; *6 dB; stereo*
* V_{IN} in mono mode without SC2 V_3 = 2 Vrms and 1 Vrms						
Max. input voltage	V_{24}	3.4			Vrms	$V_{21} \leq 1$ %
Max. input voltage	V_{25}	3.4			Vrms	$V_{22} \leq 1$ %
Max. input voltage	V_7*	2			Vrms	$V_{22} \leq 3$ %
Max. input voltage	V_8*	2			Vrms	$V_{21} \leq 3$ %
* Full tone control possible when 00,18; *Vol* $_{Pre}$ *24* Same values apply for pins 9 thru 12						
Distortion factor	THD_{30}		0.01	0.1	%	V_3 = 250 mVrms
Distortion factor	THD_{31}		0.01	0.1	%	V_1 = 250 mVrms
Distortion factor	THD_{30}		0.01	0.1	%	V_3 = 250 mVrms; 03,15 *Vol* $_{HP}$ *21*
Distortion factor	THD_{31}		0.01	0.1	%	V_3 = 250 mVrms *Vol* $_{HP}$ *21*
Same values apply for pins 7 thru 12; V_{7-12} = 600 mVrms						

Characteristics (cont'd)

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Distortion factor	THD_{22}		0.01	0.1	%	V_1 = 250 mVrms
Distortion factor	THD_{21}		0.01	0.1	%	V_3 = 250 mVrms
Distortion factor	THD_{22}		0.01	0.2	%	V_1 = 0.25 Vrms 01,2F-02,2F *Vol* $_{LSl}$ *47-Vol* $_{LSr}$ *47*
Distortion factor	THD_{21}		0.01	0.2	%	V_3 = 0.25 Vrms 01,2F-02,2F *Vol* $_{LSl}$ *47-Vol* $_{LSr}$ *47*
Distortion factor	THD_{22}		0.01	0.4	%	V_1 = 250 mVrms; 04.XX *Tone random*
Distortion factor	THD_{21}		0.01	0.4	%	V_3 = 250 mVrms; 04.XX *Tone random*
Same values apply for pins 7 thru 12; $V_{7\text{-}12}$ = 600 mVrms						
Distortion factor	THD_{14}		0.01	0.1	%	V_3 = 250 mVrms
Distortion factor	THD_{13}		0.01	0.1	%	V_1 = 250 mVrms
Same values apply for pins 7 thru 12; $V_{7\text{-}12}$ = 600 mVrms						
Antiphase crosstalk sound base	$\Delta V_{22\text{-}21}$	0.5	0.55			V_3 = 600 mVrms; f_l = 2 kHz; 09,10 *Base*
Antiphase crosstalk sound base	$\Delta V_{21\text{-}22}$	0.5	0.55			V_3 = 600 mVrms; f_l = 2 kHz; 09,10 *Base*
Sound base phase	$\Phi_{21\text{-}22}$	150	180	210	deg	V_1 = 600 mVrms; 09,10 *Base*; *f* = 2 kHz
Sound base phase	$\Phi_{22\text{-}21}$	150	180	210	deg	V_3 = 600 mVrms; 09,10 *Base*; *f* = 2 kHz
Phase rotation quasi stereo	$\Phi_{22\text{-}21}$	0	10	40	deg	V_3,1 = 600 mVrms; 09,20; *QSt*; *f* = 40 Hz
	$\Phi_{22\text{-}21}$	130	180	230	deg	V_3,1 = 600 mVrms; 09,20; *QSt*; *f* = 700 Hz
	$\Phi_{22\text{-}21}$	– 30	10	0	deg	V_3,1 = 600 mVrms; 09,20; *QSt*; *f* = 15 kHz

Characteristics (cont'd)

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Unweighted SNR	$\alpha_{S/N22}$	90	97		dB	$V_{Nrms\ 20\ Hz\text{-}20\ kHz}$; V_1 = 0.6 Vrms
Unweighted SNR	$\alpha_{S/N21}$	90	97		dB	$V_{Nrms\ 20\ Hz\text{-}20\ kHz}$; V_1 = 0.6 Vrms
Unweighted SNR	$\alpha_{S/N22}$	70	80		dB	$V_{Nrms\ 20\ Hz\text{-}20\ kHz}$; V_1 = 0.6 Vrms 01,27-02,27 *Vol* $_{LSl}$ *39-Vol* $_{LSr}$ *39*
Unweighted SNR	$\alpha_{S/N21}$	70	80		dB	$V_{Nrms\ 20\ Hz\text{-}20\ kHz}$; V_1 = 0.6 Vrms 01,27-02,27 *Vol* $_{LSl}$ *39-Vol* $_{LSr}$ *39*
Noise voltage	V_{N22}		2	10	µVrms	$V_{Nrms\ 20\ Hz\text{-}20\ kHz}$; 01,00-02,00 *Vol* $_{LSl}$ *0-Vol* $_{LSr}$ *0*
Noise voltage	V_{N21}		2	10	µVrms	$V_{Nrms\ 20\ Hz\text{-}20\ kHz}$; 01,00-02,00 *Vol* $_{LSl}$ *0-Vol* $_{LSr}$ *0*
Unweighted SNR	$\alpha_{S/N31}$	90	97		dB	$V_{Nrms\ 20\ Hz\text{-}20\ kHz}$; V_1 = 0.6 Vrms
Unweighted SNR	$\alpha_{S/N30}$	90	97		dB	$V_{Nrms\ 20\ Hz\text{-}20\ kHz}$; V_3 = 0.6 Vrms
Unweighted SNR	$\alpha_{S/N31}$	70	80		dB	$V_{Nrms\ 20\ Hz\text{-}20\ kHz}$; V_1 = 0.6 Vrms 03,10; *Vol* $_{HP}$ *16*
Unweighted SNR	$\alpha_{S/N30}$	70	80		dB	$V_{Nrms\ 20\ Hz\text{-}20\ kHz}$; V_3 = 0.6 Vrms 03,10; *Vol* $_{HP}$ *16*
Noise voltage	V_{N31}		2	10	µVrms	$V_{Nrms\ 20\ Hz\text{-}20\ kHz}$; 03,00; *Vol* $_{HP}$ *0*
Noise voltage	V_{N30}		2	10	µVrms	$V_{Nrms\ 20\ Hz\text{-}20\ kHz}$; 03,00; *Vol* $_{HP}$ *0*
Unweighted SNR	$\alpha_{S/N13}$	90	97		dB	$V_{Nrms\ 20\ Hz\text{-}20\ kHz}$; V_1 = 0.6 Vrms
Unweighted SNR	$\alpha_{S/N14}$	90	97		dB	$V_{Nrms\ 20\ Hz\text{-}20\ kHz}$; V_3 = 0.6 Vrms

Characteristics (cont'd)

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
DC transition Δ 1 bit	ΔV_{22}			± 10	mV	01,X-01,X ± 1 *Vol* $_{LSl}$ *X-Vol* $_{LSl}$ *(X ± 1)*
DC transition Δ 1 bit	ΔV_{21}			± 10	mV	02,X-02, X ± 1 *Vol* $_{LSr}$ *X-Vol* $_{LSr}$ *(X ± 1)*
DC transition Δ 1 bit	ΔV_{22}			± 10	mV	00,X-04, X ± 1 *Vol* $_{Pre}$ *X-Vol* $_{Pre}$ *(X ± 1)*
DC transition Δ 1 bit	ΔV_{21}			± 10	mV	00,X-04, X ± 1 *Vol* $_{Pre}$ *X-Vol* $_{Pre}$ *(X ± 1)*
DC transition Δ 1 bit	ΔV_{22}			± 10	mV	04,X-05, X ± 1 *Tone X-Tone (X ± 1)*
DC transition Δ 1 bit	ΔV_{21}			± 10	mV	04,X-05, X ± 1 *Tone X-Tone (X ± 1)*
DC transition Δ 1 bit	ΔV_{30}			± 10	mV	03,X-03, X ± 1 *Vol* $_{HP}$ *X-Vol* $_{HP}$ *(X ± 1)*
DC transition Δ 1 bit	ΔV_{31}			± 10	mV	03,X-03, X ± 1 *Vol* $_{HP}$ *X-Vol* $_{HP}$ *(X ± 1)*

Design-Related Data

Input resistance	R_1	22			kΩ	
Input resistance	R_3	22			kΩ	
Input resistance	R_7	25			kΩ	
Input resistance	R_8	25			kΩ	
Input resistance	R_9	25			kΩ	
Input resistance	R_{10}	25			kΩ	
Input resistance	R_{11}	25			kΩ	
Input resistance	R_{12}	25			kΩ	
Output resistance	R_{13}			60	Ω	
Output resistance	R_{14}			60	Ω	
Output resistance	R_{21}			60	Ω	
Output resistance	R_{22}			60	Ω	
Output resistance	R_{26}			200	Ω	
Output resistance	R_{27}			200	Ω	
Output resistance	R_{30}			200	Ω	
Output resistance	R_{31}			200	Ω	

Characteristics (cont'd)

Parameter	Symbol	Limit Values			Unit	Test Condition	Test Circuit
		min.	typ.	max.			
Identification-Signal Decoder							
Gain filter op-amp	V_6	13	14	15	dB	V_{IF} = 80 mVpp	1
Max. input voltage	V_6	600			mVpp	Function	2
VCO voltage PLL	V_{39}	1.3			V	f_{35} = 14.6 kHz; V_{35} = 2.5 V	2
VCO voltage PLL	V_{39}	2	3	4	V	f_{35} = 15.625 kHz; V_{35} = 2.5 V	2
VCO voltage PLL	V_{39}			4.7	V	f_{35} = 16.6 kHz; V_{35} = 2.5 V	2
VCO voltage PLL	V_{39}	1.3			V	f_{35} = 58.4 kHz; V_{35} = 2.5 V 00,40, *Line sync*	2
VCO voltage PLL	V_{39}			4.7	V	f_{35} = 66.4 kHz; V_{35} = 2.5 V 00,40, *Line sync*	2
VCO voltage PLL	V_{39}	2	3	4	V	00,40, *Line sync; Xtal*	4

$$V_{\text{ID filter}} = \frac{\sqrt{\langle V_{36} - V_{36}{*}\rangle^2 + \langle V_{38} - V_{38}{*}\rangle^2}}{V_6}$$

V_{36} or V_{38} when $V_6 = 0$
V_{36}* or V_{38}* when V_6 = 100 mVpp; m = 50 %

Parameter	Symbol	min.	typ.	max.	Unit	Test Condition	Test Circuit
Gain identification-signal filter	V_{ISF}	3.4		6.8	dB	f_6 = pilot signal: dual I²C-talk: dual	
Gain identification-signal filter	V_{ISF}	3.4		6.8	dB	f_6 = pilot signal: stereo; I²C-talk: stereo	
$V_{36\ \text{test}} = V_{36}\ (V_5 = 0) \pm \Delta V_{36}$; $V_{38\ \text{test}} = V_{38}\ (V_6 = 0) \pm \Delta V_{38}$							
Detection threshold	ΔV_{36}	900			mV	I²C-talk: stereo or dual	3
Detection threshold	$-\Delta V_{36}$	900			mV	I²C-talk: stereo or dual	3
Detection threshold	ΔV_{38}	900			mV	I²C-talk: stereo or dual	3
Detection threshold	$-\Delta V_{38}$	900			mV	I²C-talk: stereo or dual	3

Characteristics (cont'd)

Parameter	Symbol	Limit Values			Unit	Test Condition	Test Circuit
		min.	typ.	max.			
Mono threshold	ΔV_{36}	0		100	mV	I^2C-talk: mono	3
Mono threshold	$-\Delta V_{36}$	0		100	mV	I^2C-talk: mono	3
Mono threshold	ΔV_{38}	0		100	mV	I^2C-talk: mono	3
Mono threshold	$-\Delta V_{38}$	0		100	mV	I^2C-talk: mono	3
Detection response	t_{det}	0.25		0.5	t_{MPX}	I^2C-talk: stereo or dual; $\pm\Delta V_{36}$ = 1 V	3
Detection response	t_{det}	0.25		0.5	t_{MPX}	I^2C-talk: stereo or dual; $\pm\Delta V_{38}$ = 1 V	3
Switching threshold f_{REF}-input	$V_{H\text{-}IL}$	0		1.5	V		2
Switching threshold f_{REF}-input	$V_{H\text{-}IH}$	3.5		V_{21}	V		2
Amplitude crystal oscillator	V_{35}*		2		Vpp	to = 4.00000 MHz Series rsonance	4
External 1-MHz or 4-MHz clock	V_{35}		0.3		Vpp		3
Multiplexer clock	t_{MPX}		1.08		s	09,C8, *MPX = 1 s*	
Multiplexer clock	t_{MPX}		2.17		s	09,08, *MPX = 2 s*	
Multiplexer clock	t_{MPX}		4.34		s	09,48, *MPX = 4 s*	
Multiplexer clock	t_{MPX}		8.68		s	09,88, *MPX = 8 s*	

Design-Related Data

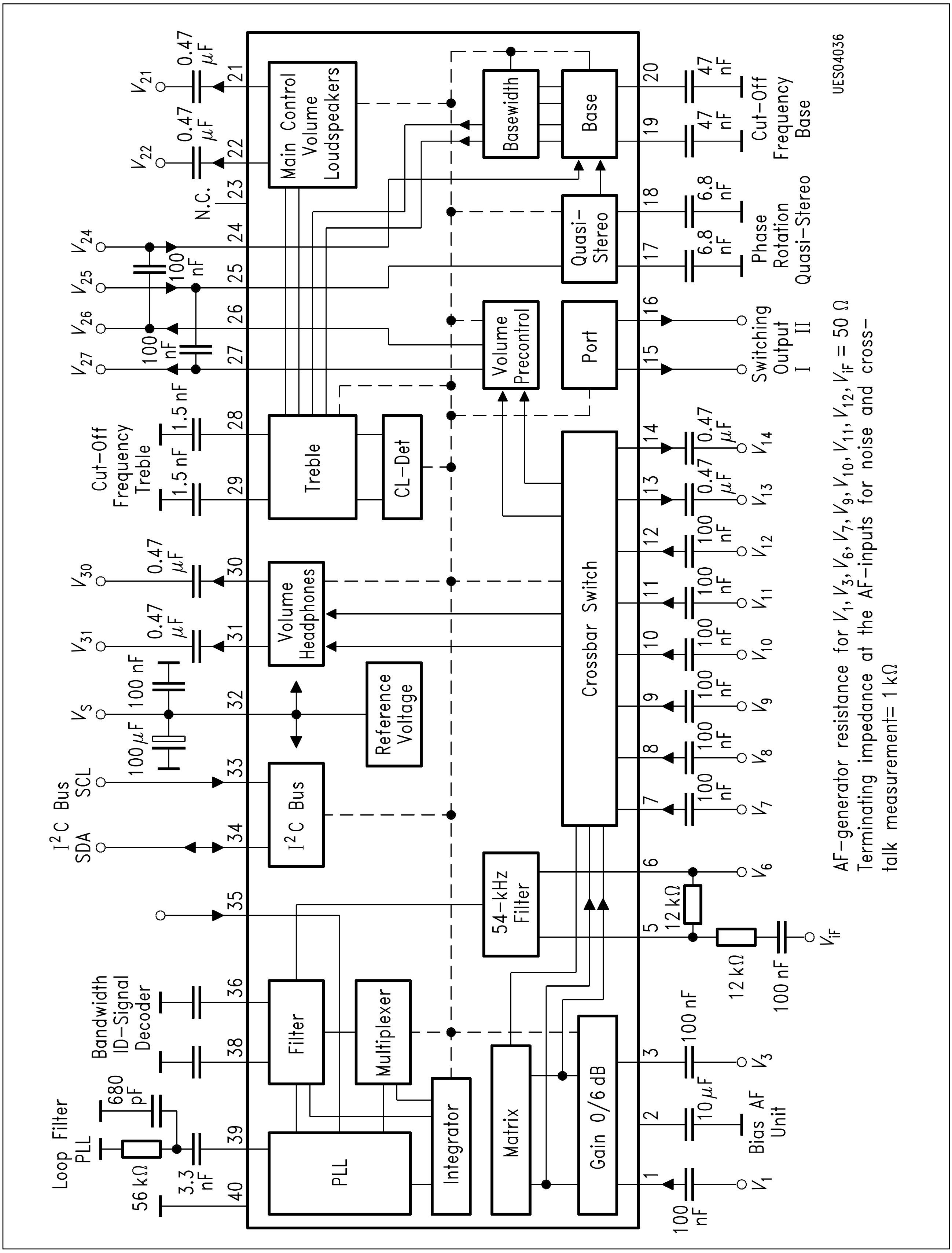
Filter output resistance	$R_{36,38}$	110			kΩ		
f_{REF} input resistance	R_{35}	800			Ω		
Input impedance crystal oscillator	Z_{35}	– 600	– 500	– 400	Ω		
Crystal oscillator series resistance	R_{Q1}			100	Ω	$P_{tot\ QU}$ = 1µW; 4 MHz	
Crystal oscillator series resistance	R_{Q3}	300			Ω	$P_{tot\ QU}$ = 1µW; 12 MHz	
		20			dB	$P_{tot\ QU}$ = 1µW; f <15 MHz	

I²C Bus (SCL, SDA)

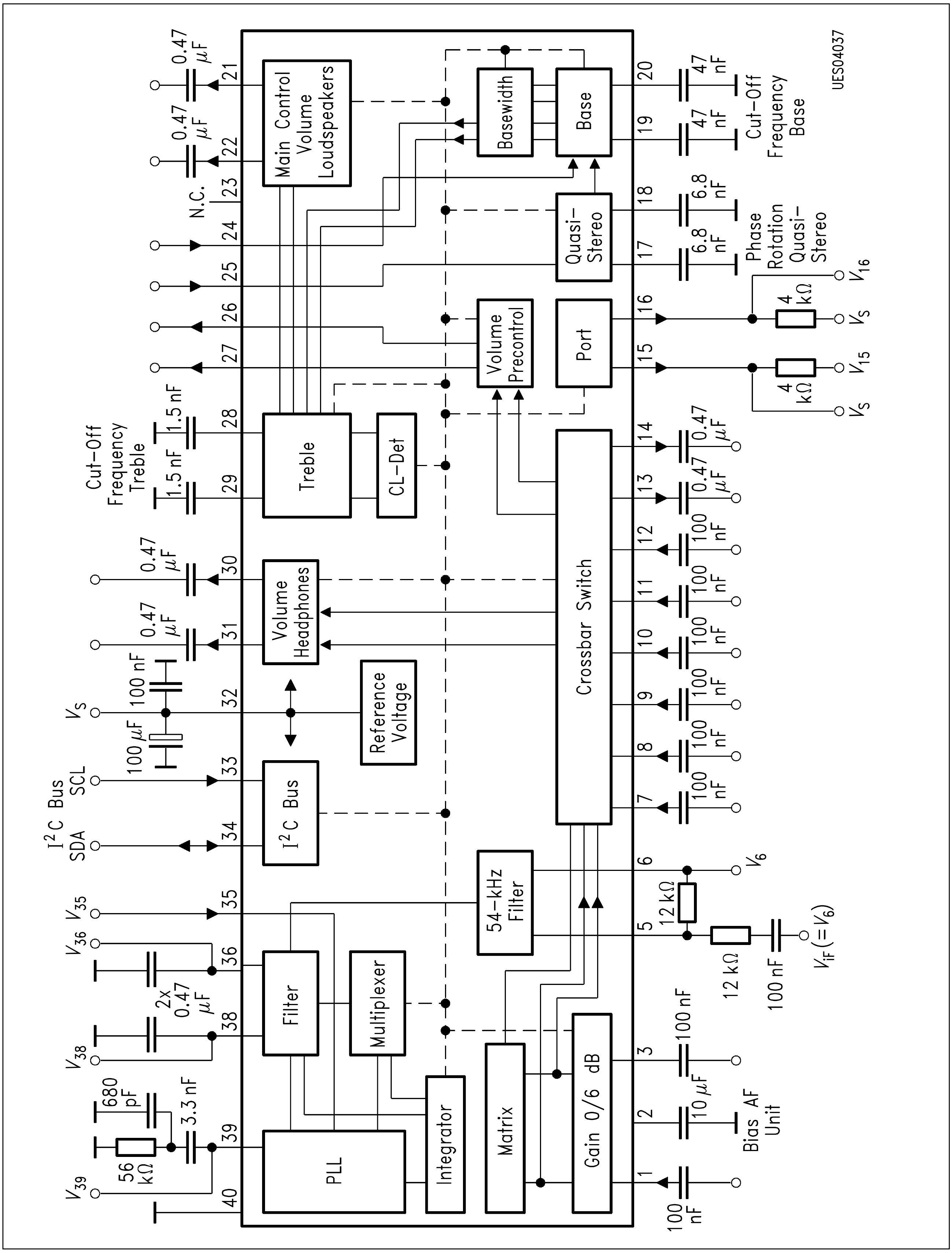
Edges SCL, SDA							
Rise time	t_R			1	µs		
Fall time	t_F			300	ns		

Characteristics (cont'd)

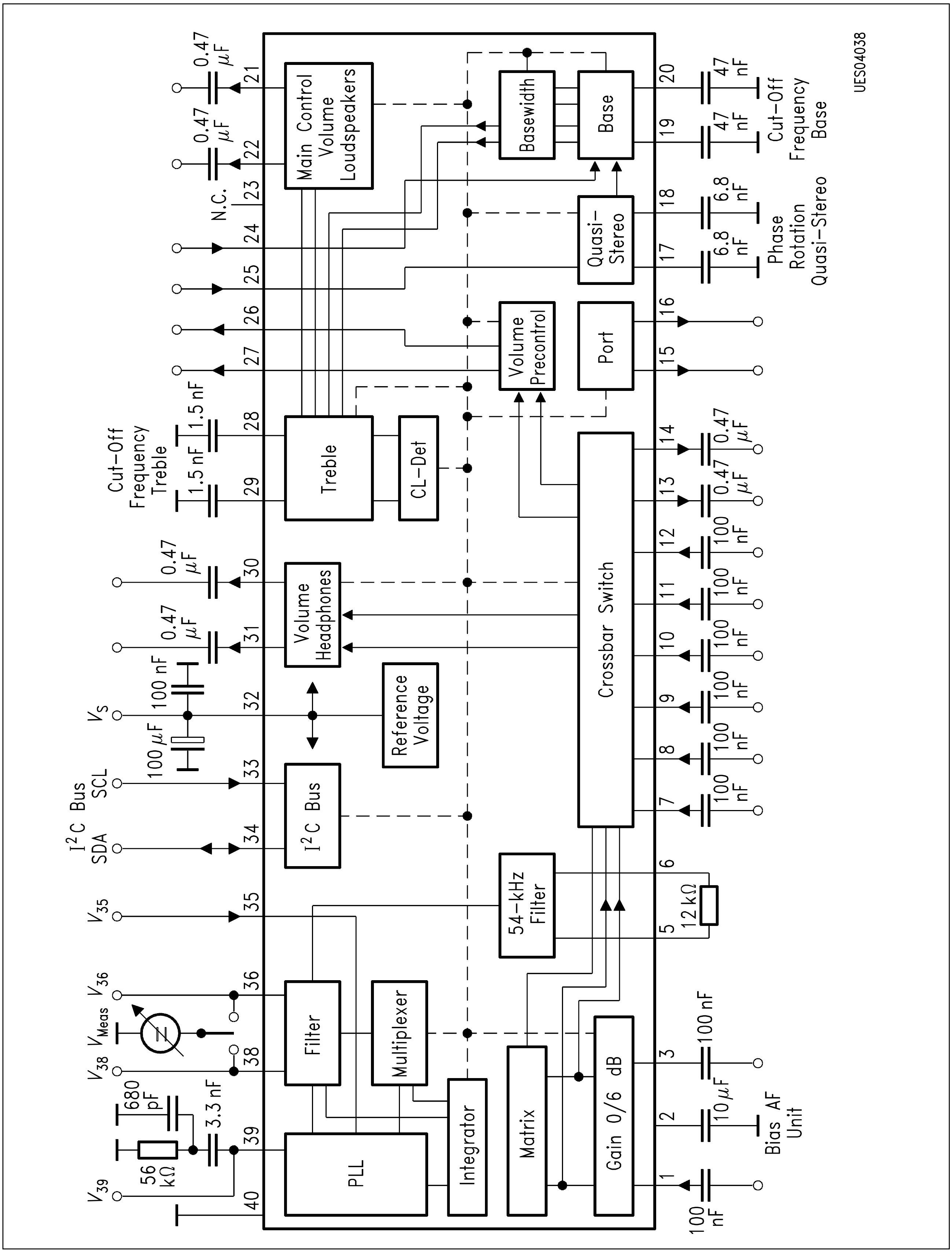
Parameter	Symbol	Limit Values			Unit	Test Condition	Test Circuit
		min.	typ.	max.			
Shift register clock SCL Frequency H-pulse width L-pulse width	 f_{SCL} t_H t_L	 0 4 4		 100	kHz µs µs		
Start Setup time Hold time	 t_{SUSTA} t_{HDSTA}	 4 4			 µs µs		
Stop Setup time Bus free	 t_{SUSTO} t_{BUF}	 4 4			 µs µs		
Data change Setup time Hold time	 t_{SUDAT} t_{HDDAT}	 1 600			 µs ns		
Input SCL, SDA Input voltage Input current	 V_{IH} V_{IL} I_{IH} I_{IL}	 2.4		 5.5 1 50 100	 V V µA µA		
Output SDA (open collector) Output voltage	V_{QH} V_{QL}	5.4		 0.4	V V	R_L = 2.5 kΩ I_{QL} = 3 mA	
Output voltage port 1	V_{15H} V_{15L}		V_S	 0.4	V V	R_L = 2.5 kΩ; 09,04 I_{QL} = 3 mA; 09,00	2 2
Output voltage port 1	V_{15H} V_{15L}		V_S	 0.4	V V	R_L = 2.5 kΩ; 02,02 I_{QL} = 3 mA; 09,00	2 2



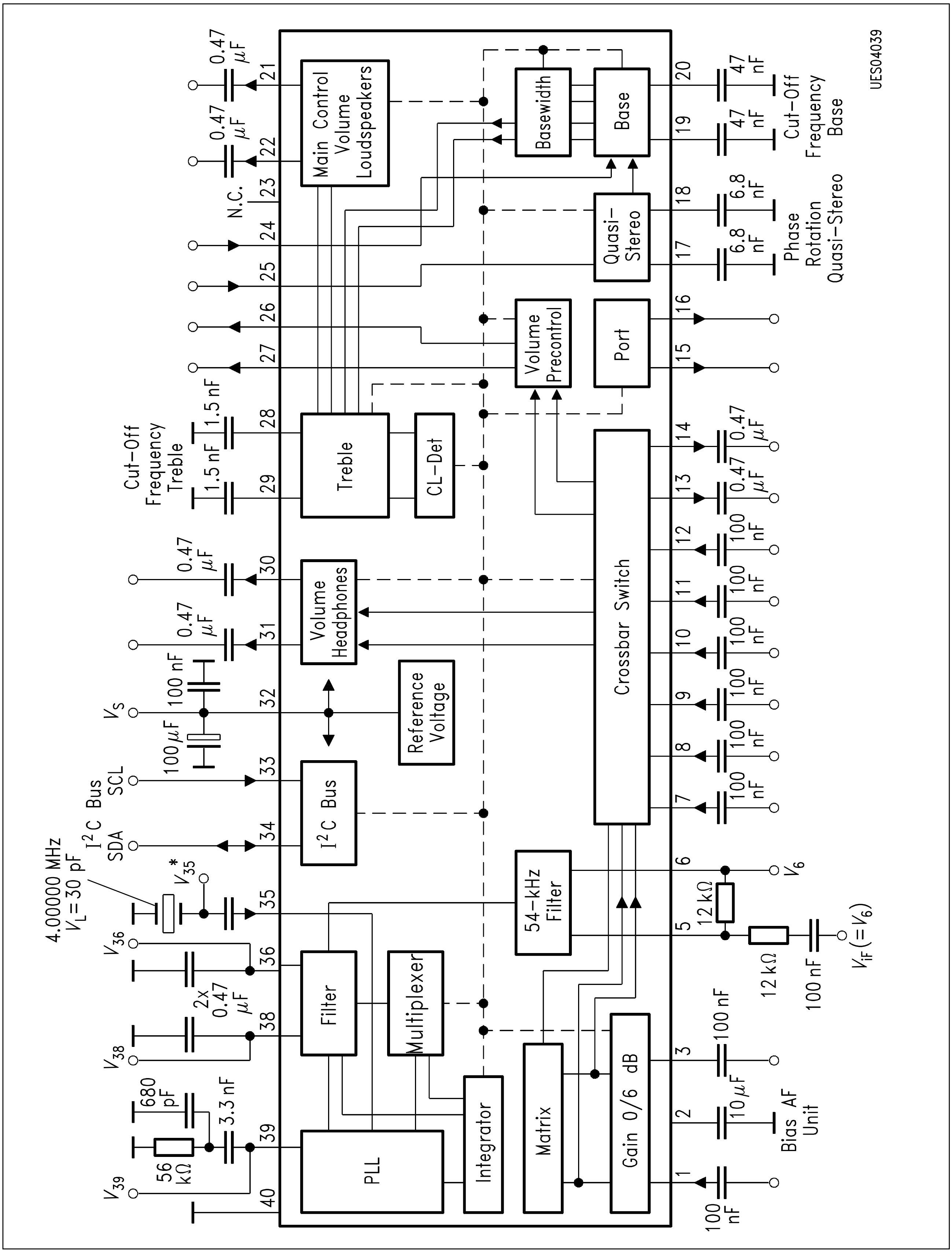
Test Circuit 1



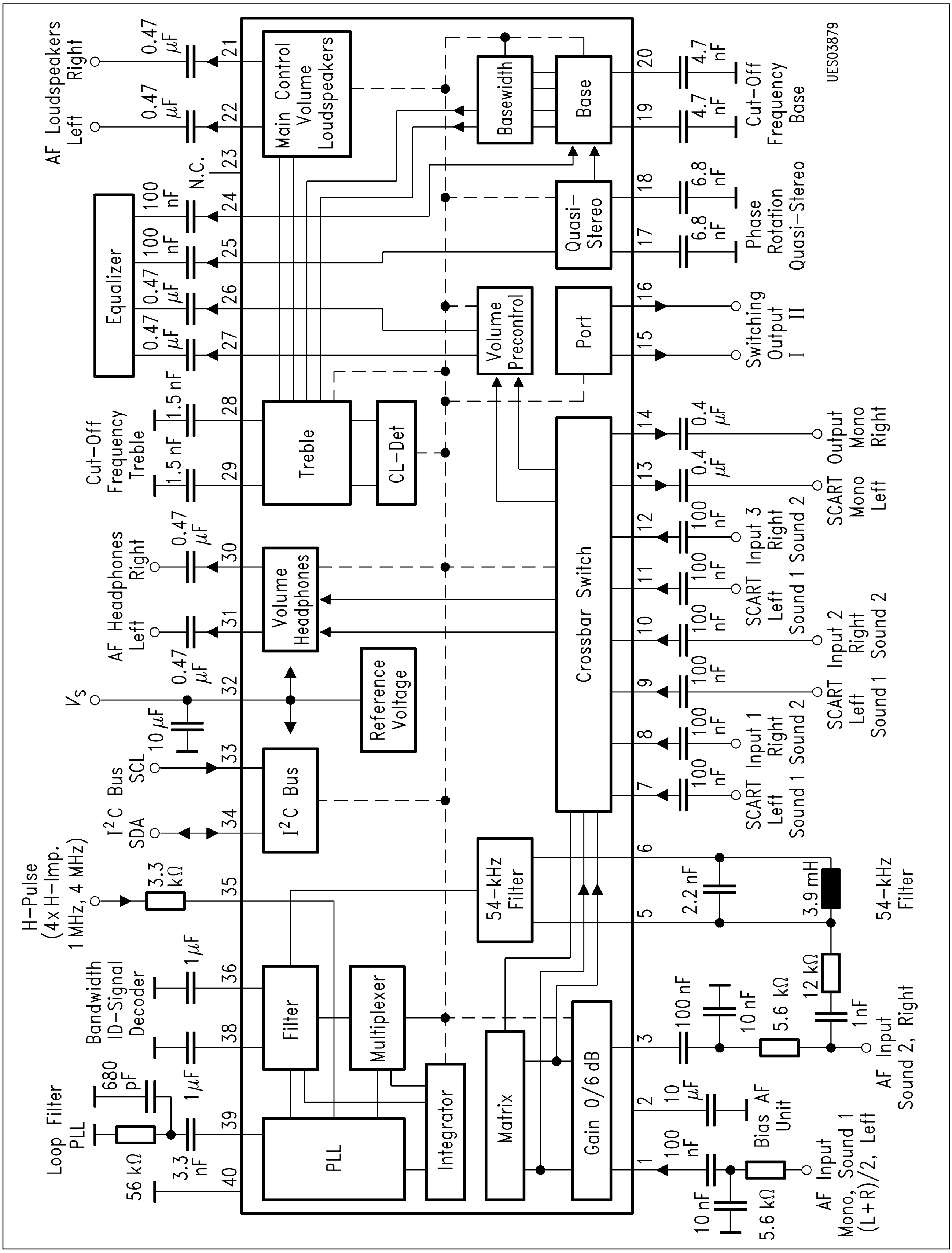
Test Circuit 2



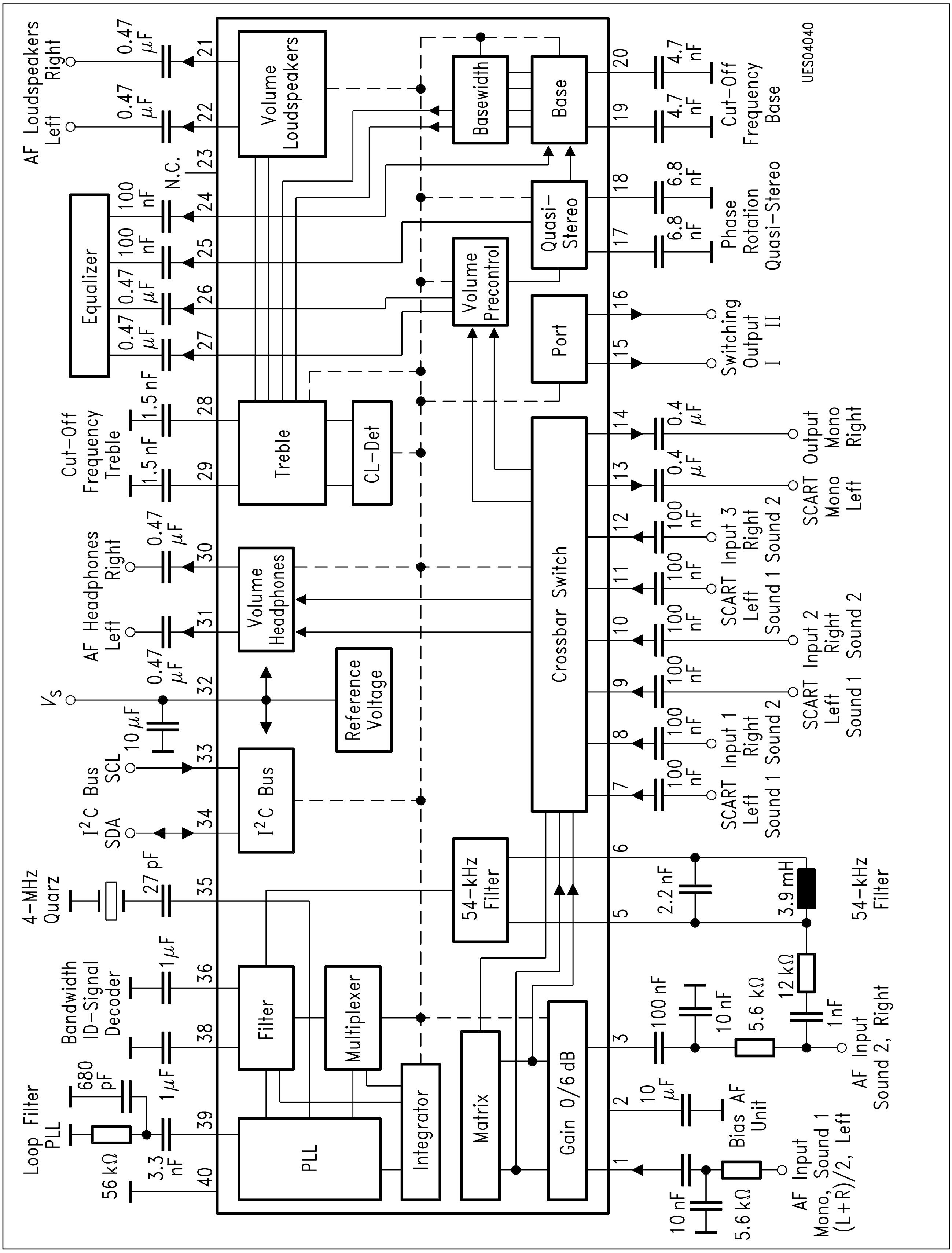
Test Circuit 3



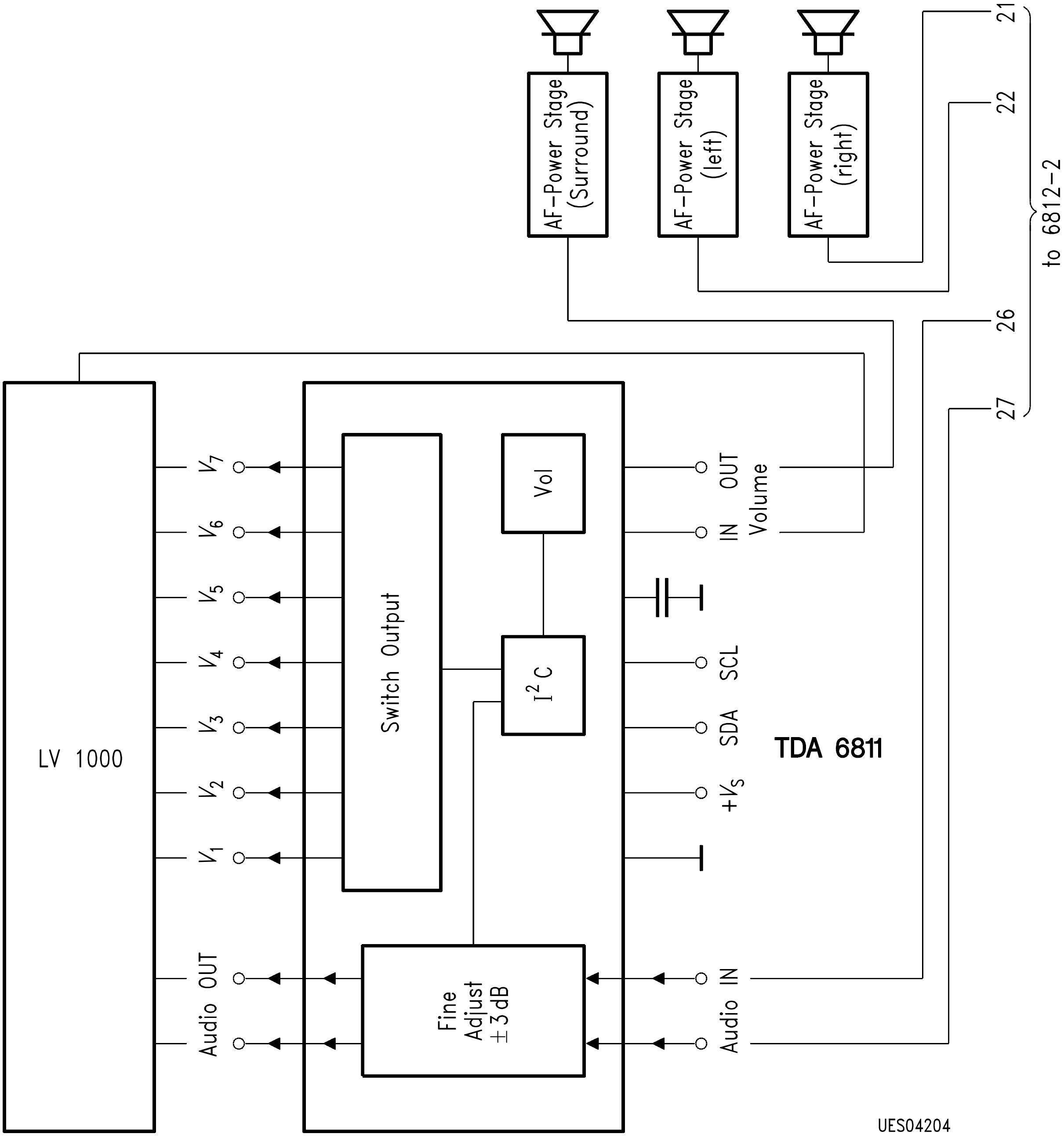
Test Circuit 4



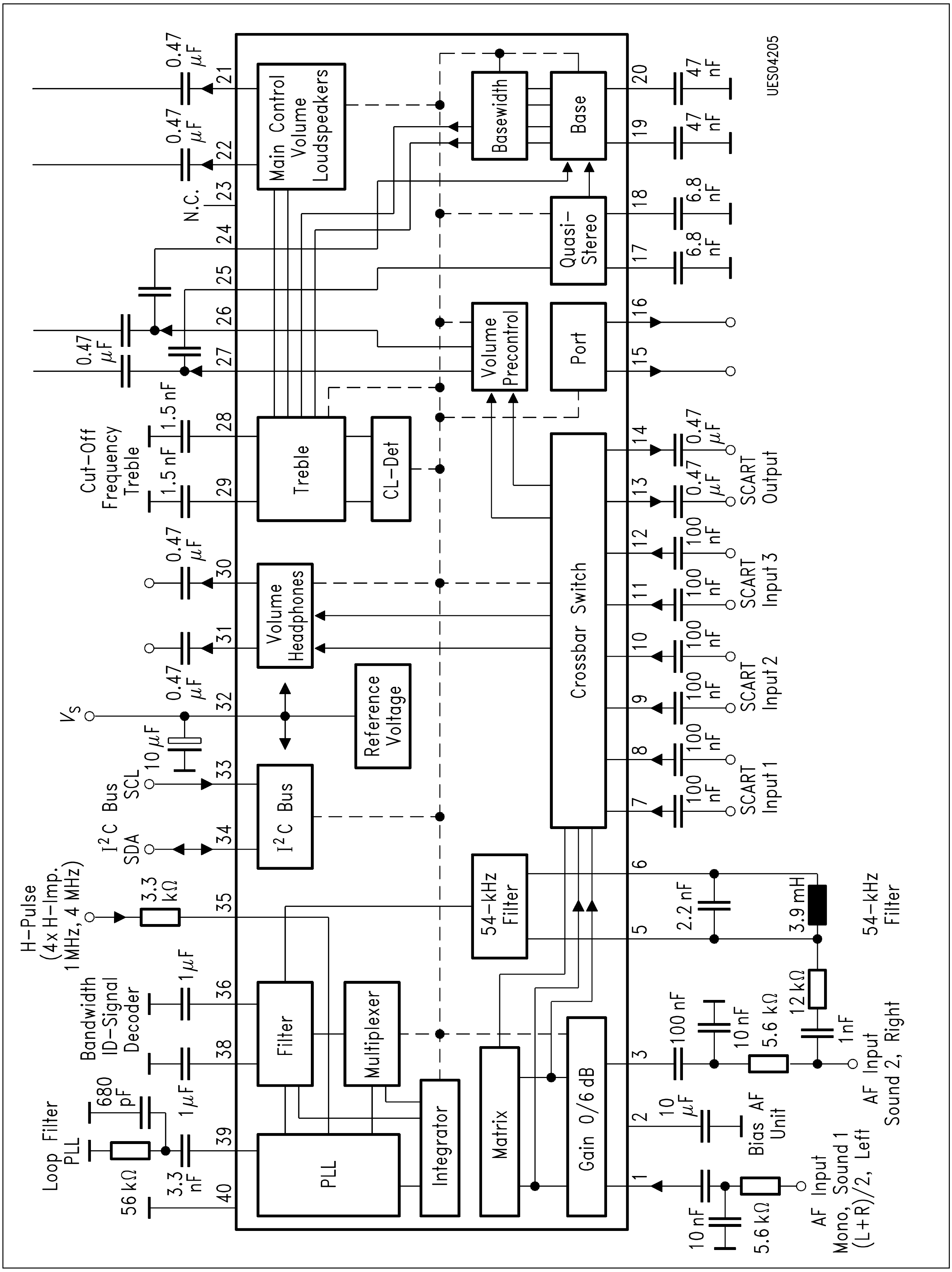
Application Circuit 1

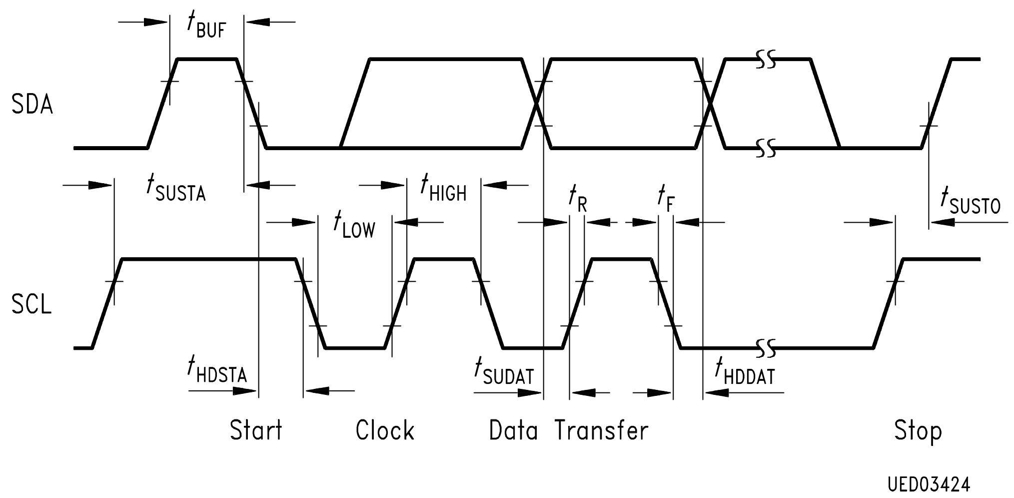


Application Circuit 2



TV-Soundconcept with Dolby-Surround-Option


Main Control Volume Loudspeakers
Basewidth
Base
Quasi-Stereo
Volume Precontrol
Port
Treble
CL-Det
Volume Headphones
Crossbar Switch
Reference Voltage
I2C Bus
54-kHz Filter
Filter
Multiplexer
PLL
Integrator
Matrix
Gain 0/6 dB
UES04205
N.C.
Cut-Off Frequency Treble
VS
I2C Bus SCL
SDA
H-Pulse (4 x H-Imp. 1 MHz, 4 MHz)
Bandwidth ID-Signal Decoder
Loop Filter PLL
SCART Output
SCART Input 3
SCART Input 2
SCART Input 1
54-kHz Filter
AF Input Sound 2, Right
Bias AF Unit
AF Input Mono, Sound 1 (L+R)/2, Left
0.47 μF
47 nF
6.8 nF
1.5 nF
100 nF
10 μF
3.3 kΩ
1 μF
680 pF
56 kΩ
3.3 nF
2.2 nF
3.9 mH
12 kΩ
10 nF
5.6 kΩ
1 nF



I²C Bus Timing Diagram

t_{SUSTA}	Setup time (start)
t_{HDSTA}	Hold time (start)
t_H	H-pulse width (clock)
t_L	L-pulse width (clock)
t_{SUDAT}	Setup time (data change)
t_{HDDAT}	Hold time (data change)
t_{SUSTO}	Setup time (stop)
t_{BUF}	Bus free time
t_F	Fall time
t_R	Rise time

All times referred to V_{IH} and V_{IL} values.