

Foxconn Precision Co. Inc.

AWA01 Schematic

Fab.A Date: 2003/11/28

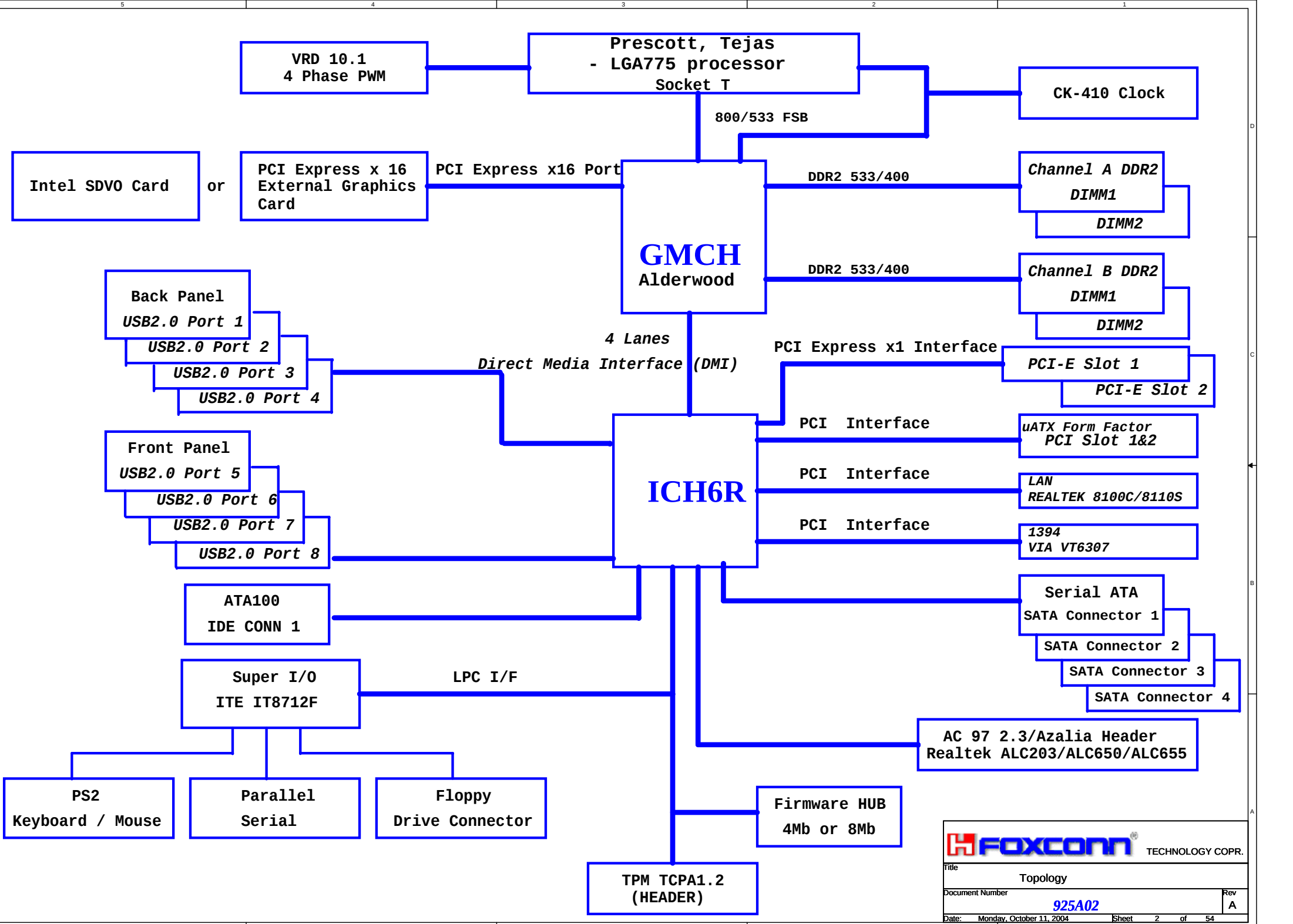
Page Index

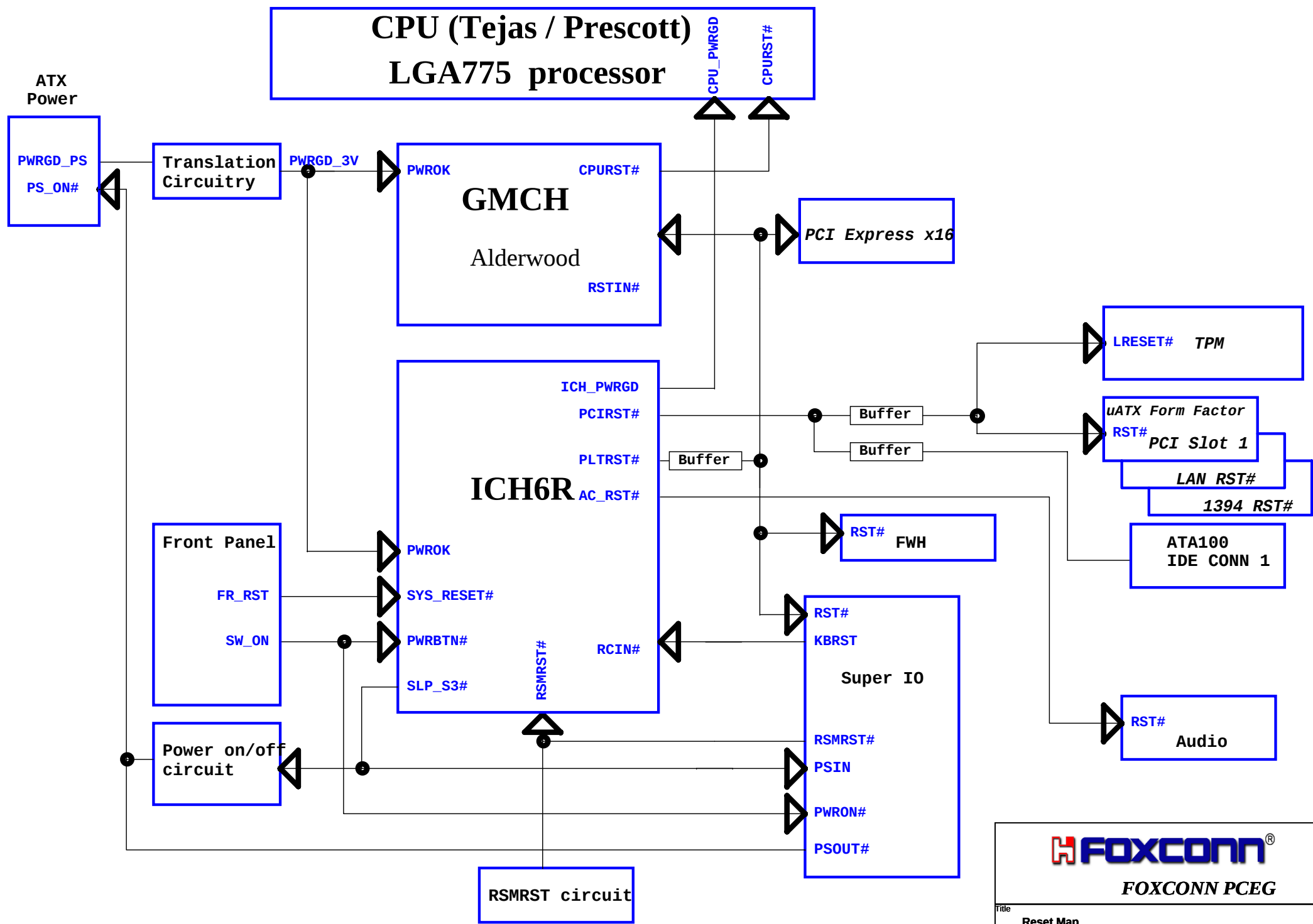
01. Index Page	25. ICH6R-2
02. Topology	26. ICH6R-3
03. Rest Map	27. LAN RTL8110S
04. Clock Distribution	28. RT8110S/C-POWER
05. Power Delivery Map	29. LAN Connectors
06. Power Sequence	30. AC' 97 2.3/Azalia Codec
07. CK410 ClockGen	31. FWH
08. VRD10.1 (SC2646, 3P)	32. USB Connectors
09. VRD10.1 (SC1211)	33. Power Conn. / 3V_SB/FAN
10. DDR2 POWER	34. Front Panel / MISC Conn.
11. Power 1.5V/1.2V	35. PCI Express x1 Slot 1
12. 2.5V_MCH	36. PCI Express x1 Slot 2
13. LGA775 -1	37. PCI Slots 1
14. LGA775 -2	38. Super I/O
15. Alderwood DDR2-GMCH -1	39. HW Monitor
16. Alderwood DDR2-GMCH -2	40. Keyboard / Mouse
17. Alderwood DDR2-GMCH -3	41. Serial / Parallel
18. DDR2 Channel A Term.	42. VT6307_1394
19. DDR2 Channel A DIMM1, 2	43. 1394 CON
20. DDR2 Channel B Term.	44. TPM
21. DDR2 Channel B DIMM1, 2	45. VID Controller
22. PCI Express x16 Gfx Slot	46. GPIO / IRQ / IDSEL Map
23. VGA Connector	47. Jumper Setting Table
24. ICH6R-1	48. Modify List

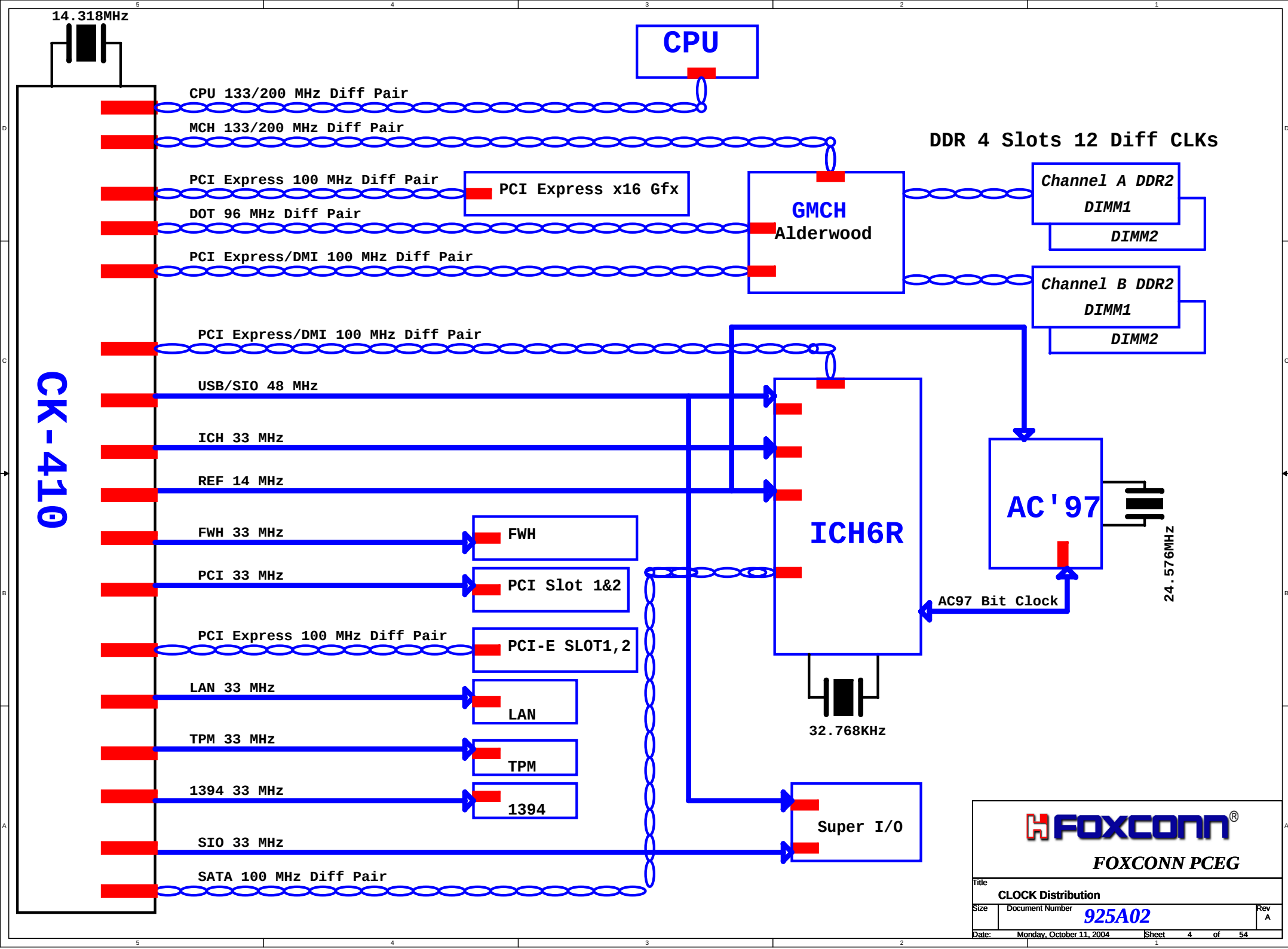


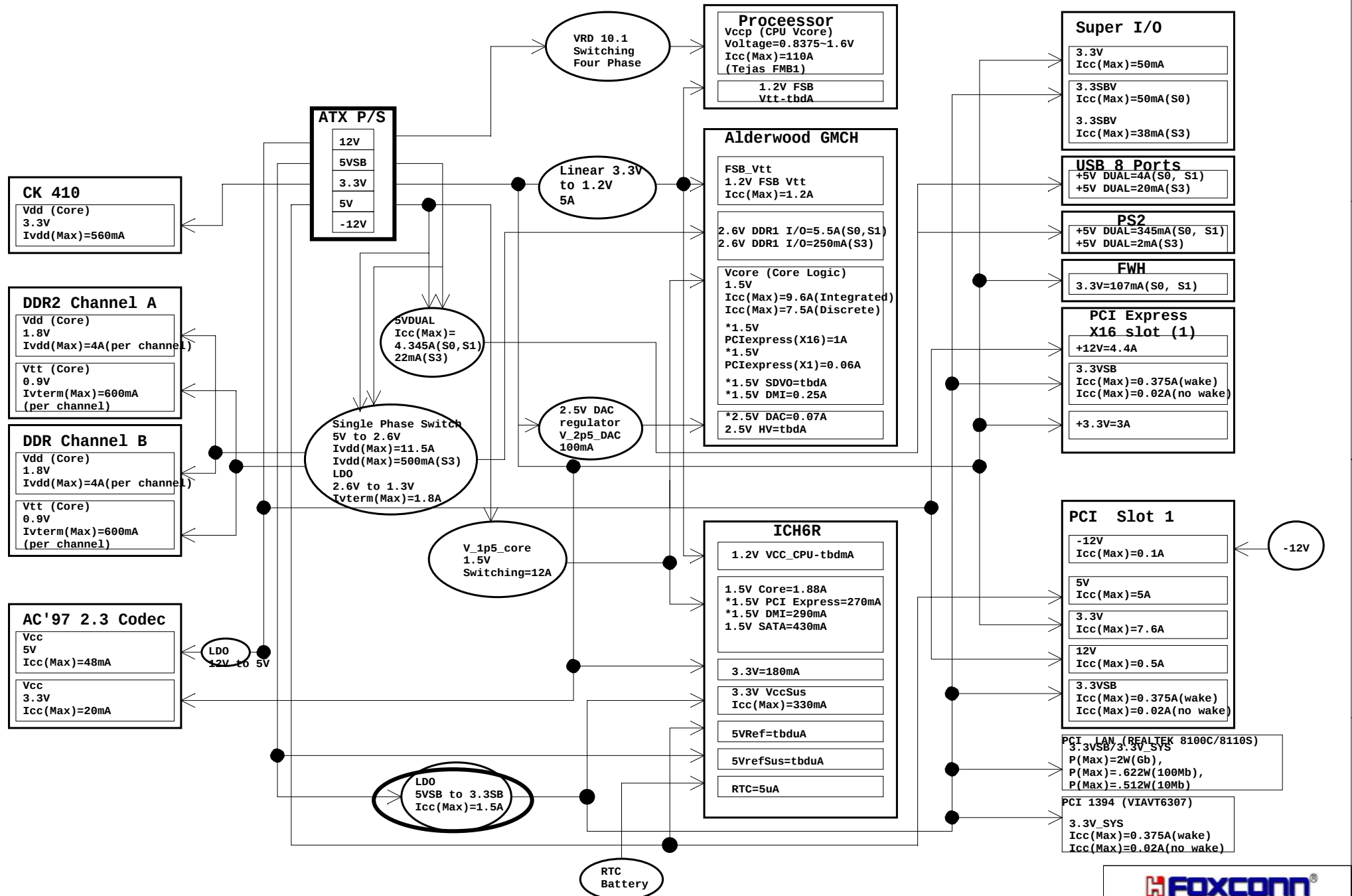
FOXCONN PCEG

Title		
Index Page		
Size	Document Number	Rev
	925A02	A
Date:	Monday, October 11, 2004	Sheet 1 of 54



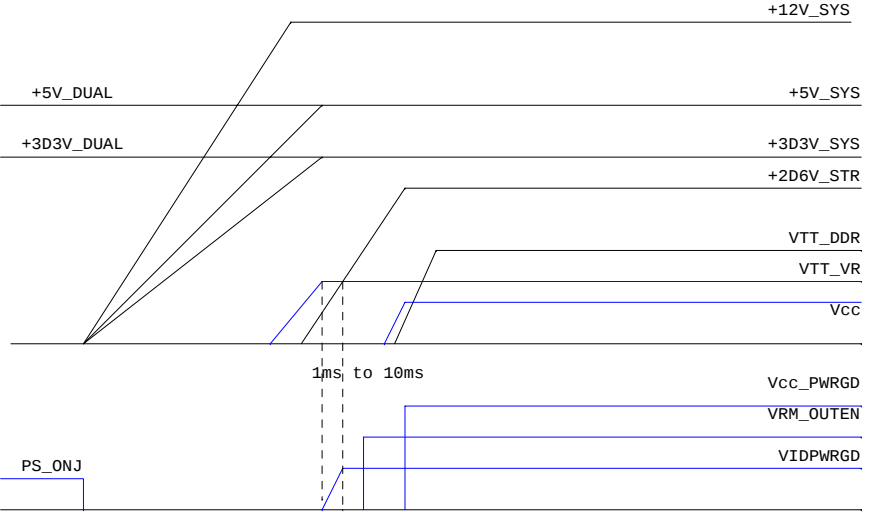




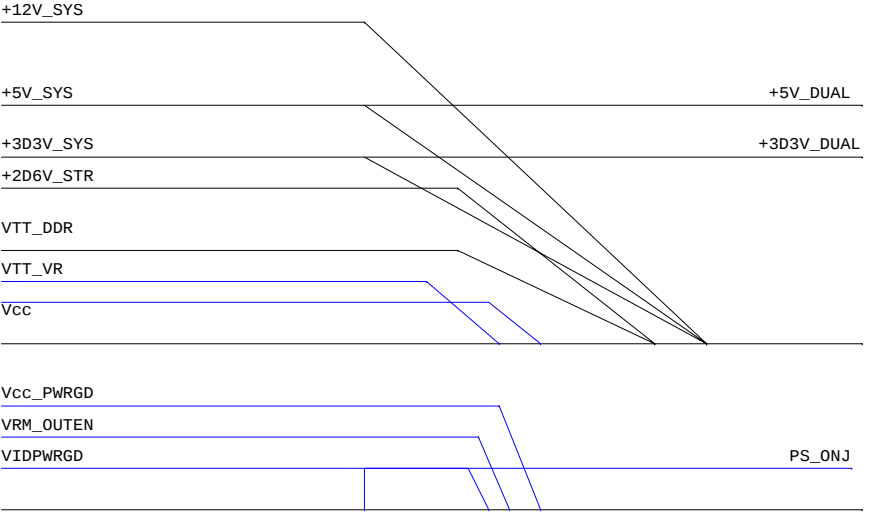


*Power derived through filter

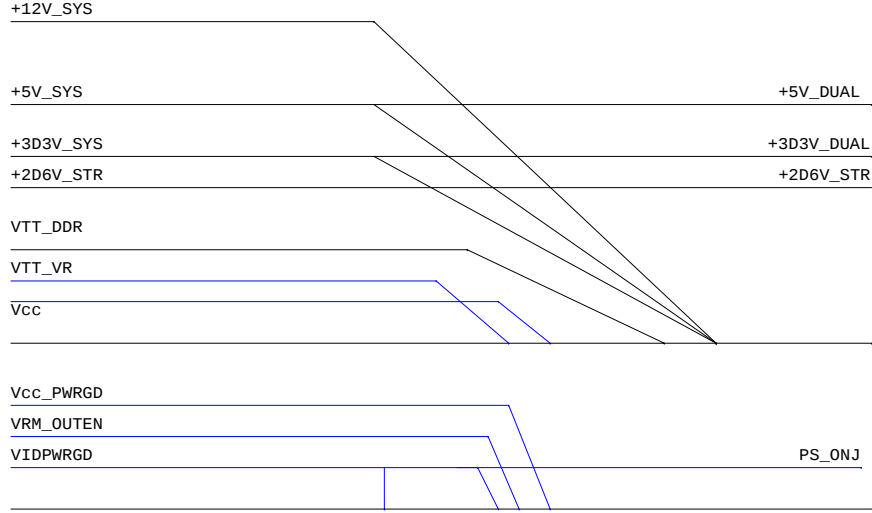
S5->S0



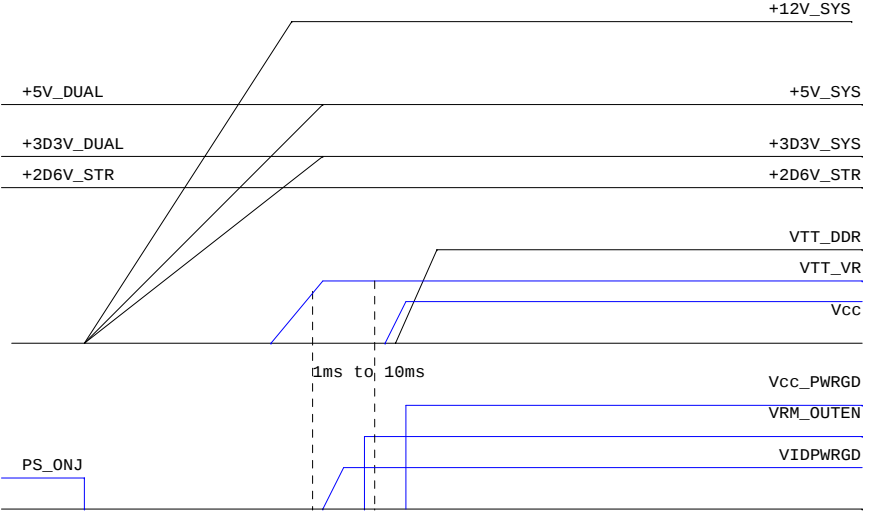
S0->S5

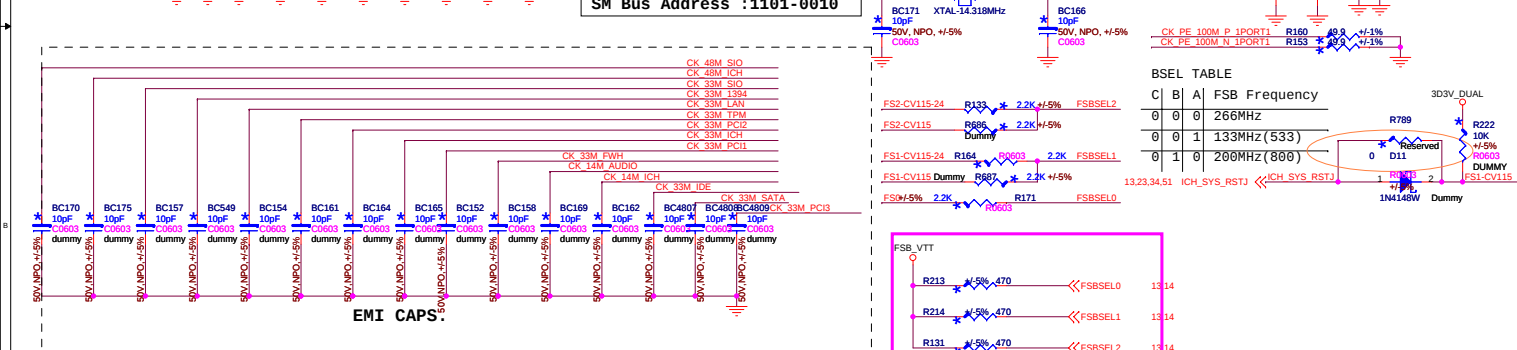


S0->S3



S3->S0





BSEL TABLE

C	B	A	FSB Frequency
0	0	0	266MHz
0	0	1	133MHz(533)
0	1	0	200MHz(800)

13.23.34.51 ICH_SYS_RSTJ << ICH_SYS_RSTJ

3D3V_DUAL

R789

Reserved

D11

0

1

2

1N4148W

Dummy

R222

10K

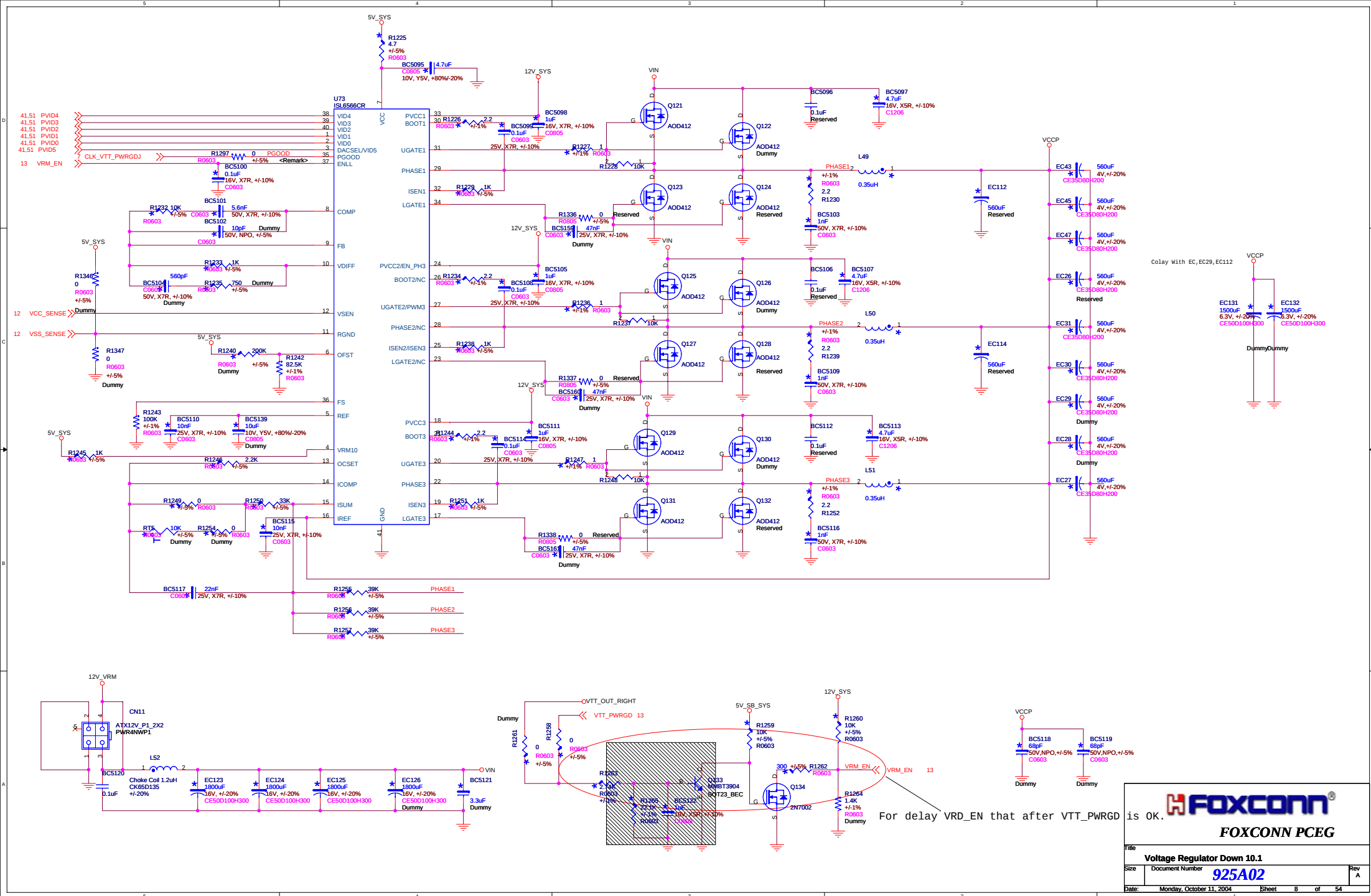
+5%

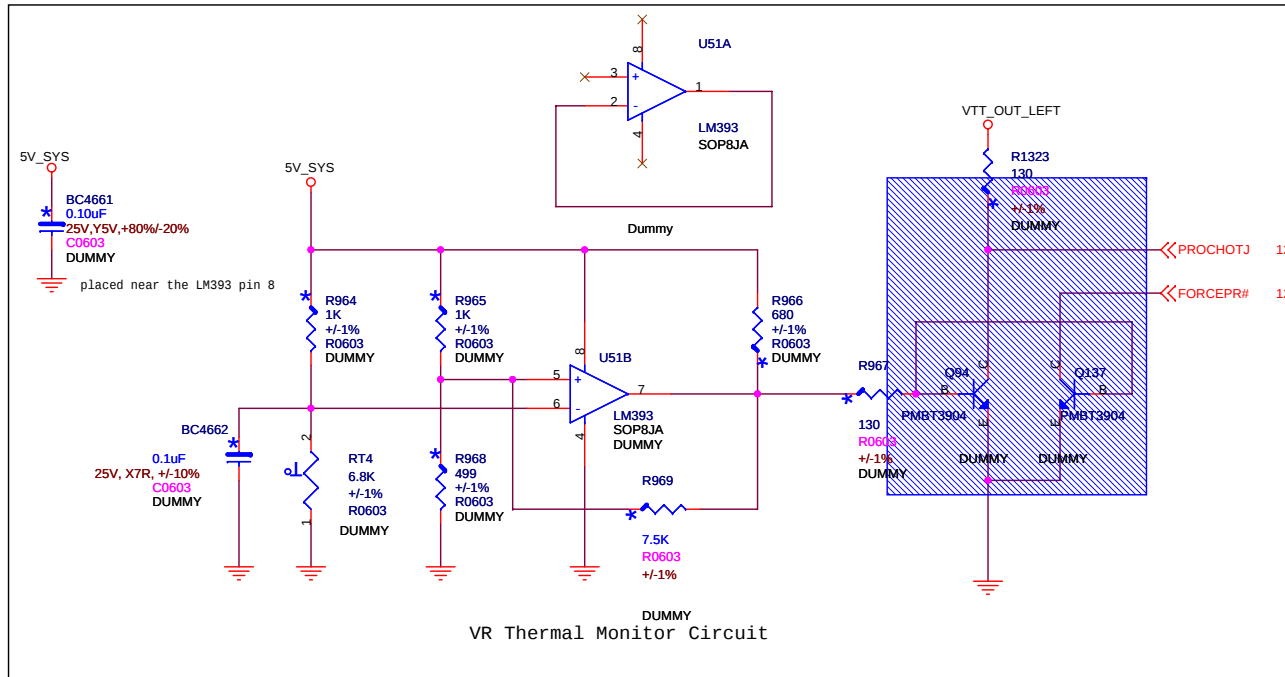
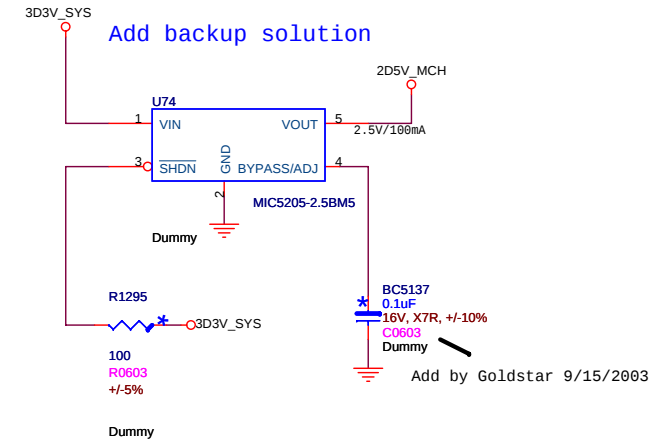
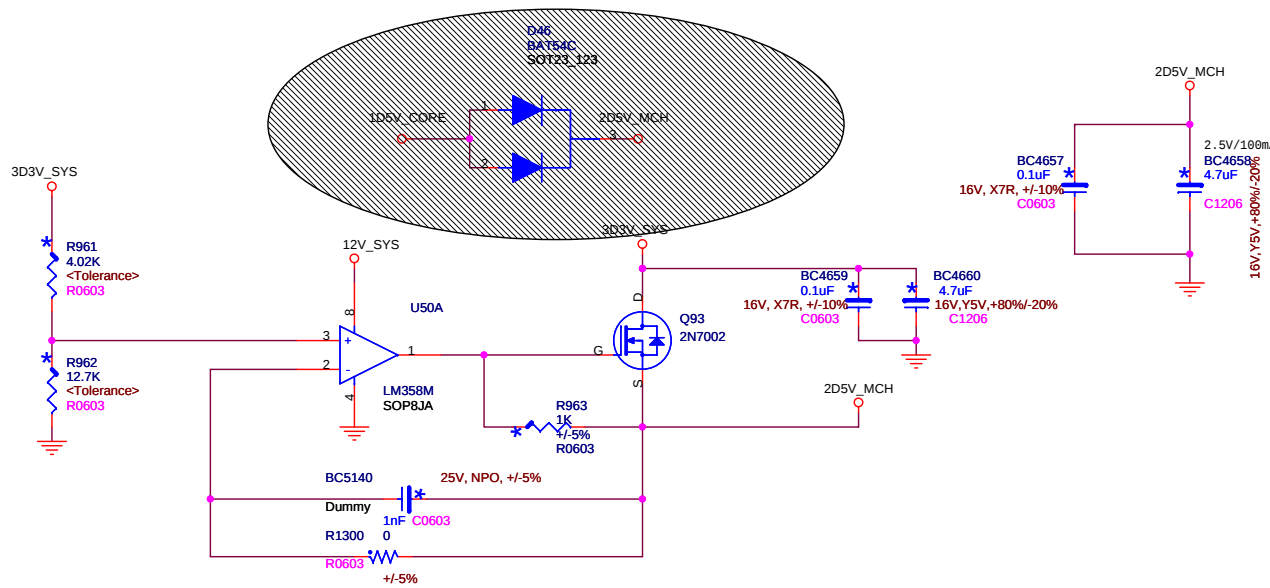
R0000

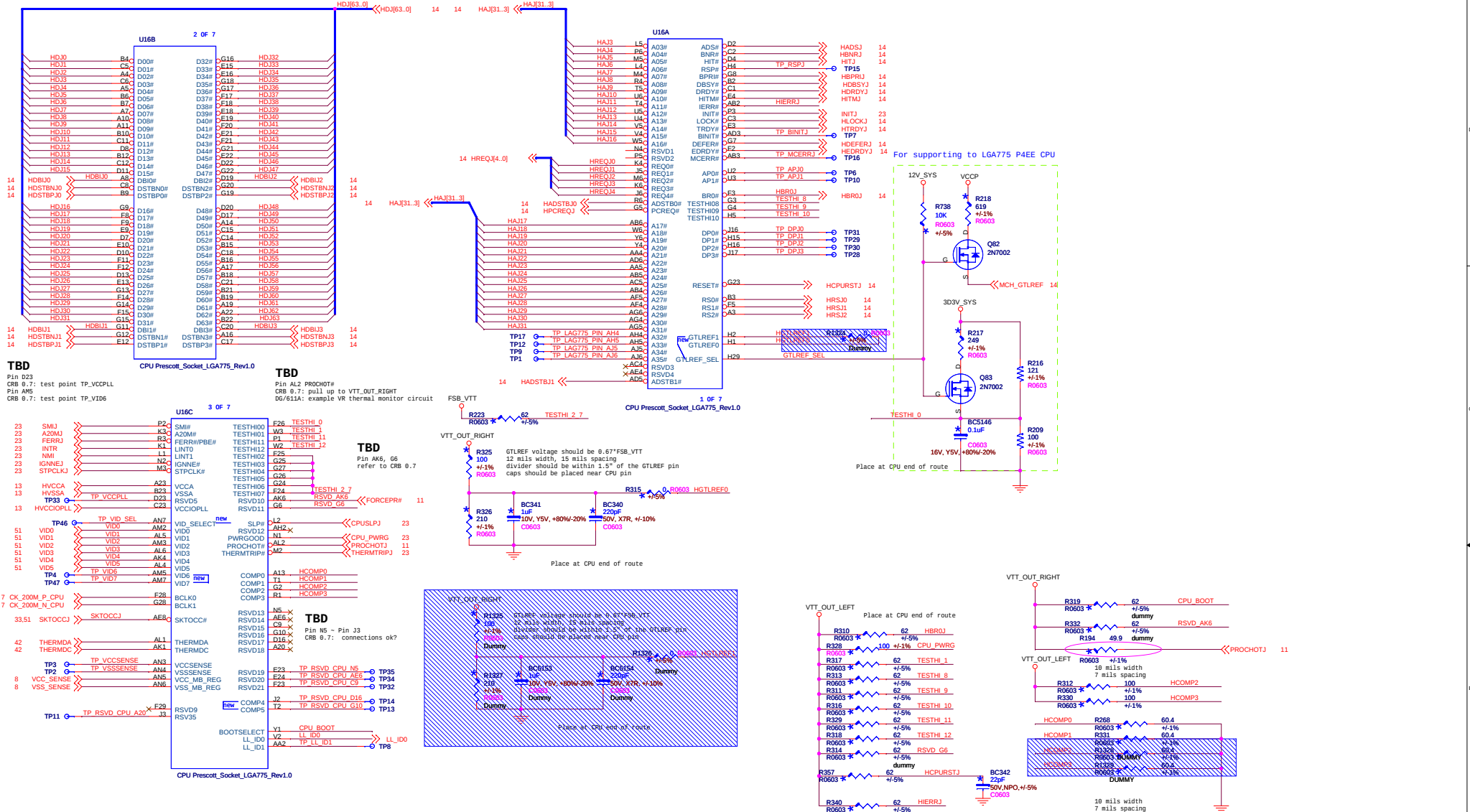
DUMMY

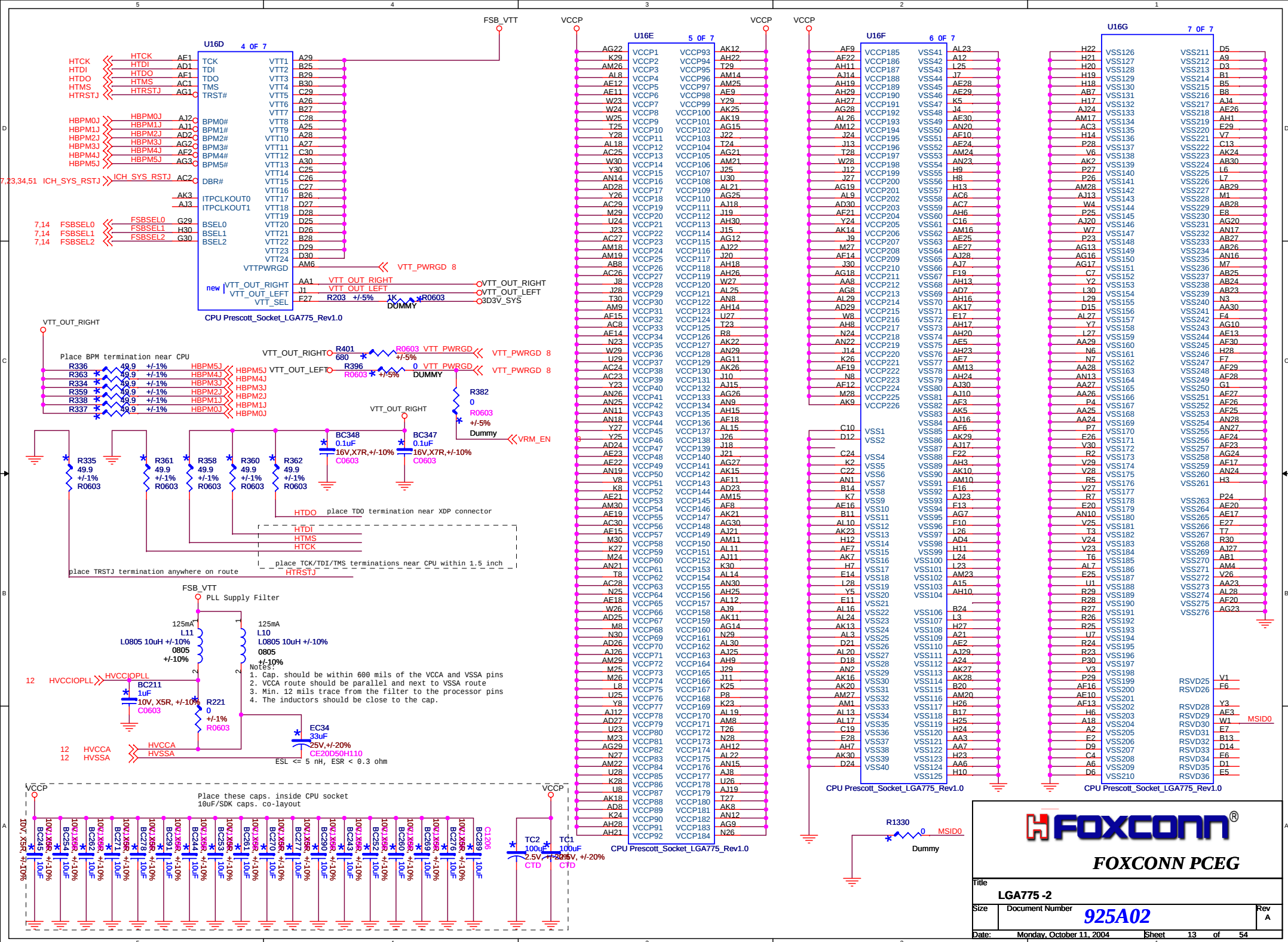
PS1-CV1.15

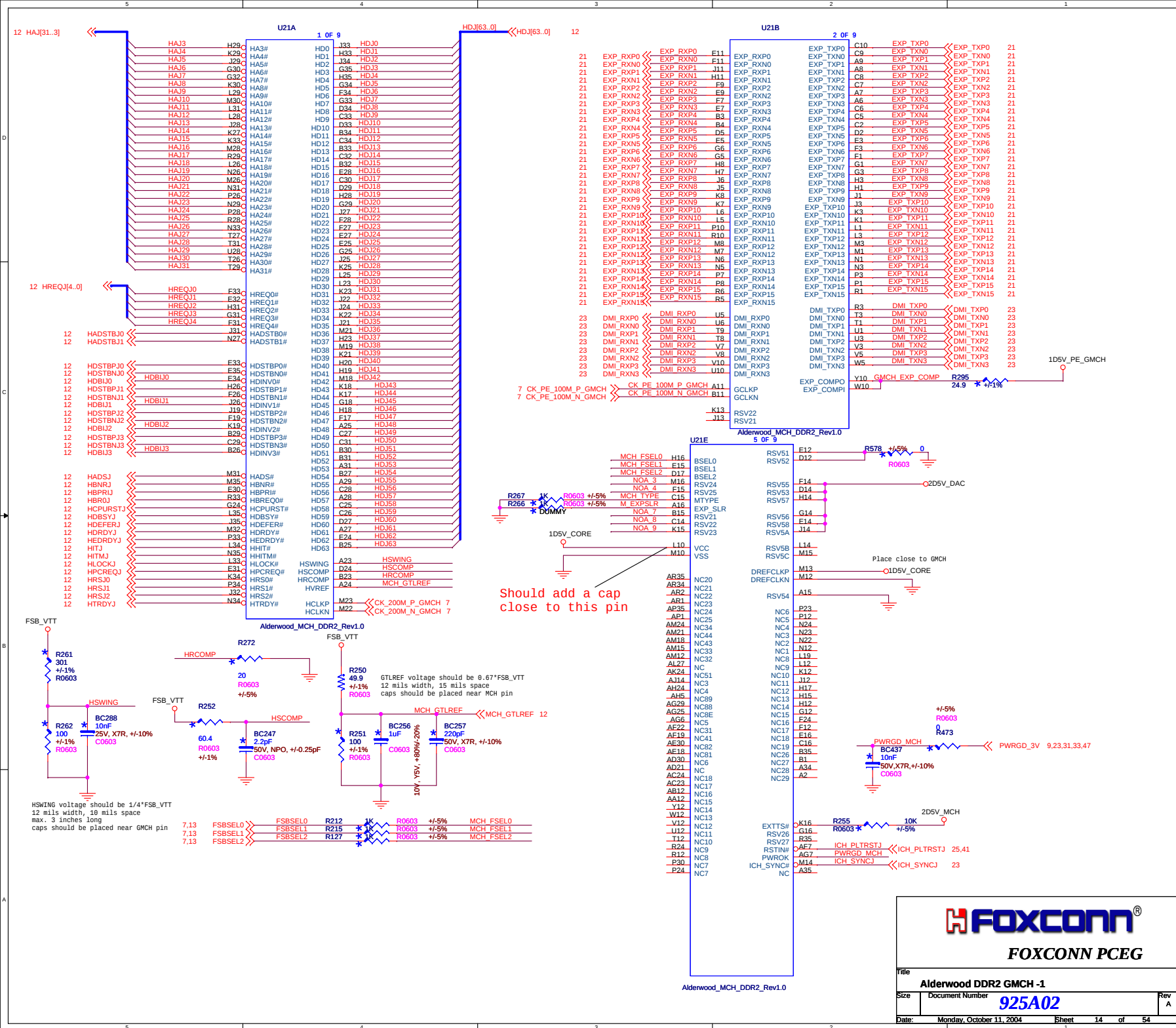


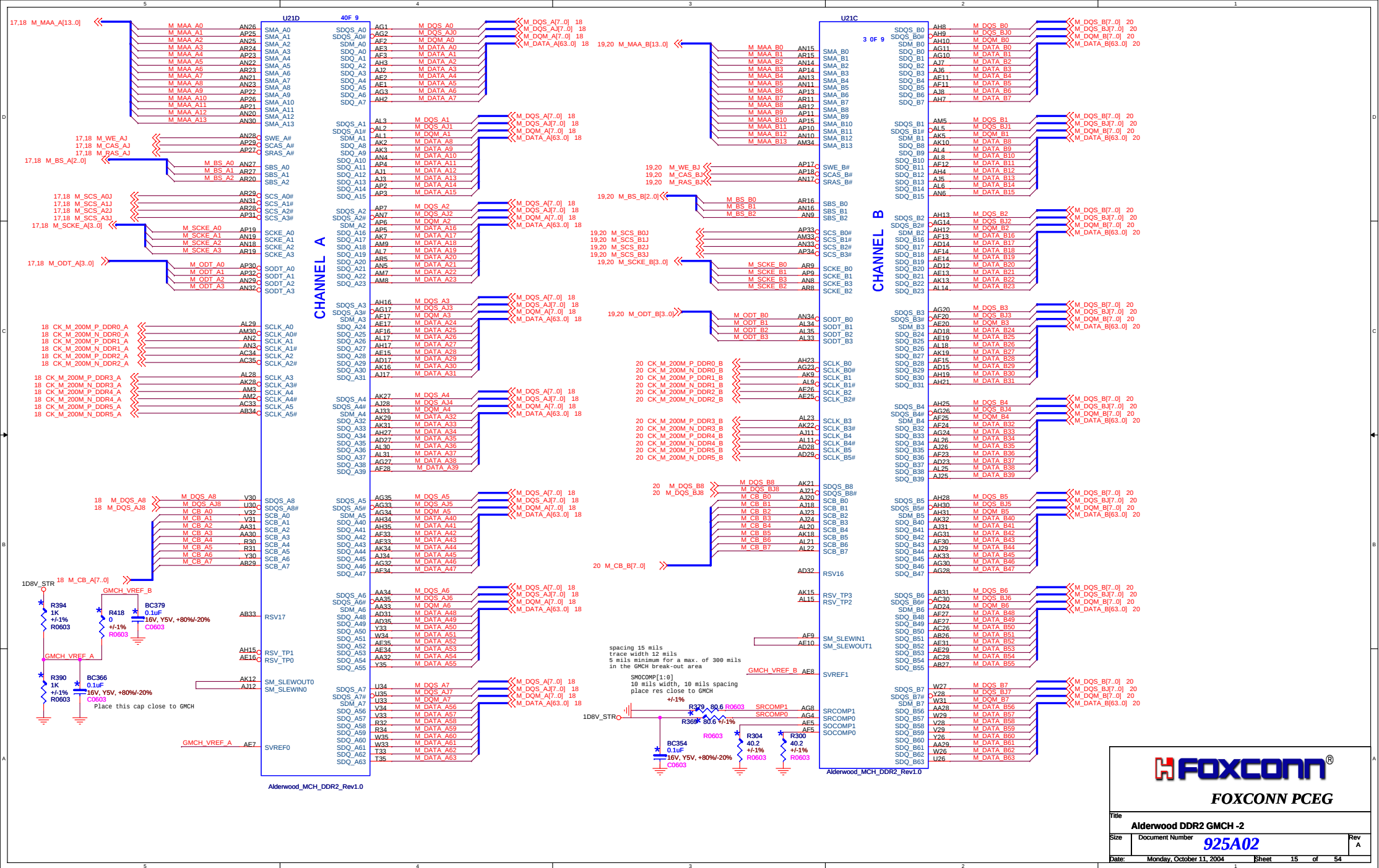


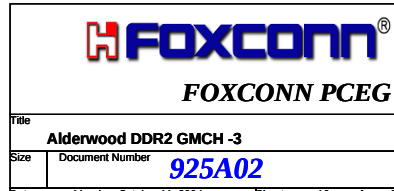


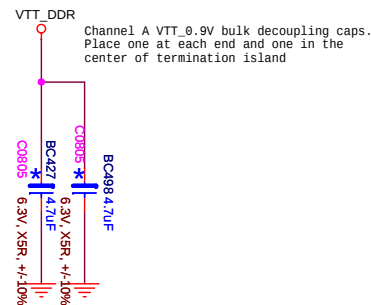
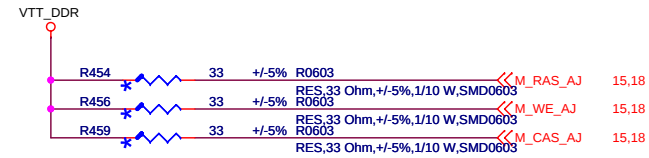
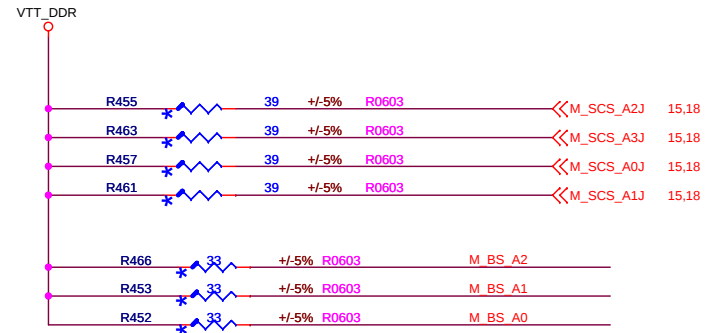
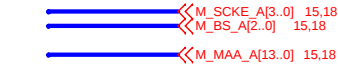


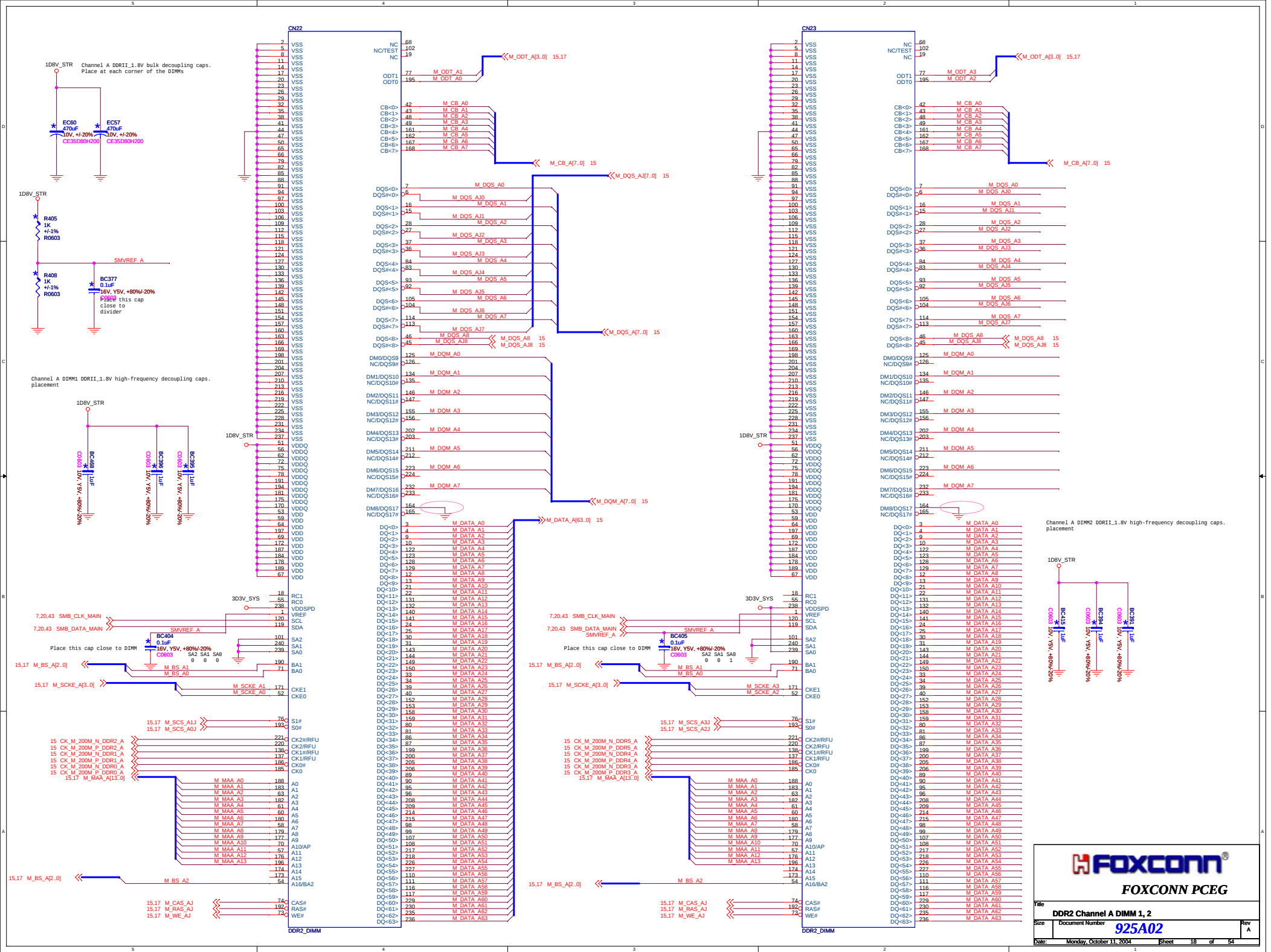


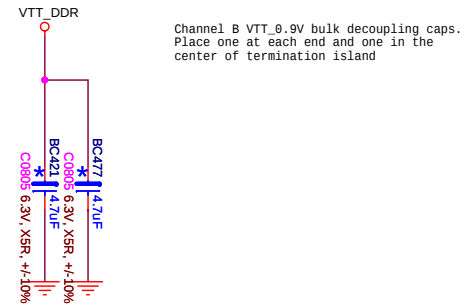
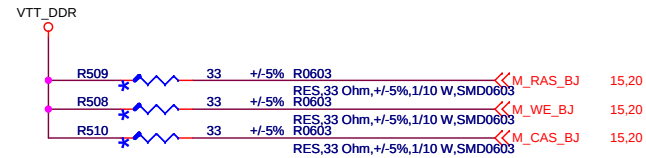
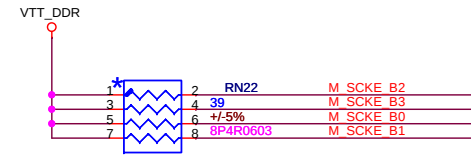
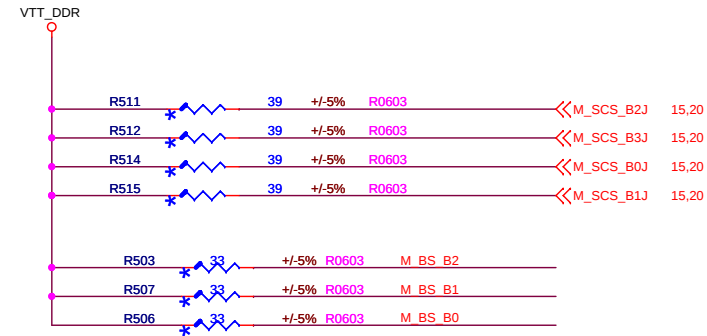
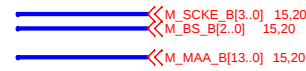
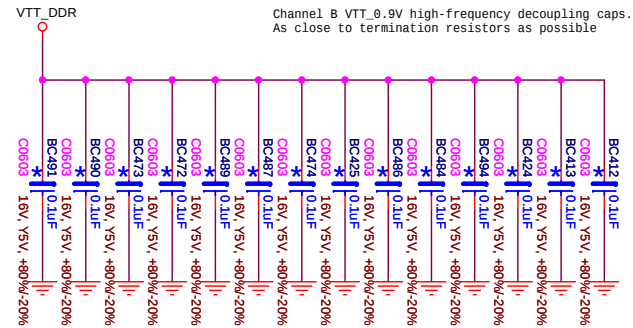
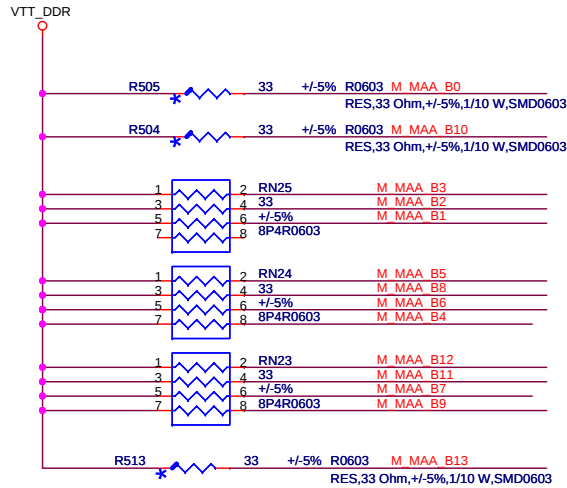
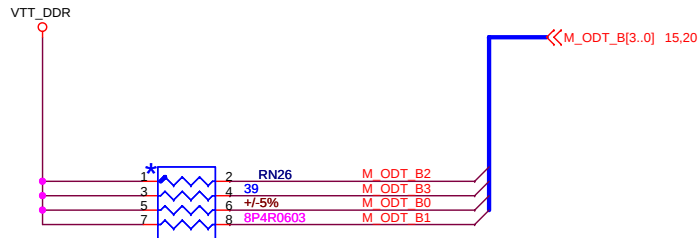






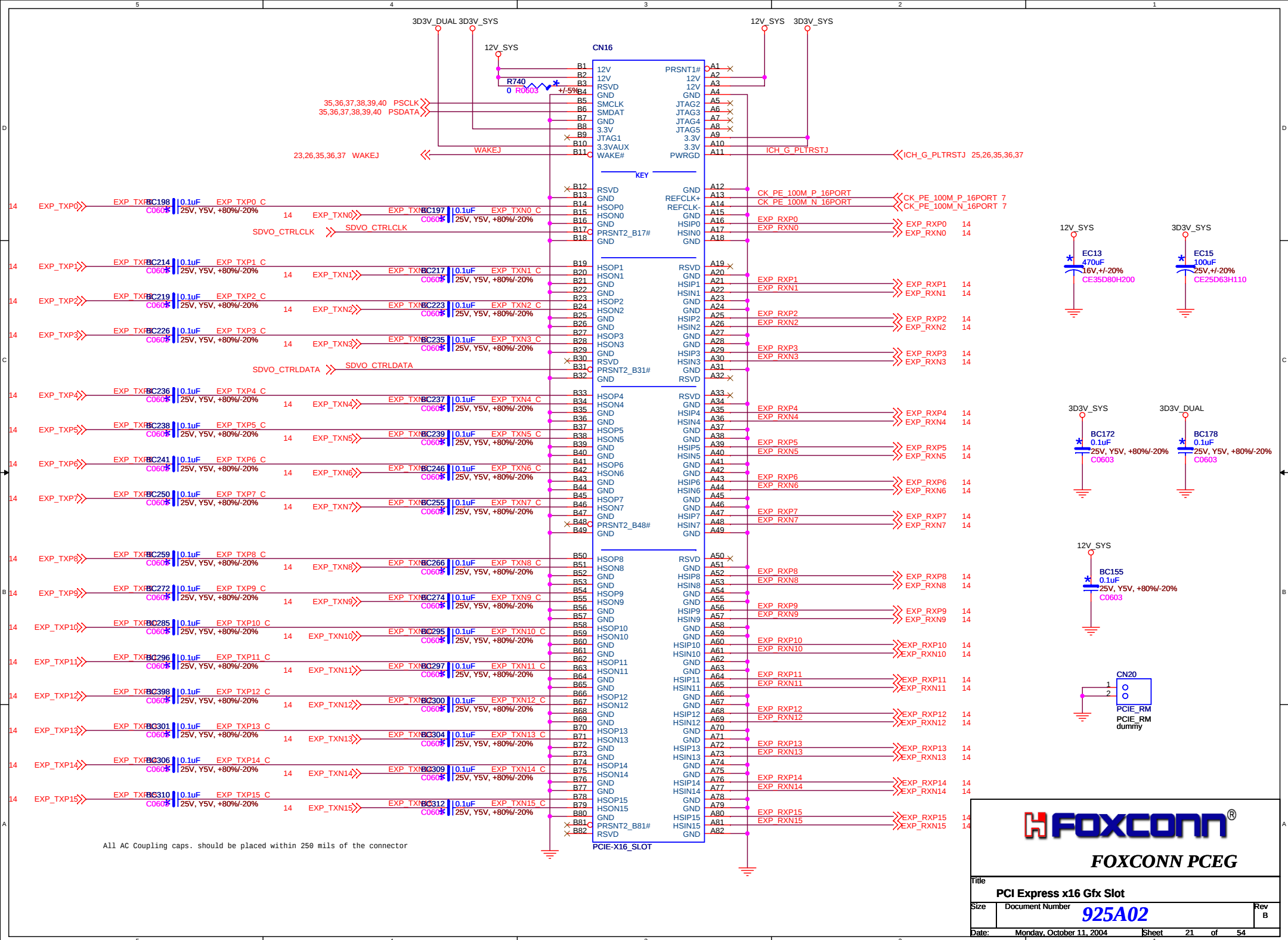






FOXCONN
FOXCONN PCEG



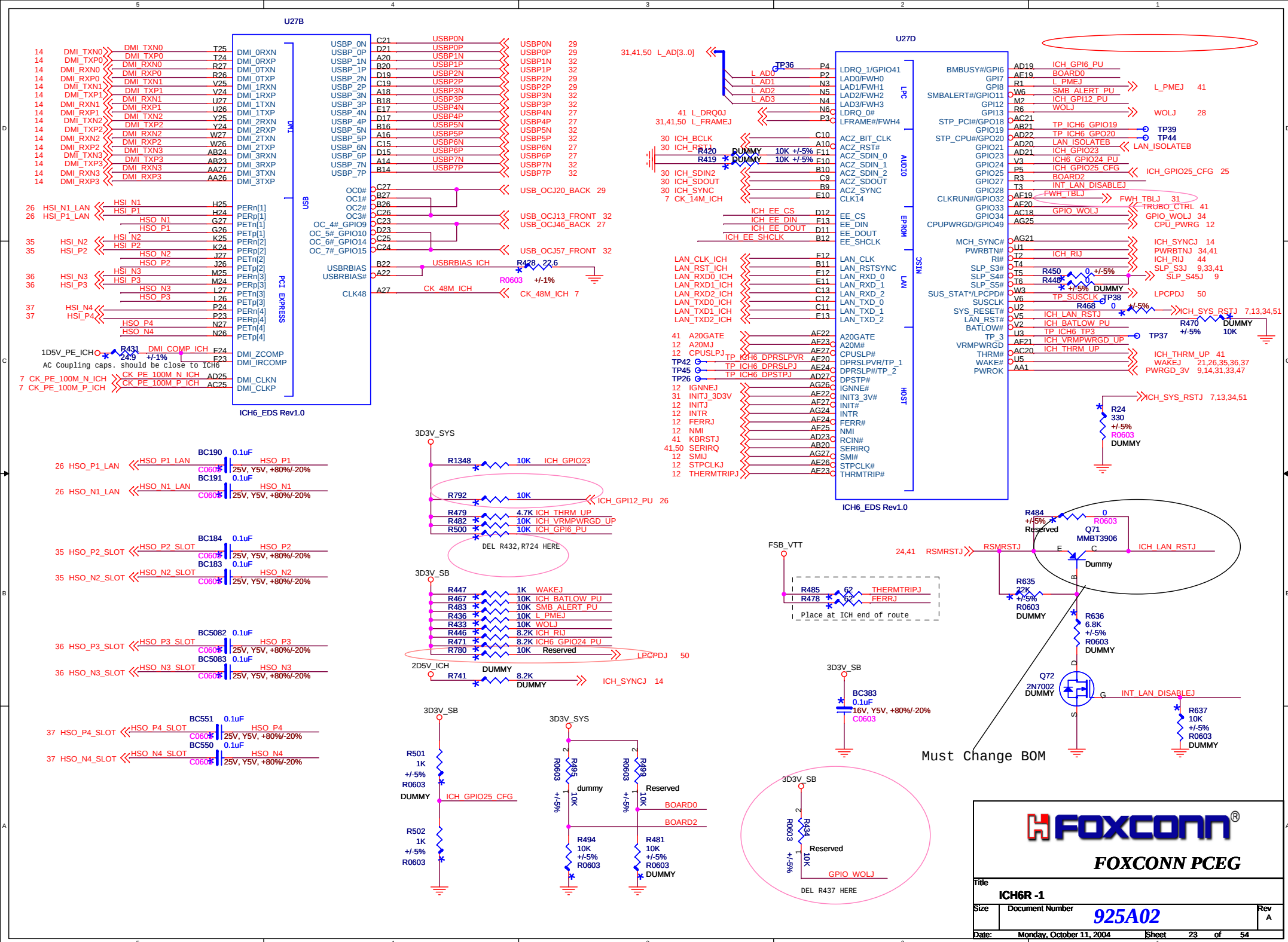


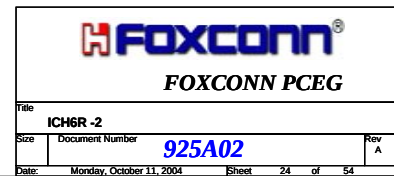
Blank

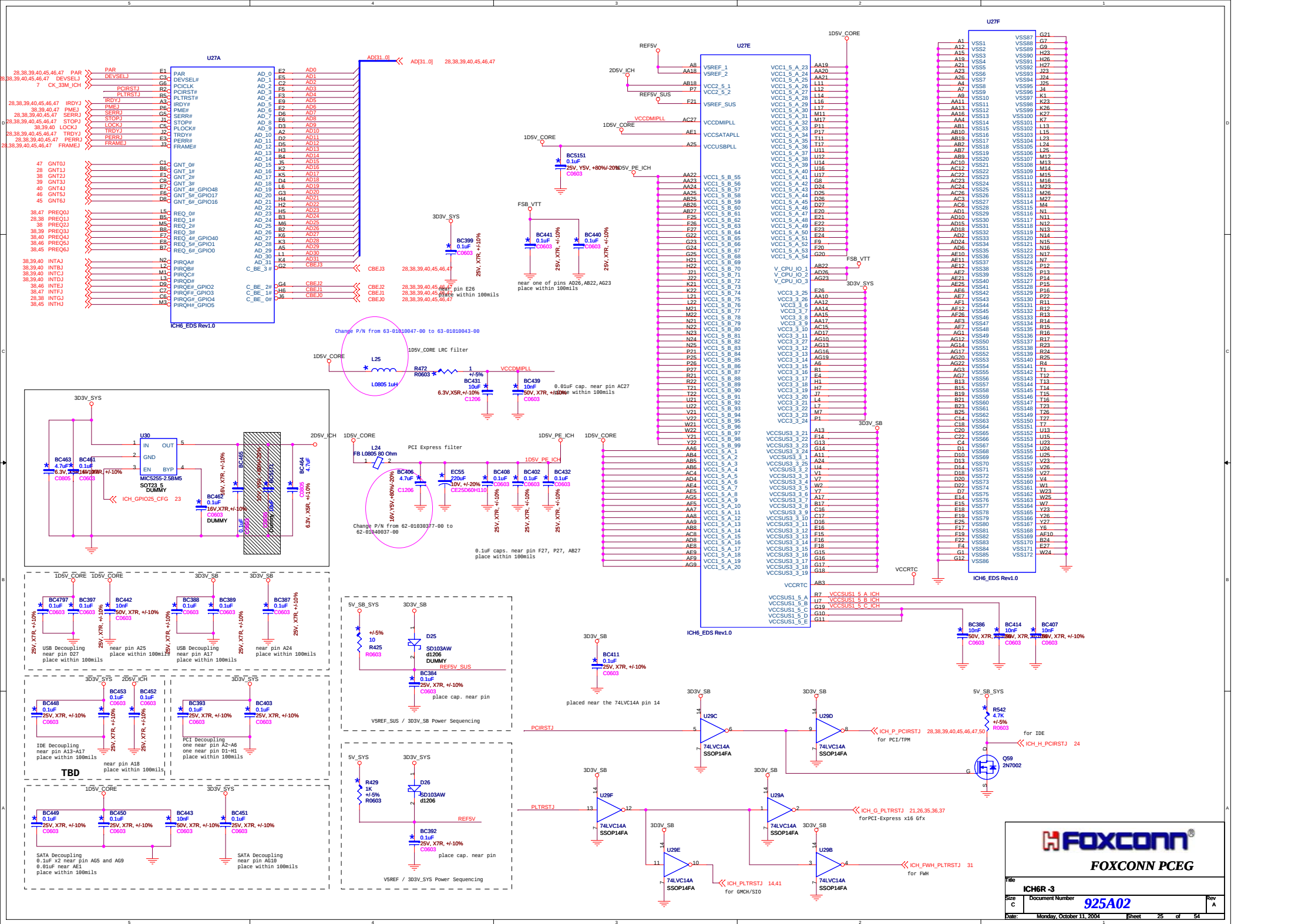


FOXCONN PCEG

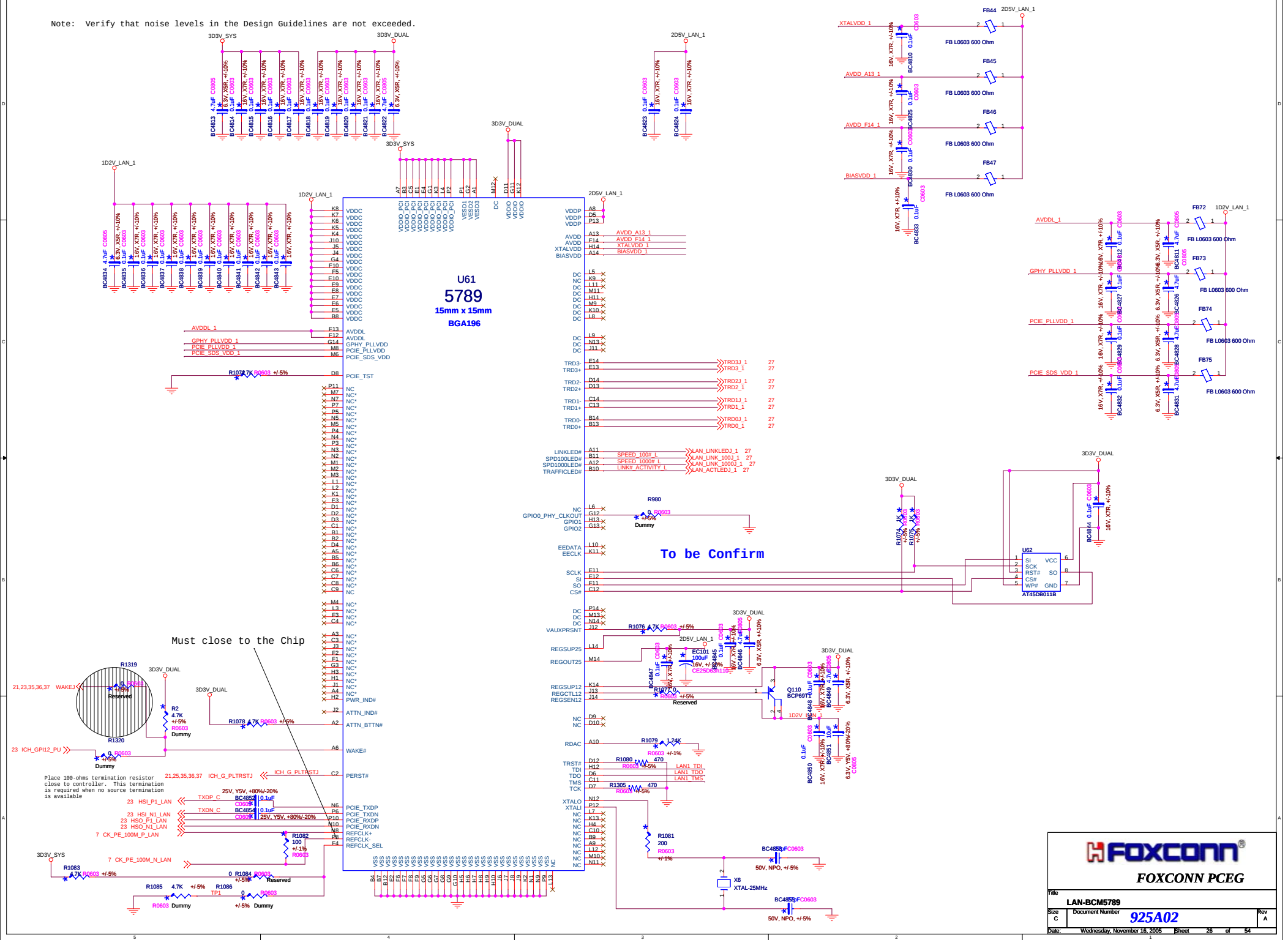
Title		
VGA Connector		
Size	Document Number	Rev
	AWA01	A
Date:	Monday, October 11, 2004	Sheet 22 of 54







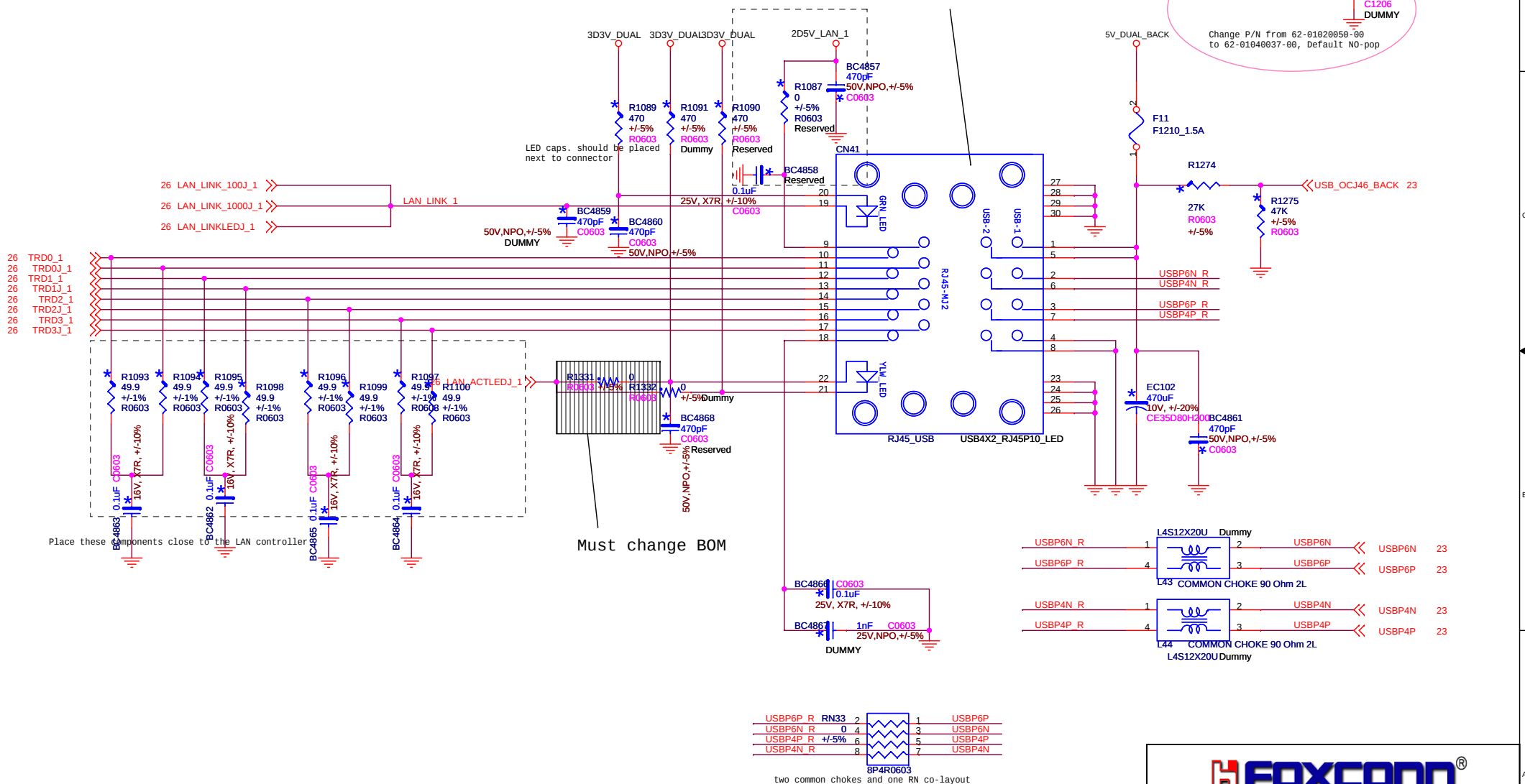
Note: Verify that noise levels in the Design Guidelines are not exceeded.



USE CONNECTOR(Foxconn P/N: JFM31U1A-01U5W) WITH GIGABIT DESIGN

For 5789 Mac LED Register =0000

Can be change to cost down conn
P/N = JFM31U1A-01U5W For GIGA LAN



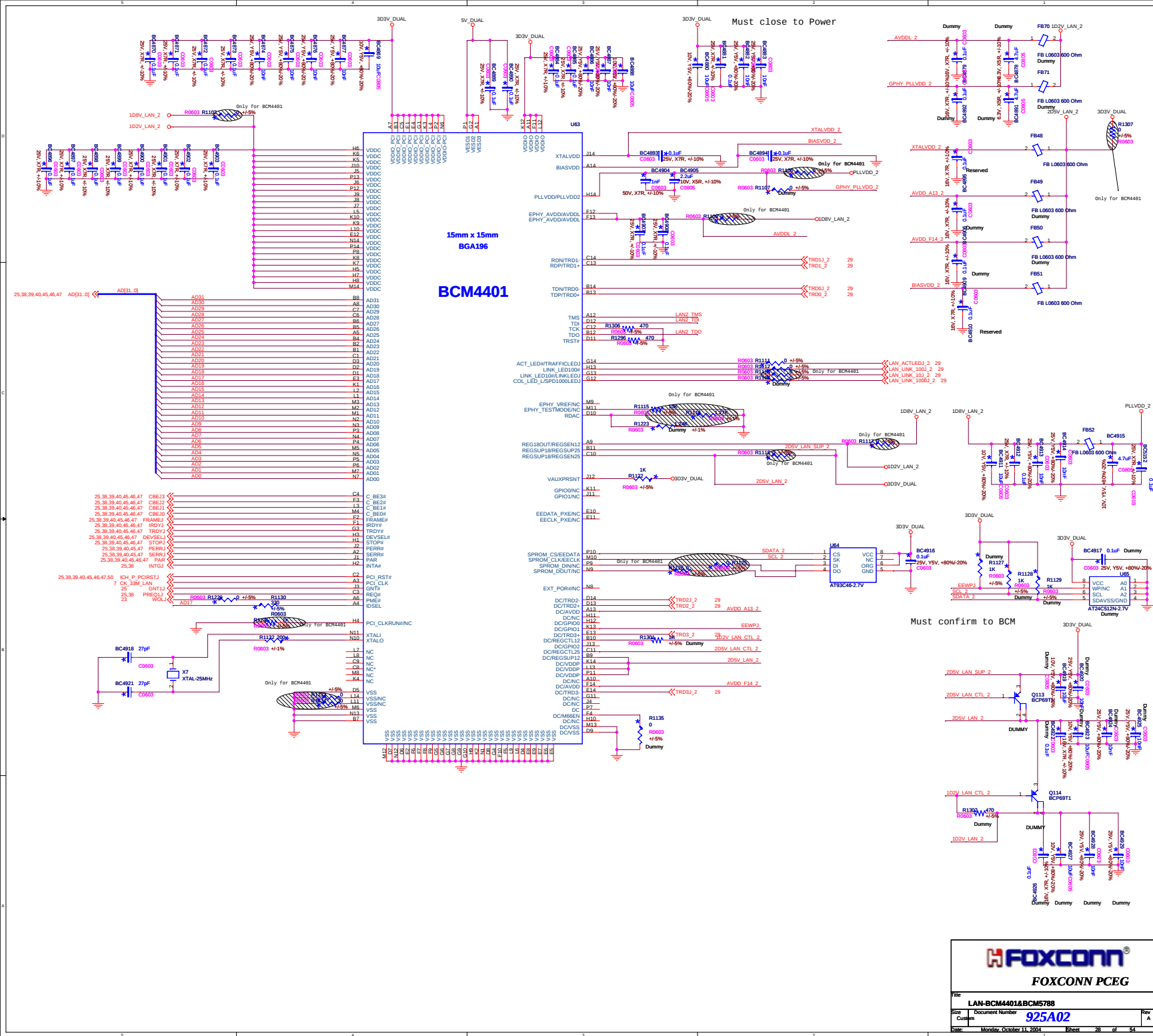
FOXCONN PCEG

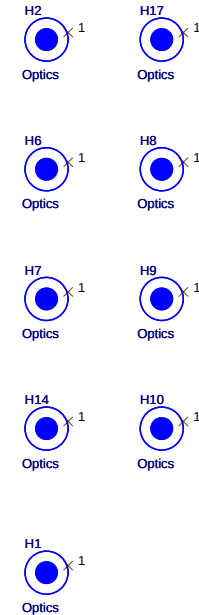
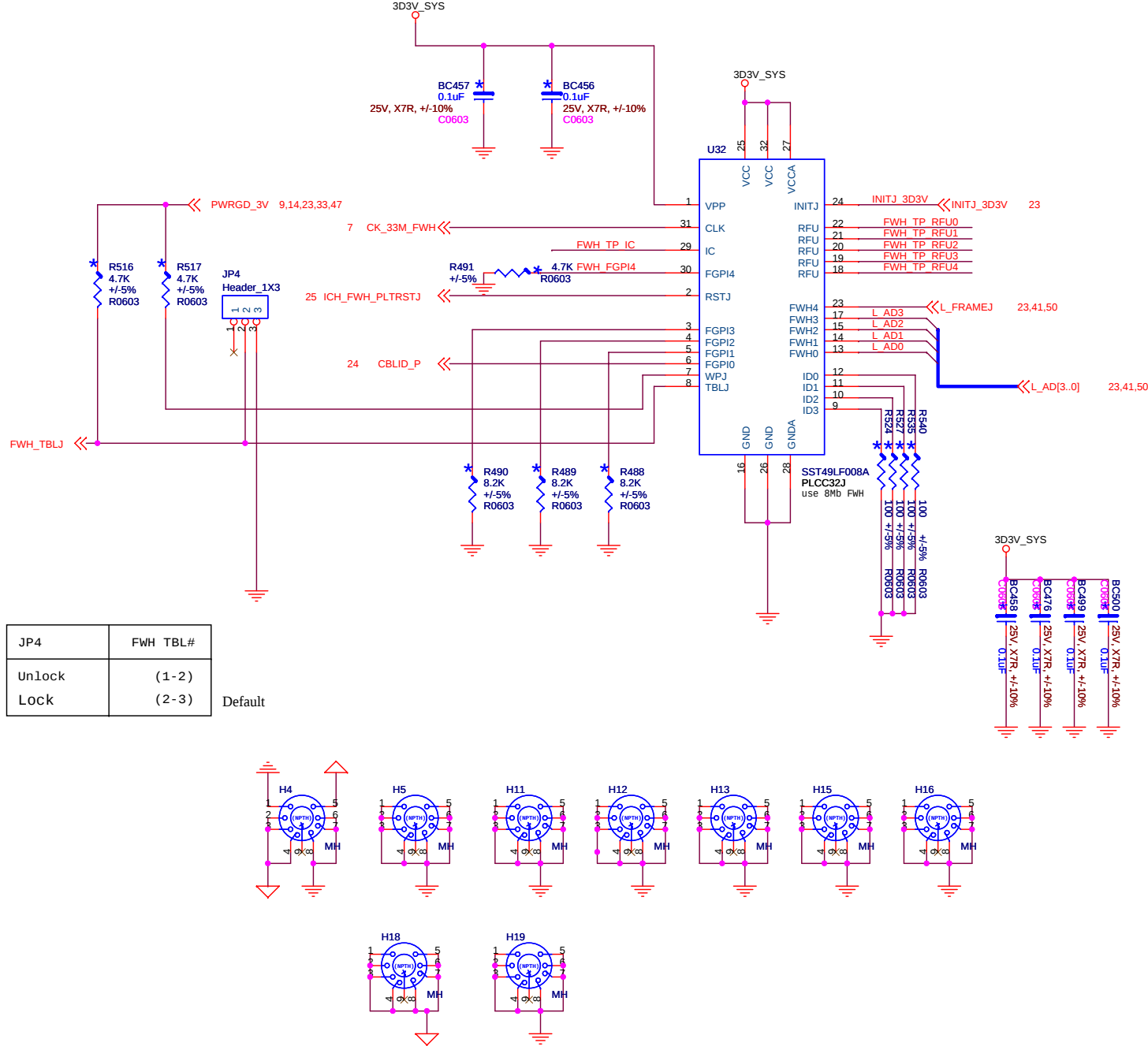
Title	LAN Connectors For BCM5789
-------	-----------------------------------

Size	Document Number
	925A02

Date:	Monday, October 11, 2004	Sheet	27	of	54
-------	--------------------------	-------	----	----	----

Re

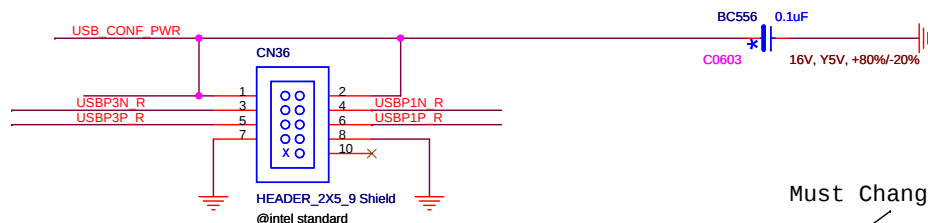
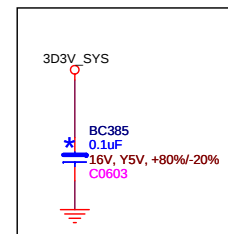
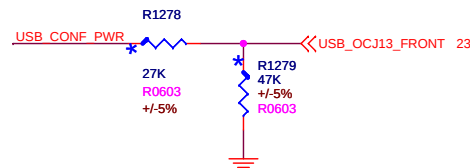
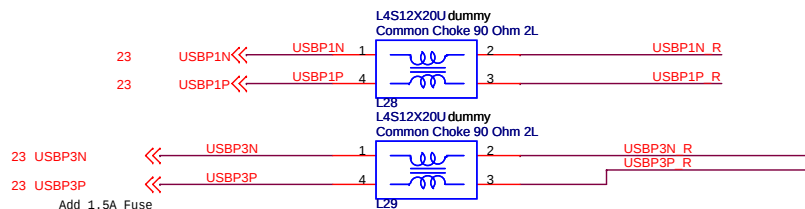
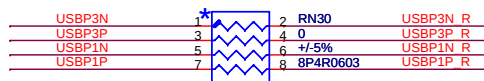




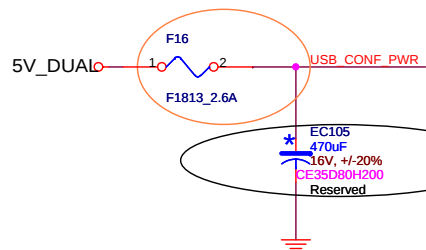
FOXCONN®
FOXCONN PCEG

USB Connector: Back side 4 ports and Front side 4 ports.

two common chokes and one RN co-layout

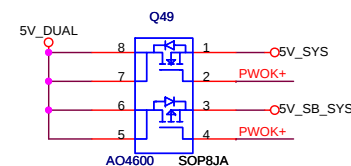
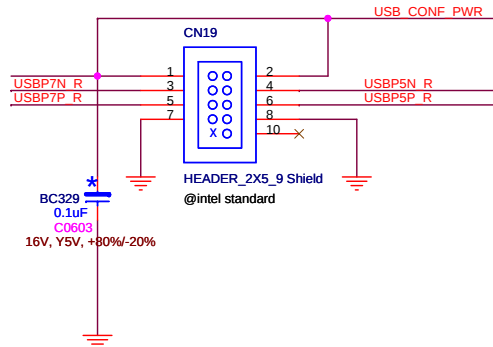
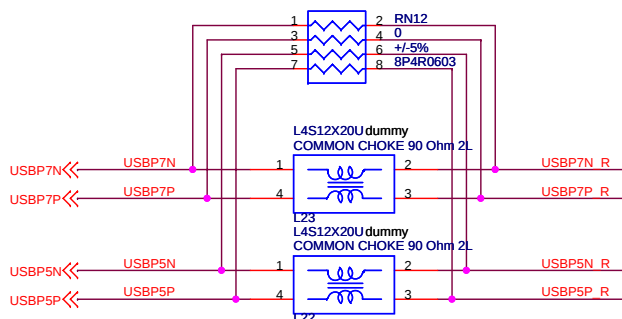


Must Change BOM

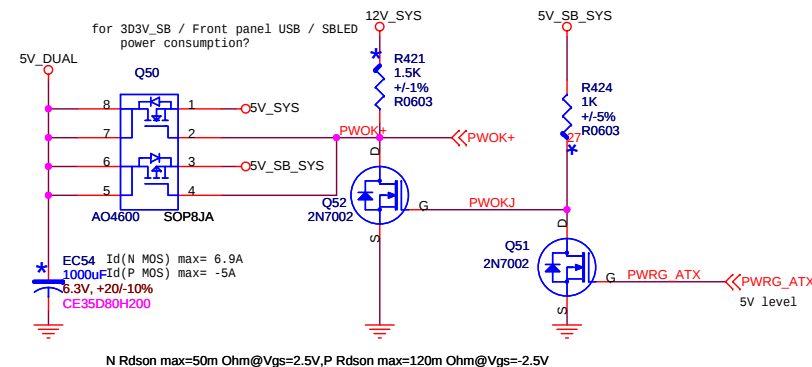


Change 2.6A to 1.5A

two common chokes and one RN co-layout



N Rdson max=50m Ohm@Vgs=2.5V,P Rdson max=120m Ohm@Vgs=-2.5V

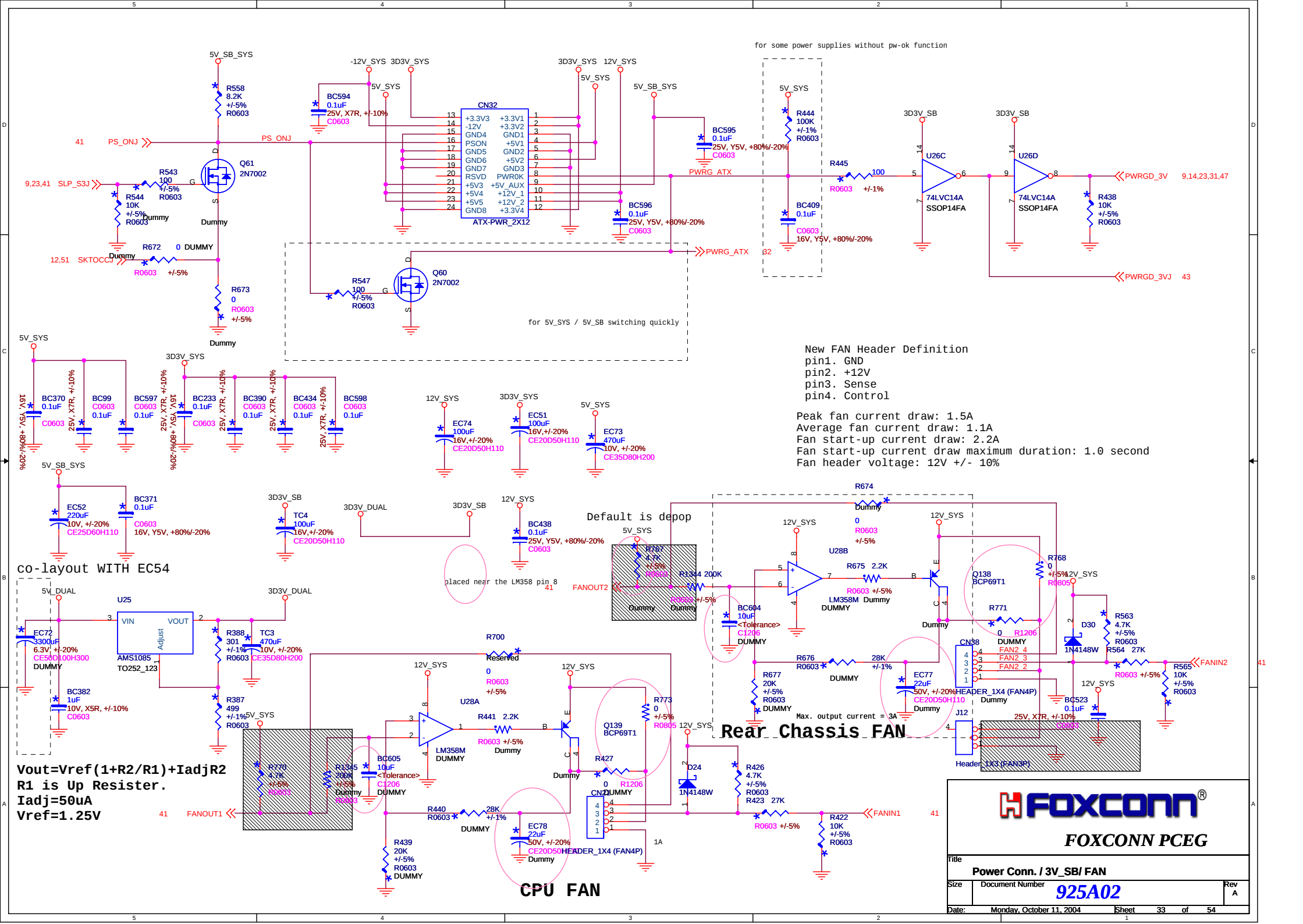


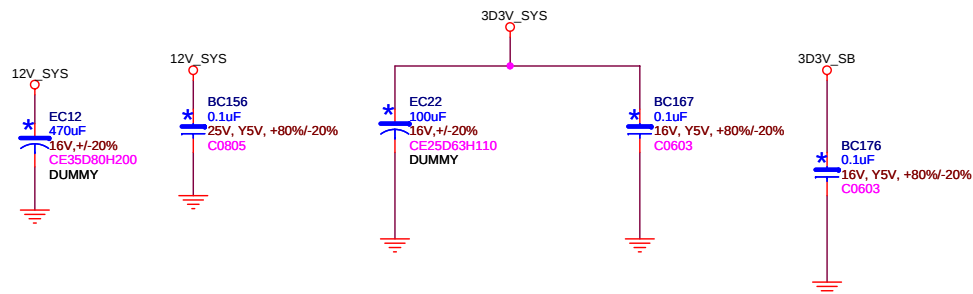
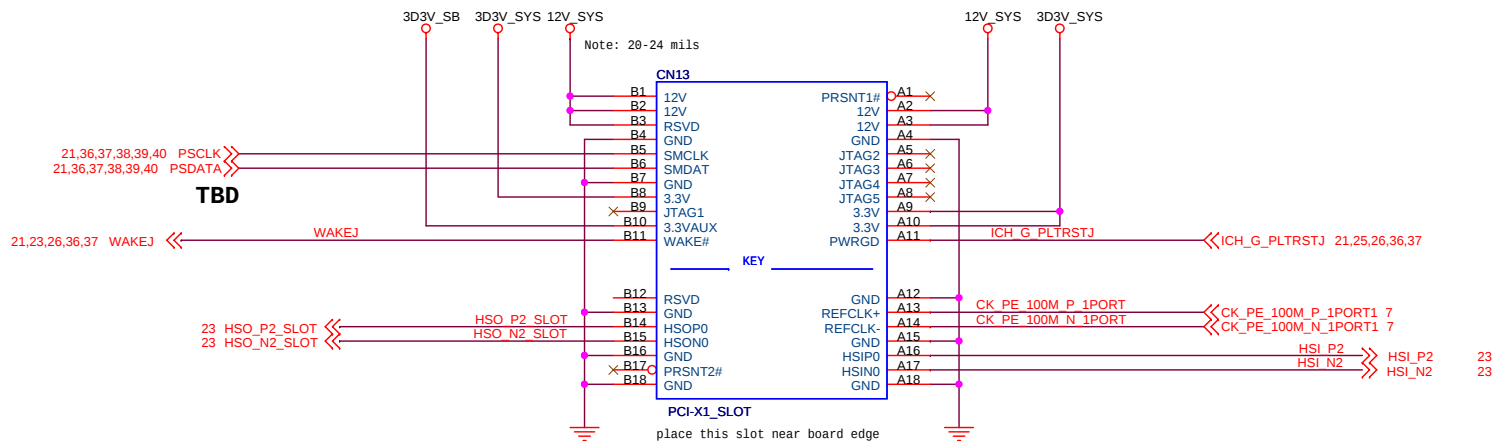
N Rdson max=50m Ohm@Vgs=2.5V,P Rdson max=120m Ohm@Vgs=-2.5V

FOXCONN®

FOXCONN PCEG

Title		
USB Connectors		
Size	Document Number	Rev
	925A02	A
Date:	Monday, October 11, 2004	Sheet 32 of 54

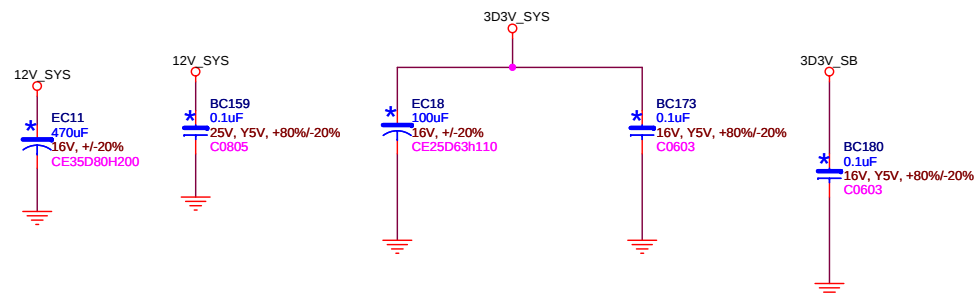
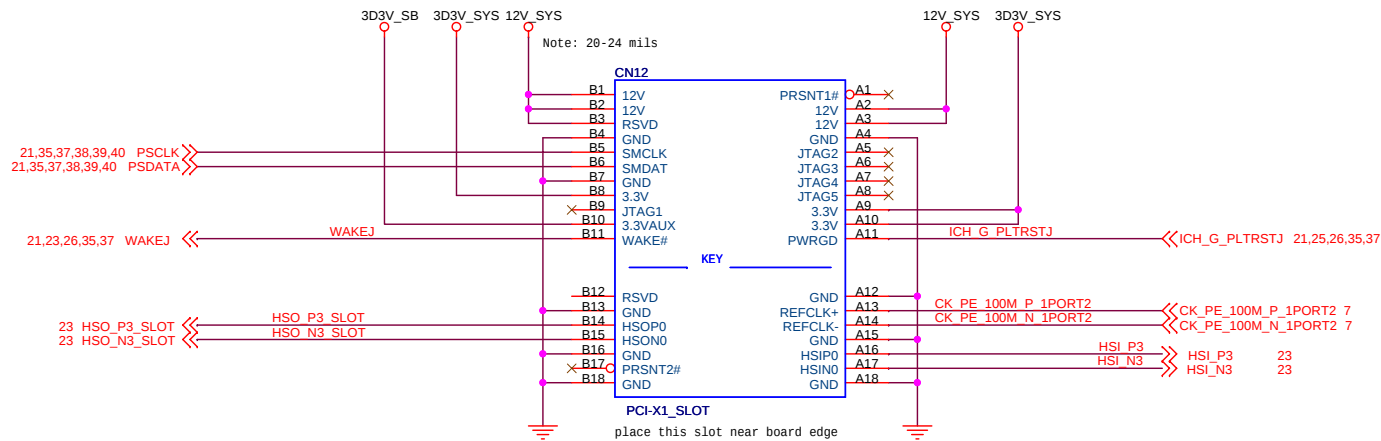




FOXCONN®

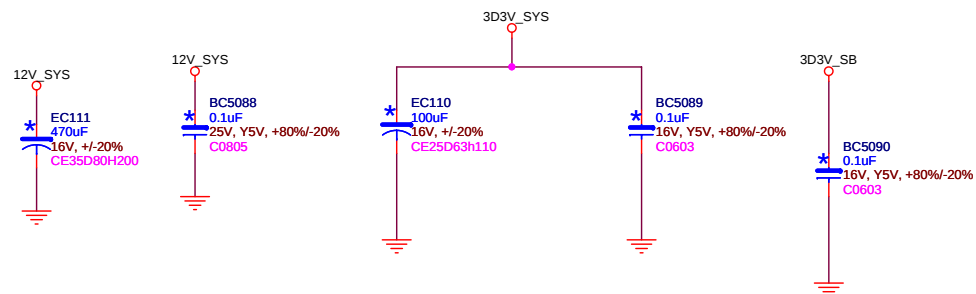
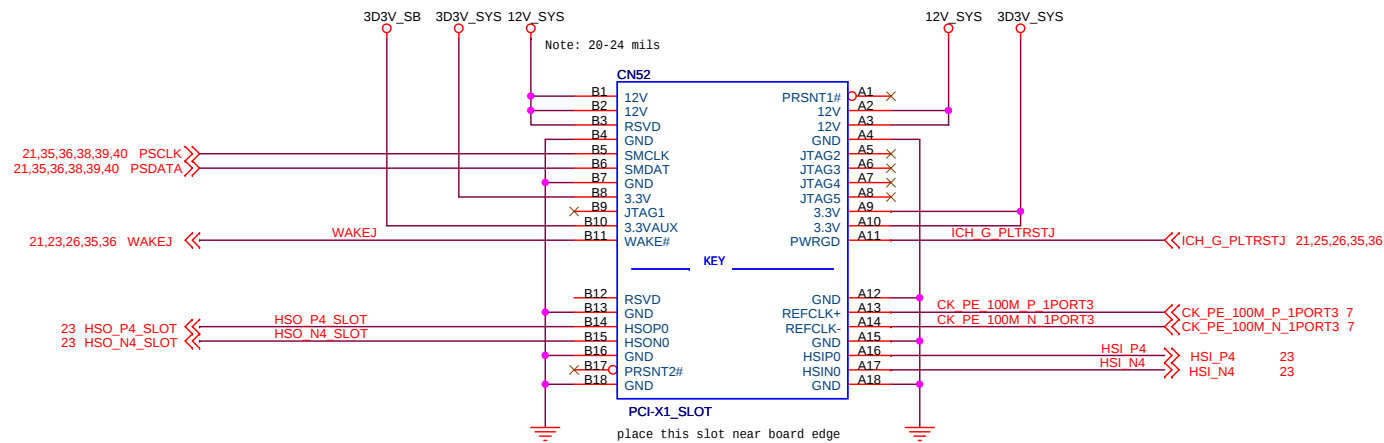
FOXCONN PCEG

Title		
PCI Express x1 Slot 1		
Size	Document Number	Rev
	925A02	A
Date:	Monday, October 11, 2004	Sheet 35 of 54



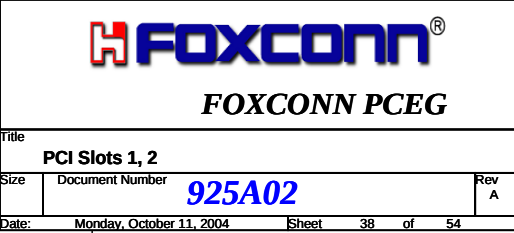
FOXCONN PCEG

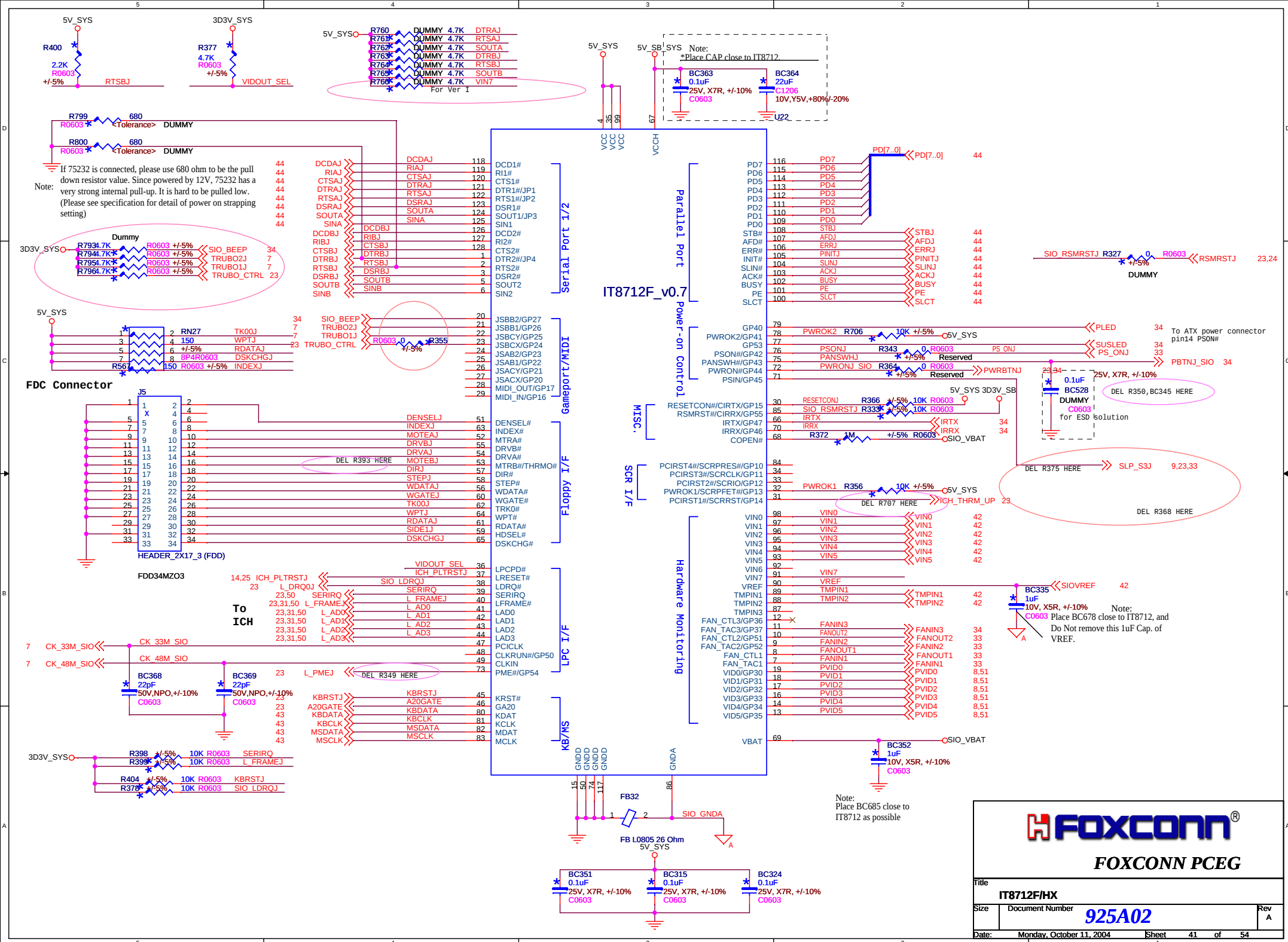
Title		
PCI Express x1 Slot 2		
Size	Document Number	Rev
	925A02	A
Date:	Monday, October 11, 2004	Sheet 36 of 54

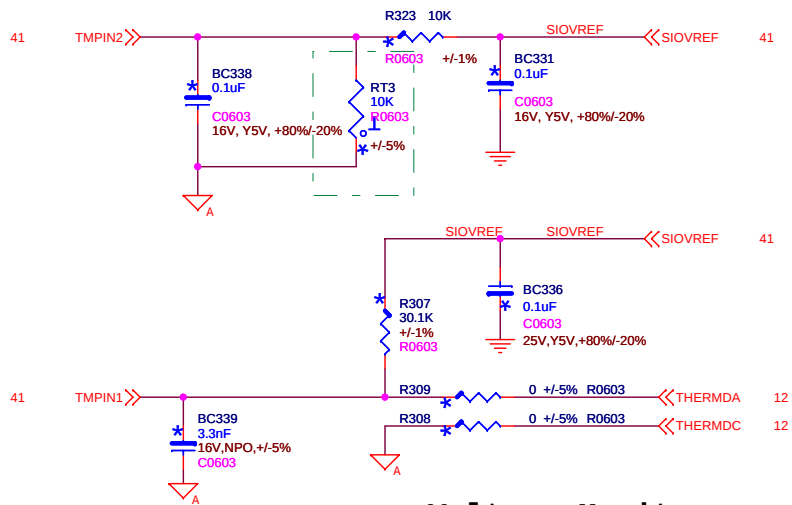


FOXCONN PCEG

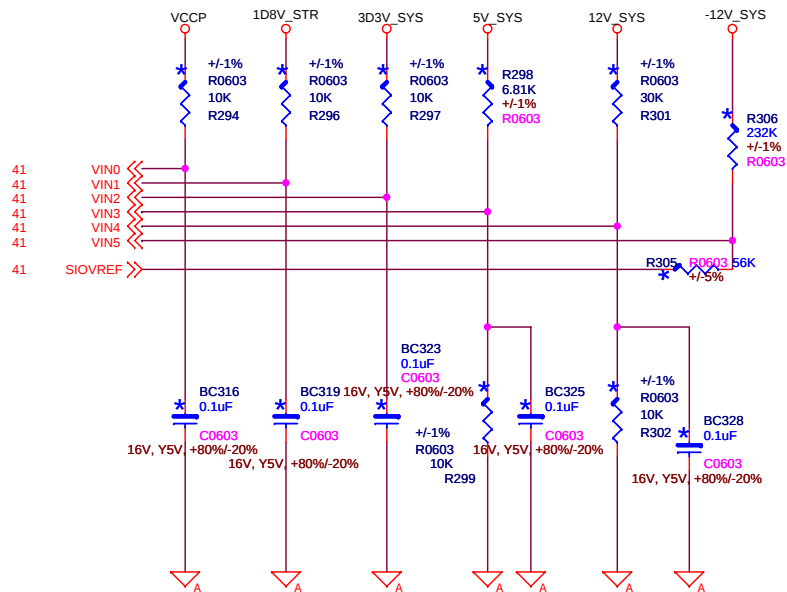
Title		
PCI Express x1 Slot 3		
Size	Document Number	Rev
	925A02	A
Date:	Monday, October 11, 2004	Sheet 37 of 54







Voltage Monitor



Power On Strapping Options

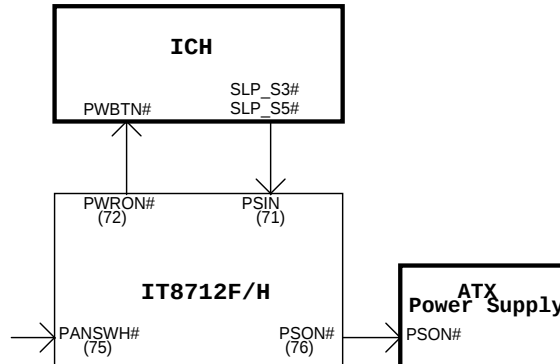
	Symbol	value	Description
DTR1#/JP1	KBCEN	1	KBC is enabled.
		0	KBC is disabled.
RTS1#/JP2	KBC_IROM	1	KBC's ROM is built in.
		0	KBC's ROM is external.
SOUT1/J3	CHIP_SEL	--	Chip selection in configuration.
DTR2#/JP4	BUF_SEL	1	The output buffers of PCIRST1#, PCIRST2#, PCIRST3#, and PCIRST4# are enhanced open-drain. It will drive high about 10~20ns when the signal transit from low to high, and then Hi-Z.
		0	The output buffers are push-pull.

*Recommended net "VCCH" minimum trace width 12mils.

The different function pins between IT8712F/H and IT8712F/G

Pin	IT8712F/HX	Pin	IT8712F/GX
13	VID5/GP35	13	WTI#/GP35
30	RESETCON#/CIRTX/GP15	30	CIRTX/GP15
31	PCIRST1#/SCRRST/GP14	31	SCRRST/GP14
32	PWROK1/SCRPFET#/GP13	32	SCRPFET#/GP13
33	PCIRST2#/SCRIO/GP12	33	SCRIO/ GP12
34	PCIRST3#/SCRCLK/GP11	34	SCRCLK/ GP11
77	GP53	77	RING#/GP53
78	PWROK2/GP41	78	GP41
84	PCIRST4#/SCRPRES#/GP10	84	SCRPRES#/GP10
85	RSMRST#/CIRRX/GP55	85	CIRRX/COPENO#/GP55

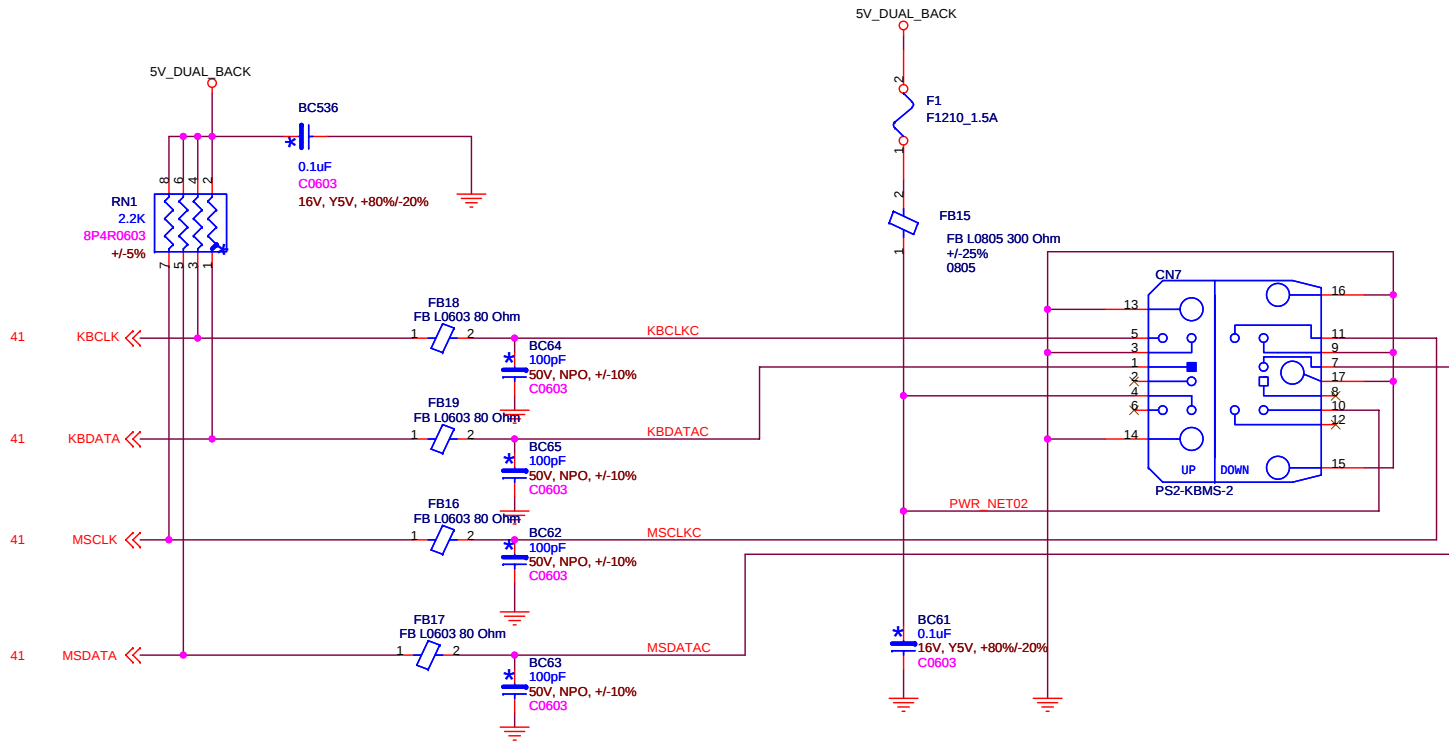
POWER ON SCHEME



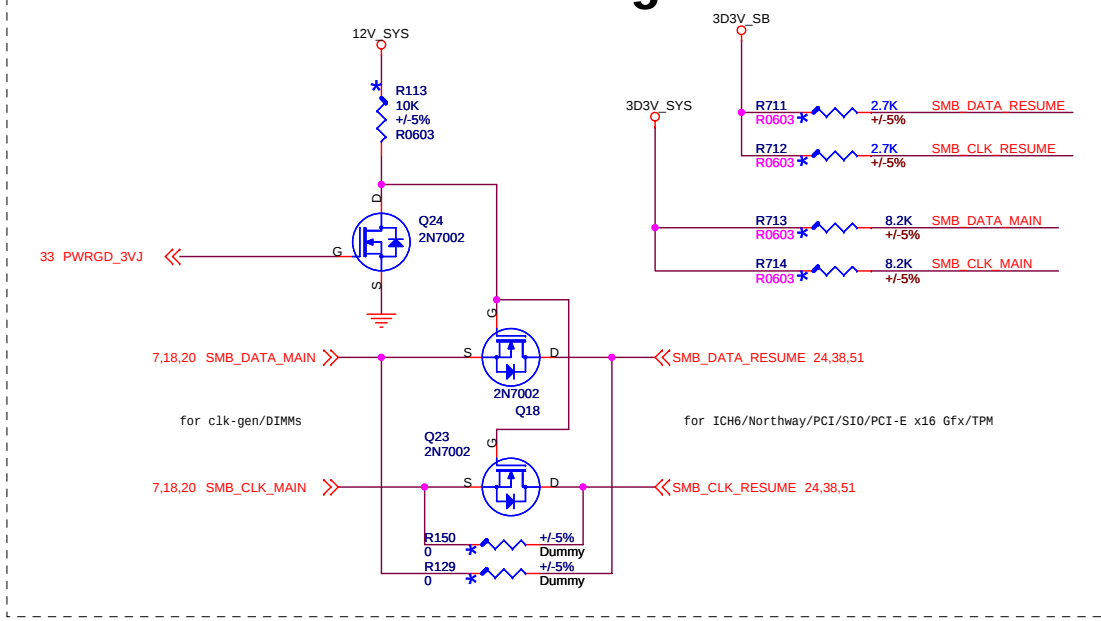
FOXCONN®

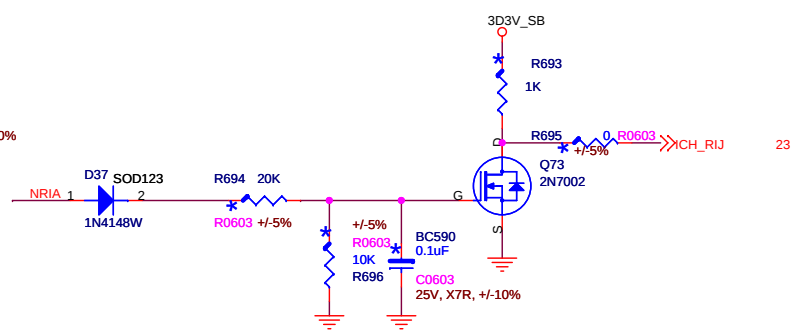
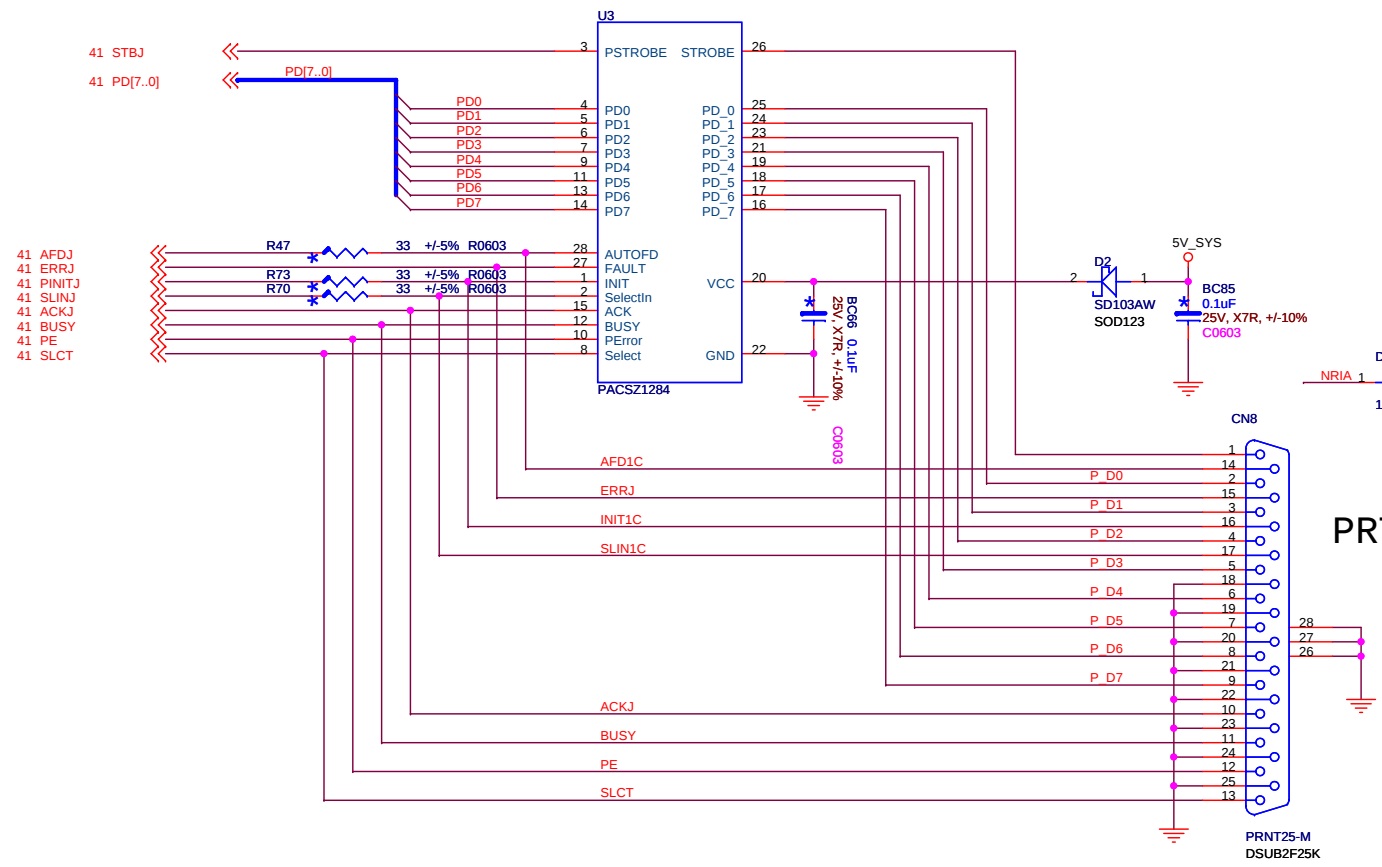
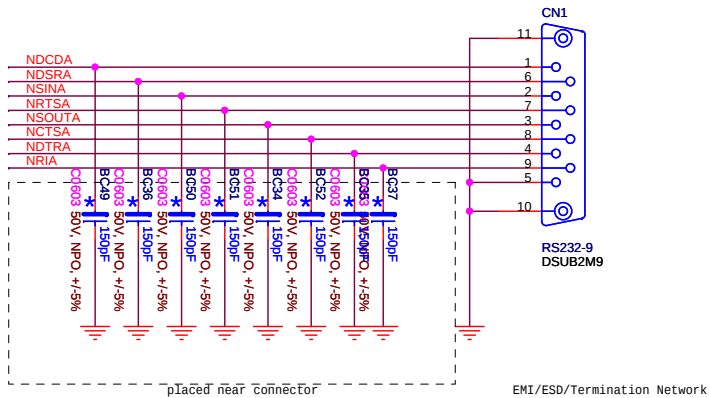
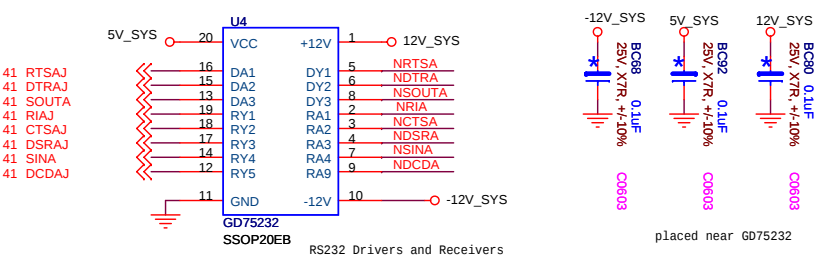
FOXCONN PCEG

Title HW Monitor		
Size	Document Number 925A02	Rev A
Date:	Monday, October 11, 2004	Sheet 42 of 54



SM Bus Bridge

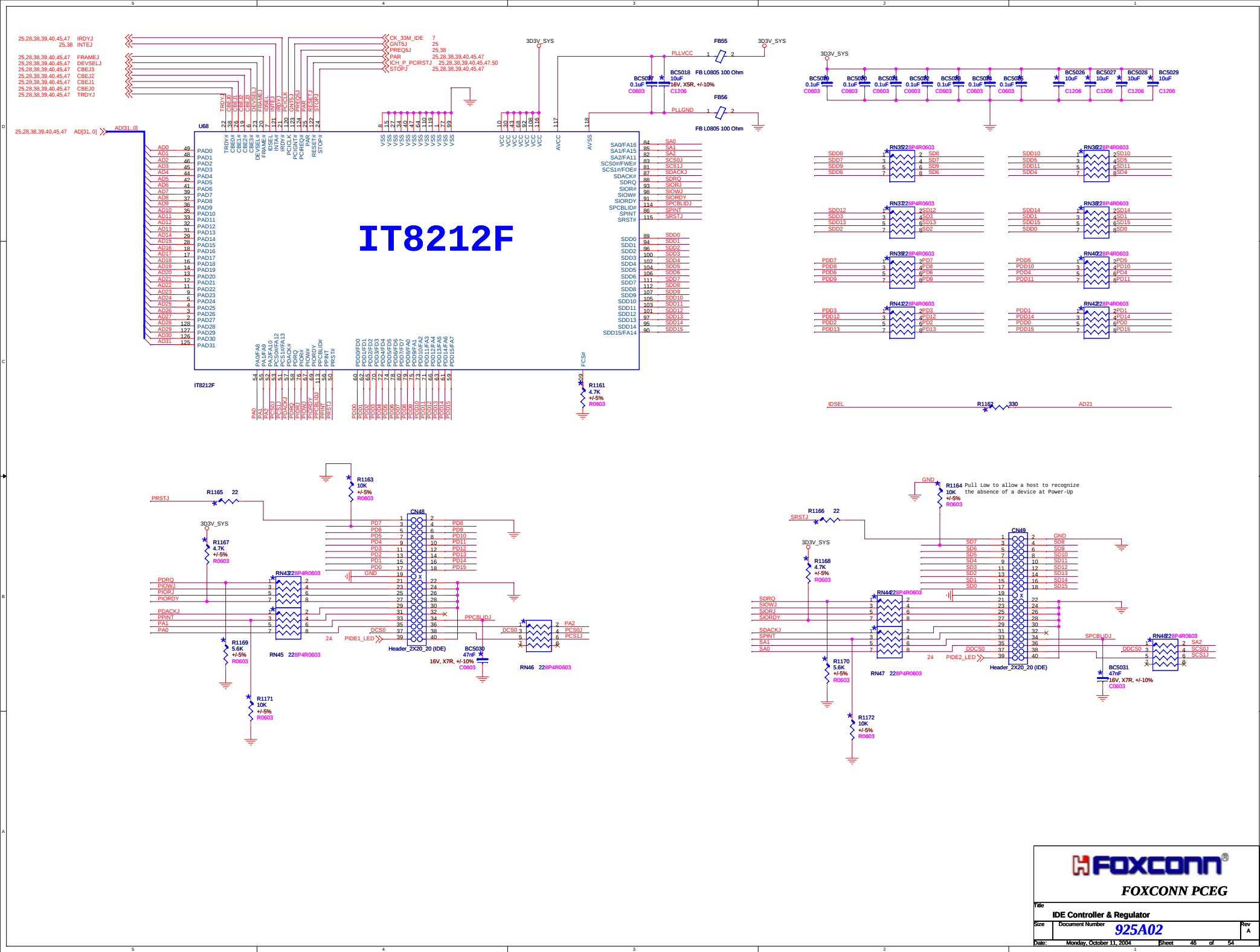


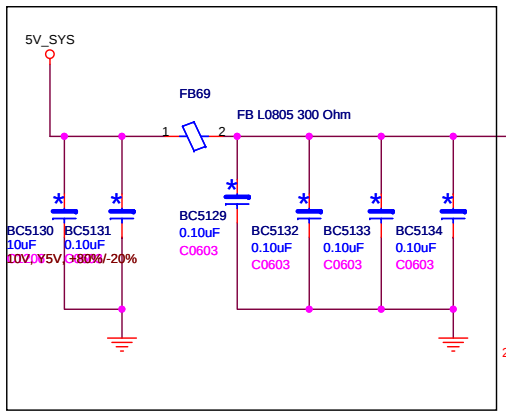


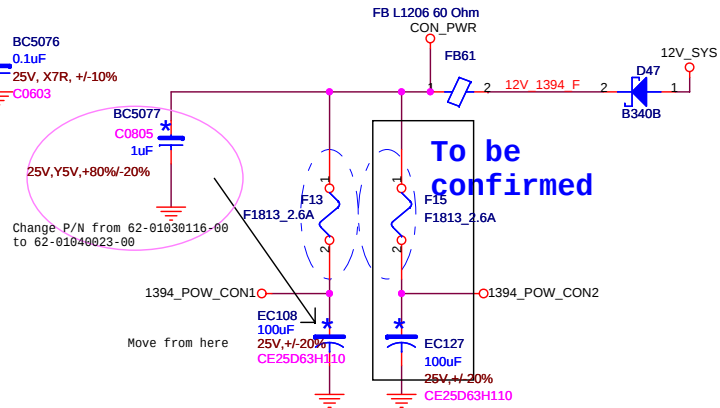
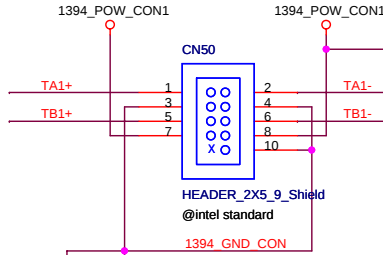
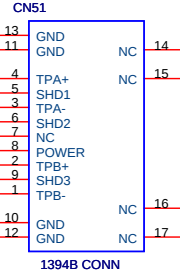
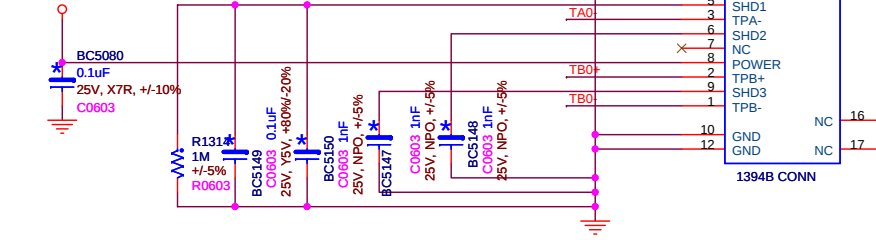
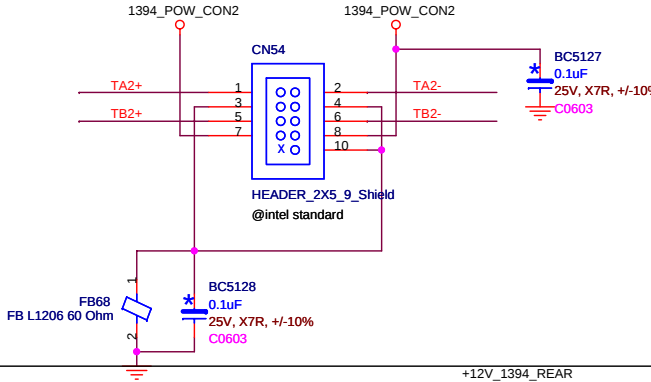
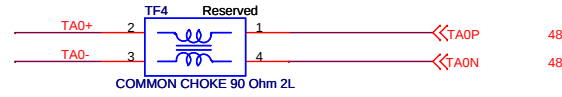
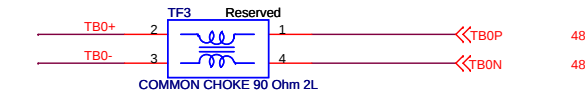
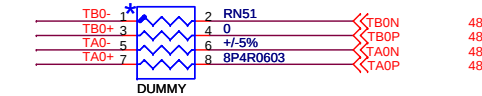
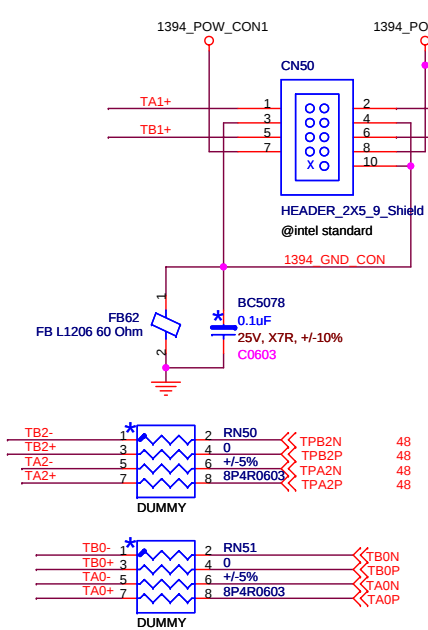
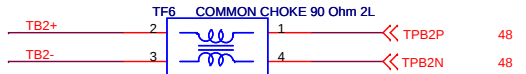
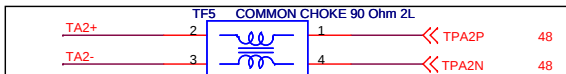
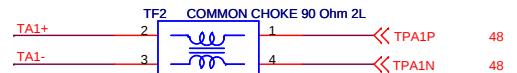
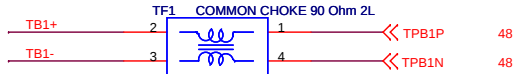
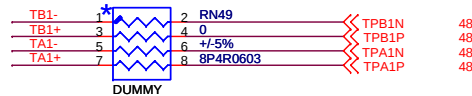


FOXCONN PCEG

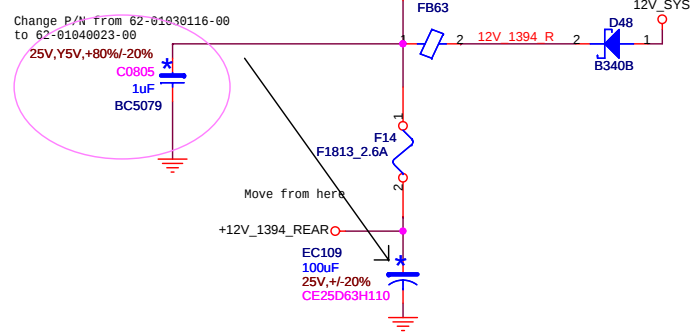
Title Serial / Parallel		
Size	Document Number 925A02	Rev A
Date:	Monday, October 11, 2004	Sheet 44 of 54

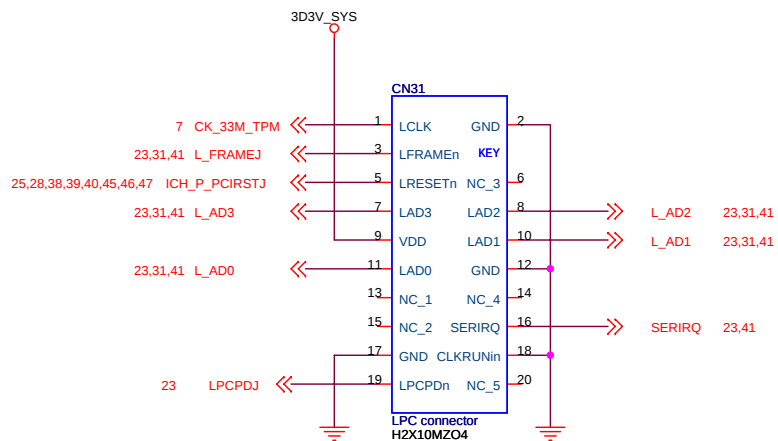






To be confirmed





FOXCONN PCEG

Title		
TPM		
Size	Document Number	Rev
	925A02	A
Date:	Monday, October 11, 2004	Sheet 50 of 54

ICH6 GPIO Summary

Name	Power Well	Type	Description
GPIO	V5REF	I	REQ_6#
GPIO1	V5REF	I	REQ_5#
GPIO2	V5REF	I	PIRQE#
GPIO3	V5REF	I	PIRQF#
GPIO4	V5REF	I	PIRQG#
GPIO5	V5REF	I	PIRQH#
GPIO6	Vcc3_3	I	Pull-up through 10K resistor(Unused)
GPIO7	Vcc3_3	I	Board ID0
GPIO8	VccSus3_3	I	LPC PME#
GPIO9	VccSus3_3	I	USB OC4#
GPIO10	VccSus3_3	I	USB OC5#
GPIO11	VccSus3_3	I	Pull-up through 10K resistor(Unused)
GPIO12	Vcc3_3	I	Pull-up through 10K resistor(Unused)
GPIO13	VccSus3_3	I	Wake On LAN
GPIO14	VccSus3_3	I	USB OC6#
GPIO15	VccSus3_3	I	USB OC7#
GPIO16	Vcc3_3	O	GNT_6#
GPIO17	Vcc3_3	O	GNT_5#
GPIO18	Vcc3_3	O	GP018(Unused)
GPIO19	Vcc3_3	O	GP019(Unused)
GPIO20	Vcc3_3	O	GP020(Unused)
GPIO21	Vcc3_3	O	GP021(Unused)
GPIO22	N/A	N/A	Not Implemented
GPIO23	Vcc3_3	O	GP023(Unused)
GPIO24	VccSus3_3	I/O	GPIO24(Unused)
GPIO25	VccSus3_3	I/O	GPIO25 Strap: 2.5 VRM Enable
GPIO26	Vcc3_3	I	SATA_0GP
GPIO27	VccSus3_3	I/O	Board ID2
GPIO28	VccSus3_3	I/O	GPIO LAN Disable
GPIO29	Vcc3_3	I	SATA_1GP
GPIO30	Vcc3_3	I	SATA_2GP
GPIO31	Vcc3_3	I	SATA_3GP
GPIO32	Vcc3_3	I/O	Board ID1
GPIO33	Vcc3_3	I/O	THERMAL CONTROL
GPIO34	Vcc3_3	I/O	Board ID3
GPIO35	N/A	N/A	Not Implemented
GPIO36	N/A	N/A	Not Implemented
GPIO37	N/A	N/A	Not Implemented
GPIO38	N/A	N/A	Not Implemented
GPIO39	N/A	N/A	Not Implemented
GPIO40	V5REF	I	REQ_4#
GPIO41	Vcc3_3	I	TBD
GPIO42	N/A	N/A	Not Implemented
GPIO43	N/A	N/A	Not Implemented
GPIO44	N/A	N/A	Not Implemented
GPIO45	N/A	N/A	Not Implemented
GPIO46	N/A	N/A	Not Implemented
GPIO47	N/A	N/A	Not Implemented
GPIO48	Vcc3_3	O	GNT_4#
GPIO49	V_CPU_IO	OD	CPUPWRGD

Super I/O GPIO Summary

Name	Power Plane	Type	Description
GPIO10-17	Main	I/O	Not Implemented
GPIO20	Main	I/O	SIO-BEEP
GPIO30	Main	I/O	VID0
GPIO31	Main	I/O	VID1
GPIO32	Main	I/O	VID2
GPIO33	Main	I/O	VID3
GPIO34	Main	I/O	VID4
GPIO35	Main	I/O	VID5
GPIO40	Main	I/O	POWER LED
GPIO41	Main	I/O	SUSPEND LED
GPIO42	Main	I/O	PS-ON TO ATX POWER CONN.
GPIO43	Main	I/O	POWER BUTTON-IN
GPIO44	Main	I/O	POWER BUTTON TO ICH6
GPIO45	Main	I/O	PS-IN
GPIO46	Main	I/O	IRRX
GPIO47	Main	I/O	IRTX
GPIO50	Main	I/O	Not Implemented
GPIO43	Main	I/O	POWER BUTTON-IN
GPIO44	Main	I/O	POWER BUTTON TO ICH6
GPIO45	Main	I/O	PS-IN
GPIO46	Main	I/O	IRRX
GPIO47	Main	I/O	IRTX
GPIO51	Main	I/O	FAN_CTRL2
GPIO52	Main	I/O	FAN_TAC2
GPIO53	Main	I/O	THERM-UP TO ICH6
GPIO54	Main	I/O	PME
GPIO55	5V_SB	I/O	RSMRST

FWH GPIO Summary

Name	Power Plane	Type	Description
FGPIO	Main	I	IDE1 Cable Detection(33 or 66/100)
FGPIO1	Main	I	Unused
FGPIO2	Main	I	Unused
FGPIO3	Main	I	Unused

PCI Routing Summary

	PCI1	PCI2	PCI3	1394	LAN
INTA#	B	A	C		
INTB#	C	B	D		
INTC#	D	C	A		
INTD#	A	D	B		
INTE#					
INTF#				A	
INTG#					A
INTH#					
REG#/GNT#	2	3	4	0	1
IDSEL	18	19	20	16	17

Jumper Setting Summary

JP5	Clear CMOS 1-2 : Normal (Default) 2-3 : Clear CMOS
JP4	FWH TBL# 1-2 : Unlock 2-3 : Lock

TBD

GrantsDale Family Option Table

82570EI and 82562EX Option Table

ALC655, ALC650 and ALC203 Option Table

- Changed from GDM03 FAB-A: Date: 12/22/2003
1. Change R562 from dummy to 5.6K (P34)
 2. Change D13 to D340B package
 3. Add ICH_LAN_RST circuit (p24)
 4. Change PW_ON solution from SI0 to ICH (P33,34,38)
 5. Change U26, U28 P/N
 6. Del VGA portion (P23)
 7. Co-lay VRD output coil (P9)
 8. Add processor present detect circuit (P34,13)
 9. Change BC62-BC64 from 220pF to 100pF to solve PS2 mouse crazy issue (P42)
 10. swap u28(LM358) pin 2,3 (p33)
 11. Change Grantsdale to Alderwood and the peripheral circuit (p15-17)
 12. Add ECC signal to DDR2 (P18,20)
 13. Change R342 from 330 to 0 to solve pw-on too slow (P34)
 14. De-pop BC432 and U30, add R502 to enable ICH6 internal 2.5v Regulator (P26,24)
 15. De-pop Q48, R389, add R324 to combine 3vsb and 3vdau1 (P33)
 16. De-pop R400-R403 for LAD0-3 has internal pull-up res in ICH (P40)
 17. Change power decoupling 1uF Cap BC24,BC119,BC138,BC322, BC212,BC213,BC501,BC512,BC525,BC516,BC544,BC531,BC532 from Y5V TO X7R

- Changed from FAB-A to B: Date: 2/13/2003
18. Add co-lay circuit for JFET on DDR2 HS, Vcore LS(P9,10)

22. Change CLOCK GEN IDTCV115-2:
23. Change VID controller from PAC651 to IT8266R (P45)
24. Add Azalia conn. colay with AC97 conn. (P30)
25. Change Rear FAN circuit (P33)
26. Add com port ring circuit (P41)
27. Change all SMT CAP for power from Y5V to X7R
28. Add leakage current prevent circuit (P24)
29. Change Lan led and conn pin9 circuit (p29)
30. Change LAN pin23 circuit(P27)
31. Change 1394 clock pin conn(p7).
32. Add Rear line_out 2 resistor R704,R705 colay to 2 CAP(P30)

FAB-B to FAB-C(Include BOM) Changed items:

1. Add optional signal (PWRGD) for overclock fail reset(P7)
2. Change L19, L26 to R0520-120106Y-L3.4(P11,10)
3. Add R789 for short diode(P8)
4. Add substitution circuit for 2.5_MCH power sequency according to Intel CRB sch 1.3(P12)
5. Seperate on-board LAN/LAN card/Modem card wake-up fucntion(P34,P27)
6. Change BC292-4,BC286 to 3.3V_1394_CHIP and pop BC230,BC231(P44)
7. Add CMI9880 colayout circuit and remove SPDIF-IN (P30)
8. Change FAN control ciucuit(P33)
9. Add L34 for cost down opportunity(P17)
10. Add LPC_PD pull up res. (P24)
11. Add SPK 4 pin header(p34)
12. Change FWH_WP to FWH_TBL to let driver know the status of TBL(P24,31)
13. Del R432 for it's redundant to pull up FWH_TBL (P21)
14. Change 1394 clock from pin5 to pin4(P7)
14. Change 1394 clock from pin5 to pin4(P7)



FOXCONN PCEG

Title			
Modify List			
Size	Document Number		Rev
	925A02		A
Date:	Monday, October 11, 2004		Sheet 54 of 54