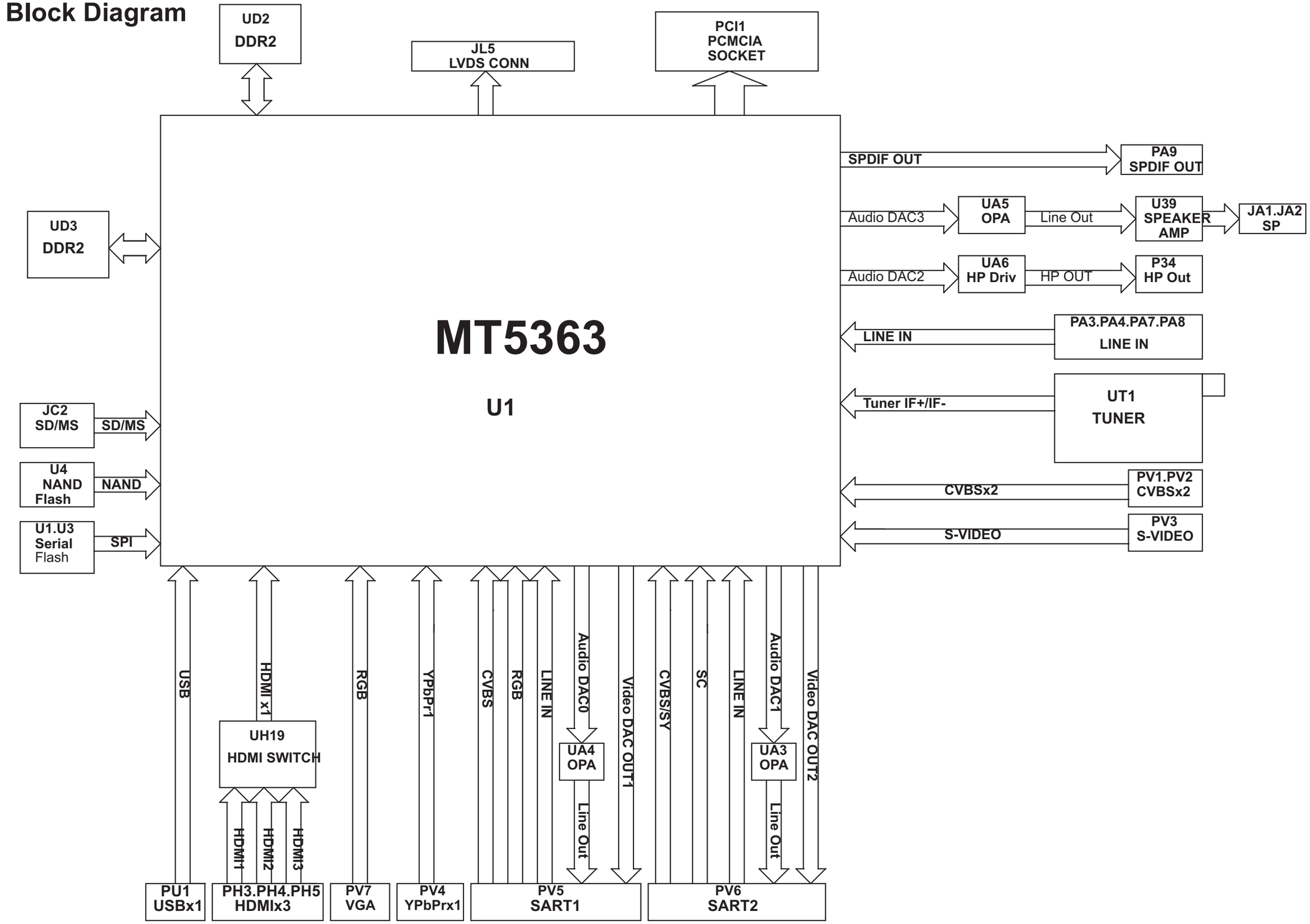
Block Diagram



01	12/05/11		Liberação inicial		
Revisão	Data	Documento	Descrição		
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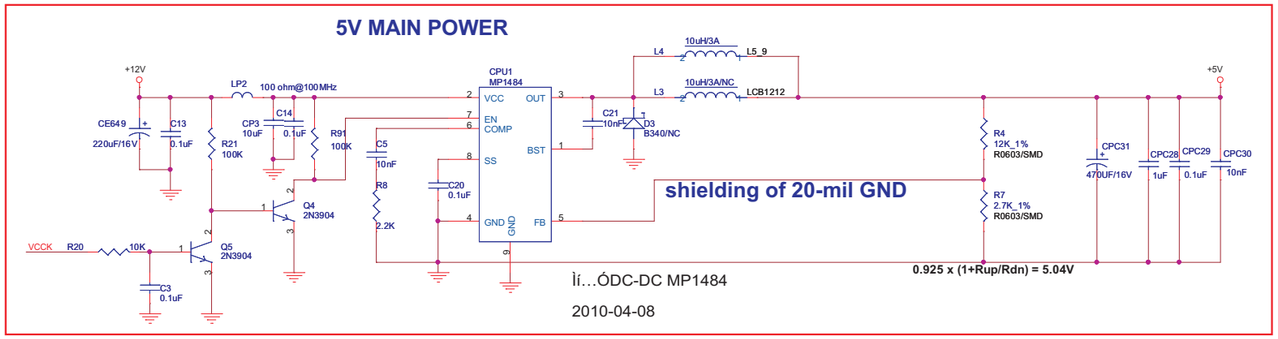
Escala S/E	Dimensão mm	Tol.não especificada	Página 1/21	Código matriz	
PCI principal HBTV-32L02HD / HBVT-42L02FD				Código sistema	BUSTER

MAIN POWER

Note :
The power connected to RP4 should turn UP8 off when +5V is turning on. Therefore,
If +5VSB lead +5V, please insert RP38.
If +5V lead +5VSB, please insert RP41.

5V MAIN POWER



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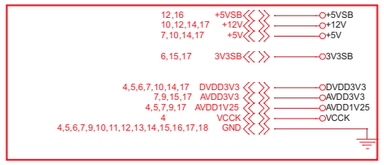
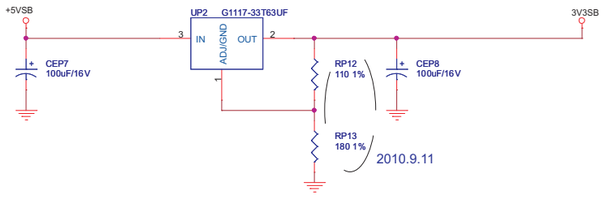
2010-04-08

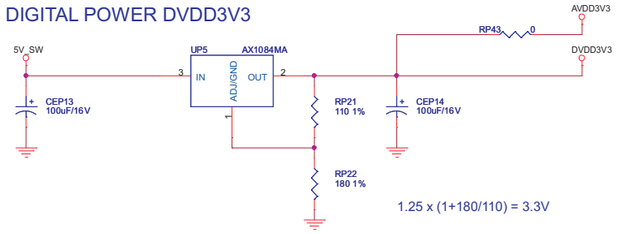


Other Control Interface

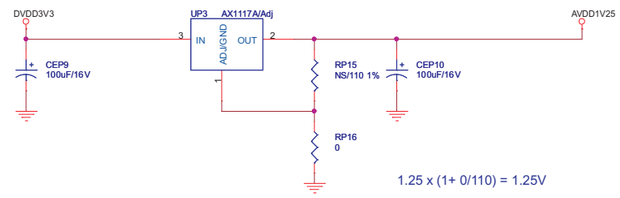
STANDBY POWER 3V3SB

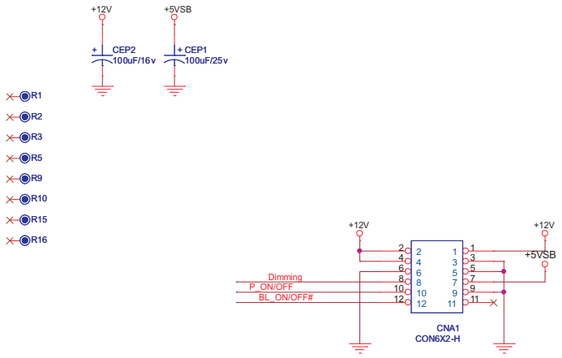


DIGITAL POWER DVDD3V3

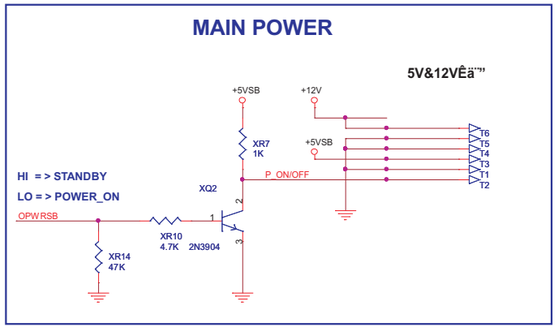


ANALOG POWER AVDD1V25

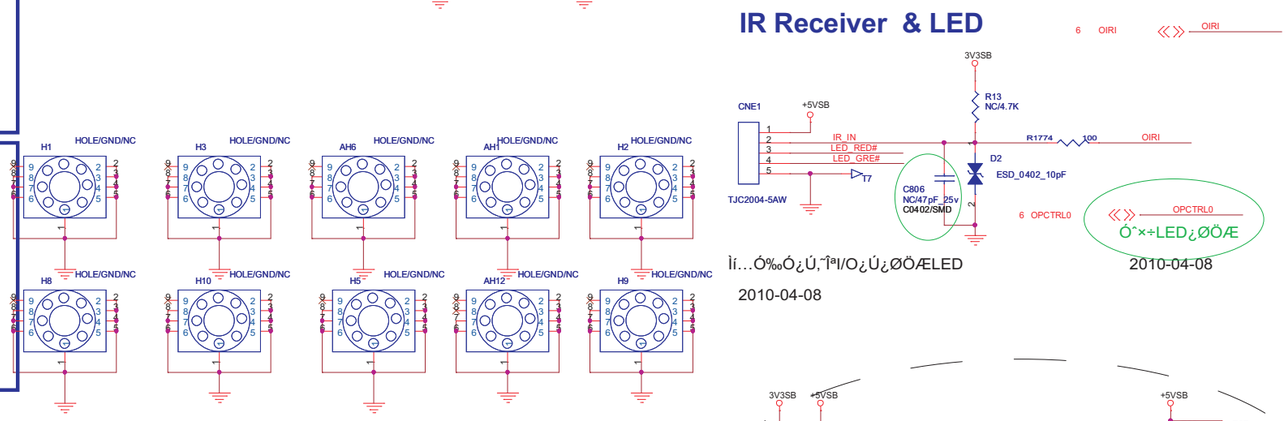




MAIN POWER



IR Receiver & LED



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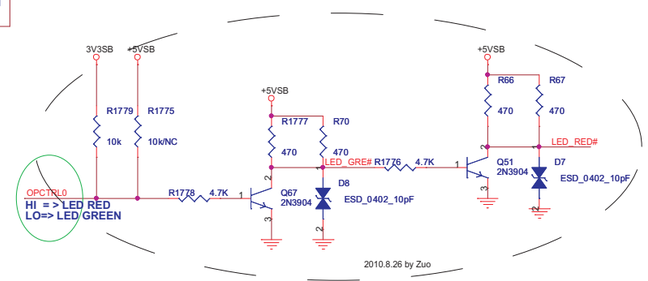
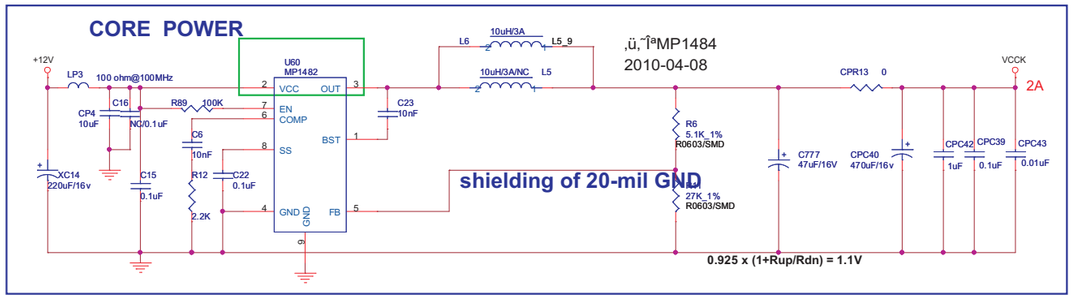


CORE POWER



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2010-04-08

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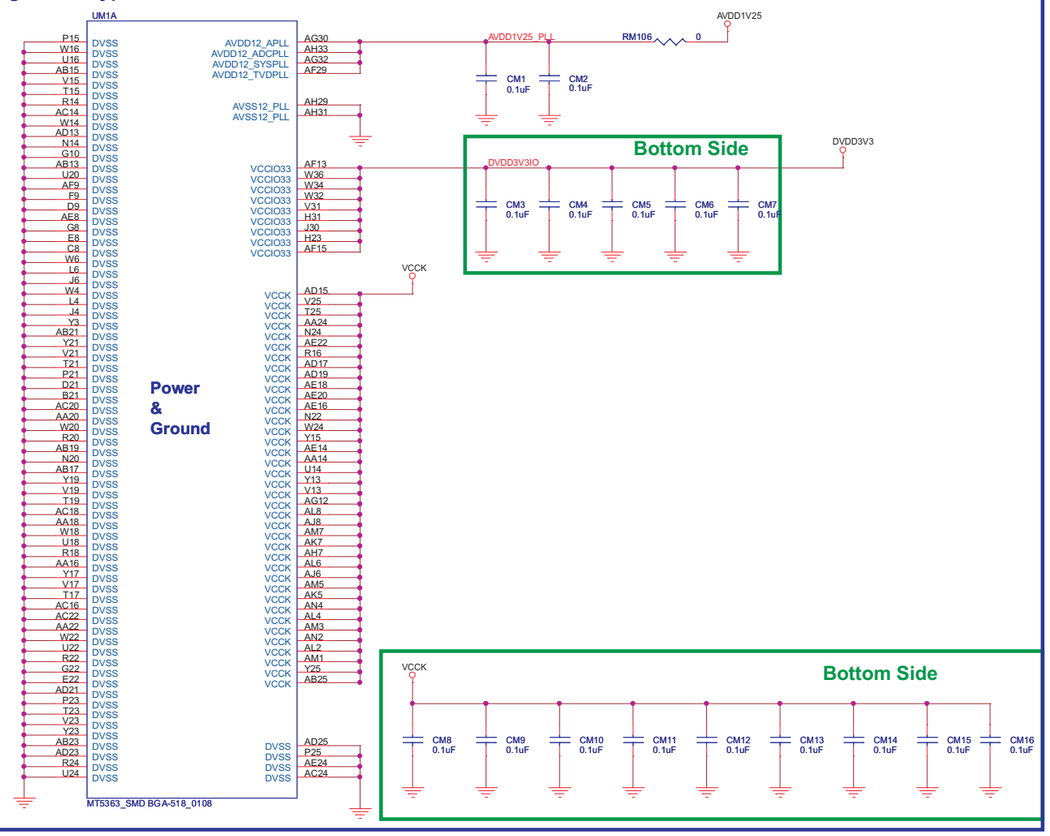
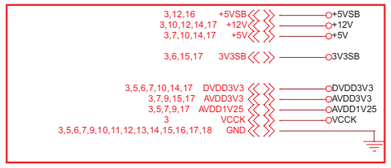
PCI principal HBTV-32L02HD / HBVT-42L02FD					Código sistema

BUSTER®

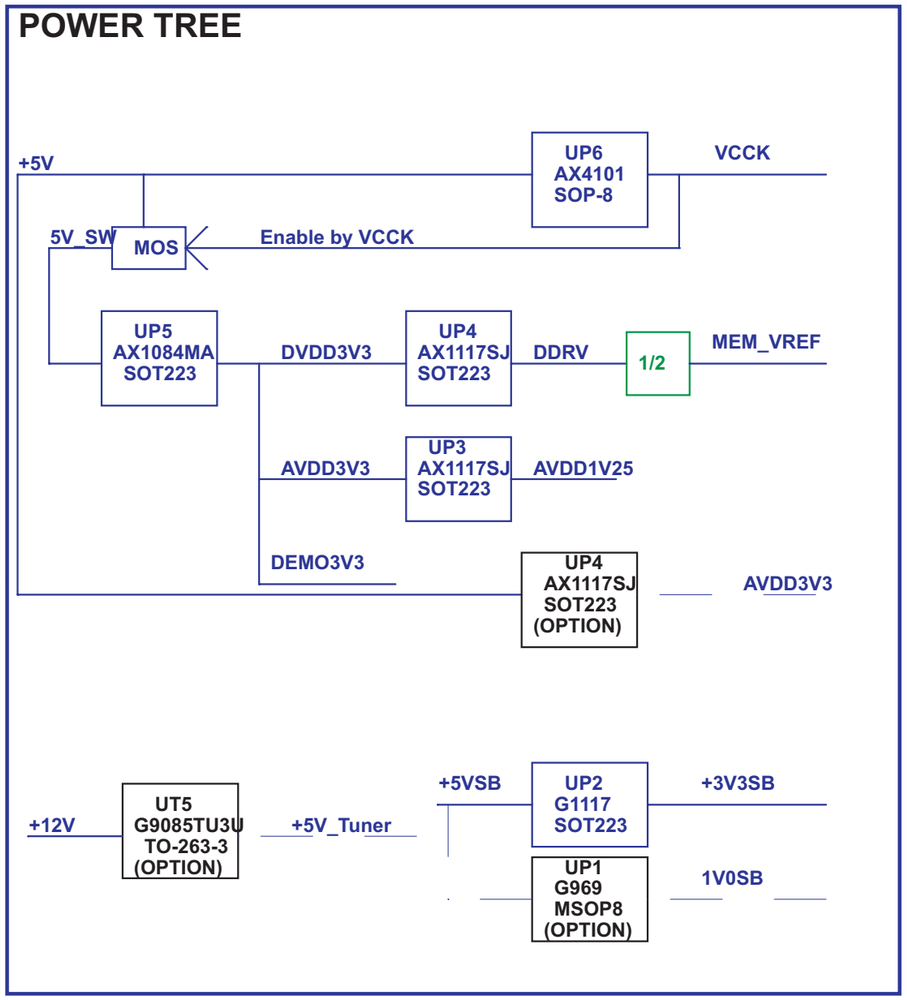
VCCK and Digital I/O Bypass





HW Strap Setting

POWER TREE

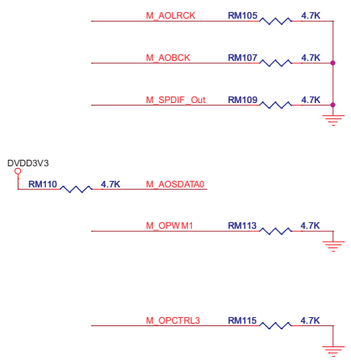


MT5363 STRAPPING MODE

Strapping Mode	AOLRCK	AOBCK	ASPDIF
ICE Mode + Serial Boot	0	0	0
ICE mode + ROM Boot	0	0	1

Strapping Mode	AOSDATA0	OPWM1
XTAL 54MHz	1	0

Strapping Mode	OPCTRL3(O)
PDWNC Normal	0



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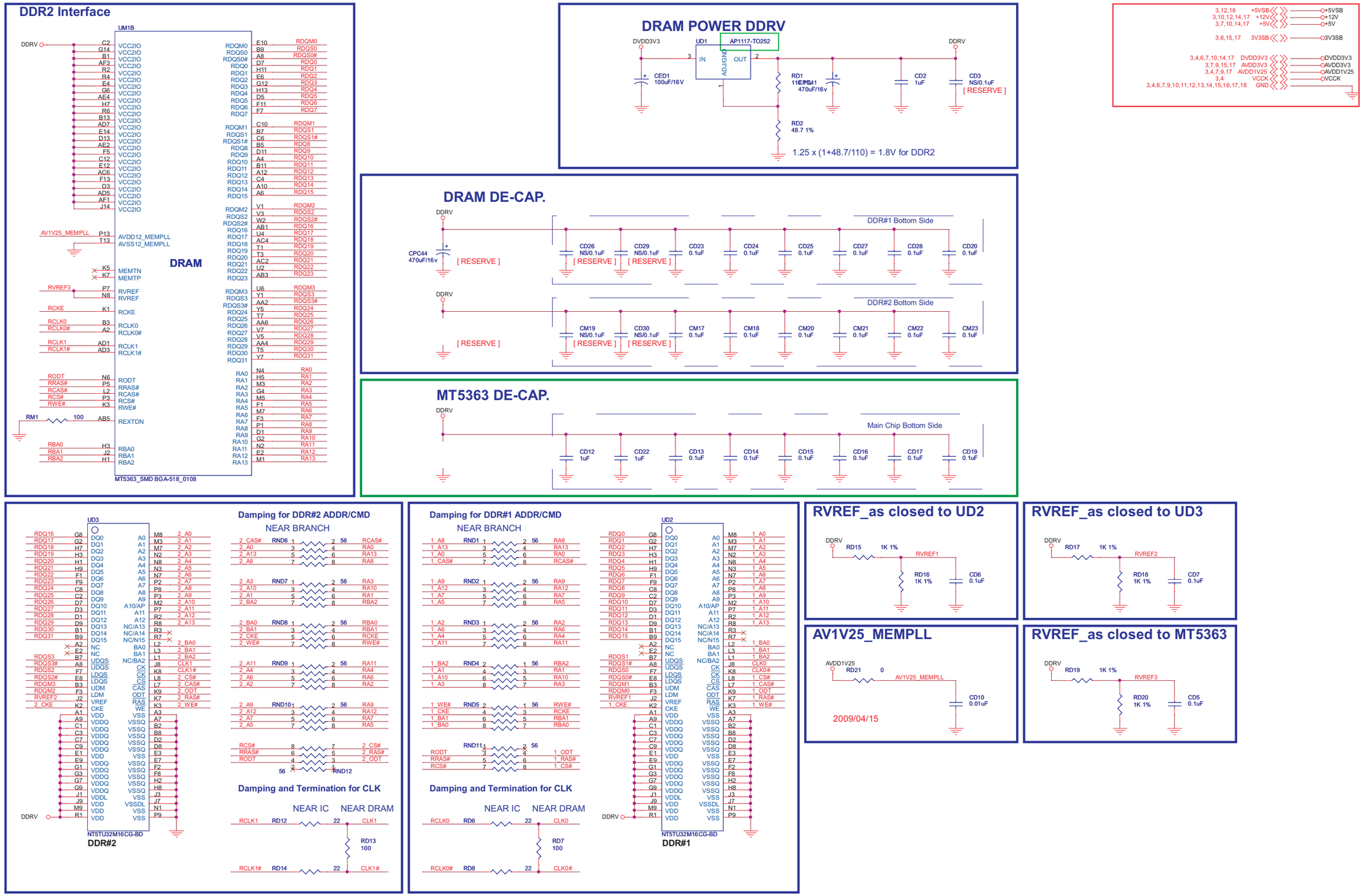
BUSTER



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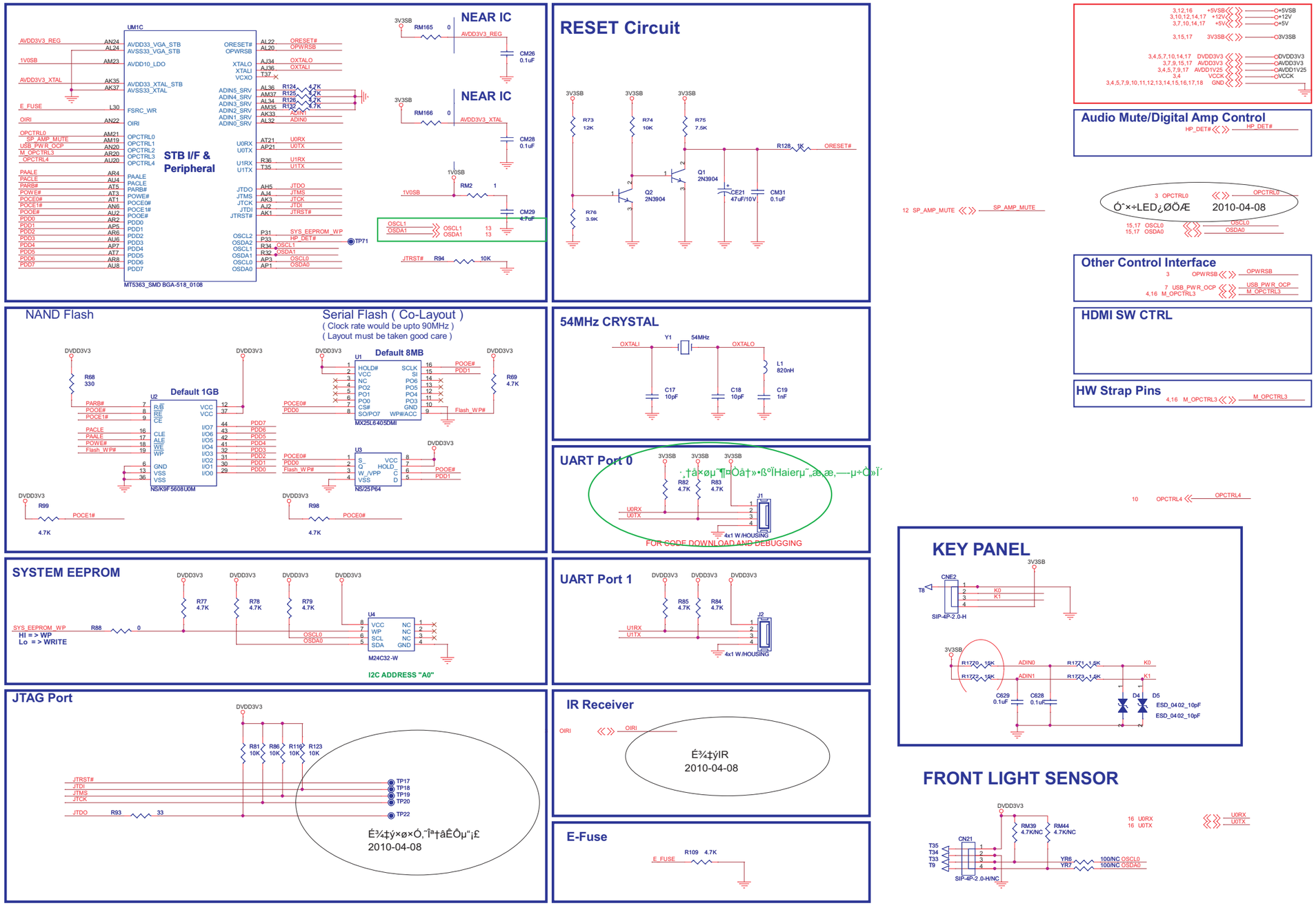
BUSTER



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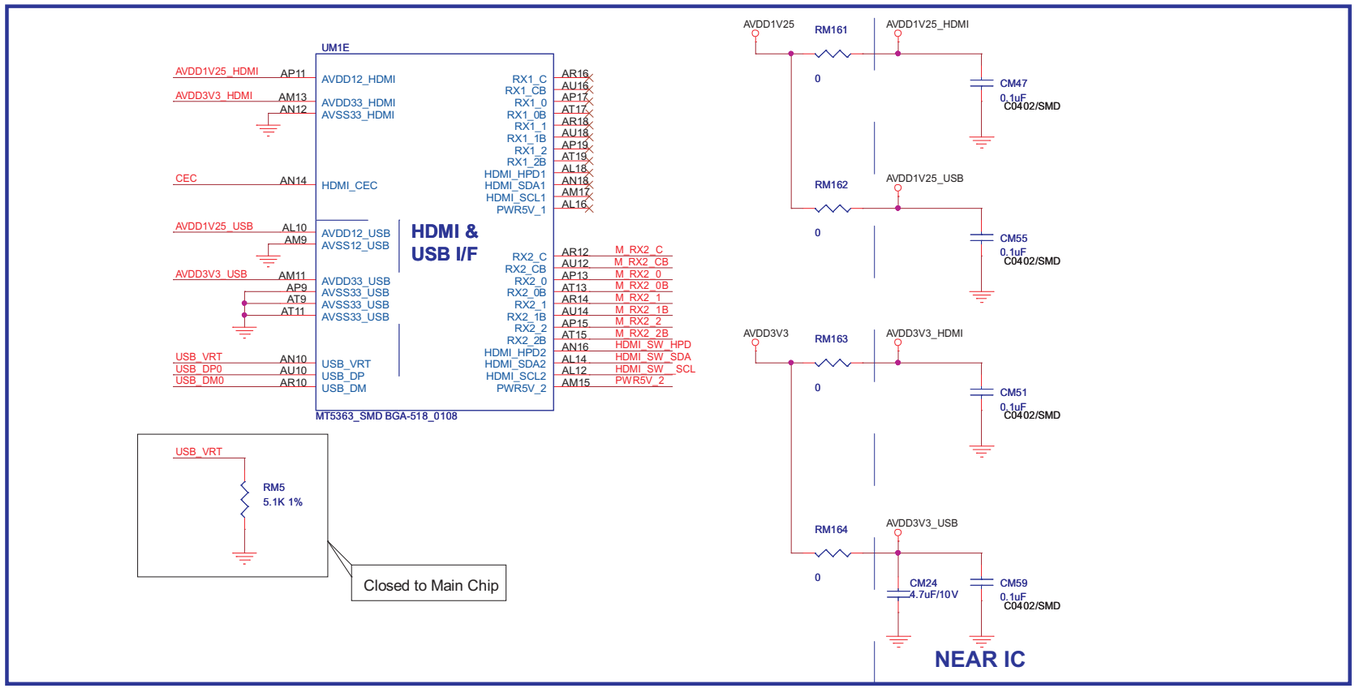
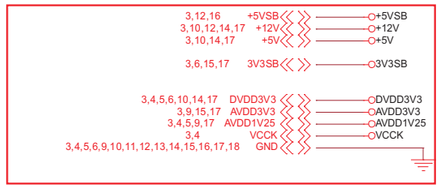
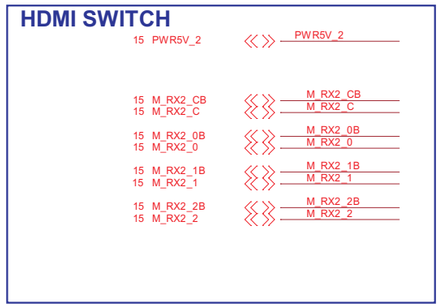


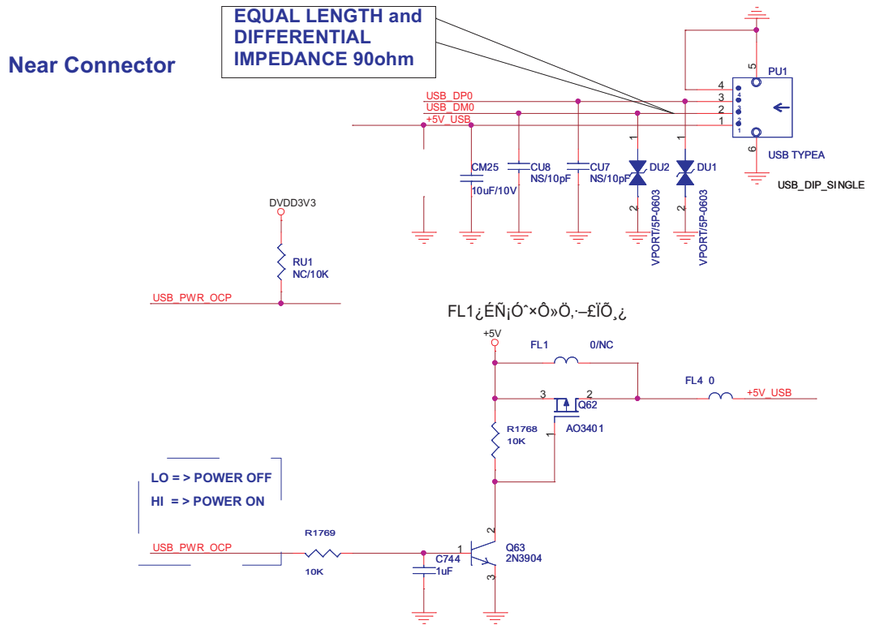


Other Control Interface

HDMI SWITCH



Near Connector



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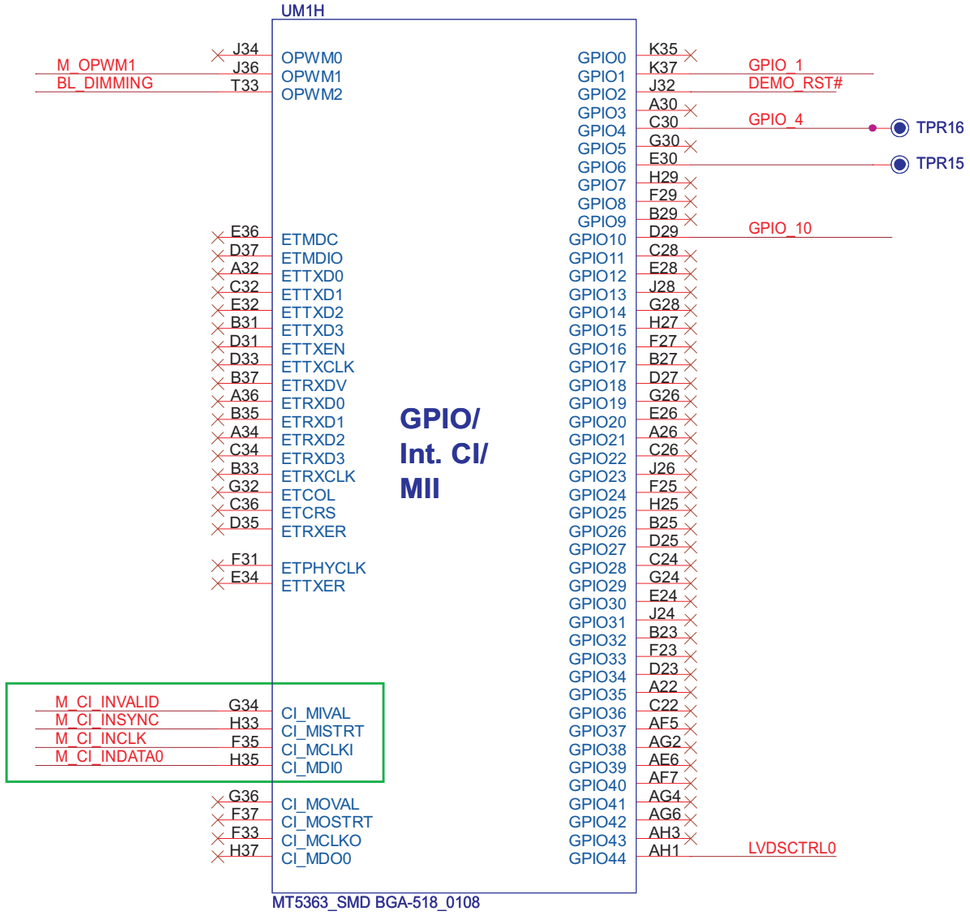
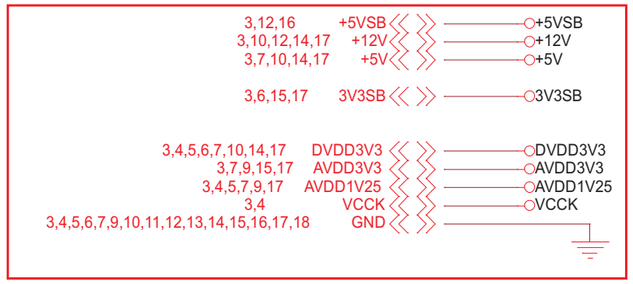
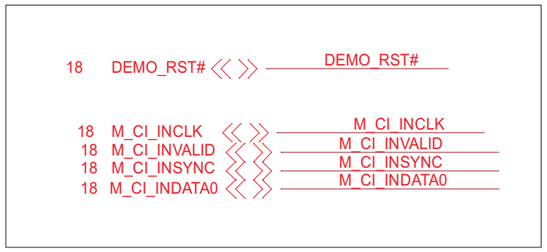


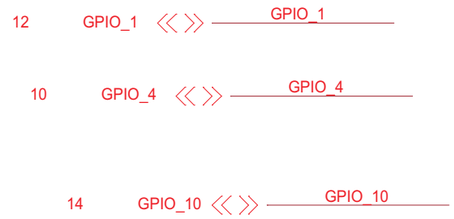


LVDS Control Interface

For CID Test Only

HW Strapping





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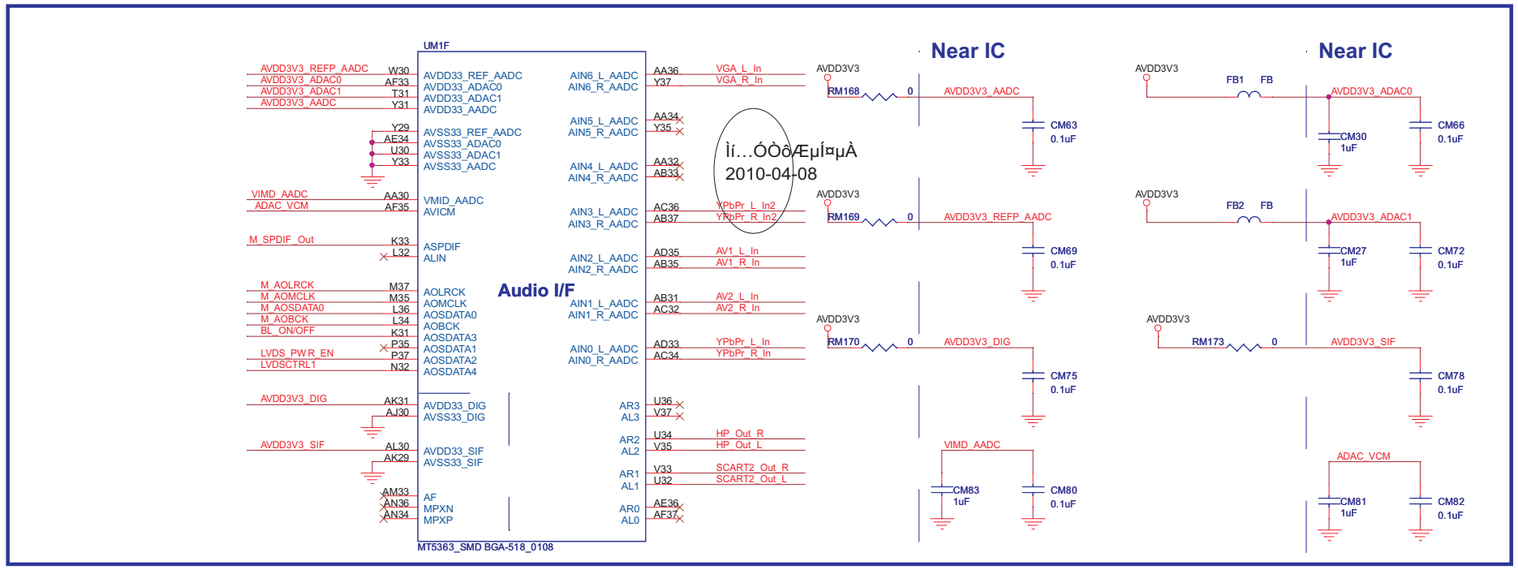
PCI principal HBTV-32L02HD / HBVT-42L02FD					Código sistema

BUSTER



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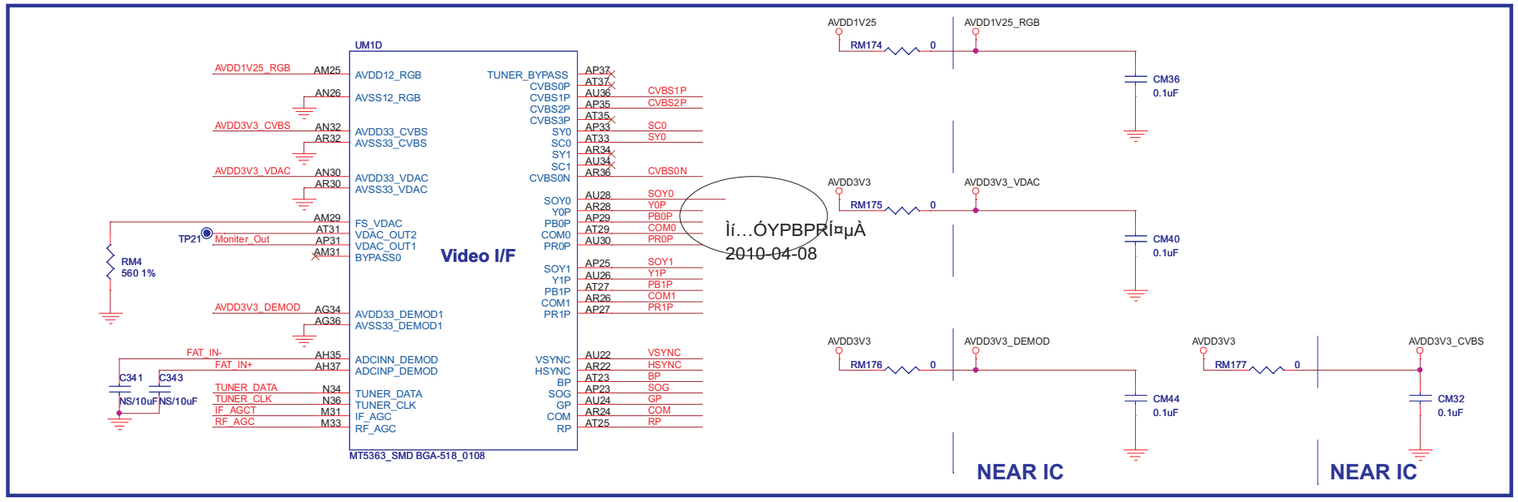
2010-04-08



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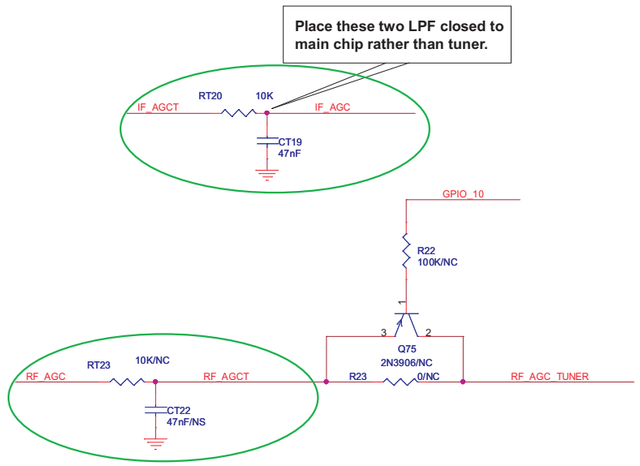
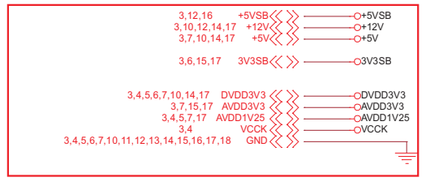
2010-04-08



14 GPIO_10 — GPIO_10

4,8 M_AOSDATA0 — M_AOSDATA0
4,8 M_AOLRCK — M_AOLRCK
4,8 M_AOBCK — M_AOBCK
4,8 M_AOMCLK — M_AOMCLK

14 RF_AGC_TUNER — RF_AGC_TUNER



Audio Input

16 VGA_L_In — VGA_L_In
16 VGA_R_In — VGA_R_In

11 YPbPr_L_In2 — YPbPr_L_In2
11 YPbPr_R_In2 — YPbPr_R_In2
11 AV1_L_In — AV1_L_In
11 AV1_R_In — AV1_R_In
11 AV2_L_In — AV2_L_In
11 AV2_R_In — AV2_R_In
11 YPbPr_L_In — YPbPr_L_In
11 YPbPr_R_In — YPbPr_R_In

Audio Output

10 SCART2_Out_R — SCART2_Out_R
10 SCART2_Out_L — SCART2_Out_L
10 HP_Out_R — HP_Out_R
10 HP_Out_L — HP_Out_L

Video Input

11 CVBS1P — CVBS1P
11 CVBS2P — CVBS2P

11 SC0 — SC0
11 SY0 — SY0

11,14 CVBS0N — CVBS0N
11 SOY0 — SOY0
11 Y0P — Y0P
11 PB0P — PB0P
11 COM0 — COM0
11 PR0P — PR0P
11 SOY1 — SOY1
11 Y1P — Y1P
11 PB1P — PB1P
11 COM1 — COM1
11 PR1P — PR1P
16 VSYNC — VSYNC
16 HSYNC — HSYNC
16 BP — BP
16 SOG — SOG
16 GP — GP
16 COM — COM
16 RP — RP

Video Output

13 Moniter_Out — Moniter_Out

Tuner I/O Interface

14 FAT_IN- — FAT_IN-
14 FAT_IN+ — FAT_IN+
14,18 TUNER_DATA — TUNER_DATA
14,18 TUNER_CLK — TUNER_CLK
14,18 IF_AGC — IF_AGC

LVDS Control Interface

17 BL_ON/OFF — BL_ON/OFF
17 LVDS_PWR_EN — LVDS_PWR_EN
17 LVDSCTRL1 — LVDSCTRL1

Audio Mute Control

SPDIF

4,10 M_SPDIF_Out — M_SPDIF_Out

HW Strap Setting

4 M_AOLRCK — M_AOLRCK
4 M_AOBCK — M_AOBCK
4 M_AOSDATA0 — M_AOSDATA0
4,10 M_SPDIF_Out — M_SPDIF_Out

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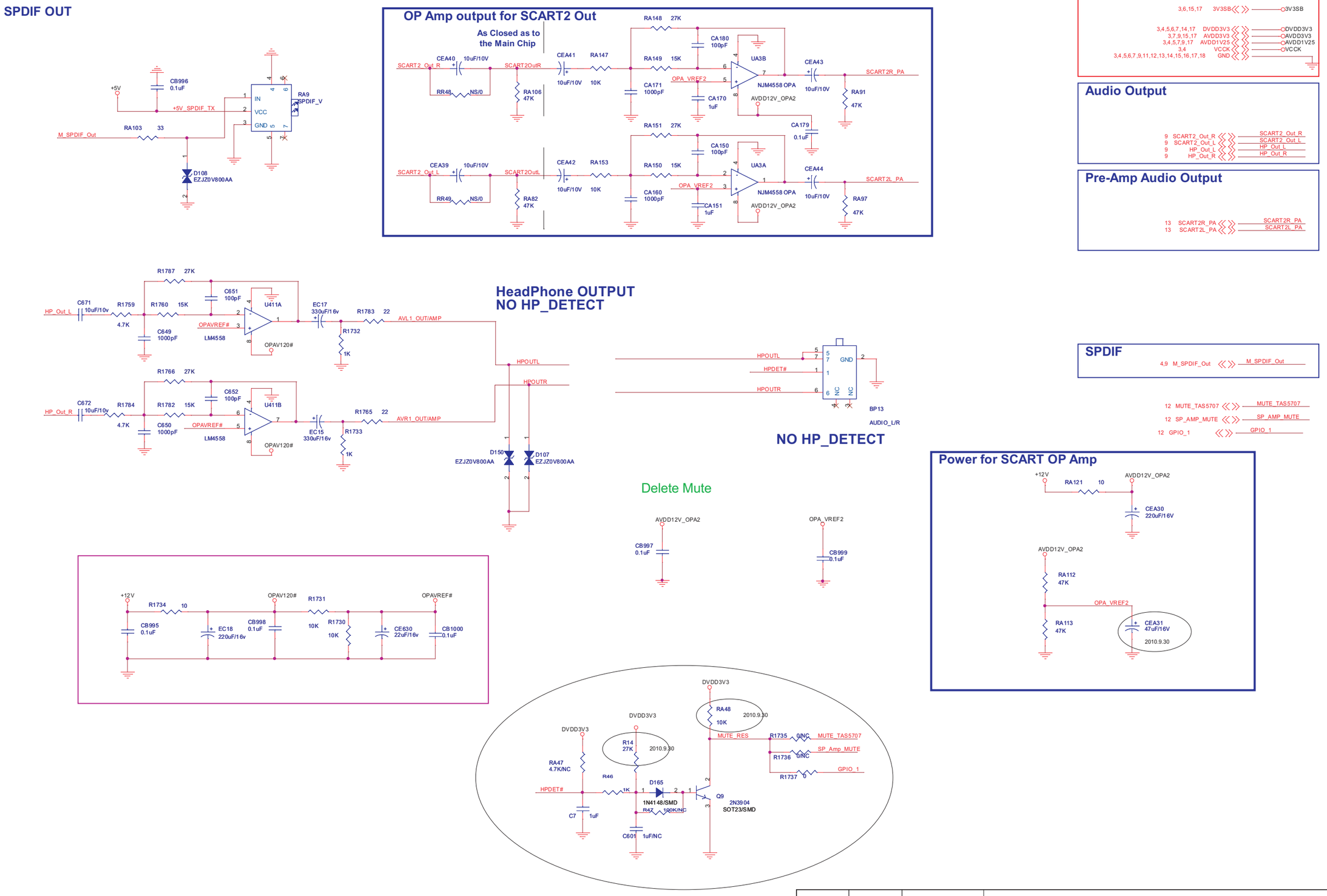

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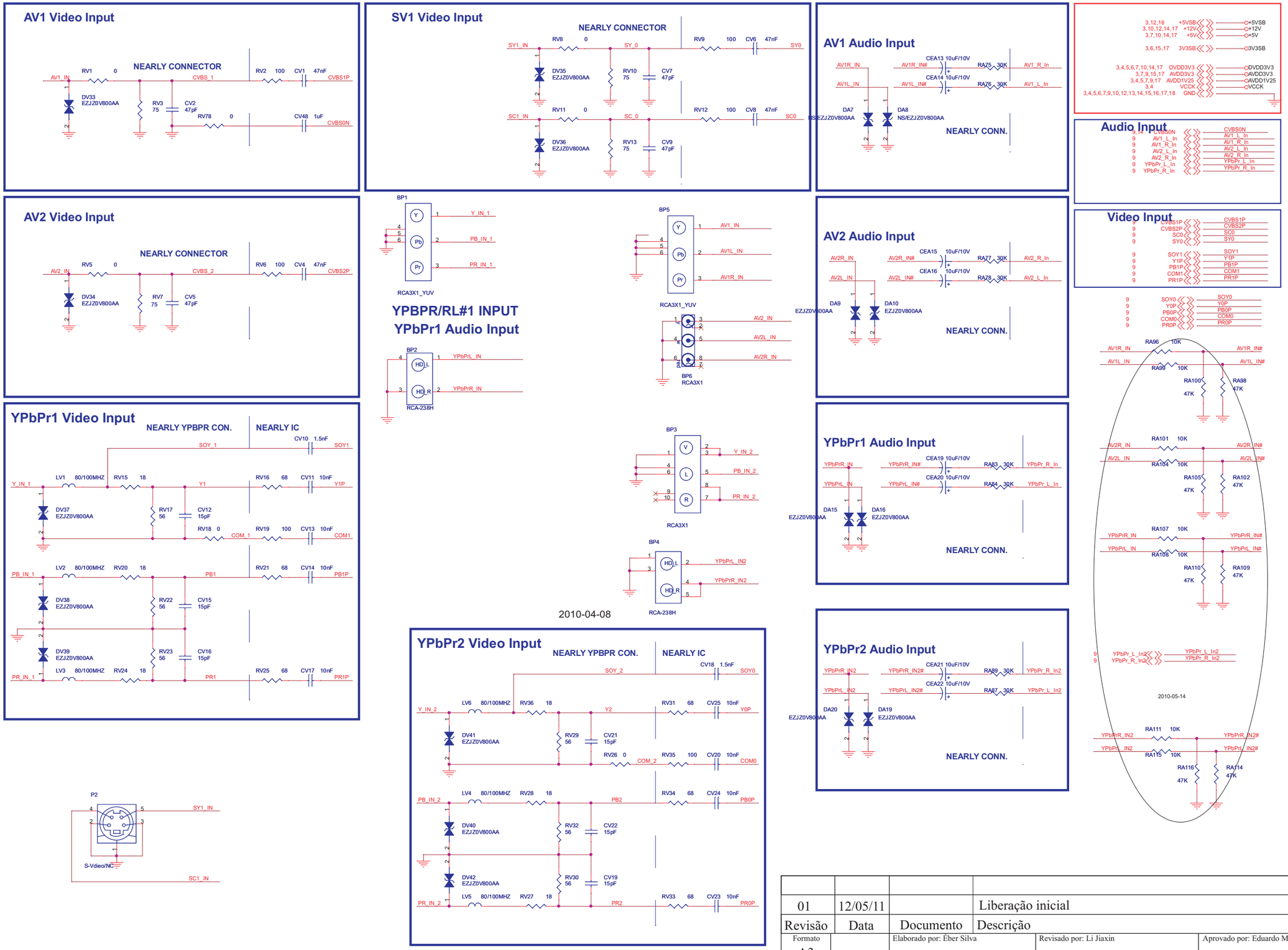
BUSTER®



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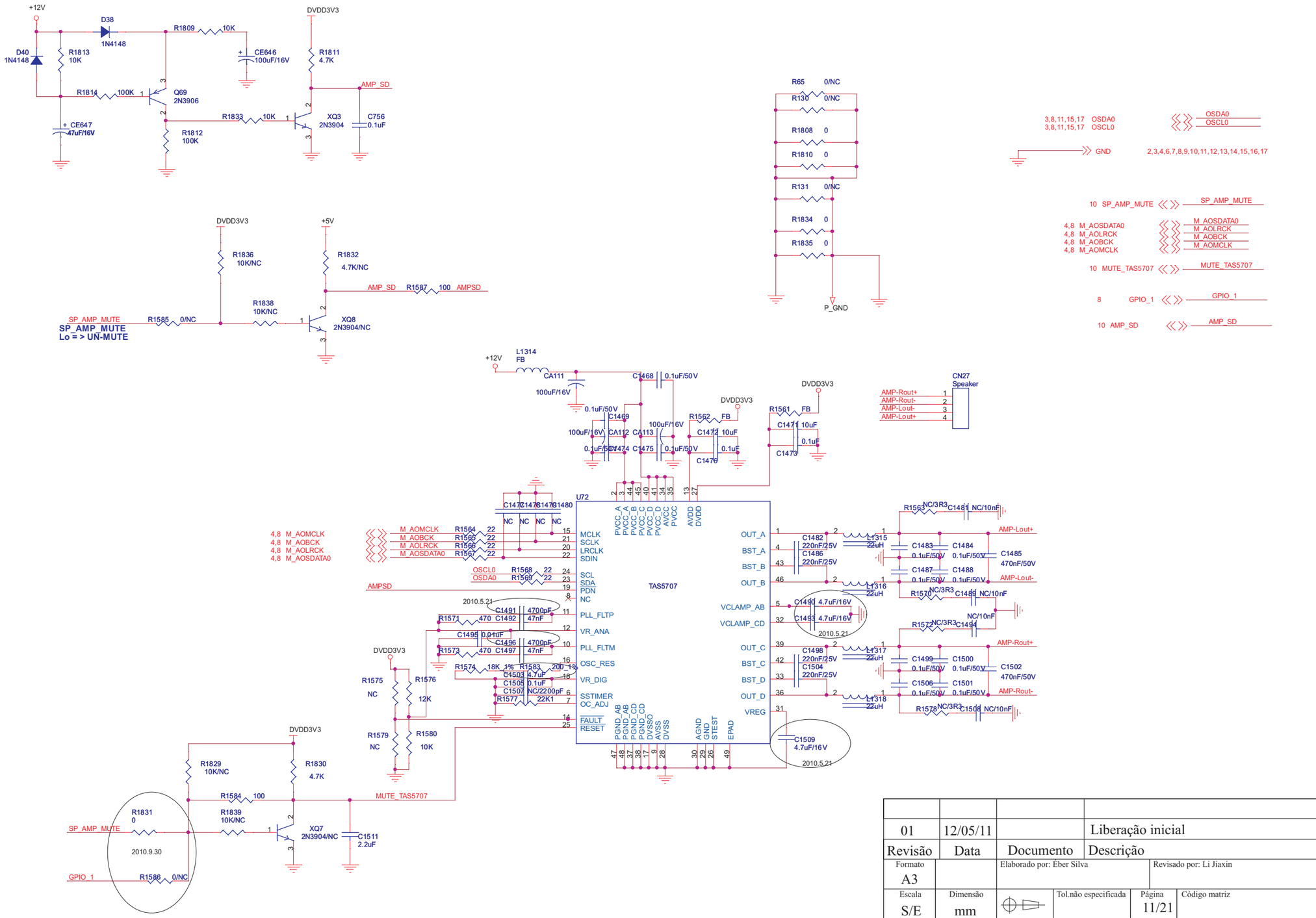
MUTE Circuit



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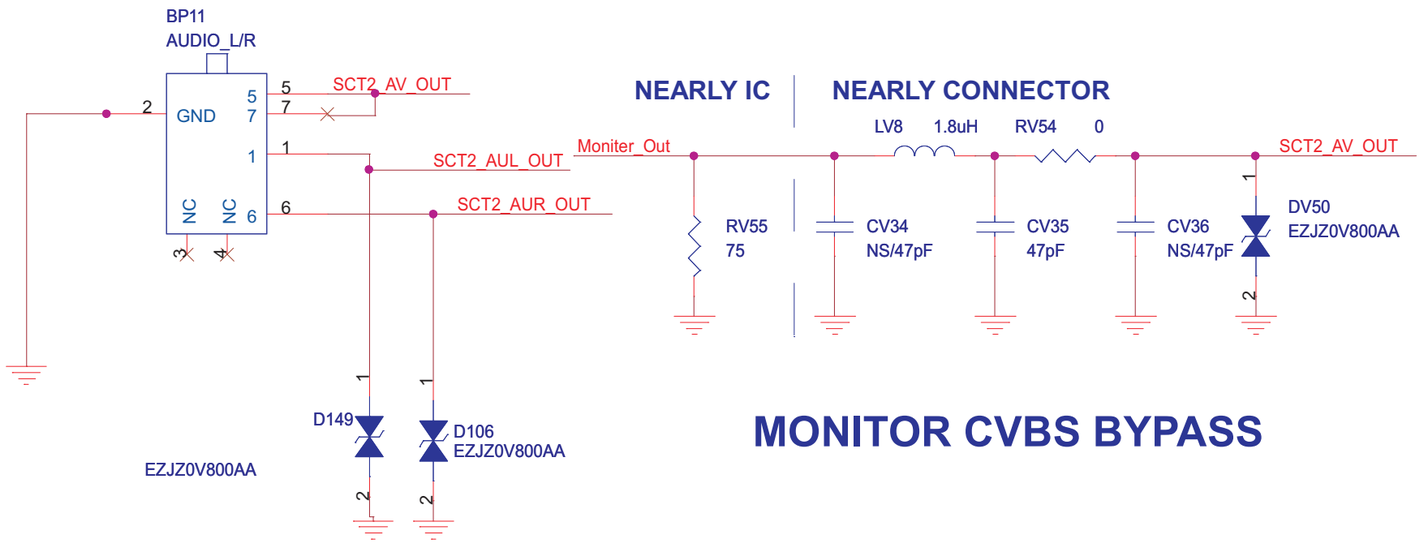
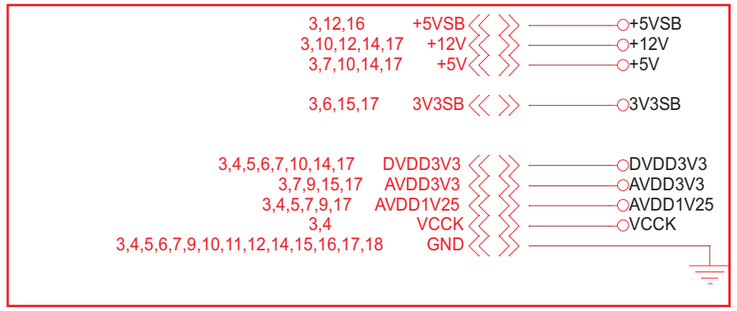
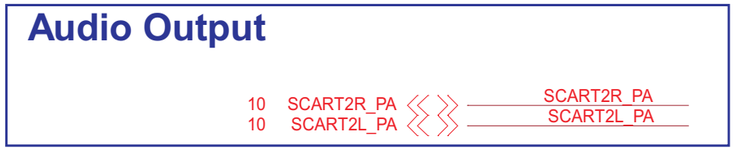
BUSTER



MONITOR CVBS BYPASS



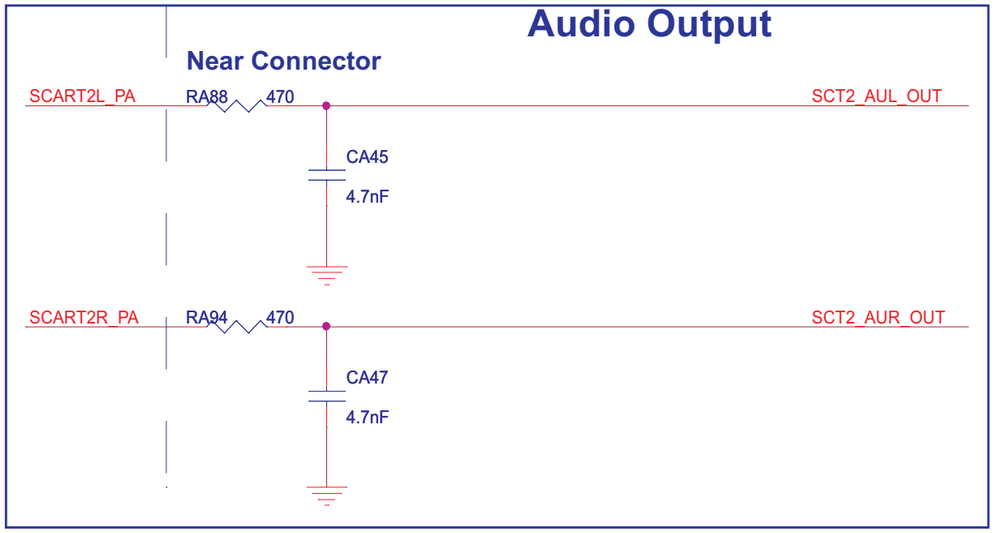
Audio Output



Video Output

Audio Mute Control

Audio Output



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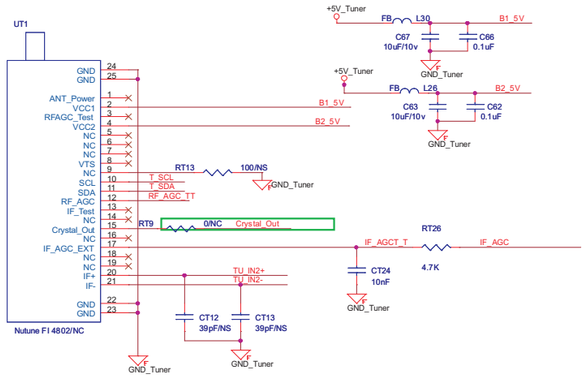
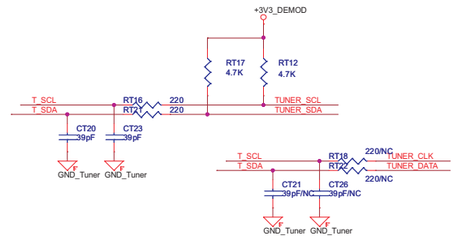
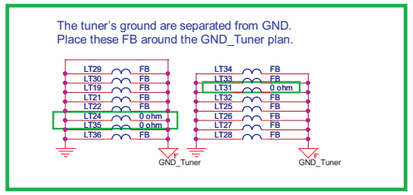
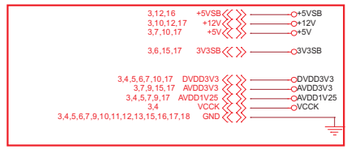
BUSTER®





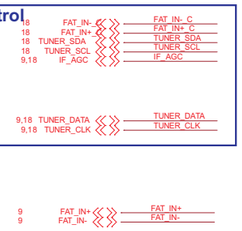




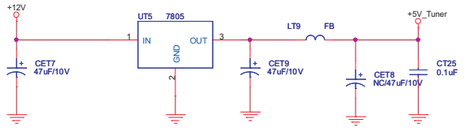
Audio Input

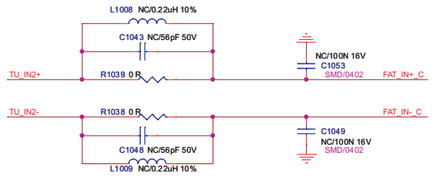
Video Input

Tuner Control



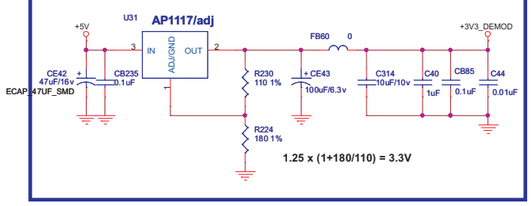
TUNER POWER +5V_TUNER



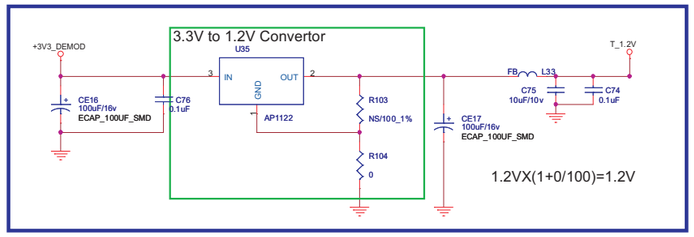


Close to ISDB-T Demod

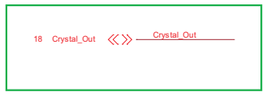
DEMOD POWER

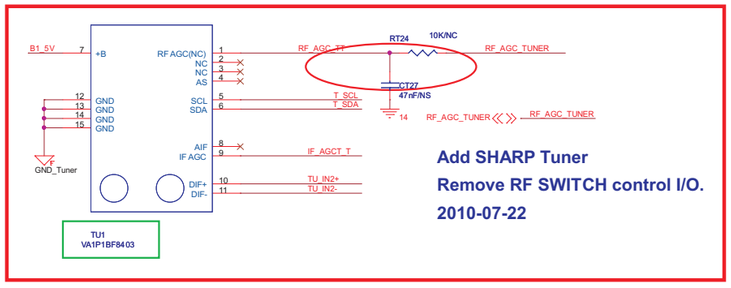


1.25 x (1+180/110) = 3.3V

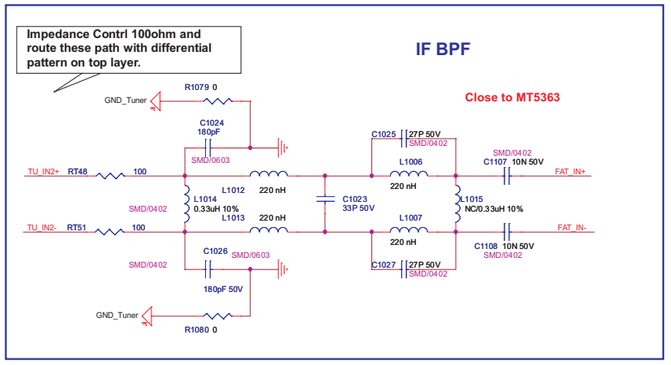


1.2VX(1+0/100)=1.2V





Add SHARP Tuner
Remove RF SWITCH control I/O.
2010-07-22



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PCI principal HBTV-32L02HD / HBVT-42L02FD					Código sistema

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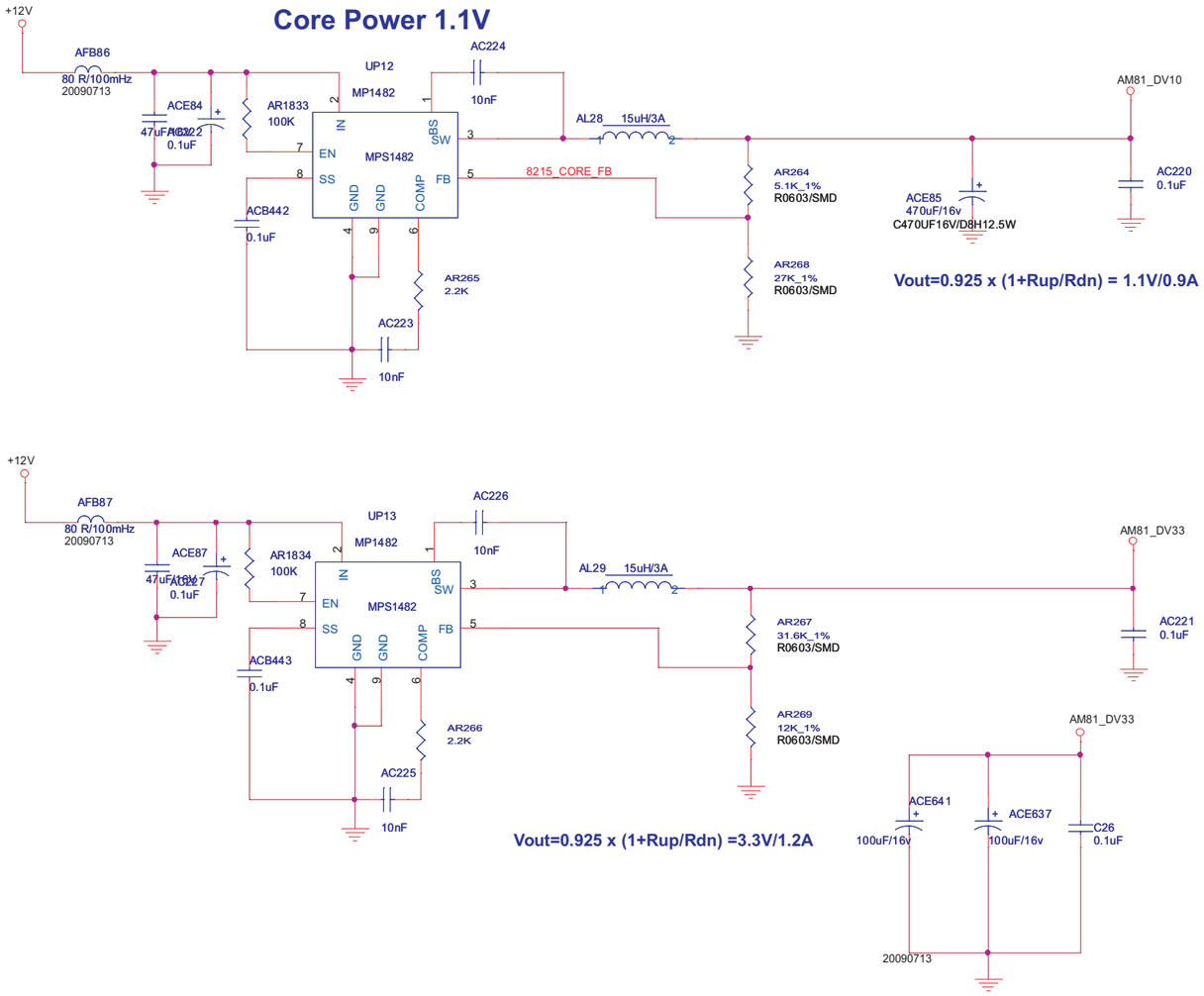

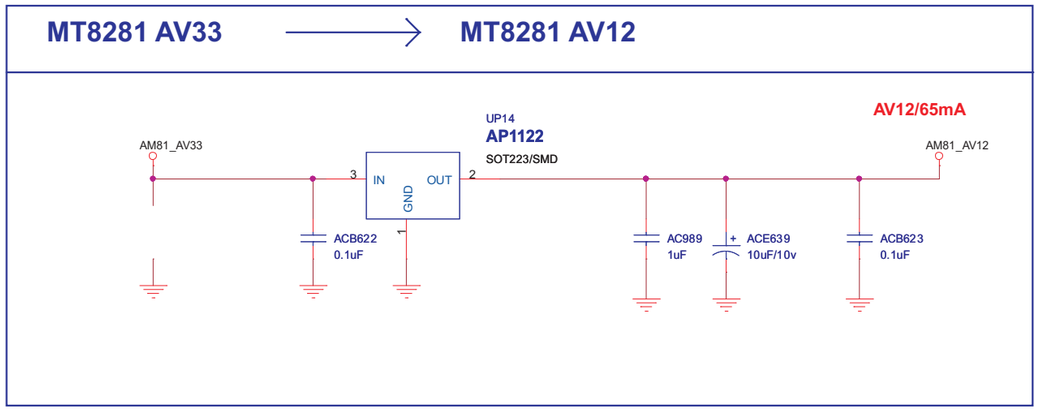

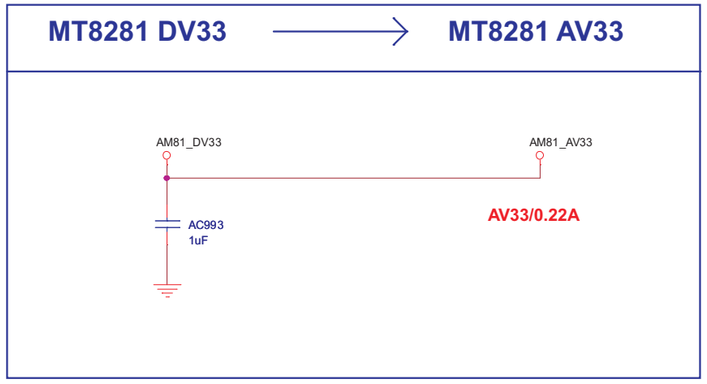

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PCI principal HBTV-32L02HD / HBVT-42L02FD					Código sistema

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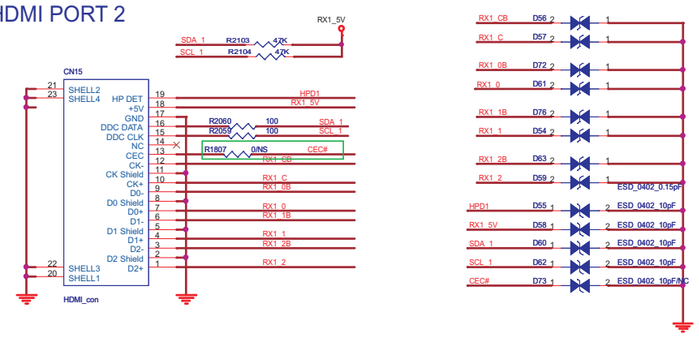
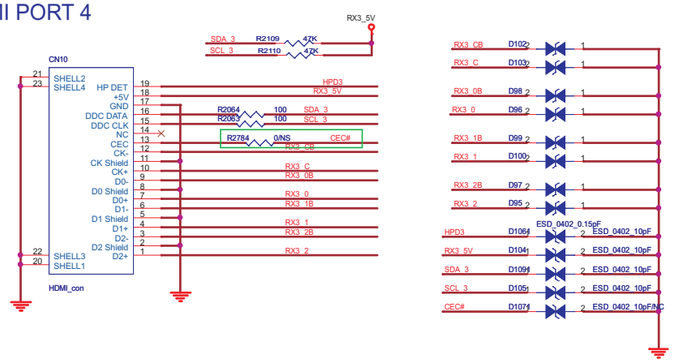
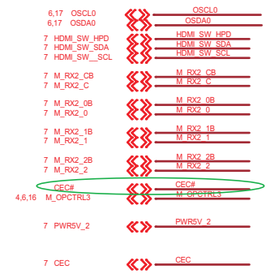
HDMI PORT 2

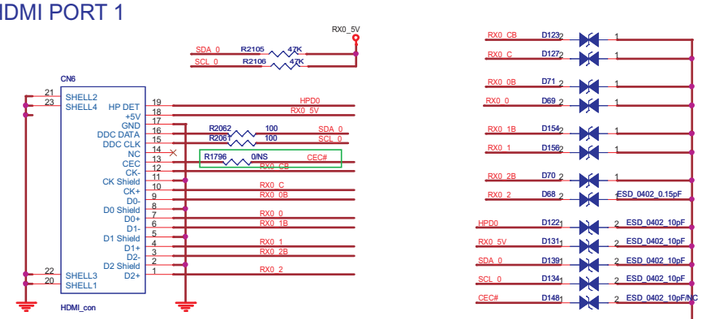


HDMI PORT 4



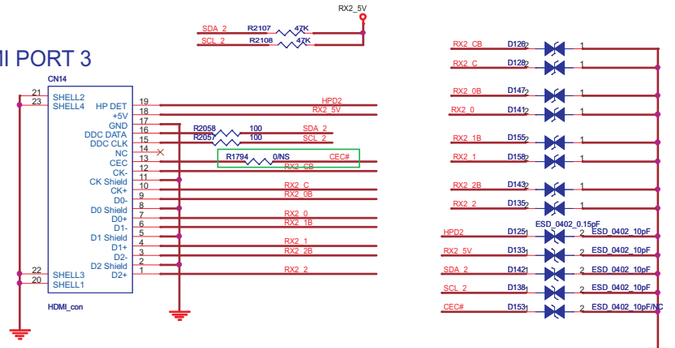


HDMI PORT 1

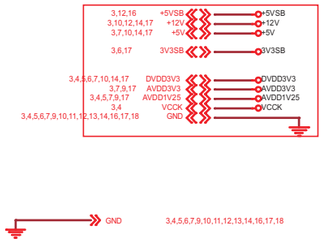


HORIZONTAL MOUNT

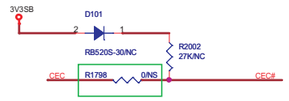
HDMI PORT 3

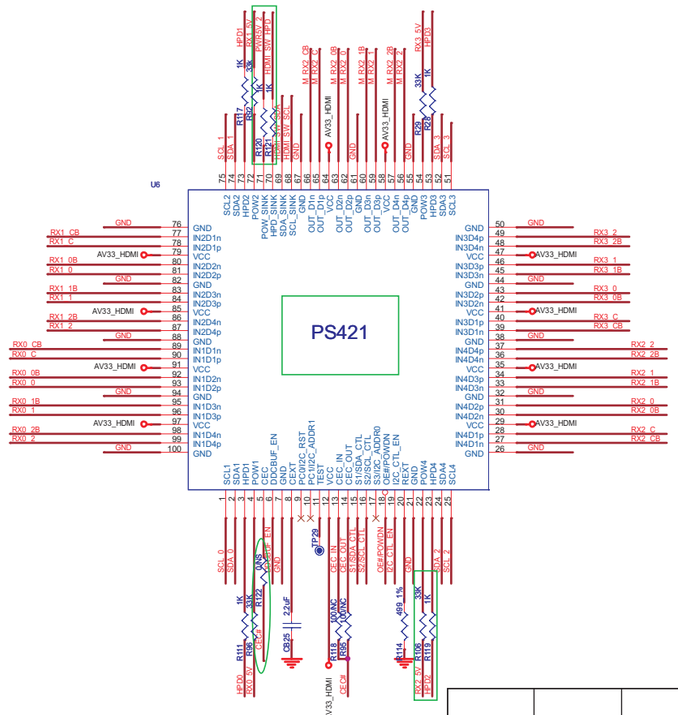


HORIZONTAL MOUNT

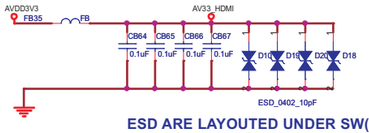


HDMI SWITCH



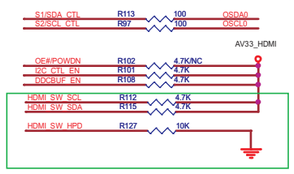


NEARLY SW IC



ESD ARE LAYOUTED UNDER SW(Square).

Pulled up to 3.3V on CPU side.
I2C CONTROL ADDRESS:0x9C/9D
EDID SHADOW ADDRESS:0x9E/9F



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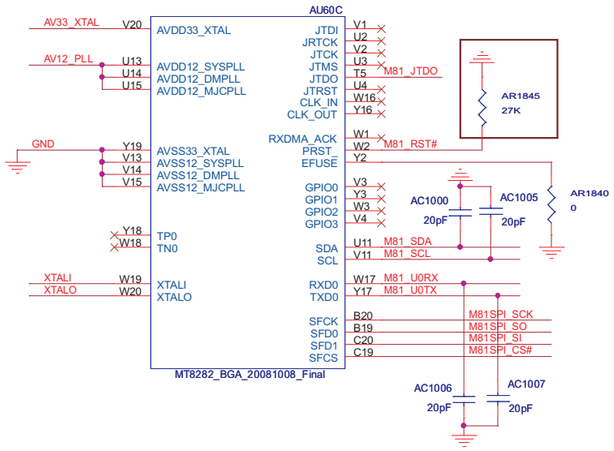
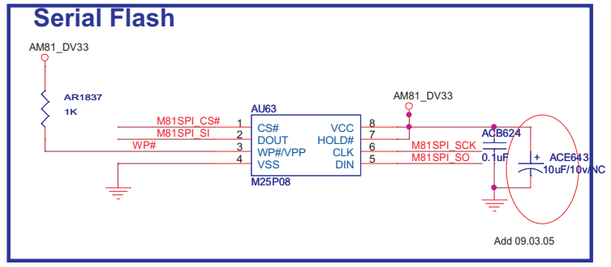
PCI principal HBTV-32L02HD / HBVT-42L02FD				Código sistema	

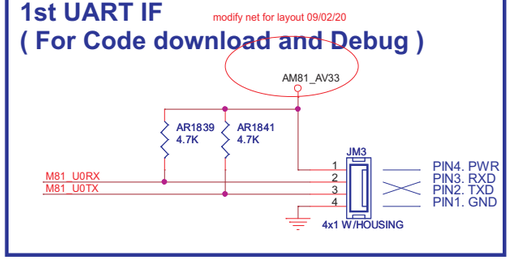
Peripheral components

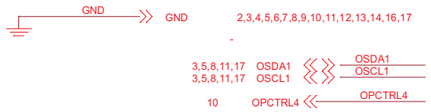


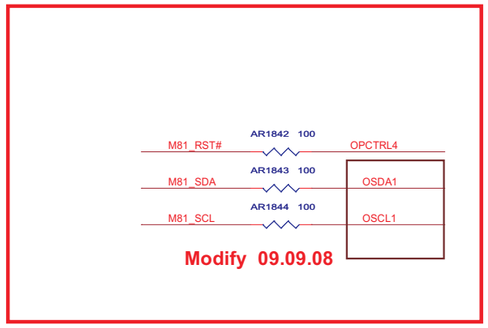
Serial Flash



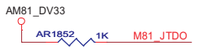
1st UART IF
(For Code download and Debug)



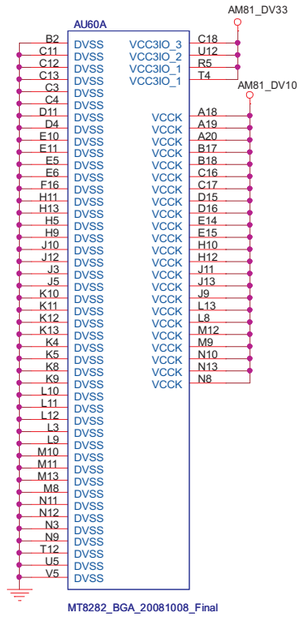




Trapping :
Default Low when no configuration external



Core Powe 1.0V
IO Power 3.3V

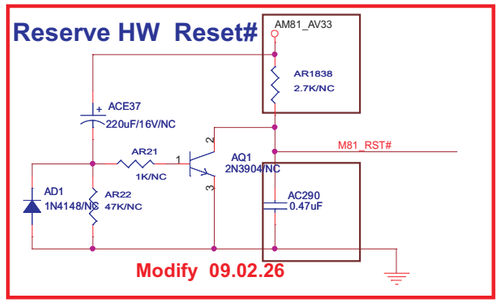


Pad_jtdo	Description
0	pad_jtdo tie 0 => dram boot
1	pad_jtdo tie 1 => flash boot

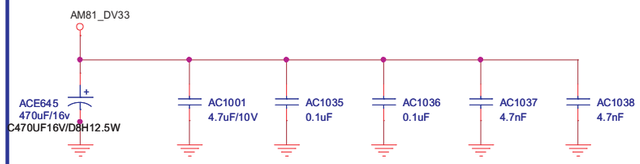
Crystal

Modify for accuracy

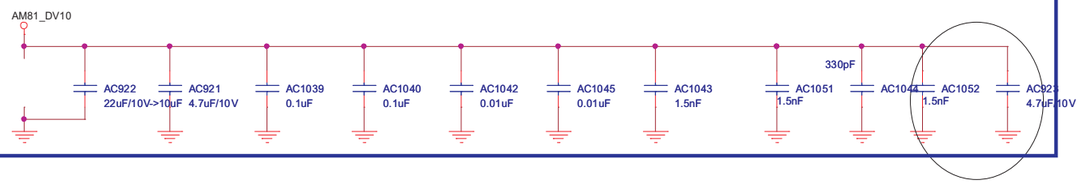
Reserve HW Reset#



DV33 IO POWER

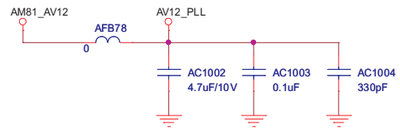


DV10 CORE POWER



AV33 XTAL POWER

AV12 PLL POWER



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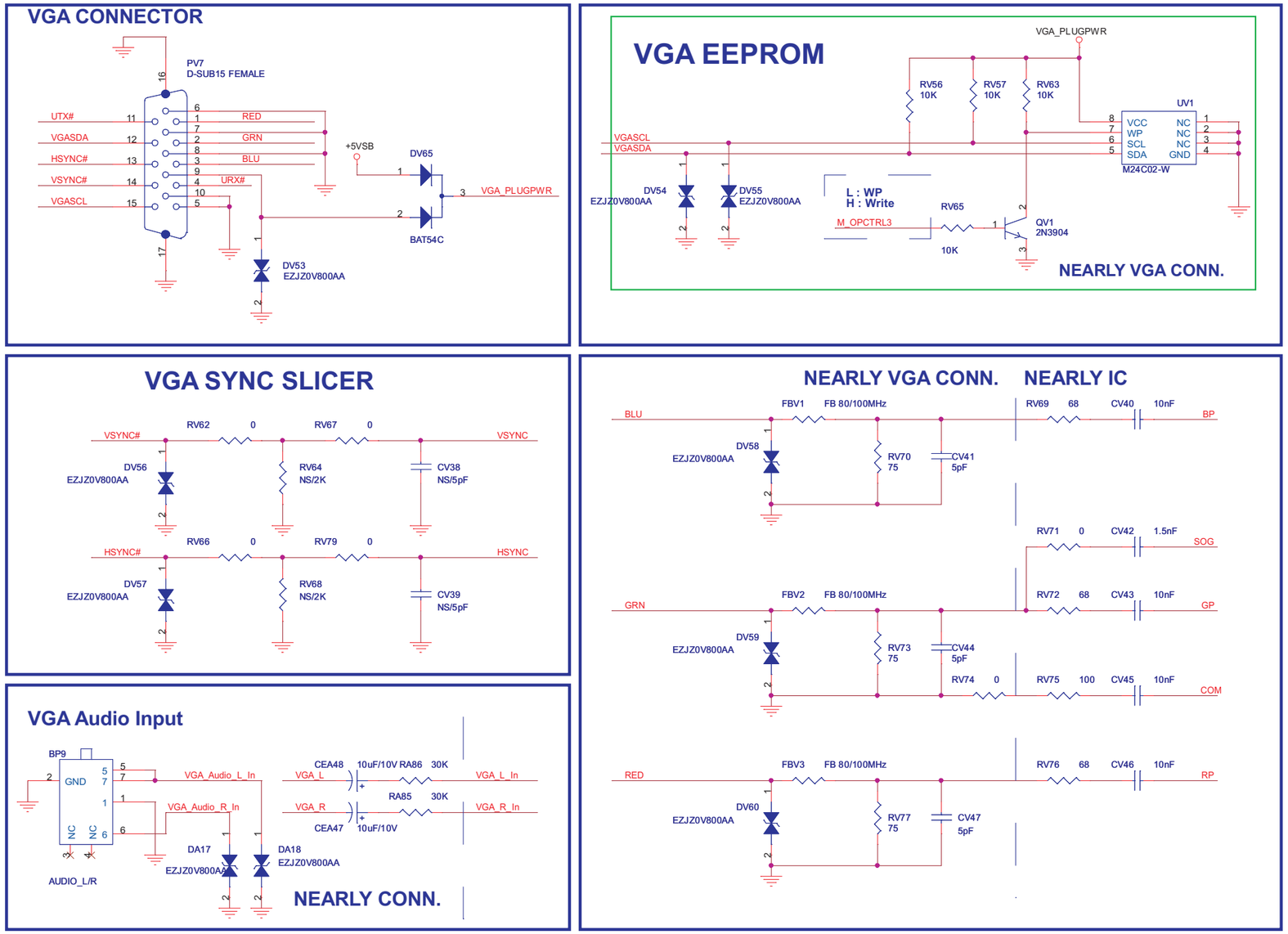

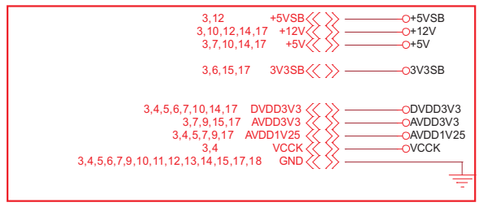

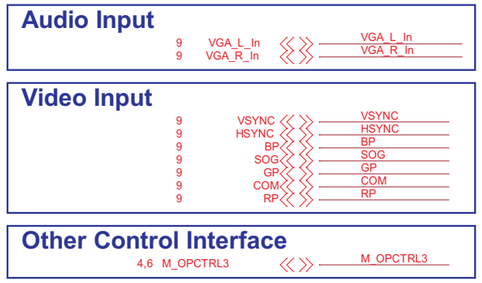

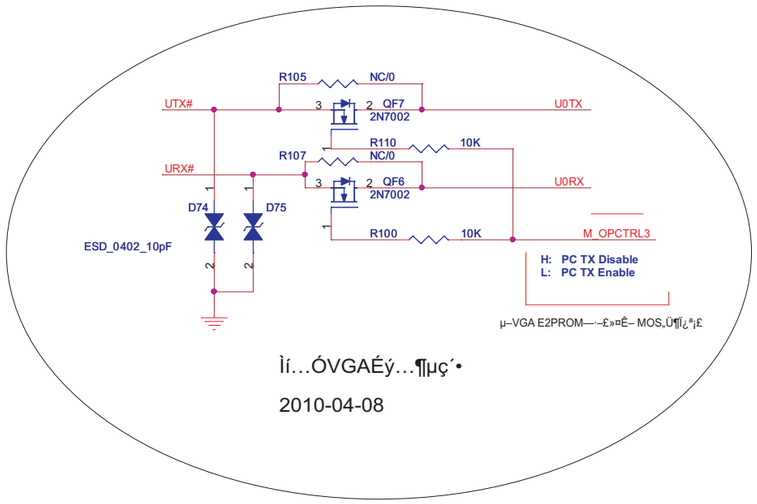

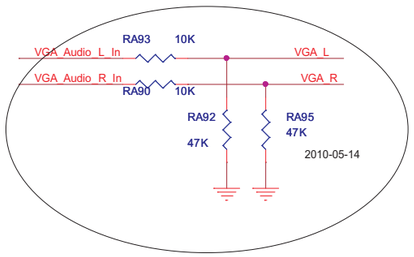

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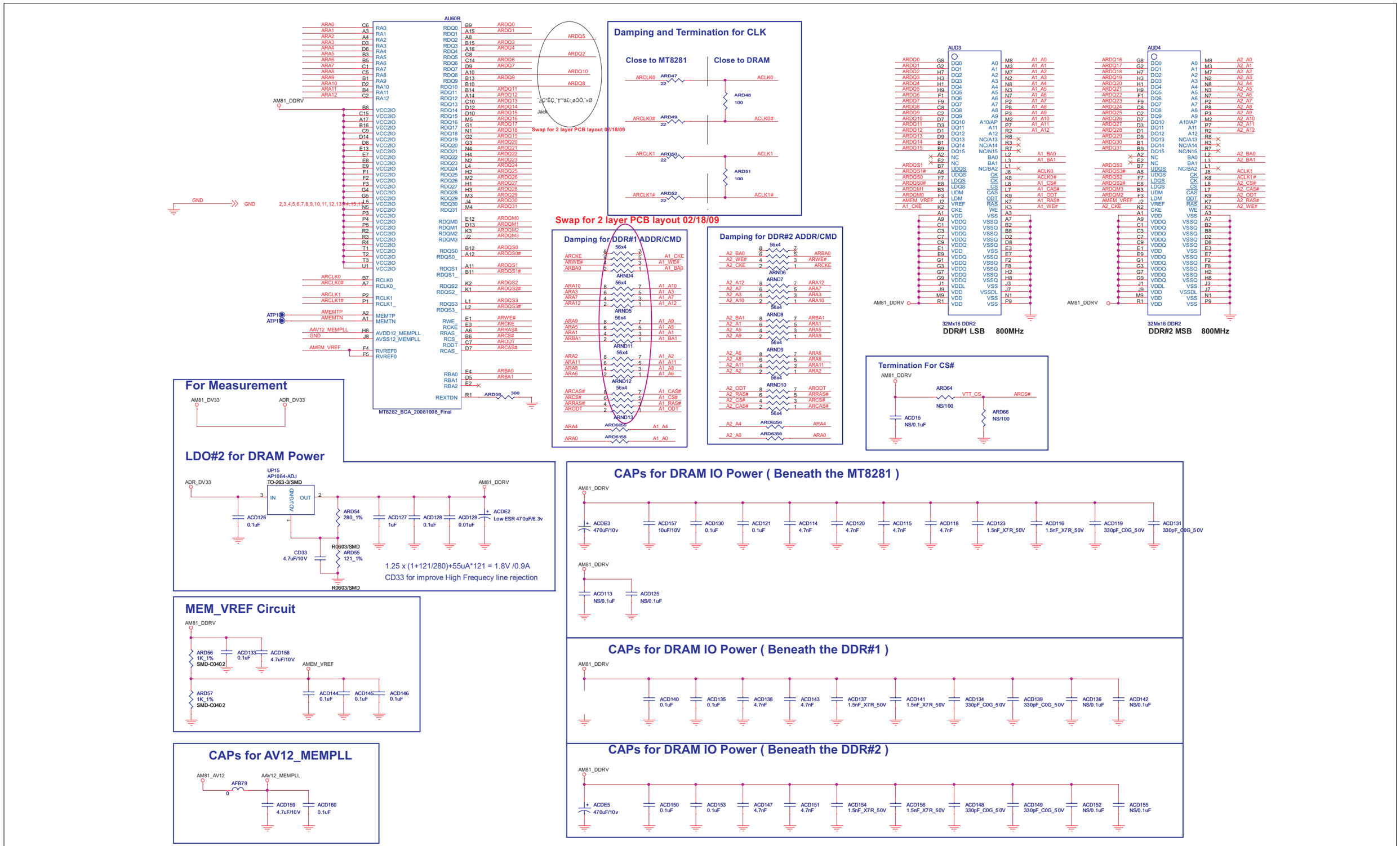

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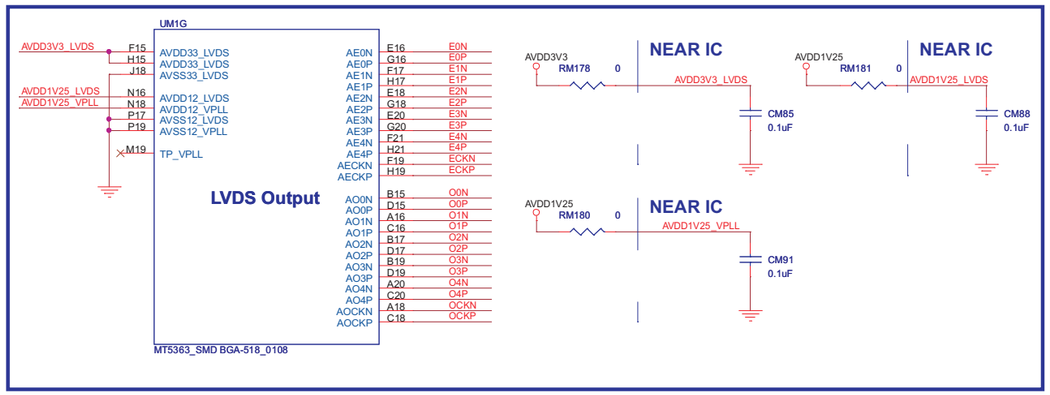
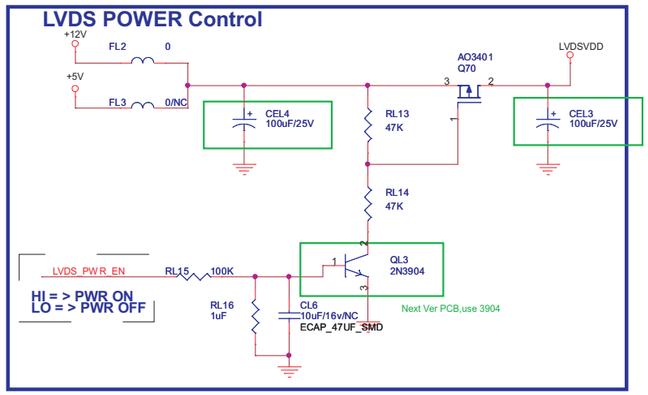
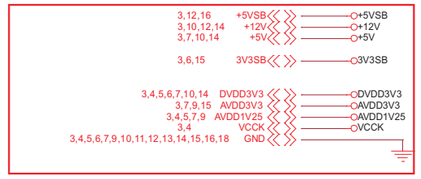
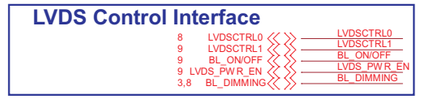
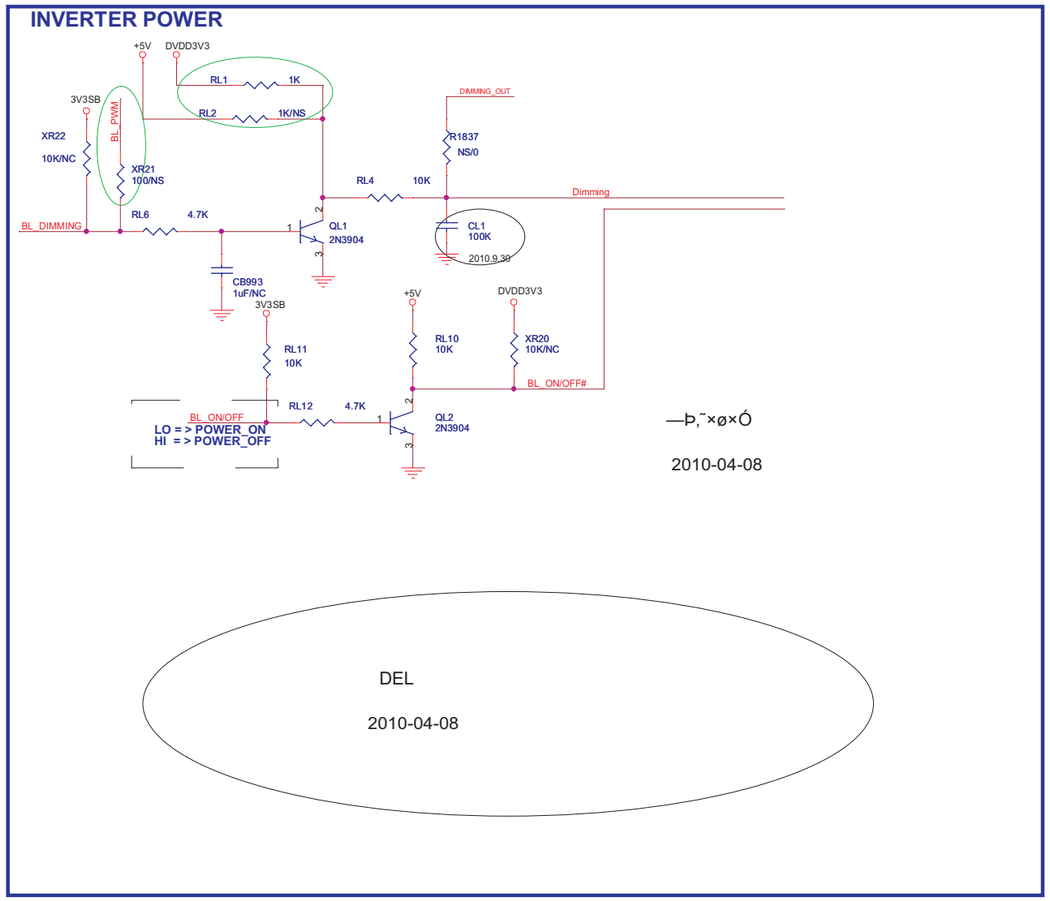
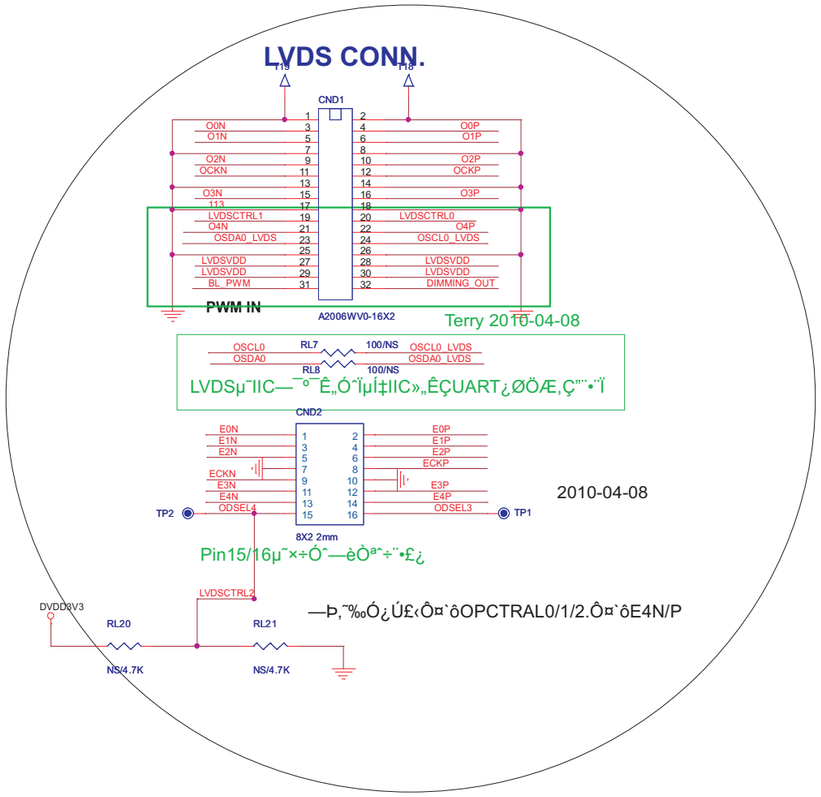


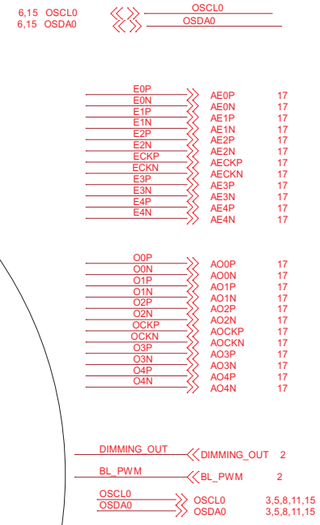






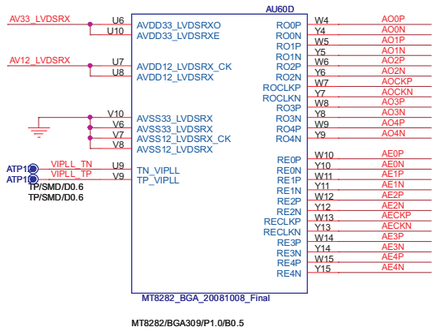


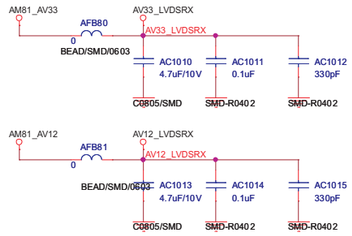


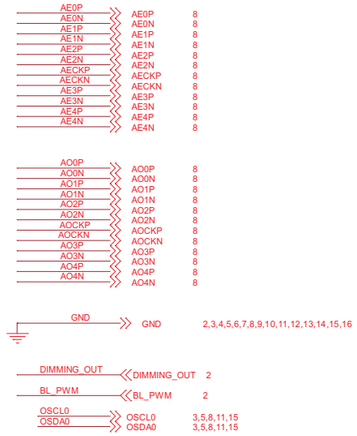


01	12/05/11		Liberação inicial		
Revisão	Data	Documento	Descrição		
Formato A3		Elaborado por: Éber Silva	Revisado por: Li Jiaxin	Aprovado por: Eduardo Macedo	Modificado por:
Escala S/E	Dimensão mm	Tol.não especificada	Página 19/21	Código matriz	
PCI principal HBTV-32L02HD / HBVT-42L02FD				Código sistema	BUSTER

LVDS RX

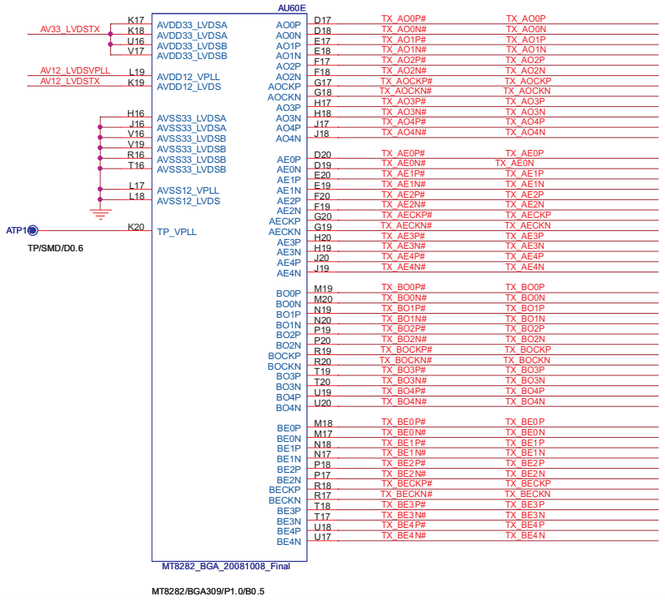


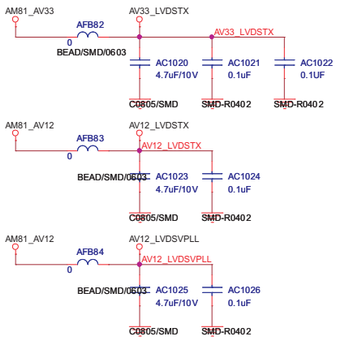




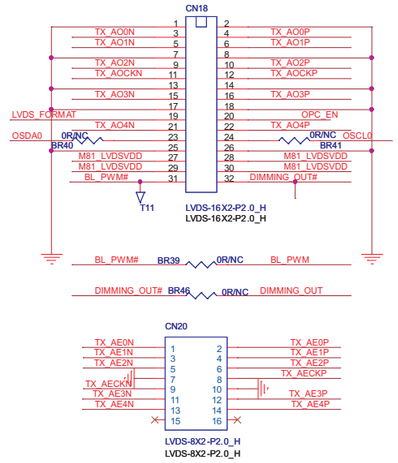
LVDS TX

Close to 8215
Pls. swap Pin for LAYOUT



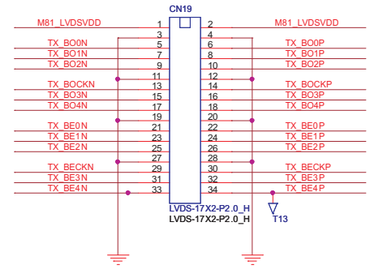


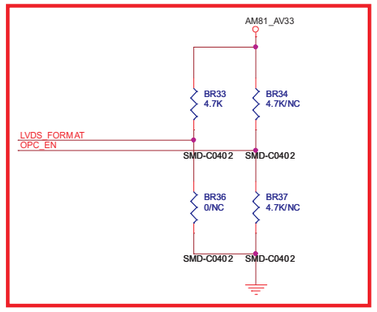
LVDS PORT A(HORIZONTAL)



LVDS PORT B(HORIZONTAL)

For 1080P 120Hz





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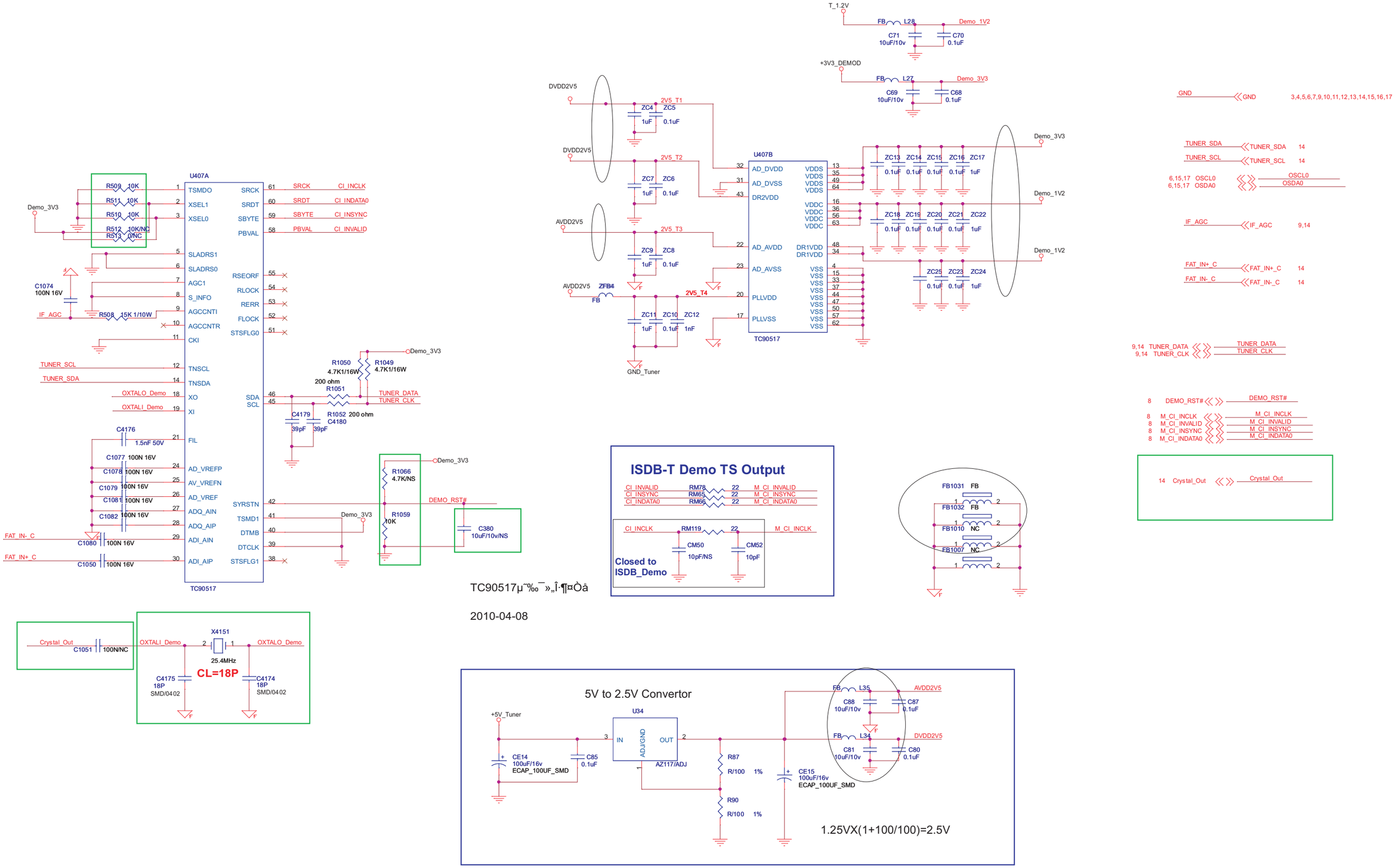
Escala S/E	Dimensão mm		Tol.não especificada	Página 20/21	Código matriz
PCI principal HBTV-32L02HD / HBVT-42L02FD					Código sistema

BUSTER



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2010-04-08

01	12/05/11		Liberação inicial		
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Formato A3		Elaborado por: Éber Silva	Revisado por: Li Jiaxin	Aprovado por: Eduardo Macedo	Modificado por:
Escala S/E	Dimensão mm	Tol.não especificada	Página 21/21	Código matriz	BUSTER
PCI principal HBTV-32L02HD / HBVT-42L02FD				Código sistema	