

ZXMP3F37DN8

30V SO8 Dual P-channel enhancement mode MOSFET

Summary

$V_{(BR)DSS}$ (V)	$R_{DS(on)}$ (Ω)	I_D (A)
-30	0.025 @ $V_{GS} = -10V$	-8.3
	0.041 @ $V_{GS} = -4.5V$	



Description

This new generation Trench MOSFET from Zetex has been designed to minimize the on-state resistance ($R_{DS(on)}$) and yet maintain superior switching performance, making it ideal for high efficiency power management applications.

Features

- Low on-resistance
- Fast switching speed
- Low gate drive
- Dual SO8 package

Applications

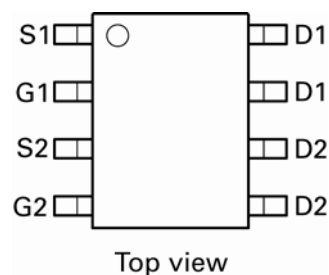
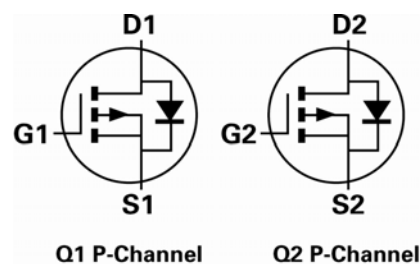
- DC-DC Converters
- Power management functions
- Disconnect switches
- Motor control

Ordering information

Device	Reel size (inches)	Tape width (mm)	Quantity per reel
ZXMP3F37DN8TA	7	12	500

Device marking

ZXMP 3F37D



ZXMP3F37DN8

Absolute maximum ratings

Parameter	Symbol	Limit	Unit
Drain-Source voltage	V_{DSS}	-30	V
Gate-Source voltage	V_{GS}	± 20	V
Continuous Drain current @ $V_{GS} = -10V$; $T_A = 25^\circ C$ (b)(d) @ $V_{GS} = -10V$; $T_A = 70^\circ C$ (b)(d) @ $V_{GS} = -10V$; $T_A = 25^\circ C$ (a)(d) @ $V_{GS} = -10V$; $T_L = 25^\circ C$ (f)	I_D	-7.3 -5.9 -5.7 -8.3	V
Pulsed Drain current (c)	I_{DM}	-36	A
Continuous Source current (Body diode) (b)	I_S	-3.5	A
Pulsed Source current (Body diode) (c)	I_{SM}	-36	A
Power dissipation at $T_A = 25^\circ C$ (a)(d) Linear derating factor	P_D	1.25 10	W mW/ $^\circ C$
Power dissipation at $T_A = 25^\circ C$ (a)(e) Linear derating factor	P_D	1.8 14	W mW/ $^\circ C$
Power dissipation at $T_L = 25^\circ C$ (b)(d) Linear derating factor	P_D	2.1 17	W mW/ $^\circ C$
Power dissipation at $T_L = 25^\circ C$ (a)(f) Linear derating factor	P_D	2.7 21.5	W mW/ $^\circ C$
Operating and storage temperature range	T_j, T_{stg}	-55 to 150	$^\circ C$

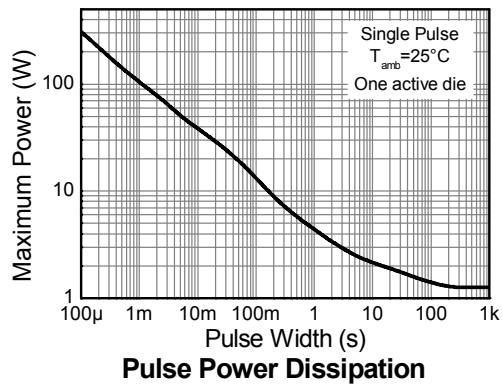
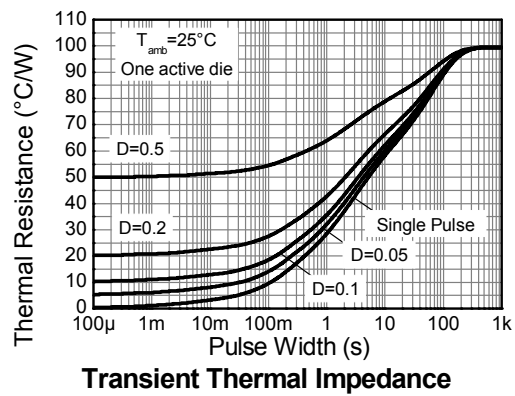
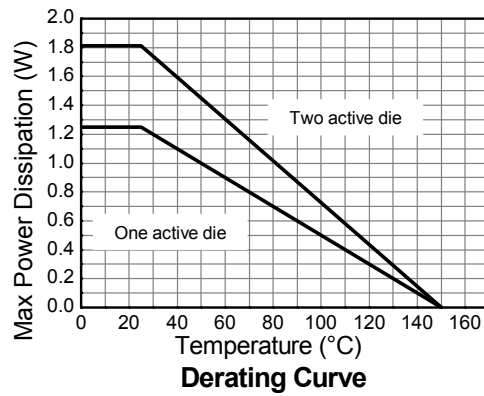
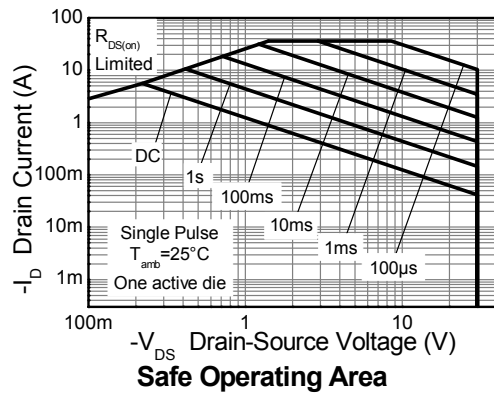
Thermal resistance

Parameter	Symbol	Value	Unit
Junction to ambient (a)(d)	$R_{\theta JA}$	100	$^\circ C/W$
Junction to ambient (b)(e)	$R_{\theta JA}$	70	$^\circ C/W$
Junction to ambient (b)(d)	$R_{\theta JA}$	60	$^\circ C/W$
Junction to lead (a)(f)	$R_{\theta JL}$	46.42	$^\circ C/W$

NOTES:

- (a) For a dual device surface mounted on 25mm x 25mm x 1.6mm FR4 PCB with high coverage of single sided 1oz copper, in still air conditions.
- (b) For a dual device surface mounted on FR4 PCB measured at $t \leq 10$ sec.
- (c) Repetitive rating on 25mm x 25mm FR4 PCB, $D=0.02$, pulse width 300us – pulse width limited by maximum junction temperature.
- (d) For a dual device with one active die.
- (e) For a dual device with 2 active die running at equal power.
- (f) Thermal resistance from junction to solder-point (at the end of the drain lead).

Thermal characteristics



ZXMP3F37DN8

Electrical characteristics (at $T_{amb} = 25^{\circ}\text{C}$ unless otherwise stated) Q1 and Q2

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Static						
Drain-Source breakdown voltage	V _{(BR)DSS}	-30			V	I _D = -250μA, V _{GS} =0V
Zero Gate voltage Drain current	I _{DSS}			-1.0	μA	V _{DS} =-YV, V _{GS} =0V
Gate-Body leakage	I _{GSS}			100	nA	V _{GS} =±20V, V _{DS} =0V
Gate-Source threshold voltage	V _{GS(th)}	-1.3		-2.5	V	I _D = -250μA, V _{DS} =V _{GS}
Static Drain-Source on-state resistance ^(*)	R _{DS(on)}			0.025 0.041	Ω	V _{GS} = -10V, I _D = -7.1A V _{GS} = -4.5V, I _D = -5.5A
Forward Transconductance ^(*) (†)	g _{fs}		18.6		S	V _{DS} = -15V, I _D = -7.1A
Dynamic ^(†)						
Input capacitance	C _{iSS}		1678		pF	V _{DS} = -15V, V _{GS} =0V f=1MHz
Output capacitance	C _{oSS}		303		pF	
Reverse transfer capacitance	C _{rSS}		178		pF	
Switching ^(‡) (†)						
Turn-on-delay time	t _{d(on)}		3.5		ns	V _{DD} = -15V, V _{GS} = -10V I _D = -1A R _G ≅ 6.0Ω,
Rise time	t _r		4.9		ns	
Turn-off delay time	t _{d(off)}		44		ns	
Fall time	t _f		28		ns	
Gate charge						
Total Gate charge	Q _g		31.6		nC	V _{DS} = -15V, V _{GS} = -10V I _D = -7.1A
Gate-Source charge	Q _{gs}		4.3		nC	
Gate-Drain charge	Q _{gd}		6.2		nC	
Source–Drain diode						
Diode forward voltage ^(*)	V _{SD}		-0.80	-1.2	V	I _S = -1.7A,V _{GS} =0V
Reverse recovery time ^(‡)	t _{rr}		16.2		ns	I _S = -2.2A,di/dt=100A/μs
Reverse recovery charge ^(‡)	Q _{rr}		10		nC	

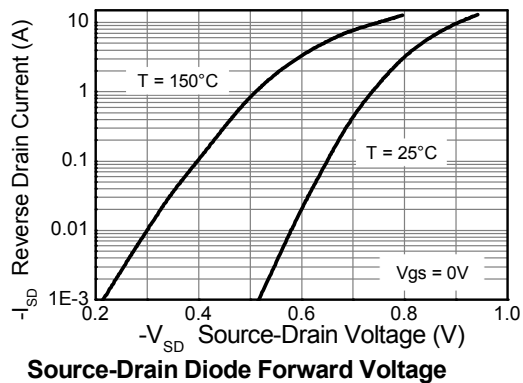
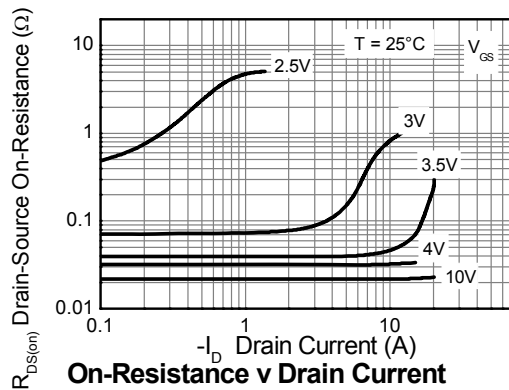
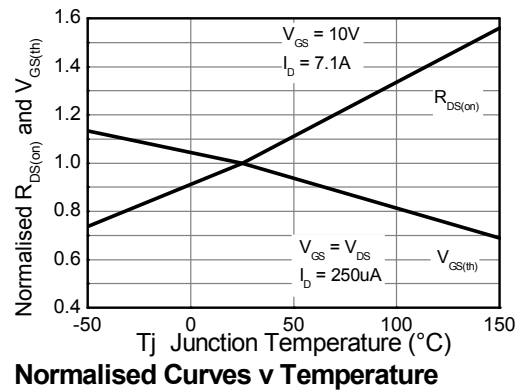
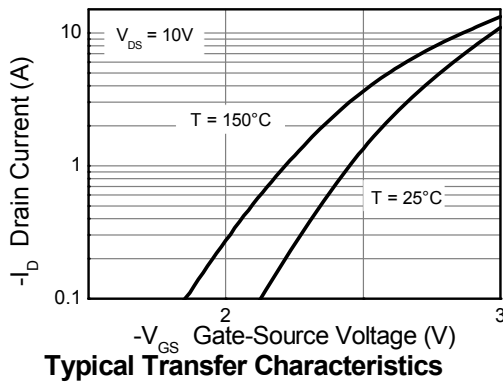
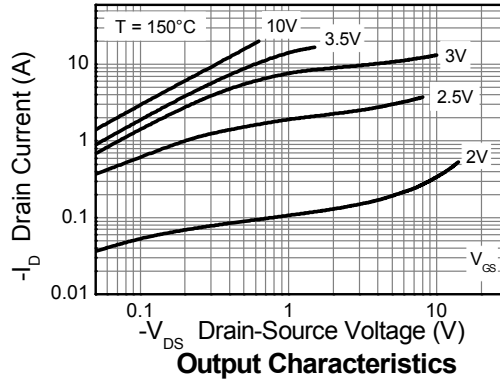
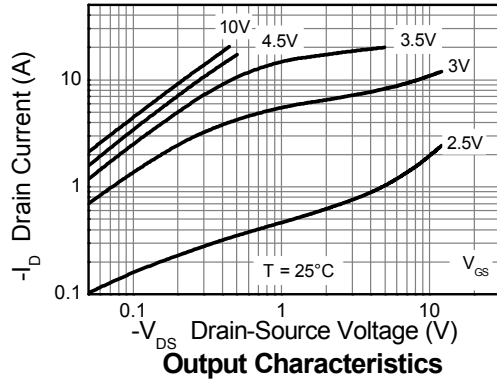
NOTES:

(*) Measured under pulsed conditions. Pulse width $\leq 300\mu\text{s}$; duty cycle $\leq 2\%$.

(†) Switching characteristics are independent of operating junction temperature.

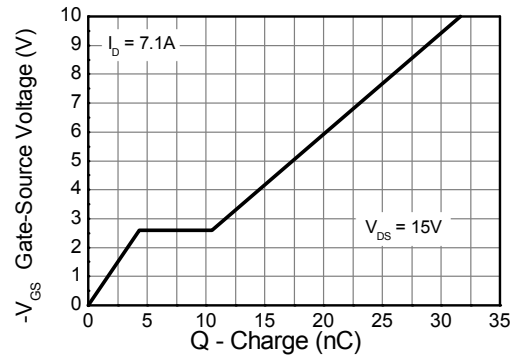
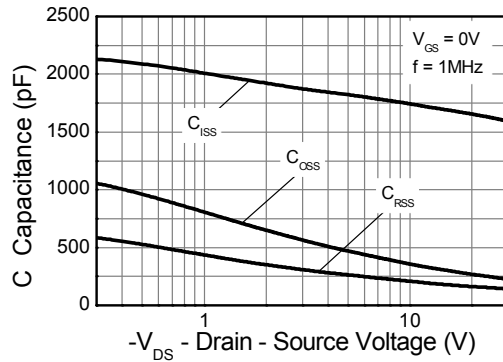
(‡) For design aid only, not subject to production testing

Typical characteristics

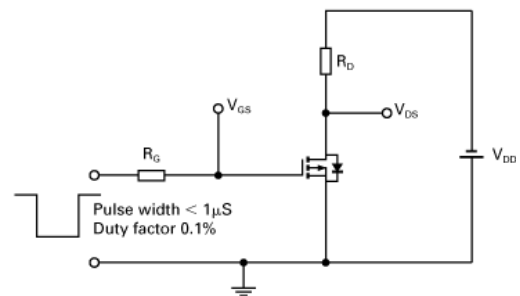
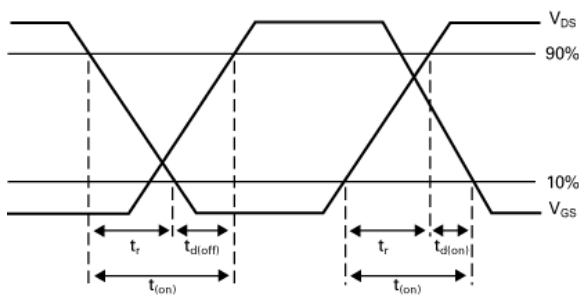
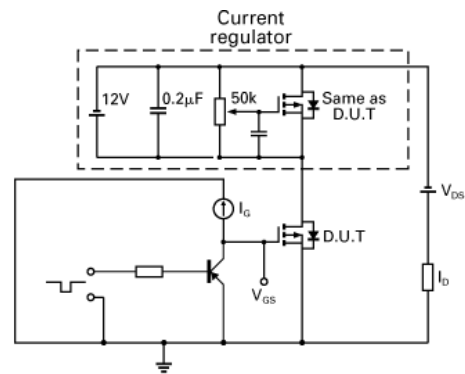
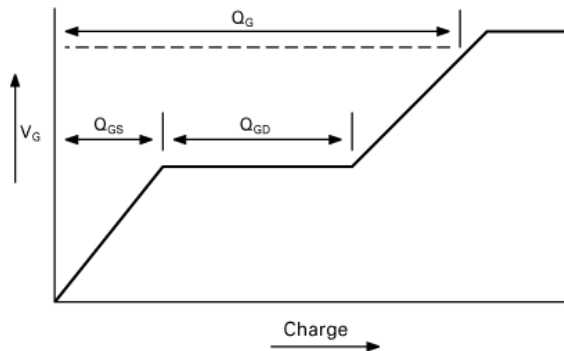


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Typical characteristics

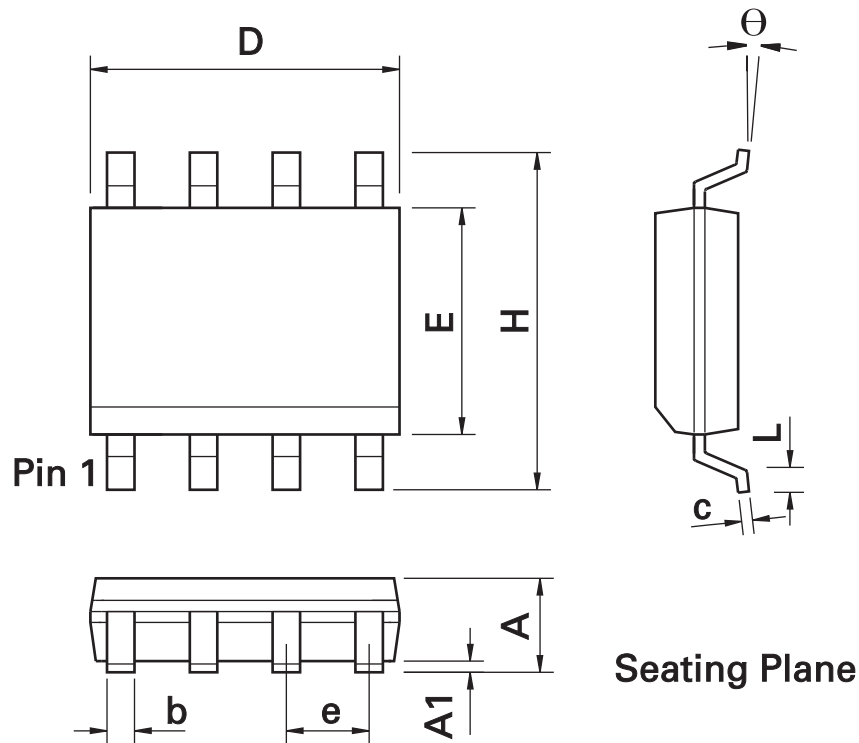


Test circuits



ZXMP3F37DN8

Package outline SO8



SO8 Package Information

DIM	Inches		Millimeters		DIM	Inches		Millimeters	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	0.053	0.069	1.35	1.75	e	0.050 BSC		1.27 BSC	
A1	0.004	0.010	0.10	0.25	b	0.013	0.020	0.33	0.51
D	0.189	0.197	4.80	5.00	c	0.008	0.010	0.19	0.25
H	0.228	0.244	5.80	6.20	U	0°	8°	0°	8°
E	0.150	0.157	3.80	4.00	h	0.010	0.020	0.25	0.50
L	0.016	0.050	0.40	1.27	-	-	-	-	-

Note: Controlling dimensions are in inches. Approximate dimensions are provided in millimeters

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