AM4953P

Analog Power

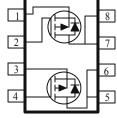
Dual P-Channel 30-V (D-S) MOSFET

These miniature surface mount MOSFETs utilize High Cell Density process. Low $r_{DS(on)}$ assures minimal power loss and conserves energy, making this device ideal for use in power management circuitry. Typical applications are PWMDC-DC converters, power management in portable and battery-powered products such as computers, printers, battery charger, telecommunication power system, and telephones power system.

- Low r_{DS(on)} Provides Higher Efficiency and Extends Battery Life
- Miniature SO-8 Surface Mount Package Saves Board Space
- High power and current handling capability
- Extended VGS range (±25) for battery pack applications

PRODUCT SUMMARY				
V _{DS} (V)	$r_{DS(on)} m(\Omega)$	I _D (A)		
-30	$52 @ V_{GS} = -10V$	-5.2		
	$89 @ V_{GS} = -4.5V$	-4.0		





ABSOLUTE MAXIMUM RATINGS (T _A = 25 °C UNLESS OTHERWISE NOTED)					
Parameter		Symbol	Maximum	Units	
Drain-Source Voltage		V _{DS}	-30	V	
Gate-Source Voltage		V _{GS}	±25	v	
Continuous Drain Current ^a	T _A =25°C	Τ_	±5.2		
	$T_{A}=25^{\circ}C$ $T_{A}=70^{\circ}C$	чD	±4.2	А	
Pulsed Drain Current ^b		I _{DM}	±30		
Continuous Source Current (Diode Conduction) ^a		I _S	-1.6	А	
Power Dissipation ^a	T _A =25°C	P_	2.1	W	
	$T_{A}=25^{\circ}C$ $T_{A}=70^{\circ}C$	1 D	1.3	vv	
Operating Junction and Storage Temperature Range		T _J , T _{stg}	-55 to 150	°C	

THERMAL RESISTANCE RATING	S			
Parameter		Symbol	Maximum	Units
Maximum Junction-to-Case ^a	t <= 5 sec	$R_{\theta JC}$	40	°C/W
Maximum Junction-to-Ambient ^a	t <= 10 sec	$R_{\theta JA}$	60	°C/W

Notes

- a. Surface Mounted on 1" x 1" FR4 Board.
- b. Pulse width limited by maximum junction temperature

SPECIFICATIONS ($T_A = 25^{\circ}C$ UNLESS OTHERWISE NOTED)							
Parameter	Southal	Test Conditions	Limits			Unit	
rarameter	Symbol	Test Conditions	Min	Тур	Max	Omt	
Static							
Gate-Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_D = -250 \text{ uA}$	-1				
Gate-Body Leakage	I _{GSS}	$V_{DS} = 0 V, V_{GS} = \pm 25 V$			±100	nA	
Zero Gate Voltage Drain Current	Т	$V_{DS} = -24 V, V_{GS} = 0 V$			-1	11.4	
Zero Gate Voltage Drain Current	I _{DSS}	$V_{DS} = -24 V, V_{GS} = 0 V, T_J = 55^{\circ}C$			-5	uA	
On-State Drain Current ^A	I _{D(on)}	$V_{DS} = -5 V, V_{GS} = -10 V$	-30			Α	
	r _{DS(on)}	$V_{GS} = -10 \text{ V}, I_D = -5.2 \text{ A}$			52	mΩ	
Drain-Source On-Resistance ^A		$V_{GS} = -4.5 \text{ V}, I_D = -4.0 \text{ A}$			89		
Forward Tranconductance ^A	$g_{\rm fs}$	$V_{\rm DS}$ = -15 V, $I_{\rm D}$ = -5.2 A		19		S	
Diode Forward Voltage	V _{SD}	$I_{\rm S} = -2.1 \text{ A}, V_{\rm GS} = 0 \text{ V}$		-0.7		V	
Dynamic ^b							
Total Gate Charge	Qg	$V_{DS} = -15 \text{ V}, V_{GS} = -10 \text{ V},$ $I_D = -5.2 \text{ A}$		15		nC	
Gate-Source Charge	Q _{gs}			2.2			
Gate-Drain Charge	Q _{gd}			1.7			
Turn-On Delay Time	t _{d(on)}			10			
Rise Time	t _r	V_{DD} = -15 V, R_L = 15 Ω , ID = -1 A,		2.8		nS	
Turn-Off Delay Time	t _{d(off)}	VGEN = -10 V, $RG = 6\Omega$		53.6			
Fall-Time	t _f	1		46			

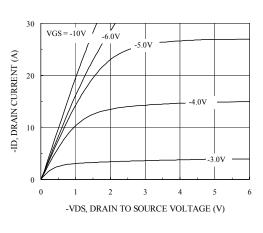
Notes

(C)

- a. Pulse test: $PW \le 300$ us duty cycle $\le 2\%$.
- b. Guaranteed by design, not subject to production testing.

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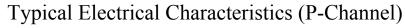


Figure 1. On-Region Characteristics

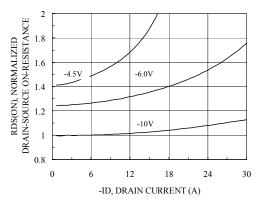


Figure 3. On Resistance Vs Vgs Voltage

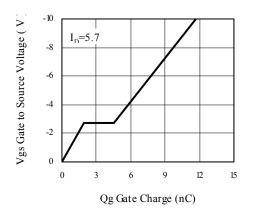


Figure 5. Gate Charge Characteristics

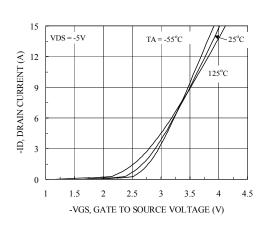


Figure 2. Body Diode Forward Voltage Variation with Source Current and Temperature

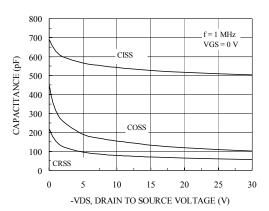


Figure 4. Capacitance Characteristics

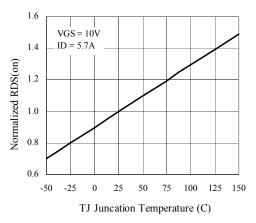
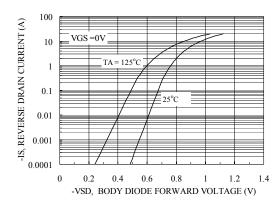
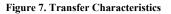


Figure 6. On-Resistance Variation with Temperature



Typical Electrical Characteristics (P-Channel)



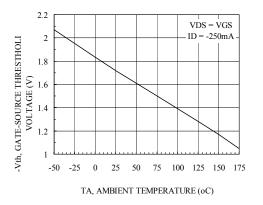


Figure 9. Vth Gate to Source Voltage Vs Temperature

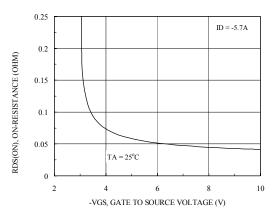


Figure 8. On-Resistance with Gate to Source Voltage

