Single-chip Type with Built-in FET Switching Regulators

Simple Step-down Switching Regulator with Built-in Power MOSFET

BD9329AEFJ

No.11027EAT56

●Description

The BD9329AEFJ is a synchronous step-down switching regulator that integrates 2 low resistance N-channel MOSFETs. It achieves 3A continuous output current over a wide input supply range. Current mode operation provides fast transient response and easy phase compensation.

●Features

1) Wide operating INPUT Range 4.2V～18.0V
2) 3A Output Current
3) Hi-side / Lo-side FET ON-resistance; 0.15 / 0.13Ω Power Switch
4) Low ESR Output Ceramic Capacitors are Available
5) Low Standby Current during Shutdown Mode
6) 380 kHz Fixed Operating Frequency
7) Feedback voltage 0.9V ±1.5% Accuracy at room temp. (±2.0% guaranteed for -25℃ to 85℃ temperature range)
8) Protection Circuits
   - Under Voltage Lockout Protection
   - Thermal Shutdown
   - Over Current Protection
9) HTSOP-J8 Package with Exposed thermal PAD.

●Applications

Distributed Power System
Pre-Regulator for Linear Regulator

●Absolute maximum ratings (Ta = 25℃)

Parameter	Symbol	Ratings	Unit
Supply Voltage	VIN	20	V
Switch Voltage	V_{SW}	20	V
Power Dissipation for HTSOP-J8	Pd	3760 *1	mW
Package thermal resistance θja *2	θja	29.27	℃/W
Package thermal resistance θjc *2	θjc	3.75	℃/W
Operating Temperature Range	Topr	-40～+85	℃
Storage Temperature Range	Tstg	-55～+150	℃
Junction Temperature	Tjmax	150	℃
BST Voltage	V_{BST}	V_{SW}+7	V
EN Voltage	V_{EN}	20	V
All other pins	V_{OTH}	20	V

*1 Derating in done 30.08 mW/℃ for operating above Ta≧25℃(Mount on 4-layer 70.0mm×70.0mm×1.6mm board)
*2 Mount on 4-layer 50mm x 30mm x 1.6mm application board

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●**Operation Range** (Ta= -40～85℃)

Parameter	Symbol	Ratings			Unit
		Min	Typ	Max	
Supply Voltage	V_{IN}	4.2	12	18	V
SW Voltage	V_{SW}	-0.5	-	18	V
Output current	I_{SW3}	-	-	3	A
Output voltage range	V_{RANGE}	0.9	-	V_{IN} x 0.7	V

●**Electrical characteristics** (Unless otherwise specified VIN=12V Ta=25℃)

Parameter	Symbol	Limits			Unit	Conditions
		Min	Typ	Max		
Error amplifier block						
FB input bias current	I_{FB}	-	0.02	2	μA	
Feedback voltage1	V_{FB1}	0.886	0.900	0.914	V	Voltage follower
Feedback voltage2	V_{FB2}	0.882	0.900	0.918	V	Ta=-25℃～85℃
SW block – SW						
Hi-side FET On-resistance	R_{ONH}	-	0.15	-	Ω	I_{SW}= -0.8A
Lo-side FET On-resistance	R_{ONL}	-	0.13	-	Ω	I_{SW}= 0.8A
Hi/Lo-side FET Leak current	I_{LEAKN}	-	0	10	μA	V_{IN}= 18V, V_{SW} = 0V / 18V
Switch Current Limit	I_{LIMIT3}	3.5	-	-	A	
Maximum duty cycle	M_{DUTY}	-	90	-	%	V_{FB}= 0V
General						
Enable Sink current	I_{EN}	90	180	270	μA	V_{EN}= 12V
Enable Threshold voltage	V_{EN}	1.0	1.2	1.4	V	
Under Voltage Lockout threshold	V_{UVLO}	3.5	3.75	4.0	V	V_{IN} rising
Under Voltage Lockout Hysteresis	V_{HYS}	-	0.3	-	V	
Soft Start Current	I_{SS}	5	10	15	μA	V_{SS}= 0 V
Soft Start Time	T_{SS}	-	22	-	ms	C_{SS}= 0.1 μF
Operating Frequency	F_{OSC}	300	380	460	kHz	
Circuit Current	I_{CC}	-	1.2	3	mA	V_{FB}= 1.5V, V_{EN}= 12V
Quiescent Current	I_{QUI}	-	15	27	μA	V_{EN}= 0V

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●Block Diagram

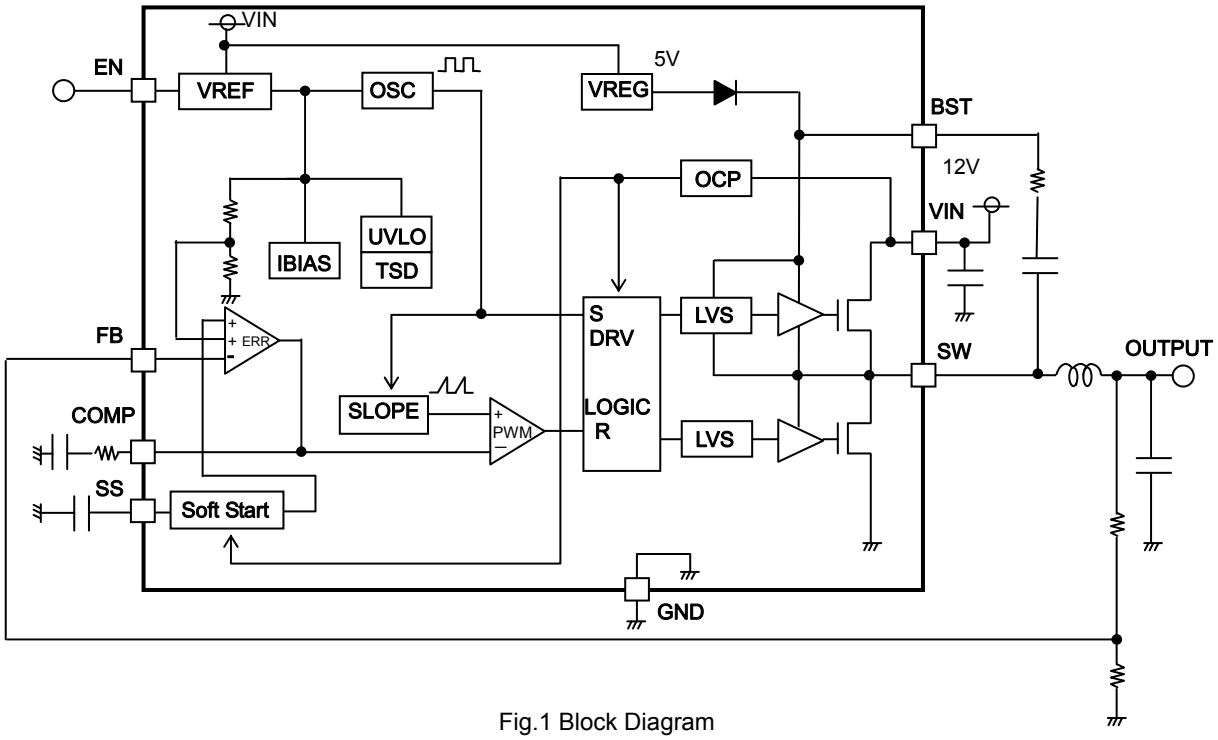
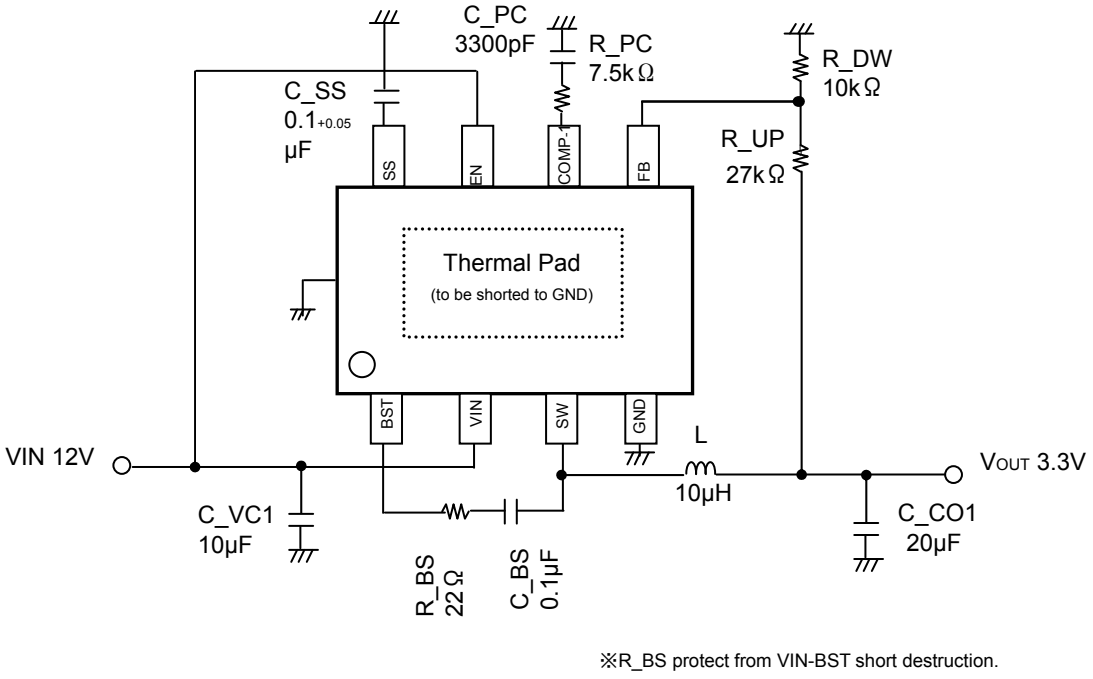


Fig.1 Block Diagram

●Typical Application Circuit



※R_BS protect from VIN-BST short destruction.

Fig.2 Application Circuit

	Symbol	Maker	Part No	
Input capacitor	C_VC1	TDK	C3225JB1E106K	10μF/25V
Output capacitor	C_CO1	TDK	C3216JB1C106M	10μF/16V
Inductor	L	TDK	SLF10165-100M3R8	10μH/3.8A

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●Block Operation

・VREG
A block to generate constant-voltage for DC/DC boosting.

・VREF
A block that generates internal reference voltage of 5.1 V (Typ.).

・TSD/UVLO
TSD (Thermal shutdown)/UVLO (Under Voltage Lockout) protection block.
The TSD circuit shuts down IC at high temperature.
The UVLO circuit shuts down the IC when the VCC is Low Voltage.

・Error amp block (ERR)
This is the circuit to compare the reference voltage and the feedback voltage of output voltage. The COMP pin voltage resulting from this comparison determines the switching duty. At the time of startup, since the soft start is operated by the SS pin voltage, the COMP pin voltage is limited to the SS pin voltage.

・Oscillator block (OSC)
This block generates the oscillating frequency.

・SLOPE block
This block generates the triangular waveform from the clock created by OSC. Generated triangular waveform is sent to the PWM comparator.

・PWM block
The COMP pin voltage output by the error amp is compared to the SLOPE block's triangular waveform to determine the switching duty. Since the switching duty is limited by the maximum duty ratio which is determined internally, it does not become 100%.

・DRV block
A DC/DC driver block. A signal from the PWM is input to drive the power FETs.

・Soft start circuit
Since the output voltage rises gradually while restricting the current at the time of startup, it is possible to prevent the output voltage overshoot or the rush current.

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●Outward form

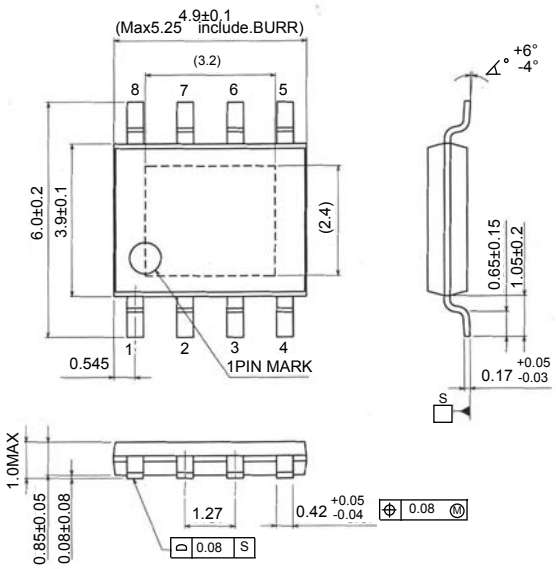


Fig.3 HTSOP-J8 Package
(Unit:mm)

●Pin Assignment and Pin Function

Pin No.	Pin name	Function
1	BST	High-Side Gate Drive Boost Input
2	VIN	Power Input
3	SW	Power Switching Output
4	GND	Ground
5	FB	Feed Back Input
6	COMP	Compensation Node
7	EN	Enable Input
8	SS	Soft Start Control Input

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●**Typical Performance Characteristics** (Unless otherwise specified, VIN= 12V Ta = 25℃)

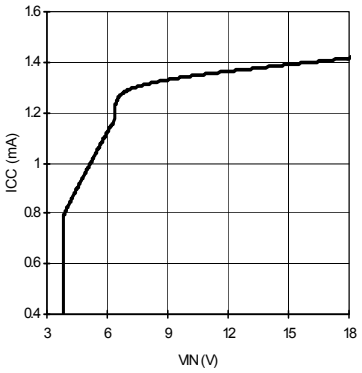


Fig.4 Circuit Current
(No switching)

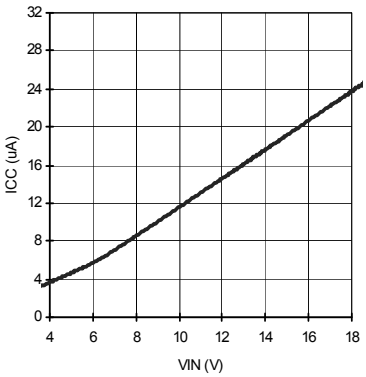


Fig.5 Stand by current
(IC not active)

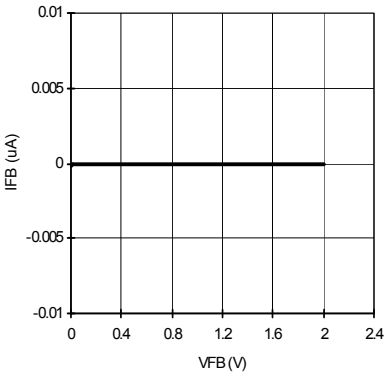


Fig.6 Input Bias Current

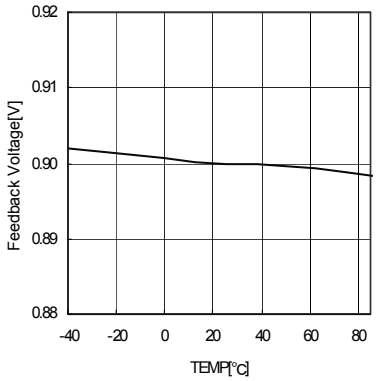


Fig.7 Feedback voltage

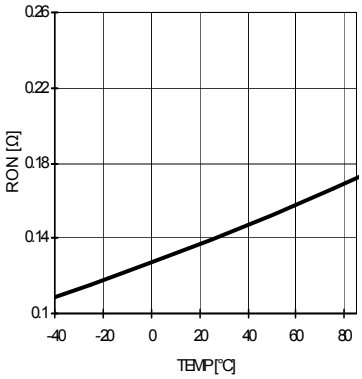


Fig.8 Hi,Low-Side
On-resistance

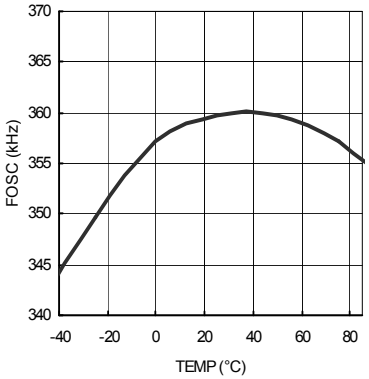


Fig.9 Operating Frequency

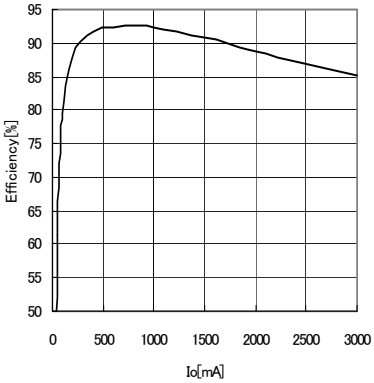


Fig.10 STEP Down Efficiency
(VIN= 12V VOUT= 3.3V L=10μH)

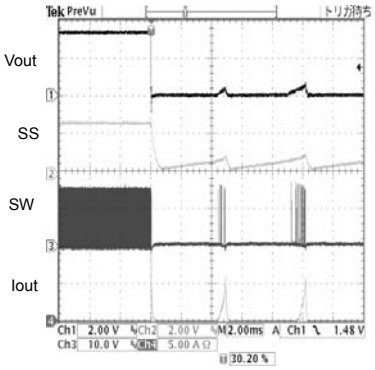


Fig.11 OverCurrent Protection
(VOUT is shorted to GND)

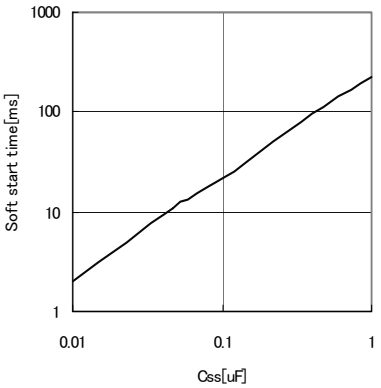


Fig.12 Soft Start Time

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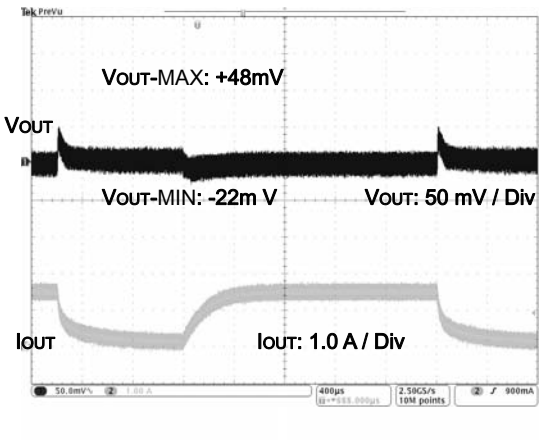


Fig.13 Transcient Response
(VIN= 12V VOUT= 3.3V L= 10μH Cout =22μF Iout= 0.2-1.0A)

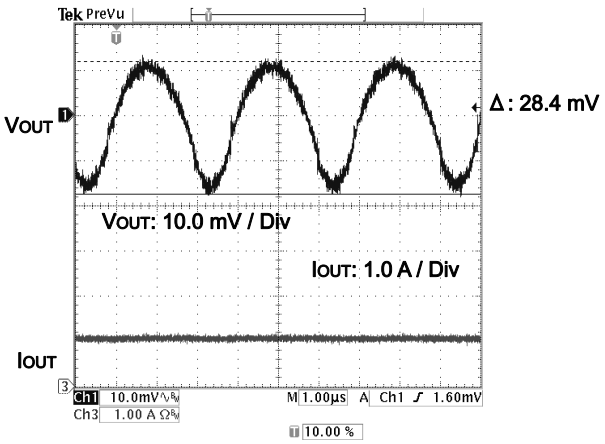


Fig.14 Output Ripple Voltage
(VIN= 12V VOUT= 3.3V L= 10μH Cout =22μF I out= 1.0A)

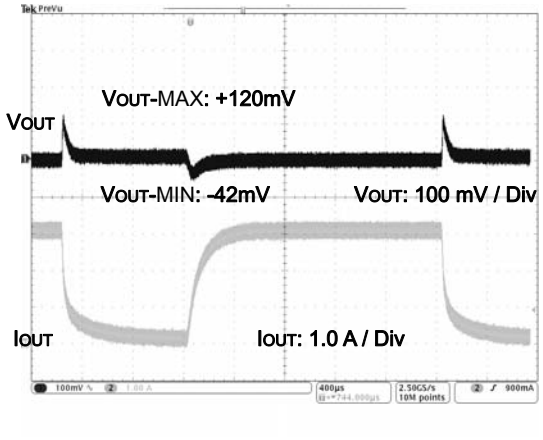


Fig.15 Transcient Response
(VIN= 12V VOUT= 3.3V L= 10μH Cout =22μF Iout= 0.2-3.0A)

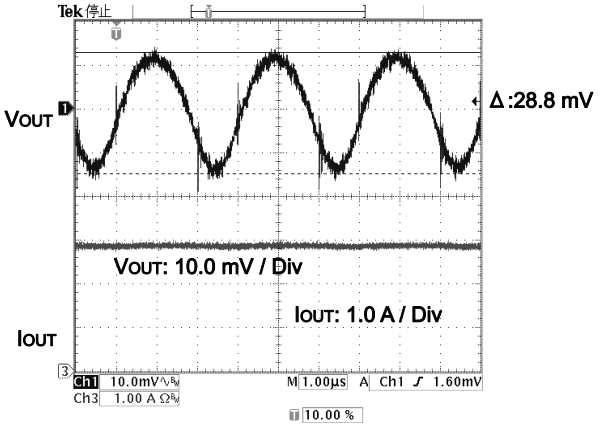


Fig.16 Output Ripple Voltage
(VIN= 12V VOUT= 3.3V L= 10μH Cout =22μF I out= 3 .0A)

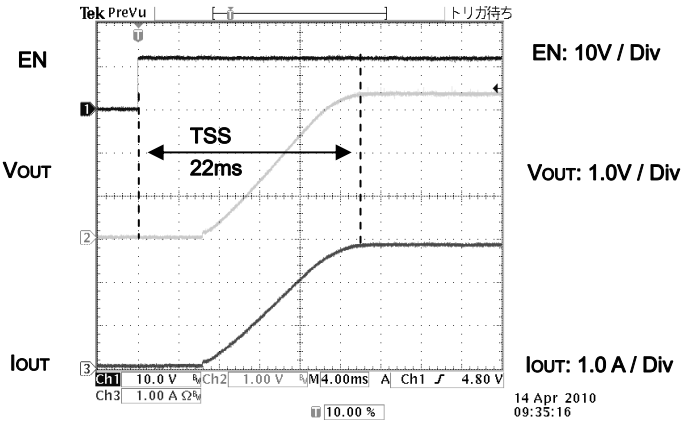


Fig.17 Start Up waveform
(VIN= 12V VOUT= 3.3V L= 10μH CSS= 0.1μF)

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●Selecting Application Components

(1) Output LC filter constant selection (Buck Converter)
The Output LC filter is required to supply constant current to the output load. A larger value inductance at this filter results in less inductor ripple current (ΔIL) and less output ripple voltage. However, the larger value inductors tend to have less fast load transient-response, a larger physical size, a lower saturation current and higher series resistance. A smaller value inductance has almost opposite characteristics above.So Choosing the Inductor ripple current (ΔIL) between 20 to 40% of the averaged inductor current (equivalent to the output load current) is a good compromise.

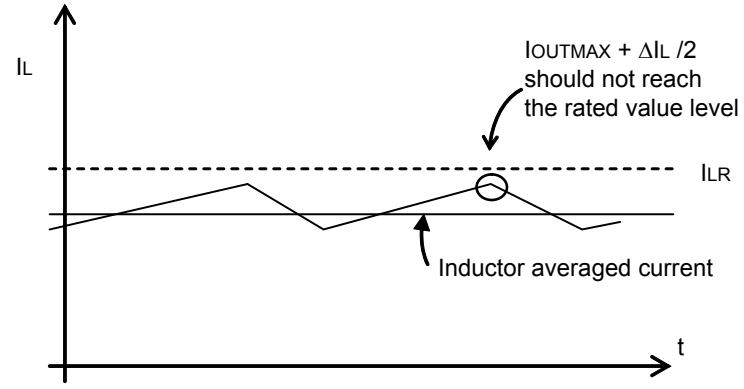


Fig.18

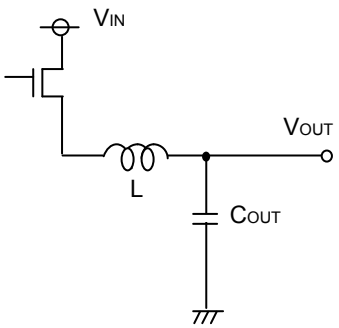


Fig.19

Setting ΔIL = 30% x Averaged Inductor current (2A) = 0.6 [A]

$$L = V_{OUT} \times (V_{IN} - V_{OUT}) \times \frac{1}{V_{IN} \times F_{OSC} \times \Delta I_L} = 10\mu\,[H]$$

Where VIN= 12V, VOUT= 3.3V, FOSC= 380 kHz,
; FOSC is a switching frequency

Also the inductor should have the higher saturation current than IOUTMAX + ΔIL / 2.

The output capacitor COUT affects the output ripple-voltage. Choose the large capacitor to achieve the small ripple-voltage enough to meet the application requirement.

Output ripple voltage ΔVRPL is calculated by the following equation.

$$\Delta V_{RPL} = \Delta I_L \times \left(R_{ESR} + \frac{1}{8 \times C_{OUT} \times F_{OSC}} \right) \quad [V]$$

Where RESR is a parasitic series resistance in output capacitor.

Setting COUT = 20μF, RESR = 10mΩ

ΔVRPL = 0.6 x (10m + 1 / (8 x 20u x 380k)) = 15.8mV

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(2) Loop Compensation
Choosing compensation capacitor C_{CMP} and resistor R_{CMP}

The current-mode buck converter has 2-poles and 1-zero system. Choosing the compensation resistor and capacitor is important for a good load-transient response and good stability.
The example of DC/DC converter application bode plot is shown below.

The compensation resistor R_{CMP} will decides the cross over frequency F_{CRS} (the frequency that the total DC-DC loop-gain falls to 0dB).
Setting the higher cross over frequency achieves good response speed, however less stability. While setting the lower cross over frequency shows good stability but worse response speed.
The 1/10 of switching frequency for the cross over frequency shows a good performance at most applications.

(i) Choosing phase compensation resistor R_{CMP}
The compensation resistor R_{CMP} can be on following formula.

$$R_{CMP} = \frac{2\pi \times V_{OUT} \times F_{CRS} \times C_{OUT}}{V_{FB} \times G_{MP} \times G_{MA}} \quad [\Omega]$$

Where
V_{OUT} ; Output voltage, **F_{CRS}** ; Cross over frequency, **C_{OUT}** ; Output Capacitor,
V_{FB} ; internal feedback voltage (**0.9V(TYP)**), **G_{MP}** ; Current Sense Gain (**7.8A/V(TYP)**) ,
G_{MA} ; Error Amplifier Trans-conductance (**300μA/V(TYP)**)

Setting V_{OUT}= 3.3V, F_{CRS}= 38kHz, C_{OUT}= 20μF;

$$R_{CMP} = \frac{2\pi \times 3.3 \times 38k \times 20u}{0.9 \times 7.8 \times 300u} = 7.48k \sim= 7.5k \quad [\Omega]$$

(ii) Choosing phase compensation capacitor CCMP
For the stability of DC/DC converter, canceling the phase delay that derives from output capacitor C_{OUT} and resistive load R_{OUT} by inserting the phase advance.
The phase advance can be added by the zero on compensation resistor R_{CMP} and capacitor C_{CMP}.
Making Fz= F_{CRS} / 6 gives a first-order estimate of C_{CMP}.

$$\text{Compensation Capacitor} \quad C_{CMP} = \frac{1}{2\pi \times R_{CMP} \times Fz} \quad [F]$$

Setting Fz= F_{CRS}/6 = 6.3kHz;

$$\text{Compensation Capacitor} \quad C_{CMP} = \frac{1}{2\pi \times 7.5k \times 6.3k} = 3.54n \sim= 3.3n \quad [F]$$

(iii) The condition of the loop compensation stability
The stability of DC/DC converter is important. To secure the operating stability, please check the loop compensation has the enough phase-margin. For the condition of loop compensation stability, the phase-delay must be less than 150 degree where Gain is 0 dB.
Feed forward capacitor C_{RUP} boosts phase margin over a limited frequency range and is sometimes used to improve loop response. C_{RUP} will be more effective if $R_{UP} >> R_{UP}||R_{DW}$

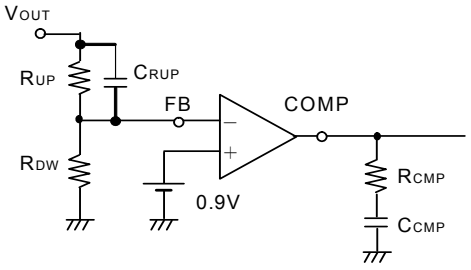


Fig.20

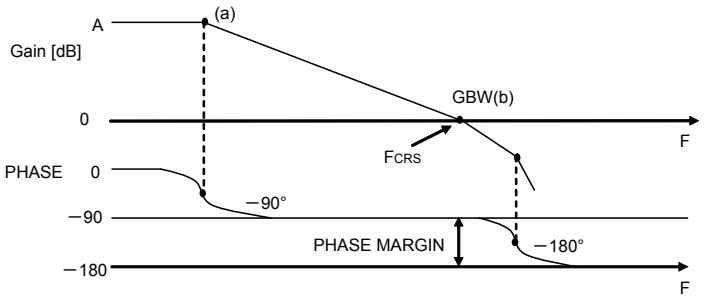


Fig.21

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(3) Design of Feedback Resistance constant
Set the feedback resistance as shown below.

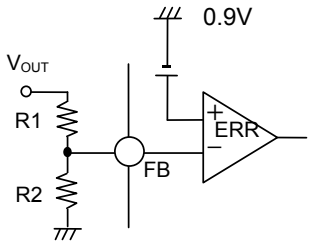


Fig.22

$$V_{OUT} = \frac{R1 + R2}{R2} \times 0.9 \quad [V]$$

●Soft Start Function

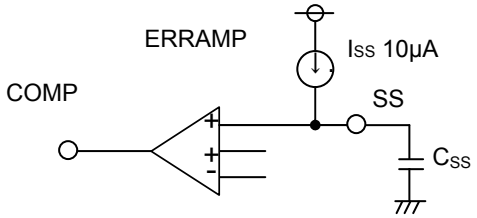


Fig.23

An adjustable soft-start function to prevent high inrush current during start-up is available.
The soft-start time is set by the external capacitor connected to SS pin.
The soft start time is given by;

T_{SS} [s] = 2.2 x Css / I_{SS}

Setting C_{SS}= 0.1μF;
T_{SS}= 2.2 x 0.1μ / 10μ = 22 [ms]

Please confirm the overshoot of the output voltage and inrush current when deciding the SS capacitor value.

●EN Function

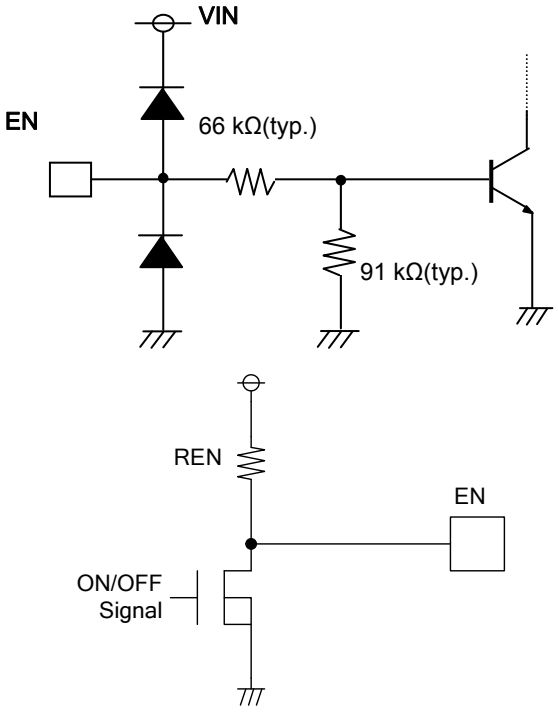


Fig.24

The EN terminal control IC's shut down.
Leaving EN terminal open makes IC shutdown.
To start the IC, EN terminal should be connected to VIN or the other power source output.
When the EN voltage exceed 1.2V (typ.), the IC start operating.

(Attention)
Chattering happens if standing lowering speed is slow when standing of EN pin is lowered.
The reverse current in which the input side and the pressure operation are done from the output side is generated when chattering operates with the output voltage remained, and there is a case to destruction.
Please set to stand within 100us when you control ON/OFF by the EN signal.
This necessity doesn't exist when EN pin is connected with VIN and EN is not controlled.
The control by open drain MOSFET shown in a left chart is recommended.

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●Layout Pattern Consideration

Two high pulsing current flowing loops exist in the buck regulator system. The first loop, when FET is ON, starts from the input capacitors, to the VIN terminal, to the SW terminal, to the inductor, to the output capacitors, and then returns to the input capacitor through GND. The second loop, when FET is OFF, starts from the low FET, to the inductor, to the output capacitor, and then returns to the low FET through GND. To reduce the noise and improve the efficiency, please minimize these two loop area. Especially input capacitor, output capacitor and low FET should be connected to GND plain. PCB Layout may affect the thermal performance, noise and efficiency greatly. So please take extra care when designing PCB Layout patterns.

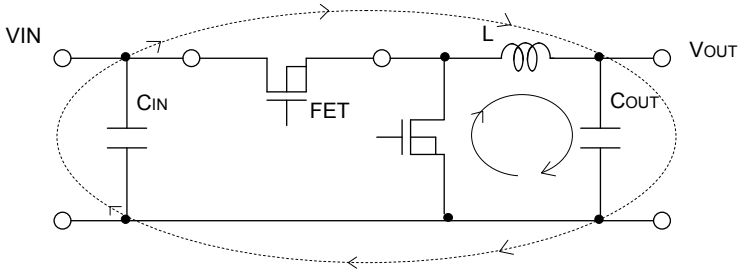


Fig.25 Current loop in Buck regulator system

- The thermal Pad on the back side of IC has the great thermal conduction to the chip. So using the GND plain as broad and wide as possible can help thermal dissipation. And a lot of thermal via for helping the spread of heat to the different layer is also effective.
- The input capacitors should be connected as close as possible to the VIN terminal.
- Keep sensitive signal traces such as trace connected FB and COMP away from SW pin.
- The inductor and the output capacitors should be placed close to SW pin as much as possible.

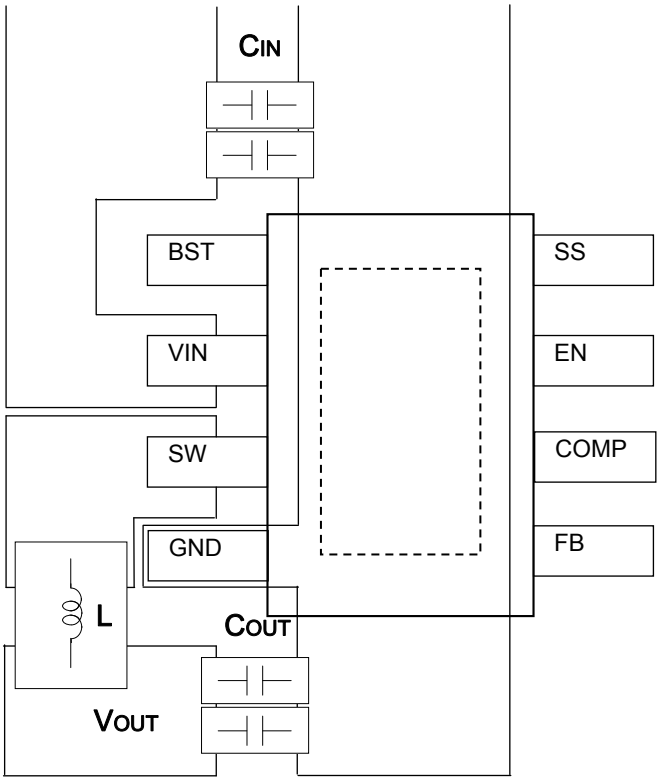
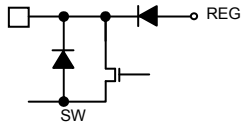
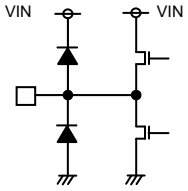
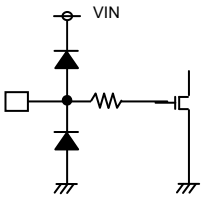
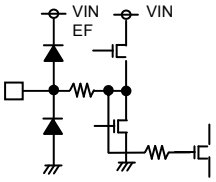
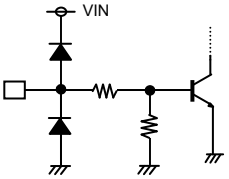
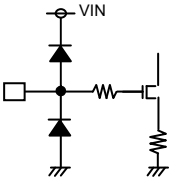


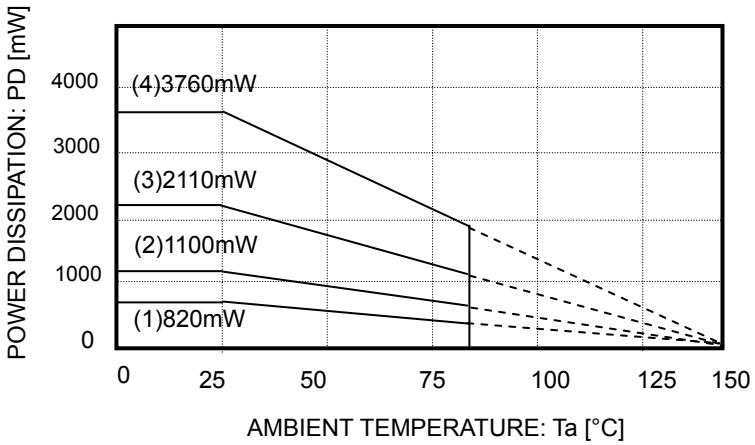
Fig.26 The example of PCB layout pattern

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●I/O Equivalent Circuit Diagram

1.BST	3.SW	5.FB
		
6.COMP	**7.EN**	**8.SS**
		

●Power Dissipation



HTSOP-J8 Package
On 70 × 70 × 1.6 mm glass epoxy PCB
(1) 1-layer board (Backside copper foil area 0 mm× 0 mm)
(2) 2-layer board (Backside copper foil area 15 mm × 15 mm)
(3) 2-layer board (Backside copper foil area 70 mm × 70 mm)
(4) 4-layer board (Backside copper foil area 70 mm × 70 mm)

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●Notes for use

1) Absolute maximum ratings
Use of the IC in excess of absolute maximum ratings such as the applied voltage or operating temperature range may result in IC damage. Assumptions should not be made regarding the state of the IC (short mode or open mode) when such damage is suffered. A physical safety measure such as a fuse should be implemented when use of the IC in a special mode where the absolute maximum ratings may be exceeded is anticipated.

2) GND potential
Ensure a minimum GND pin potential in all operating conditions.

3) Setting of heat
Use a thermal design that allows for a sufficient margin in light of the power dissipation (Pd) in actual operating conditions.

4) Pin short and mistake fitting
Use caution when orienting and positioning the IC for mounting on printed circuit boards. Improper mounting may result in damage to the IC. Shorts between output pins or between output pins and the power supply and GND pins caused by the presence of a foreign object may result in damage to the IC.

5) Actions in strong magnetic field
Use caution when using the IC in the presence of a strong magnetic field as doing so may cause the IC to malfunction.

6) Testing on application boards
When testing the IC on an application board, connecting a capacitor to a pin with low impedance subjects the IC to stress. Always discharge capacitors after each process or step. Ground the IC during assembly steps as an antistatic measure, and use similar caution when transporting or storing the IC. Always turn the IC's power supply off before connecting it to or removing it from a jig or fixture during the inspection process.

7) Ground wiring patterns
When using both small signal and large current GND patterns, it is recommended to isolate the two ground patterns, placing a single ground point at the application's reference point so that the pattern wiring resistance and voltage variations caused by large currents do not cause variations in the small signal ground voltage. Be careful not to change the GND wiring patterns of any external components.

8) Regarding input pin of the IC
This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P/N junctions are formed at the intersection of these P layers with the N layers of other elements to create a variety of parasitic elements.
For example, when the resistors and transistors are connected to the pins as shown in Fig.27 , a parasitic diode or a transistor operates by inverting the pin voltage and GND voltage.
The formation of parasitic elements as a result of the relationships of the potentials of different pins is an inevitable result of the IC's architecture. The operation of parasitic elements can cause interference with circuit operation as well as IC malfunction and damage. For these reasons, it is necessary to use caution so that the IC is not used in a way that will trigger the operation of parasitic elements such as by the application of voltages lower than the GND (P substrate) voltage to input and output pins.

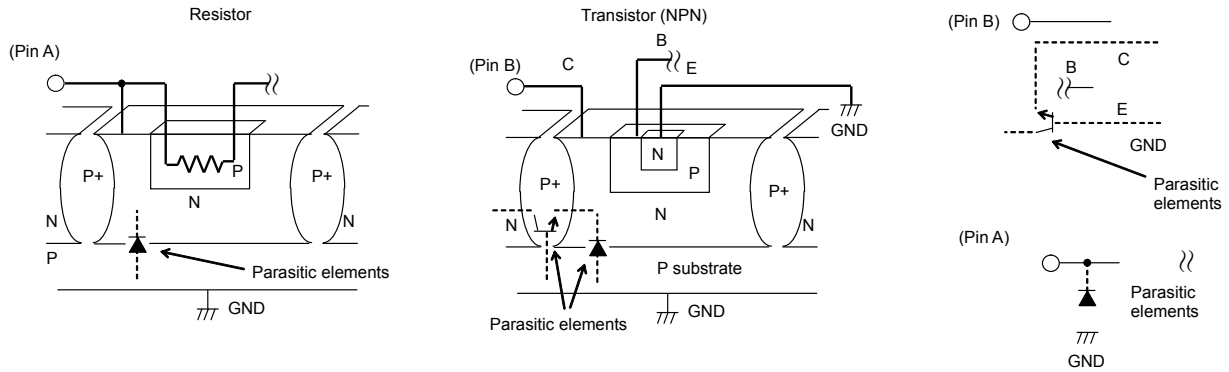


Fig.27 Example of a Simple Monolithic IC Architecture

9) Overcurrent protection circuits
An overcurrent protection circuit designed according to the output current is incorporated for the prevention of IC damage that may result in the event of load shorting. This protection circuit is effective in preventing damage due to sudden and unexpected accidents. However, the IC should not be used in applications characterized by the continuous operation or transitioning of the protection circuits. At the time of thermal designing, keep in mind that the current capacity has negative characteristics to temperatures.

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10) Thermal shutdown circuit (TSD)
This IC incorporates a built-in TSD circuit for the protection from thermal destruction. The IC should be used within the specified power dissipation range. However, in the event that the IC continues to be operated in excess of its power dissipation limits, the attendant rise in the chip's junction temperature Tj will trigger the TSD circuit to turn off all output power elements. Operation of the TSD circuit presumes that the IC's absolute maximum ratings have been exceeded. Application designs should never make use of the TSD circuit.

11) Testing on application boards
At the time of inspection of the installation boards, when the capacitor is connected to the pin with low impedance, be sure to discharge electricity per process because it may load stresses to the IC. Always turn the IC's power supply off before connecting it to or removing it from a jig or fixture during the inspection process. Ground the IC during assembly steps as an antistatic measure, and use similar caution when transporting or storing the IC.

12) EN control speed
Chattering happens if standing lowering speed is slow when standing of EN pin is lowered. The reverse current in which the input side and the pressure operation are done from the output side is generated when chattering operates with the output voltage remained, and there is a case to destruction. Please set to stand within 100μs when you control ON/OFF by the EN signal.

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●Ordering part number

B	D	9	3	2	9	A	E	F	J	-	E	2

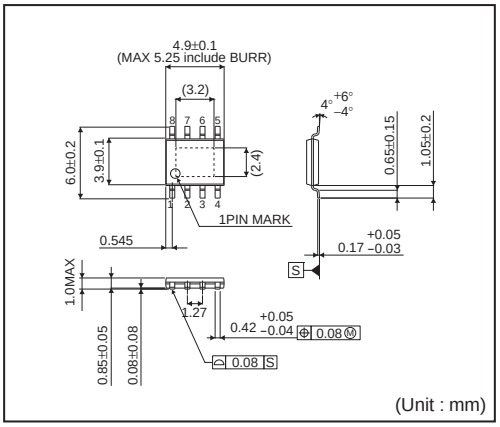
Part No. (BD)

Part No. (9329A)

Package
EFJ: HTSOP-J8

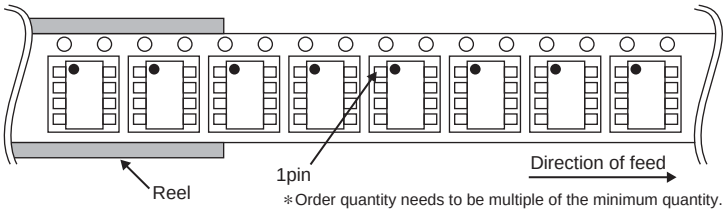
Packaging and forming specification
E2: Embossed tape and reel

HTSOP-J8



<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



∗Order quantity needs to be multiple of the minimum quantity.

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