PRELIMINARY

1024-Bit Serial (3V and 5V) Electrically Erasable PROM

FEATURES

- State-of-the-art Architecture
  - Non-volatile data storage
  - 3V to 5V operation
  - 1024, accessed in 16-bit registers
  - Auto-increment of register address, for continuous READ
- Hardware and Software Write Protection
  - Defaults to write-disabled state at power up
  - Pin-enabled writes to memory and Protect Register
  - Software instructions for write-enable/disable
  - Temporary or permanent protection of selected registers
- Low Power Consumption
  - 1mA active (typical)
  - 1μA standby (typical)
- Advanced Low Voltage CMOS EEPROM Technology
- Versatile, easy-to-use Interface
  - Self-timed programming cycle
  - Automatic erase-before-write
  - Programming Status Indicator
- Durable and Reliable
  - 10-year data retention
  - Up to 100,000 write cycles

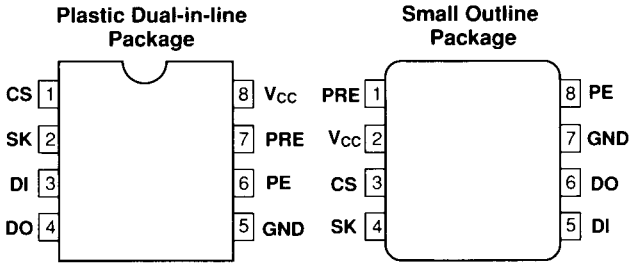
OVERVIEW

The BR93CS46 is a 16-bit serial EEPROM. The device provides 64,16-bit registers. Any number of the registers can be protected against data modification by programming the on-chip Protect Register. This register holds the address of the lowest memory register to be protected. The value in the Protect Register can be frozen, ensuring that the selected range of registers can never be altered.

The READ instruction uses an address pointer that automatically increments when all 16 bits in one register have been clocked out. If clocking continues, successive registers are accessed, allowing the BR93CS46 memory to function as non-volatile shift registers. Data can be read as a continuous data stream or as individual registers, providing from 16 to 1024 bits.

The self-timed write cycle (one register per write) includes an automatic erase-before-write capability. To protect against inadvertent writes, the WRITE instruction is accepted only while Program Enable (PE) is held HIGH, and only functions if the selected address is less than the address in the Protect Register. Data is written 16 bits per instruction, into the selected register. If Chip Select (CS) is brought HIGH after initiation of the write cycle, the Data Output (DO) pin will indicate the READY/BUSY status of the chip.

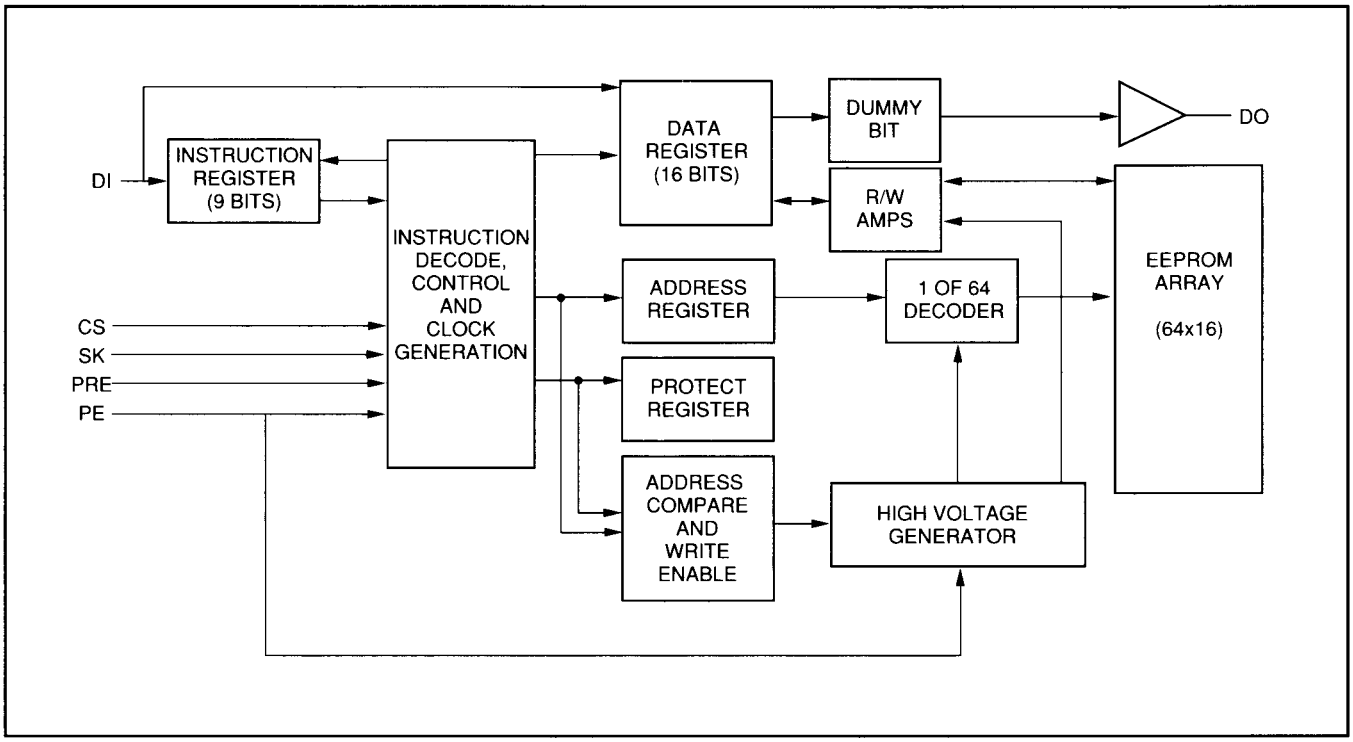
PIN CONFIGURATIONS



PIN NAMES

CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
GND	Ground
PE	Program Enable
PRE	Protect Register Enable
Vcc	Power Supply

BLOCK DIAGRAM



APPLICATIONS

The BR93CS46 is ideal for high volume applications requiring low power and low density storage. This device uses a low cost, space saving 8-pin package. Candidate applications include robotics, alarm devices, electronic locks, meters and instrumentation settings.

ENDURANCE AND DATA RETENTION

The BR93CS46 is designed for applications requiring up to 100,000 write cycles. It provides 10 years of secure data retention, with or without power applied.

ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range.....-40 to +85°C
Storage Temperature.....-65 to +125°C
Voltage with Respect to Ground.....-0.3 to +6.5V

NOTE: These are STRESS ratings only. Appropriate conditions for operating these devices are given elsewhere in this specification. Stresses beyond those listed here may permanently damage the part. Prolonged exposure to maximum ratings may affect device reliability.

DEVICE OPERATION

The BR93CS46 is controlled by twelve 9-bit instructions. Instructions are clocked in (serially) on the DI pin. Each instruction begins with a logical "1" (the start bit). This is followed by the opcode (2-bits), the address field (6-bits), and data, if appropriate.

Read (READ)

The READ instruction causes data to be output serially on the DO pin. Data is transferred from the selected memory register into a 16-bit serial-out shift register. A dummy bit (logical "0") precedes the actual output string. The data on the DO pin changes with the LOW to HIGH transition of the SK clock. If CS remains HIGH, the address pointer automatically cycles to the next higher register address, giving a continuous string of outputdata depending on the device and the starting address. (See Figure 3.)

Write Enable (WEN)

The write enable (WEN) instruction must be executed before any device programming can be done. When V_{CC} is applied to the part, it "powers up" in the Write Disable (WDS) state. Therefore, all programming modes must be preceded by a Write Enable (WEN) instruction. Once a Write Enable instruction is executed programming remains enabled until a Write Disable (WDS) instruction is executed or V_{CC} is removed from the part.

Write (WRITE)

The WRITE instruction includes 16 bits of data to be written into the specified register. After the last data bit has been applied to DI, and before the next rising edge of SK, CS must be brought LOW. (The falling edge of CS initiates the self-timed programming cycle.) Before a WRITE instruction can be executed, the device must be write enabled (see WEN). While the WRITE instruction is being loaded, the PE pin must be held HIGH; then it becomes a DON'T-CARE.

After a minimum wait of 250ns (tCS), if CS is brought HIGH, D0 will indicate the READY/BUSY status of the chip: logical "0" means programming is still in progress; logical "1" means the selected register has been written, and the part is ready for another instruction. (See Figure 5.)

INSTRUCTION SET

Instruction	Start Bit	OP Code	Address	Input Data	PRE Pin	PE Pin
READ	1	10	(A5-A0)		0	X
WEN (Write Enable)	1	00	11XXXX		0	1
WRITE	1	01	(A5-A0)	D15-D0	0	1
WRALL (Write All Registers)	1	00	01XXXX	D15-D0	0	1
WDS (Write Disable)	1	00	00XXXX		0	X
PRREAD (Protect Register Read)	1	10	XXXXXX		1	X
PREN (Protect Register Enable)	1	00	11XXXX		1	1
PRCLEAR (Protect Register Clear)	1	11	111111		1	1
PRWRITE (Protect Register Write)	1	01	(A5-A0)		1	1
PRDS (Protect Register Disable)	1	00	000000		1	1
ERASE	1	11	(A5-A0)		0	1
ERAL (Erase All Registers)	1	00	10XXXX		0	1

Write All (WRALL)
The write all (WRALL) instruction programs all registers with the data pattern specified in the instruction. The WRALL instruction functions only when the Protect Register has been cleared by a PRCLEAR instruction. While the WRALL instruction is being loaded, the PE pin must be held HIGH; then it becomes a DON'T-CARE. (See Figure 6.)

As with the WRITE instruction, if CS is brought HIGH after a minimum wait of 250ns (tCS), the DO pin indicates the READY/BUSY status of the chip. (See Figure 6.)

Write Disable (WDS)
The write disable (WDS) instruction disables all programming capabilities. This protects the entire part against accidental modification of data until a WEN instruction is executed. (When Vcc is applied, this part powers up in the write disabled state).To protect data, a WDS instruction should be executed upon completion of each programming operation. (NOTE: Neither the WEN nor the WDS instruction has any effect on the READ instruction.) (See Figure 7.)

Protect Register Read (PRREAD)
The protect register read (PRREAD) instruction causes the address stored in the Protect Register to be output on the DO pin. Data is transferred from the Protect Register into a serial-out shift register. A dummy bit (logical "0") precedes the actual output string. The data on the DO pin changes with the LOW to HIGH transition of the SK clock. While the PRREAD instruction is being loaded, the PRE pin must be held HIGH; then it becomes a DON'T-CARE. (See Figure 8.)

After a PRCLEAR instruction is executed, a PRREAD instruction will return all 1's, even though the highest register is NOT protected.

Protect Register Enable (PREN)
The protect register enable (PREN) instruction enables execution of the PRCLEAR, PRWRITE and PRDS instructions. It must be executed immediately before each of these instructions. (The PREN instruction functions only if the part has been write enabled; see the WEN instruction). Both the PRE and PE pins must be held HIGH while the PREN instruction is being loaded; then they become DON'T-CAREs. (See Figure 9.)

Protect Register Clear (PRCLEAR)
The protect register clear (PRCLEAR) instruction clears the address stored in the Protect Register, making all registers accessible to the WRITE and WRALL instructions. If a PRDS instruction has been executed, the PRCLEAR instruction will not function. A PREN instruction must be executed immediately before a PRCLEAR instruction. While the PRCLEAR instruction is being loaded, the PRE and PE pins must be held HIGH; then they become DON'T-CAREs.

As with the WRITE instruction, if CS is brought HIGH after a minimum wait of 250ns (tCS), the DO pin indicates the READY/BUSY status of the chip. (See Figure10.)

Protect Register Write (PRWRITE)
The protect register write (PRWRITE) instruction is used to load the Protect Register with the address of the lowest register to be protected. After the PRWRITE instruction is executed, only registers with addresses less than the address in the Protect Register can be written by the WRITE instruction. The Protect Register must have been cleared (see the PRCLEAR instruction) before executing a PRWRITE instruction. A PREN instruction must be executed immediately before the PRWRITE instruction. While the PRWRITE instruction is being loaded, the PRE and PE pins must be held HIGH; then they become DON'T-CAREs.

As with the WRITE instruction, if CS is brought HIGH after a minimum wait of 250ns (tCS), the DO pin indicates the READY/BUSY status of the chip. (See Figure 11.)

Protect Register Disable (PRDS)
The protect register disable (PRDS) instruction is effective exactly once per part. After this instruction has been executed, the Protect Register will accept no further modifications. All registers with addresses greater than or equal to the address in the Protect Register are permanently protected from the WRITE and WRALL operations. A PREN instruction must be executed immediately before the PRDS instruction. While the PRDS instruction is being loaded, the PRE and PE pins must be held HIGH; then they become DON'T-CAREs.

As with the WRITE instruction, if CS is brought HIGH after a minimum wait of 250ns (tCS), the DO pin indicates the READY/BUSY status of the chip. (See Figure 12.)

Erase Register
After the erase instruction is entered, CS must be brought low. The falling edge of CS initiates the self-timed internal programming cycle. Bringing CS HIGH after a minimum of tCS, will cause DO to indicate the READ/BUSY status of the chip: a logical "0" indicates programming is still in progress; a logical "1" indicates the erase cycle is complete and the part is ready for another instruction. Registers protected by the protect register write (PRWRITE) or protect register disable (PRDS) commands cannot be erased. (See Figure 13.)

Erase All (ERAL)
Full chip erase is provided for ease of programming. Erasing the entire chip involves setting all bits in the entire memory array to a logical "1". The erase all (ERAL) command will not erase registers protected by the protect register write (PRWRITE) or protect register disable (PRDS) commands. (See Figure 14.)

ABSOLUTE MAXIMUM RATINGS

Temperature under bias — BR93CS46-3/BR93CS46F = 0° TO +70°C
— BR93CS46-3E/BR93CS46F-E = -40° TO +85°C

DC ELECTRICAL CHARACTERISTICS

Vcc = 3 V ±10%

Symbol	Parameter	Conditions	93CS46-3		93CS46-3E		Units
			Min	Max	Min	Max	
I_{CC1}	Operating Current	CS = V_{IH}, SK = 1KHz CMOS Input Levels		2		2	mA
I_{CC2}	Operating Current	CS = V_{IH}, SK = 1KHz TTL Input Levels		3		3	mA
I_{CC3}	Standby Current	PRE = CS = 0V DI = SK = PE = Vcc		2		2	µA
I_{IL}	Input Leakage	V_{IN} = 0V to Vcc	-10.0	10.0	-20.0	20.0	µA
I_{OL}	Output Leakage	V_{OUT} = 0V to Vcc	-1	1	-1	1	µA
V_{IL}	Input Low Voltage		-0.1	0.15Vcc		0.15 Vcc	V
V_{IH}	Input High Voltage		0.8 Vcc	Vcc	0.8 Vcc	Vcc	V
V_{OL2}	Output Low Voltage	I_{OL} = 1.0mA CMOS		0.3		0.3	V
V_{OH2}	Output High Voltage	I_{OH} = -10µA CMOS	Vcc-0.2		Vcc-0.2		V

AC ELECTRICAL CHARACTERISTICS

Vcc = 3 V ±10%

Symbol	Parameter	Conditions	93CS46-3		93CS46-3E		Units
			Min	Max	Min	Max	
f_{SK}	SK Clock Frequency		0	250	0	250	KHz
t_{SKH}	SK High Time		1		1		µs
t_{SKL}	SK Low Time		1		1		µs
t_{CS}	Minimum CS Low Time		1		1		µs
t_{CSS}	CS Setup Time	Relative to SK	200		200		ns
t_{PRES}	PRE Setup Time	Relative to SK	200		200		ns
t_{PES}	PE setup Time	Relative to SK	200		200		ns
t_{DIS}	DI Setup Time	Relative to SK	400		400		ns
t_{CSH}	CS Hold Time	Relative to SK	0		0		ns
t_{PEH}	PE Hold Time	Relative to CS	200		200		ns
t_{PREH}	PRE Hold Time	Relative to CS	200		200		ns
t_{DIH}	DI Hold Time	Relative to SK	400		400		ns
t_{PD1}	Output Delay to "1"	AC Test		2		2	µs
t_{PD0}	Output Delay to "0"	AC Test		2		2	µs
t_{SV}	CS to Status Valid	AC Test		2		2	µs
t_{DF}	CS to DO in 3-state	CS = V_{IL}		400		400	ns
t_{WP}	Write Cycle Time			20		20	ms

ABSOLUTE MAXIMUM RATINGS

Temperature under bias — BR93CS46/BR93CS46F = 0° TO +70°C
— BR93CS46-E/BR93CS46F-E = -40° TO +85°C

DC ELECTRICAL CHARACTERISTICS

Vcc = 5V ±10%

Symbol	Parameter	Conditions	93CS46		93CS46-E		Units
			Min	Max	Min	Max	
I_{CC1}	Operating Current	CS = V_{IH}, SK = 1MHz CMOS Input Levels		2		2	mA
I_{CC2}	Operating Current	CS = V_{IH}, SK = 1MHz TTL Input Levels		5		5	mA
I_{CC3}	Standby Current	PRE = CS = 0V DI = SK = PE = Vcc		2		2	µA
I_{IL}	Input Leakage	V_{IN} = 0V to Vcc	-10.0	10.0	-10.0	1.0	µA
I_{OL}	Output Leakage	V_{OUT} = 0V to Vcc	-10.0	10.0	-10.0	10.0	µA
V_{IL}	Input Low Voltage		-0.1	0.8	-0.1	0.8	V
V_{IH}	Input High Voltage		2	Vcc	2	Vcc	V
V_{OL1}	Output Low Voltage	I_{OL} = 2.1mA TTL		0.4		0.4	V
V_{OH1}	Output High Voltage	I_{OH} = -400µA TTL	2.4		2.4		V
V_{OL2}	Output Low Voltage	I_{OL} = 10µA CMOS		0.2		0.2	V
V_{OH2}	Output High Voltage	I_{OH} = -10µA CMOS	Vcc-0.2		Vcc-0.2		V

AC ELECTRICAL CHARACTERISTICS

Vcc = 5V ±10%

Symbol	Parameter	Conditions	93CS46		93CS46-E		Units
			Min	Max	Min	Max	
f_{SK}	SK Clock Frequency		0	1	0	1	MHz
t_{SKH}	SK High Time		400		400		ns
t_{SKL}	SK Low Time		250		250		ns
t_{CS}	Minimum CS Low Time		250		250		ns
t_{CSS}	CS Setup Time	Relative to SK	50		50		ns
t_{PRES}	PRE Setup Time	Relative to SK	50		50		ns
t_{PES}	PE setup Time	Relative to SK	50		50		ns
t_{DIS}	DI Setup Time	Relative to SK	100		100		ns
t_{CSH}	CS Hold Time	Relative to SK	0		0		ns
t_{PEH}	PE Hold Time	Relative to CS	50		50		ns
t_{PREH}	PRE Hold Time	Relative to CS	50		50		ns
t_{DIH}	DI Hold Time	Relative to SK	100		100		ns
t_{PD1}	Output Delay to "1"	AC Test		500		500	ns
t_{PD0}	Output Delay to "0"	AC Test		500		500	ns
t_{SV}	CS to Status Valid	AC Test		500		500	ns
t_{DF}	CS to DO in 3-state	CS = V_{IL}		100		100	ns
t_{WP}	Write Cycle Time			10		10	ms

CAPACITANCE

TA = 25°C, f = 1MHz

Symbol	Parameter	Max	Units
C_{OUT}	Output Capacitance	5	pF
C_{IN}	Input Capacitance	5	pF

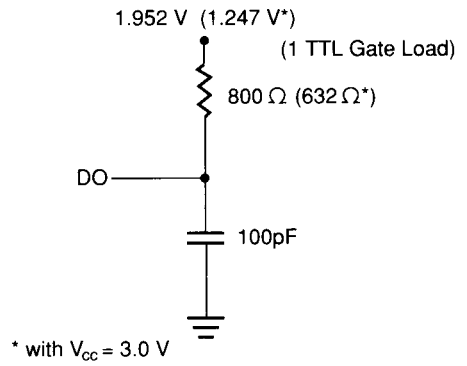


FIGURE 1. AC TEST CONDITIONS

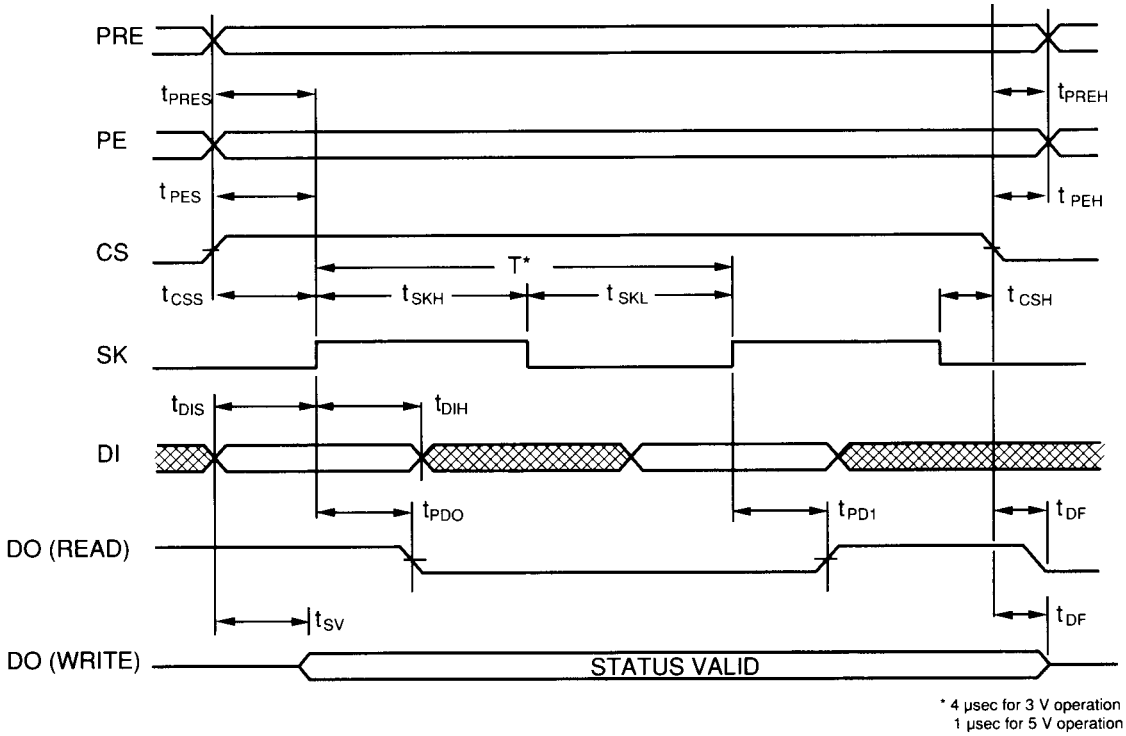
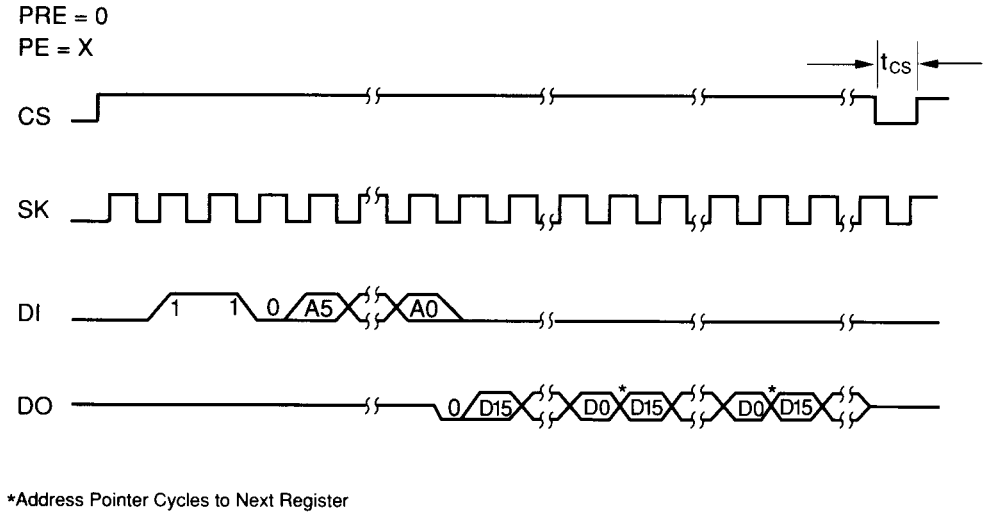
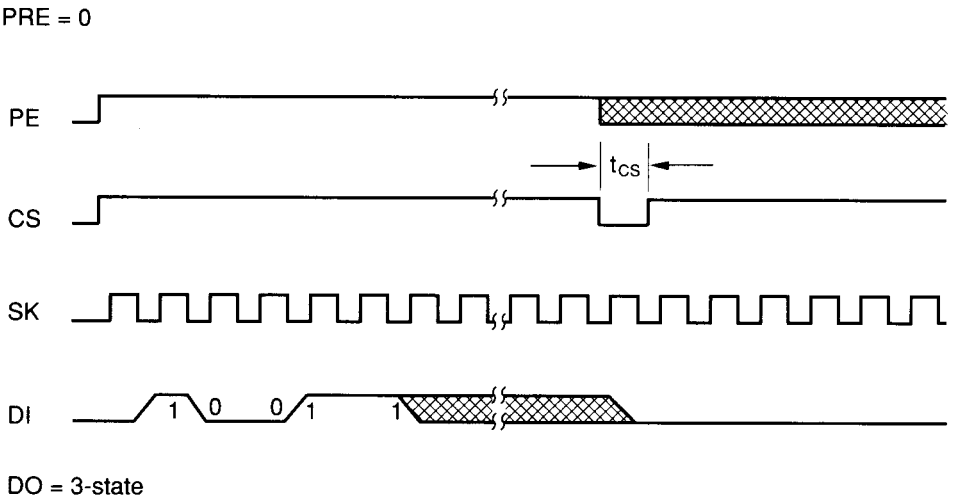


FIGURE 2. SYNCHRONOUS DATA TIMING



*Address Pointer Cycles to Next Register

FIGURE 3. READ CYCLE TIMING



DO = 3-state

FIGURE 4. WRITE ENABLE (WEN) CYCLE TIMING

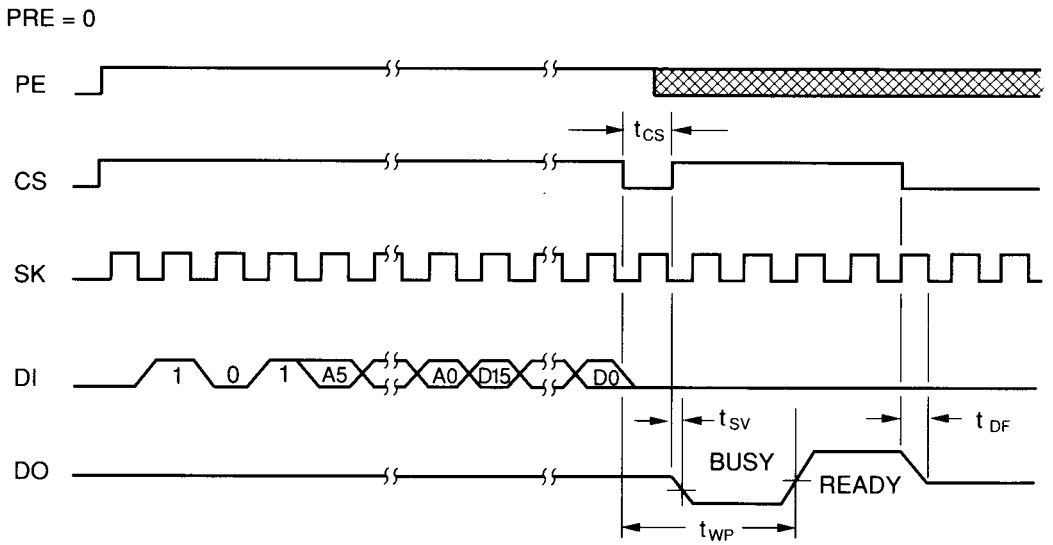


FIGURE 5. WRITE CYCLE TIMING

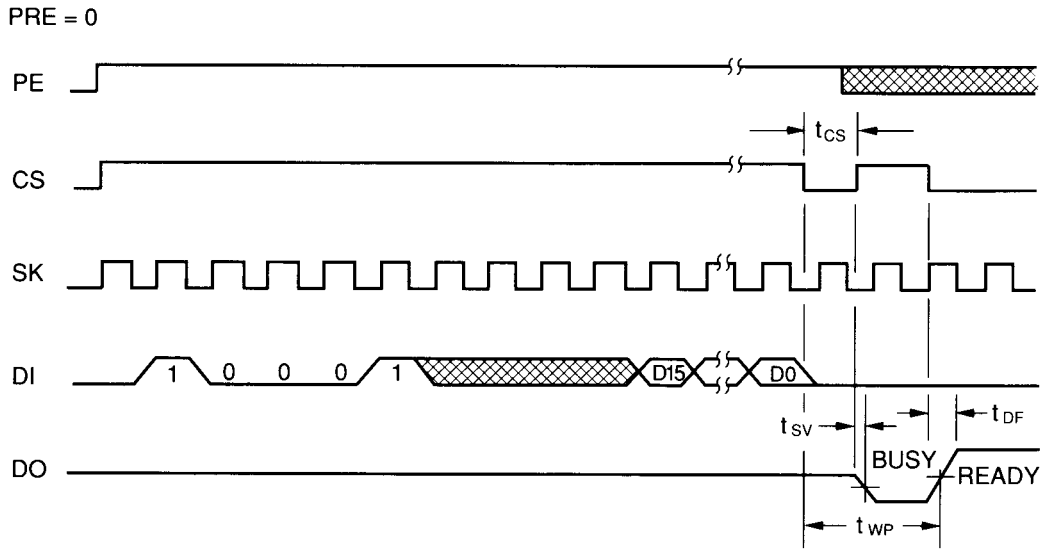


FIGURE 6. WRITE ALL (WRALL) CYCLE TIMING

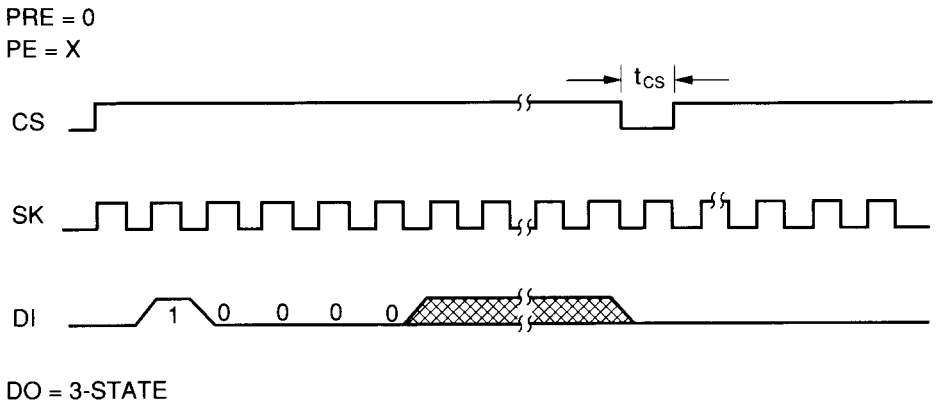


FIGURE 7. WRITE DISABLE (WDS) CYCLE TIMING

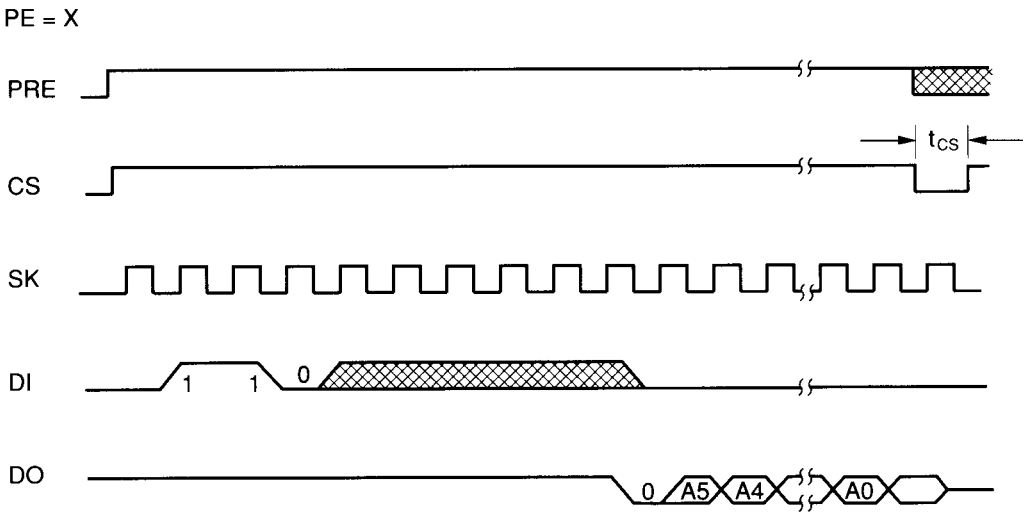


FIGURE 8. PROTECT REGISTER READ (PRREAD) CYCLE TIMING

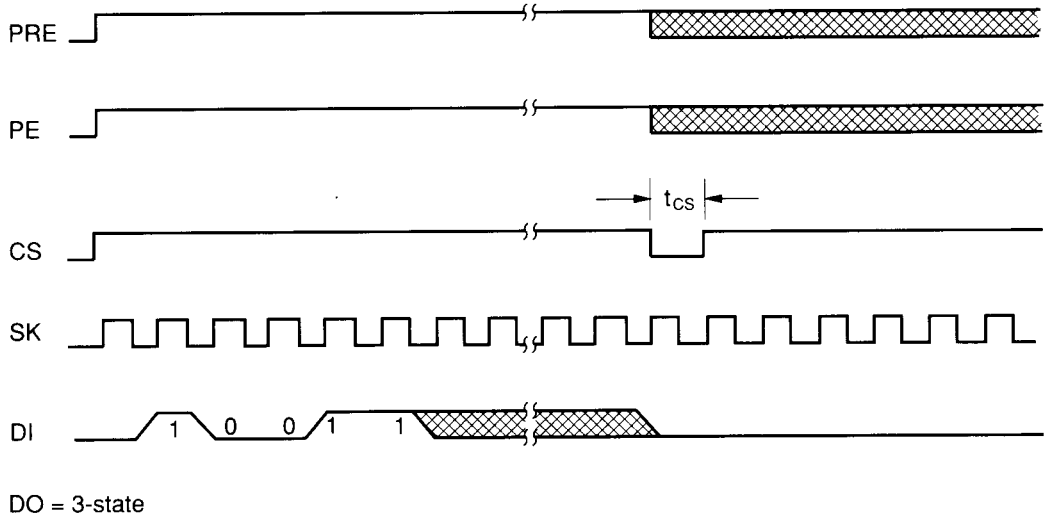


FIGURE 9. PROTECT REGISTER ENABLE (PREN) CYCLE TIMING

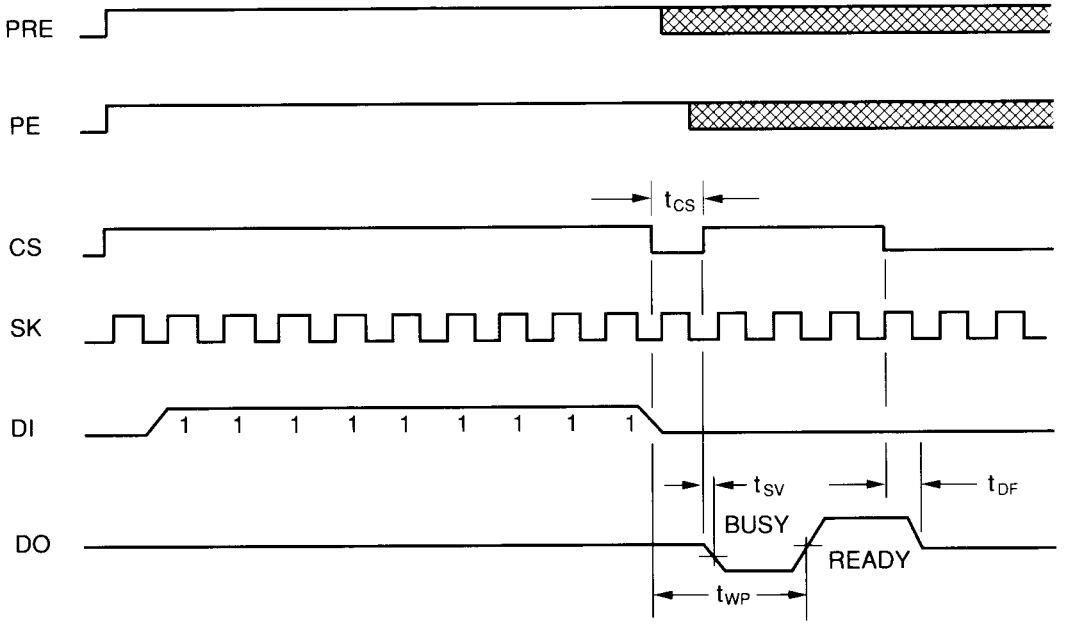


FIGURE 10. PROTECT REGISTER CLEAR (PRCLEAR) CYCLE TIMING

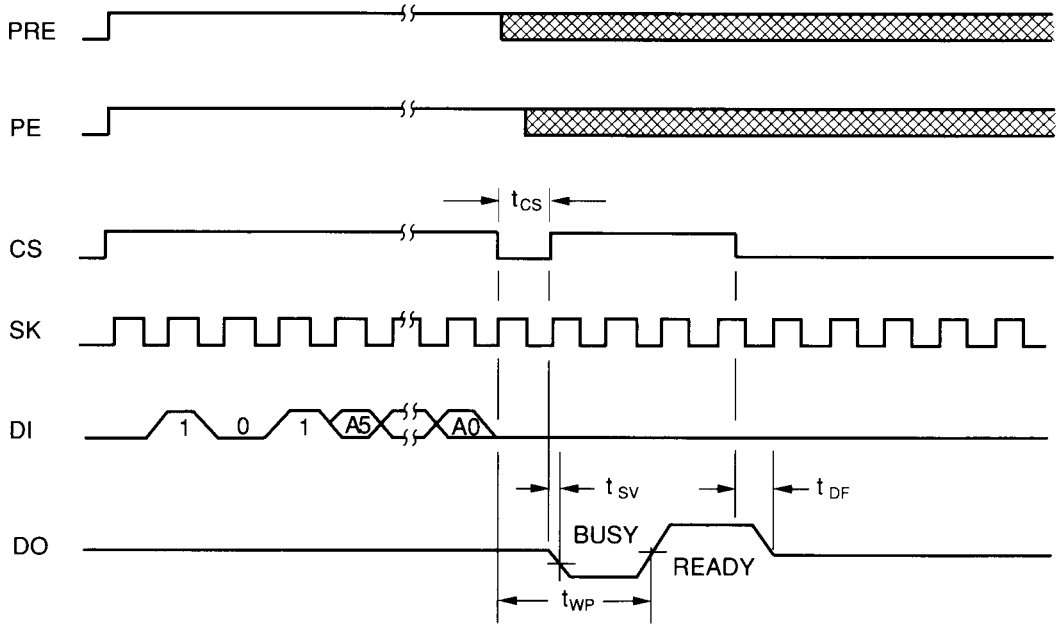


FIGURE 11. PROTECT REGISTER WRITE (PRWRITE) CYCLE TIMING

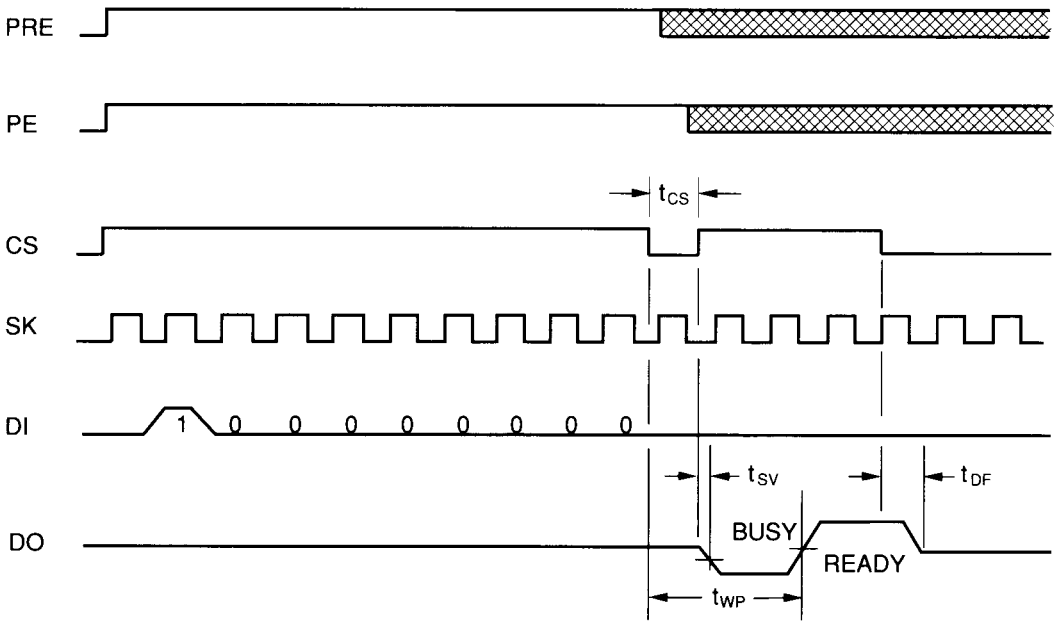


FIGURE 12. PROTECT REGISTER DISABLE (PRDS) CYCLE TIMING

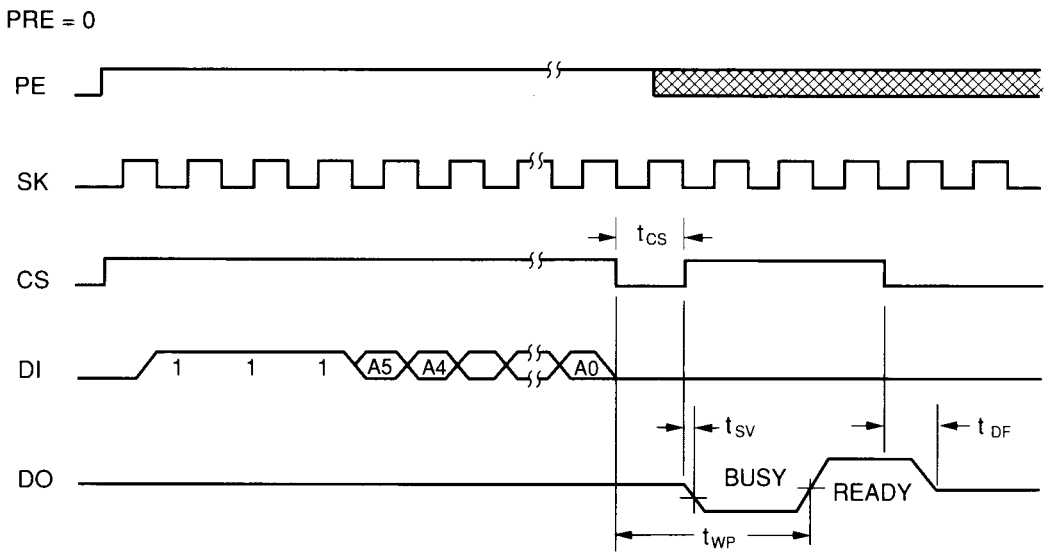


FIGURE 13. Erase (Register) Cycle Timing

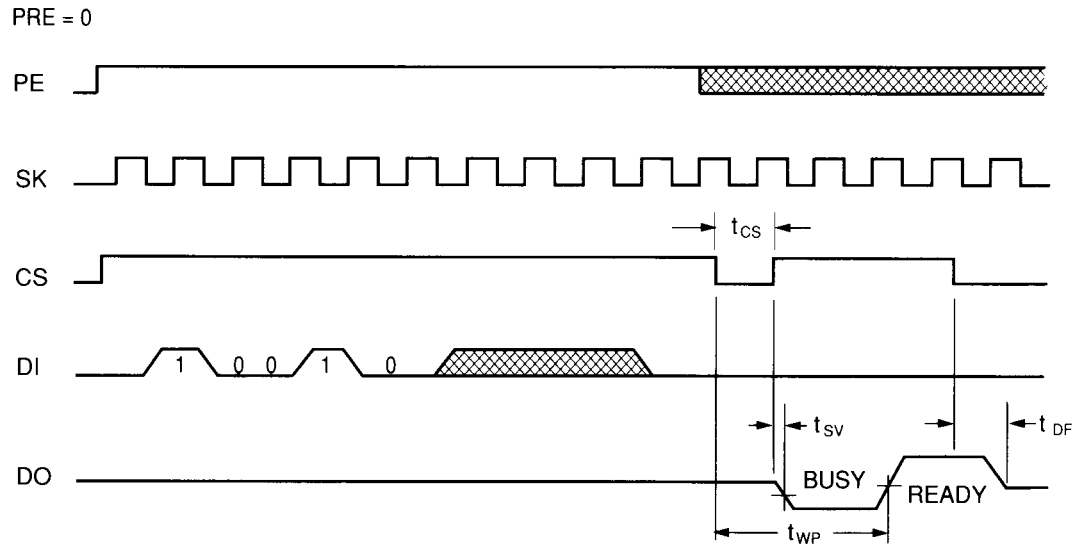


FIGURE 14. Erase All Cycle Timing

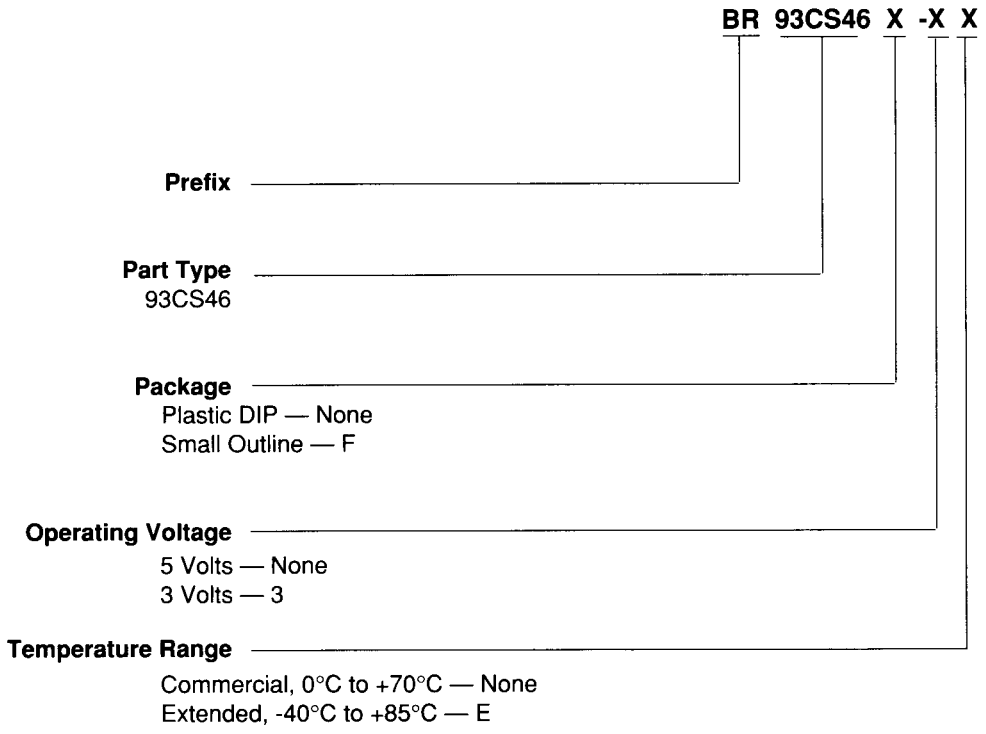
ORDERING INFORMATION

Standard Configurations

Prefix	Part Type	Package Type	Operating Voltage	Operating Teperature
BR	93CS46	PDIP, SOIC	5V, 3V	Commercial Industrial

*CONTACT ROHM FOR YOUR SPECIAL TEMPERATURE AND PACKAGING REQUIREMENTS

Part Numbers:



NOTE: SOIC extended temperature package marking is a white dot.

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