LP2273 Data Sheet

LP2273

【SWITCHING MODE POWER SUPPLY】

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CONTENTS

Description

LP2273 is a highly integrated current mode PWM control IC optimized for high performance, low standby power and cost effective offline flyback converter applications.

PWM switching frequency at normal operation is internally fixed and is trimmed to tight range. At no load or light load condition, the IC operates in extended 'burst mode' to minimize switching loss. Lower standby power and higher conversion efficiency is thus achieved.

VDD low startup current and low operating current contribute to reliable power on startup and low standby design with LP2273.

LP2273 offers complete coverage with auto-recovery including Cycle-by-Cycle current limiting (OCP), over load protection (OLP), and VDD under voltage lockout (UVLO). It also provides the protections without latched shut down including over temperature protection (OTP), and over voltage (fixed or adjustable) protection (OVP). Excellent EMI performance is achieved with frequency shuffling technique.

The tone energy at below 20KHZ is minimized in the design and audio noise is eliminated during operation.

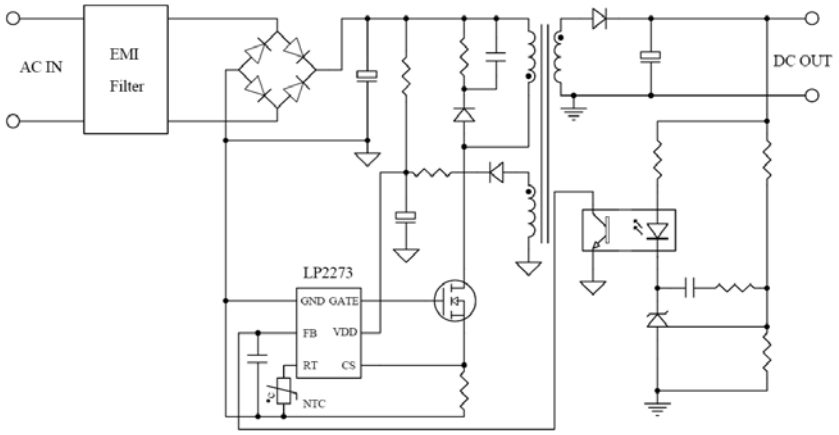


FIG 1 .TYPICAL APPLICATION

Features

- Power on Soft Start Reducing MOSFET Vds Stress
- Frequency shuffling for EMI
- Extended Burst Mode Control For Improved Efficiency and Minimum Standby Power Design
- Audio Noise Free Operation
- Fixed 65KHZ Switching Frequency
- Co mp ehensive Protection Coverage
  - VDD Under Voltage Lockout with Hysteresis(UVLO)
  - Cycle-by-Cycle over current threshold setting for constant output power limiting over universal input voltage range
  - Overload Protection (OLP) with autorecovery
  - Over Temperature Protection (OTP) without latch shut down
  - VDD Over Voltage Protection (OVP) without latch shut down
  - Adjustable OVP through external Zener

APPLICATIONS

Offline AC/DC flyback converter for

- Battery Charger
- Power Adaptor
- Set-Top Box Power Supplies
- Open-frame SMPS

Pin Configuration

LP2273 is offered in SOT23-6 package

Pin Name	I/O	Description
GND	P	Ground
FB	I	Feedback input pin. The PWM duty cycle is determined by voltage level into this pin and the current-sense signal at Pin 4.
RT	I	Dual function pin. Either connected through a NTC resistor to ground for over temperature shutdown/latch control or connected through Zener to VDD for adjustable over voltage protection.
CS	I	Current sense input
VDD	P	Power supply
GATE	O	Totem-pole gate driver output for power Mosfet.

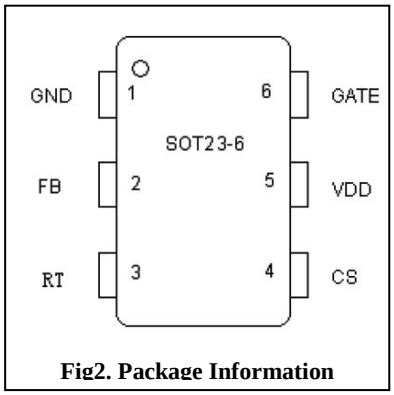


Fig2. Package Information

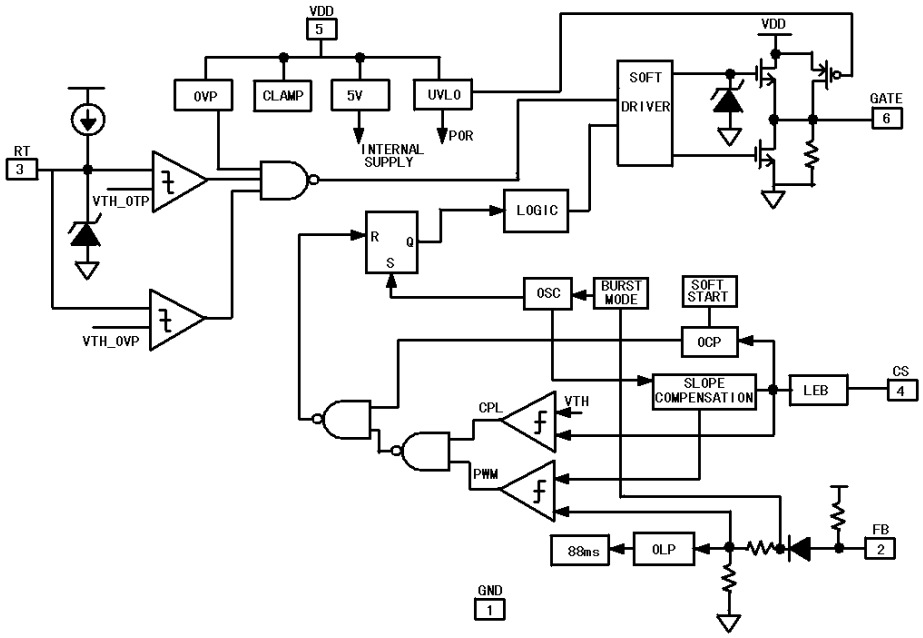


Fig 3. BLOCK DIAGRAM

OPERATION DESCRIPTION

LP2273 is a highly integrated current mode PWM control IC optimized for high performance, low standby power and cost effective offline flyback converter applications. The 'Extended burst mode' control greatly reduces the standby power consumption and helps the design easily to meet the international power conservation requirements.

Startup Current and Startup Control

Startup current of LP2273 is designed to be very low so that VDD could be charged up above UVLO threshold level and device starts up quickly. A large value startup resistor can therefore be used to minimize the power loss yet achieved reliable startup in application.

Operating Current

The operating current of LP2273 is low at 1.4mA. Good efficiency is achieved with LP2273 low operating current together with the 'Extended burst mode' control features.

Soft Start

LP2273 features an internal 4ms soft start to soften the electrical stress occurring in the power supply during startup. It is activated during the power on sequence. As soon as VDD reaches UVLO(OFF), the CS peak voltage is gradually increased from 0.15V to maximum level. Every restart up is followed by a soft start.

Frequency shuffling for EMI improvement

The frequency shuffling (switching frequency modulation) is implemented in LP2273. The oscillation frequency is modulated so that the tone energy is spread out. The spread spectrum minimizes the conduction band EMI and therefore eases the system design.

Extended Burst Mode Operation

At light load or zero load condition, most of the power dissipation in a switching mode power supply is from switching loss on the MOSFET, the core loss of the transformer and the loss on the snubber circuit. The magnitude of power loss is in proportion to the switching frequency. Lower switching frequency leads to the reduction on the power loss and thus conserves the energy.

The switching frequency is internally adjusted at no load or light load condition. The switch frequency reduces at light/no load condition to improve the conversion efficiency. At light load or no load condition, the FB input drops below burst mode threshold level and device enters Burst Mode control. The Gate drive output switches only when VDD voltage drops below a preset level and FB input is active to output an on state. Otherwise the gate drive remains at off state to minimize the switching loss and reduces the standby power consumption to the greatest extend.

The switching frequency control also eliminates the audio noise at any loading conditions.

Oscillator Operation

The switching frequency is internally fixed at 65KHZ. No external frequency setting components are required for PCB design simplification.

Current Sensing and Leading Edge Blanking

Cycle-by-Cycle current limiting is offered in LP2273 current mode PWM control. The switch current is detected by a sense resistor into the CS pin. An internal leading edge blanking circuit chops off the sensed voltage spike at initial internal power MOSFET on state due to snubber diode reverse recovery and surge gate current of power MOSFET. The current limiting comparator is disabled and cannot turn off the internal power MOSFET during the blanking period. The PWM duty cycle is determined by the current sense input voltage and the FB input voltage.

Internal Synchronized Slope Compensation

Bulilt-in slope compensation circuit adds voltage ramp onto current sense input voltage for PWM generation. It greatly improves the close loop stability at CCM and prevents the subharmonic oscillation and thus reduces the output ripple voltage.

Drive

The power MOSFET is driven by a dedicated gate drive for power switch control. Too weak the gate driver strength results in higher conduction and switch loss of MOSFET while too strong gate drive results the compromise of EMI.

A good tradeoff is achieved through the built-in totem pole gate design with right output strength and dead time control. The low idle loss and good EMI system design is easier to achieve with this dedicate control scheme.

Protection Controls

Good power supply system reliability is achieved with auto-recovery protection features including Cycle-by-Cycle current limiting (OCP), Over Load Protection (OLP), and Under Voltage Lockout on VDD (UVLO), and without latch shutdown features including Over Temperature Protection (OTP), fixed or adjustable VDD Over Voltage Protection (OVP). The OCP is line voltage compensated to achieve constant output power limit over the universal input voltage range.

At overload condition when FB input voltage exceeds power limit threshold value for more than TD_PL, control circuit reacts to shut down the converter. It restarts when FB input voltage below power limit threshold.

ABSOLUTE MAXIMUM RATINGS

VDD DC Supply Voltage…… 30V
VDD Zener Clamp Voltage……VDD_Clamp+0.1V
VDD DC Clamp Current……10mA
FB Input Voltage……-0.3V to 7V
CS Input Voltage……-0.3V to 7V
RT Input Voltage……-0.3V to 7V
Min/Max Operating Junction Temperature TJ…… -20 to 150℃
Min/Max Operating Storage Temperature Tstg…… -55 to 165℃
Lead Temperature (Soldering, 10secs)……260℃

RECOMMENDED OPERATING CONDITION

VDD Supply Voltage……10V to 23.5V
Operating Ambient Temperature……-20 to 85℃

ELECTRICAL CHARACTERISTICS

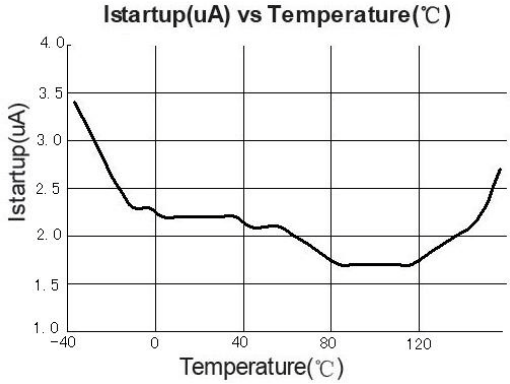
（T_A=25℃，VDD=16V，unless otherwise noted）

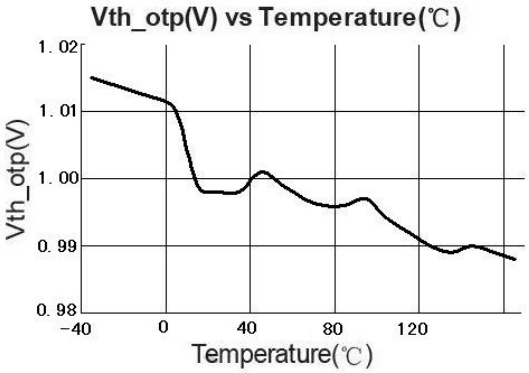
Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
Supply Voltage（VDD）						
I _Startup	VDD Start Up Current	VDD=UVLO(OFF)-1V, measure leakage current into VDD		5	20	uA
I_VDD_Ops	Operation Current	VFB=3V		1.4	2.5	mA
UVLO(ON)	VDD Under Voltage Lockout Enter		8	9	10	V
UVLO(OFF)	VDD Under Voltage Lockout Exit (Recovery)		14.5	15.5	16.5	V
Vpull_up	Pull-up PMOS active			13		V
Vdd_Clamp		IVDD=10mA	30	32	34	V
OVP(ON)	Over Voltage Protection voltage	CS=0.3V,FB=3V, Ramp up VDD until gate clock is off	26	28	30	V
Feedback Input Section（FB Pin）						
VFB_Open	VFB Open Loop Voltage		3.9	4.2		V
AVCS	PWM input gain Δ VFB/ Δ VCS			2		V/V
Maximum duty cycle	Max duty cycle @ VDD=14V, FB=3V, VCS=0.3V		75	80	85	%
Vref_green	The threshold enter green mode			1.4		V
Vref_burst_H	The threshold exit burst mode			0.675		V
Vref_burst_L	The threshold enter burst mode			0.575		V
IFB_Short	FB pin short circuit current	Short FB pin to GND and measure current		0.4		mA
VTH_PL	Power Limiting FB Threshold Voltage			3.6		V

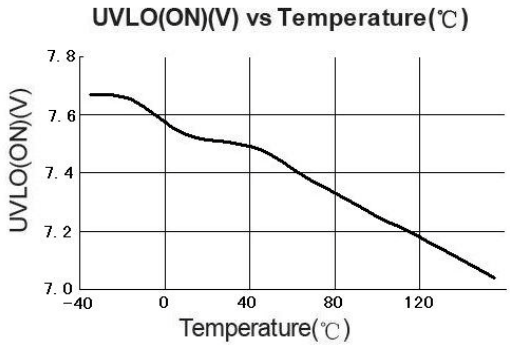
TD_PL	Power limiting Debounce Time		80	88	96	mS
ZFB_IN	Input Impedance			16		KΩ
Current Sense Input（CS pin）						
SST	Soft start time			4		ms
T_blanking	Leading edge blanking time			220		ns
T_D_OC	Over Current Detection and Control Delay	From Over Current Occurs till the Gatedriver output start to turn off		120		ns
VTH_OC	Internal Current Limiting Threshold Voltage with zero duty cycle			0.75		V
Vocp_clamping	CS voltage clamper			0.9		V
Oscillator						
Fosc	Normal Oscillation Frequency	VDD=14V, FB=3V, CS=0.3V	60	65	70	KHZ
Δf_OSC	Frequency jittering			+/-4		%
f_shuffling	Shuffling frequency			32		HZ
F_Burst	Burst Mode Switch Frequency			22		KHz
Gate Driver						
VOL	Output low level	VDD=14V，IO=6mA			1	V
VOH	Output high level	VDD=14V，IO=5mA	6			V
V_Clamping	Output clamp voltage			12		V
T_r	Output rising time 1V~12V @ CL=1000pF			175		ns
T_f	Output falling time 12V~1V @ CL=1000pF			85		ns
Over temperature protection						
IRT	Output current of RT pin		95	100	105	μA
VOTP	Threshold voltage for OTP		0.95	1	1.05	V
Td_OTP	OTP debounce time			32		Cycle
VRT_FL	Float voltage at RT pin			2.3		V
Vth_OVP	External OVP threshold voltage			4.0		V

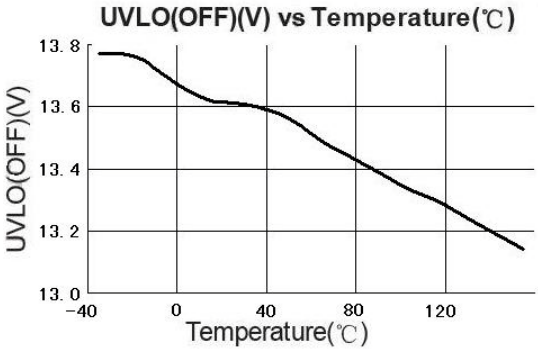
CHARACTERIZATION PLOTS

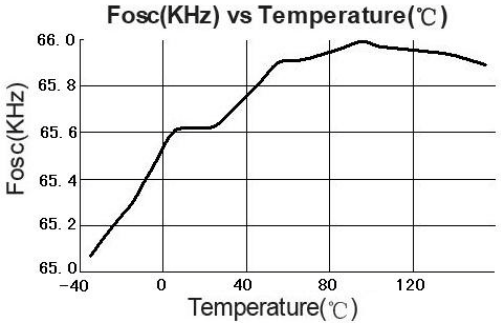
VDD=18V, TA=25℃ condition applies if not otherwise noted.

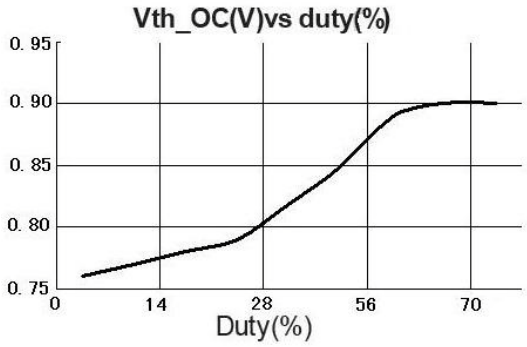






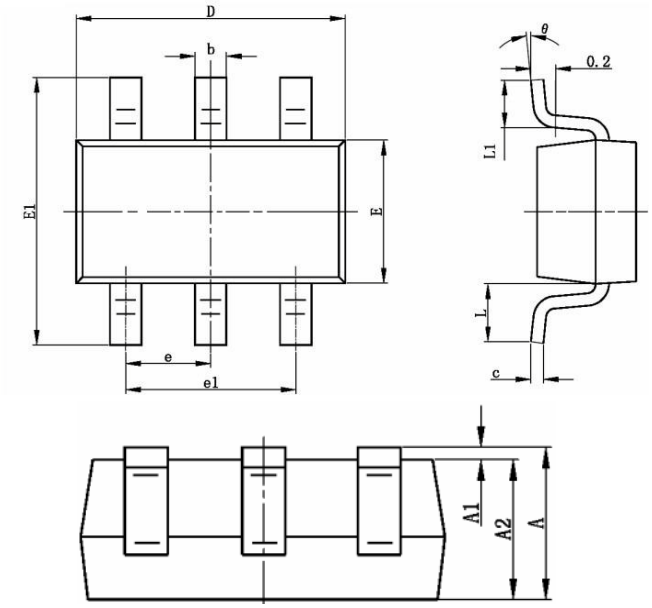






PACKAGE MECHANACAL DATA

SOT-23-6 PACKAGE OUTLINE DIMENSIONS



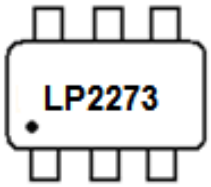
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.400	0.012	0.016
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950TYP		0.037TYP	
e1	1.800	2.000	0.071	0.079
L	0.700REF		0.028REF	
L1	0.300	0.600	0.012	0.024
θ	0^0	8^0	0^0	8^0

Package Dissipation Rating

Package	RθJA (°C/W)
SOT23-6	200

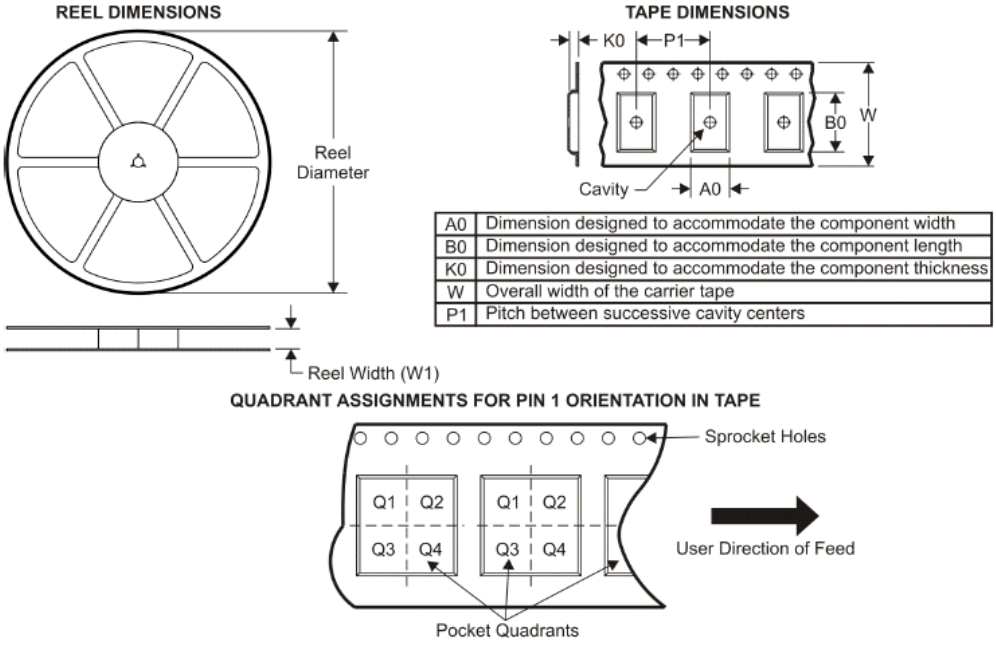
Marking Information

SOT23-6



芯片正面打印： LP2273

Packaging Information



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

Standard Size

Device	Package Type	Pins	SPQ	Reel Diammeter (mm)	Reel Width W1(mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP2273	SOT-23	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3