Atmel AT34C02D

I²C-compatible (2-wire) Serial EEPROM with Permanent and Reversible Software Write Protection
2K (256 x 8)

DATASHEET

Features

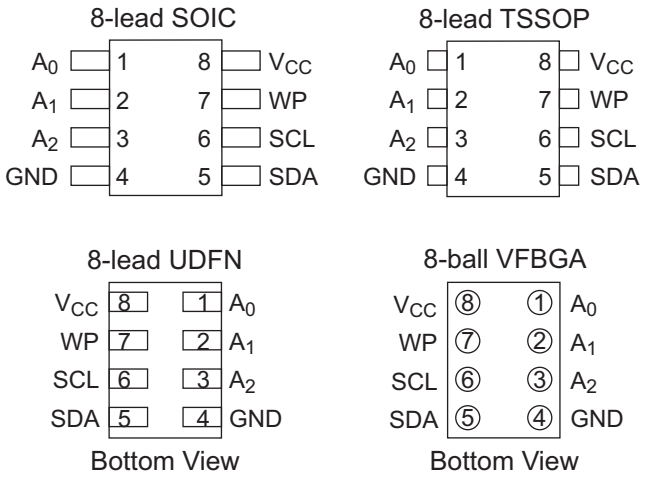
- Permanent and reversible software write protection for the first-half of the array
  - Software procedure to verify write protect status
- Hardware write protection for the entire array
- Low-voltage and standard-voltage operation
  - V_{CC} = 1.7V to 5.5V
- Internally organized 256 x 8
- 2-wire serial interface
- Schmitt Trigger, filtered inputs for noise suppression
- Bidirectional data transfer protocol
- 400kHz (1.7V) and 1MHz (2.5V and 5.0V) compatibility
- 16-byte page write modes
- Partial page writes are allowed
- Self-timed write cycle (5ms max)
- High-reliability
  - Endurance: 1 million write cycles
  - Data retention: 100 years
- 8-lead JEDEC SOIC, 8-lead TSSOP, 8-lead UDFN (MLP 2x3), and 8-ball VFBGA packages
- Die sales: wafer form, tape and reel, and bumped wafers

Description

The Atmel® AT34C02D provides 2048 bits of serial electrically-erasable and programmable read only memory (EEPROM) organized as 256 words of 8 bits each. The first-half of the device incorporates a permanent and a reversible software write protection feature while hardware write protection for the entire array is available via an external pin. Once the permanent software write protection is enabled, by sending a special command to the device, it cannot be reversed. However, the reversible software write protection is enabled and can be reversed by sending a special command. The hardware write protection is controlled by the WP pin state and can be used to protect the entire array regardless of whether or not the software write protection has been enabled. The software and hardware write protection features allow the user the flexibility to protect none, first-half, or the entire memory array depending on the specific needs of the application. The device is optimized for use in many industrial and commercial applications where low-power and low-voltage operations are essential. The AT34C02D is available in space saving 8-lead JEDEC SOIC, 8-lead TSSOP, 8-lead UDFN (MLP 2x3), and 8-ball VFBGA packages and is accessed via an I²C-compatible 2-wire serial interface. The AT34C02D operates over a wide V_{CC} range, from 1.7V to 5.5V.

Figure 1. Pin Configurations

Pin Name	Function
A_0 - A_2	Address Inputs
GND	Ground
SDA	Serial Data
SCL	Serial Clock Input
WP	Write Protect
V_{CC}	Power Supply

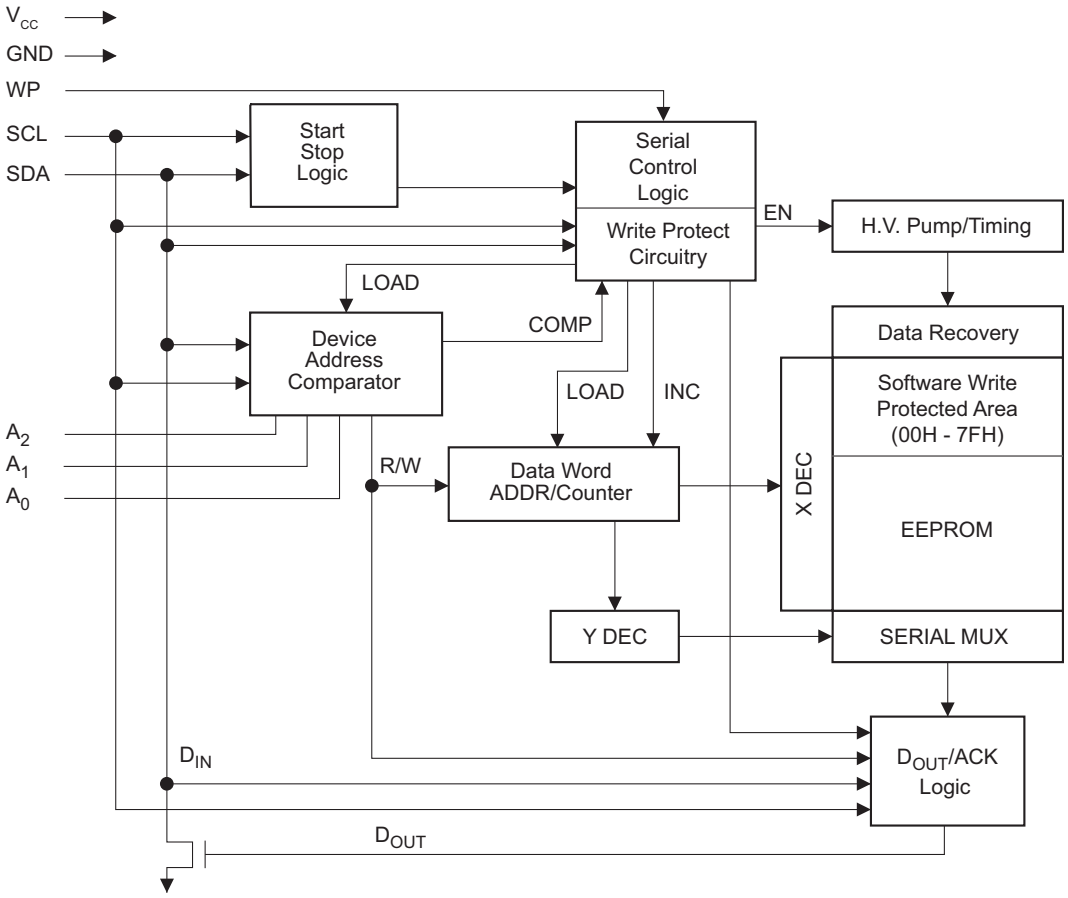


1. Absolute Maximum Ratings*

Operating Temperature	–55°C to +125°C
Storage Temperature	–65°C to +150°C
Voltage on any pin with respect to ground	–1.0V to +7.0V
Maximum Operating Voltage	6.25V
DC Output Current	5.0mA

*Notice: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 1-1. Block Diagram



2. Pin Description

Serial Clock (SCL): The SCL input is used to positive edge clock data into each EEPROM device and negative edge clock data out of each device.

Serial Data (SDA): The SDA pin is bidirectional for serial data transfer. This pin is open-drain driven and may be wire-ORed with any number of other open-drain or open collector devices.

Device Addresses (A_2, A_1, and A_0): The A_2, A_1, and A_0 pins are device address inputs that are hardwired (directly to GND or to Vcc) for compatibility with other Atmel AT24Cxx devices. When the pins are hardwired, as many as eight 2K devices may be addressed on a single bus system. See Section 5. “Device Addressing” on page 10 for more details. A device is selected when a corresponding hardware and software match is true. If these pins are left floating, the A_2, A_1, and A_0 pins will be internally pulled down to GND. However, due to capacitive coupling that may appear during customer applications, Atmel recommends always connecting the address pins to a known state. When using a pull-up resistor, Atmel recommends using 10kΩ or less.

Write Protect (WP): The write protect input, when connected to GND, allows normal write operations. When WP is connected directly to V_{CC}, all write operations to the memory are inhibited. If the pin is left floating, the WP pin will be internally pulled down to GND. However, due to capacitive coupling that may appear during customer applications, Atmel recommends always connecting the WP pins to a known state. When using a pull-up resistor, Atmel recommends using 10kΩ or less.

Table 2-1. Atmel AT34C02D Write Protection Modes

WP Pin Status	Permanent Write Protect Register	Reversible Write Protect Register	Part of the Array Write Protected
V_{CC}	–	–	Full Array (2K)
GND or Floating	Not Programmed	Not Programmed	Normal Read/Write
GND or Floating	Programmed	–	First-half of Array (1K: 00h - 7Fh)
GND or Floating	–	Programmed	First-half of Array (1K: 00h - 7Fh)

2.1 Pin Capacitance[1]

Applicable over recommended operating range from T_A = 25°C, f = 100kHz, V_{CC} = 1.7V to 5.5V

Symbol	Test Condition	Max	Units	Conditions
$C_{I/O}$	Input/Output Capacitance (SDA)	8	pF	$V_{I/O}$ = 0V
C_{IN}	Input Capacitance (A_0, A_1, A_2, SCL)	6	pF	V_{IN} = 0V

Note: 1. This parameter is characterized and is not 100% tested.

2.2 DC Characteristics

Applicable over recommended operating range from: T_{AI} = –40°C to +85°C, V_{CC} = 1.7V to 5.5V, (unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
V_{CC}	Supply Voltage		1.7		5.5	V
I_{CC1}	Supply Current V_{CC} = 5.0V	Read at 400kHz		1.0	2.0	mA
I_{CC2}	Supply Current V_{CC} = 5.0V	Write at 400kHz		2.0	3.0	mA
I_{SB1}	Standby Current V_{CC} = 1.7V	V_{IN} = V_{CC} or V_{SS}			1.0	µA
I_{SB2}	Standby Current V_{CC} = 3.6V	V_{IN} = V_{CC} or V_{SS}			3.0	µA
I_{SB3}	Standby Current V_{CC} = 5.5V	V_{IN} = V_{CC} or V_{SS}, A_0 = V_{SS}			6.0	µA
I_{LI}	Input Leakage Current	V_{IN} = V_{CC} or V_{SS}		0.10	3.0	µA
I_{LO}	Output Leakage Current	V_{OUT} = V_{CC} or V_{SS}		0.05	3.0	µA
V_{IL}	Input Low Level[1]		–0.6		V_{CC} x 0.3	V
V_{IH}	Input High Level[1]		V_{CC} x 0.7		V_{CC} + 0.5	V
V_{OL2}	Output Low Level V_{CC} = 3.0V	I_{OL} = 2.1mA			0.4	V
V_{OL1}	Output Low Level V_{CC} = 1.7V	I_{OL} = 0.15mA			0.2	V

Note: 1. V_{IL} min and V_{IH} max are reference only and are not tested.

2.3 AC Characteristics

Symbol	Parameter	1.7V		2.5V, 5.0V		Units
		Min	Max	Min	Max	
f_{SCL}	Clock Frequency, SCL		400		1000	kHz
t_{LOW}	Clock Pulse Width Low	1.2		0.4		µs
t_{HIGH}	Clock Pulse Width High	0.6		0.4		µs
t_I	Noise Suppression Time(1)		100		50	ns
t_{AA}	Clock Low To Data Out Valid	0.1	0.9	0.05	0.55	µs
t_{BUF}	Time the bus must be free before a new transmission can start(1)	1.3		0.5		µs
$t_{HD.STA}$	Start Hold Time	0.6		0.25		µs
$t_{SU.STA}$	Start Set-up Time	0.6		0.25		µs
$t_{HD.DAT}$	Data in Hold Time	0		0		µs
$t_{SU.DAT}$	Data in Set-up Time	100		100		ns
t_R	Inputs Rise Time(1)		3.0		0.3	µs
t_F	Inputs Fall Time(1)		300		100	ns
$t_{SU.STO}$	Stop Set-up Time	0.6		0.25		µs
t_{DH}	Data Out Hold Time	50		50		ns
t_{WR}	Write Cycle Time		5		5	ms
Endurance(1)	25°C, Page Mode, 3.3V	1M		1M		Write Cycles

Note: 1. This parameter is characterized and is not 100% tested.

3. Memory Organization

Atmel AT34C02D, 2K Serial EEPROM: The 2K is internally organized with 16 pages of 16 bytes of EEPROM each. Random word addressing requires a 8-bit data word address.

4. Device Operation

Clock and Data Transitions: The SDA pin is normally pulled high with an external device. Data on the SDA pin may change only during SCL low time periods (see Figure 4-4 on page 9). Data changes during SCL high periods will indicate a Start or Stop condition as defined below.

Start Condition: A high-to-low transition of SDA with SCL high is a Start condition which must precede any other command (see Figure 4-5 on page 9).

Stop Condition: A low-to-high transition of SDA with SCL high is a Stop condition. After a read sequence, the Stop command will place the EEPROM in a standby power mode (see Figure 4-5 on page 9).

Acknowledge: All addresses and data words are serially transmitted to and from the EEPROM in 8-bit words. The EEPROM sends a zero to acknowledge that it has received each word. This happens during the ninth clock cycle (see Figure 4-6 on page 9).

Standby Mode: The AT34C02D features a low-power standby mode which is enabled:

- Upon power-up or
- After the receipt of the Stop bit and the completion of any internal operations

Memory Reset: After an interruption in protocol, power loss or system reset, any 2-wire part can be reset by following these steps:

1. Create a Start bit condition
2. Clock nine cycles
3. Create another Start bit followed by Stop bit condition as shown below

Figure 4-1. Software Reset

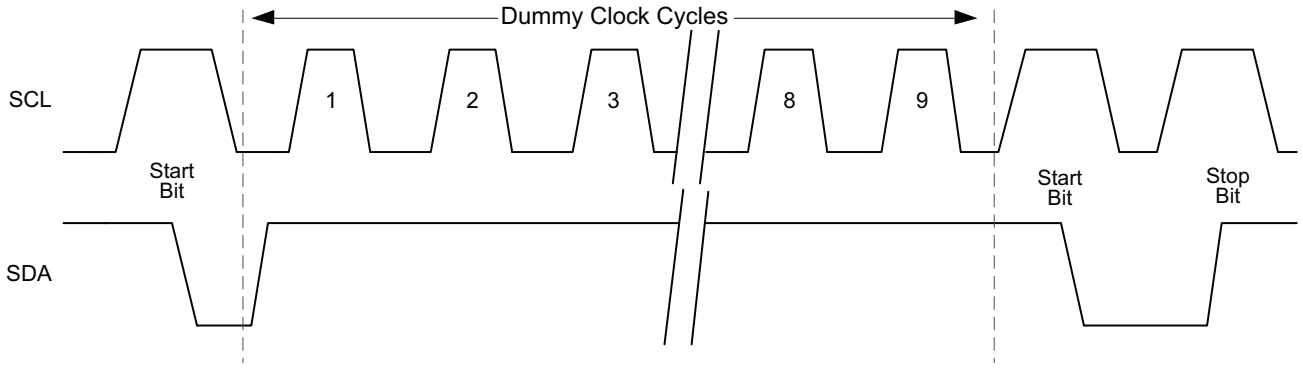


Figure 4-2. Bus Timing SCL

Serial Clock, SDA: Serial Data I/O

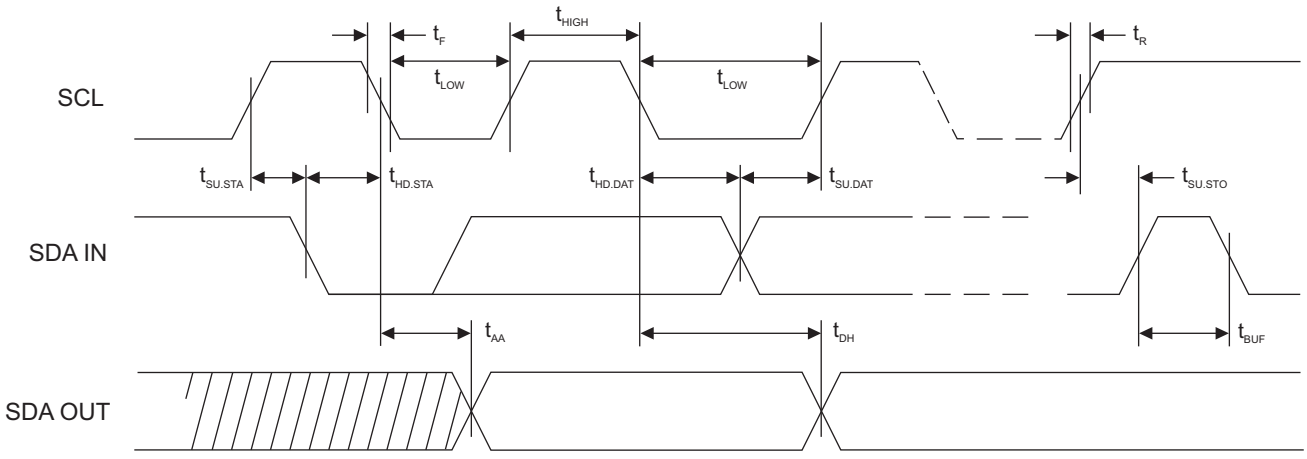
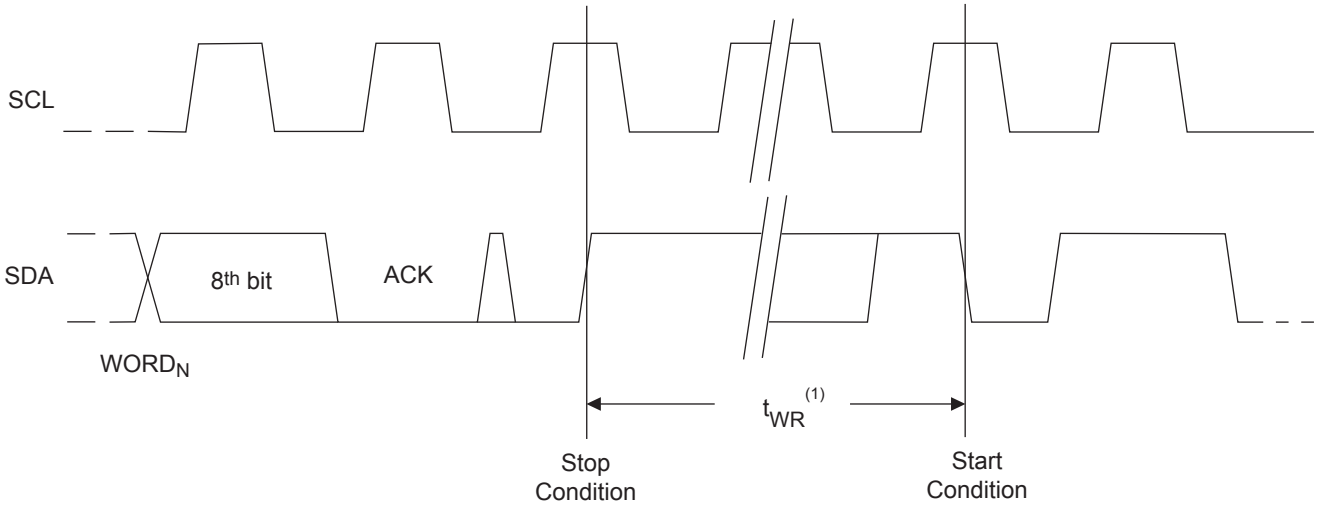


Figure 4-3. Write Cycle Timing SCL

Serial Clock, SDA: Serial Data I/O



Note: 1. The write cycle time t_{WR} is the time from a valid Stop condition of a write sequence to the end of the internal clear/write cycle.

Figure 4-4. Data Validity

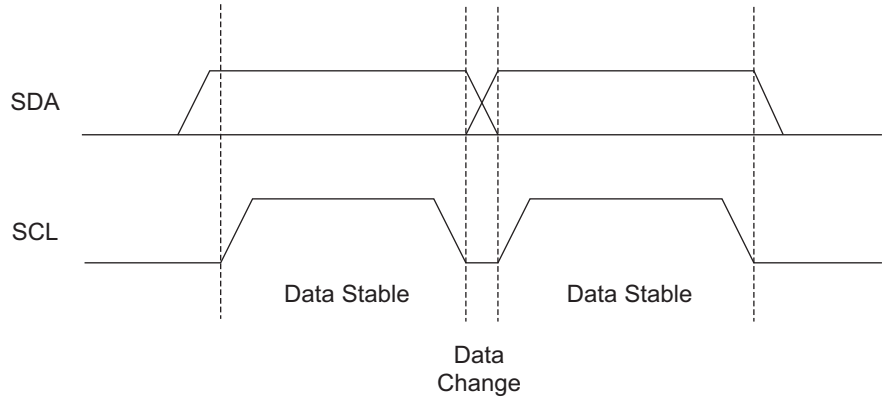


Figure 4-5. Start and Stop Condition

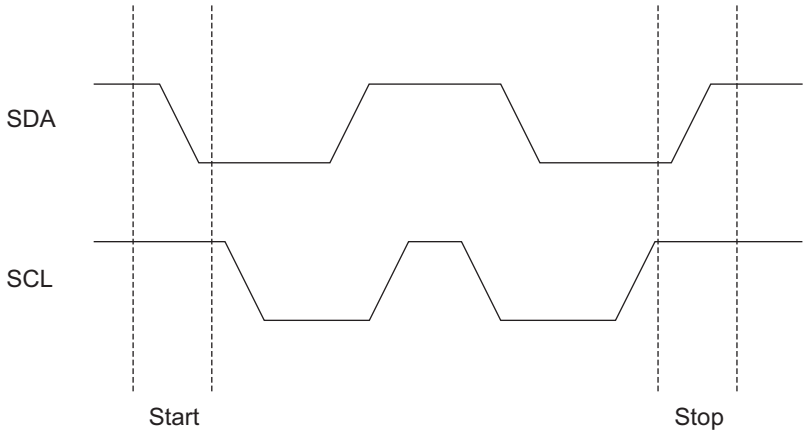
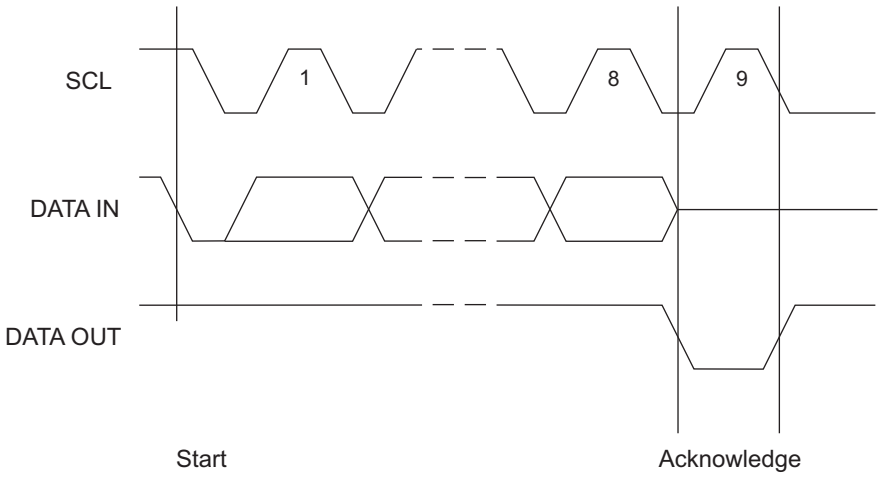


Figure 4-6. Output Acknowledge



5. Device Addressing

The 2K EEPROM device requires an 8-bit device address word following a start condition to enable the chip for a read or write operation (see Figure 8-1 on page 15).

The device address word consists of a mandatory '1010' (0xA) sequence for the first four most-significant bits for normal read and write operations and '0110' (0x6) for writing to the software write protect register.

The next three bits are the A_2, A_1, and A_0 device address bits for the AT34C02D EEPROM. These three bits must match their corresponding hard-wired input pins in order for the part to acknowledge.

The eighth bit of the device address is the read/write operation select bit. A read operation is initiated if this bit is high and a write operation is initiated if this bit is low.

Upon a compare of the device address, the EEPROM will acknowledge by outputting a zero. If a compare is not made, the chip will return to a standby state. The device will not acknowledge if the write protect register has been programmed and the control code is '0110' (0x6).

6. Write Operations

Byte Write: A write operation requires an 8-bit data word address following the device address word and acknowledgment. Upon receipt of this address, the EEPROM will again acknowledge or respond with a zero and then clock in the first 8-bit data word. Following receipt of the 8-bit data word, the EEPROM will output a zero and the addressing device, such as a microcontroller, must terminate the write sequence with a stop condition. At this time the EEPROM enters an internally-timed write cycle, t_{WR}, to the nonvolatile memory. All inputs are disabled during this write cycle and the EEPROM will not respond until the write is complete (see Figure 8-2 on page 16).

The device will acknowledge a write command, but not write the data, if the software or hardware write protection has been enabled. The write cycle time must be observed even when the write protection is enabled.

Page Write: The 2K device is capable of 16-byte page write.

A page write is initiated the same as a byte write, but the microcontroller does not send a stop condition after the first data word is clocked in. Instead, after the EEPROM acknowledges receipt of the first data word, the microcontroller can transmit up to fifteen more data words. The EEPROM will respond with a zero after each data word received. The microcontroller must terminate the page write sequence with a stop condition (see Figure 8-3 on page 16).

The data word address lower four bits are internally incremented following the receipt of each data word. The higher data word address bits are not incremented, retaining the memory page row location. When the word address, internally generated, reaches the page boundary, the following byte is placed at the beginning of the same page. If more than sixteen data words are transmitted to the EEPROM, the data word address will “roll over” and previous data will be overwritten. The address “roll over” during write is from the last byte of the current page to the first byte of the same page.

The device will acknowledge a write command, but not write the data, if the software or hardware write protection has been enabled. The write cycle time must be observed even when the write protection is enabled.

Acknowledge Polling: Once the internally-timed write cycle has started and the EEPROM inputs are disabled, acknowledge polling can be initiated. This involves sending a start condition followed by the device address word. The read/write bit is representative of the operation desired. Only if the internal write cycle has completed will the EEPROM respond with a zero allowing the read or write sequence to continue.

7. Write Protection

The software write protection, once enabled, write protects only the first-half of the array (addresses 0x00 - 0x7F) while the hardware write protection, via the WP pin, is used to protect the entire array.

Permanent Software Write Protection: The permanent software write protection is enabled by sending a command to the device, similar to a normal write command, which programs the permanent write protect register. This must be done with the WP pin low. The write protect register is programmed by sending a write command with the device address of '0110' (0x6) instead of '1010' (0xA) with the address and data bit(s) being don't cares (see Figure 7-1 on page 11). Once the permanent software write protection has been enabled, the device will no longer acknowledge the '0110' (0x6) control byte. The permanent software write protection cannot be reversed even if the device is powered down. The write cycle time must be observed.

Reversible Software Write Protection: The reversible software write protection is enabled by sending a command to the device, similar to a normal write command, which programs the reversible write protect register. This must be done with the WP pin low. The reversible write protect register is programmed by sending a write command '01100010' (0x62) with pins A_2 and A_1 tied to ground and pin A_0 connected to V_{HV} (see Figure 7-2). The reversible write protection can be reversed by sending a command '01100110' (0x66) with pin A_2 tied to ground, pin A_1 tied to V_{CC} and pin A_0 tied to V_{HV} (see Figure 7-3).

Hardware Write Protection: The WP pin can be connected to V_{CC}, GND, or left floating. Connecting the WP pin to V_{CC} will write protect the entire array, regardless of whether or not the software write protection has been enabled or invoked. The software write protection register cannot be programmed when the WP pin is connected to V_{CC}. If the WP pin is connected to GND or left floating, the write protection mode is determined by the status of the software write protect register.

Figure 7-1. Setting Permanent Write Protect Register (PSWP)

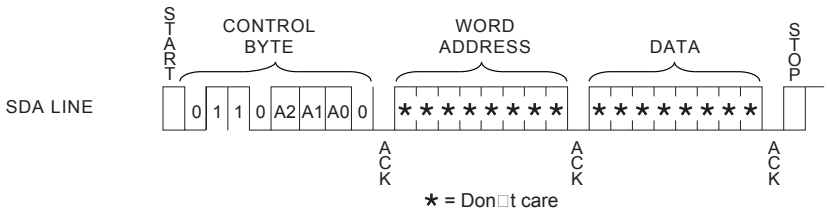


Figure 7-2. Setting Reversible Write Protect Register (RSWP)

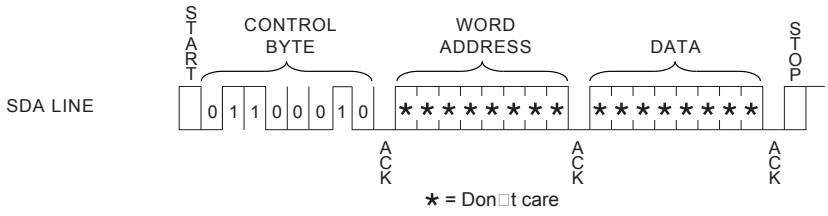


Figure 7-3. Clearing Reversible Write Protect Register (RSWP)

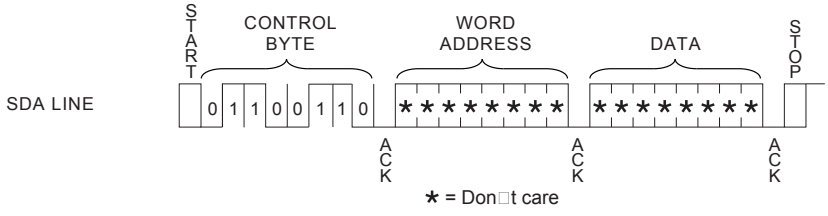


Table 7-1. Write Protection

	Pin State/Voltage			Preamble							R/W
Command	**A_2**	**A_1**	**A_0**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Set PSWP	A_2	A_1	A_0	0	1	1	0	A_2	A1	A_0	0
Set RSWP	0	0	V_{HV}	0	1	1	0	0	0	1	0
Clear RSWP	0	V_{CC}	V_{HV}	0	1	1	0	0	1	1	0

Table 7-2. V_{HV}

	Min	Max	Units
V_{HV}	7	10	V

Note: $V_{HV} - V_{CC} > 4.8V$

Table 7-3. WP Connected to GND or Floating

WP Connected to GND or Floating					
Command	**R/W Bit**	**Permanent Write Protect Register PSWP**	**Reversible Write Protect Register RSWP**	**Acknowledgment from Device**	**Action from Device**
1010	R	X	X	ACK	Read Array
1010	W	Programmed	X	ACK	Can write to second-half (80h - FFh) only
1010	W	X	Programmed	ACK	Can write to second-half (80h - FFh) only
1010	W	Not Programmed	Not Programmed	ACK	Can write to Full Array
Read PSWP	R	Programmed	X	No ACK	STOP - Indicates permanent write protect register is programmed
Read PSWP	R	Not Programmed	X	ACK	Read out data undefined. Indicates PSWP register is not programmed
Set PSWP	W	Programmed	X	No ACK	STOP - Indicates permanent write protect register is programmed
Set PSWP	W	Not Programmed	X	ACK	Program permanent write protect register (irreversible)
Read RSWP	R	X	Programmed	No ACK	STOP - Indicates reversible write protect register is programmed
Read RSWP	R	X	Not Programmed	ACK	Read out data undefined. Indicates RSWP register is not programmed
Set RSWP	W	X	Programmed	No ACK	STOP - Indicates reversible write protect register is programmed
Set RSWP	W	X	Not Programmed	ACK	Program reversible write protect register (reversible)
Clear RSWP	W	Programmed	X	No ACK	STOP - Indicates permanent write protect register is programmed
Clear RSWP	W	Not Programmed	X	ACK	Clear (unprogram) reversible write protect register (reversible)

Table 7-4. WP Connected to Vcc

WP connected to V_{CC}					
Command	**R/W Bit**	**Permanent Write Protect Register PSWP**	**Reversible Write Protect Register RSWP**	**Acknowledgment from Device**	**Action from Device**
1010	R	X	X	ACK	Read Array
1010	W	X	X	ACK	Device Write Protect
Read PSWP	R	Programmed	X	No ACK	STOP - Indicates permanent write protect register is programmed
Read PSWP	R	Not Programmed	X	ACK	Read out data undefined. Indicates PSWP register is not programmed
Set PSWP	W	Programmed	X	No ACK	STOP - Indicates permanent write protect register is programmed
Set PSWP	W	Not Programmed	X	ACK	Cannot program write protect registers
Read RSWP	R	X	Programmed	No ACK	STOP - Indicates reversible write protect register is programmed
Read RSWP	R	X	Not Programmed	ACK	Read out data undefined. Indicates RSWP register is not programmed
Set RSWP	W	X	Programmed	No ACK	STOP - Indicates reversible write protect register is programmed
Set RSWP	W	X	Not Programmed	ACK	Cannot program write protect registers
Clear RSWP	W	Programmed	X	No ACK	STOP - Indicates permanent write protect register is programmed
Clear RSWP	W	Not Programmed	X	ACK	Cannot write to write protect registers

8. Read Operations

Read operations are initiated the same way as write operations with the exception that the read/write select bit in the device address word is set to one. There are three read operations:

- Current Address Read
- Random Address Read
- Sequential Read

Current Address Read: The internal data word address counter maintains the last address accessed during the last read or write operation, incremented by one. This address stays valid between operations as long as the chip power is maintained. The address "roll over" during read is from the last byte of the last memory page to the first byte of the first page.

Once the device address with the read/write select bit set to one is clocked in and acknowledged by the EEPROM, the current address data word is serially clocked out. To end the command, the microcontroller does not respond with a zero but does generate a stop condition in the subsequent clock cycle. (see Figure 8-4 on page 16).

Random Read: A random read requires a "dummy" byte write sequence to load in the data word address. Once the device address word and data word address are clocked in and acknowledged by the EEPROM, the microcontroller must generate another start condition. The microcontroller now initiates a current address read by sending a device address with the read/write select bit high. The EEPROM acknowledges the device address and serially clocks out the data word. To end the command, the microcontroller does not respond with a zero but does generate a stop condition in the subsequent clock cycle. (see Figure 8-5 on page 16).

Sequential Read: Sequential Reads are initiated by either a current address read or a random address read. After the microcontroller receives a data word, it responds with an acknowledge. As long as the EEPROM receives an acknowledge, it will continue to increment the data word address and serially clock out sequential data words. When the memory address limit is reached, the data word address will "roll over" and the sequential read will continue. The sequential read operation is terminated when the microcontroller does not respond with a zero but does generate a stop condition in the subsequent clock cycle (see Figure 8-6 on page 16).

Permanent Write Protect Register (PSWP) Status: Determining the status of the permanent write protect register can be accomplished by sending a similar command to the device as was used when programming the register, except the R/W bit must now be set to a one. If the device returns an acknowledge, the permanent write protect register has not been programmed. Otherwise, it has been programmed and the first-half of the array is permanently write protected.

Reversible Write Protect Register (RSWP) Status: Determining the status of the reversible write protect register can be accomplished by sending a similar command to the device as was used when programming the register, except the R/W bit must be set to one. If the returns an device acknowledge, then the reversible write protect register has not been programmed. The first-half of the array is write protected, but remains reversible.

Table 8-1. PSWP and RSWP Status

	Pin State/Voltage			Preamble							R/W
Command	A_2	A_1	A_0	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Read PSWP	A_2	A_1	A_0	0	1	1	0	A2	A1	A0	1
Read RSWP	0	0	A_0	0	1	1	0	0	0	1	1

Figure 8-1. Device Address

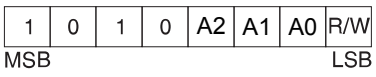


Figure 8-2. Byte Write

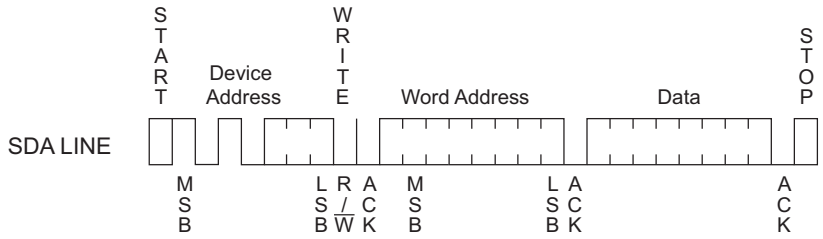


Figure 8-3. Page Write

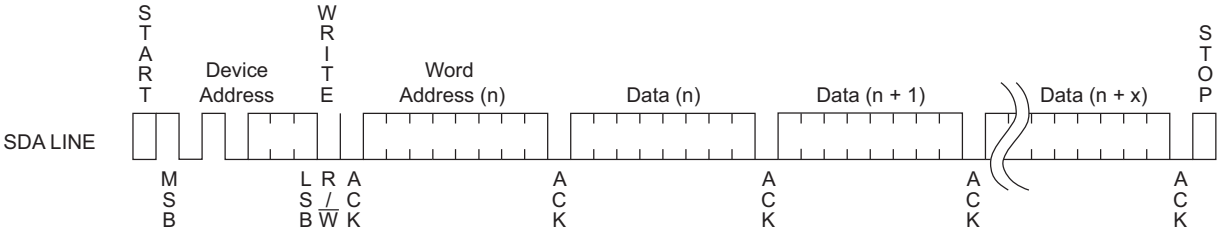


Figure 8-4. Current Address Read

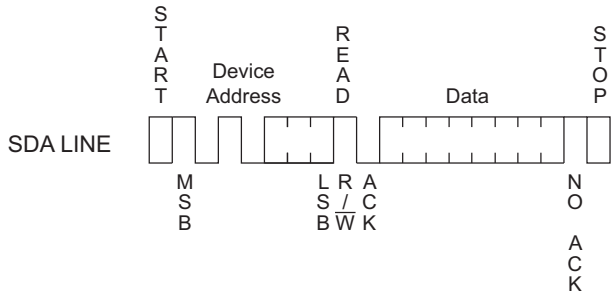


Figure 8-5. Random Read

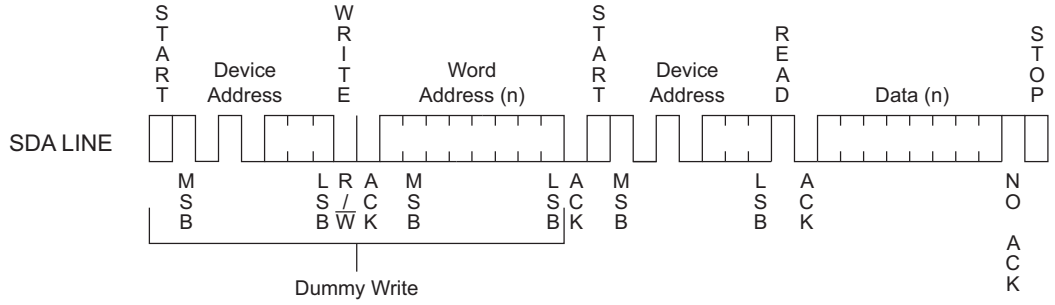
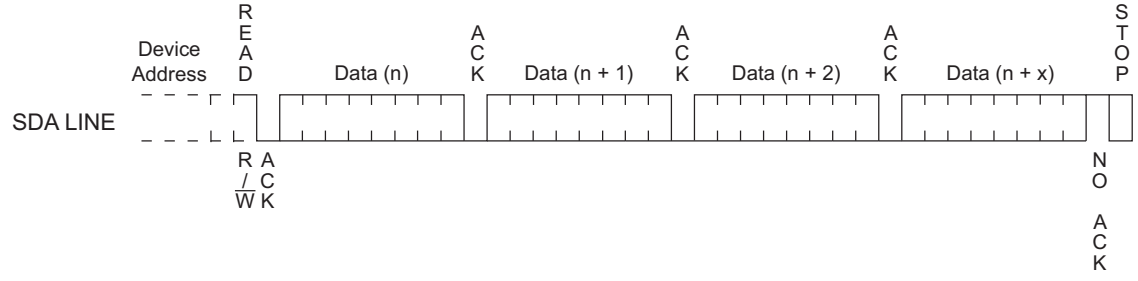
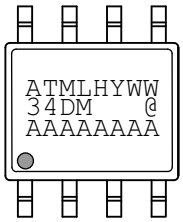
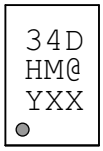
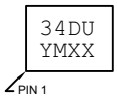


Figure 8-6. Sequential Read



9. Part Markings

AT34C02D: Package Marking Information

8-lead SOIC	8-lead TSSOP
	
8-lead UDFN	**8-ball VFBGA**
2.0 x 3.0 mm Body	1.5 x 2.0 mm Body
	

Note 1: ● *designates pin 1*

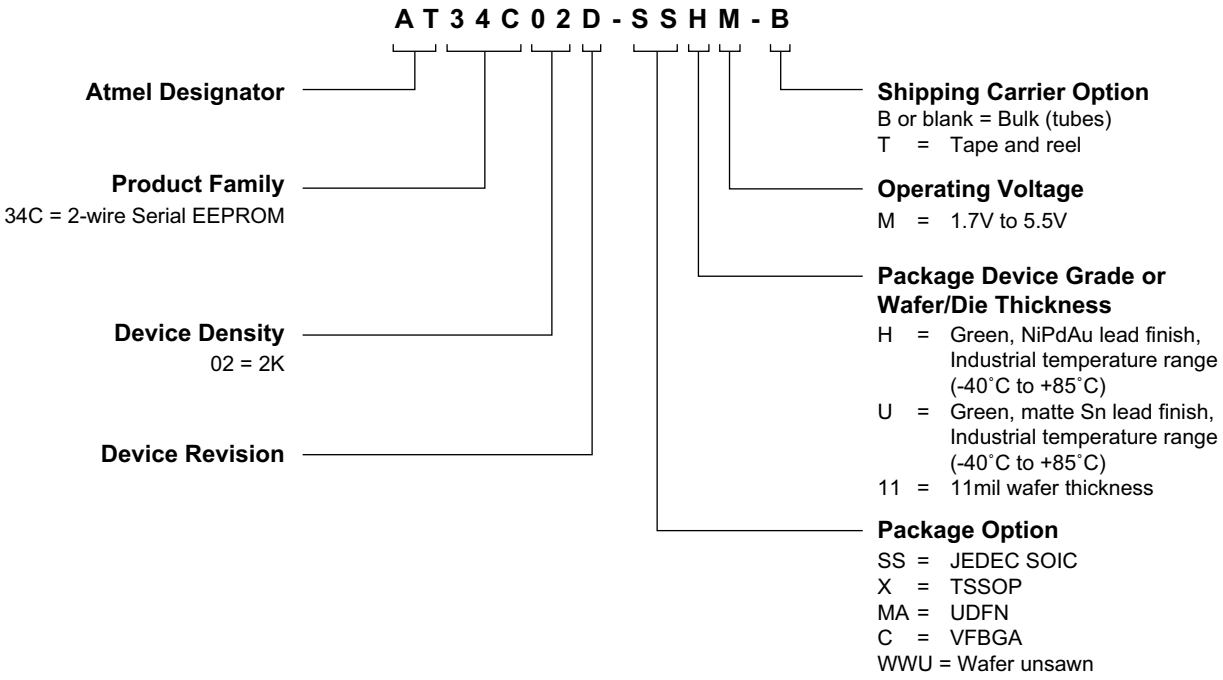
Note 2: Package drawings are not to scale

Catalog Number Truncation			
AT34C02D		Truncation Code ###: 34D	
Date Codes			**Voltages**
Y = Year	M = Month	WW = Work Week of Assembly	M: 1.7V min
2: 2012 6: 2016 3: 2013 7: 2017 4: 2014 8: 2018 5: 2015 9: 2019	A: January B: February ... L: December	02: Week 2 04: Week 4 ... 52: Week 52	
Country of Assembly	**Lot Number**		**Grade/Lead Finish Material**
@ = Country of Assembly	AAA...A = Atmel Wafer Lot Number		U: Industrial/Matte Tin H: Industrial/NiPdAu
Trace Code			**Atmel Truncation**
XX = Trace Code (Atmel Lot Numbers Correspond to Code) Example: AA, AB.... YZ, ZZ			AT: Atmel ATM: Atmel ATML: Atmel

3/5/12

Atmel Package Mark Contact: DL-CSO-Assy_eng@atmel.com	TITLE	DRAWING NO.	REV.
	34C02DSM, AT34C02D Package Marking Information	34C02DSM	C

10. Ordering Code Detail



11. Atmel AT34C02D Ordering Information

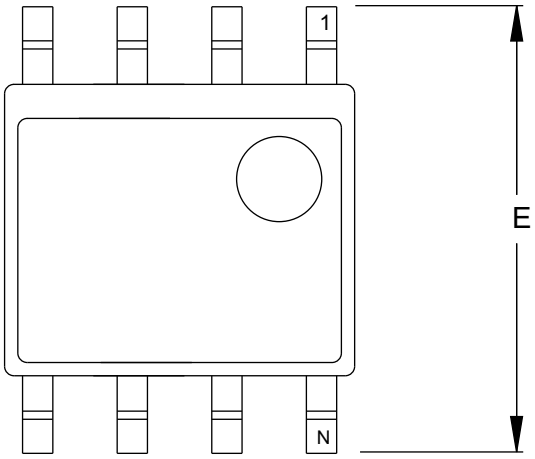
Atmel Ordering Code	Package	Voltage	Operation Range
AT34C02D-SSHM-B[1] (NiPdAu lead finish)	8S1	1.7V to 5.5V	Lead-free/Halogen-free/ Industrial Temperature (–40°C to 85°C)
AT34C02D-SSHM-T[2] (NiPdAu lead finish)	8S1		
AT34C02D-XHM-B[1] (NiPdAu lead finish)	8X		
AT34C02D-XHM-T[2] (NiPdAu lead finish)	8X		
AT34C02D-MAHM-T[2] (NiPdAu lead finish)	8MA2		
AT34C02D-CUM-T[2]	8U3-1		
AT34C02D-WWU11M[3]	Wafer Sale		

Notes:
1. B = Bulk
2. T = Tape and reel
   - SOIC = 4K per reel
   - TSSOP, UDFN, and VFBGA = 5K per reel
3. For Wafer sales, please contact Atmel Sales.

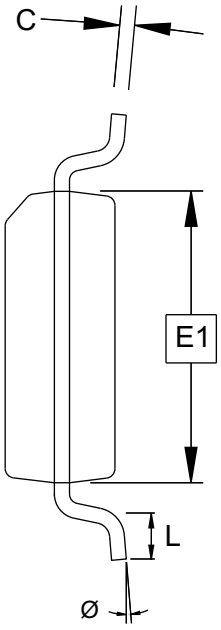
Package Type	
8S1	8-lead, 0.150" wide body, Plastic Gull Wing Small Outline (JEDEC SOIC)
8X	8-lead, 4.4mm body, Plastic Thin Shrink Small Outline (TSSOP)
8MA2	8-pad, 2.00mm x 3.00mm, 0.60mm body, Ultra Thin Dual Flat No Lead (UDFN), (MLP 2x3mm)
8U3-1	8-ball, 1.50 x 2.00mm body, 0.50mm pitch, die Ball Grid Array (VFBGA)

12. Packaging Information

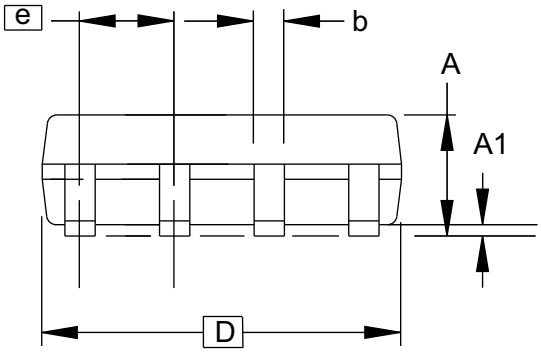
12.1 8S1 – JEDEC SOIC



TOP VIEW



END VIEW



SIDE VIEW

Notes: This drawing is for general information only.
Refer to JEDEC Drawing MS-012, Variation AA
for proper dimensions, tolerances, datums, etc.

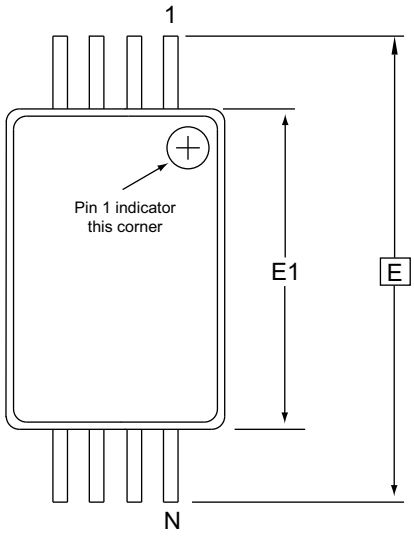
COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	1.35	–	1.75	
A1	0.10	–	0.25	
b	0.31	–	0.51	
C	0.17	–	0.25	
D	4.80	–	5.05	
E1	3.81	–	3.99	
E	5.79	–	6.20	
e	1.27 BSC			
L	0.40	–	1.27	
Ø	0°	–	8°	

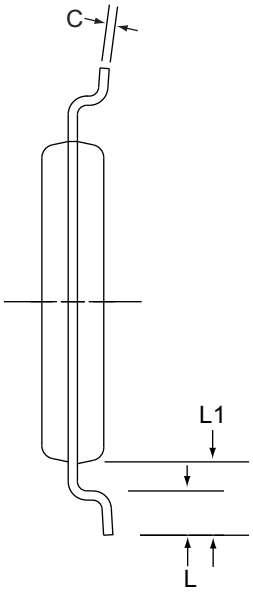
6/22/11

Atmel Package Drawing Contact: packagedrawings@atmel.com	**TITLE** 8S1, 8-lead (0.150” Wide Body), Plastic Gull Wing Small Outline (JEDEC SOIC)	**GPC** SWB	**DRAWING NO.** 8S1	**REV.** G

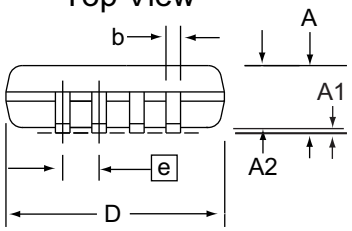
12.2 8X – TSSOP



Top View



End View



Side View

Notes:
1. This drawing is for general information only. Refer to JEDEC Drawing MO-153, Variation AA, for proper dimensions, tolerances, datums, etc.
2. Dimension D does not include mold Flash, protrusions or gate burrs. Mold Flash, protrusions and gate burrs shall not exceed 0.15mm (0.006in) per side.
3. Dimension E1 does not include inter-lead Flash or protrusions. Inter-lead Flash and protrusions shall not exceed 0.25mm (0.010in) per side.
4. Dimension b does not include Dambar protrusion. Allowable Dambar protrusion shall be 0.08mm total in excess of the b dimension at maximum material condition. Dambar cannot be located on the lower radius of the foot. Minimum space between protrusion and adjacent lead is 0.07mm.
5. Dimension D and E1 to be determined at Datum Plane H.

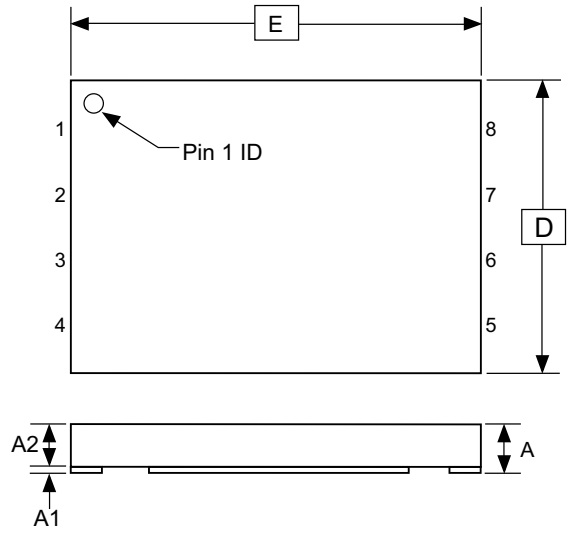
COMMON DIMENSIONS
(Unit of Measure = mm)

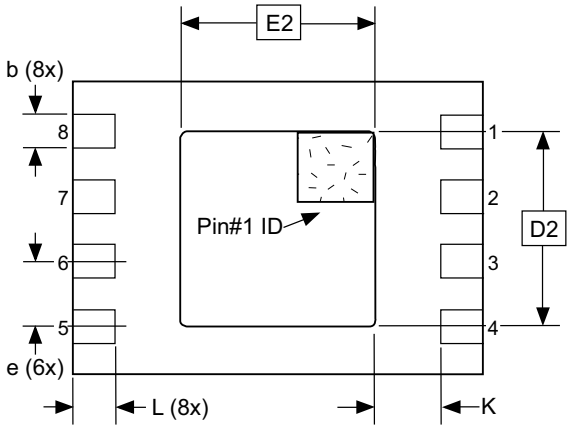
SYMBOL	MIN	NOM	MAX	NOTE
A	-	-	1.20	
A1	0.05	-	0.15	
A2	0.80	1.00	1.05	
D	2.90	3.00	3.10	2, 5
E		6.40 BSC		
E1	4.30	4.40	4.50	3, 5
b	0.19	–	0.30	4
e		0.65 BSC		
L	0.45	0.60	0.75	
L1		1.00 REF		
C		0.09	-	0.20

6/22/11

Atmel Package Drawing Contact: packagedrawings@atmel.com	**TITLE** 8X, 8-lead 4.4mm Body, Plastic Thin Shrink Small Outline Package (TSSOP)	**GPC** TNR	**DRAWING NO.** 8X	**REV.** D

12.3 8MA2 – UDFN





COMMON DIMENSIONS
(Unit of Measure = mm)

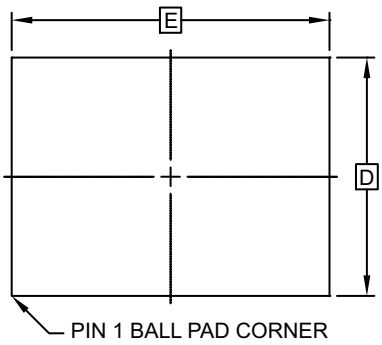
SYMBOL	MIN	NOM	MAX	NOTE
D		2.00 BSC		
E		3.00 BSC		
D2	1.40	1.50	1.60	
E2	1.20	1.30	1.40	
A	0.50	0.55	0.60	
A1	0.0	0.02	0.05	
A2	–	–	0.55	
C		0.152 REF		
L	0.30	0.35	0.40	
e		0.50 BSC		
b	0.18	0.25	0.30	3
K	0.20	–	–	

Notes:
1. This drawing is for general information only. Refer to JEDEC Drawing MO-229, for proper dimensions, tolerances, datums, etc.
2. The terminal #1 ID is a laser-marked feature.
3. Dimension b applies to metallized terminal and is measured between 0.15 mm and 0.30 mm from the terminal tip. If the terminal has the optional radius on the other end of the terminal, the dimension should not be measured in that radius area.

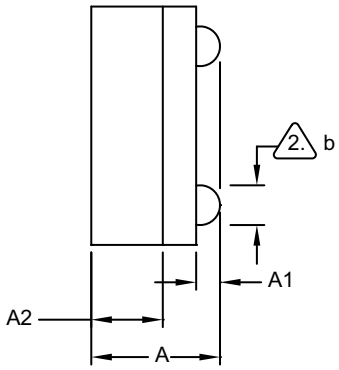
7/15/11

Atmel Package Drawing Contact: packagedrawings@atmel.com	**TITLE** 8MA2, 8-pad, 2 x 3 x 0.6 mm Body, Thermally Enhanced Plastic Ultra Thin Dual Flat No Lead Package (UDFN)	**GPC** YNZ	**DRAWING NO.** 8MA2	**REV.** B

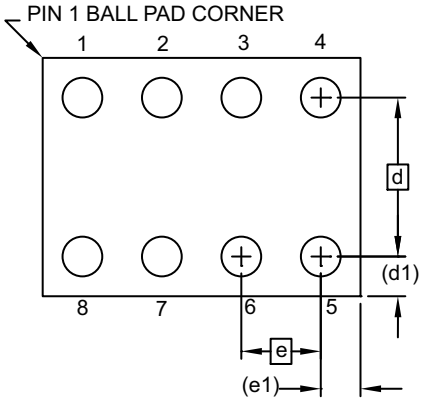
12.4 8U3-1 – VFBGA



TOP VIEW



SIDE VIEW



BOTTOM VIEW
8 SOLDER BALLS

Notes:

1. This drawing is for general information only.
2. Dimension 'b' is measured at maximum solder ball diameter.
3. Solder ball composition shall be 95.5Sn-4.0Ag-.5Cu.

COMMON DIMENSIONS
(Unit of Measure - mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	0.73	0.79	0.85	
A1	0.09	0.14	0.19	
A2	0.40	0.45	0.50	
b	0.20	0.25	0.30	2
D	1.50 BSC			
E	2.0 BSC			
e	0.50 BSC			
e1	0.25 REF			
d	1.00 BSC			
d1	0.25 REF			

3/27/12

Atmel Package Drawing Contact: packagedrawings@atmel.com	TITLE 8U3-1, 8-ball, 1.50mm x 2.00mm body, 0.50mm pitch, VFBGA Package	GPC GXU	DRAWING NO. 8U3-1	REV. E

13. Revision History

Doc. Rev.	Date	Comments
8781B	06/2012	Correct ordering code: - AT34C02D-WWU11, Die Sale to AT34C02D-WWU11M, Wafer Sale. Update template.
8781A	03/2012	Initial document release.

Atmel | Enabling Unlimited Possibilities®

Atmel Corporation
1600 Technology Drive
San Jose, CA 95110
USA
Tel: (+1) (408) 441-0311
Fax: (+1) (408) 487-2600
www.atmel.com

Atmel Asia Limited
Unit 01-5 & 16, 19F
BEA Tower, Millennium City 5
418 Kwun Tong Roa
Kwun Tong, Kowloon
HONG KONG
Tel: (+852) 2245-6100
Fax: (+852) 2722-1369

Atmel Munich GmbH
Business Campus
Parkring 4
D-85748 Garching b. Munich
GERMANY
Tel: (+49) 89-31970-0
Fax: (+49) 89-3194621

Atmel Japan G.K.
16F Shin-Osaki Kangyo Bldg
1-6-4 Osaki, Shinagawa-ku
Tokyo 141-0032
JAPAN
Tel: (+81) (3) 6417-0300
Fax: (+81) (3) 6417-0370