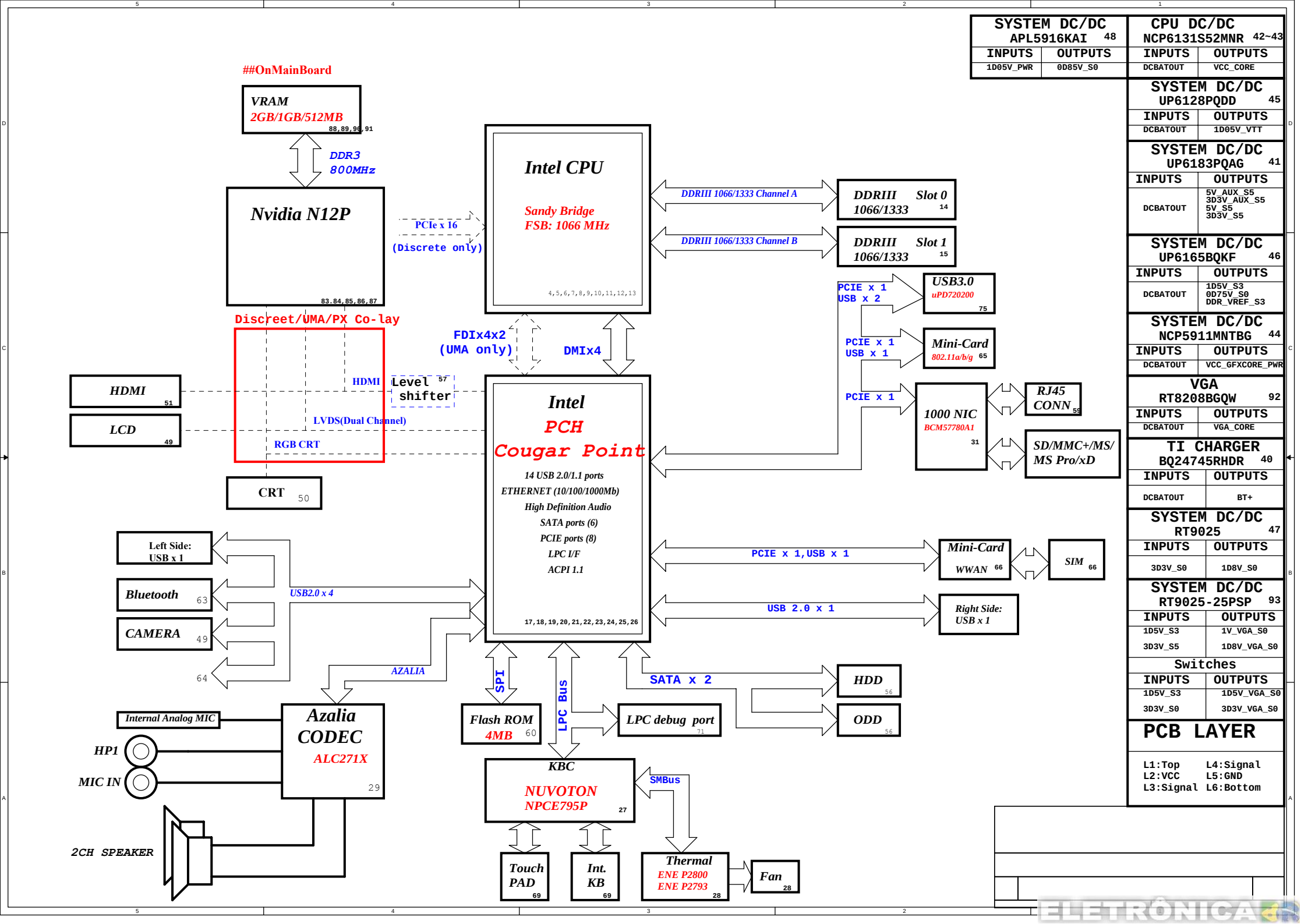


SYSTEM DC/DC APL5916KAI 48	
INPUTS	OUTPUTS
1D05V_PWR	0D85V_S0

CPU DC/DC NCP6131S52MNR 42~43	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE

SYSTEM DC/DC UP6128PQDD 45	
INPUTS	OUTPUTS
DCBATOUT	1D05V_VTT

SYSTEM DC/DC UP6183PQAG 41	
INPUTS	OUTPUTS
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5 5V_S5 3D3V_S5

SYSTEM DC/DC UP6165BQKF 46	
INPUTS	OUTPUTS
DCBATOUT	1D5V_S3 0D75V_S0 DDR_VREF_S3

SYSTEM DC/DC NCP5911MNTBG 44	
INPUTS	OUTPUTS
DCBATOUT	VCC_GFXCORE_PWR

VGA RT8208BGQW 92	
INPUTS	OUTPUTS
DCBATOUT	VGA_CORE

TI CHARGER BQ24745RHDR 40	
INPUTS	OUTPUTS
DCBATOUT	BT+

SYSTEM DC/DC RT9025 47	
INPUTS	OUTPUTS
3D3V_S0	1D8V_S0

SYSTEM DC/DC RT9025-25PSP 93	
INPUTS	OUTPUTS
1D5V_S3	1V_VGA_S0
3D3V_S5	1D8V_VGA_S0
Switches	
INPUTS	OUTPUTS
1D5V_S3	1D5V_VGA_S0
3D3V_S0	3D3V_VGA_S0

PCB LAYER

L1:Top L4:Signal
L2:VCC L5:GND
L3:Signal L6:Bottom

PCH Strapping

Huron River Schematic Checklist Rev.0_7

Name	Schematics Notes
SPKR	**Reboot option at power-up** **Default Mode:** Internal weak Pull-down. **No Reboot Mode with TCO Disabled:** Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-up. Leave as "No Connect".
GNT3#/GPIO55 GNT2#/GPIO53 GNT1#/GPIO51	GNT[3:0]# functionality is not available on Mobile. Mobile: Used as GPIO only Pull-up resistors are not required on these signals. If pull-ups are used, they should be tied to the Vcc3_3power rail.
SPI_MOSI	**Enable Danbury:** Connect to Vcc3_3 with 8.2-k? weak pull-up resistor. **Disable Danbury:** Left floating, no pull-down required.
NV_ALE	**Enable Danbury:** Connect to +NVRAM_VCCQ with 8.2-kohm weak pull-up resistor [CRB has it pulled up with 1-kohm no-stuff resistor] **Disable Danbury:** Leave floating (internal pull-down)
NC_CLE	DMI termination voltage. Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	Low (0) - Flash Descriptor Security will be overridden. Also, when this signals is sampled on the rising edge of PWROK then it will also disable Intel ME and its features. High (1) - Security measure defined in the Flash Descriptor will be enabled. Platform design should provide appropriate pull-up or pull-down depending on the desired settings. If a jumper option is used to tie this signal to GND as required by the functional strap, the signal should be pulled low through a weak pull-down in order to avoid asserting HDA_DOCK_EN# inadvertently. Note: CRB recommends 1-kohm pull-down for FD Override. There is an internal pull-up of 20 kohm for DA_DOCK_EN# which is only enabled at boot/reset for strapping functions.
HDA_SDO	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
HDA_SYNC	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
GPIO15	Low (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality High (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality Note : This is an un-muxed signal. This signal has a weak internal pull-down of 20 kohm which is enabled when PWROK is low. Sampled at rising edge of RSMRST#. CRB has a 1-kohm pull-up on this signal to +3.3VA rail.
GPIO8	GPIO8 on PCH is the Integrated Clock Enable strap and is required to be pulled-down using a 1k +/- 5% resistor. When this signal is sampled high at the rising edge of RSMRST#, Integrated Clocking is enabled, When sampled low, Buffer Through Mode is enabled.
GPIO27	**Default = Do not connect (floating)** High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

Processor Strapping

Huron River Schematic Checklist Rev.0_7

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[2]	**PCI-Express Static Lane Reversal**	**1:** Normal Operation. **0:** Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	1
CFG[4]		**1:** Disabled - No Physical Display Port attached to Embedded DisplayPort. **0:** Enabled - An external Display Port device is connectd to the EMBEDDED display Port	0
CFG[6:5]	**PCI-Express Port Bifurcation Straps**	11 : x16 - Device 1 functions 1 and 2 disabled 10 : x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01 : Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00 : x8, x4, x4 - Device 1 functions 1 and 2 enabled	11
CFG[7]	**PEG DEFER TRAINING**	**1:** PEG Train immediately following xxRESETB de assertion **0:** PEG Wait for BIOS for training	1

POWER PLANE	VOLTAGE	Voltage Rails ACTIVE IN	DESCRIPTION
5V_S0 3D3V_S0 1D8V_S0 1D5V_S0 1D05V_VTT 0D85V_S0 0D75V_S0 VCC_CORE VCC_GFXCORE 1D8V_VGA_S0 3D3V_VGA_S0 1V_VGA_S0	5V 3.3V 1.8V 1.5V 1.05V 0.95 - 0.85V 0.75V 0.35V to 1.5V 0.4 to 1.25V 1.8V 3.3V 1V	S0	CPU Core Rail Graphics Core Rail
5V_USBX_S3 1D5V_S3 DDR_VREF_S3	5V 1.5V 0.75V	S3	
BT+ DCBATOUT 5V_S5 5V_AUX_S5 3D3V_S5 3D3V_AUX_S5	6V-14.1V 6V-14.1V 5V 5V 3.3V 3.3V	All S states	AC Brick Mode only
3D3V_LAN_S5	3.3V	WOL_EN	Legacy WOL
3D3V_AUX_KBC	3.3V	DSW, Sx	ON for supporting Deep Sleep states
3D3V_AUX_S5	3.3V	G3, Sx	Powered by Li Coin Cell in G3 and +V3ALW in Sx

USB Table

Pair	Device
0	Touch Panel / 3G SIM
1	USB Ext. port 1 (HS)
2	Fingerprint
3	BLUETOOTH
4	Mini Card2 (WWAN)
5	CARD READER
6	X
7	X
8	USB Ext. port 4 / E-SATA /USB CHARGER
9	USB Ext. port 2
10	EDP CAMERA
11	Mini Card1 (WLAN)
12	CAMERA
13	New Card

PCIE Routing

LANE1	Mini Card2(WWAN)
LANE2	Mini Card1(WLAN)
LANE3	Card Reader
LANE4	Onboard LAN
LANE5	USB3.0
LANE6	Intel GBE LAN
LANE7	Dock
LANE8	New Card

SATA Table

SATA	
Pair	Device
0	HDD1
1	HDD2
2	N/A
3	N/A
4	ODD
5	ESATA

SMBus ADDRESSES

I² C / SMBus Addresses		HURON RIVER ORB		
Device	Ref Des	Address	Hex	Bus
EC SMBus 1 Battery CHARGER				BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA
EC SMBus 2 PCH eDP				SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA
PCH SMBus SO-DIMMA (SPD) SO-DIMMB (SPD) Digital Pot G-Sensor MINI				PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK

CPU1A
SANDY
62.10055.421
Change:62.10053.611
2nd = 62.10055.321
3rd = 62.10040.821

Signal Routing Guideline:
PEG_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
PEG_ICOMPI & PEG_RCOMPO keep W/S=4/15 mils and routing length less than 500 mils.

Note:
Intel DMI supports both Lane Reversal and polarity inversion but only at PCH side. This is enabled via a soft strap.

Note:
Intel FDI supports both Lane Reversal and polarity inversion but only at PCH side. This is enabled via a soft strap.

Note:
Lane reversal does not apply to FDI sideband signals.

Signal Routing Guideline:
EDP_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
EDP_COMPIO keep W/S=4/15 mils and routing length less than 500 mils.

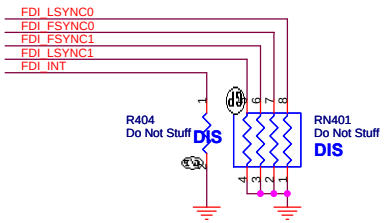
NOTE.
Processor strap CFG[4] should be pulled low to enable Embedded DisplayPort.

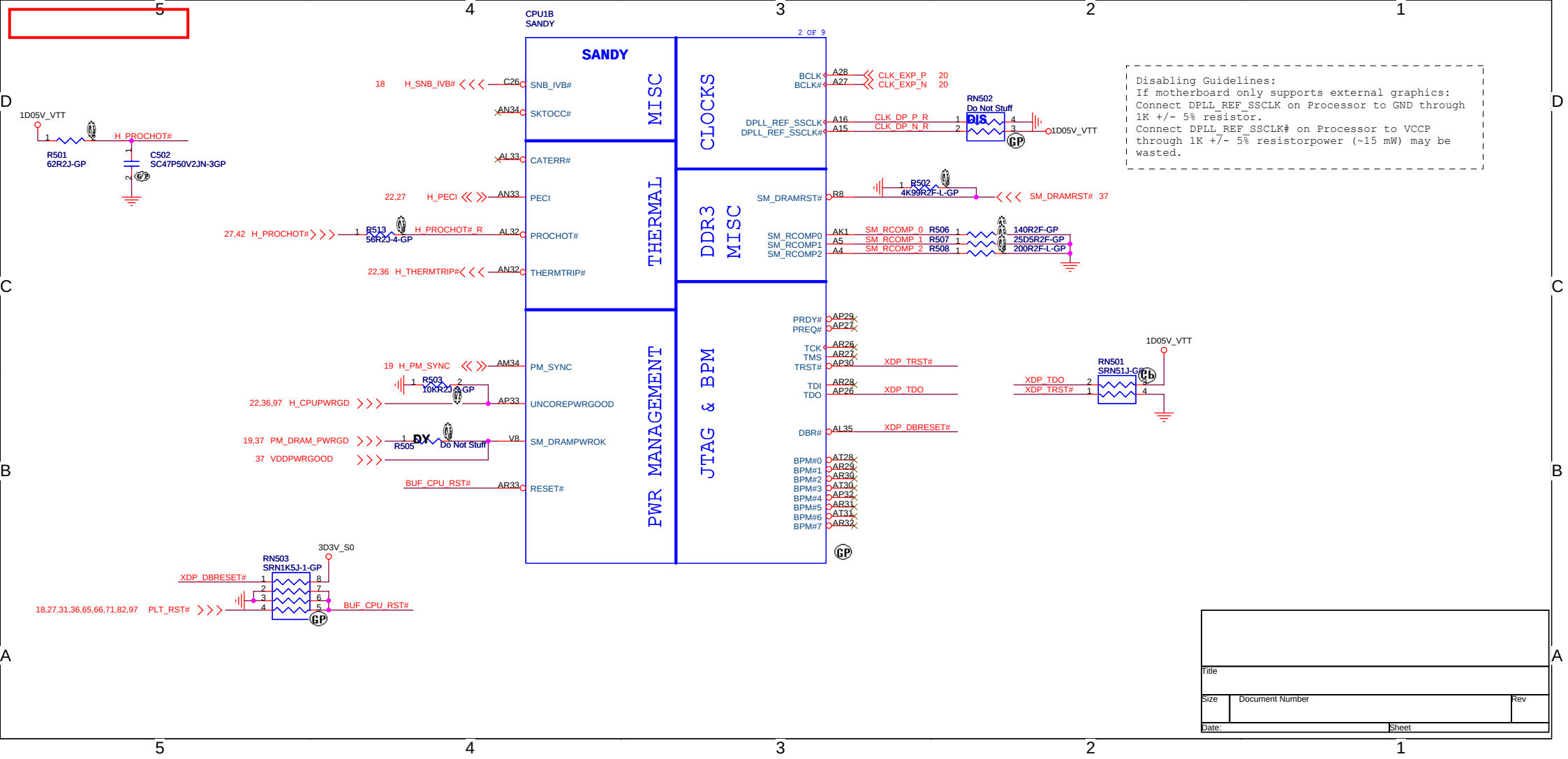
NOTE.
If PEG is not implemented, the RX&TX pairs can be left as No Connect

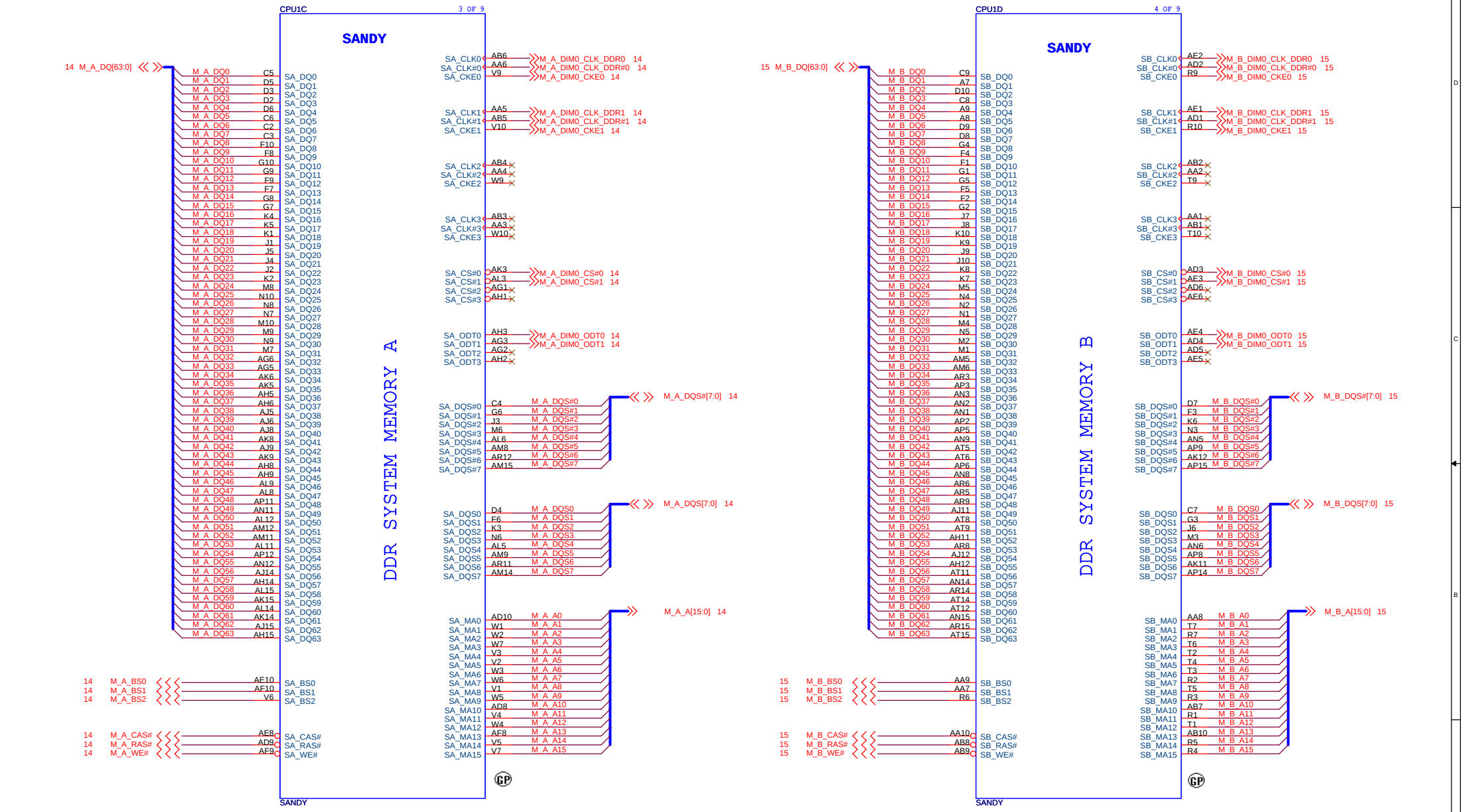
PEG Static Lane Reversal

NOTE:
Select a Fast FET similar to 2N7002E whose rise/ fall time is less than 6 ns. If HPD on eDP interface is disabled, connect it to CPU VCCIO via a 10-kΩ pull-Up resistor on the motherboard.

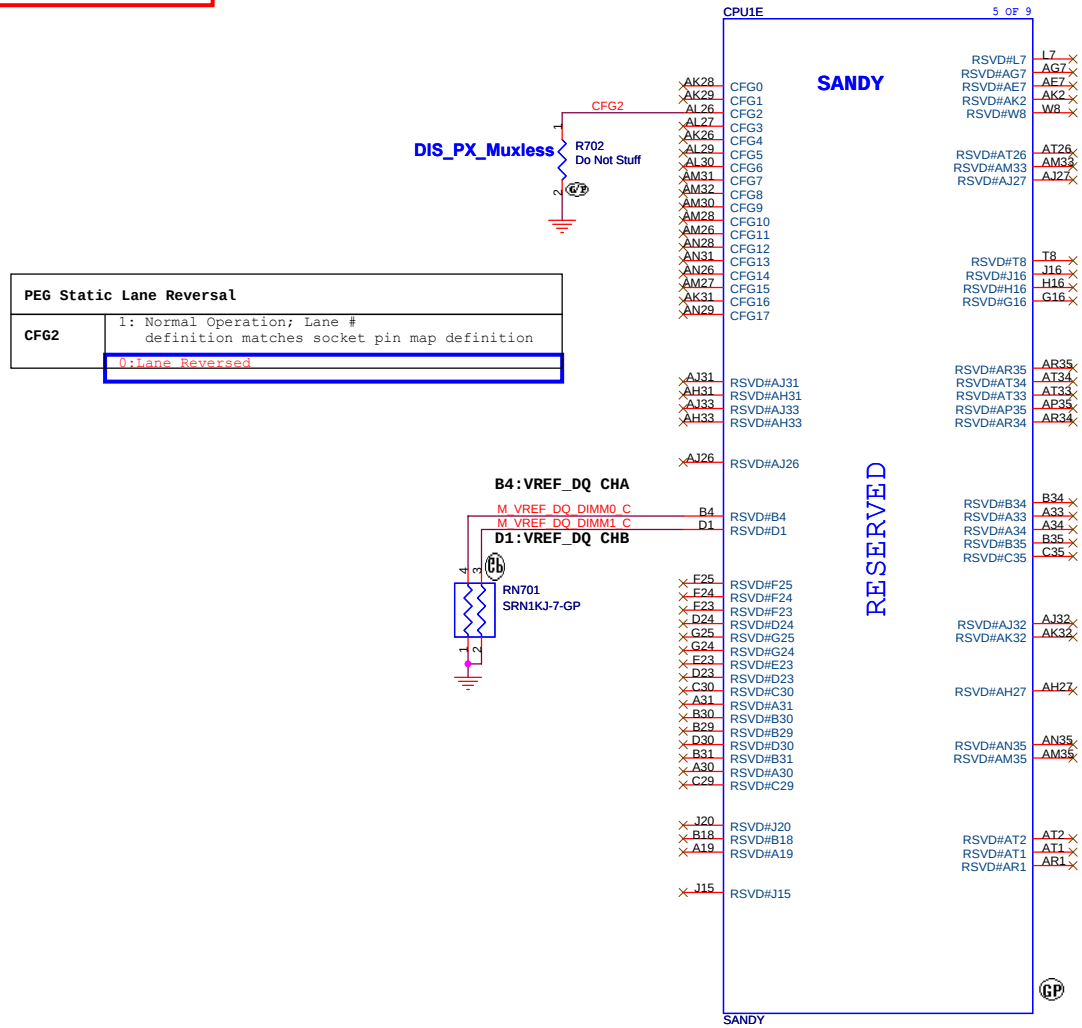
Stuff to disable internal graphics function for power saving.




CPU1B
SANDY
2 OF 9
SANDY
MISC
CLOCKS
THERMAL
DDR3 MISC
PWR MANAGEMENT
JTAG & BPM
SNB_IVB#
SKTOCC#
CATERR#
PECI
PROCHOT#
THERMTRIP#
PM_SYNC
UNCOREPWRGOOD
SM_DRAMPWROK
RESET#
BCLK
BCLK#
DPLL_REF_SSCLK
DPLL_REF_SSCLK#
SM_DRAMRST#
SM_RCOMP0
SM_RCOMP1
SM_RCOMP2
PRDY#
PREQ#
TCK
TMS
TRST#
TDI
TDO
DBR#
BPM#0
BPM#1
BPM#2
BPM#3
BPM#4
BPM#5
BPM#6
BPM#7
1D05V_VTT
H_PROCHOT#
R501
62R2J-GP
C502
SC47P50V2JN-3GP
H_SNB_IVB#
H_PECI
H_PROCHOT# R
R513
56R2J-4-GP
H_THERMTRIP#
H_PM_SYNC
R503
10KR2J-3-GP
H_CPUPWRGD
PM_DRAM_PWRGD
R505
Do Not Stuff
VDDPWRGOOD
BUF_CPU_RST#
CLK_EXP_P
CLK_EXP_N
RN502
Do Not Stuff
CLK_DP_P_R
CLK_DP_N_R
R502
4K99R2F-L-GP
SM_DRAMRST#
SM_RCOMP_0
SM_RCOMP_1
SM_RCOMP_2
R506
R507
R508
140R2F-GP
25D5R2F-GP
200R2F-L-GP
XDP_TRST#
XDP_TDO
XDP_DBRESET#
RN501
SRN51J-GP
RN503
SRN1K5J-1-GP
3D3V_S0
PLT_RST#
Disabling Guidelines:
If motherboard only supports external graphics:
Connect DPLL_REF_SSCLK on Processor to GND through 1K +/- 5% resistor.
Connect DPLL_REF_SSCLK# on Processor to VCCP through 1K +/- 5% resistorpower (~15 mW) may be wasted.
Title
Size
Document Number
Rev
Date:
Sheet



Title	
Size	Document Number
Rev	
Date:	Sheet



Title			
Size	Document Number		Rev
Date:		Sheet	

POWER

6 OF 9

CPU1F

SANDY

PROCESSOR CORE POWER

53A

VCC_CORE

C801 Do Not Stuff
C802 Do Not Stuff
C803 Do Not Stuff
C804 Do Not Stuff
C811 Do Not Stuff
C820 Do Not Stuff
C819 Do Not Stuff
C818 Do Not Stuff
C817 Do Not Stuff
C815 Do Not Stuff

C816 SC10U6D3V5KX-1GP
C821 Do Not Stuff
C822 SC10U6D3V5KX-1GP
C823 SC10U6D3V5KX-1GP
C824 SC10U6D3V5KX-1GP
C825 SC10U6D3V5KX-1GP
C826 SC10U6D3V5KX-1GP
C827 SC10U6D3V5KX-1GP

C837 SC10U6D3V5KX-1GP
C836 SC10U6D3V5KX-1GP
C835 SC10U6D3V5KX-1GP
C834 SC10U6D3V5KX-1GP
C833 SC10U6D3V5KX-1GP
C832 Do Not Stuff
C831 Do Not Stuff
C828 SC10U6D3V5KX-1GP

VCC_CORE

AG35 AG34 AG33 AG32 AG31 AG30 AG29 AG28 AG27 AG26 AE35 AE34 AE33 AE32 AE31 AE30 AE29 AE28 AE27 AE26 AD35 AD34 AD33 AD32 AD31 AD30 AD29 AD28 AD27 AD26 AC35 AC34 AC33 AC32 AC31 AC30 AC29 AC28 AC27 AC26 AA35 AA34 AA33 AA32 AA31 AA30 AA29 AA28 AA27 AA26 Y35 Y34 Y33 Y32 Y31 Y30 Y29 Y28 Y27 Y26 V35 V34 V33 V32 V31 V30 V29 V28 V27 V26 U35 U34 U33 U32 U31 U30 U29 U28 U27 U26 R35 R34 R33 R32 R31 R30 R29 R28 R27 R26 P35 P34 P33 P32 P31 P30 P29 P28 P27 P26 — VCC

CORE SUPPLY

PEG AND DDR

VCCIO: AH13 AH10 AG10 AC10 Y10 U10 P10 L10 J14 J13 J12 J11 H14 H12 H11 G14 G13 G12 F14 F13 F12 F11 E14 E12

1D05V_VTT

C805 SC10U6D3V5KX-1GP
C806 SC10U6D3V5KX-1GP
C807 SC10U6D3V5KX-1GP
C809 SC10U6D3V5KX-1GP
C810 SC10U6D3V5KX-1GP
C838 SC10U6D3V5KX-1GP
C839 SC10U6D3V5KX-1GP
C840 SC10U6D3V5KX-1GP
C841 SC10U6D3V5KX-1GP

VCCIO: F11 D14 D13 D12 D11 C14 C13 C12 C11 B14 B12 A14 A13 A12 A11

1D05V_VTT

C812 SC10U6D3V5KX-1GP
C813 SC10U6D3V5KX-1GP
C814 SC10U6D3V5KX-1GP
C829 SC10U6D3V5KX-1GP
C830 SC10U6D3V5KX-1GP
C842 Do Not Stuff
C843 Do Not Stuff
C844 SC10U6D3V5KX-1GP
C845 SC10U6D3V5KX-1GP

VCCIO: J23

SVID

VIDALERT# AJ29 — H_CPU_SVIDALRT# — R803 43R2J-GP — VR_SVID_ALERT# 42
VIDSCLK AJ30 — H_CPU_SVIDCLK 42
VIDSOUT AJ28 — H_CPU_SVIDDAT 42

For CRB VIDSOUT need to pull high 130 ohm closr to CPU and IMVP7
For CRB VIDALERT# need to pull high 75 ohm close to CPU

1D05V_VTT

H_CPU_SVIDDAT — R804 130R2F-1-GP

SENSE LINES

VCC_CORE

R801 100R2F-L1-GP-U

VCC_SENSE AJ35
VSS_SENSE AJ34
VCCSENSE 42
VSSSENSE 42

R802 100R2F-L1-GP-U

VCCIO_SENSE B10
VSSIO_SENSE A10
VCCIO_SENSE 45
VSSIO_SENSE 45

SANDY

Title		
Size	Document Number	Rev
Date:	Sheet	

POWER

VAXG Output Decoupling Recommendation:
2 x 470 uF at Bottom Socket Edge
2 x 22 uF at Top Socket Cavity
4 x 22 uF at Top Socket Edge
2 x 22 uF at Bottom Socket Cavity
4 x 22 uF at Bottom Socket Edge

R906,R907 close to CPU

VCC_GFXCORE

PROCESSOR VAXG: 24A

C901 Do Not Stuff DY UMA_PX_Muxless
C902 SC10U6D3V5KX-1GP
C903 SC10U6D3V5KX-1GP
C904 SC10U6D3V5KX-1GP
C905 SC10U6D3V5KX-1GP
C906 Do Not Stuff DY UMA_PX_Muxless
C907 Do Not Stuff DY UMA_PX_Muxless
C908 SC10U6D3V5KX-1GP
C918 Do Not Stuff DY UMA_PX_Muxless
C919 SC10U6D3V5KX-1GP
C920 SC10U6D3V5KX-1GP
C921 SC10U6D3V5KX-1GP

VCC_GFXCORE

R903 Do Not Stuff DIS
R904 Do Not Stuff DIS
R905 Do Not Stuff DIS
R901 Do Not Stuff DIS

Disabling Guidelines for External Graphics Designs:
Can connect to GND if motherboard only supports external graphics and if GFX VR is not stuffed.
Can be left floating (Gfx VR keeps VAXG rail from floating) if the VR is stuffed

CPU1G 7 OF 9

SANDY

GRAPHICS: AT24 AT23 AT21 AT20 AT18 AT17 AR24 AR23 AR21 AR20 AR18 AR17 AP24 AP23 AP21 AP20 AP18 AP17 AN24 AN23 AN21 AN20 AN18 AN17 AM24 AM23 AM21 AM20 AM18 AM17 AL24 AL23 AL21 AL20 AL18 AL17 AK24 AK23 AK21 AK20 AK18 AK17 AJ24 AJ23 AJ21 AJ20 AJ18 AJ17 AH24 AH23 AH21 AH20 AH18 AH17 — VAXG

SENSE LINES: VAXG_SENSE AK35 → VCC_AXG_SENSE 42; VSSAXG_SENSE AK34 → VSS_AXG_SENSE 42

VCC_GFXCORE
R906 100R2F-L1-GP-U
VCC_AXG_SENSE
VSS_AXG_SENSE
R907 100R2F-L1-GP-U

Refer to the latest Huron River Mainstream PDG (Doc# 436735) for more details on S3 power reduction implementation.

+V_SM_VREF_CNT should have 10 mil trace width

VREF: SM_VREF AL1 → +V_SM_VREF_CNT 37

Routing Guideline:
Power from DDR_VREF_S3 and +V_SM_VREF_CNT should have 10 mils trace width.

DDR3 -1.5V RAILS

1D5V_S0

PROCESSOR VDDQ: 10A

VDDQ: AF7 AF4 AF1 AC7 AC4 AC1 Y7 Y4 Y1 U7 U4 U1 P7 P4 P1

C909 Do Not Stuff DY
C910 SC10U6D3V5KX-1GP
C911 SC10U6D3V5KX-1GP
C912 SC10U6D3V5KX-1GP
C913 SC10U6D3V5KX-1GP
C914 Do Not Stuff DY

VDDQ Output Decoupling Recommendation:
1 x 330 uF
6 x 10 uF

0D85V_S0

PROCESSOR VCCSA: 6A

C916 Do Not Stuff DY
C915 SC10U6D3V5KX-1GP

VCCSA Output Decoupling Recommendation:
1 x 330 uF
2 x 10 uF at Bottom Socket Cavity
1 x 10 uF at Bottom Socket Edge

SA RAIL: VCCSA: M27 M26 L26 J26 J25 J24 H26 H25

0D85V_S0
R902 10R2J-2-GP
R902 need be close to pin H23.
VCCSA_SENSE H23 → VCCUSA_SENSE
TP901 Do Not Stuff

1.8V RAIL

1D8V_S0

PROCESSOR VCCPLL: 1.2A

C922 SC1U10V2KX-1GP

VCCPLL: B6 A6 A2

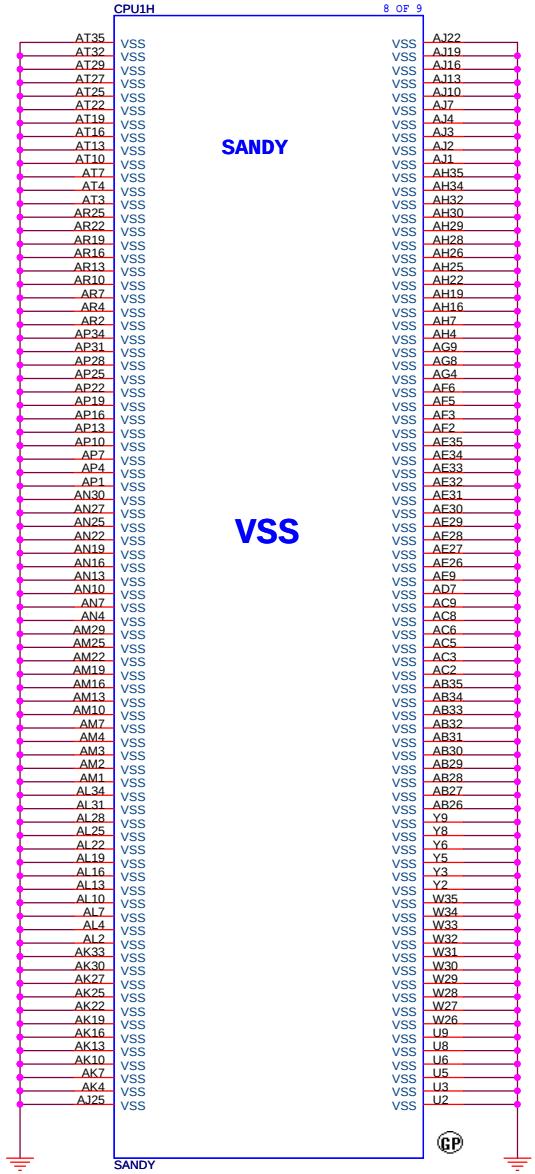
MISC: FC_C22 C22 → H_FC_C22; VCCSA_VID1 C24 → VCCSA_SEL 48

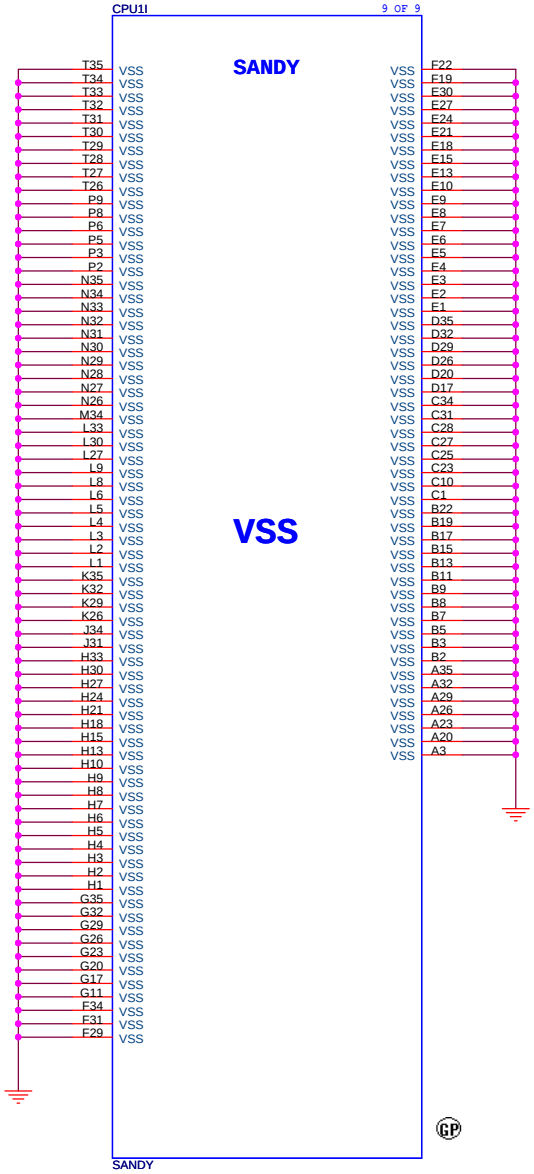
RN901 SRN1KJ-7-GP

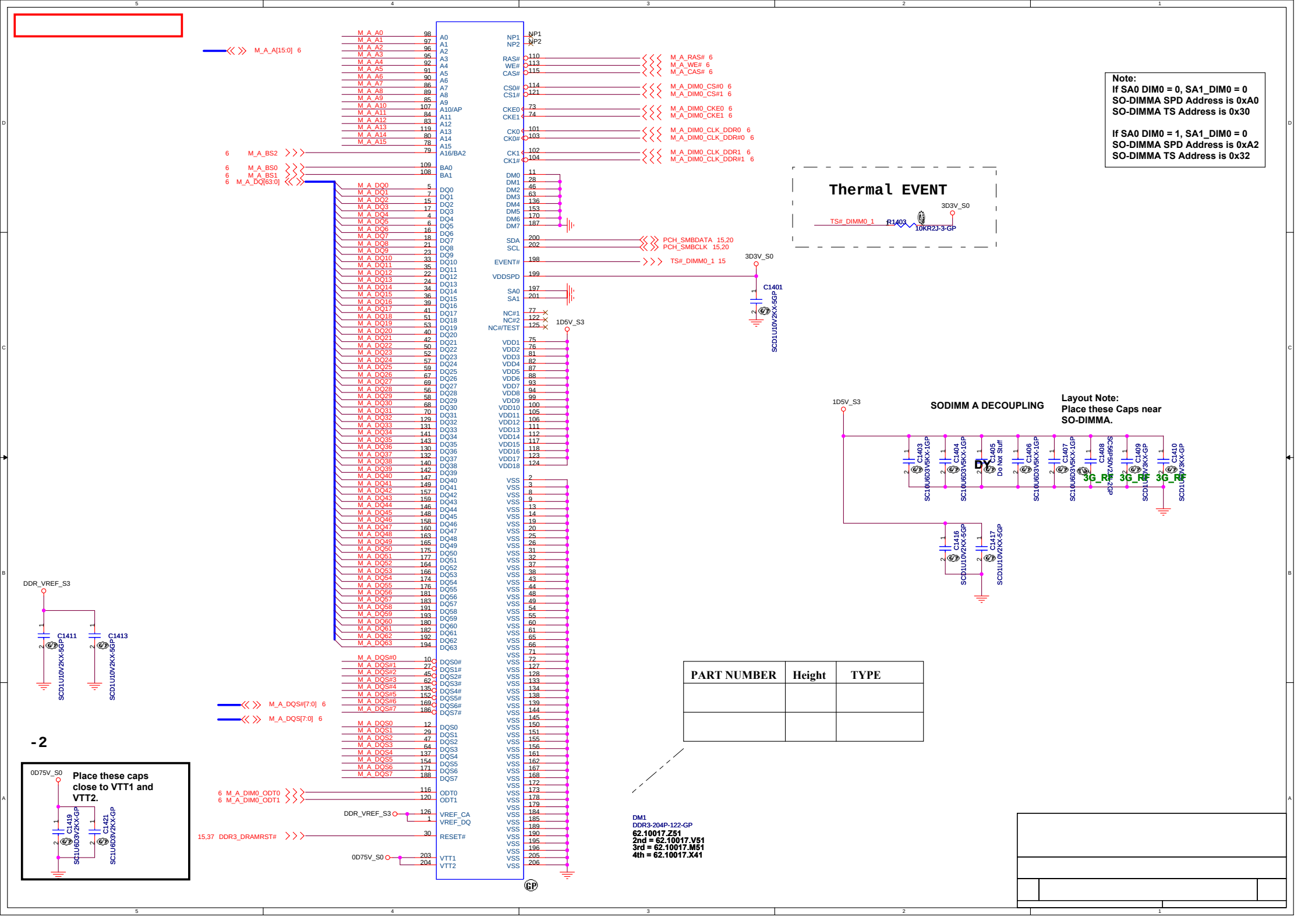
VCCPLL Output Decoupling Recommendation:
1 x 330 uF
2 x 1 uF
1 x 10 uF

SANDY

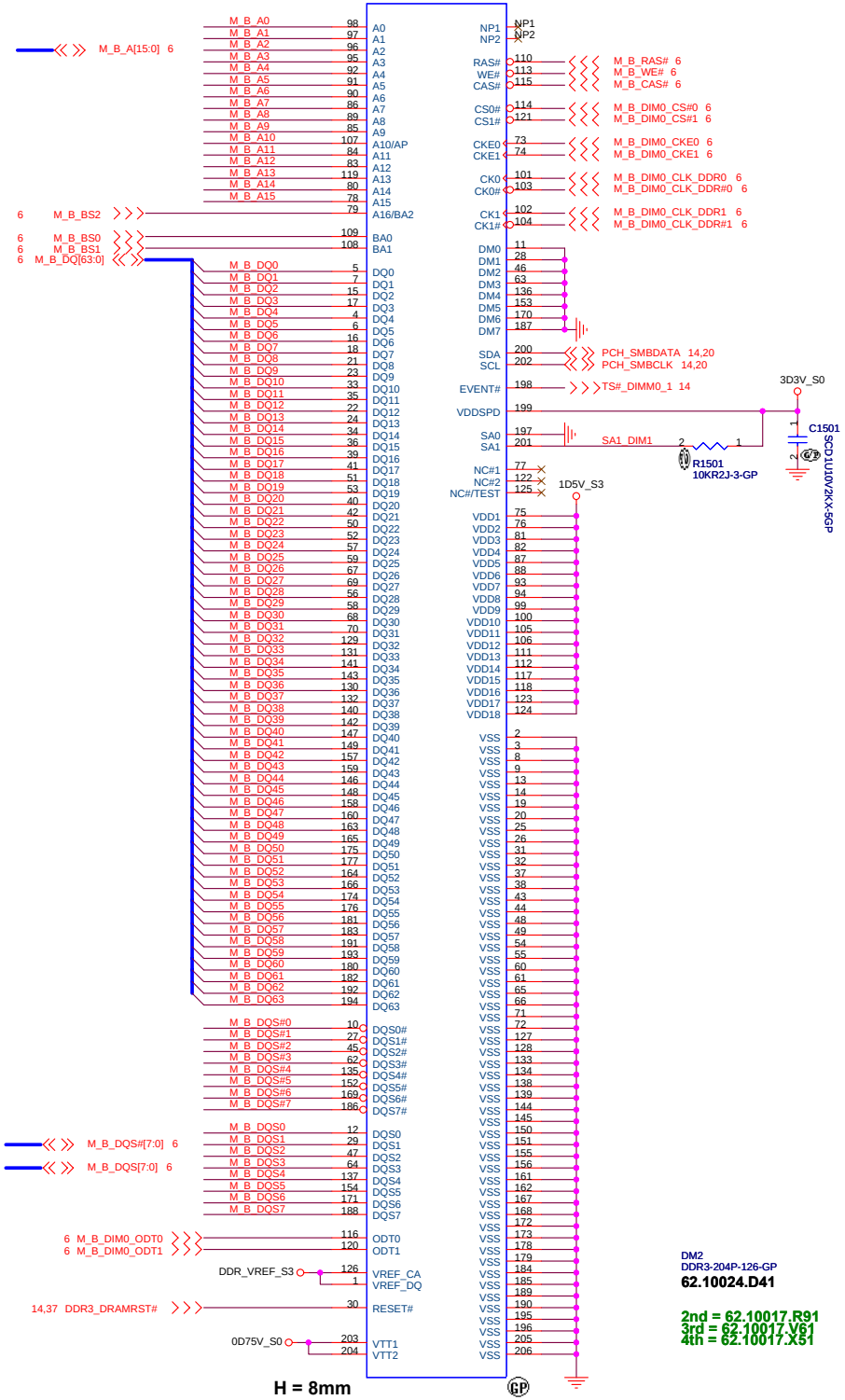
Title			
Size	Document Number		Rev
Date:		Sheet	

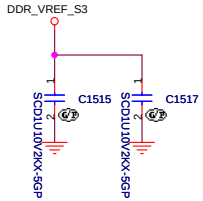

CPU1H
8 OF 9
SANDY
VSS
SANDY
AT35 AT32 AT29 AT27 AT25 AT22 AT19 AT16 AT13 AT10 AT7 AT4 AT3
AR25 AR22 AR19 AR16 AR13 AR10 AR7 AR4 AR2
AP34 AP31 AP28 AP25 AP22 AP19 AP16 AP13 AP10 AP7 AP4 AP1
AN30 AN27 AN25 AN22 AN19 AN16 AN13 AN10 AN7 AN4
AM29 AM25 AM22 AM19 AM16 AM13 AM10 AM7 AM4 AM3 AM2 AM1
AL34 AL31 AL28 AL25 AL22 AL19 AL16 AL13 AL10 AL7 AL4 AL2
AK33 AK30 AK27 AK25 AK22 AK19 AK16 AK13 AK10 AK7 AK4
AJ25
AJ22 AJ19 AJ16 AJ13 AJ10 AJ7 AJ4 AJ3 AJ2 AJ1
AH35 AH34 AH32 AH30 AH29 AH28 AH26 AH25 AH22 AH19 AH16 AH7 AH4
AG9 AG8 AG4
AF6 AF5 AF3 AF2
AE35 AE34 AE33 AE32 AE31 AE30 AE29 AE28 AE27 AE26 AE9
AD7
AC9 AC8 AC6 AC5 AC3 AC2
AB35 AB34 AB33 AB32 AB31 AB30 AB29 AB28 AB27 AB26
Y9 Y8 Y6 Y5 Y3 Y2
W35 W34 W33 W32 W31 W30 W29 W28 W27 W26
U9 U8 U6 U5 U3 U2
GP
SANDY


CPU1I
9 OF 9
SANDY
VSS
SANDY
T35 T34 T33 T32 T31 T30 T29 T28 T27 T26
P9 P8 P6 P5 P3 P2
N35 N34 N33 N32 N31 N30 N29 N28 N27 N26
M34
L33 L30 L27 L9 L8 L6 L5 L4 L3 L2 L1
K35 K32 K29 K26
J34 J31
H33 H30 H27 H24 H21 H18 H15 H13 H10 H9 H8 H7 H6 H5 H4 H3 H2 H1
G35 G32 G29 G26 G23 G20 G17 G11
F34 F31 F29
F22 F19 E30 E27 E24 E21 E18 E15 E13 E10 E9 E8 E7 E6 E5 E4 E3 E2 E1
D35 D32 D29 D26 D20 D17
C34 C31 C28 C27 C25 C23 C10 C1
B22 B19 B17 B15 B13 B11 B9 B8 B7 B5 B3 B2
A35 A32 A29 A26 A23 A20 A3
GP
SANDY

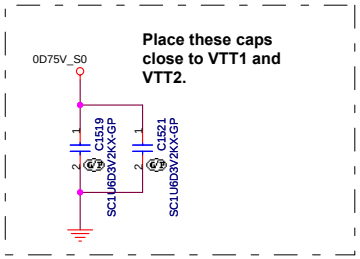

M_A_A[15:0] 6
M_A_BS2 6
M_A_BS0 6
M_A_BS1 6
M_A_DQ[63:0] 6
M_A_DQS#[7:0] 6
M_A_DQS[7:0] 6
M_A_DIM0_ODT0 6
M_A_DIM0_ODT1 6
DDR_VREF_S3
15,37 DDR3_DRAMRST#
0D75V_S0
M_A_RAS# 6
M_A_WE# 6
M_A_CAS# 6
M_A_DIM0_CS#0 6
M_A_DIM0_CS#1 6
M_A_DIM0_CKE0 6
M_A_DIM0_CKE1 6
M_A_DIM0_CLK_DDR0 6
M_A_DIM0_CLK_DDR#0 6
M_A_DIM0_CLK_DDR1 6
M_A_DIM0_CLK_DDR#1 6
PCH_SMBDATA 15,20
PCH_SMBCLK 15,20
TS#_DIMM0_1 15
3D3V_S0
1D5V_S3
DM1
DDR3-204P-122-GP
62.10017.Z51
2nd = 62.10017.V51
3rd = 62.10017.M51
4th = 62.10017.X41
Thermal EVENT
TS#_DIMM0_1
R1403
10KR2J-3-GP
SODIMM A DECOUPLING
Layout Note:
Place these Caps near
SO-DIMMA.
DY
3G_RF
Note:
If SA0 DIM0 = 0, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA0
SO-DIMMA TS Address is 0x30
If SA0 DIM0 = 1, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA2
SO-DIMMA TS Address is 0x32
PART NUMBER
Height
TYPE
-2
Place these caps
close to VTT1 and
VTT2.

SSID = MEMORY

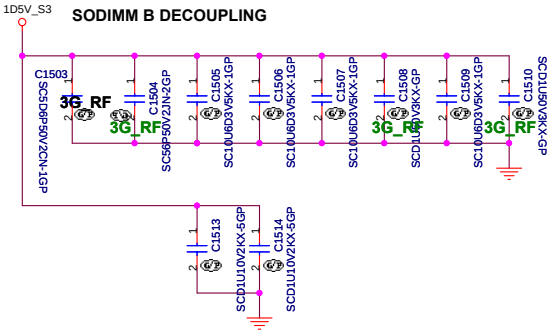




-2

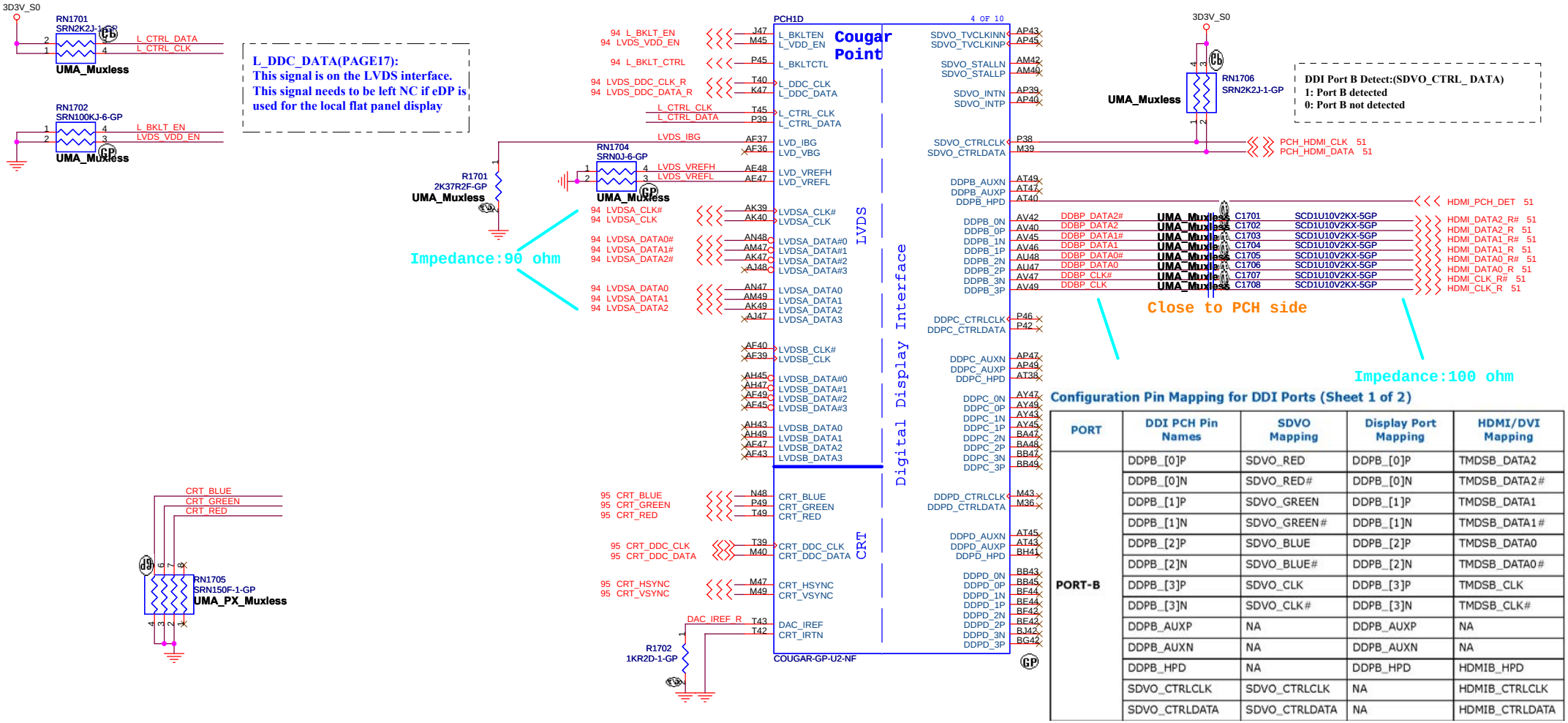


H = 8mm



Layout Note:
Place these Caps near SO-DIMMB.

Title	
Size	Document Number
Rev	
Date:	



Configuration Pin Mapping for DDI Ports (Sheet 1 of 2)

PORT	DDI PCH Pin Names	SDVO Mapping	Display Port Mapping	HDMI/DVI Mapping
PORT-B	DDPB_[0]P	SDVO_RED	DDPB_[0]P	TMDSB_DATA2
	DDPB_[0]N	SDVO_RED#	DDPB_[0]N	TMDSB_DATA2#
	DDPB_[1]P	SDVO_GREEN	DDPB_[1]P	TMDSB_DATA1
	DDPB_[1]N	SDVO_GREEN#	DDPB_[1]N	TMDSB_DATA1#
	DDPB_[2]P	SDVO_BLUE	DDPB_[2]P	TMDSB_DATA0
	DDPB_[2]N	SDVO_BLUE#	DDPB_[2]N	TMDSB_DATA0#
	DDPB_[3]P	SDVO_CLK	DDPB_[3]P	TMDSB_CLK
	DDPB_[3]N	SDVO_CLK#	DDPB_[3]N	TMDSB_CLK#
	DDPB_AUXP	NA	DDPB_AUXP	NA
	DDPB_AUXN	NA	DDPB_AUXN	NA
	DDPB_HPD	NA	DDPB_HPD	HDMIB_HPD
	SDVO_CTRLCLK	SDVO_CTRLCLK	NA	HDMIB_CTRLCLK
	SDVO_CTRLDATA	SDVO_CTRLDATA	NA	HDMIB_CTRLDATA

Title		
Size	Document Number	Rev
Date:	Sheet	

SSID = PCH

RN1801
SRN8K2J-2-GP-U

INT_PIRQH#	1	10	3D3V_S0
INT_PIRQB#	2	9	INT_PIRQD#
INT_PIRQF#	3	8	INT_PIRQE#
INT_PIRQA#	4	7	INT_PIRQC#
3D3V_S0	5	6	USB30_SMI#

A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT#3	Low = A16 swap override/Top-Block Swap Override enabled High = Default

BOOT BIOS Strap

GNT1#/GPIO51	SATA1GP/GPIO19	BOOT BIOS Location
0	0	LPC
0	1	Reserved
		SPI(Default)

PCH1E — 5 OF 10 — Cougar Point — COUGAR-GP-U2-NF

RSVD: TP1–TP20, RSVD, DF_TVS
NVRAM: RSVD, NV_CLE
PCI: PIRQA#, PIRQB#, PIRQC#, PIRQD#, REQ1#/GPIO50, REQ2#/GPIO52, REQ3#/GPIO54, GNT1#/GPIO51, GNT2#/GPIO53, GNT3#/GPIO55, PIRQE#/GPIO2, PIRQF#/GPIO3, PIRQG#/GPIO4, PIRQH#/GPIO5, PME#, PLTRST#, CLKOUT_PCI0–CLKOUT_PCI4
USB: USBP0N/P – USBP13N/P, USBRBIAS#, USBRBIAS, OC0#/GPIO59 – OC7#/GPIO14

DMI & FDI Termination Voltage	
NV_CLE	Set to Vss when LOW Set to Vcc when HIGH

1D8V_S0 — R1808 2K2R2J-2-GP — NV_CLE — R1809 1KR2J-1-GP — H_SNB_IVB# 5

RN1803
SRN10KJ-5-GP
DGPU_HOLD_RST# 2
DGPU_PWR_EN# 1
4

USB Ext. port 1 (HS)
External debug port use on Huron river platform

USB Table

Pair	Device
0	Touch Panel / 3G SIM
1	USB Ext. port 1 (HS)
2	Fingerprint
3	BLUETOOTH
4	Mini Card2 (WWAN)
5	CARD READER(DY)
6	X
7	X
8	USB Ext. port 4 / E-SATA /USB CHARGER
9	USB Ext. port 2
10	EDP CAMERA
11	Mini Card1 (WLAN)
12	CAMERA
13	New Card

Do Not Stuff TP1806 — 83 DGPU_HOLD_RST# — DGPU_SELECT#
93 DGPU_PWR_EN#
Do Not Stuff TP1804 — DGPU_PWM_SELECT#

R1813 Do Not Stuff
56 SATA_ODD_DA#
82 USB30_SMI#
INT_PIRQE#, INT_PIRQF#, INT_PIRQH#

USB_RBIAS — R1811 22D6R2F-L1-GP

3D3V_S5 — R1820 10KR2J-3-GP

5,27,31,36,65,66,71,82,97 PLT_RST#

71 CLK_PCI_LPC — R1804 22R2J-2-GP — CLK_PCI_LPC_R
20 CLK_PCI_FB — R1805 22R2J-2-GP — CLK_PCI_FB_R
27 CLK_PCI_KBC — R1806 22R2J-2-GP — CLK_PCI_KBC_R

EC1803 DY Do Not Stuff
EC1802 DY Do Not Stuff
EC1801 DY Do Not Stuff

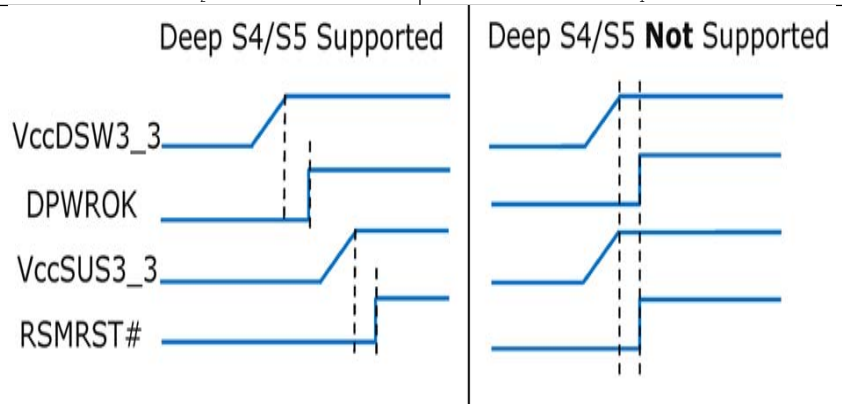
OC[3:0]# for Device 29 (Ports 0-7)
OC[7:4]# for Device 26 (Ports 8-13)

USB 2.0 Overcurrent Pin Default Usage

Pin	Default Port Mapping	Pin	Default Port Mapping
OC0#	Port 0, Port 1	OC4#	Port 8, Port 9
OC1#	Port 2, Port 3	OC5#	Port 10, Port 11
OC2#	Port 4, Port 5	OC6#	Port 12, Port 13
OC3#	Port 6, Port 7	OC7#	Not Used

Title
Size | Document Number | Rev
Date: | Sheet

SSID = PCH



PCH1C — 3 OF 10 — Cougar Point — DMI / FDI / System Power Management

DMI0RXN	BC24	4 DMI_RXN0	
DMI1RXN	BE20	4 DMI_RXN1	
DMI2RXN	BG18	4 DMI_RXN2	
DMI3RXN	BG20	4 DMI_RXN3	
DMI0RXP	BE24	4 DMI_RXP0	
DMI1RXP	BC20	4 DMI_RXP1	
DMI2RXP	BJ18	4 DMI_RXP2	
DMI3RXP	BJ20	4 DMI_RXP3	
DMI0TXN	AW24	4 DMI_TXN0	
DMI1TXN	AW20	4 DMI_TXN1	
DMI2TXN	BB18	4 DMI_TXN2	
DMI3TXN	AV18	4 DMI_TXN3	
DMI0TXP	AY24	4 DMI_TXP0	
DMI1TXP	AY20	4 DMI_TXP1	
DMI2TXP	AY18	4 DMI_TXP2	
DMI3TXP	AU18	4 DMI_TXP3	
DMI_ZCOMP	BJ24	1D05V_VTT, R1901 1 49D9R2F-GP DMI_COMP_R	
DMI_IRCOMP	BG25		
DMI2RBIAS	BH21	R1902 1 750R2F-GP RBIAS_CPY	
SUSACK#	C12	SUS_PWR_ACK	
SYS_RESET#	K3	3D3V_S0, R1905 10KR2J-3-GP, SYS_RESET#	
SYS_PWROK	P12	36 SYS_PWROK	
PWROK	L22	27,42 S0_PWR_GOOD, 2 R1924 Do Not Stuff 1 PWROK	
APWROK	L10		
DRAMPWROK	B13	5,37 PM_DRAM_PWRGD	
RSMRST#	C21	PM_RSMRST#	
SUSWARN#/SUSPWRDNACK/GPIO30	K16	27 SUS_PWR_ACK	
PWRBTN#	E20	27,97 PM_PWRBTN#	
ACPRESENT/GPIO31	H20	27 AC_PRESENT	
BATLOW#/GPIO72	E10	BATLOW#	
RI#	A10	PM_RI#	
COUGAR-GP-U2-NF			

FDI_RXN0	BJ14	FDI_TXN0 4
FDI_RXN1	AY14	FDI_TXN1 4
FDI_RXN2	BE14	FDI_TXN2 4
FDI_RXN3	BH13	FDI_TXN3 4
FDI_RXN4	BC12	FDI_TXN4 4
FDI_RXN5	BJ12	FDI_TXN5 4
FDI_RXN6	BG10	FDI_TXN6 4
FDI_RXN7	BG9	FDI_TXN7 4
FDI_RXP0	BG14	FDI_TXP0 4
FDI_RXP1	BB14	FDI_TXP1 4
FDI_RXP2	BF14	FDI_TXP2 4
FDI_RXP3	BG13	FDI_TXP3 4
FDI_RXP4	BE12	FDI_TXP4 4
FDI_RXP5	BG12	FDI_TXP5 4
FDI_RXP6	BJ10	FDI_TXP6 4
FDI_RXP7	BH9	FDI_TXP7 4
FDI_INT	AW16	FDI_INT 4
FDI_FSYNC0	AV12	FDI_FSYNC0 4
FDI_FSYNC1	BC10	FDI_FSYNC1 4
FDI_LSYNC0	AV14	FDI_LSYNC0 4
FDI_LSYNC1	BB10	FDI_LSYNC1 4
DSWVRMEN	A18	DSWODVREN
DPWROK	F22	PCH_DPWROK, R1910 Do Not Stuff, DY, R1911 Do Not Stuff, PM_RSMRST#, RTC_AUX_S5
WAKE#	B9	PCIE_WAKE# 31,65,66,82
CLKRUN#/GPIO32	N3	PM_CLKRUN# 27
SUS_STAT#/GPIO61	G8	
SUSCLK/GPIO62	N14	PCH_SUSCLK_KBC 27
SLP_S5#/GPIO63	D10	
SLP_S4#	H4	PM_SLP_S4# 27,46
SLP_S3#	F4	PM_SLP_S3# 27,36,37,47,92
SLP_A#	G10	
SLP_SUS#	G16	
PMSYNCH	AP14	H_PM_SYNC 5
SLP_LAN#/GPIO29	K14	

R1926 Do Not Stuff, DY, R1904 100KR2J-1-GP — SYS_PWROK, PWROK

0628 Modify:
Change R1904 to 100K 0402 from 10K and default stuff.

S0_PWR_GOOD after PM_SLP_S3# delay 200 ms

DSWODVREN - On Die DSW VR Enable	
HIGH	Enabled (DEFAULT)
LOW	Disabled

SB modify

RTC_AUX_S5 — R1917 330KR2J-L1-GP — DSWODVREN — R1918 DY Do Not Stuff

PM_CLKRUN# — R1919 8K2R2J-3-GP — 3D3V_S0

3D3V_S5 — RN1901 SRN10KJ-6-GP — BATLOW#, PM_RI#, AC_PRESENT, SUS_PWR_ACK — R1921 10KR2J-3-GP — PCIE_WAKE#

PCIE_WAKE#
CRB : 1K
CEKLT: 10K

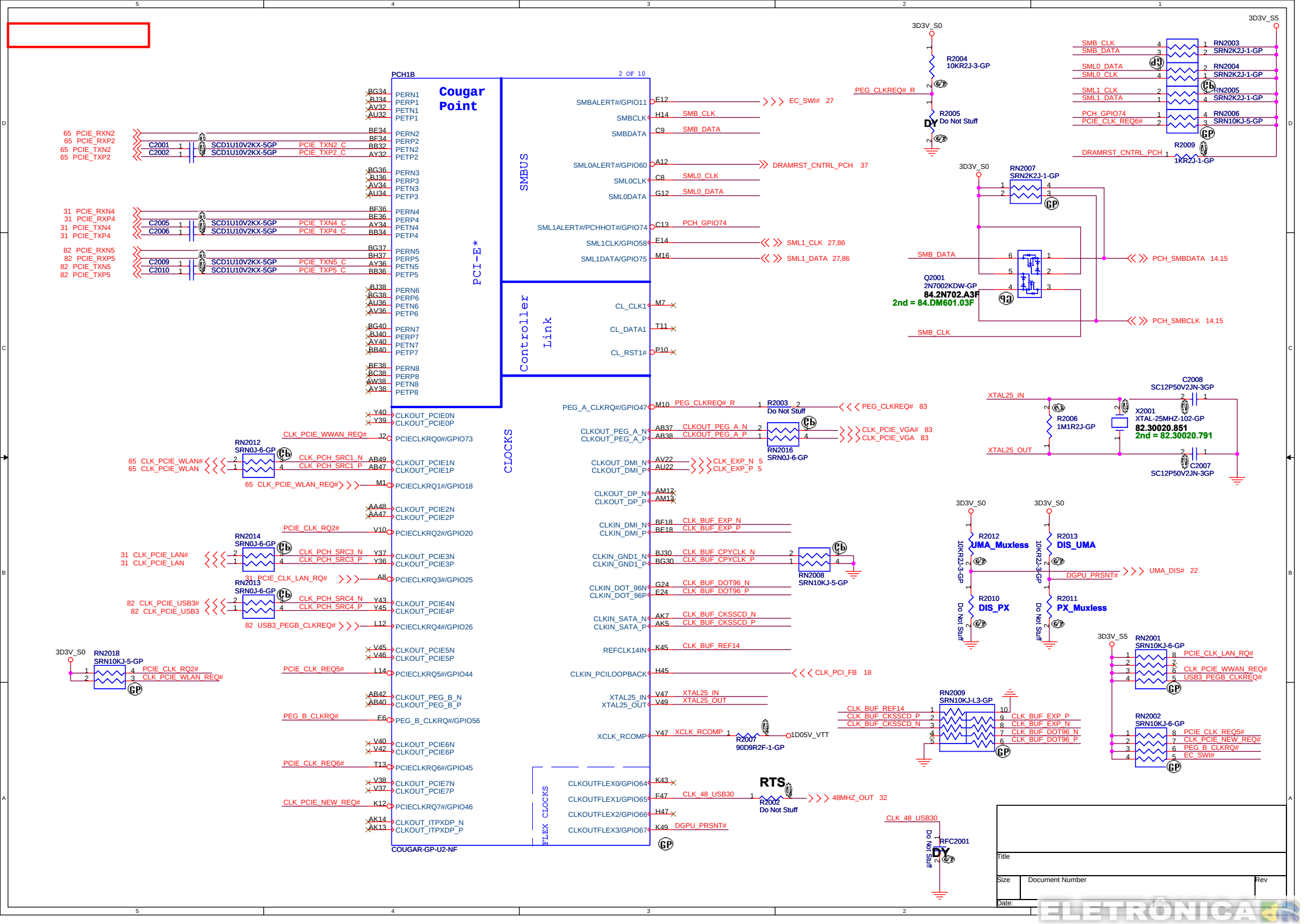
PWRBTN#
This signal has an internal pull-up resistor

R1908 100KR2J-1-GP — PM_RSMRST#

3D3V_AUX_S5 — R1909 100KR2J-1-GP — R1916 10KR2J-3-GP — 3V_5V_POK_# — Q1901 2N7002KDW-GP — PM_RSMRST# — R1912 1KR2J-1-GP — RSMRST#_KBC 27 — 3V_5V_POK 41

84.2N702.A3F
2nd = 84.DM601.03F

Title		
Size	Document Number	Rev
Date:		Sheet


PCH1B
Cougar Point
2 OF 10
PCI-E*
SMBUS
Controller Link
CLOCKS
FLEX CLOCKS
COUGAR-GP-U2-NF
3D3V_S0
3D3V_S5
R2004 10KR2J-3-GP
R2005 Do Not Stuff
R2009 1KR2J-1-GP
RN2003 SRN2K2J-1-GP
RN2004 SRN2K2J-1-GP
RN2005 SRN2K2J-1-GP
RN2006 SRN10KJ-5-GP
RN2007 SRN2K2J-1-GP
Q2001 2N7002KDW-GP
84.2N702.A3F
2nd = 84.DM601.03F
SMB_CLK
SMB_DATA
SML0_CLK
SML0_DATA
SML1_CLK
SML1_DATA
PCH_GPIO74
PCIE_CLK_REQ6#
DRAMRST_CNTRL_PCH
PCH_SMBDATA 14,15
PCH_SMBCLK 14,15
PEG_CLKREQ# R
EC_SWI# 27
DRAMRST_CNTRL_PCH 37
SML1_CLK 27,86
SML1_DATA 27,86
C2001 SCD1U10V2KX-5GP
C2002 SCD1U10V2KX-5GP
C2005 SCD1U10V2KX-5GP
C2006 SCD1U10V2KX-5GP
C2009 SCD1U10V2KX-5GP
C2010 SCD1U10V2KX-5GP
65 PCIE_RXN2
65 PCIE_RXP2
65 PCIE_TXN2
65 PCIE_TXP2
31 PCIE_RXN4
31 PCIE_RXP4
31 PCIE_TXN4
31 PCIE_TXP4
82 PCIE_RXN5
82 PCIE_RXP5
82 PCIE_TXN5
82 PCIE_TXP5
RN2012 SRN0J-6-GP
RN2013 SRN0J-6-GP
RN2014 SRN0J-6-GP
RN2016 SRN0J-6-GP
RN2008 SRN10KJ-5-GP
RN2018 SRN10KJ-5-GP
RN2009 SRN10KJ-L3-GP
RN2001 SRN10KJ-6-GP
RN2002 SRN10KJ-6-GP
R2003 Do Not Stuff
R2002 Do Not Stuff
R2007 90D9R2F-1-GP
R2006 1M1R2J-GP
X2001 XTAL-25MHZ-102-GP
82.30020.851
2nd = 82.30020.791
C2008 SC12P50V2JN-3GP
C2007 SC12P50V2JN-3GP
R2012 UMA_Muxless
R2013 DIS_UMA
R2010 DIS_PX
R2011 PX_Muxless
RFC2001
CLK_PCIE_WWAN_REQ#
CLK_PCIE_WLAN#
CLK_PCIE_WLAN
CLK_PCIE_WLAN_REQ#
CLK_PCIE_LAN#
CLK_PCIE_LAN
PCIE_CLK_LAN_RQ#
CLK_PCIE_USB3#
CLK_PCIE_USB3
USB3_PEGB_CLKREQ#
PCIE_CLK_RQ2#
PCIE_CLK_REQ5#
PEG_B_CLKRQ#
PCIE_CLK_REQ6#
CLK_PCIE_NEW_REQ#
PEG_A_CLKRQ#/GPIO47
CLKOUT_PEG_A_N
CLKOUT_PEG_A_P
CLKOUT_DMI_N
CLKOUT_DMI_P
CLKOUT_DP_N
CLKOUT_DP_P
CLKIN_DMI_N
CLKIN_DMI_P
CLKIN_GND1_N
CLKIN_GND1_P
CLKIN_DOT_96N
CLKIN_DOT_96P
CLKIN_SATA_N
CLKIN_SATA_P
REFCLK14IN
CLKIN_PCILOOPBACK
XTAL25_IN
XTAL25_OUT
XCLK_RCOMP
CLKOUTFLEX0/GPIO64
CLKOUTFLEX1/GPIO65
CLKOUTFLEX2/GPIO66
CLKOUTFLEX3/GPIO67
CLK_48_USB30
DGPU_PRSNT#
UMA_DIS# 22
CLK_EXP_N 5
CLK_EXP_P 5
CLK_PCIE_VGA# 83
CLK_PCIE_VGA 83
PEG_CLKREQ# 83
48MHZ_OUT 32
1D05V_VTT
CL_CLK1
CL_DATA1
CL_RST1#
RTS
Title
Size
Document Number
Rev
Date:
Sheet

SSID = PCH

RTC_X1
RTC_X2
R2101 10MR2J-L-GP
X2101
X-32D768KHZ-34GPU
82.30001.661
2nd = 82.30001.B21
C2101 SC5P50V2CN-2GP
C2102 SC5P50V2CN-2GP

RTC_AUX_S5
RN2104 SRN20KJ-GP-U
C2103 SC1U6D3V2KX-GP
C2104 SC1U6D3V2KX-GP
G2101 Do Not Stuff

INTVRMEN- Integrated SUS 1.05V VRM Enable
High - Enable internal VRs
Low - Enable external VRs

R2122 33R2J-2-GP
29 HDA_CODEC_SYNC
29 HDA_CODEC_SDOUT
HDA_SYNC
HDA_SDOUT
R2123 33R2J-2-GP
29 HDA_CODEC_RST#
29 HDA_CODEC_BITCLK
HDA_RST#
HDA_BITCLK
RN2102 SRN33J-5-GP-U

Flash Descriptor Security Overide	
HDA_SDOUT	Low = Default High = Enable

+3VS_+1.5VS_HDA_IO
R2102 Do Not Stuff
HDA_SDOUT

No Reboot Strap	
HDA_SPKR	Low = Default High = No Reboot

PLL ODVR VOLTAGE	
HDA_SYNC	Low = 1.8V (Default) High = 1.5V

+3VS_+1.5VS_HDA_IO
R2103 1KR2J-1-GP
HDA_SYNC

This signal has a weak internal pull down.
On Die PLL VR is supplied by 1.5V when sampled high, 1.8 V when sampled low.
Needs to be pulled High for Huron River platform.
co-operate with R2310

5V_S0
Q2101 Do Not Stuff
Do Not Stuff
2ND = 84.2N702.031
HDA_CODEC_SYNC
HDA_SYNC_R
R2124 Do Not Stuff
HDA_SYNC

HDA_SYNC: This strap is sampled on rising edge of RSMRST# and is used to sample 1.5V VccVRM supply mode. 1K external pull-up resistor is required on this signal on the board. Signal may have leakage paths via powered off devices (Audio Codec) and hence contend with the external pull-up. A blocking FET is recommended in such a case to isolate HDA_SYNC from the Audio Codec device until after the Strap sampling is complete.

27 ME_UNLOCK
R2107 1KR2J-1-GP
HDA_SDOUT

R2121 4K7R2J-2-GP
PCH_JTAG_TCK_BUF

27,60 SPI_CLK_R
27,60 SPI_CS0#_R
27,60 SPI_SI_R
27,60 SPI_SO_R
R2108 33R2J-2-GP
R2109 33R2J-2-GP
R2110 33R2J-2-GP
PCH_SPI_CLK
PCH_SPI_CS0#
PCH_SPI_SI

HDA_CODEC_BITCLK
HDA_CODEC_SDOUT
SPI_CS0#_R
EC2102 DY Do Not Stuff
EC2103 DY Do Not Stuff
EC2101 DY Do Not Stuff

PCH1A 1 OF 10
Cougar Point
COUGAR-GP-U2-NF

RTC_X1 A20 RTCX1
RTC_X2 C20 RTCX2
RTC_RST# D20 RTCRST#
SRTC_RST# G22 SRTCRST#
SM_INTRUDER# K22 INTRUDER#
PCH_INTVRMEN C17 INTVRMEN
RTC_AUX_S5 R2104 1M1R2J-GP R2105 330KR2F-L-GP

HDA_BITCLK N34 HDA_BCLK
HDA_SYNC L34 HDA_SYNC
29 HDA_SPKR T10 SPKR
HDA_RST# K34 HDA_RST#
29 HDA_SDIN0 E34 HDA_SDIN0
G34 HDA_SDIN1
C34 HDA_SDIN2
A34 HDA_SDIN3
HDA_SDOUT A36 HDA_SDO
C36 HDA_DOCK_EN#/GPIO33
N32 HDA_DOCK_RST#/GPIO13

JTAG_TCK J3
JTAG_TMS H7
JTAG_TDI K5
JTAG_TDO H1

SPI_CLK T3
SPI_CS0# Y14
SPI_CS1# T1
SPI_MOSI V4
SPI_MISO U3

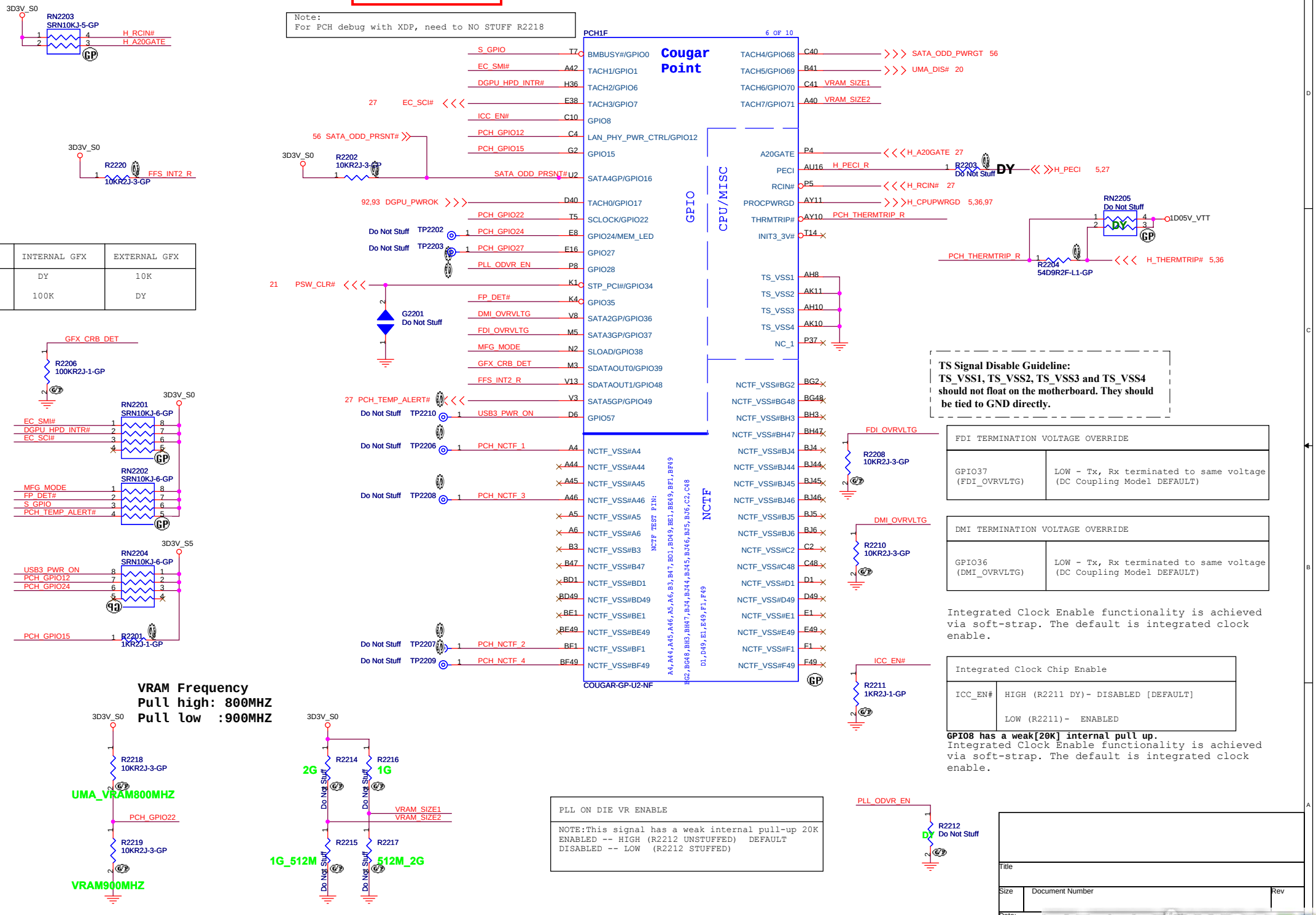
LPC
FWH0/LAD0 C38 LPC_AD0
FWH1/LAD1 A38 LPC_AD1
FWH2/LAD2 B37 LPC_AD2
FWH3/LAD3 C37 LPC_AD3
LPC_AD[0..3] 27,71
FWH4/LFRAME# D36 LPC_FRAME# 27,71
LDRQ0# E36
LDRQ1#/GPIO23 K36
SERIRQ V5 INT_SERIRQ 27

SATA 6G
SATA0RXN AM3 SATA_RXN0 56
SATA0RXP AM1 SATA_RXP0 56
SATA0TXN AP7 SATA_TXN0 56
SATA0TXP AP5 SATA_TXP0 56
HDD1
SATA1RXN AM10
SATA1RXP AM8
SATA1TXN AP11
SATA1TXP AP10
SATA2RXN AD7
SATA2RXP AD5
SATA2TXN AH5
SATA2TXP AH4

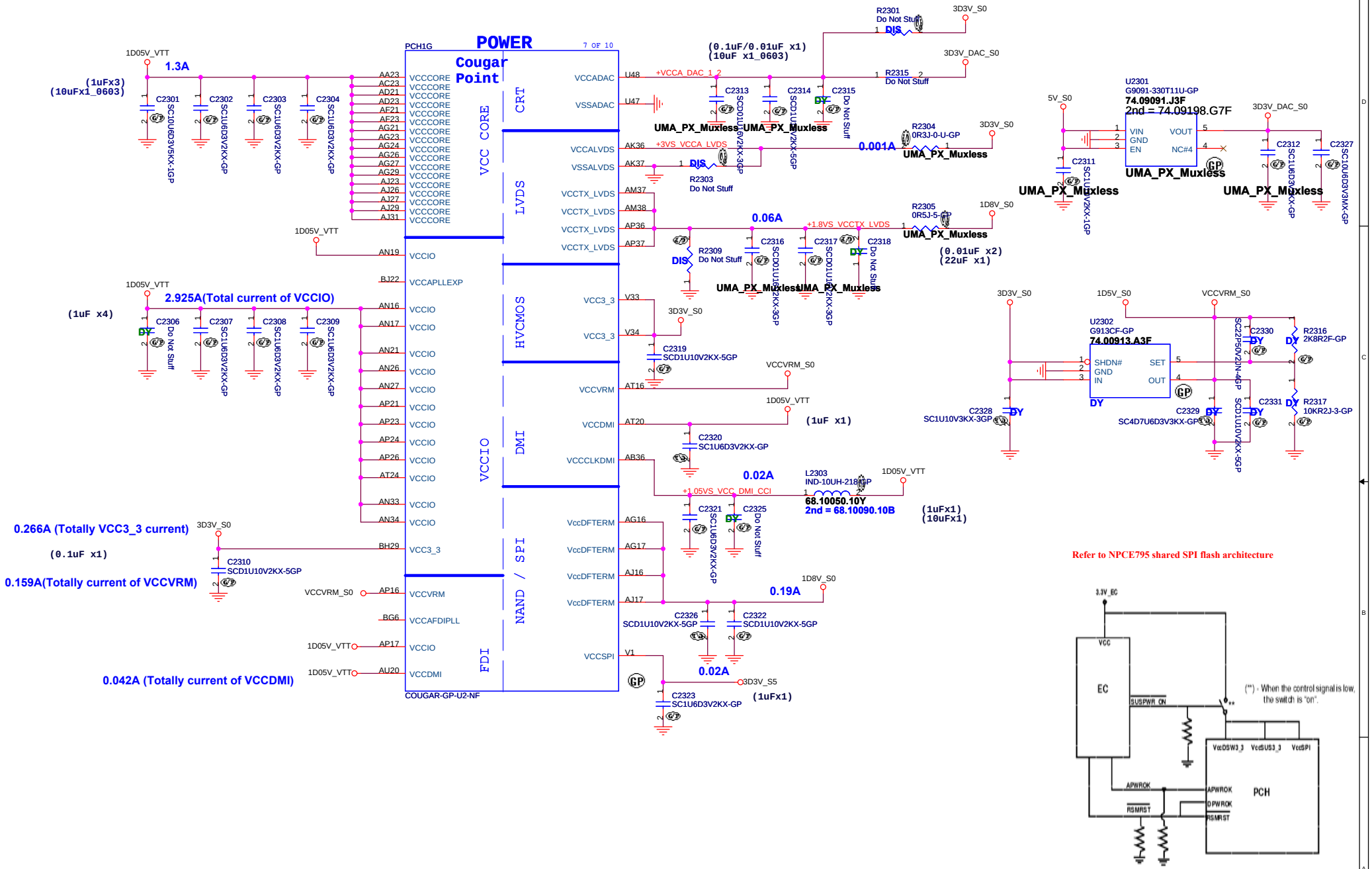
SATA
SATA3RXN AB8
SATA3RXP AB10
SATA3TXN AF3
SATA3TXP AF1
SATA4RXN Y7 SATA_RXN4 56
SATA4RXP Y5 SATA_RXP4 56
SATA4TXN AD3 SATA_TXN4 56
SATA4TXP AD1 SATA_TXP4 56
ODD
SATA5RXN Y3
SATA5RXP Y1
SATA5TXN AB3
SATA5TXP AB1
ESATA
SATAICOMPO Y11
SATAICOMPI Y10 SATA_COMP R2112 37D4R2F-GP 1D05V_VTT
SATA3RCOMPO AB12
SATA3COMPI AB13 SATA3_COMP R2113 49D9R2F-GP 1D05V_VTT
SATA3RBIAS AH1 RBIAS_SATA3 R2114 750R2F-GP
SATALED# P3 SATA_LED# 68
SATA0GP/GPIO21 V14 SATA_DET#0
SATA1GP/GPIO19 P1

22 PSW_CLR#
RN2103 SRN10KJ-6-GP 3D3V_S0
SATA_LED#
INT_SERIRQ
SATA_DET#0

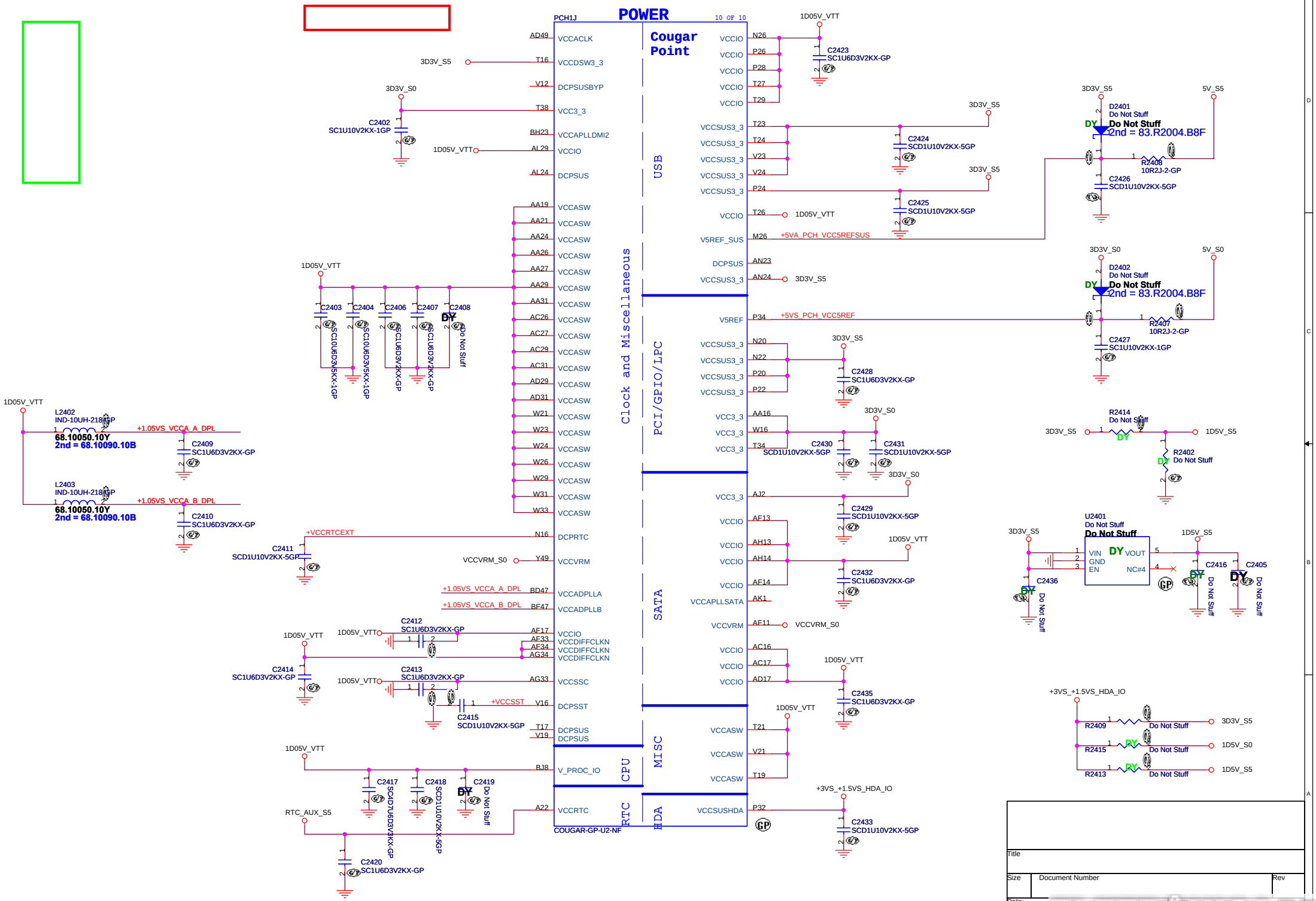
Title			
Size	Document Number		Rev
Date:		Sheet	

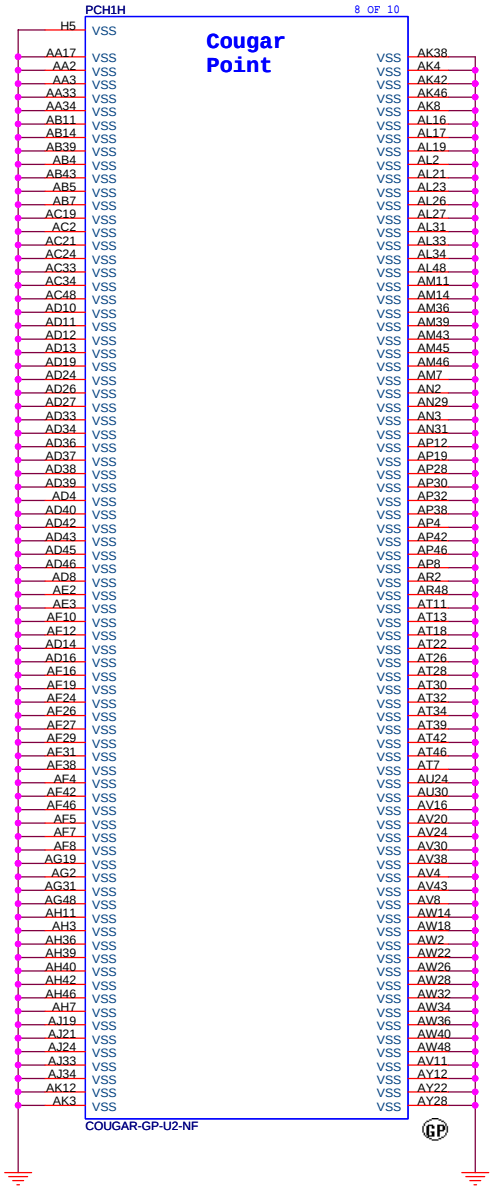

3D3V_S0
RN2203
SRN10KJ-5-GP
H_RCIN#
H_A20GATE
Note:
For PCH debug with XDP, need to NO STUFF R2218
PCH1F
6 OF 10
Cougar Point
GPIO
CPU/MISC
NCTF
S_GPIO
EC_SMI#
DGPU_HPD_INTR#
27 EC_SCI#
ICC_EN#
56 SATA_ODD_PRSNT#
PCH_GPIO12
PCH_GPIO15
92,93 DGPU_PWROK
PCH_GPIO22
Do Not Stuff TP2202
PCH_GPIO24
Do Not Stuff TP2203
PCH_GPIO27
PLL_ODVR_EN
21 PSW_CLR#
G2201
Do Not Stuff
FP_DET#
DMI_OVRVLTG
FDI_OVRVLTG
MFG_MODE
GFX_CRB_DET
FFS_INT2_R
27 PCH_TEMP_ALERT#
Do Not Stuff TP2210
USB3_PWR_ON
Do Not Stuff TP2206
PCH_NCTF_1
Do Not Stuff TP2208
PCH_NCTF_3
Do Not Stuff TP2207
PCH_NCTF_2
Do Not Stuff TP2209
PCH_NCTF_4
BMBUSY#/GPIO0
TACH1/GPIO1
TACH2/GPIO6
TACH3/GPIO7
GPIO8
LAN_PHY_PWR_CTRL/GPIO12
GPIO15
SATA4GP/GPIO16
TACH0/GPIO17
SCLOCK/GPIO22
GPIO24/MEM_LED
GPIO27
GPIO28
STP_PCI#/GPIO34
GPIO35
SATA2GP/GPIO36
SATA3GP/GPIO37
SLOAD/GPIO38
SDATAOUT0/GPIO39
SDATAOUT1/GPIO48
SATA5GP/GPIO49
GPIO57
NCTF_VSS#A4
NCTF_VSS#A44
NCTF_VSS#A45
NCTF_VSS#A46
NCTF_VSS#A5
NCTF_VSS#A6
NCTF_VSS#B3
NCTF_VSS#B47
NCTF_VSS#BD1
NCTF_VSS#BD49
NCTF_VSS#BE1
NCTF_VSS#BE49
NCTF_VSS#BF1
NCTF_VSS#BF49
NCTF TEST PIN: A4,A44,A45,A46,A5,A6,B3,B47,BD1,BD49,BE1,BE49,BF1,BF49
BG2,BG48,BH3,BH47,BJ4,BJ44,BJ45,BJ46,BJ5,BJ6,C2,C48
D1,D49,E1,E49,F1,F49
COUGAR-GP-U2-NF
TACH4/GPIO68
TACH5/GPIO69
TACH6/GPIO70
TACH7/GPIO71
A20GATE
PECI
RCIN#
PROCPWRGD
THRMTRIP#
INIT3_3V#
TS_VSS1
TS_VSS2
TS_VSS3
TS_VSS4
NC_1
NCTF_VSS#BG2
NCTF_VSS#BG48
NCTF_VSS#BH3
NCTF_VSS#BH47
NCTF_VSS#BJ4
NCTF_VSS#BJ44
NCTF_VSS#BJ45
NCTF_VSS#BJ46
NCTF_VSS#BJ5
NCTF_VSS#BJ6
NCTF_VSS#C2
NCTF_VSS#C48
NCTF_VSS#D1
NCTF_VSS#D49
NCTF_VSS#E1
NCTF_VSS#E49
NCTF_VSS#F1
NCTF_VSS#F49
SATA_ODD_PWRGT 56
UMA_DIS# 20
VRAM_SIZE1
VRAM_SIZE2
H_A20GATE 27
H_PECI_R
R2203
Do Not Stuff
DY
H_PECI 5,27
H_RCIN# 27
H_CPUPWRGD 5,36,97
PCH_THERMTRIP_R
H_THERMTRIP# 5,36
RN2205
Do Not Stuff
1D05V_VTT
R2204
54D9R2F-L1-GP
TS Signal Disable Guideline:
TS_VSS1, TS_VSS2, TS_VSS3 and TS_VSS4 should not float on the motherboard. They should be tied to GND directly.
FDI TERMINATION VOLTAGE OVERRIDE
GPIO37 (FDI_OVRVLTG)
LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)
DMI TERMINATION VOLTAGE OVERRIDE
GPIO36 (DMI_OVRVLTG)
LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)
Integrated Clock Enable functionality is achieved via soft-strap. The default is integrated clock enable.
Integrated Clock Chip Enable
ICC_EN# HIGH (R2211 DY)- DISABLED [DEFAULT]
LOW (R2211)- ENABLED
GPIO8 has a weak[20K] internal pull up.
Integrated Clock Enable functionality is achieved via soft-strap. The default is integrated clock enable.
PLL ON DIE VR ENABLE
NOTE:This signal has a weak internal pull-up 20K
ENABLED -- HIGH (R2212 UNSTUFFED) DEFAULT
DISABLED -- LOW (R2212 STUFFED)
PLL_ODVR_EN
R2212
DY
Do Not Stuff
R2220
10KR2J-3-GP
FFS_INT2_R
R2202
10KR2J-3-GP
SATA_ODD_PRSNT#
R2206
100KR2J-1-GP
GFX_CRB_DET
RN2201
SRN10KJ-6-GP
EC_SMI#
DGPU_HPD_INTR#
EC_SCI#
RN2202
SRN10KJ-6-GP
MFG_MODE
FP_DET#
S_GPIO
PCH_TEMP_ALERT#
3D3V_S5
RN2204
SRN10KJ-6-GP
USB3_PWR_ON
PCH_GPIO12
PCH_GPIO24
R2201
1KR2J-1-GP
PCH_GPIO15
R2208
10KR2J-3-GP
FDI_OVRVLTG
R2210
10KR2J-3-GP
DMI_OVRVLTG
R2211
1KR2J-1-GP
ICC_EN#
VRAM Frequency
Pull high: 800MHZ
Pull low :900MHZ
R2218
10KR2J-3-GP
UMA_VRAM800MHZ
PCH_GPIO22
R2219
10KR2J-3-GP
VRAM900MHZ
2G
R2214
Do Not Stuff
1G
R2216
Do Not Stuff
VRAM_SIZE1
VRAM_SIZE2
R2215
Do Not Stuff
R2217
Do Not Stuff
1G_512M
512M_2G
INTERNAL GFX
EXTERNAL GFX
R2205 DY 10K
R2206 100K DY
Title
Size
Document Number
Rev
Date:
Sheet

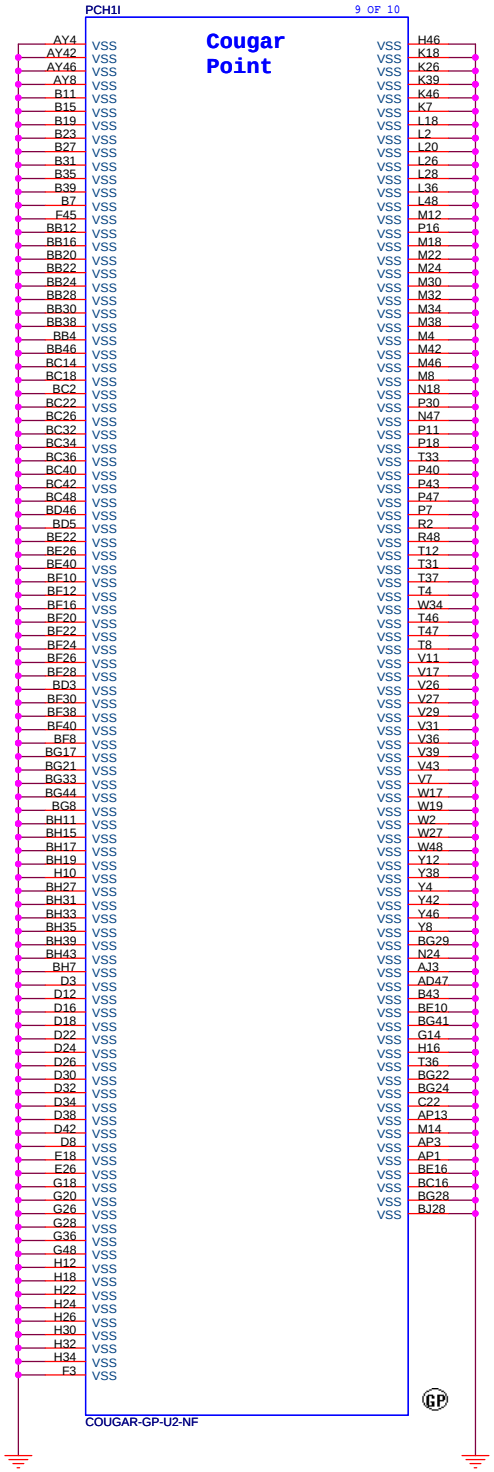
SSID = PCH



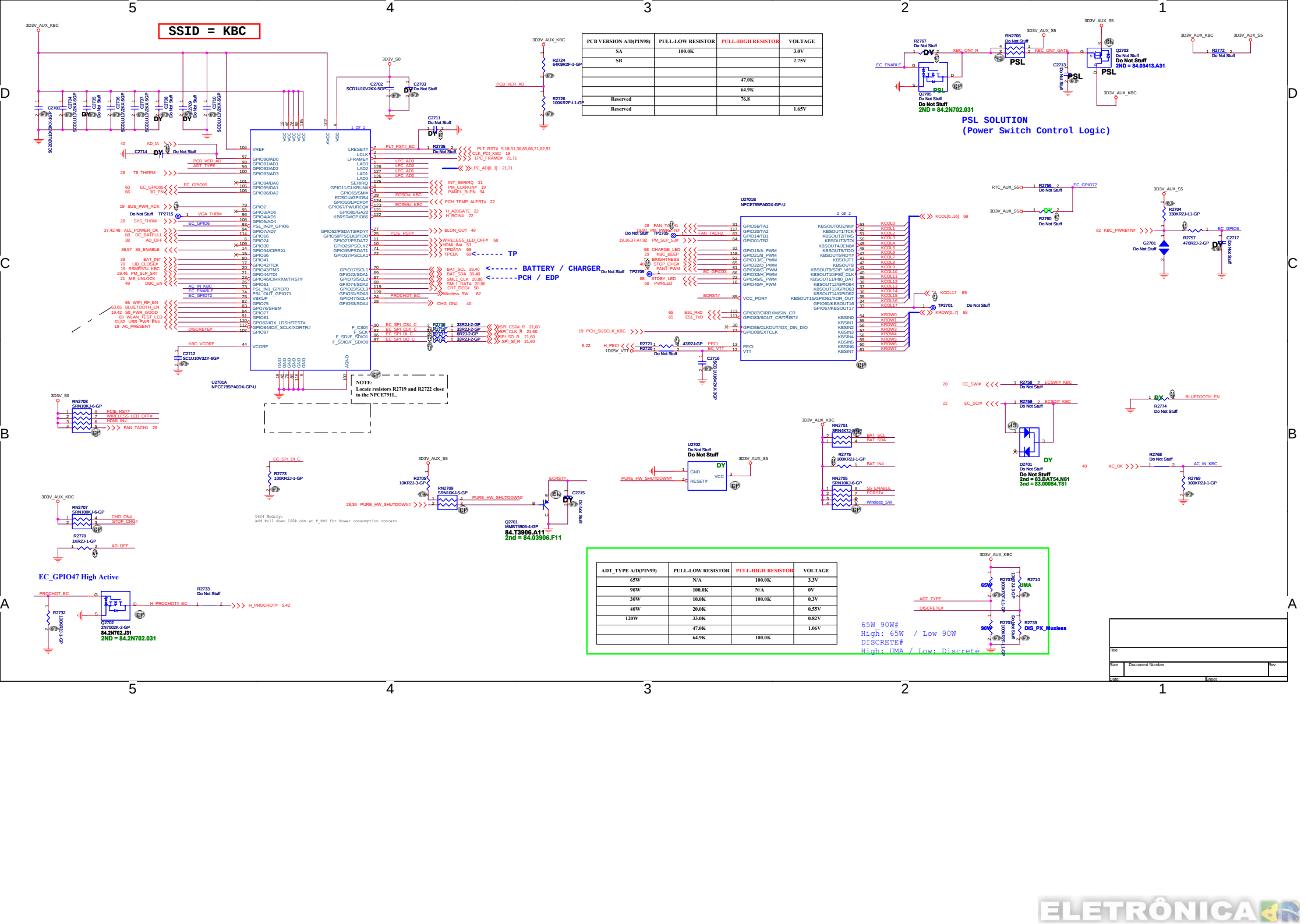
Title		
Size	Document Number	Rev
Date:		Sheet

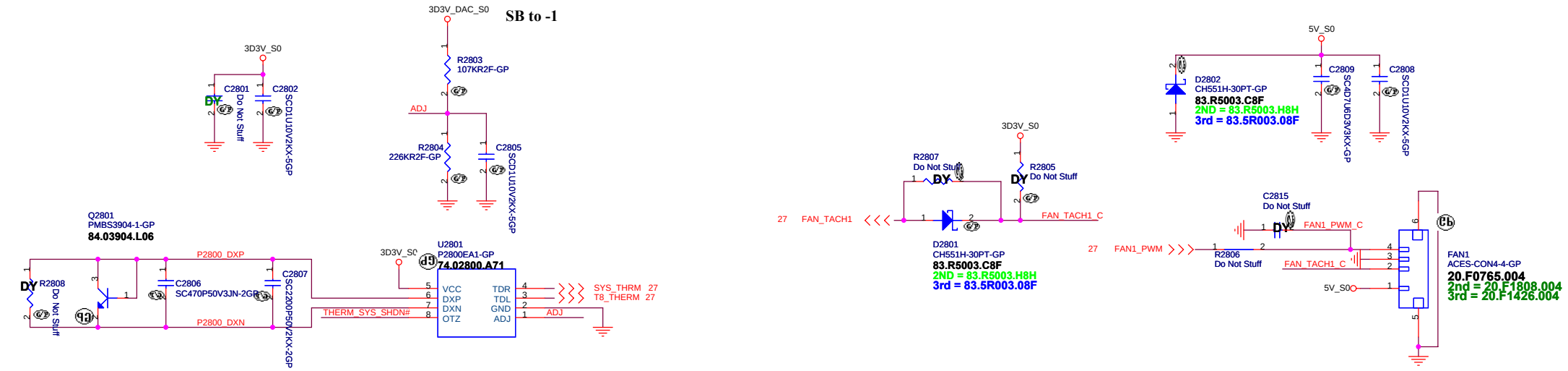

POWER
PCH1J
10 OF 10
Cougar Point
COUGAR-GP-U2-NF
USB
Clock and Miscellaneous
PCI/GPIO/LPC
SATA
MISC
CPU
RTC
HDA
VCCACLK
VCCDSW3_3
DCPSUSBYP
VCC3_3
VCCAPLLDMI2
VCCIO
DCPSUS
VCCASW
DCPRTC
VCCVRM
VCCADPLLA
VCCADPLLB
VCCIO
VCCDIFFCLKN
VCCSSC
DCPSST
V_PROC_IO
VCCRTC
VCCSUS3_3
V5REF_SUS
V5REF
VCCAPLLSATA
VCCSUSHDA
3D3V_S5
3D3V_S0
1D05V_VTT
5V_S5
5V_S0
+5VA_PCH_VCC5REFSUS
+5VS_PCH_VCC5REF
+1.05VS_VCCA_A_DPL
+1.05VS_VCCA_B_DPL
+VCCRTCEXT
+VCCSST
VCCVRM_S0
RTC_AUX_S5
+3VS_+1.5VS_HDA_IO
L2402
IND-10UH-218GP
68.10050.10Y
2nd = 68.10090.10B
L2403
C2402 SC1U10V2KX-1GP
C2403 C2404 C2406 C2407 C2408 SC10U6D3V5KX-1GP SC1U6D3V2KX-GP Do Not Stuff
C2409 C2410 SC1U6D3V2KX-GP
C2411 SCD1U10V2KX-5GP
C2412 C2413 SC1U6D3V2KX-GP
C2414 SC1U6D3V2KX-GP
C2415 SCD1U10V2KX-5GP
C2417 C2418 SCD47U6D3V5KX-GP SCD1U10V2KX-5GP
C2419 Do Not Stuff
C2420 SC1U6D3V2KX-GP
C2423 C2424 C2425 SC1U6D3V2KX-GP SCD1U10V2KX-5GP
C2426 SCD1U10V2KX-5GP
C2427 SC1U10V2KX-1GP
C2428 C2429 C2430 C2431 C2432 SC1U6D3V2KX-GP SCD1U10V2KX-5GP
C2433 C2435 SC1U6D3V2KX-GP SCD1U10V2KX-5GP
D2401 D2402 Do Not Stuff
2nd = 83.R2004.B8F
R2407 R2408 10R2J-2-GP
R2409 R2413 R2414 R2415 Do Not Stuff
R2402 Do Not Stuff
U2401 Do Not Stuff
VIN GND EN VOUT NC#4
C2436 C2405 C2416 Do Not Stuff
DY
GP
Title
Size
Document Number
Rev
Date:
Sheet





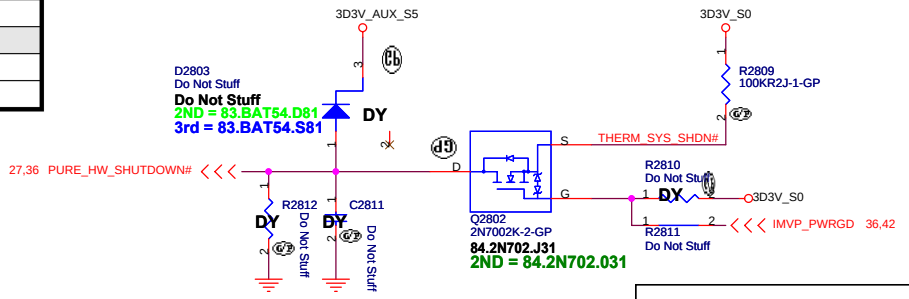
Title		
Size	Document Number	Rev
Date:	Sheet	


SSID = KBC
PCB VERSION A/D(PIN98) | PULL-LOW RESISTOR | PULL-HIGH RESISTOR | VOLTAGE
SA | 100.0K | | 3.0V
SB | | | 2.75V
| | 47.0K |
| | 64.9K |
Reserved | | 76.8 |
Reserved | | | 1.65V
PSL SOLUTION
(Power Switch Control Logic)
2ND = 84.2N702.031
84.T3906.A11
2nd = 84.03906.F11
84.2N702.J31
2ND = 84.2N702.031
EC_GPIO47 High Active
<------ TP
<------ BATTERY / CHARGER
<------PCH / EDP
NOTE:
Locate resistors R2719 and R2722 close to the NPCE791L.
ADT_TYPE A/D(PIN99) | PULL-LOW RESISTOR | PULL-HIGH RESISTOR | VOLTAGE
65W | N/A | 100.0K | 3.3V
90W | 100.0K | N/A | 0V
30W | 10.0K | 100.0K | 0.3V
40W | 20.0K | | 0.55V
120W | 33.0K | | 0.82V
| 47.0K | | 1.06V
| 64.9K | 100.0K |
65W_90W#
High: 65W / Low 90W
DISCRETE#
High: UMA / Low: Discrete
ELETRÔNICA



ADJ Table (Reference to SYNTON-TECH Metal Film Resistor E-96 ±1% Series)

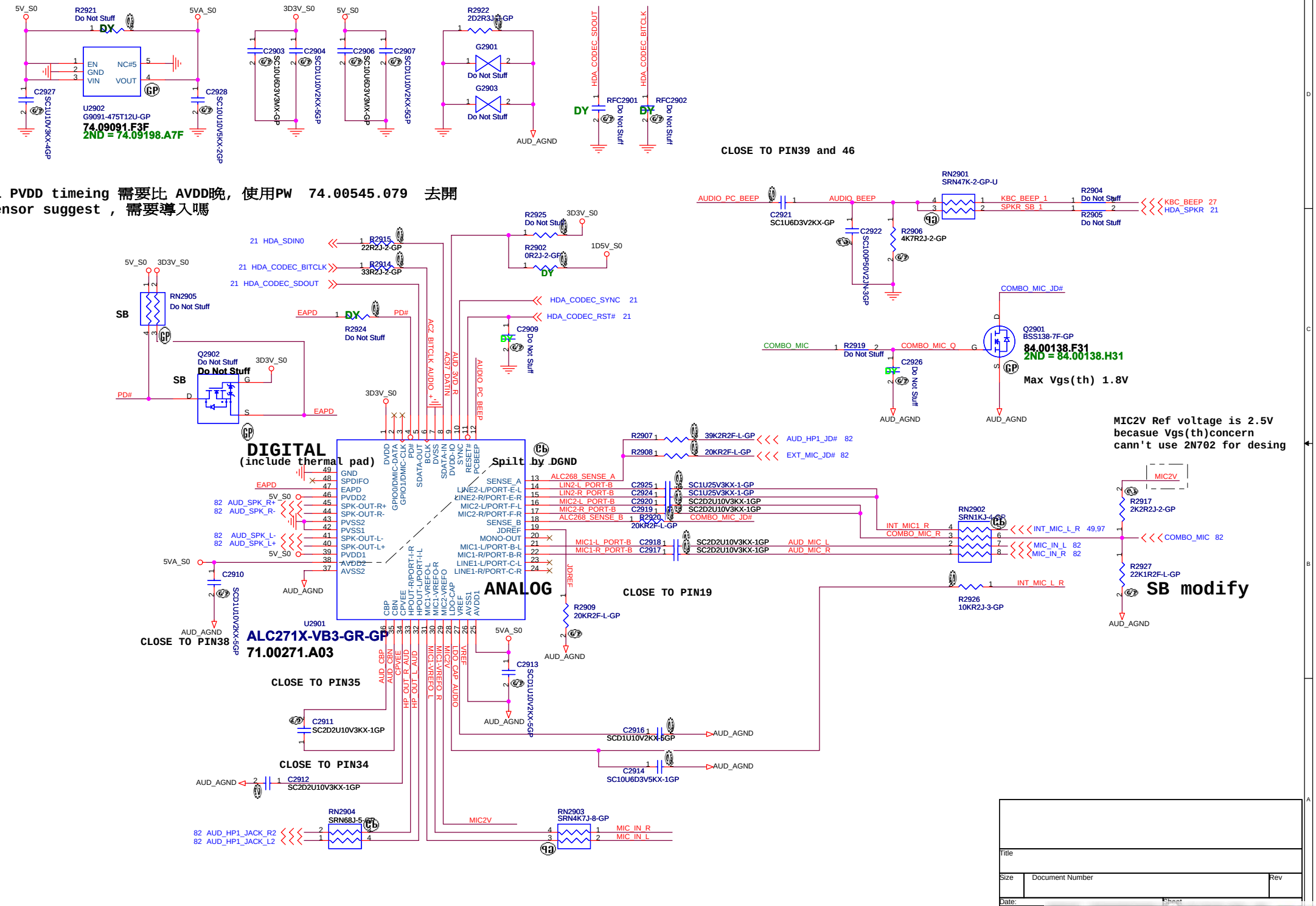
R_{ADJ1} (KΩ)	R_{ADJ2} (KΩ)	V_{ADJ} (v)	OTZ Threshold Temperature (°C)
124	226	2.13	101
118	226	2.17	96.3
113	226	2.20	92.1
110	226	2.22	89.6
107	226	2.24	87
105	226	2.25	85.3
100	226	2.29	80.9

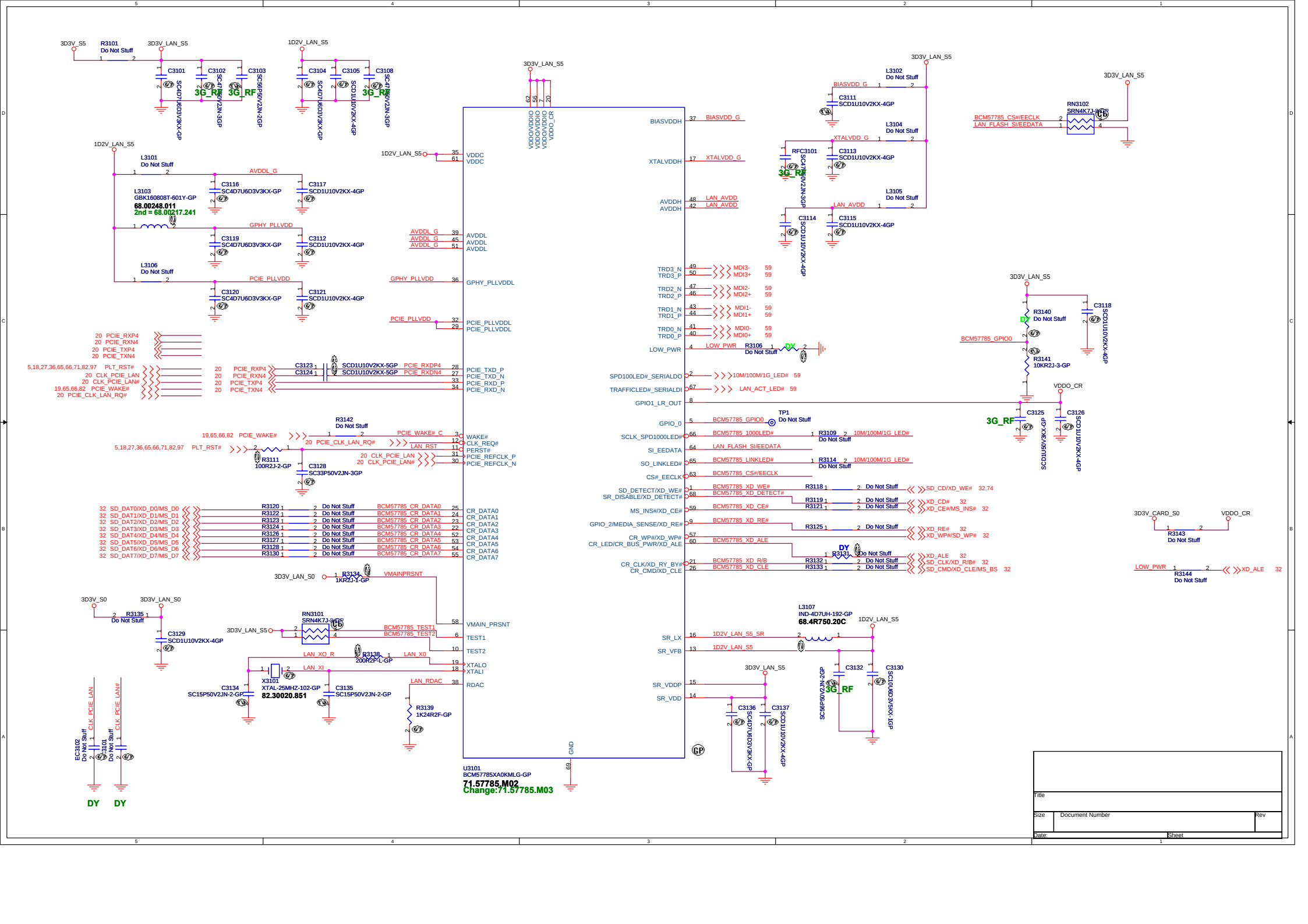


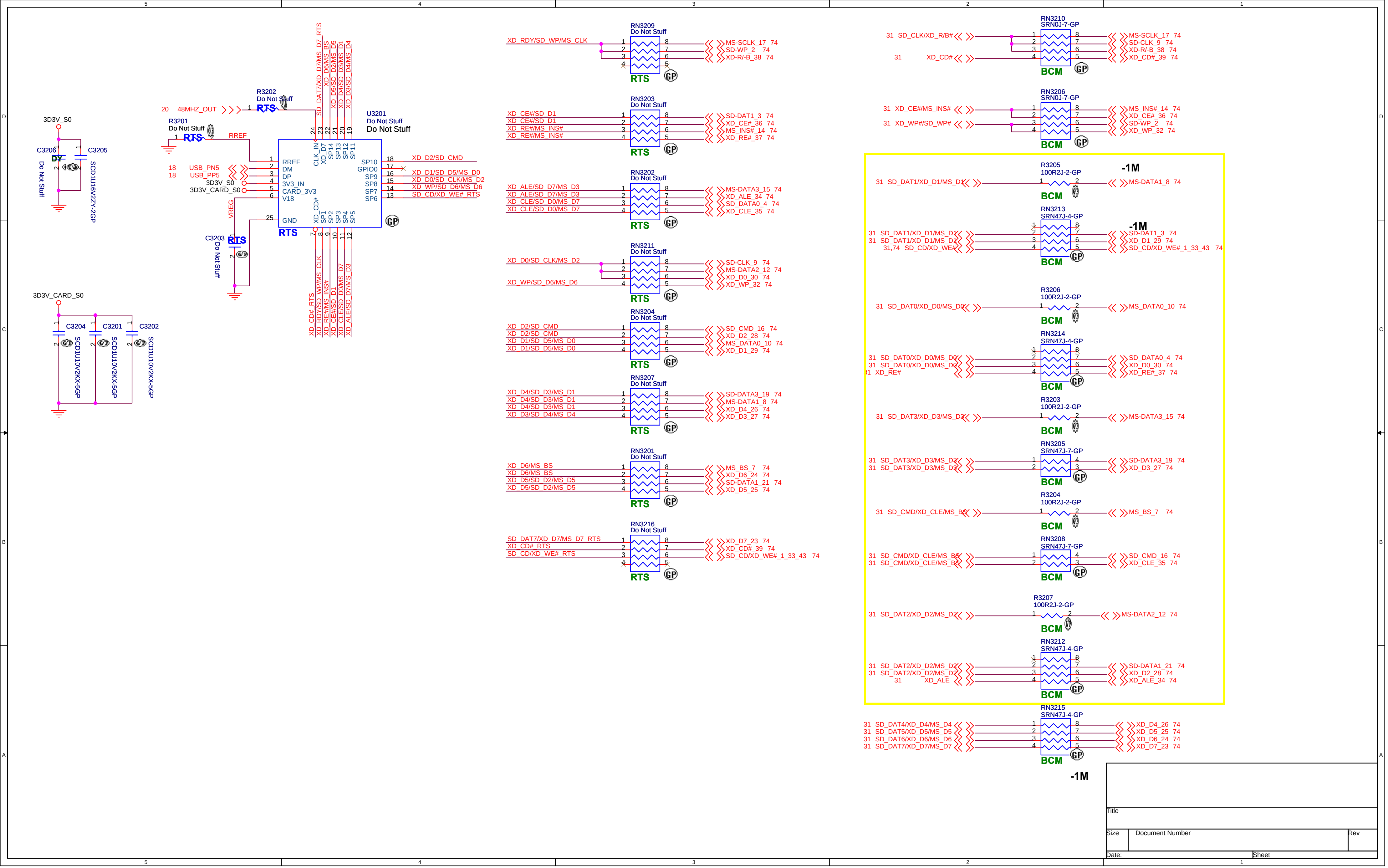
Title

Size | Document Number | Rev

Date: | Sheet

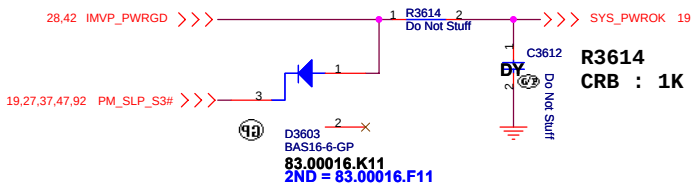

-1 PVDD timeing 需要比 AVDD晚, 使用PW 74.00545.079 去開
vensor suggest , 需要導入嗎
CLOSE TO PIN39 and 46
MIC2V Ref voltage is 2.5V
becasue Vgs(th)concern
cann't use 2N702 for desing
Max Vgs(th) 1.8V
DIGITAL
(include thermal pad)
Spilt by DGND
ANALOG
ALC271X-VB3-GR-GP
71.00271.A03
U2901
CLOSE TO PIN38
CLOSE TO PIN35
CLOSE TO PIN34
CLOSE TO PIN19
SB modify
R2921 Do Not Stuff
U2902 G9091-475T12U-GP
74.09091.F3F
2ND = 74.09198.A7F
R2922 2D2R3J-GP
G2901 Do Not Stuff
G2903 Do Not Stuff
RFC2901 Do Not Stuff
RFC2902 Do Not Stuff
RN2901 SRN47K-2-GP-U
RN2905 Do Not Stuff
Q2902 Do Not Stuff
Q2901 BSS138-7-F-GP
84.00138.F31
2ND = 84.00138.H31
RN2902 SRN1KJ-4-GP
RN2904 SRN68J-5-GP
RN2903 SRN4K7J-8-GP
R2924 Do Not Stuff
R2925 Do Not Stuff
R2902 0R2J-2-GP
R2907 39K2R2F-L-GP
R2908 20KR2F-L-GP
R2909 20KR2F-L-GP
R2926 10KR2J-3-GP
R2927 22K1R2F-L-GP
R2917 2K2R2J-2-GP
C2921 SC1U6D3V2KX-GP
C2922 SC100P50V2JN-3GP
R2906 4K7R2J-2-GP
R2904 Do Not Stuff
R2905 Do Not Stuff
C2926 Do Not Stuff
C2909 Do Not Stuff
R2919 Do Not Stuff
C2910 SCD1U10V2KX-5GP
C2911 SC2D2U10V3KX-1GP
C2912 SC2D2U10V3KX-1GP
C2913 SCD1U10V2KX-5GP
C2914 SC10U6D3V5KX-1GP
C2916 SCD1U10V2KX-5GP
C2925 SC1U25V3KX-1GP
C2924 SC1U25V3KX-1GP
C2920 SC2D2U10V3KX-1GP
C2919 SC2D2U10V3KX-1GP
R2920 20KR2F-L-GP
C2918 SC2D2U10V3KX-1GP
C2917 SC2D2U10V3KX-1GP
C2927 SC1U10V3KX-4GP
C2928 SC10U10V5KX-2GP
C2903 SC10U6D3V3MX-GP
C2904 SCD1U10V2KX-5GP
C2906 SC10U6D3V3MX-GP
C2907 SCD1U10V2KX-5GP
Title
Size
Document Number
Rev
Date:
Sheet
ELETRONICA


3D3V_S5
R3101
Do Not Stuff
3D3V_LAN_S5
C3101
C3102
C3103
1D2V_LAN_S5
C3104
C3105
C3108
3G_RF
3D3V_LAN_S5
VDDO_CR
VDDO_DDIO
VDDO_DDIO
VDDO_DDIO
VDDO_CR
1D2V_LAN_S5
L3101
Do Not Stuff
AVDDL_G
C3116
C3117
L3103
GBK160808T-601Y-GP
68.00248.011
2nd = 68.00217.241
GPHY_PLLVDD
C3119
C3112
L3106
Do Not Stuff
PCIE_PLLVDD
C3120
C3121
VDDC
VDDC
AVDDL_G
AVDDL_G
AVDDL_G
AVDDL
AVDDL
AVDDL
GPHY_PLLVDD
GPHY_PLLVDDL
PCIE_PLLVDD
PCIE_PLLVDDL
PCIE_PLLVDDL
20 PCIE_RXP4
20 PCIE_RXN4
20 PCIE_TXP4
20 PCIE_TXN4
5,18,27,36,65,66,71,82,97 PLT_RST#
20 CLK_PCIE_LAN
20 CLK_PCIE_LAN#
19,65,66,82 PCIE_WAKE#
20 PCIE_CLK_LAN_RQ#
C3123
C3124
SCD1U10V2KX-5GP
PCIE_RXDP4
PCIE_RXDN4
PCIE_TXD_P
PCIE_TXD_N
PCIE_RXD_P
PCIE_RXD_N
R3142
Do Not Stuff
PCIE_WAKE# C
WAKE#
CLK_REQ#
PERST#
LAN_RST
R3111
100R2J-2-GP
C3128
SC33P50V2JN-3GP
PCIE_REFCLK_P
PCIE_REFCLK_N
32 SD_DAT0/XD_D0/MS_D0
32 SD_DAT1/XD_D1/MS_D1
32 SD_DAT2/XD_D2/MS_D2
32 SD_DAT3/XD_D3/MS_D3
32 SD_DAT4/XD_D4/MS_D4
32 SD_DAT5/XD_D5/MS_D5
32 SD_DAT6/XD_D6/MS_D6
32 SD_DAT7/XD_D7/MS_D7
R3120
R3122
R3123
R3124
R3126
R3127
R3128
R3130
Do Not Stuff
BCM57785_CR_DATA0
BCM57785_CR_DATA1
BCM57785_CR_DATA2
BCM57785_CR_DATA3
BCM57785_CR_DATA4
BCM57785_CR_DATA5
BCM57785_CR_DATA6
BCM57785_CR_DATA7
CR_DATA0
CR_DATA1
CR_DATA2
CR_DATA3
CR_DATA4
CR_DATA5
CR_DATA6
CR_DATA7
3D3V_LAN_S0
R3134
1KR2J-1-GP
VMAINPRSNT
3D3V_S0
3D3V_LAN_S0
R3135
Do Not Stuff
C3129
SCD1U10V2KX-4GP
3D3V_LAN_S5
RN3101
SRN4K7J-8GP
BCM57785_TEST1
BCM57785_TEST2
LAN_XO_R
R3138
200R2F-L-GP
LAN_X0
LAN_XI
X3101
XTAL-25MHZ-102-GP
82.30020.851
C3134
SC15P50V2JN-2-GP
C3135
SC15P50V2JN-2-GP
LAN_RDAC
R3139
1K24R2F-GP
VMAIN_PRSNT
TEST1
TEST2
XTALO
XTALI
RDAC
EC3102
Do Not Stuff
CLK_PCIE_LAN
3101
Do Not Stuff
CLK_PCIE_LAN#
DY
DY
U3101
BCM57785XA0KMLG-GP
71.57785.M02
Change:71.57785.M03
GND
BIASVDDH
XTALVDDH
AVDDH
AVDDH
BIASVDD_G
XTALVDD_G
LAN_AVDD
LAN_AVDD
TRD3_N
TRD3_P
TRD2_N
TRD2_P
TRD1_N
TRD1_P
TRD0_N
TRD0_P
MDI3-
MDI3+
MDI2-
MDI2+
MDI1-
MDI1+
MDI0-
MDI0+
LOW_PWR
R3106
Do Not Stuff
SPD100LED#_SERIALDO
TRAFFICLED#_SERIALDI
GPIO1_LR_OUT
GPIO_0
SCLK_SPD1000LED#
SI_EEDATA
SO_LINKLED#
CS#_EECLK
SD_DETECT/XD_WE#
SR_DISABLE/XD_DETECT#
MS_INS#/XD_CE#
GPIO_2/MEDIA_SENSE/XD_RE#
CR_WP#/XD_WP#
CR_LED/CR_BUS_PWR/XD_ALE
CR_CLK/XD_RY_BY#
CR_CMD/XD_CLE
10M/100M/1G_LED#
LAN_ACT_LED#
BCM57785_GPIO0
BCM57785_1000LED#
LAN_FLASH_SI/EEDATA
BCM57785_LINKLED#
BCM57785_CS#/EECLK
BCM57785_XD_WE#
BCM57785_XD_DETECT#
BCM57785_XD_CE#
BCM57785_XD_RE#
BCM57785_XD_ALE
BCM57785_XD_R/B
BCM57785_XD_CLE
SD_CD/XD_WE#
XD_CD#
XD_CE#/MS_INS#
XD_RE#
XD_WP#/SD_WP#
XD_ALE
SD_CLK/XD_R/B#
SD_CMD/XD_CLE/MS_BS
L3102
Do Not Stuff
BIASVDD_G
C3111
L3104
Do Not Stuff
XTALVDD_G
C3113
RFC3101
L3105
Do Not Stuff
LAN_AVDD
C3114
C3115
L3107
IND-4D7UH-192-GP
68.4R750.20C
1D2V_LAN_S5_SR
1D2V_LAN_S5
SR_LX
SR_VFB
SR_VDDP
SR_VDD
C3136
C3137
C3132
C3130
RN3102
SRN4K7J-8GP
BCM57785_CS#/EECLK
LAN_FLASH_SI/EEDATA
R3140
DY
Do Not Stuff
R3141
10KR2J-3-GP
C3118
C3125
C3126
3D3V_CARD_S0
R3143
Do Not Stuff
LOW_PWR
R3144
Do Not Stuff
Title
Size
Document Number
Rev
Date:
Sheet

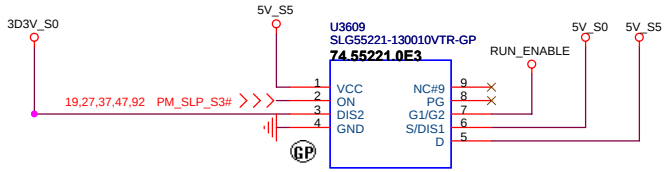


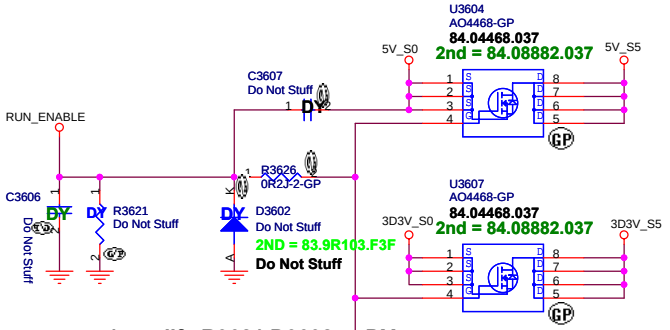
U3201
Do Not Stuff
RTS
RN3209
RN3203
RN3202
RN3211
RN3204
RN3207
RN3201
RN3216
RN3210
RN3206
BCM
-1M
RN3215
Title
Size
Document Number
Rev
Date:
Sheet

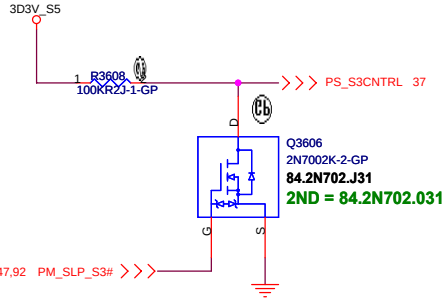
Power Sequence



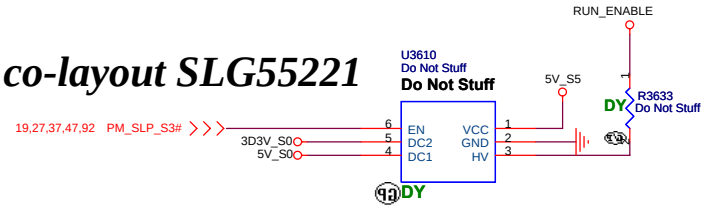
ANNIE Run Power

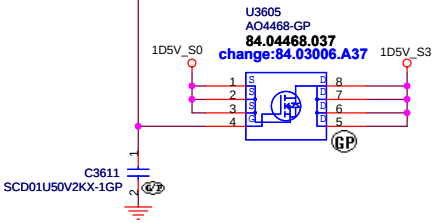






-1 co-layout SLG55221

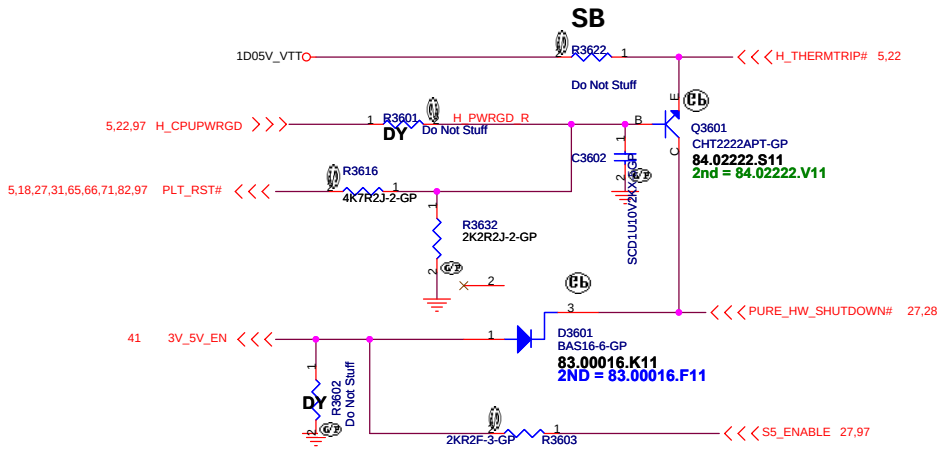




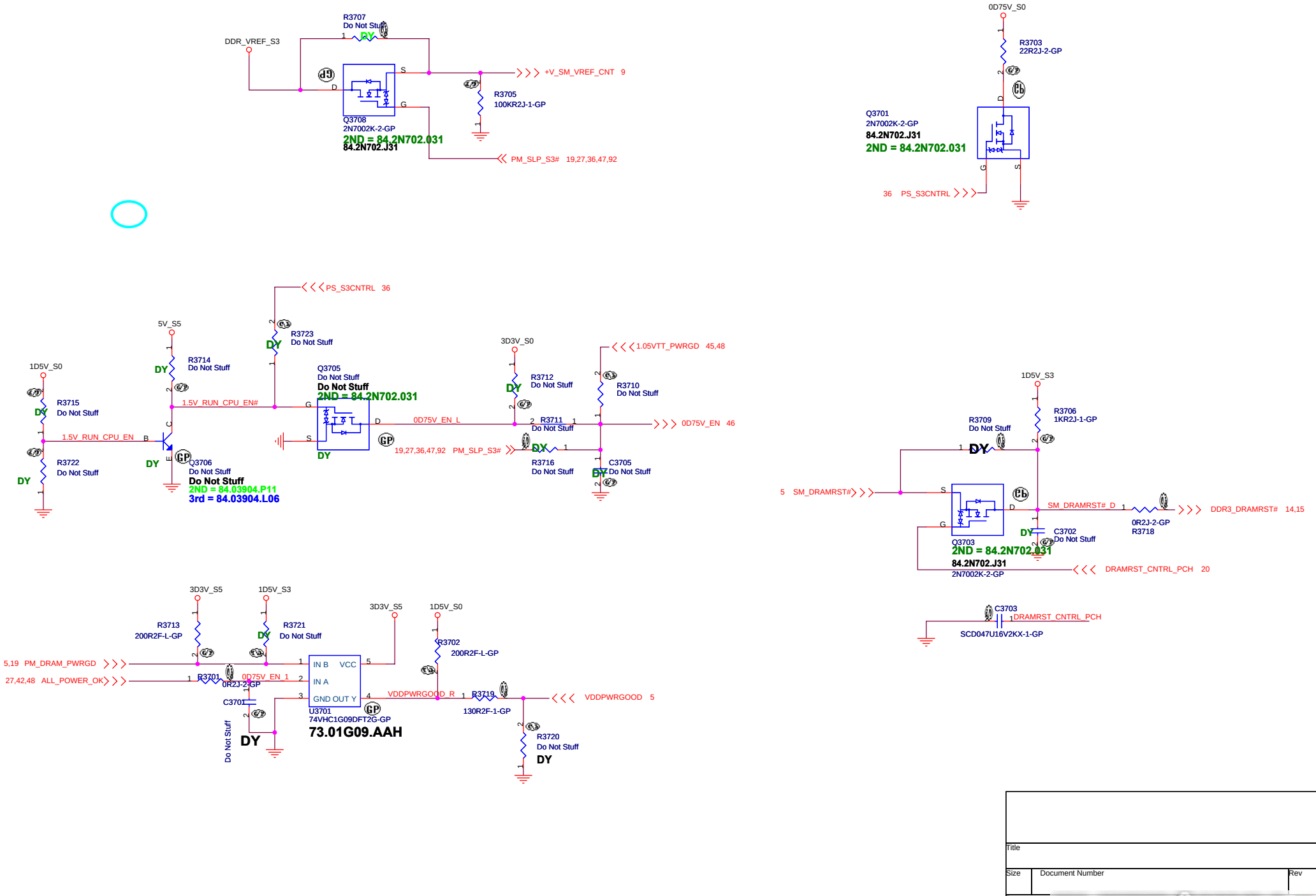
1D5V_S0

MAX Current 3000 mA
Design Current 2100 mA
Total= 11.39A

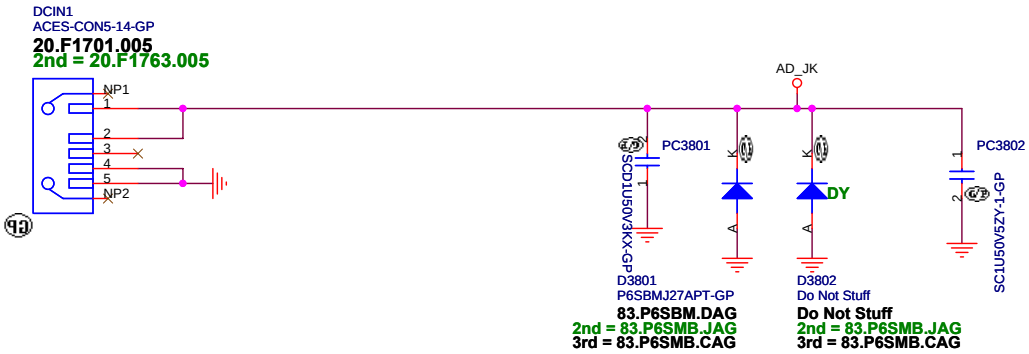
SB

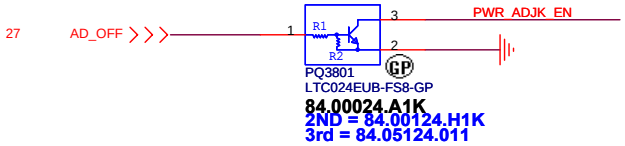


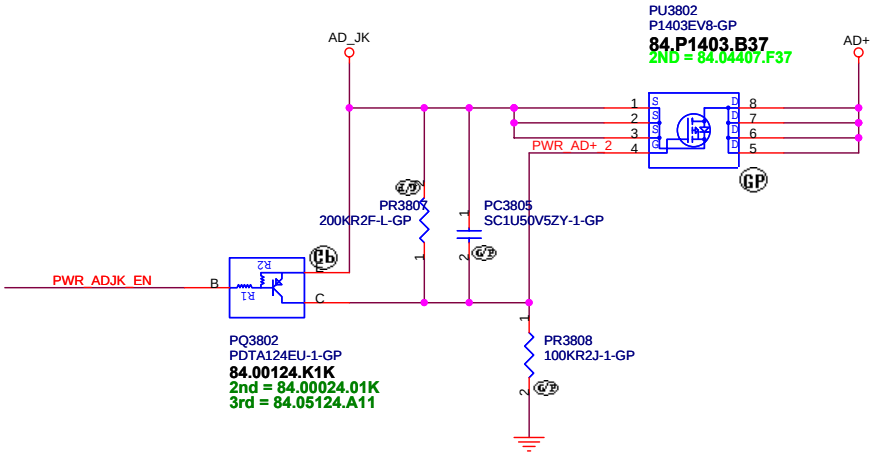
Title		
Size	Document Number	Rev
Date:	Sheet	



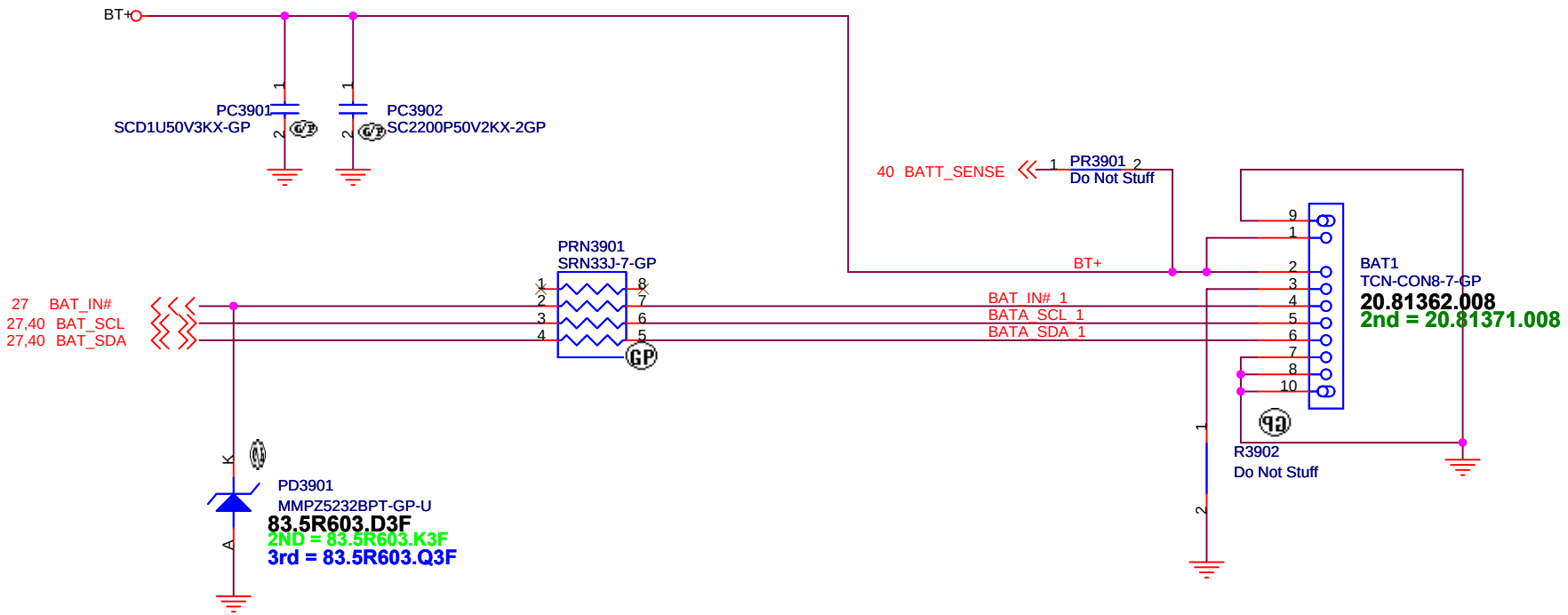
Title		
Size	Document Number	Rev
Date:		Sheet







Title		
Size	Document Number	Rev
Date:		Sheet



Title		
Size	Document Number	Rev
Date:	Sheet	

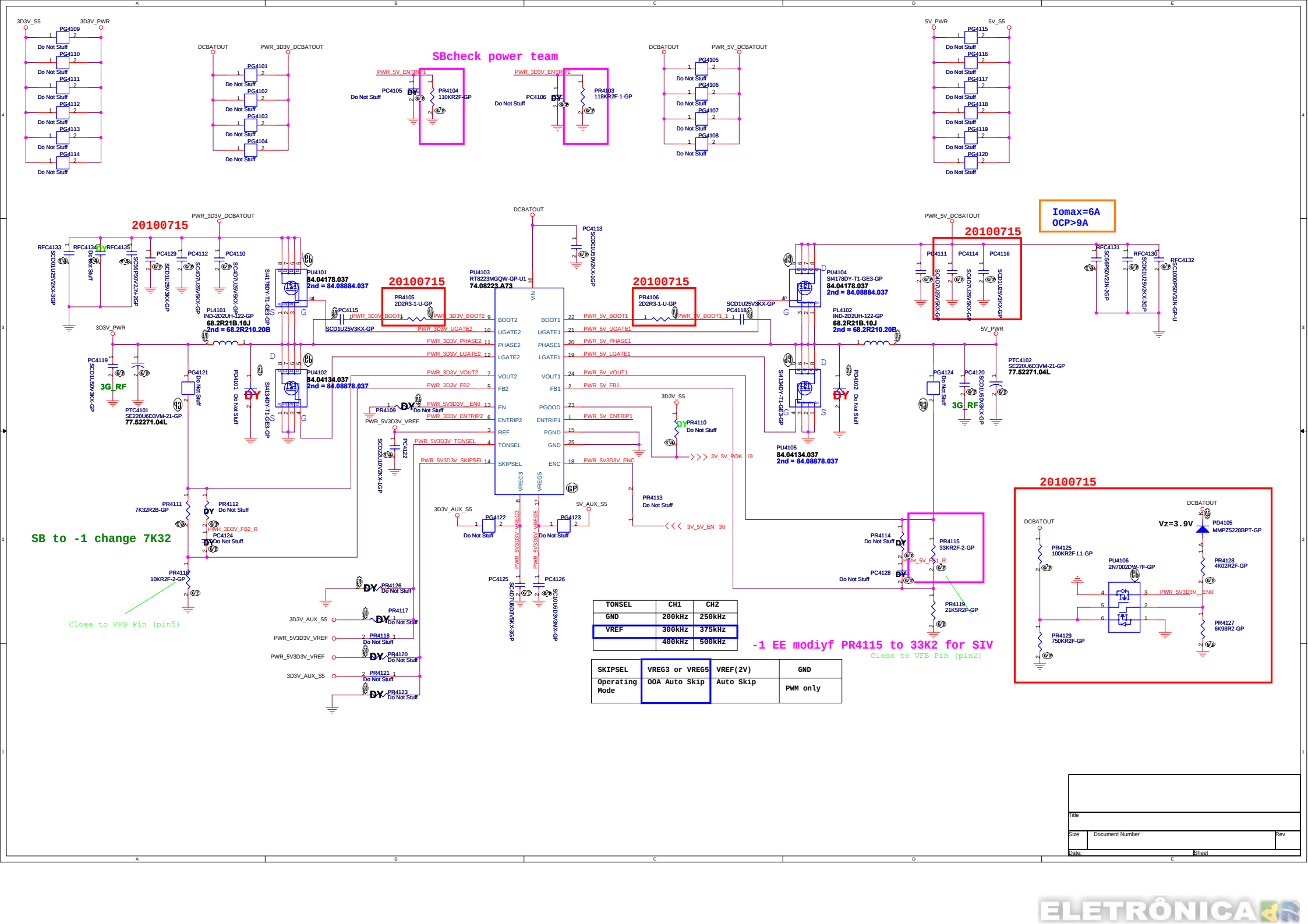
AD+ total power	R1	R2	AD+ total power		
65w	187k	49.9k	80w	137k	49.9k
90w	121k	49.9k			

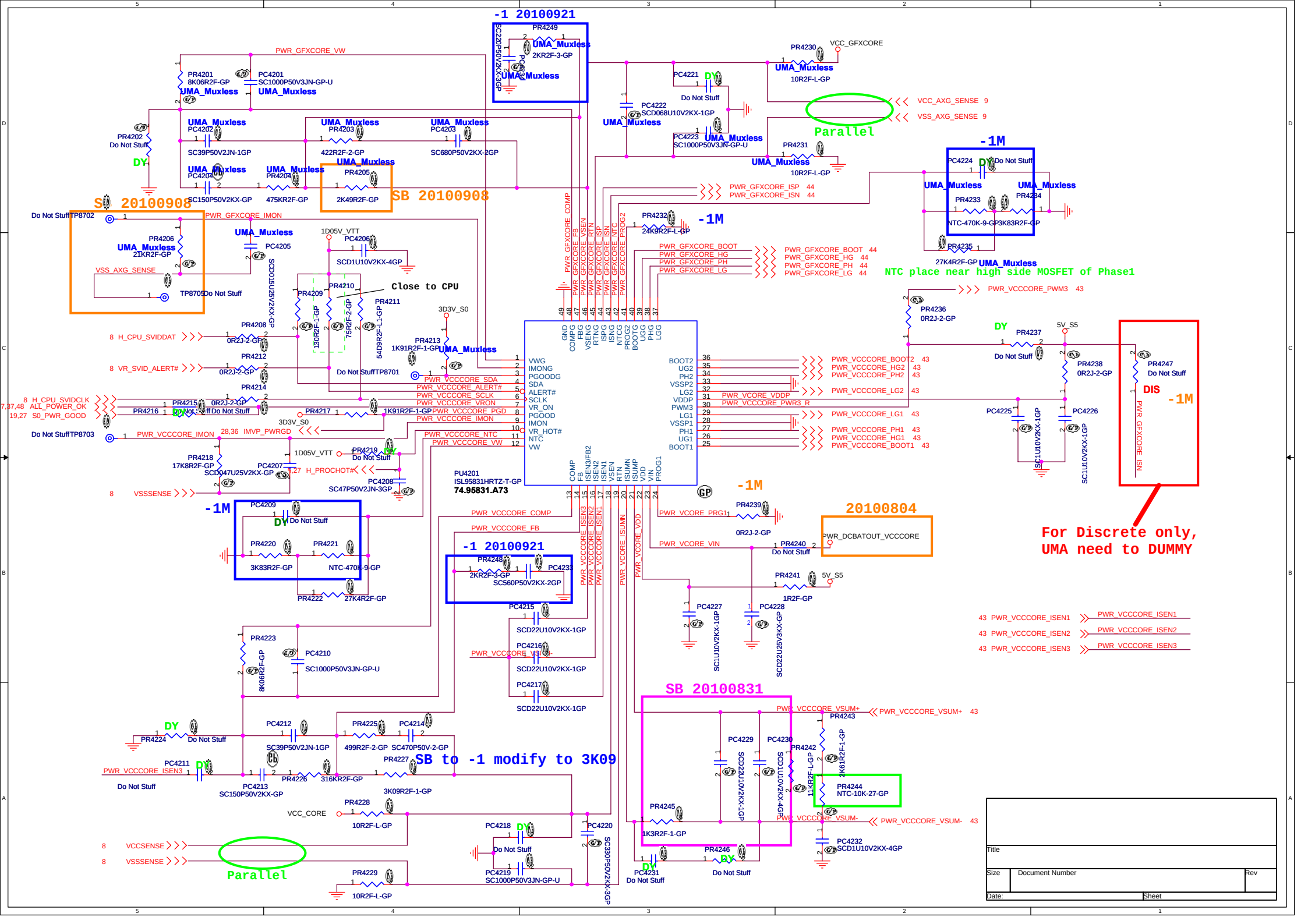
20100706 Wayne

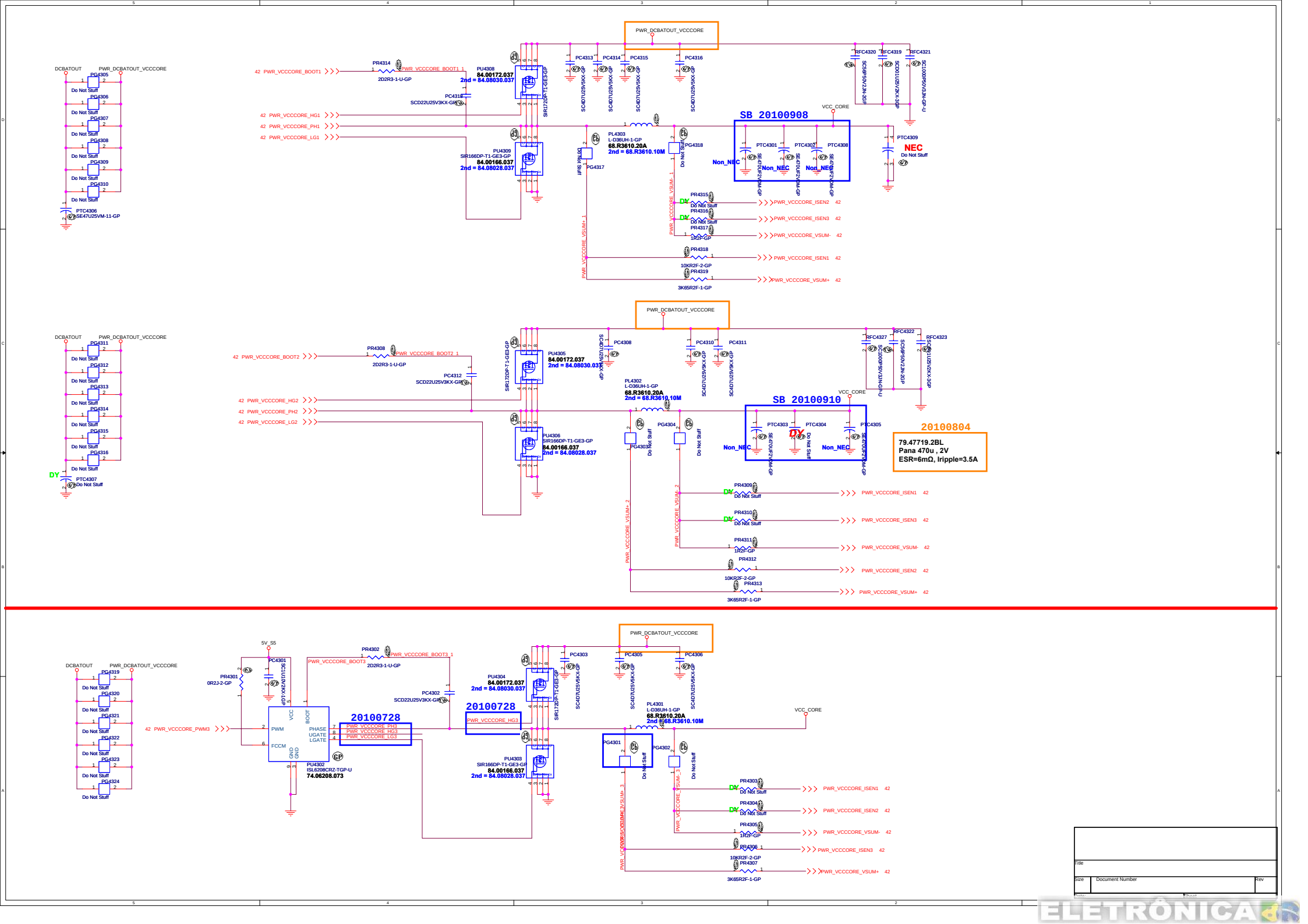
20101018

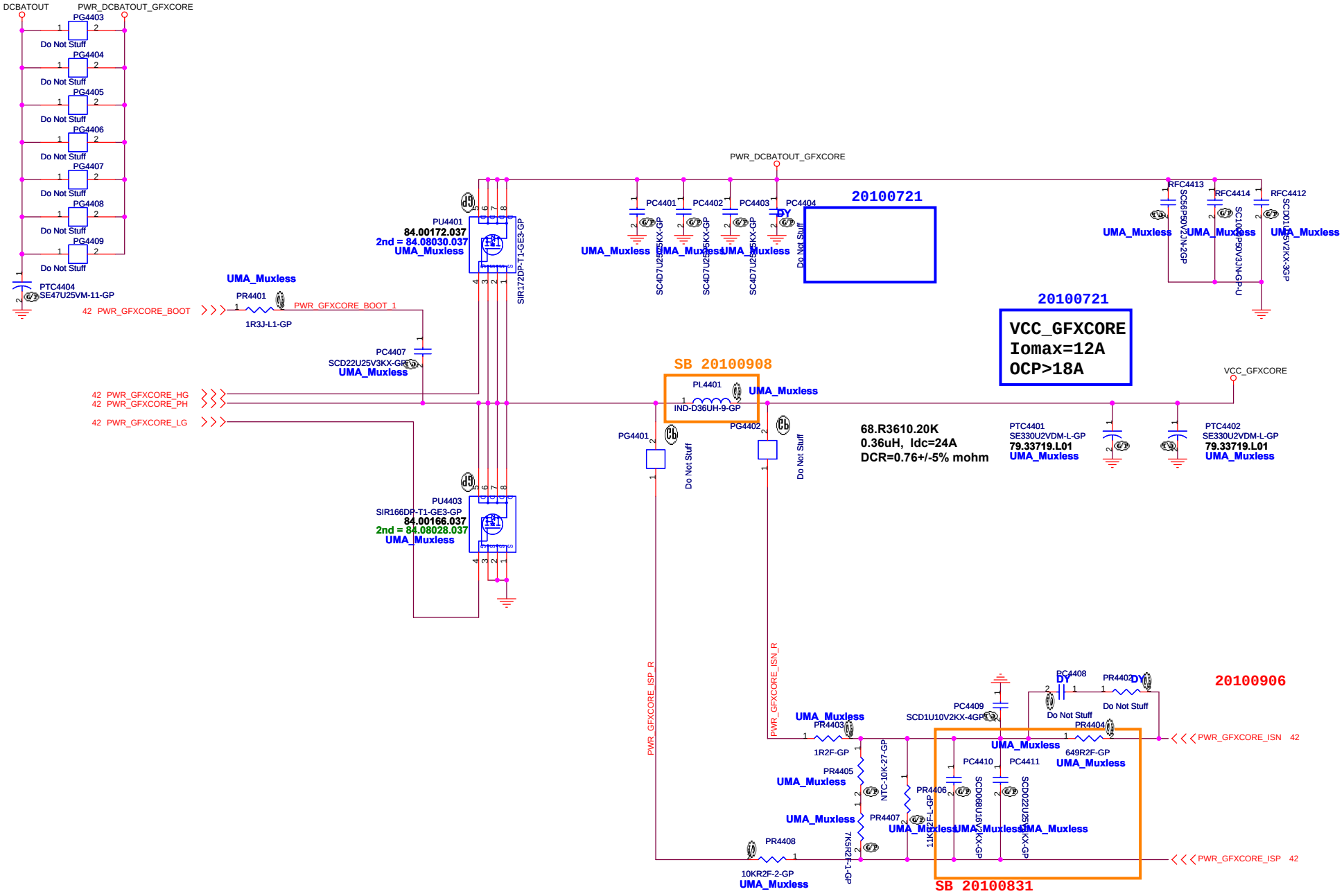
-1M

-1M

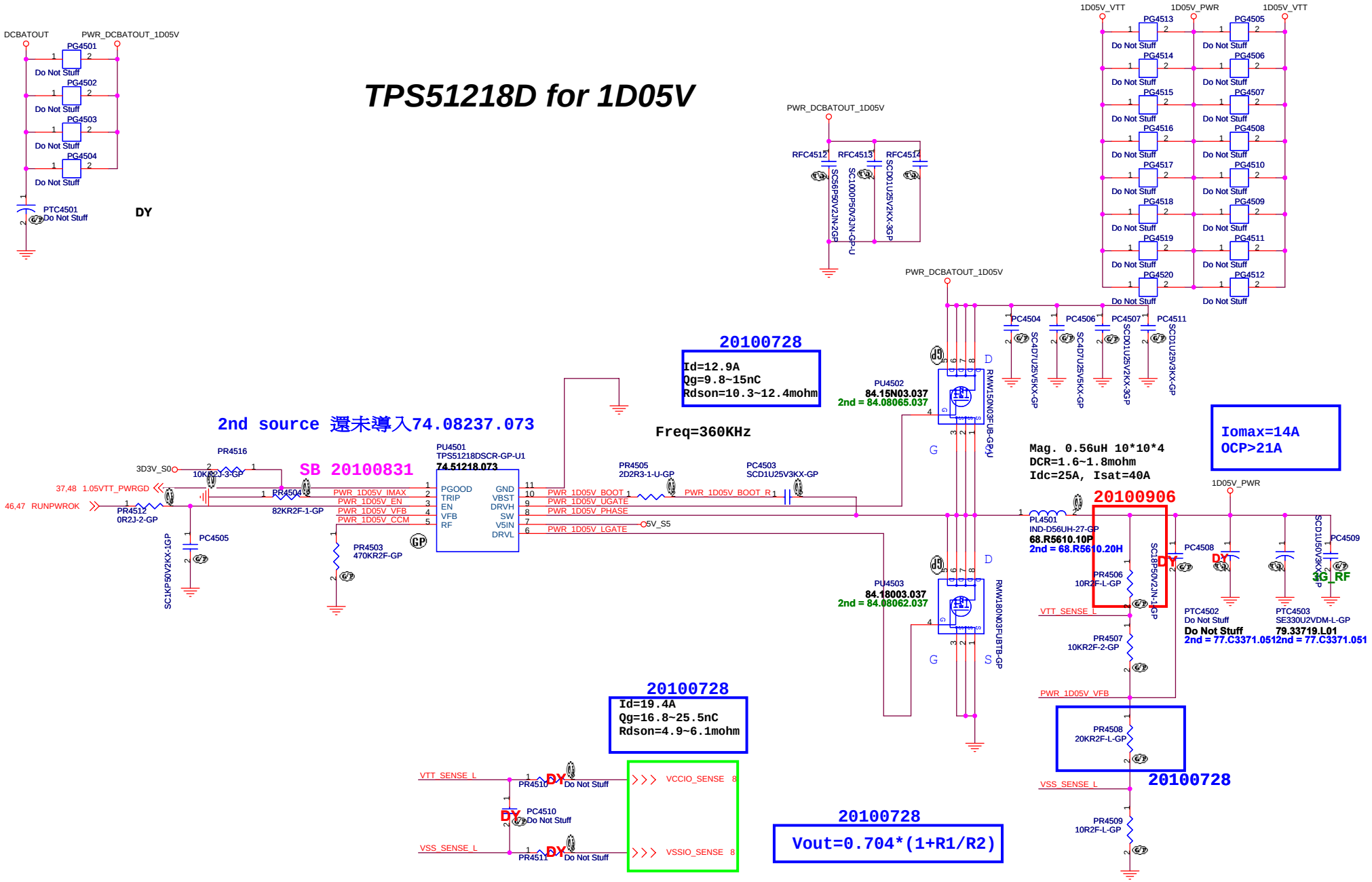

SBcheck power team
20100715
20100715
20100715
20100715
Iomax=6A
OCP>9A
SB to -1 change 7K32
Close to VFB Pin (pin5)
-1 EE modiyf PR4115 to 33K2 for SIV
Close to VFB Pin (pin2)
Vz=3.9V
PU4101 84.04178.037 2nd = 84.08884.037
PU4102 84.04134.037 2nd = 84.08878.037
PU4103 RT8223MGQW-GP-U1 74.08223.A73
PU4104 SI4178DY-T1-GE3-GP 84.04178.037 2nd = 84.08884.037
PU4105 84.04134.037 2nd = 84.08878.037
PU4106 2N7002DW-7F-GP
PL4101 IND-2D2UH-122-GP 68.2R21B.10J 2nd = 68.2R210.20B
PL4102 IND-2D2UH-122-GP 68.2R21B.10J 2nd = 68.2R210.20B
PTC4101 SE220U6D3VM-21-GP 77.52271.04L
PTC4102 SE220U6D3VM-21-GP 77.52271.04L
PR4105 2D2R3-1-U-GP
PR4106 2D2R3-1-U-GP
PR4111 7K32R2B-GP
PR4112 Do Not Stuff
PR4113 Do Not Stuff
PR4114 10KR2F-2-GP
PR4115 33KR2F-2-GP
PR4119 21K5R2F-GP
PR4125 100KR2F-L1-GP
PR4127 6K98R2-GP
PR4128 4K02R2F-GP
PR4129 750KR2F-GP
PC4125 SC4D7U6D3V6KX-3GP
PC4126 SCD1U6D3V6KX-GP
PC4128 Do Not Stuff
PWR_5V_ENTRIP1
PWR_3D3V_ENTRIP2
PWR_3D3V_DCBATOUT
PWR_5V_DCBATOUT
DCBATOUT
3D3V_S5
3D3V_PWR
5V_PWR
5V_S5
3D3V_AUX_S5
5V_AUX_S5
PWR_5V3D3V_VREF
PWR_5V3D3V_TONSEL
PWR_5V3D3V_SKIPSEL
PWR_5V3D3V_EN0
PWR_5V3D3V_ENTRIP2
PWR_3D3V_BOOT2
PWR_3D3V_UGATE2
PWR_3D3V_PHASE2
PWR_3D3V_LGATE2
PWR_3D3V_VOUT2
PWR_3D3V_FB2
PWR_5V_BOOT1
PWR_5V_UGATE1
PWR_5V_PHASE1
PWR_5V_LGATE1
PWR_5V_VOUT1
PWR_5V_FB1
PWR_5V_ENTRIP1
PWR_5V3D3V_ENC
3V_5V_POK 19
3V_5V_EN 36
BOOT2
UGATE2
PHASE2
LGATE2
VOUT2
FB2
EN
ENTRIP2
REF
TONSEL
SKIPSEL
VREG3
VREG5
BOOT1
UGATE1
PHASE1
LGATE1
VOUT1
FB1
PGOOD
ENTRIP1
PGND
GND
ENC
VIN
3G_RF
TONSEL | CH1 | CH2
GND | 200kHz | 250kHz
VREF | 300kHz | 375kHz
 | 400kHz | 500kHz
SKIPSEL | VREG3 or VREG5 | VREF(2V) | GND
Operating Mode | OOA Auto Skip | Auto Skip | PWM only


-1 20100921
SB 20100908
-1M
20100804
SB 20100831
SB to -1 modify to 3K09
Close to CPU
NTC place near high side MOSFET of Phase1
Parallel
For Discrete only,
UMA need to DUMMY
PU4201
ISL95831HRTZ-T-GP
74.95831.A73
PWR_GFXCORE_VW
VCC_GFXCORE
VCC_AXG_SENSE 9
VSS_AXG_SENSE 9
PWR_GFXCORE_IMON
PWR_GFXCORE_ISP 44
PWR_GFXCORE_ISN 44
PWR_GFXCORE_BOOT 44
PWR_GFXCORE_HG 44
PWR_GFXCORE_PH 44
PWR_GFXCORE_LG 44
PWR_VCCCORE_PWM3 43
PWR_VCCCORE_BOOT2 43
PWR_VCCCORE_HG2 43
PWR_VCCCORE_PH2 43
PWR_VCCCORE_LG2 43
PWR_VCCCORE_LG1 43
PWR_VCCCORE_PH1 43
PWR_VCCCORE_HG1 43
PWR_VCCCORE_BOOT1 43
PWR_VCCCORE_ISEN1 43
PWR_VCCCORE_ISEN2 43
PWR_VCCCORE_ISEN3 43
PWR_VCCCORE_VSUM+ 43
PWR_VCCCORE_VSUM- 43
PWR_DCBATOUT_VCCCORE
VCC_CORE
1D05V_VTT
3D3V_S0
5V_S5
VSSSENSE
VCCSENSE
H_CPU_SVIDDAT
VR_SVID_ALERT#
H_CPU_SVIDCLK
ALL_POWER_OK
S0_PWR_GOOD
IMVP_PWRGD
H_PROCHOT#
PWR_VCCCORE_SDA
PWR_VCCCORE_ALERT#
PWR_VCCCORE_SCLK
PWR_VCCCORE_VRON
PWR_VCCCORE_PGD
PWR_VCCCORE_IMON
PWR_VCCCORE_NTC
PWR_VCCCORE_VW
PWR_VCCCORE_COMP
PWR_VCCCORE_FB
PWR_VCORE_PRG1
PWR_VCORE_VIN
PWR_VCORE_VDDP
PWR_VCCCORE_PWR3_R
PWR_VCORE_ISUMN
PWR_VCORE_VDD
PR4201 8K06R2F-GP UMA_Muxless
PC4201 SC1000P50V3JN-GP-U UMA_Muxless
PR4202 Do Not Stuff DY
PC4202 SC39P50V2JN-1GP UMA_Muxless
PR4203 422R2F-2-GP UMA_Muxless
PC4203 SC680P50V2KX-2GP UMA_Muxless
PC4204 SC150P50V2KX-GP UMA_Muxless
PR4204 475KR2F-GP UMA_Muxless
PR4205 2K49R2F-GP UMA_Muxless
PR4249 2KR2F-3-GP UMA_Muxless
PC4249 SC220P50V2KX-3GP UMA_Muxless
PR4230 10R2F-L-GP UMA_Muxless
PC4221 Do Not Stuff DY
PC4222 SCD068U10V2KX-1GP UMA_Muxless
PC4223 SC1000P50V3JN-GP-U UMA_Muxless
PR4231 10R2F-L-GP UMA_Muxless
PC4224 Do Not Stuff DY
PR4233 NTC-470K-9-GP UMA_Muxless
PR4234 3K83R2F-GP UMA_Muxless
PR4235 27K4R2F-GP UMA_Muxless
PR4232 24K9R2F-L-GP
PR4206 21KR2F-GP UMA_Muxless
PC4205 SCD015U25V2KX-5GP UMA_Muxless
PC4206 SCD1U10V2KX-4GP 1D05V_VTT
PR4209 130R2F-1-GP
PR4210 75R2F-2-GP
PR4211 54D9R2F-L1-GP
PR4208 0R2J-2-GP
PR4212 0R2J-2-GP
PR4213 1K91R2F-1-GP UMA_Muxless
PR4214 0R2J-2-GP
PR4215 0R2J-2-GP
PR4216 Do Not Stuff DY
PR4217 1K91R2F-1-GP
PR4218 17K8R2F-GP
PC4207 SCD047U25V2KX-GP
PC4208 SC47P50V2JN-3GP
PR4219 Do Not Stuff DY
PC4209 Do Not Stuff DY
PR4220 3K83R2F-GP
PR4221 NTC-470K-9-GP
PR4222 27K4R2F-GP
PR4223 8K06R2F-GP
PC4210 SC1000P50V3JN-GP-U
PR4248 2KR2F-3-GP
PC4233 SC560P50V2KX-2GP
PC4215 SCD22U10V2KX-1GP
PC4216 SCD22U10V2KX-1GP
PC4217 SCD22U10V2KX-1GP
PR4239 0R2J-2-GP
PR4240 Do Not Stuff
PR4241 1R2F-GP 5V_S5
PC4227 SC1U10V2KX-1GP
PC4228 SCD22U25V3KX-GP
PR4236 0R2J-2-GP
PR4237 Do Not Stuff DY 5V_S5
PR4238 0R2J-2-GP
PR4247 Do Not Stuff DIS -1M
PC4225 SC1U10V2KX-1GP
PC4226 SC1U10V2KX-1GP
PR4243 2K61R2F-1-GP
PR4244 NTC-10K-27-GP
PC4229 SCD22U10V2KX-1GP
PC4230 SC1U10V2KX-4GP
PR4242 11KR2F-L-GP
PR4245 1K3R2F-1-GP
PR4246 Do Not Stuff DY
PC4231 Do Not Stuff DY
PC4232 SCD1U10V2KX-4GP
PR4224 Do Not Stuff DY
PC4212 SC39P50V2JN-1GP
PR4225 499R2F-2-GP
PC4214 SC470P50V-2-GP
PC4211 Do Not Stuff DY
PC4213 SC150P50V2KX-GP
PR4226 316KR2F-GP
PR4227 3K09R2F-1-GP
PR4228 10R2F-L-GP
PC4218 Do Not Stuff DY
PC4219 SC1000P50V3JN-GP-U
PC4220 SC330P50V2KX-3GP
PR4229 10R2F-L-GP
TP8702 Do Not Stuff
TP8705 Do Not Stuff
TP8701 Do Not Stuff
TP8703 Do Not Stuff
Title
Size
Document Number
Rev
Date:
Sheet


PWR_DCBATOUT_VCCCORE
DCBATOUT
SB 20100908
Non_NEC
NEC
Do Not Stuff
VCC_CORE
PU4308
84.00172.037
2nd = 84.08030.037
PU4309
SIR166DP-T1-GE3-GP
84.00166.037
2nd = 84.08028.037
PL4303
L-D36UH-1-GP
68.R3610.20A
2nd = 68.R3610.10M
PR4314
2D2R3-1-U-GP
PWR_VCCCORE_BOOT1_1
PC4318
SCD22U25V3KX-GP
PWR_VCCCORE_HG1
PWR_VCCCORE_PH1
PWR_VCCCORE_LG1
PWR_VCCCORE_ISEN2
PWR_VCCCORE_ISEN3
PWR_VCCCORE_VSUM-
PWR_VCCCORE_ISEN1
PWR_VCCCORE_VSUM+
PR4315
PR4316
PR4317
1K2F-GP
PR4318
10KR2F-2-GP
PR4319
3K65R2F-1-GP
PTC4306
SE47U25VM-11-GP
PTC4307
PU4306
PU4305
PL4302
SB 20100910
20100804
79.47719.2BL
Pana 470u , 2V
ESR=6mΩ, Iripple=3.5A
PR4308
2D2R3-1-U-GP
PWR_VCCCORE_BOOT2_1
PC4312
PWR_VCCCORE_HG2
PWR_VCCCORE_PH2
PWR_VCCCORE_LG2
PR4309
PR4310
PR4311
PR4312
PR4313
PTC4307
PWR_DCBATOUT_VCCCORE
DCBATOUT
20100728
PU4304
84.00172.037
2nd = 84.08030.037
PU4303
SIR166DP-T1-GE3-GP
84.00166.037
2nd = 84.08028.037
PU4302
ISL6208CRZ-TGP-U
74.06208.073
PL4301
L-D36UH-1-GP
68.R3610.20A
2nd = 68.R3610.10M
PR4301
0R2J-2-GP
PR4302
2D2R3-1-U-GP
PWR_VCCCORE_BOOT3_1
PC4302
SCD22U25V3KX-GP
PWR_VCCCORE_PWM3
PWR_VCCCORE_PH3
PWR_VCCCORE_HG3
PWR_VCCCORE_LG3
PR4303
PR4304
PR4305
PR4306
PR4307
PTC4309
PTC4301
PTC4302
PTC4308
PTC4303
PTC4304
PTC4305
PWR_VCCCORE_VSUM-_1
PWR_VCCCORE_VSUM+_1
PWR_VCCCORE_VSUM-_2
PWR_VCCCORE_VSUM+_2
PWR_VCCCORE_VSUM-_3
PWR_VCCCORE_VSUM+_3
Title
Size
Document Number
Rev


DCBATOUT
PWR_DCBATOUT_GFXCORE
PG4403
PG4404
PG4405
PG4406
PG4407
PG4408
PG4409
Do Not Stuff
PTC4404
SE47U25VM-11-GP
UMA_Muxless
PR4401
1R3J-L1-GP
42 PWR_GFXCORE_BOOT
PWR_GFXCORE_BOOT_1
PC4407
SCD22U25V3KX-GP
42 PWR_GFXCORE_HG
42 PWR_GFXCORE_PH
42 PWR_GFXCORE_LG
PU4401
84.00172.037
2nd = 84.08030.037
SIR172DP-T1-GE3-GP
PU4403
SIR166DP-T1-GE3-GP
84.00166.037
2nd = 84.08028.037
PC4401
PC4402
PC4403
PC4404
SC4D7U25V5KX-GP
20100721
RFC4413
RFC4414
RFC4412
SC56P50V2JN-2GP
SC100P50V3JN-GP-U
SCD01U25V2KX-3GP
VCC_GFXCORE
Iomax=12A
OCP>18A
SB 20100908
PL4401
IND-D36UH-9-GP
PG4401
PG4402
68.R3610.20K
0.36uH, Idc=24A
DCR=0.76+/-5% mohm
PTC4401
SE330U2VDM-L-GP
79.33719.L01
PTC4402
PWR_GFXCORE_ISP_R
PWR_GFXCORE_ISN_R
PC4408
PR4402
PC4409
SCD1U10V2KX-4GP
PR4403
1R2F-GP
PR4404
649R2F-GP
PR4405
NTC-10K-27-GP
PC4410
PC4411
SCD068U6V3KX-GP
SCD022U25V2KX-GP
PR4406
11K2F-L-GP
PR4407
7K5R2F-1-GP
PR4408
10KR2F-2-GP
PWR_GFXCORE_ISN 42
PWR_GFXCORE_ISP 42
20100906
SB 20100831
Title
Size
Document Number
Rev
Date:
Sheet

TPS51218D for 1D05V



SSID = PWR.Plane.Regulator_1p5v0p75v

20100805

RT8207L for 1D5V

DCBATOUT PWR_DCBATOUT_1D5V
PG4601 PG4602 PG4603 PG4604 Do Not Stuff
PTC4601 Do Not Stuff
DY

19,27 PM_SLP_S4# PR4612 Do Not Stuff PWR_1D5V_EN
PC4612 Do Not Stuff
DY

SB 20100831

PWR_1D5V_VCC5 PR4604 5D1R2F-GP 5V_S5
PC4606 SC1U10V2KX-1GP
PC4602 SC1K50V2KX-1GP
PR4603 12K4R2F-GP
PWR_1D5V_VDDP PR4605 Do Not Stuff 5V_S5
C694 SC1U10V2KX-1GP
PWR_1D5V_CS

3D3V_S5 PR4602 10KR2F-2-GP
Close to pin23
45,47 RUNPWROK
PWR_DCBATOUT_1D5V PR4610 620KR2F-GP PWR_1D5V_TON
PWR_1D5V_EN
PWR_0D75V_EN
PWR_1D5V_VTTIN
1D5V_S3 PG4605 Do Not Stuff PG4606 Do Not Stuff PC4603 SC10U6D3V5MX-3GP
1D5V_S3 PG4607 Do Not Stuff PWR_1D5V_VDDQ
DDR_VREF_PWR
Close to pin23

CS VDD VDDP BOOT UGATE PHASE LGATE PGND NC#17 VDDQ FB DEM VTTREF
PGOOD TON S5 S3 VLDOIN NC#7 VTTGND MODE VTT VTTSNS GND GND

PU4601 RT8207LGQW-GP-U1 74.08207.B73

20100728
Id=12.9A
Qg=9.8~15nC
Rdson=10.3~12.4mohm

SB
PR4606 2D2R3-1-U-GP
PC4609 SCD1U25V3KX-GP
PWR_1D5V_BOOT PWR_1D5V_PHASE_L PWR_1D5V_UGATE PWR_1D5V_PHASE PWR_1D5V_LGATE PWR_1D5V_VDDQ PWR_1D5V_FB 5V_S5

-1 PR4608 需要將來都改32K4R

R1 PR4608 33KR2F-GP DY PC4610 Do Not Stuff
R2 PR4609 30KR2F-GP

Close to output cap pin1, not inside of the output cap
2nd source 還未導入74.51116.073

PR4607 Do Not Stuff DDR_VREF_S3
PWR_1D5V_VTTREF
PC4608 SCD033U16V2KX-GP
Close to PIN9

37 0D75V_EN PR4615 Do Not Stuff PWR_0D75V_EN

+0.75VS
Iomax: 1.2A

0D75V_S0 PG4608 Do Not Stuff PG4609 Do Not Stuff DDR_VREF_PWR
PC4604 SC10U6D3V5MX-3GP PC4605 Do Not Stuff DY

PWR_DCBATOUT_1D5V
RFC4617 SC1U25V2KX-3GP RFC4618 SC1000P50V3JN-GP-U RFC4616 SC56P50V2JN-2GP

20100906

PWR_DCBATOUT_1D5V
PC4611 PC4614 PC4616 PC4617 PC4615 SC4D7U25V5KX-GP SCD1U25V3KX-GP

PU4602 84.15N03.037 2nd = 84.08065.037 RMW150N03FUB-GP-U1
PU4603 84.18003.037 2nd = 84.18002.037 RMW180N03FUBTB-GP

Mag. 1.0uH 10*10*4
DCR=2.9~3.3mohm
Idc=18A, Isat=36A
Iomax=12A
OCP>20A

1D5V_S3 PL4601 IND-1UH-93-GP 68.1R01B.10J 2nd = 68.1R01C.10Q
PC4613 Do Not Stuff DY
PTC4602 SE390U2D5VM-7GP 79.3971V.30L 2nd = 79.3971V.6AL
Matsuki cap 390uF 2.5V, ESR=10mohm

Vout=0.75*(1+R1/R2)

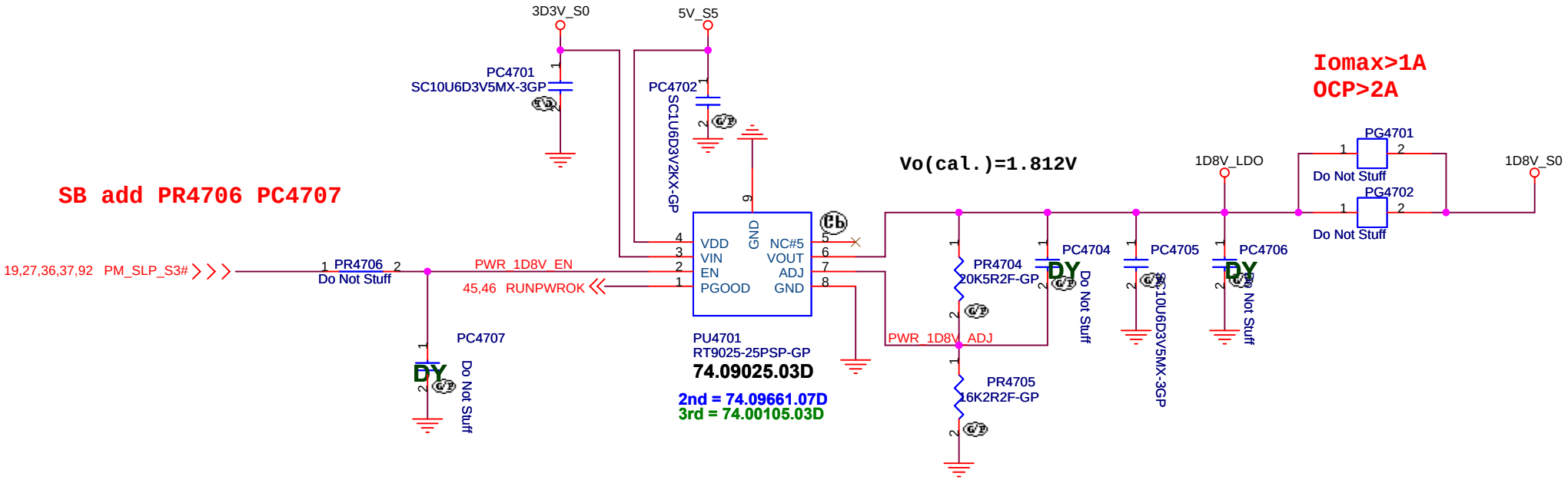
20100728

SB R4608 chekc 修改31K6R
Vout 需再1.55V 以上

Title		
Size	Document Number	Rev
Date:	Sheet	

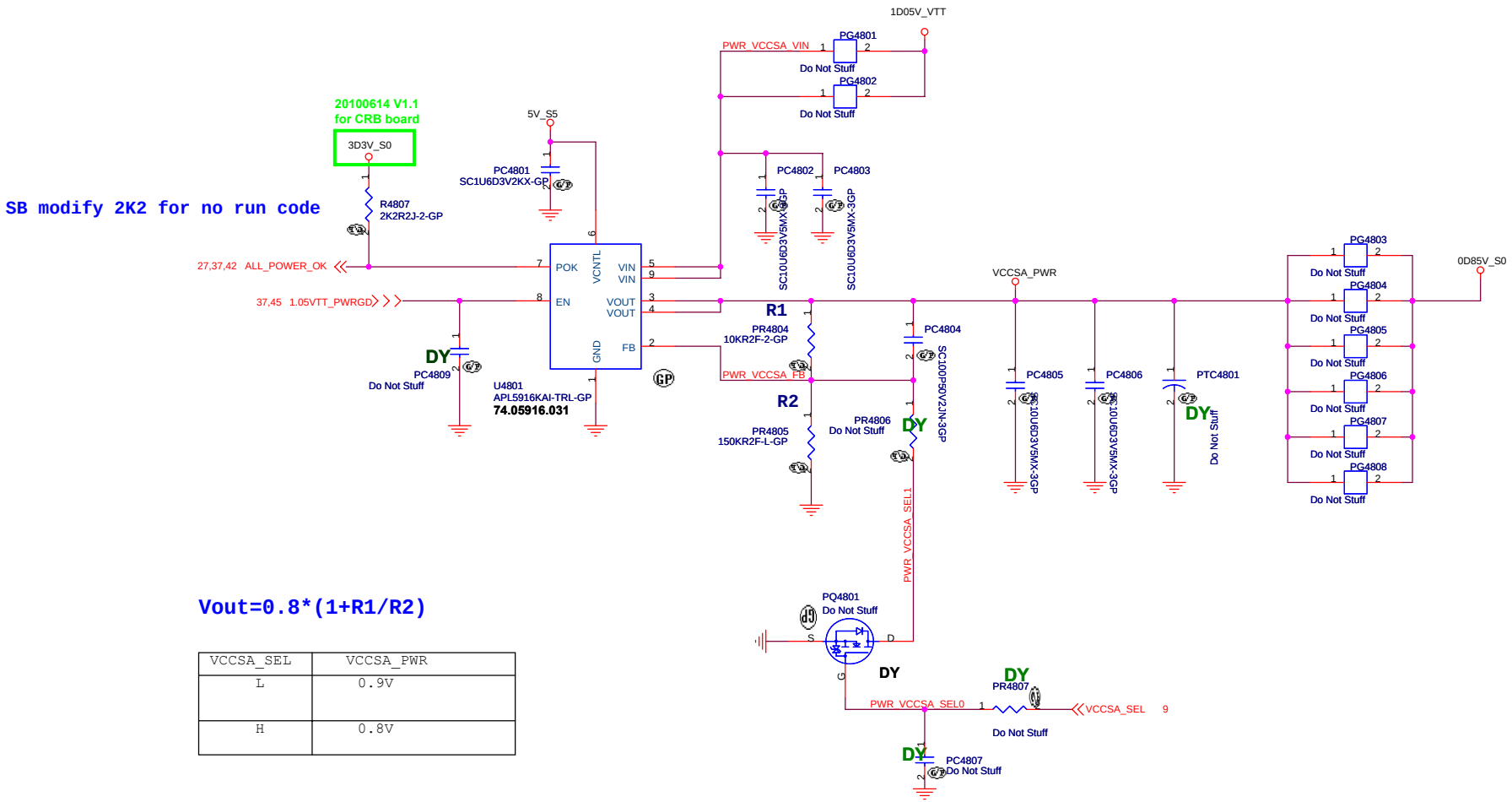
SSID = PWR.Plane.Regulator_1p8v

RT9025 for 1D8V_S0



Title		
Size	Document Number	Rev
Date:	Sheet	

APL5916 for VCCSA

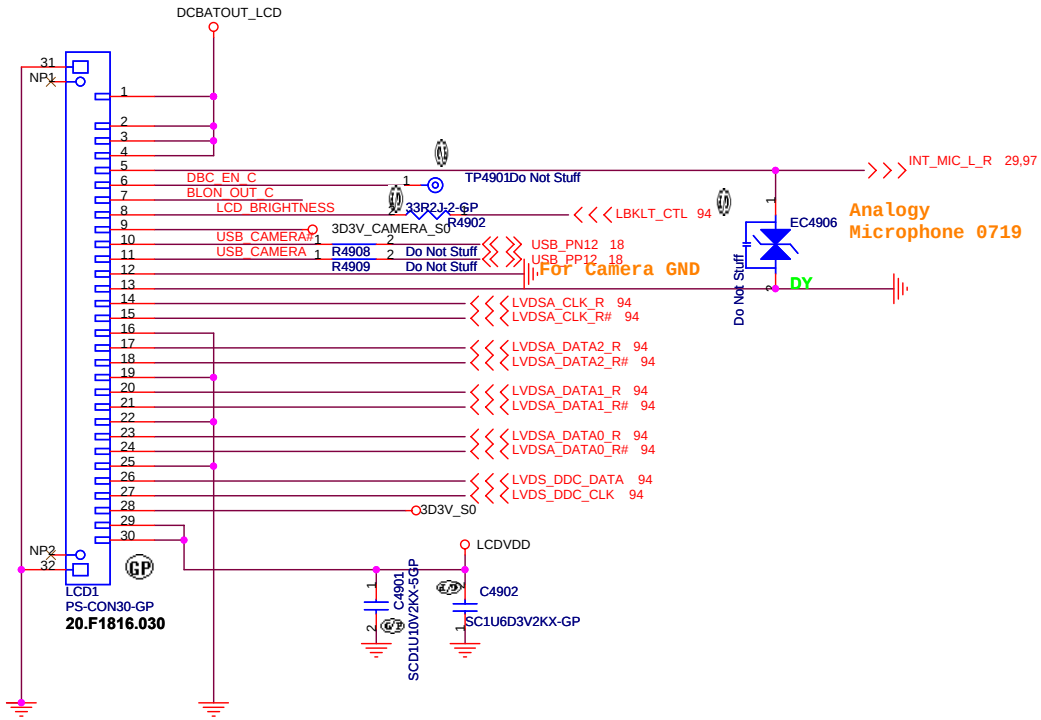


Vout=0.8*(1+R1/R2)

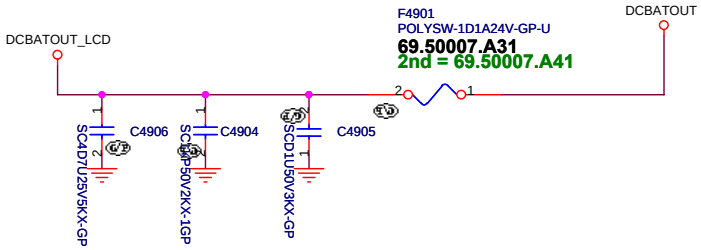
VCCSA_SEL	VCCSA_PWR
L	0.9V
H	0.8V

Title		
Size	Document Number	Rev
Date:	Sheet	

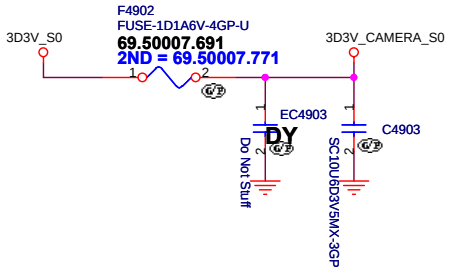
LVDS CONNECTOR



INVERTER POWER

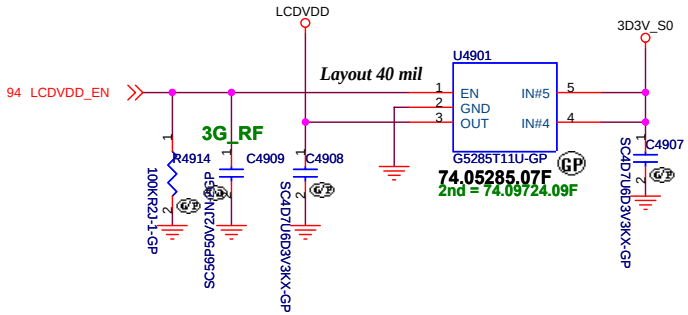


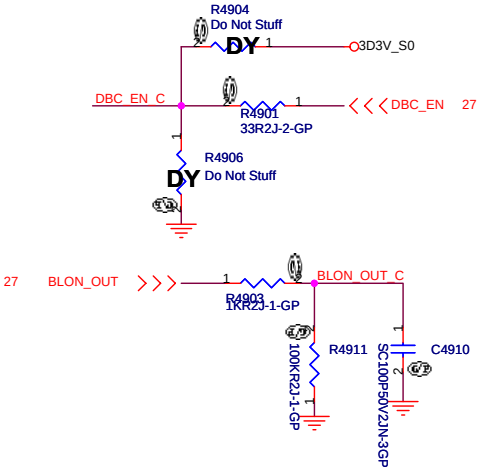
Camera Power



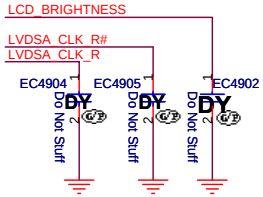
SSID = VIDEO

LCD POWER for ANNIE

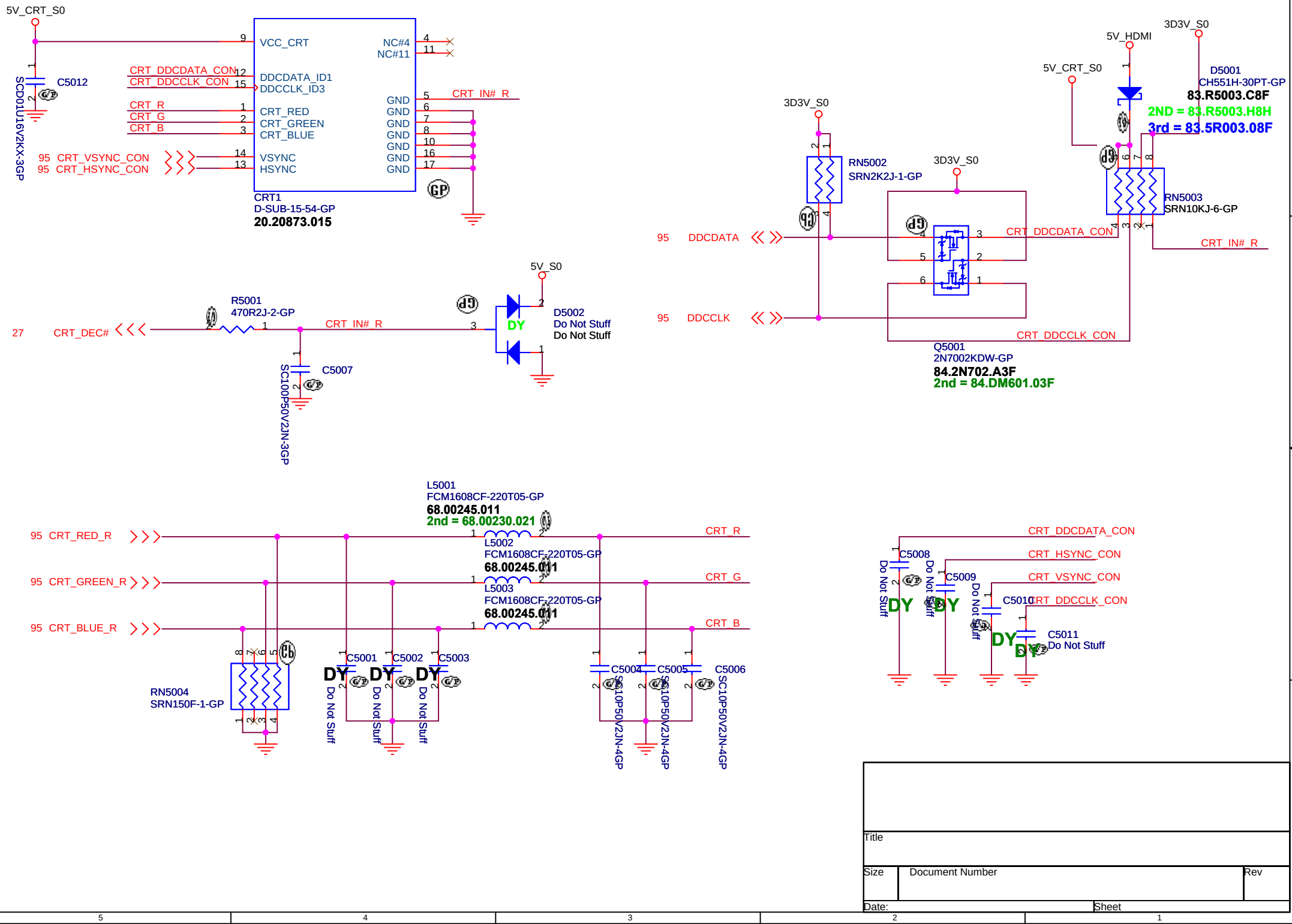




For EMI request
Close to LVDS connector



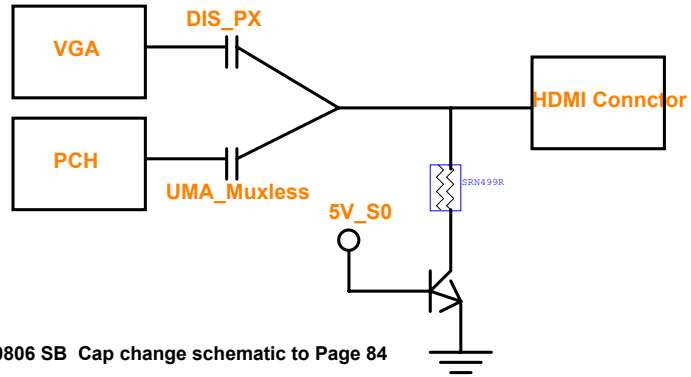
Title		
Size	Document Number	Rev
Date:	Sheet	


5V_CRT_S0
C5012
SCD01U16V2KX-3GP
CRT_DDCDATA_CON
CRT_DDCCLK_CON
CRT_R
CRT_G
CRT_B
95 CRT_VSYNC_CON
95 CRT_HSYNC_CON
VCC_CRT
DDCDATA_ID1
DDCCLK_ID3
CRT_RED
CRT_GREEN
CRT_BLUE
VSYNC
HSYNC
NC#4
NC#11
GND
CRT_IN#_R
CRT1
D-SUB-15-54-GP
20.20873.015
3D3V_S0
5V_HDMI
5V_CRT_S0
D5001
CH551H-30PT-GP
83.R5003.C8F
2ND = 83.R5003.H8H
3rd = 83.5R003.08F
RN5002
SRN2K2J-1-GP
RN5003
SRN10KJ-6-GP
95 DDCDATA
95 DDCCLK
CRT_DDCDATA_CON
CRT_DDCCLK_CON
CRT_IN#_R
Q5001
2N7002KDW-GP
84.2N702.A3F
2nd = 84.DM601.03F
5V_S0
R5001
470R2J-2-GP
27 CRT_DEC#
CRT_IN#_R
D5002
Do Not Stuff
Do Not Stuff
C5007
SC100P50V2JN-3GP
L5001
FCM1608CF-220T05-GP
68.00245.011
2nd = 68.00230.021
L5002
FCM1608CF-220T05-GP
68.00245.011
L5003
FCM1608CF-220T05-GP
68.00245.011
95 CRT_RED_R
95 CRT_GREEN_R
95 CRT_BLUE_R
CRT_R
CRT_G
CRT_B
RN5004
SRN150F-1-GP
C5001
C5002
C5003
C5004
C5005
C5006
DY
Do Not Stuff
SC10P50V2JN-4GP
C5008
C5009
C5010
C5011
CRT_DDCDATA_CON
CRT_HSYNC_CON
CRT_VSYNC_CON
CRT_DDCCLK_CON
Title
Size
Document Number
Rev
Date:
Sheet

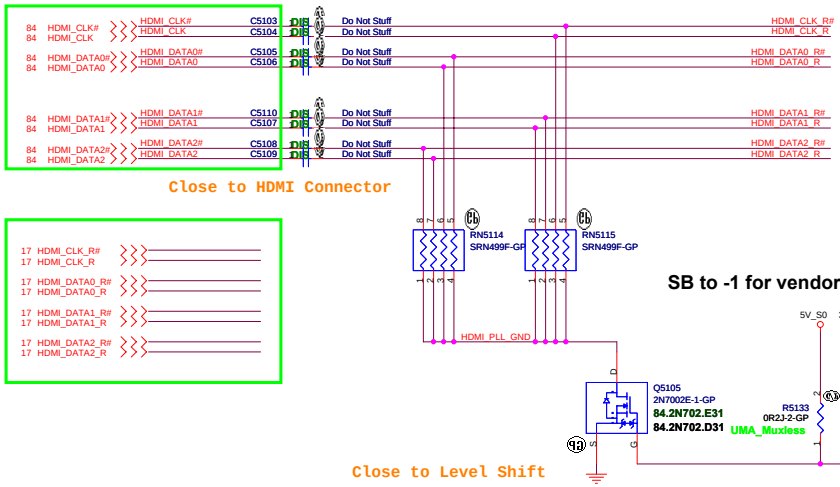
HDMI Level Shifter & CONNECTOR

UMA_Muxless : default setting used PS8101. if don't used PS8101
please change C5103~C5110 to 0 ohm resister

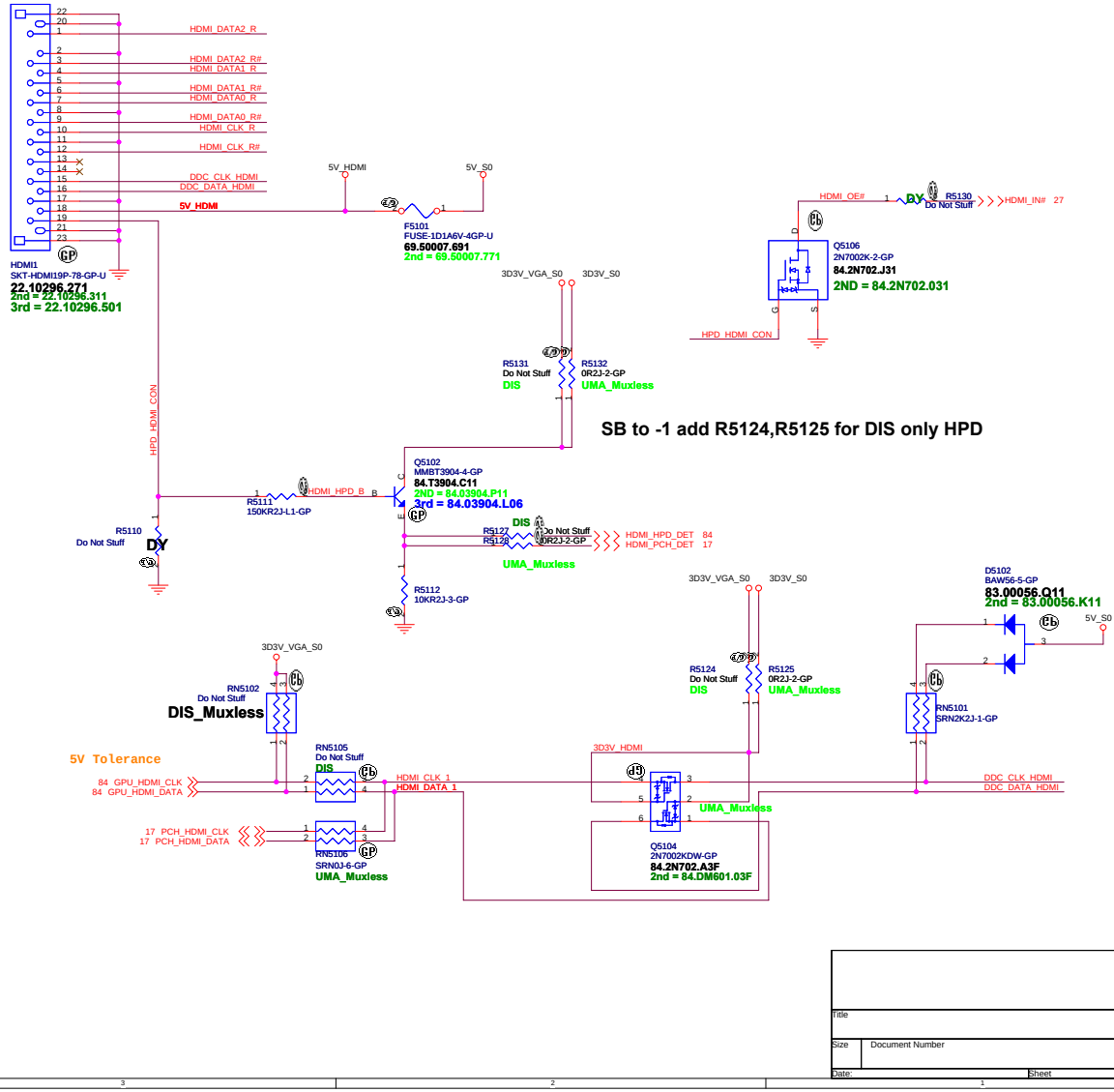
HDMI DISCRETE/ UMA Co-lay



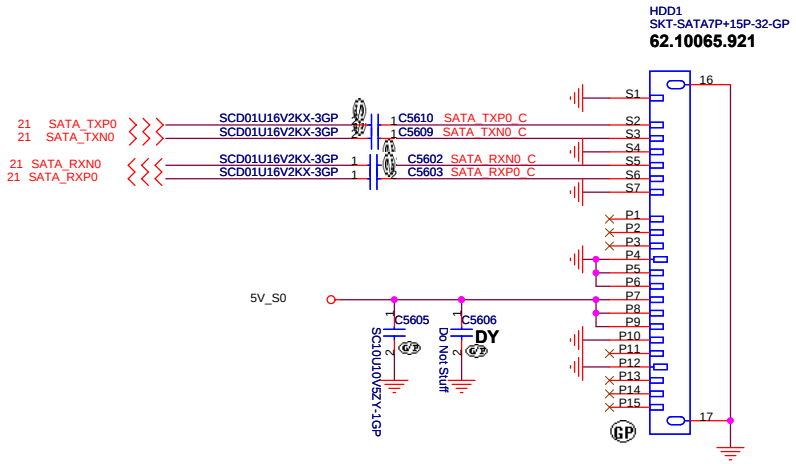
0806 SB Cap change schematic to Page 84



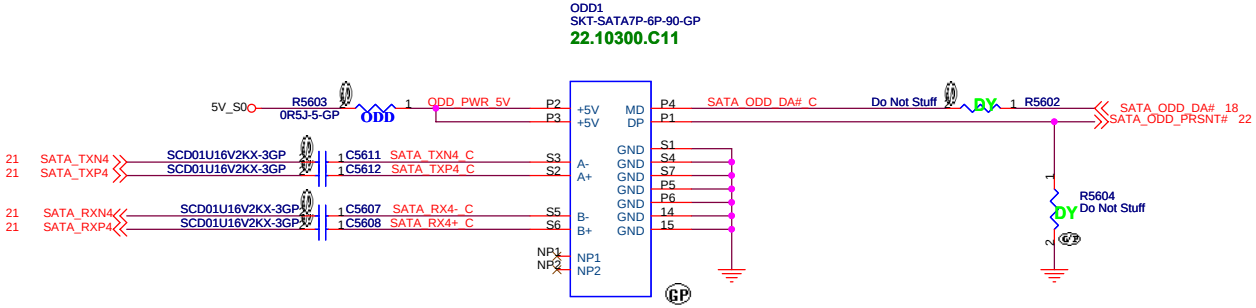
HDMI CONN

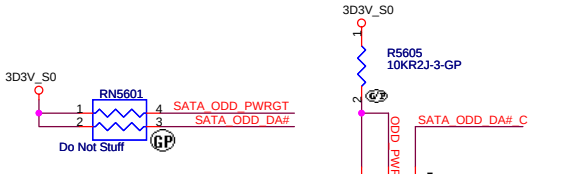


Title		
Size	Document Number	Rev
Date:		Sheet



ODD Connector



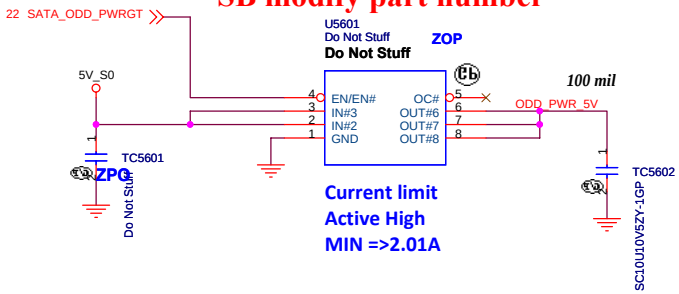


0707 Modify:
Change Q5601 to DUAL 2N7002 for isolate MD/DA signal between PCH and ODD.

SB

SATA Zero Power ODD

SB modify part number



Title		
Size	Document Number	Rev
Date:	Sheet	

GIGA Lan Transformer

LAN MDI Off-Page

XF5901
XFORM-12P-36-GP
68.HD081.30B
Change:68.68160.30B
2nd = 68.HD081.30B

XF5902
XFORM-12P-36-GP
68.HD081.30B
Change:68.68160.30B
2nd = 68.HD081.30B

SB modiyf Pin9 Pin10 SWAP

LED COLOR
10(+) 9(-)::GREEN
12(+) 13(-):ORANGE

RJ45
RJ45-12P-16-GP
22.10321.Y21
2nd = 22.10321.Y91

RN5901
SRN470J-4-GP-U

EC5901 EC5902
Do Not Stuff
DY DY

SB modify For EMI

U5901 U5902 U5903 U5904
TVLST2304AD0-GP
SURGE

GDT1 GDT2 GDT3 GDT4
SURGE

C5905
SC1KP2KV6KX-GP

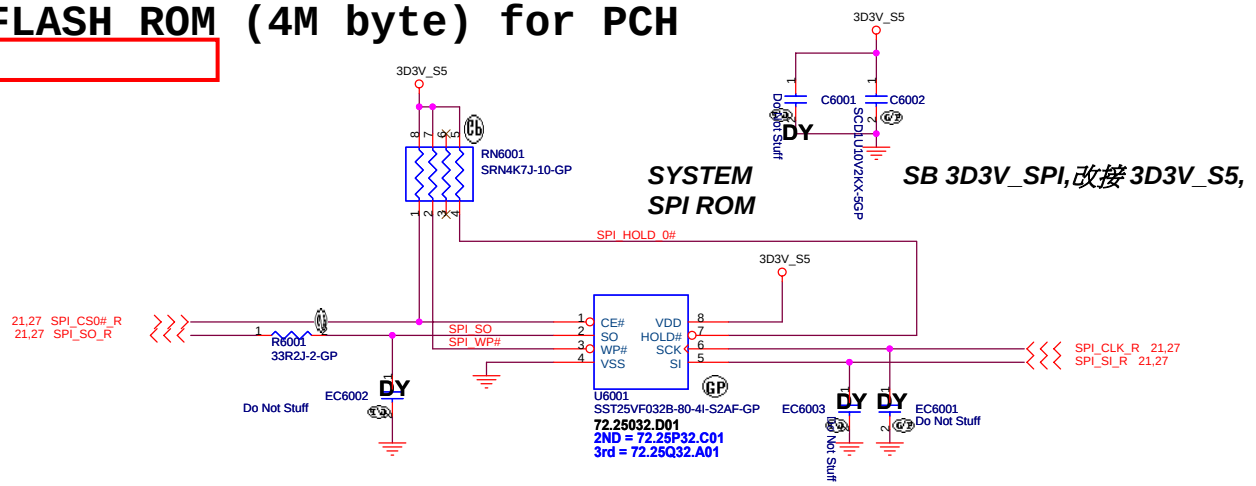
C5907 C5906
DY DY
Do Not Stuff

C5916 C5917 C5918 C5919
DY Do Not Stuff

EC5910 EC5909 EC5903 EC5904 EC5905 EC5906 EC5908 EC5907
Do Not Stuff

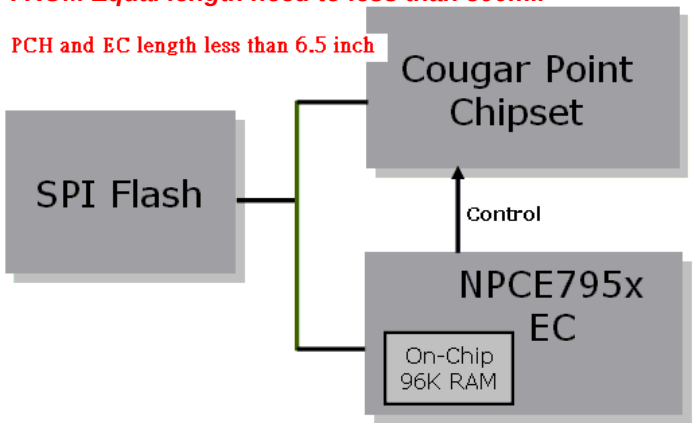
Title
Size Document Number Rev
Date: Sheet

SPI FLASH ROM (4M byte) for PCH

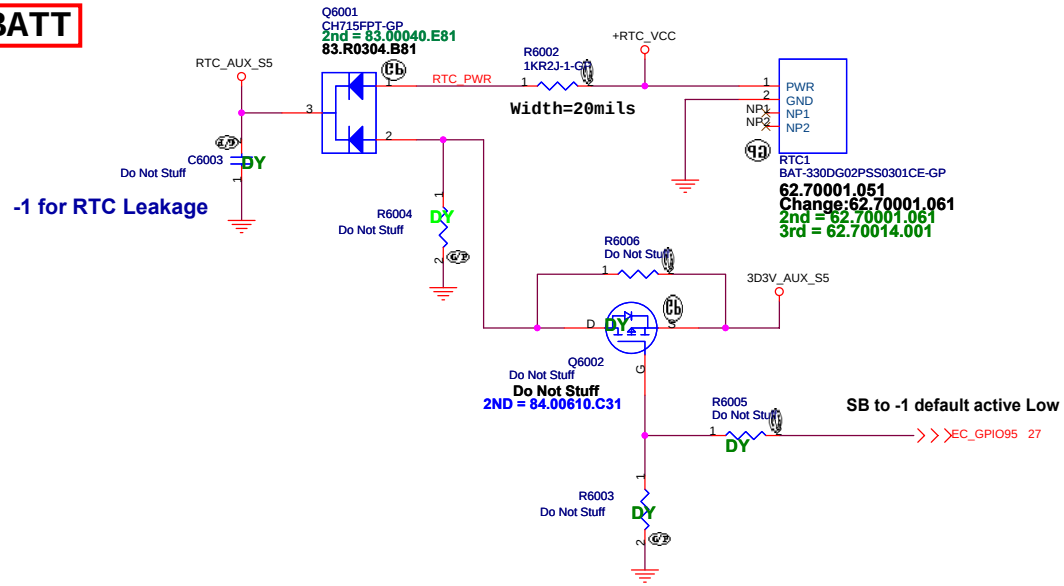


SPI ROM Equal length need to less than 500mil

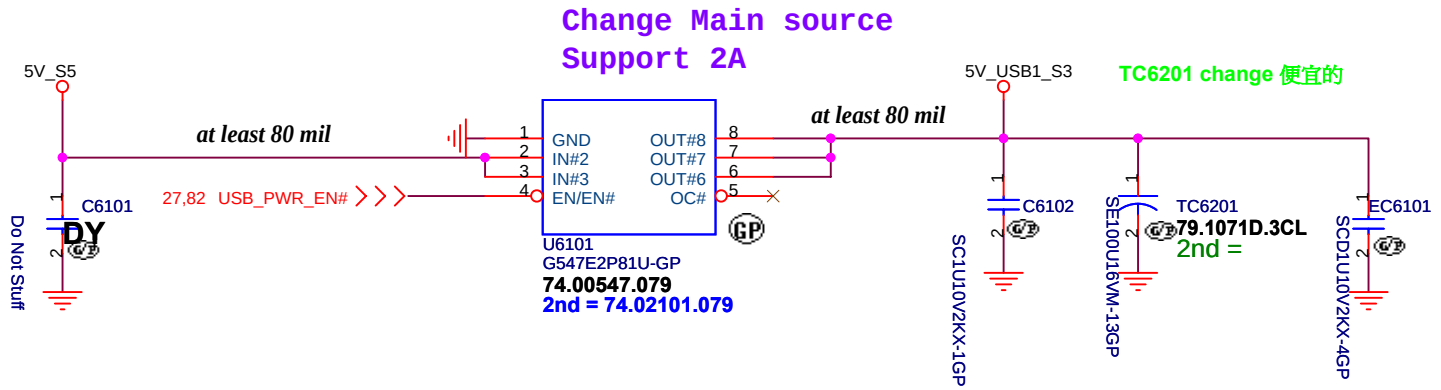
PCH and EC length less than 6.5 inch

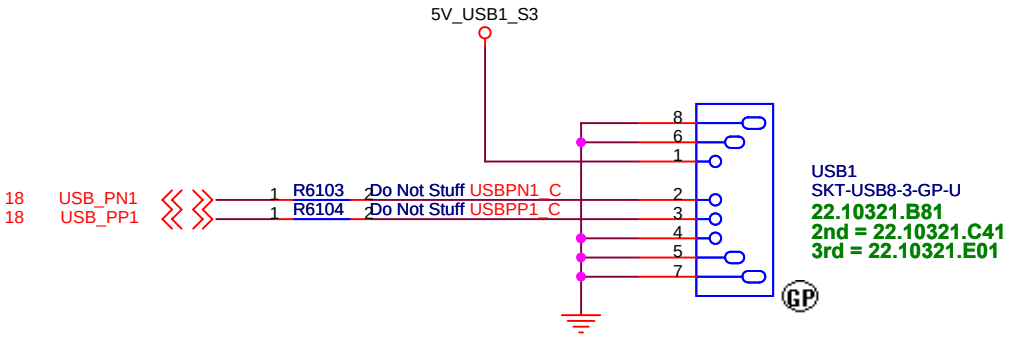


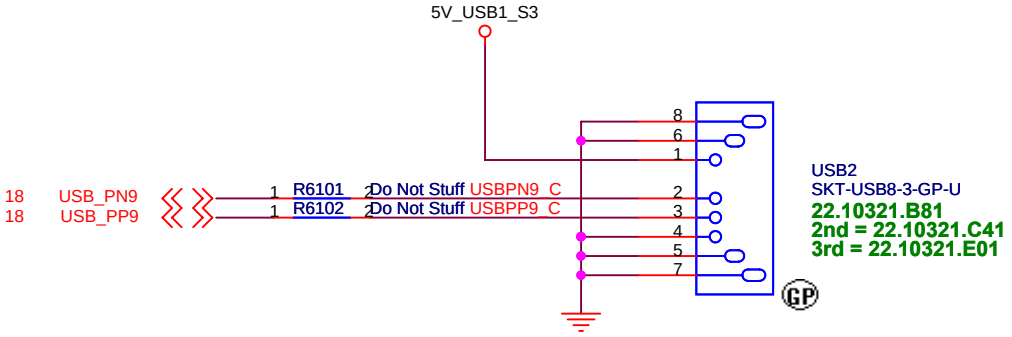
SSID = RBATT



Title		
Size	Document Number	Rev
Date:	Sheet	



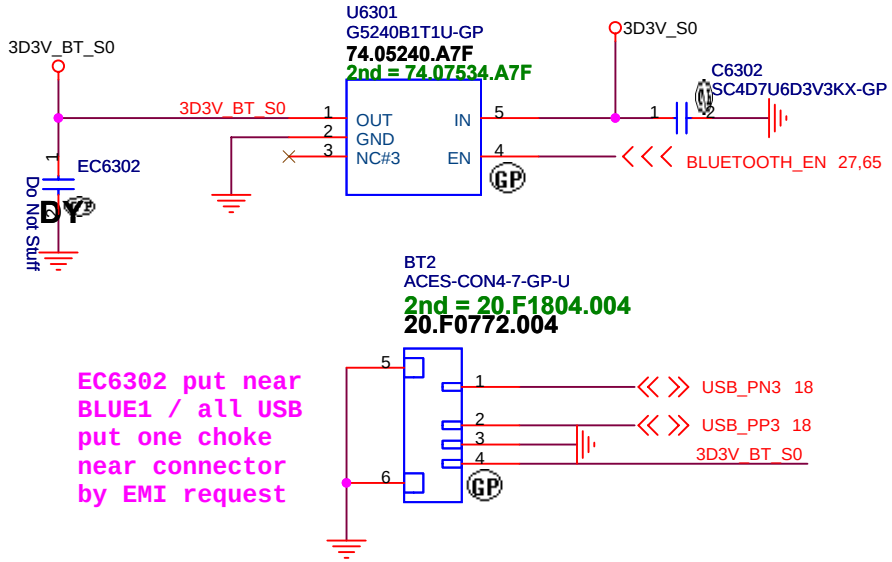




Title		
Size	Document Number	Rev
Date:	Sheet	

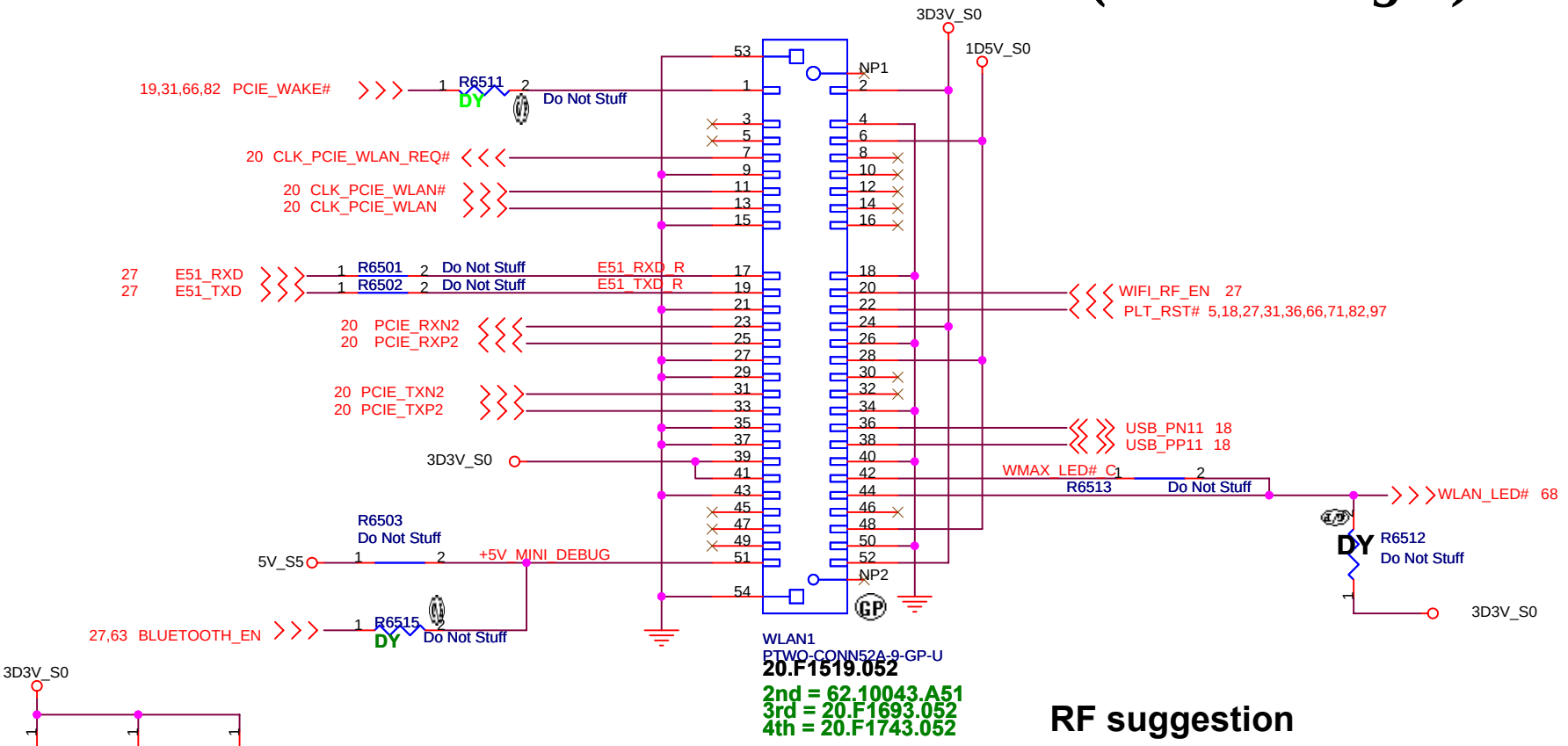
Bluetooth Module conn.

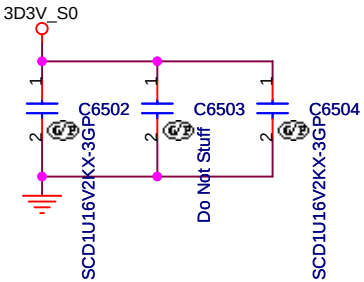
ANNIE Bluetooth Module



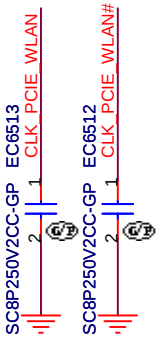
Title		
Size	Document Number	Rev
Date:	Sheet	

Mini Card Connector(802.11a/b/g/n)

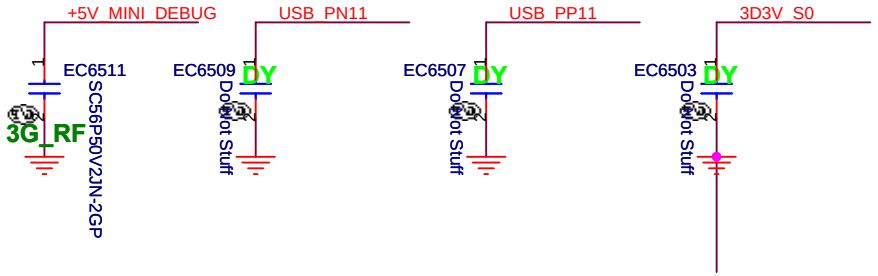




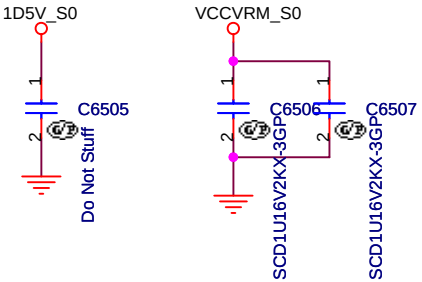
SB modify for SIV



RF suggestion



-2

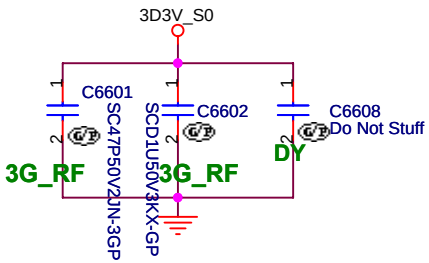


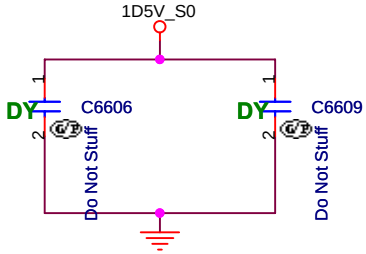
Title		
Size	Document Number	Rev
Date:	Sheet	

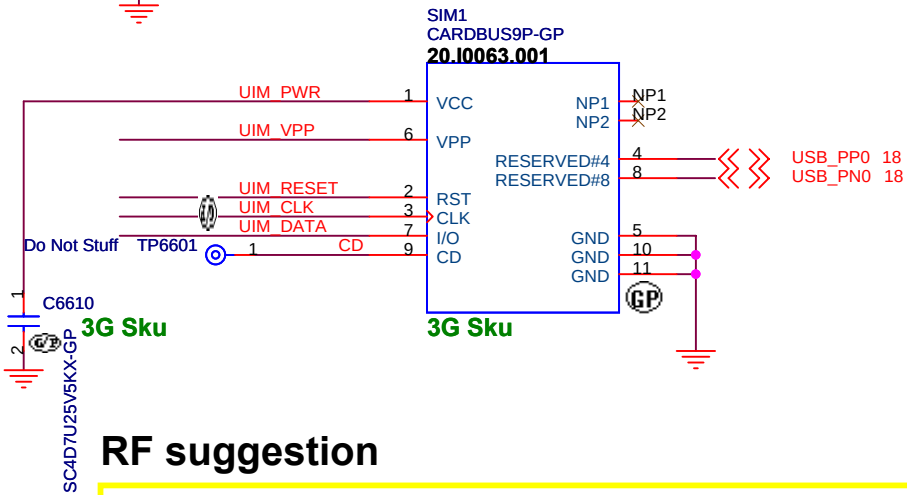
Mini Card Connector(WWAN)

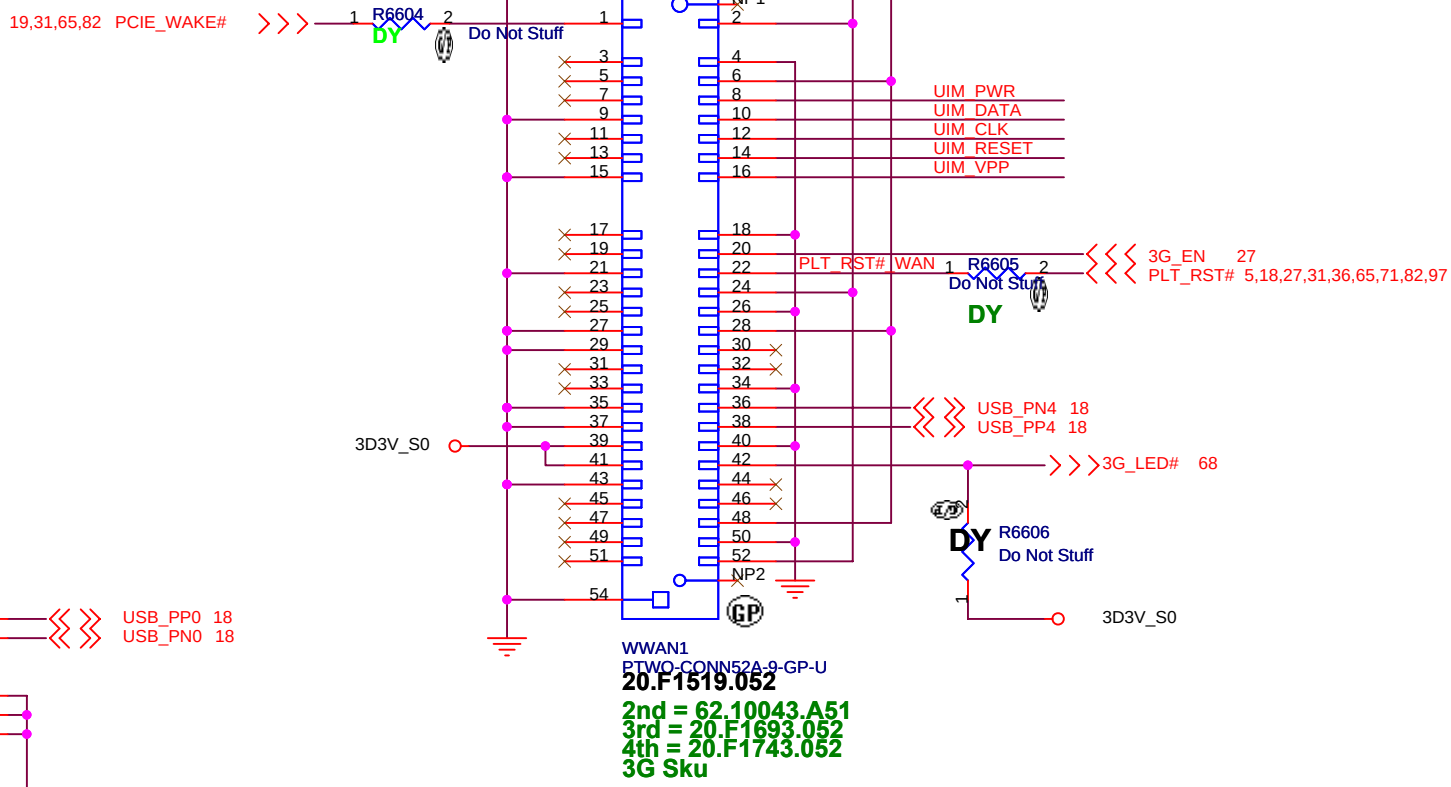
20100712 V1.5

Place near MINI Card CONN

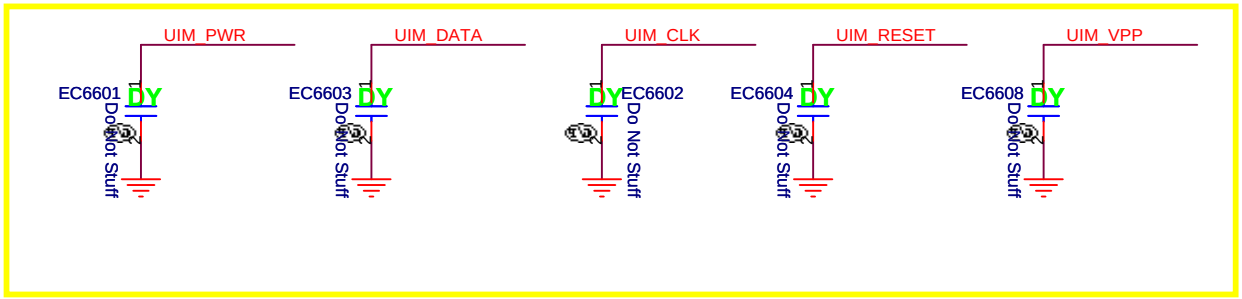




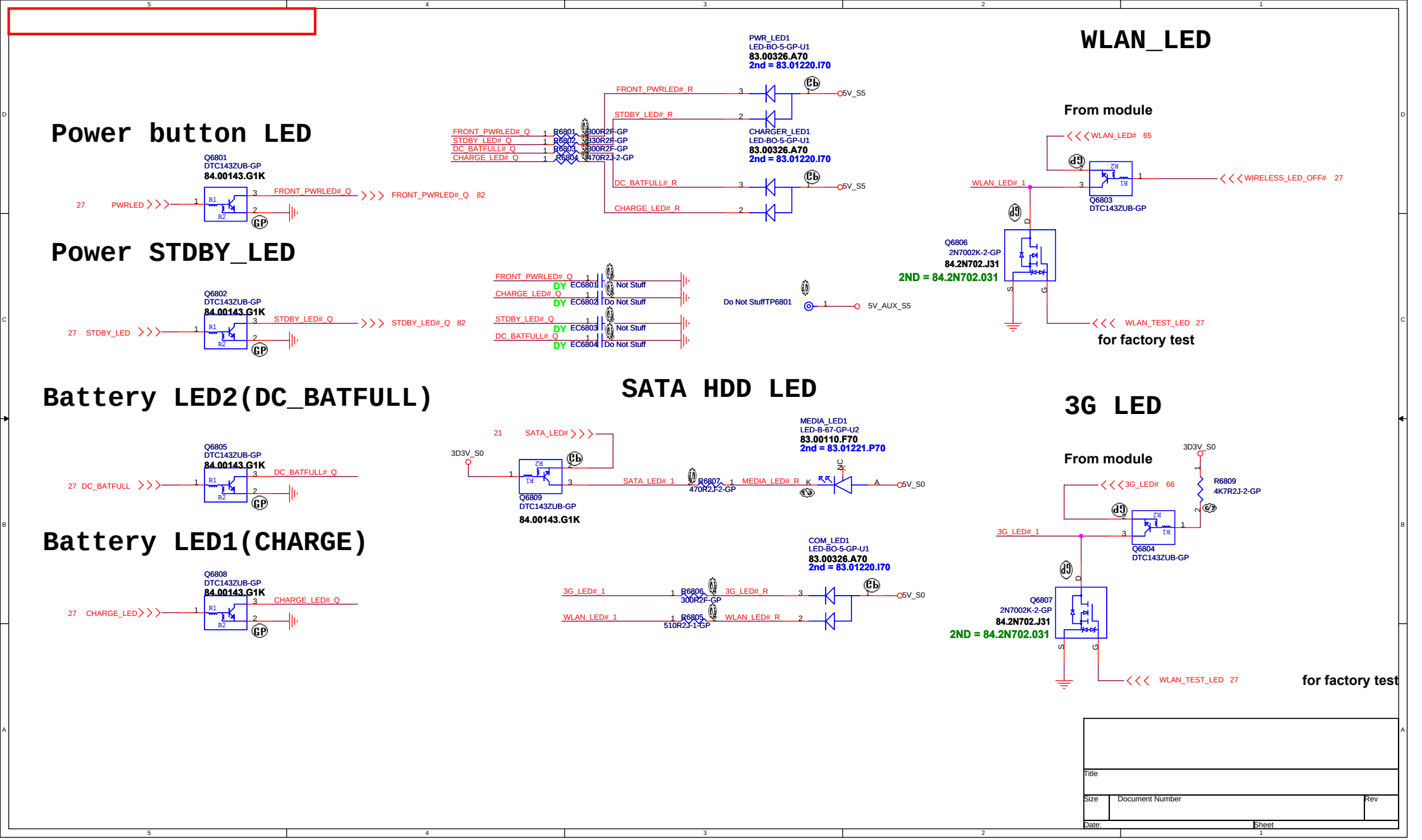




RF suggestion



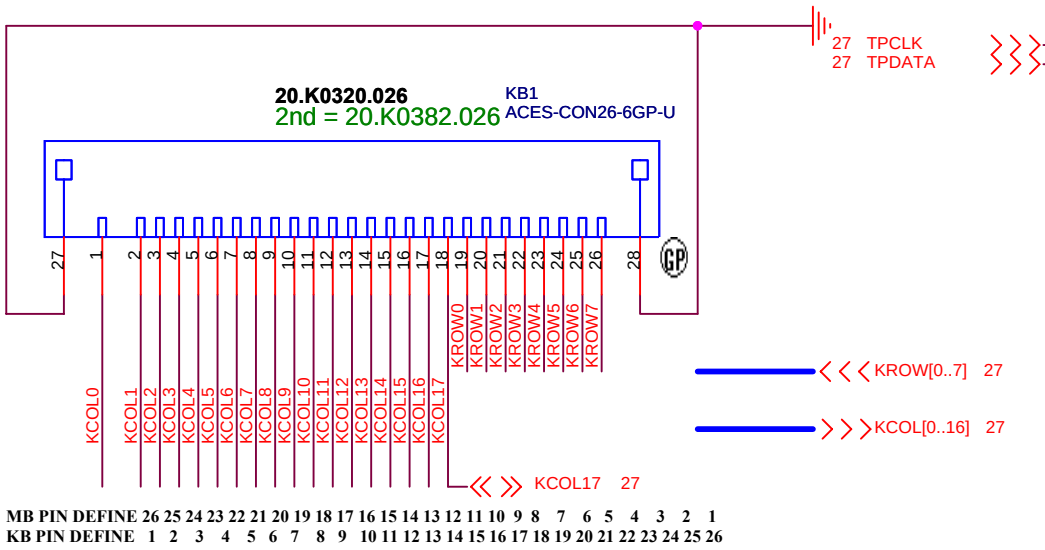
Title		
Size	Document Number	Rev
Date:		Sheet


Power button LED
Q6801
DTC143ZUB-GP
84.00143.G1K
27 PWRLED
FRONT_PWRLED# Q
FRONT_PWRLED# Q 82
PWR_LED1
LED-BO-5-GP-U1
83.00326.A70
2nd = 83.01220.I70
FRONT_PWRLED# R
STDBY_LED# R
5V_S5
FRONT_PWRLED# Q
STDBY_LED# Q
DC_BATFULL# Q
CHARGE_LED# Q
R6801 300R2F-GP
R6802 330R2F-GP
R6803 300R2F-GP
R6804 470R2J-2-GP
CHARGER_LED1
LED-BO-5-GP-U1
83.00326.A70
2nd = 83.01220.I70
DC_BATFULL# R
CHARGE_LED# R
Power STDBY_LED
Q6802
DTC143ZUB-GP
84.00143.G1K
27 STDBY_LED
STDBY_LED# Q
STDBY_LED# Q 82
FRONT_PWRLED# Q
CHARGE_LED# Q
STDBY_LED# Q
DC_BATFULL# Q
DY EC6801 Not Stuff
DY EC6802 Do Not Stuff
DY EC6803 Not Stuff
DY EC6804 Do Not Stuff
Do Not StuffTP6801
5V_AUX_S5
WLAN_LED
From module
WLAN_LED# 65
WLAN_LED# 1
WIRELESS_LED_OFF# 27
Q6803
DTC143ZUB-GP
Q6806
2N7002K-2-GP
84.2N702.J31
2ND = 84.2N702.031
WLAN_TEST_LED 27
for factory test
Battery LED2(DC_BATFULL)
Q6805
DTC143ZUB-GP
84.00143.G1K
27 DC_BATFULL
DC_BATFULL# Q
SATA HDD LED
21 SATA_LED#
3D3V_S0
Q6809
DTC143ZUB-GP
84.00143.G1K
SATA_LED# 1
R6807
470R2J-2-GP
MEDIA_LED1
LED-B-67-GP-U2
83.00110.F70
2nd = 83.01221.P70
MEDIA_LED# R
5V_S0
3G LED
From module
3D3V_S0
3G_LED# 66
R6809
4K7R2J-2-GP
3G_LED# 1
Q6804
DTC143ZUB-GP
Q6807
2N7002K-2-GP
84.2N702.J31
2ND = 84.2N702.031
WLAN_TEST_LED 27
for factory test
Battery LED1(CHARGE)
Q6808
DTC143ZUB-GP
84.00143.G1K
27 CHARGE_LED
CHARGE_LED# Q
COM_LED1
LED-BO-5-GP-U1
83.00326.A70
2nd = 83.01220.I70
3G_LED# 1
R6806
300R2F-GP
3G_LED# R
WLAN_LED# 1
R6805
510R2J-1-GP
WLAN_LED# R
5V_S0
Title
Size
Document Number
Rev
Date:
Sheet

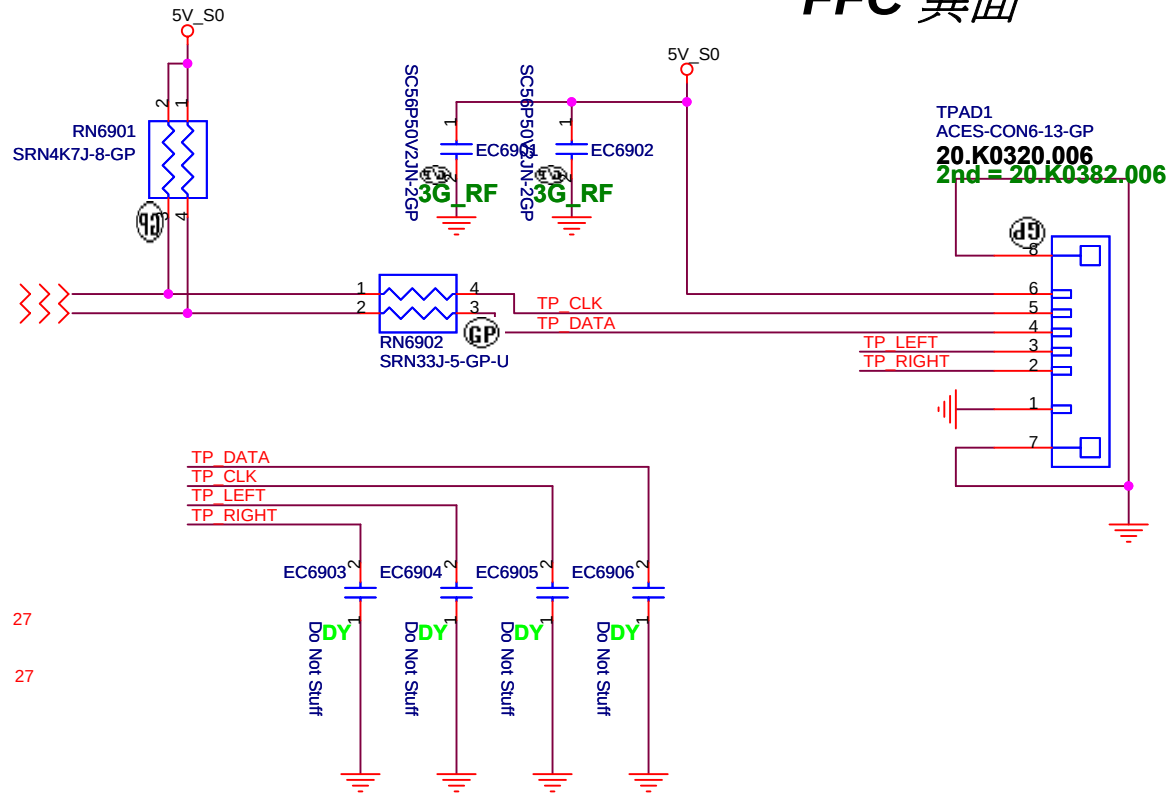
TOUCH PAD

FFC 異面

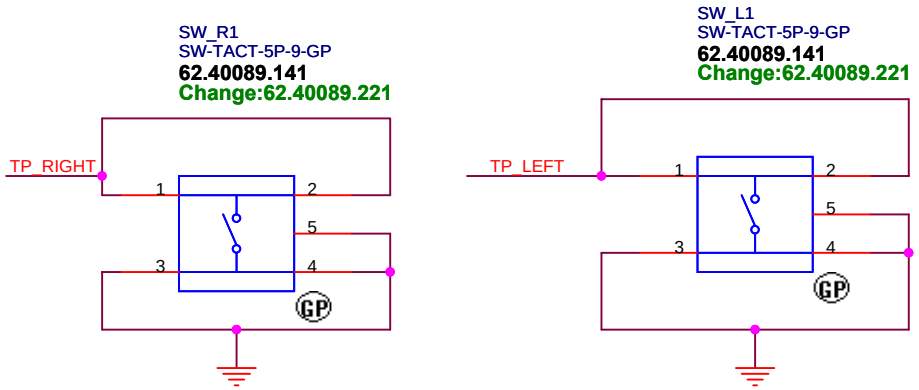
Internal KeyBoard Connector



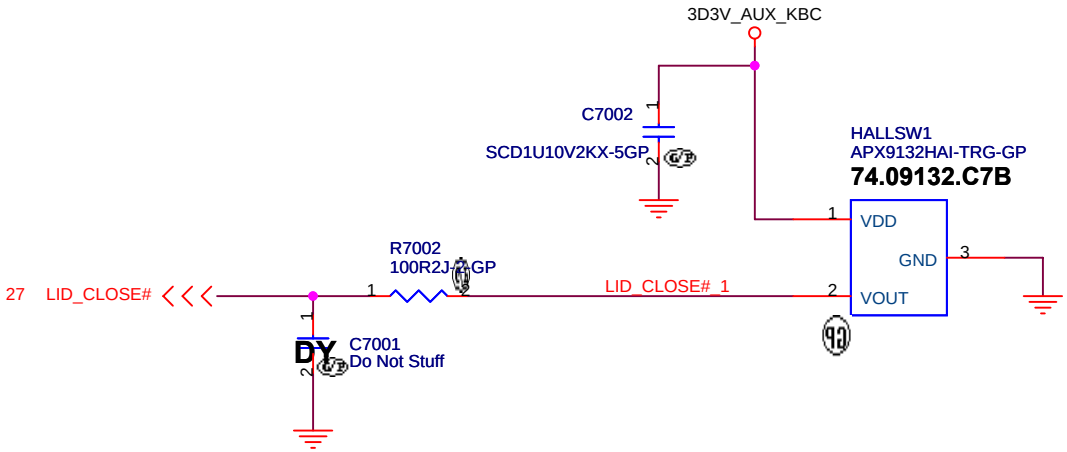
MB PIN DEFINE 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
KB PIN DEFINE 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26



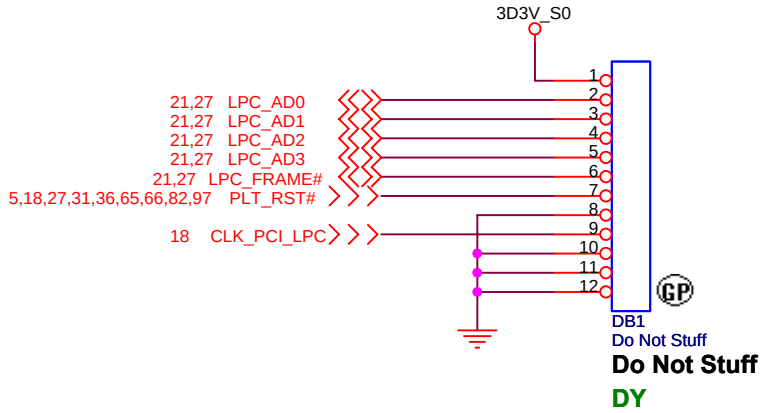
26 K/B 1 **SB to -1 modify Part number**



Title		
Size	Document Number	Rev
Date:		Sheet

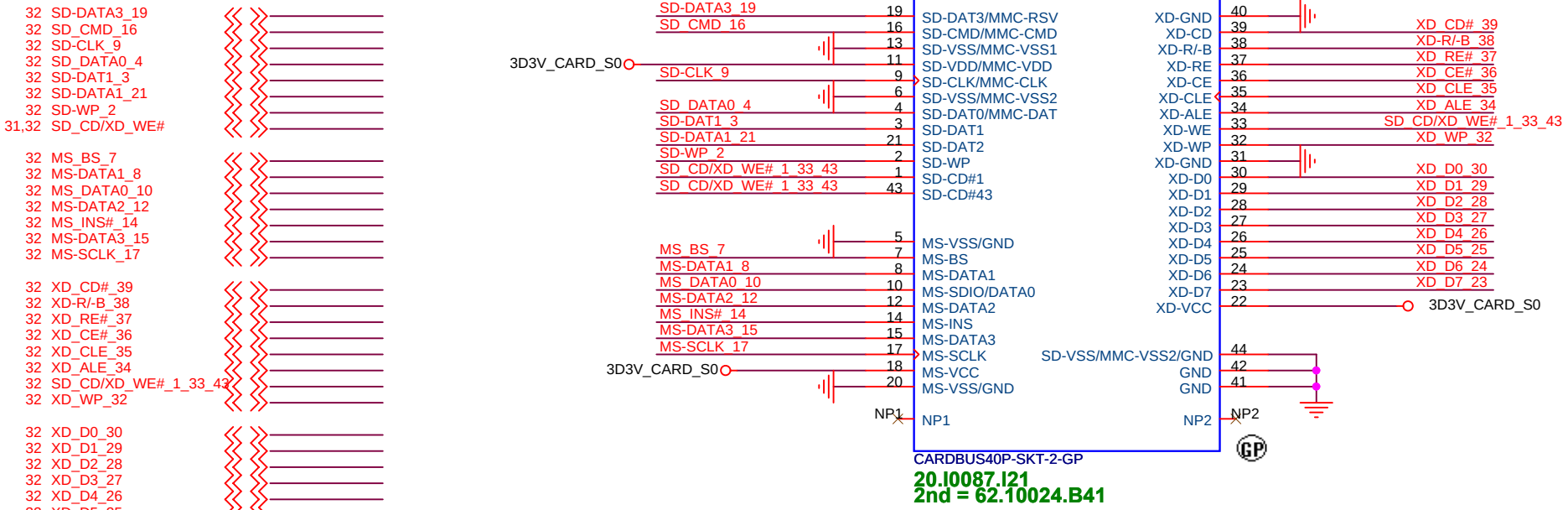


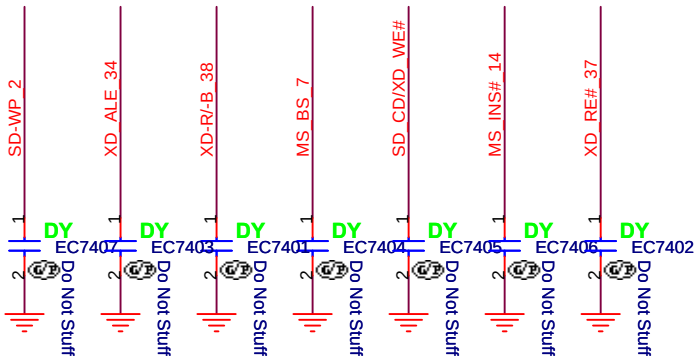
Title		
Size	Document Number	Rev
Date:	Sheet	



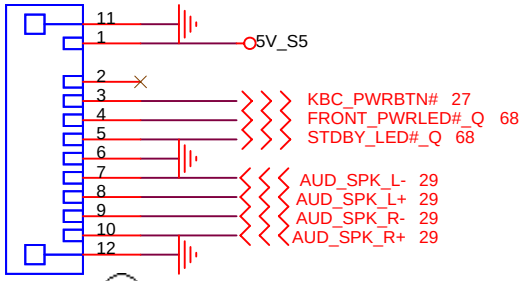
Title		
Size	Document Number	Rev
Date:		Sheet

SD/XD/MS Card Reader

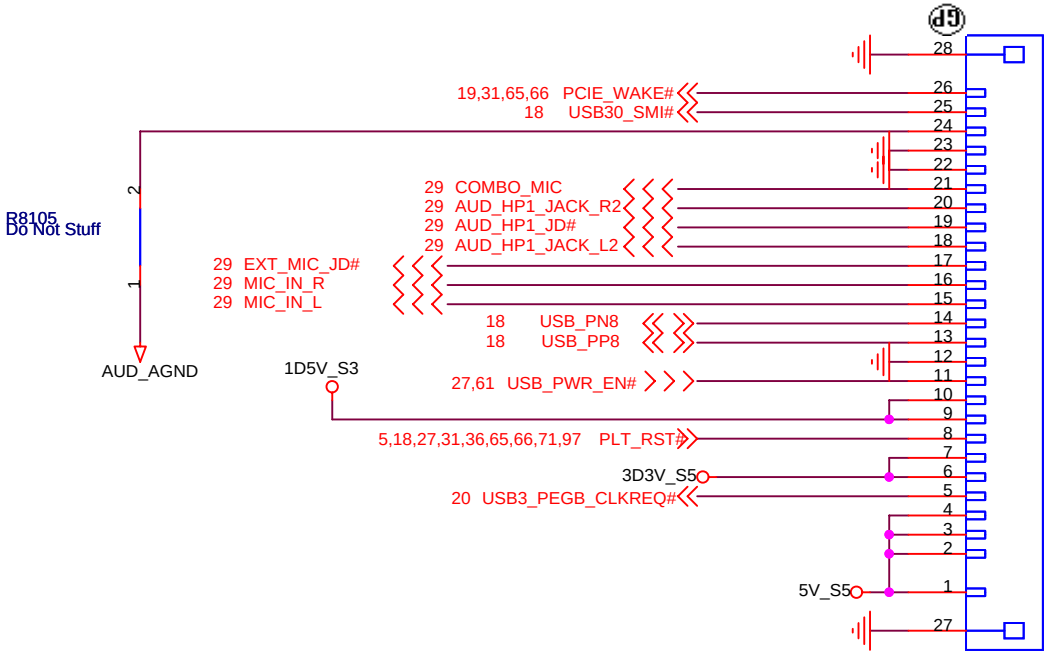




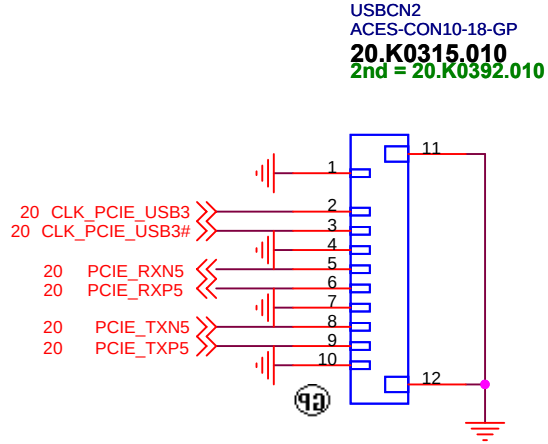
Title		
Size	Document Number	Rev
Date:	Sheet	



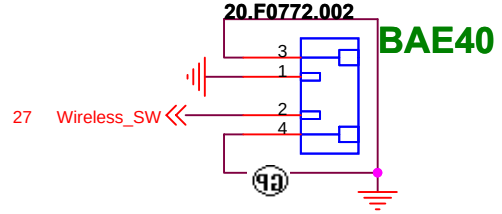
PWRCN1
ACES-CON10-20-GP
20.K0422.010
2nd = 20.K0382.010



USBCN1
ACES-CON26-11-GP
20.K0315.026
2nd = 20.K0370.026

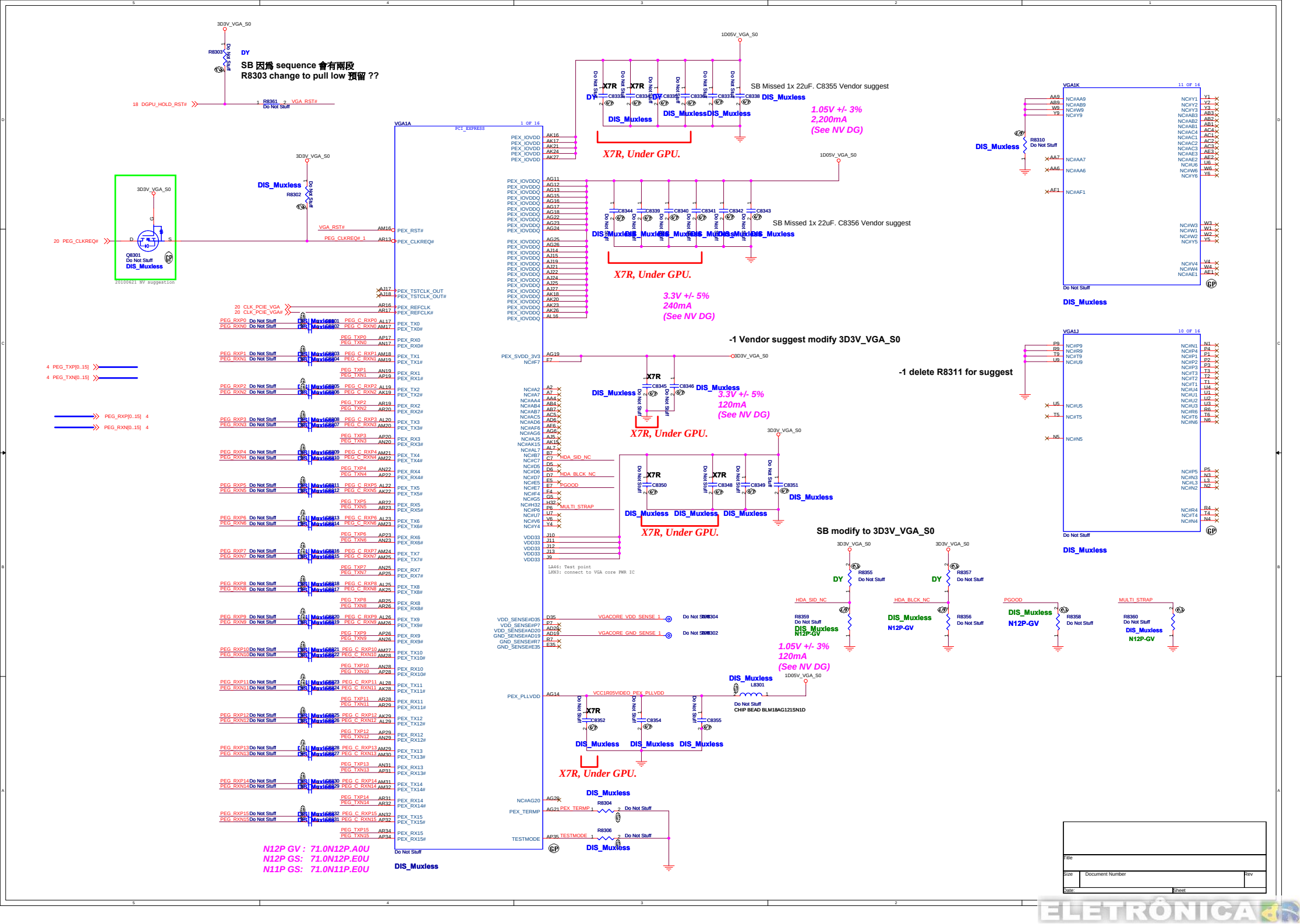


USBCN2
ACES-CON10-18-GP
20.K0315.010
2nd = 20.K0392.010

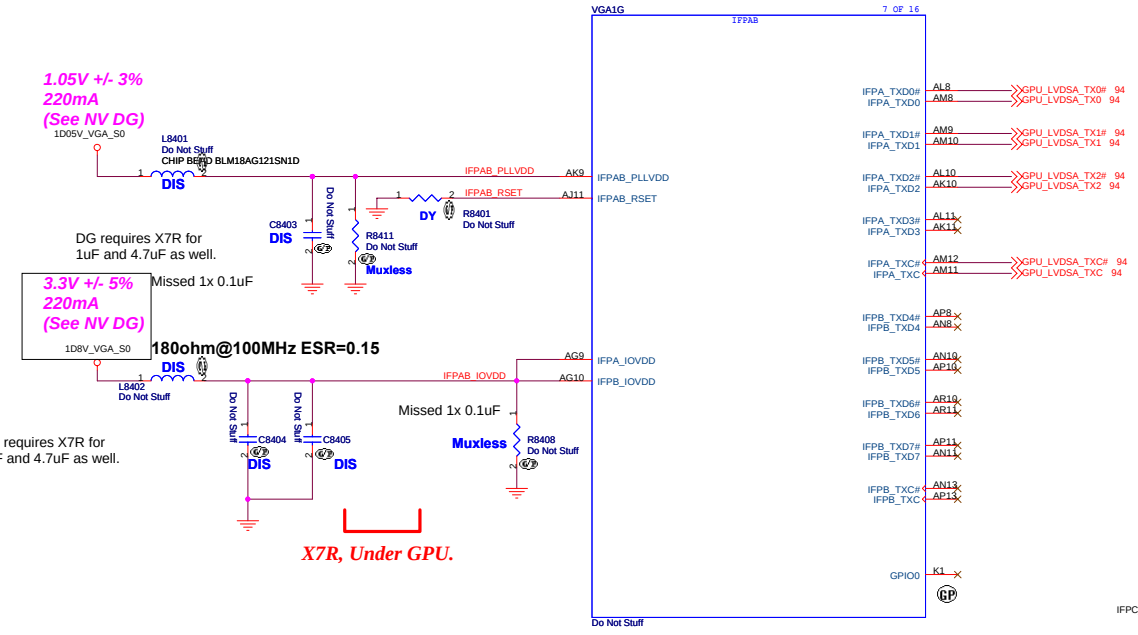


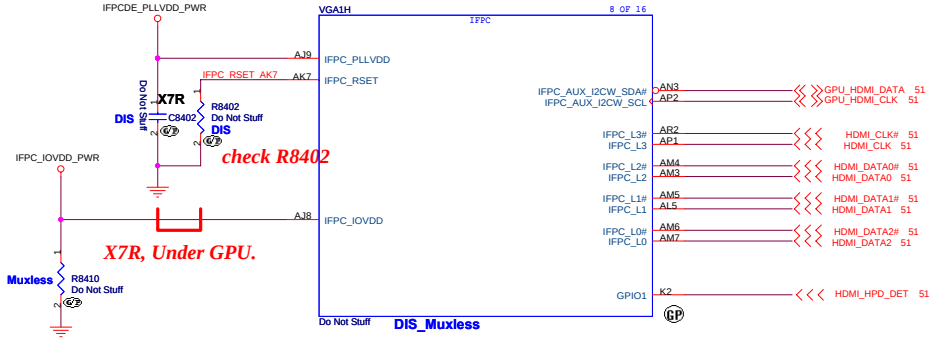
RF_CN1
ACES-CON2-11-GP
20.F0772.002
BAE40

Title		
Size	Document Number	Rev
Date:	Sheet	

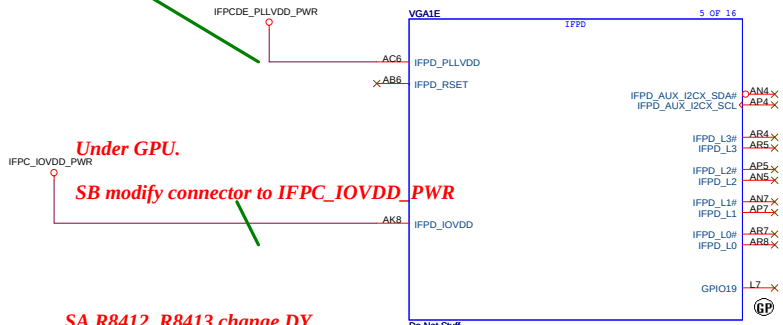

SB 因爲 sequence 會有兩段
R8303 change to pull low 預留 ??
SB Missed 1x 22uF. C8355 Vendor suggest
1.05V +/- 3%
2,200mA
(See NV DG)
X7R, Under GPU.
SB Missed 1x 22uF. C8356 Vendor suggest
3.3V +/- 5%
240mA
(See NV DG)
-1 Vendor suggest modify 3D3V_VGA_S0
3.3V +/- 5%
120mA
(See NV DG)
-1 delete R8311 for suggest
SB modify to 3D3V_VGA_S0
1.05V +/- 3%
120mA
(See NV DG)
N12P GV : 71.0N12P.A0U
N12P GS: 71.0N12P.E0U
N11P GS: 71.0N11P.E0U
20100621 NV suggestion

LVDS Interface

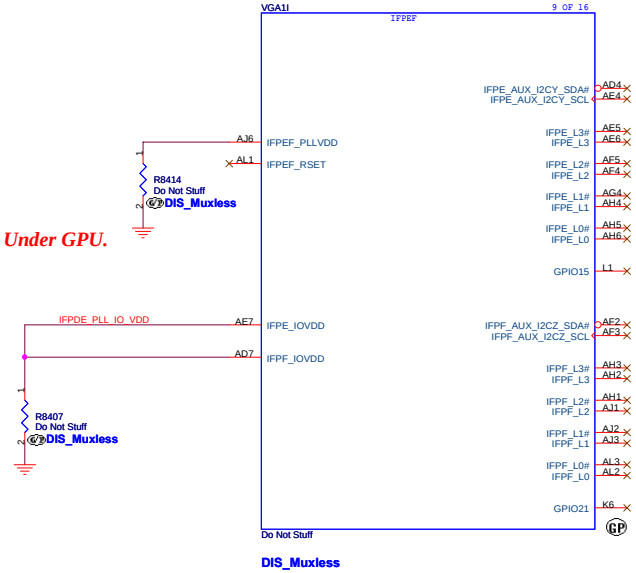




SB modify connector to IFPCDE_PLLVDD_PWR

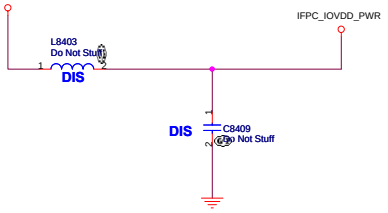


SA R8412, R8413 change DY
SB R8412, R8413 change delete

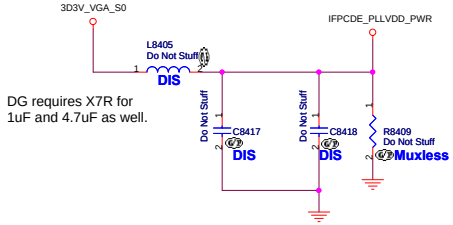


HDMI Interface

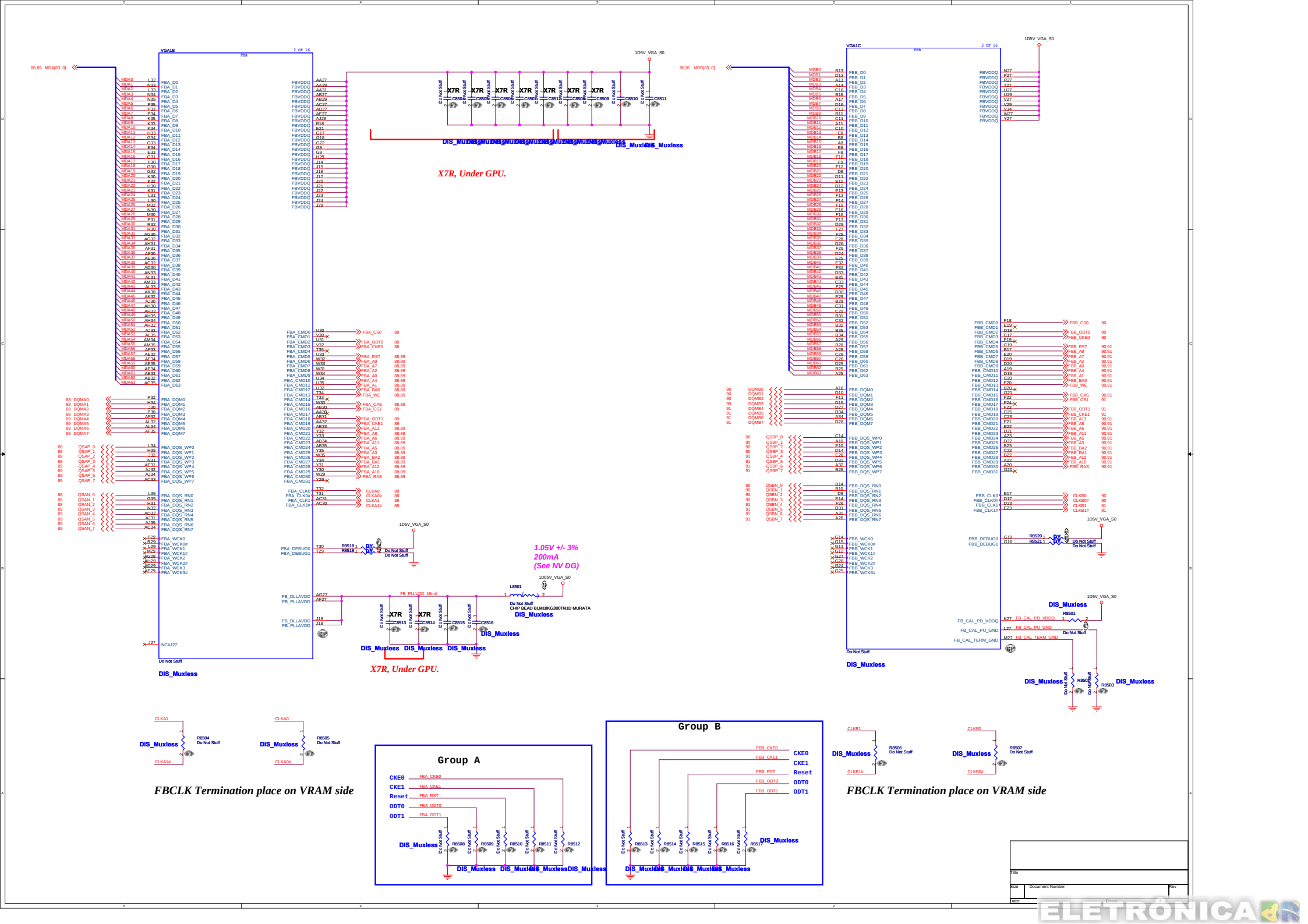
1.05V +/- 3%
285mA
(See NV DG)
1D05V_VGA_S0
220ohm@100MHz ESR=0.05

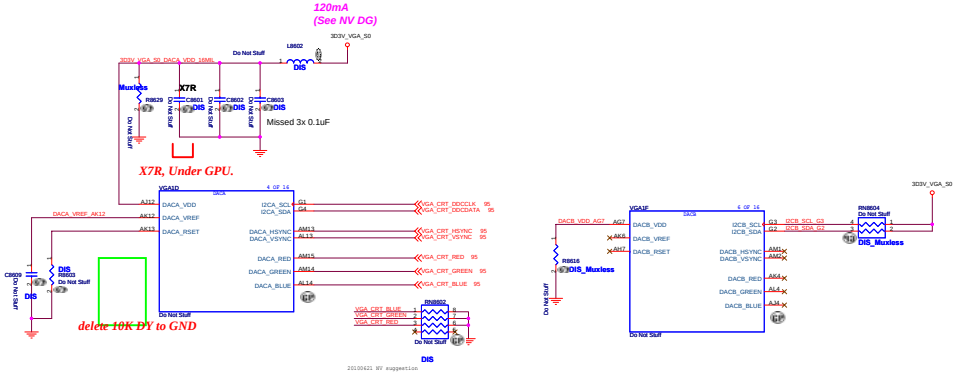


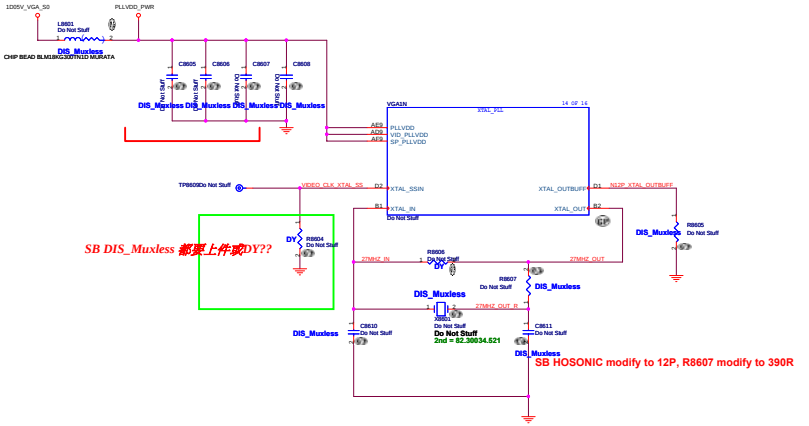
3.3V +/- 5%
440mA (220mA each, max 2 links)
(See NV DG)
300ohm@100MHz ESR=0.25



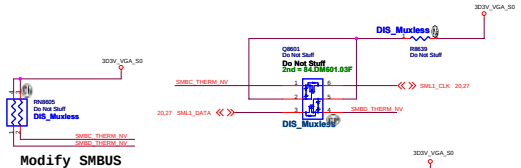
Title		
Size	Document Number	Rev
Date:		Sheet

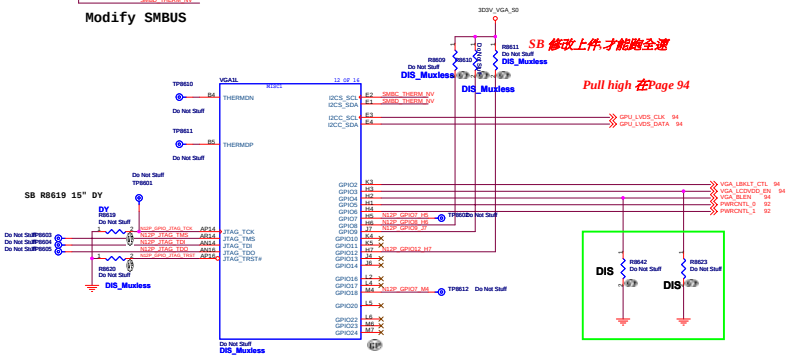

VGA1B
FBA
2 OF 16
VGA1C
FBB
3 OF 16
1D5V_VGA_S0
X7R, Under GPU.
1.05V +/- 3%
200mA
(See NV DG)
DIS_Muxless
Do Not Stuff
FBCLK Termination place on VRAM side
Group A
Group B
CKE0
CKE1
Reset
ODT0
ODT1



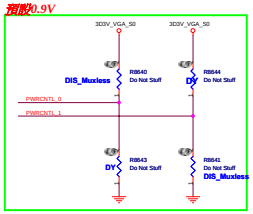


VGA Thermal sensor P2800





SJM50-CP SUPPORT						
P-STATE	NVVDD_ALT_V1	NVVDD_ALT_V0	N11M-GE1	N11M-GE2	N11M-GP1	N11P-GE1	N11P-GE Fermi
P12	0	0	0.85V	0.85V	0.85V	0.85V	0.85V
P8	0	1	0.85V	0.85V	0.85V	0.85V	0.9V
P0	1	0	1.03V	1.03V	1.03V	0.95V	0.95V



NVIDIA TABLE

	Hynix 2G 0110 128*16*8 800MHZ	Hynix 1G 0000 64*16*8 800MHZ	Samsung 1G 0011 64*16*8 800MHZ	Samsung 512 64*16*4 800MHZ	Samsung 2G 0111 128*16*8 800MHZ
RO M_SIPD R8627	34.8Kohm 64.34825.6DL	5Kohm 64.49915.6DL	20Kohm 64.20025.6DL	20Kohm 64.20025.6DL	45Kohm 64.45325.6DL

GPU_ROM_SI

for 1Gbit Hynix VRAM	for 2Gbit Hynix VRAM	for 1Gbit Samsung VRAM	for 2Gbit Samsung VRAM
RAM_CFG[0]=0	RAM_CFG[0]=0	RAM_CFG[0]=1	RAM_CFG[0]=1
RAM_CFG[1]=1	RAM_CFG[1]=1	RAM_CFG[1]=1	RAM_CFG[1]=1
RAM_CFG[2]=0	RAM_CFG[2]=1	RAM_CFG[2]=0	RAM_CFG[2]=1
RAM_CFG[3]=0	RAM_CFG[3]=0	RAM_CFG[3]=0	RAM_CFG[3]=0

GPU_ROM_SO

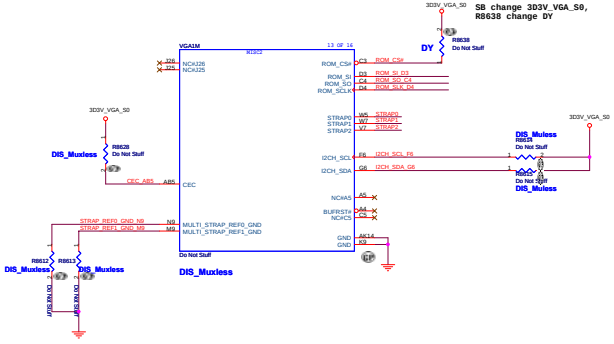
VGA_DEVICE =1 (low bit)
SMB_ALT_ADDR =0
FB_0_BAR_SIZE =0
XCLK_417 =0 (High bit)

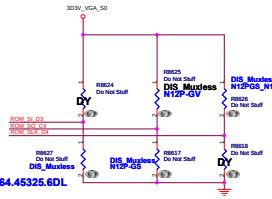
GPU_ROM_SCLK

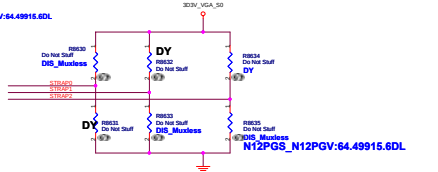
PEX_PLL_EN_TERM =0
SLOT_CLK_CFG =1
SUB_VENDOR =0
PCI_DEVID[4] =1 N11P Fermi QS 1

Logical Strap Bit Mapping

Resistor	Pull-up	Pull-down
5Kohms	1000	0000
10Kohms	1001	0001
15Kohms	1010	0010
20Kohms	1011	0011
25Kohms	1100	0100
30Kohms	1101	0101
35Kohms	1110	0110
45Kohms	1111	0111







Hy2G_64.34825.6DL,Hy1G_64.15025.6DL,Sam1G512M_64.20025.6DL,Sam2G_64.45325.6DL

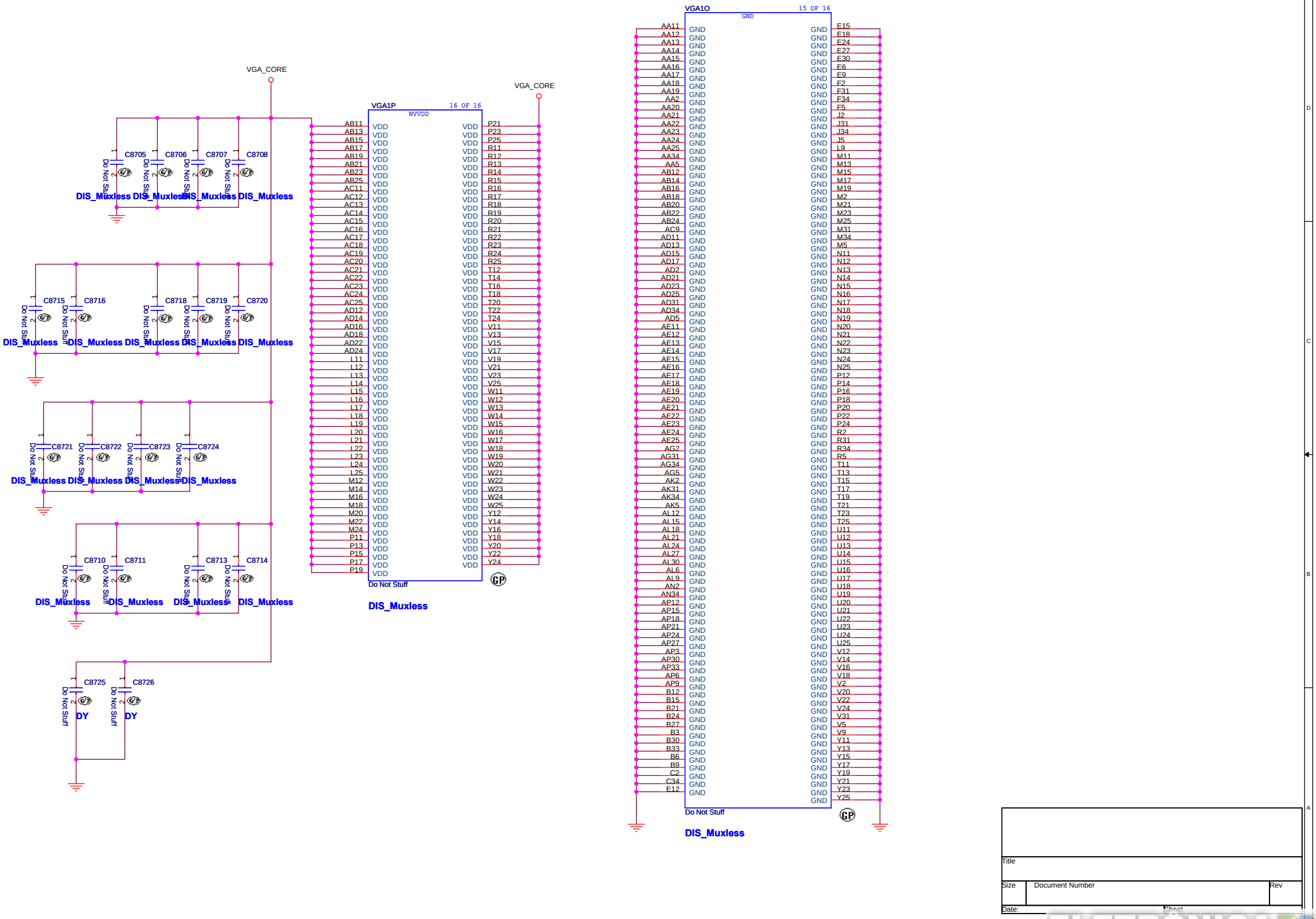
TABLE NVIDIA 71.0N12P.E0U -1 modify N12P GV setting 71.0N12P.A0U

	N12P-GS DEV ID: 0x0DF4	N12P-GV DEV ID: 0x1050	N11P-GE Fermi DEV ID: 0x0DF1 (0001)	N11P-GS Fermi DEV ID: 0x0DF0 (0000)	N12P-GE DEV ID: 0x0DF5 (0101)
STRAP2 PU	25Kohm 64.24925.6DL	45Kohm ES 45K QS 5K 64.49915.6DL	10Kohm 63.10334.1DL	5Kohm 64.49915.6DL	30Kohm 64.30025.6DL

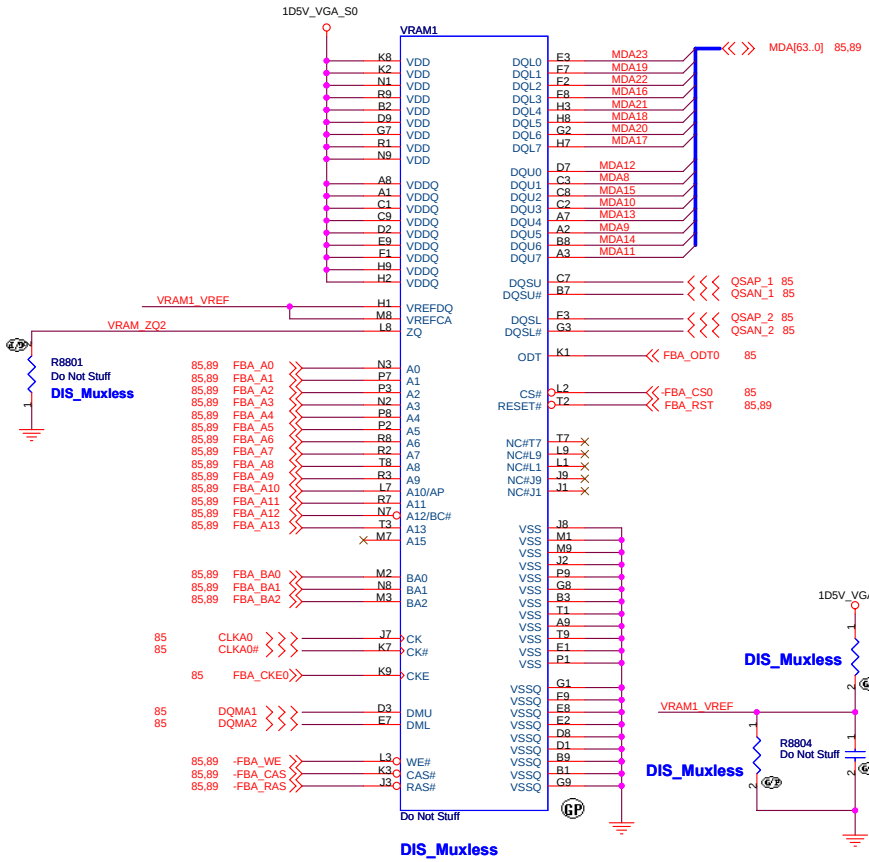
STRAP0 USER[0]=1 USER[1]=1 USER[2]=1 USER[3]=1 — N12P-GS USE 1111 (45K) | N12P-GV | N11P-GE Pull Low | N11P-GS Pull Low | N12P-GE

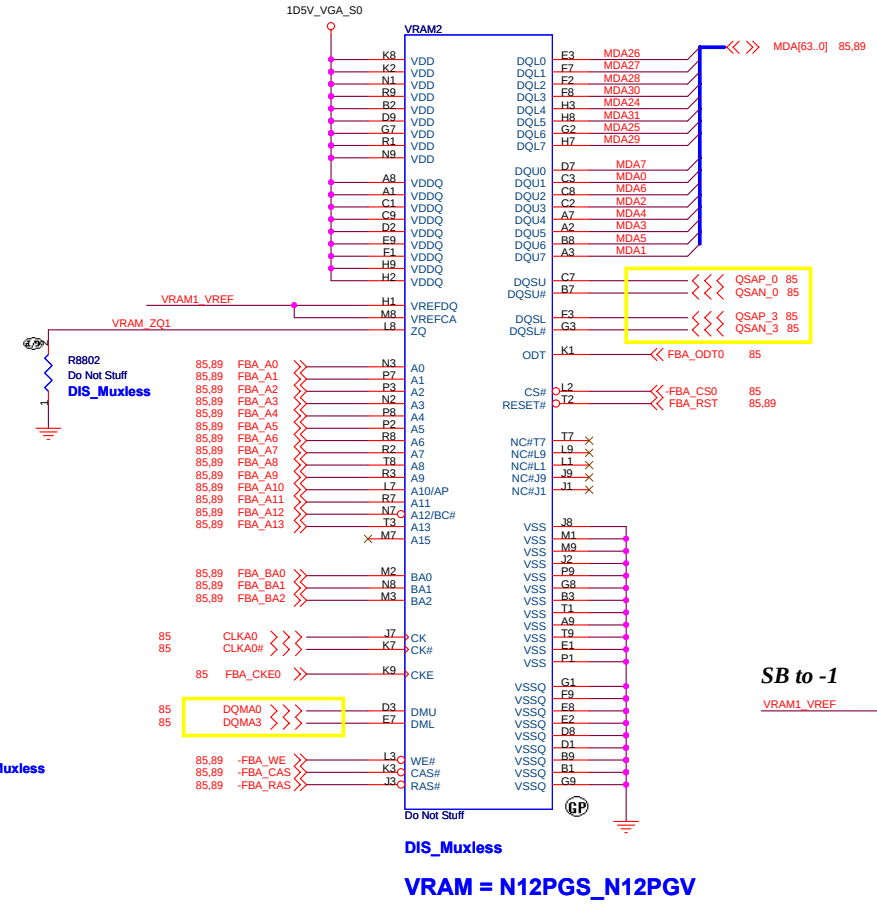
STRAP1 3GIO_PADCFG[0]=0 3GIO_PADCFG[1]=1 3GIO_PADCFG[2]=1 3GIO_PADCFG[3]=1 — USE 0110 (35K)

STRAP2
PCI_DEVID[0]=1 N12P-GS GF108-730-A1 0x0DF4 (0X4) (0100)
PCI_DEVID[1]=0 N12P-GV1 GF108-705-A1 0x0DF7 (0X7) (0111)
PCI_DEVID[2]=0 N11P-GS Fermi 0x0DF0 (0000)
PCI_DEVID[3]=0 N11P-GE Fermi 0x0DF1 (0001)

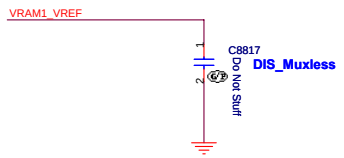


Title		
Size	Document Number	Rev
Date:		Sheet

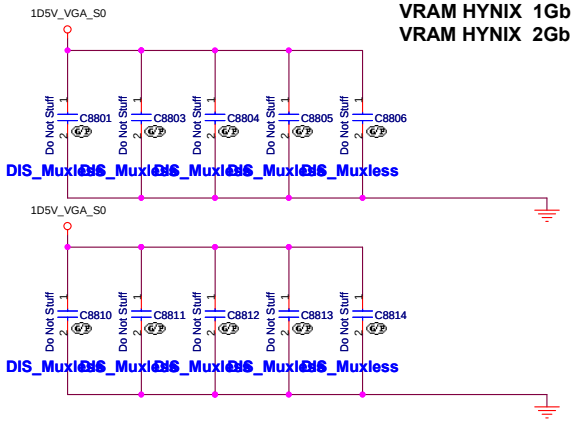


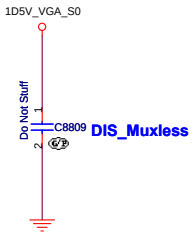


SB to -1

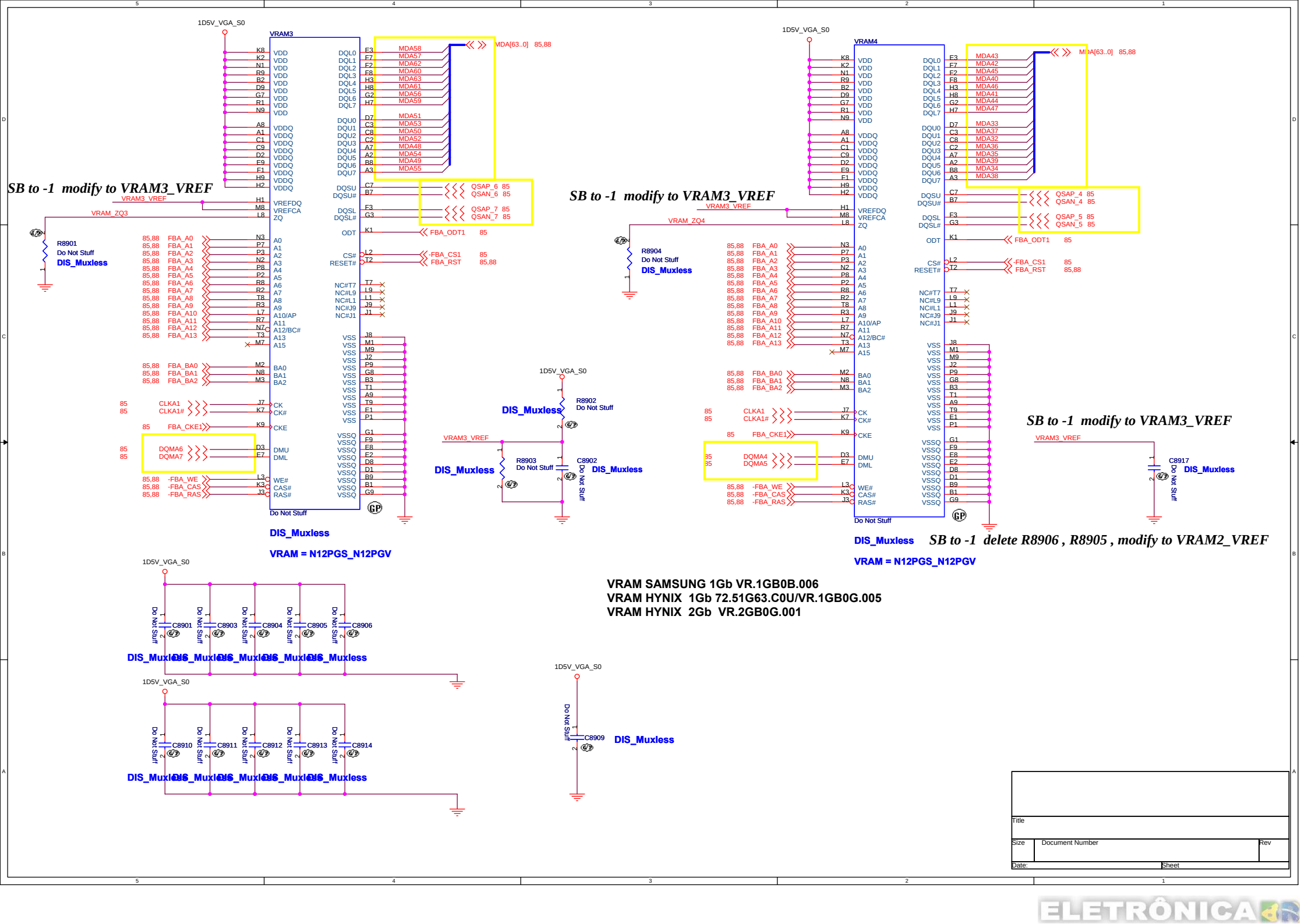


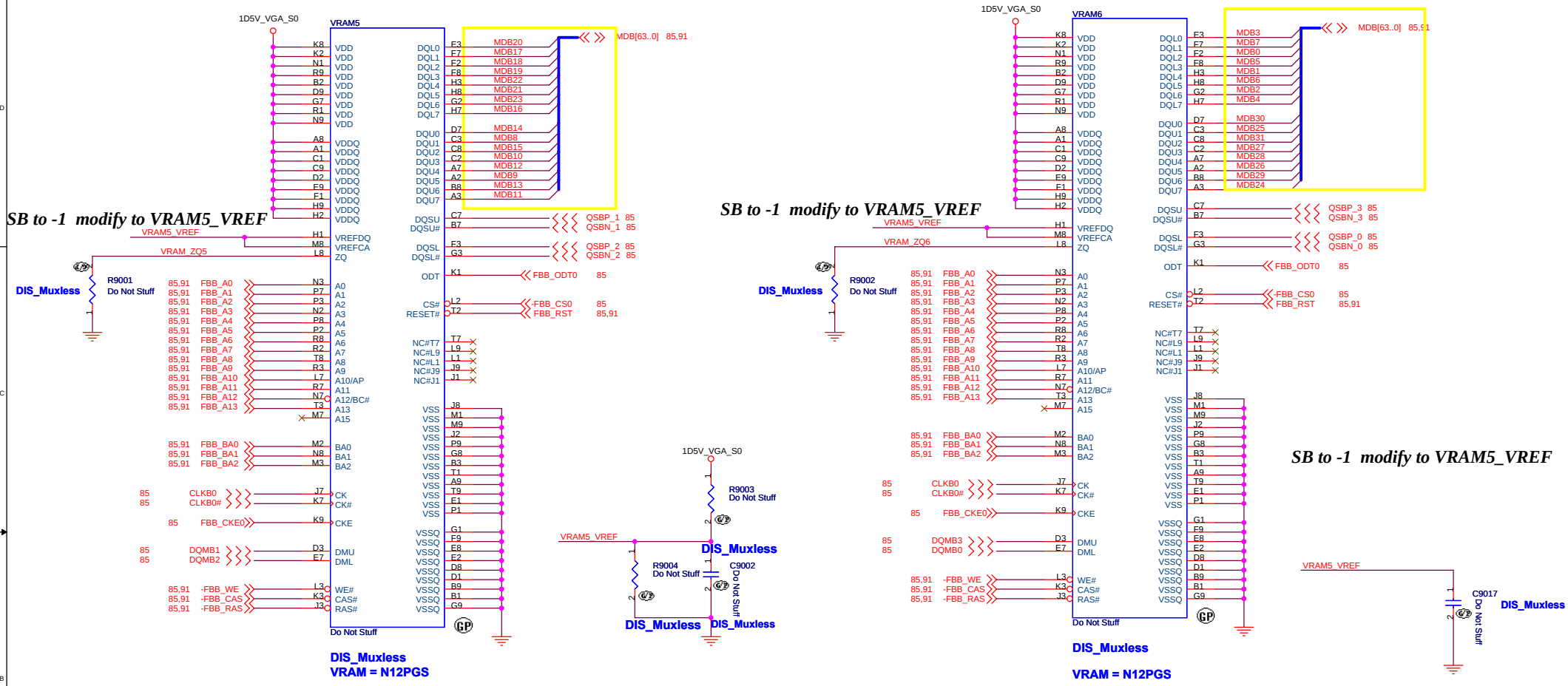
VRAM SAMSUNG 1Gb VR.1GB0B.006
VRAM HYNIX 1Gb 72.51G63.C0U/VR.1GB0G.005
VRAM HYNIX 2Gb VR.2GB0G.001



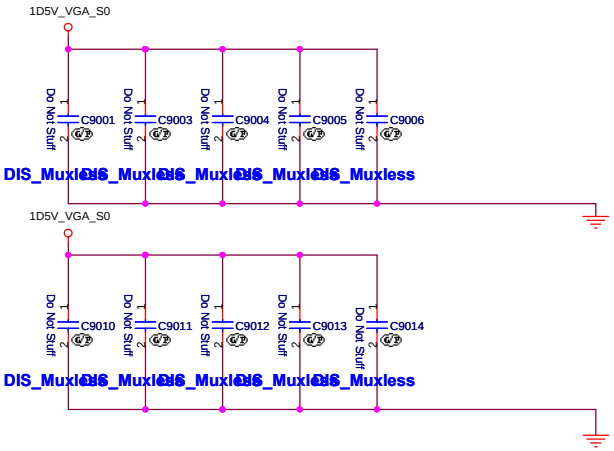


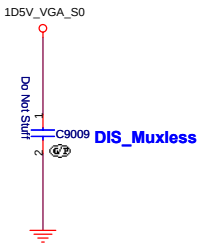
Title		
Size	Document Number	Rev
Date:		Sheet


1D5V_VGA_S0
VRAM3
VRAM4
SB to -1 modify to VRAM3_VREF
SB to -1 modify to VRAM3_VREF
SB to -1 modify to VRAM3_VREF
SB to -1 delete R8906 , R8905 , modify to VRAM2_VREF
R8901 Do Not Stuff DIS_Muxless
R8904 Do Not Stuff DIS_Muxless
R8902 Do Not Stuff DIS_Muxless
R8903 Do Not Stuff DIS_Muxless
C8902 Do Not Stuff DIS_Muxless
C8917 Do Not Stuff DIS_Muxless
C8901 C8903 C8904 C8905 C8906 Do Not Stuff DIS_Muxless
C8910 C8911 C8912 C8913 C8914 Do Not Stuff DIS_Muxless
C8909 Do Not Stuff DIS_Muxless
VRAM3_VREF
VRAM_ZQ3
VRAM_ZQ4
Do Not Stuff
DIS_Muxless
VRAM = N12PGS_N12PGV
VRAM SAMSUNG 1Gb VR.1GB0B.006
VRAM HYNIX 1Gb 72.51G63.C0U/VR.1GB0G.005
VRAM HYNIX 2Gb VR.2GB0G.001
Title
Size
Document Number
Rev
Date:
Sheet

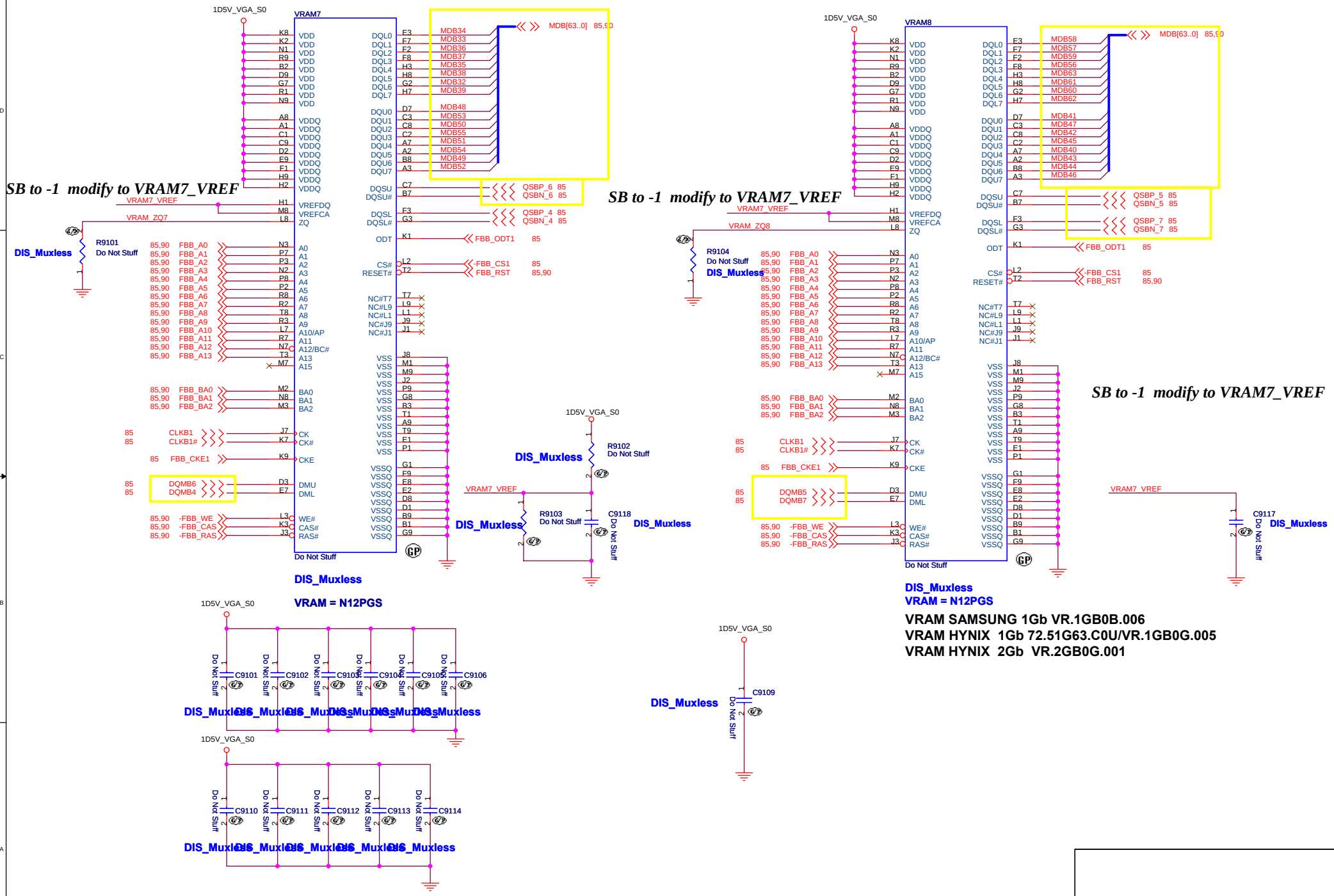


VRAM SAMSUNG 1Gb VR.1GB0B.006
VRAM HYNIX 1Gb 72.51G63.C0U/VR.1GB0G.005
VRAM HYNIX 2Gb VR.2GB0G.001





Title		
Size	Document Number	Rev
Date:		Sheet


1D5V_VGA_S0
VRAM7
MDB[63..0] 85,90
SB to -1 modify to VRAM7_VREF
VRAM7_VREF
VRAM_ZQ7
R9101
Do Not Stuff
DIS_Muxless
QSBP_6 85
QSBN_6 85
QSBP_4 85
QSBN_4 85
FBB_ODT1 85
-FBB_CS1 85
FBB_RST 85,90
FBB_A0
FBB_A1
FBB_A2
FBB_A3
FBB_A4
FBB_A5
FBB_A6
FBB_A7
FBB_A8
FBB_A9
FBB_A10
FBB_A11
FBB_A12
FBB_A13
FBB_BA0
FBB_BA1
FBB_BA2
CLKB1
CLKB1#
FBB_CKE1
DQMB6
DQMB4
-FBB_WE
-FBB_CAS
-FBB_RAS
R9102
Do Not Stuff
R9103
Do Not Stuff
C9118
DIS_Muxless
VRAM = N12PGS
VRAM8
SB to -1 modify to VRAM7_VREF
VRAM7_VREF
VRAM_ZQ8
R9104
Do Not Stuff
DIS_Muxless
QSBP_5 85
QSBN_5 85
QSBP_7 85
QSBN_7 85
FBB_ODT1 85
-FBB_CS1 85
FBB_RST 85,90
DQMB5
DQMB7
C9117
DIS_Muxless
VRAM = N12PGS
VRAM SAMSUNG 1Gb VR.1GB0B.006
VRAM HYNIX 1Gb 72.51G63.C0U/VR.1GB0G.005
VRAM HYNIX 2Gb VR.2GB0G.001
C9101
C9102
C9103
C9104
C9105
C9106
C9109
C9110
C9111
C9112
C9113
C9114
Do Not Stuff
Title
Size
Document Number
Rev
Date:
Sheet

20100715

SSID = PWR.Plane.Regulator_GFX

20100719

SB 20100831

SB 20100831

RT8208A

N12P GS

P-State	PWR_VGA_CORE_D1	PWR_VGA_CORE_D0	VGA_CORE_PWR
P8 , P12	L	L	0.825V
P0 - HOT	L	H	0.975V
P0 - COLD	H	L	1.00V
	H	H	

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 1.5UH PCMC104T-1R5MN Cyntec DCR:4.2mohm Isat =33Arms 68.1R510.10J
O/P cap: 330U 2V EEFSX0D331ER 9mOhm 3Arms Panasonic/ 79.33719.L01
H/S: SI7686DP/ POWERPAK-8/11mOhm/14mOhm@4.5Vgs/ 84.07686.037
L/S: SiR460DP/ POWERPAK-8/ 4.9mOhm/6.1mohm@4.5Vgs/ 84.00460.037

Switching freq-->350KHz

Frequency setting
470K --->165KHz
200K --->323KHz
100K --->500KHz

N12P GV

P-State	PWR_VGA_CORE_D1	PWR_VGA_CORE_D0	VGA_CORE_PWR
P8 , P12	L	L	0.85V
P0 - HOT	L	H	1.00V
P0 - COLD	H	L	1.025V
	H	H	

Vout=0.75V*(R1+R2)/R2

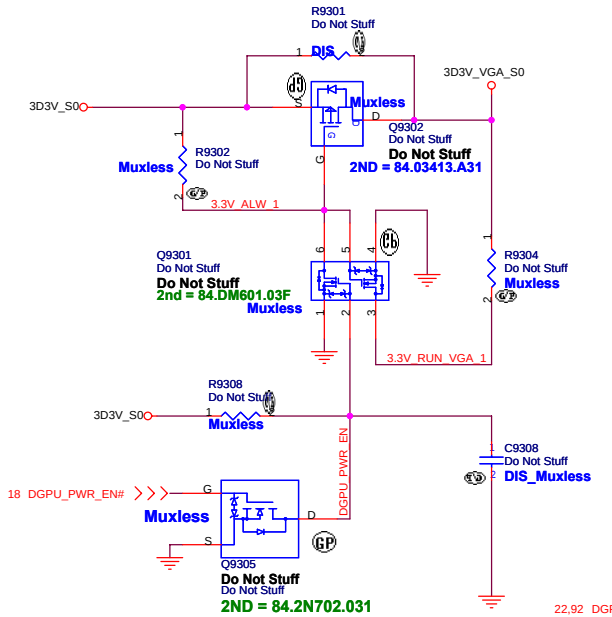
Design Current = 21.94A
24.14A<OCP< 28.53A

Vout=0.75V*(R1+R2)/R2

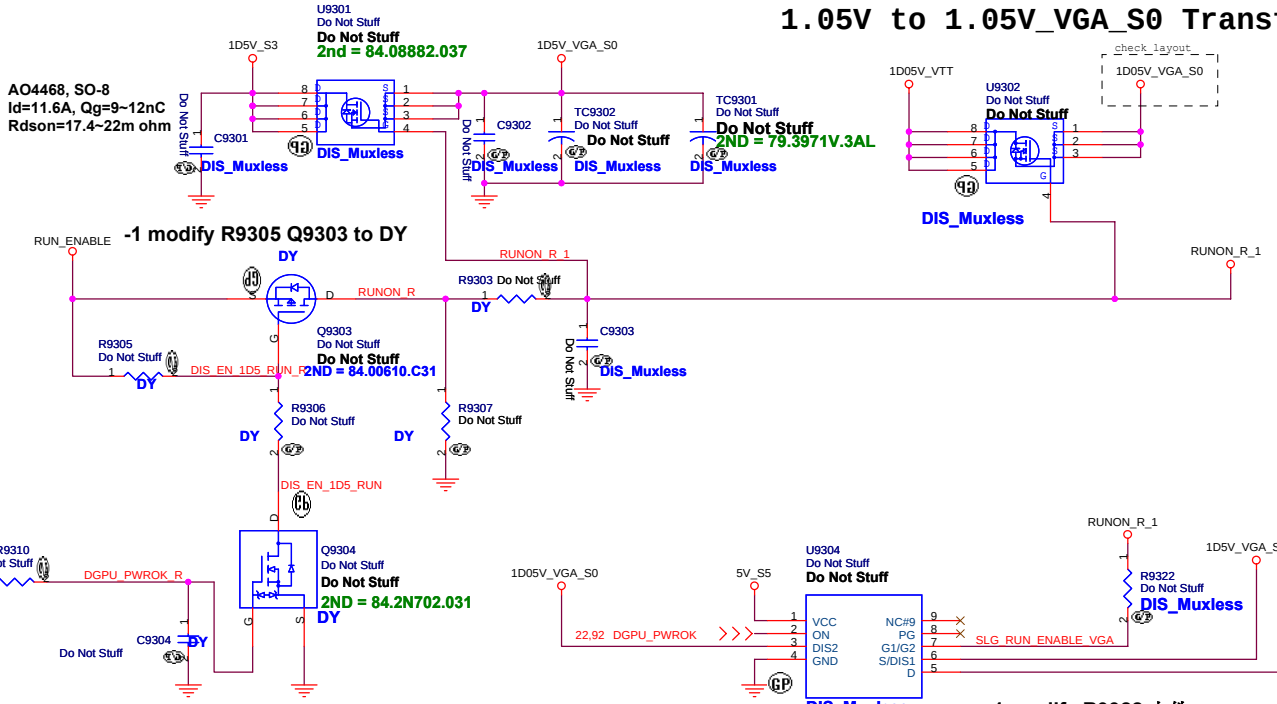
SB to -1 modify PR9213 VGA_Core to 1.05V

Title	
Size	Document Number / Rev
Date:	Sheet

+3VS to 3.3V_DELAY Transfer



1D5V_VGA_S0

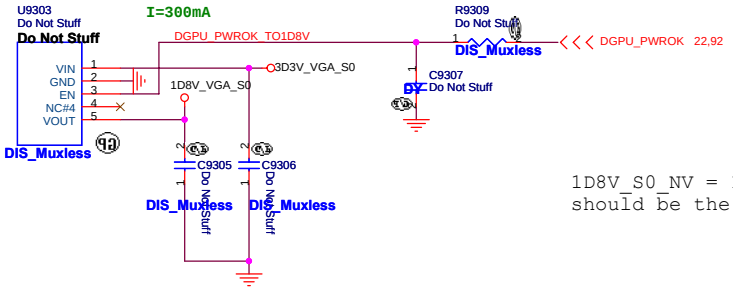


SB modify to 84.03006.A37

1.05V to 1.05V_VGA_S0 Transfer

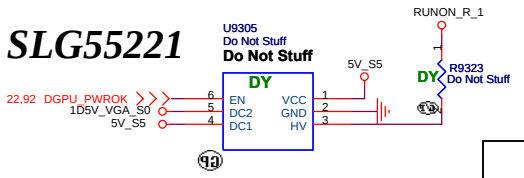
-1 modify R9322 上件

+3VS to 1.8V Transfer

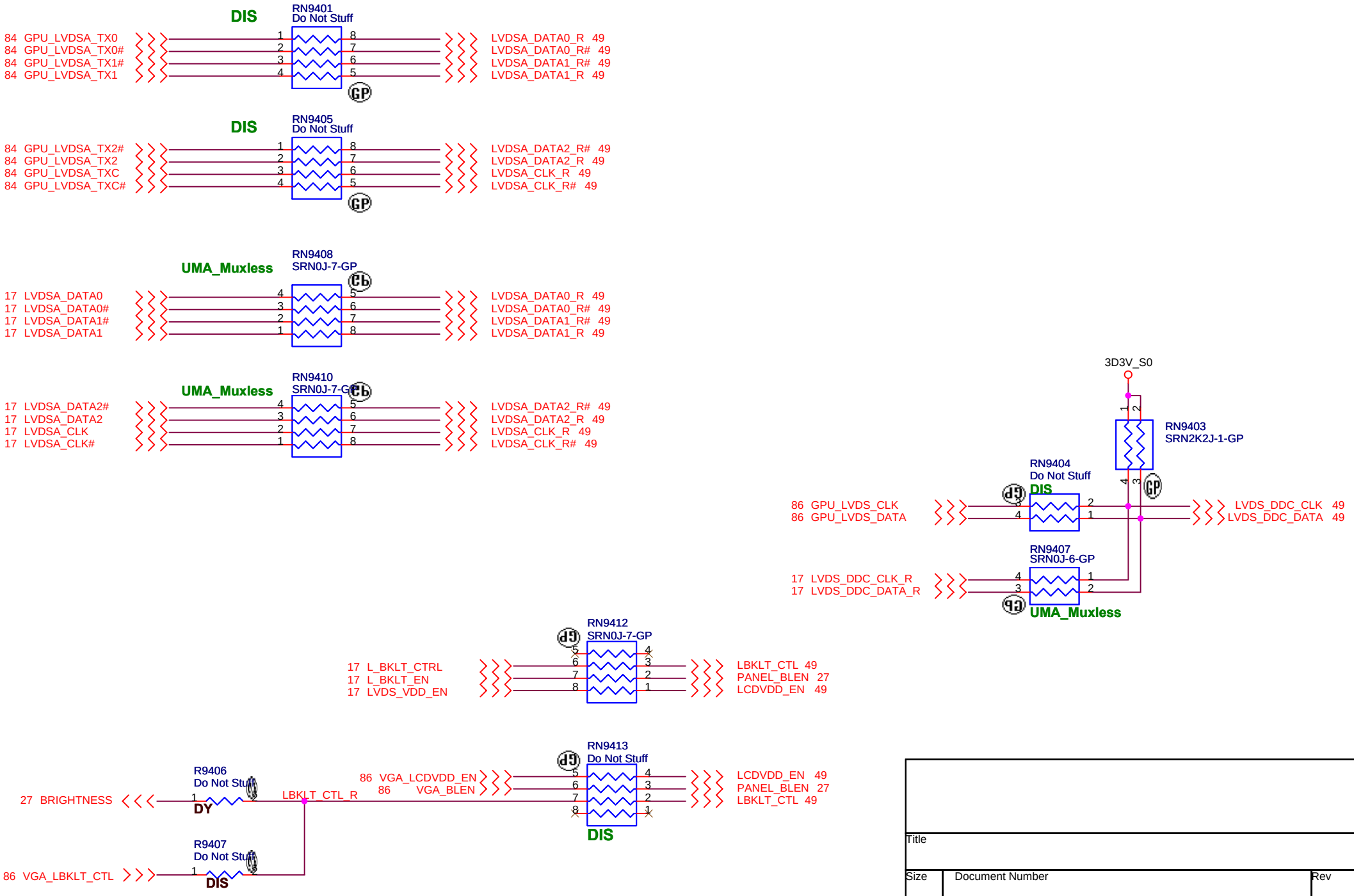


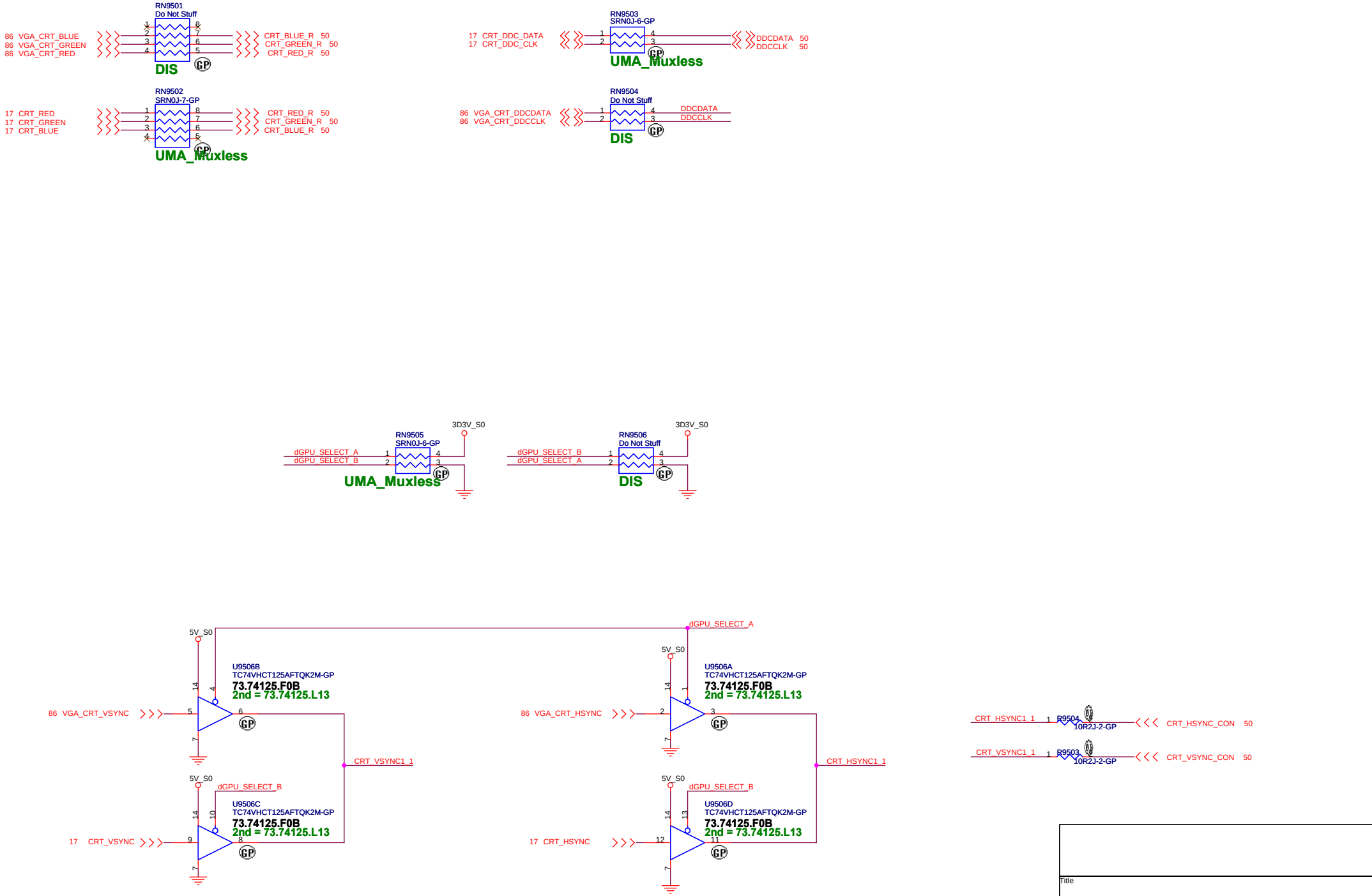
1D8V_S0_NV = IFPA_IOVDD & IFPB_IOVDD, it should be the latest ramp up rail.

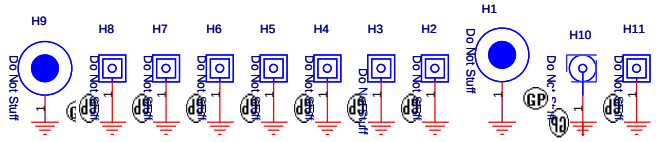
-1 co-layout SLG55221



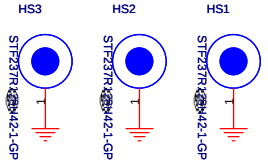
Title		
Size	Document Number	Rev
Date:		Sheet


DIS
RN9401
Do Not Stuff
84 GPU_LVDSA_TX0
84 GPU_LVDSA_TX0#
84 GPU_LVDSA_TX1#
84 GPU_LVDSA_TX1
LVDSA_DATA0_R 49
LVDSA_DATA0_R# 49
LVDSA_DATA1_R# 49
LVDSA_DATA1_R 49
DIS
RN9405
Do Not Stuff
84 GPU_LVDSA_TX2#
84 GPU_LVDSA_TX2
84 GPU_LVDSA_TXC
84 GPU_LVDSA_TXC#
LVDSA_DATA2_R# 49
LVDSA_DATA2_R 49
LVDSA_CLK_R 49
LVDSA_CLK_R# 49
UMA_Muxless
RN9408
SRN0J-7-GP
17 LVDSA_DATA0
17 LVDSA_DATA0#
17 LVDSA_DATA1#
17 LVDSA_DATA1
LVDSA_DATA0_R 49
LVDSA_DATA0_R# 49
LVDSA_DATA1_R# 49
LVDSA_DATA1_R 49
UMA_Muxless
RN9410
SRN0J-7-GP
17 LVDSA_DATA2#
17 LVDSA_DATA2
17 LVDSA_CLK
17 LVDSA_CLK#
LVDSA_DATA2_R# 49
LVDSA_DATA2_R 49
LVDSA_CLK_R 49
LVDSA_CLK_R# 49
3D3V_S0
RN9403
SRN2K2J-1-GP
RN9404
Do Not Stuff
DIS
86 GPU_LVDS_CLK
86 GPU_LVDS_DATA
LVDS_DDC_CLK 49
LVDS_DDC_DATA 49
RN9407
SRN0J-6-GP
17 LVDS_DDC_CLK_R
17 LVDS_DDC_DATA_R
UMA_Muxless
RN9412
SRN0J-7-GP
17 L_BKLT_CTRL
17 L_BKLT_EN
17 LVDS_VDD_EN
LBKLT_CTL 49
PANEL_BLEN 27
LCDVDD_EN 49
RN9413
Do Not Stuff
86 VGA_LCDVDD_EN
86 VGA_BLEN
LCDVDD_EN 49
PANEL_BLEN 27
LBKLT_CTL 49
DIS
R9406
Do Not Stuff
27 BRIGHTNESS
LBKLT_CTL_R
DY
R9407
Do Not Stuff
86 VGA_LBKLT_CTL
DIS
Title
Size
Document Number
Rev
Date:
Sheet

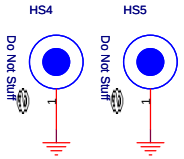

RN9501
Do Not Stuff
86 VGA_CRT_BLUE
86 VGA_CRT_GREEN
86 VGA_CRT_RED
CRT_BLUE_R 50
CRT_GREEN_R 50
CRT_RED_R 50
DIS
RN9503
SRN0J-6-GP
17 CRT_DDC_DATA
17 CRT_DDC_CLK
DDCDATA 50
DDCCLK 50
UMA_Muxless
RN9502
SRN0J-7-GP
17 CRT_RED
17 CRT_GREEN
17 CRT_BLUE
CRT_RED_R 50
CRT_GREEN_R 50
CRT_BLUE_R 50
UMA_Muxless
RN9504
Do Not Stuff
86 VGA_CRT_DDCDATA
86 VGA_CRT_DDCCLK
DDCDATA
DDCCLK
DIS
3D3V_S0
RN9505
SRN0J-6-GP
dGPU_SELECT_A
dGPU_SELECT_B
UMA_Muxless
3D3V_S0
RN9506
Do Not Stuff
dGPU_SELECT_B
dGPU_SELECT_A
DIS
5V_S0
U9506B
TC74VHCT125AFTQK2M-GP
73.74125.F0B
2nd = 73.74125.L13
86 VGA_CRT_VSYNC
CRT_VSYNC1_1
dGPU_SELECT_A
5V_S0
U9506A
TC74VHCT125AFTQK2M-GP
73.74125.F0B
2nd = 73.74125.L13
86 VGA_CRT_HSYNC
CRT_HSYNC1_1
CRT_HSYNC1_1
R9504
10R2J-2-GP
CRT_HSYNC_CON 50
CRT_VSYNC1_1
R9503
10R2J-2-GP
CRT_VSYNC_CON 50
5V_S0
dGPU_SELECT_B
U9506C
TC74VHCT125AFTQK2M-GP
73.74125.F0B
2nd = 73.74125.L13
17 CRT_VSYNC
5V_S0
dGPU_SELECT_B
U9506D
TC74VHCT125AFTQK2M-GP
73.74125.F0B
2nd = 73.74125.L13
17 CRT_HSYNC
Title
Size
Document Number
Rev
Date:
Sheet



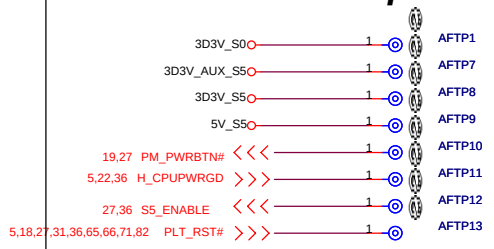
CPU



VGA



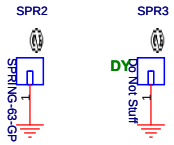
Check test point



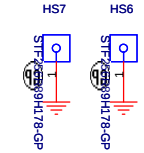
Test Point放在Dimm Door打開可量測處

SB to -1 BOM add SPR2

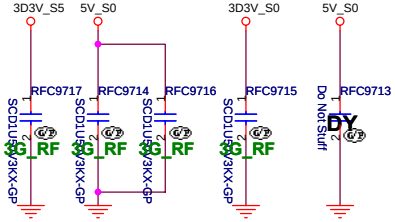
-2 delete SPR5

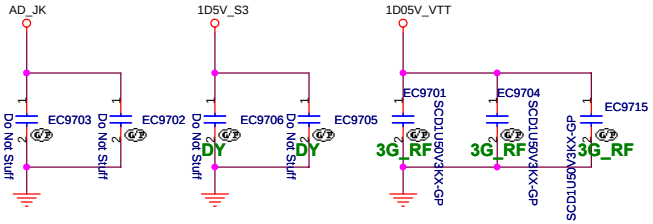


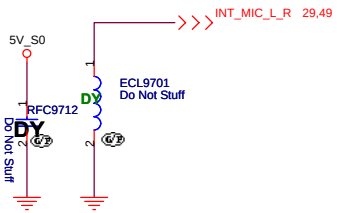
Change:34.40V16.001

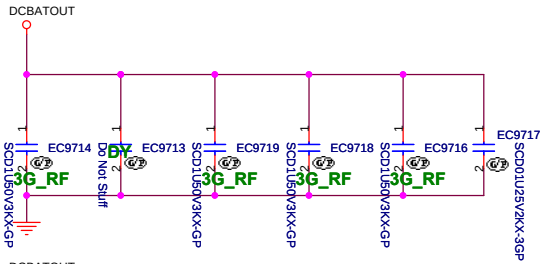


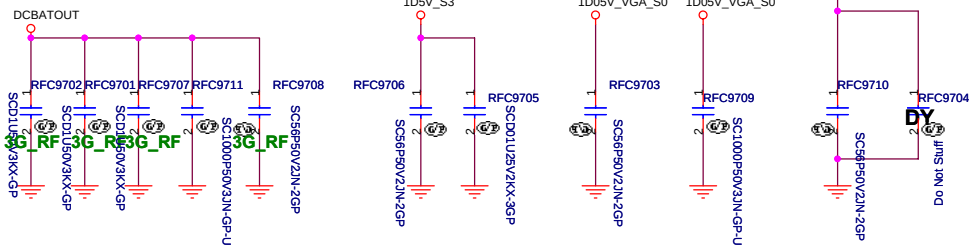
3G Sku

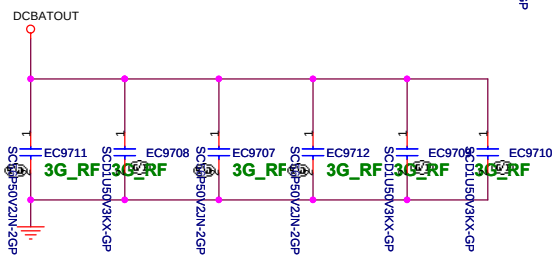




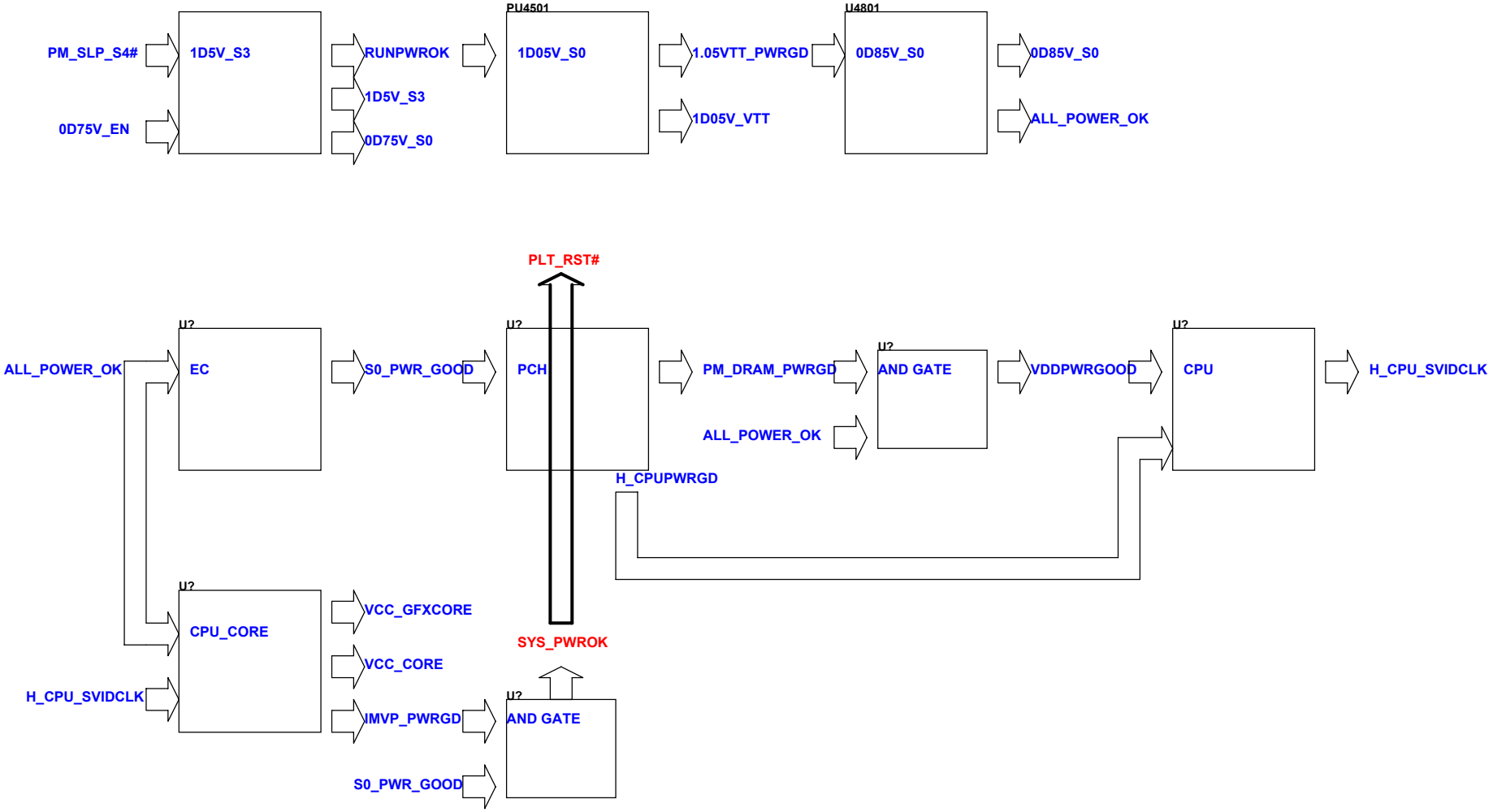








Title		
Size	Document Number	Rev
Date:	Sheet	

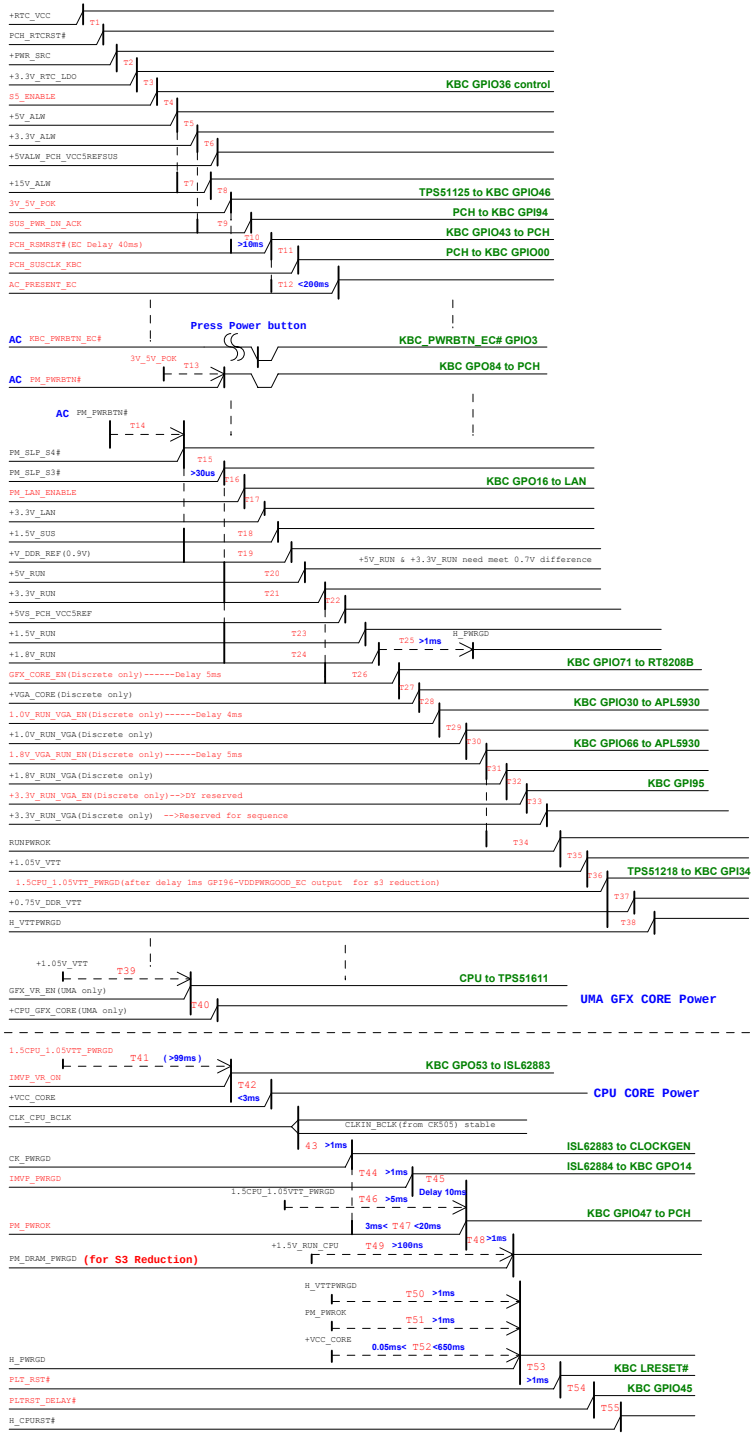


Title		
Size	Document Number	Rev
Date:	Sheet	

Intel-Power Up Sequence

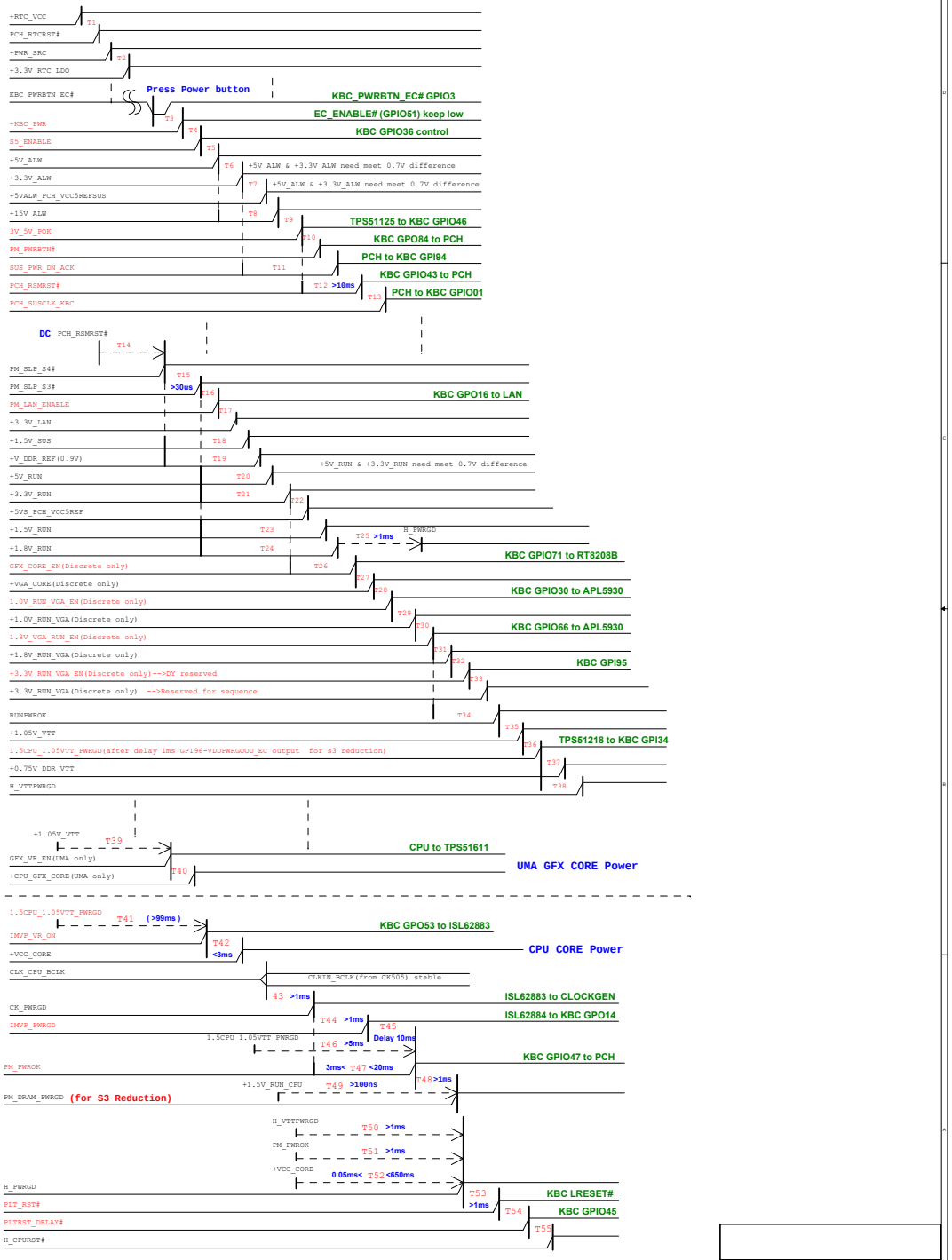
(AC mode)

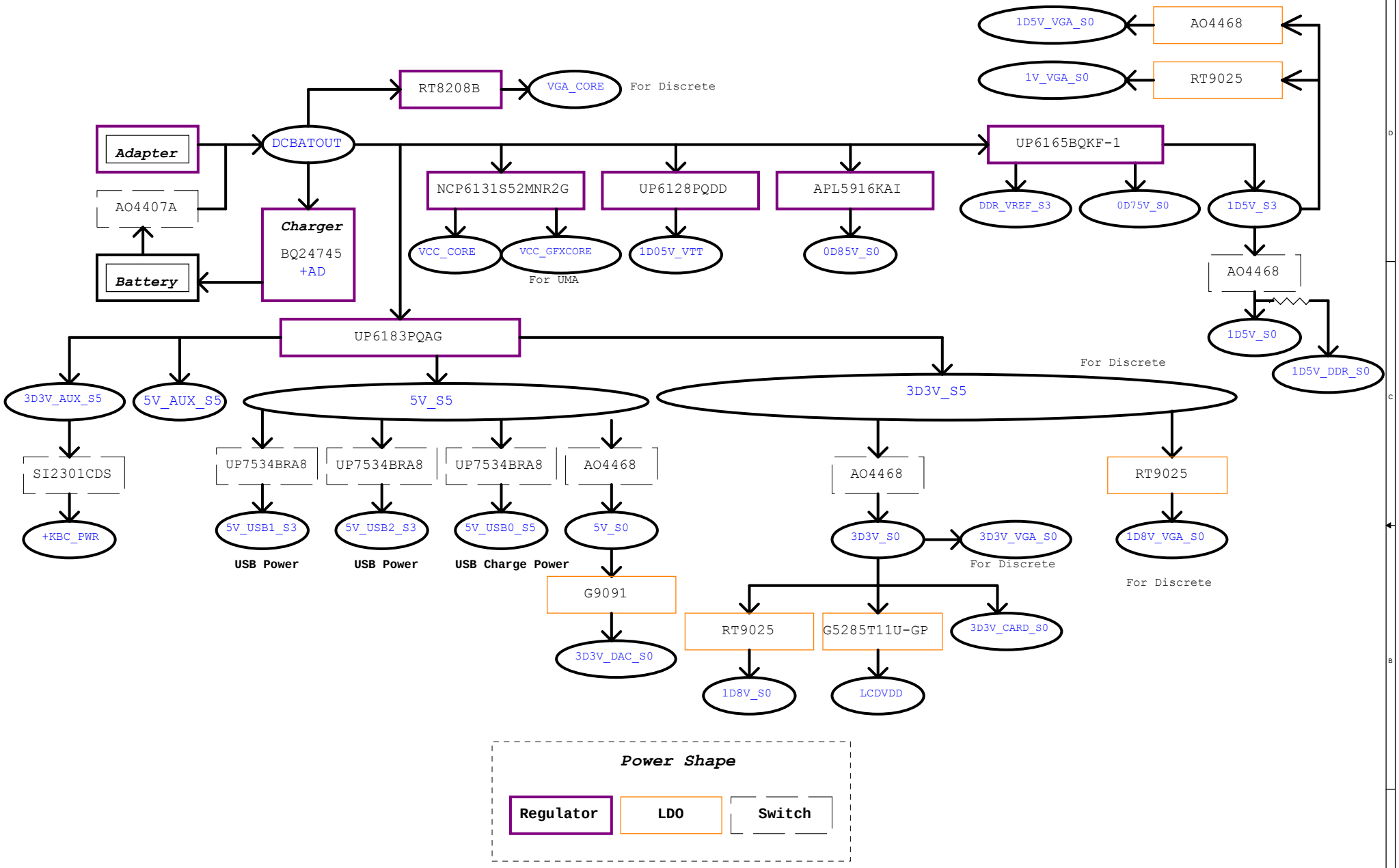
red word: KBC GPIO



(DC mode)

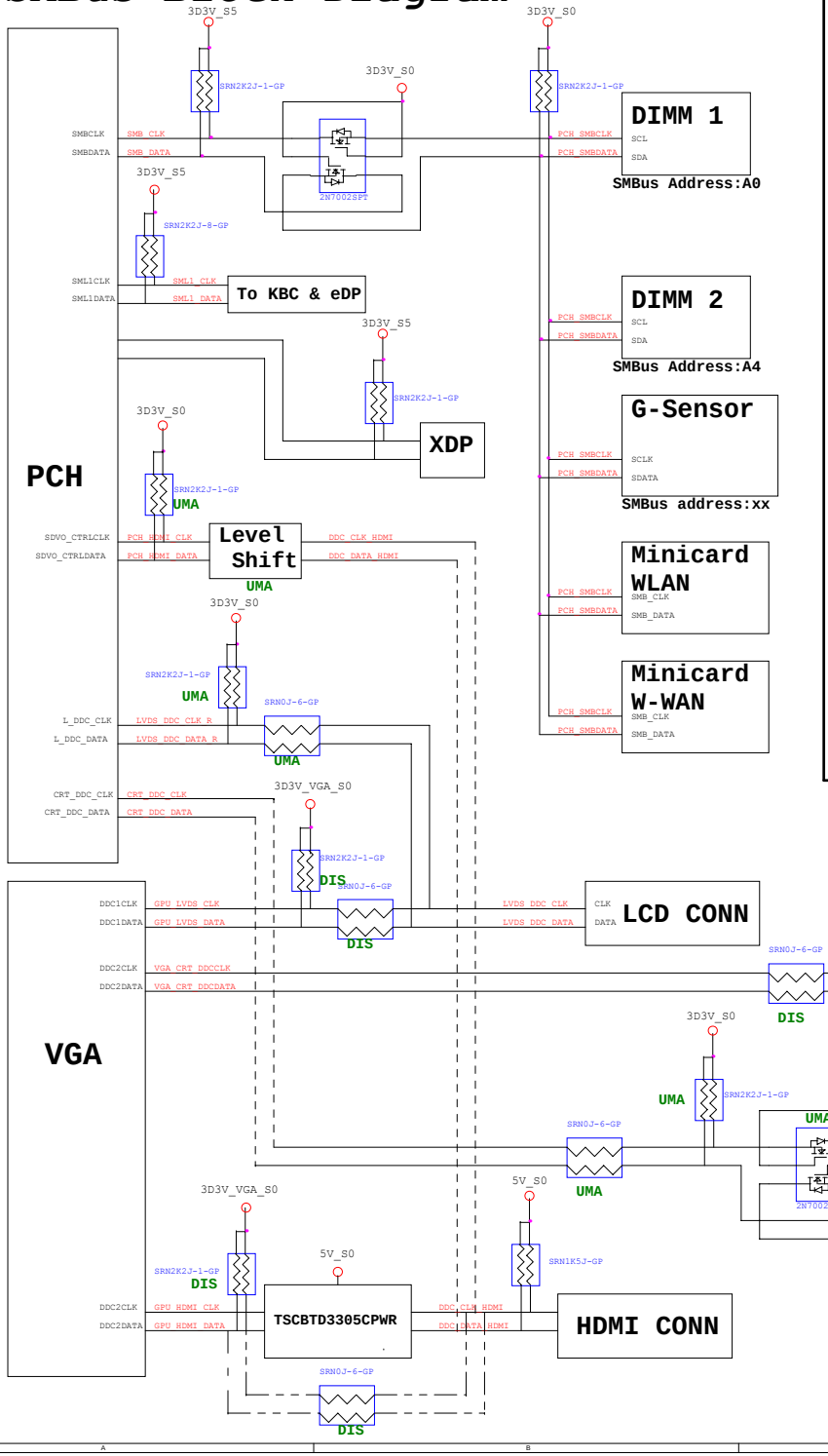
red word: KBC GPIO



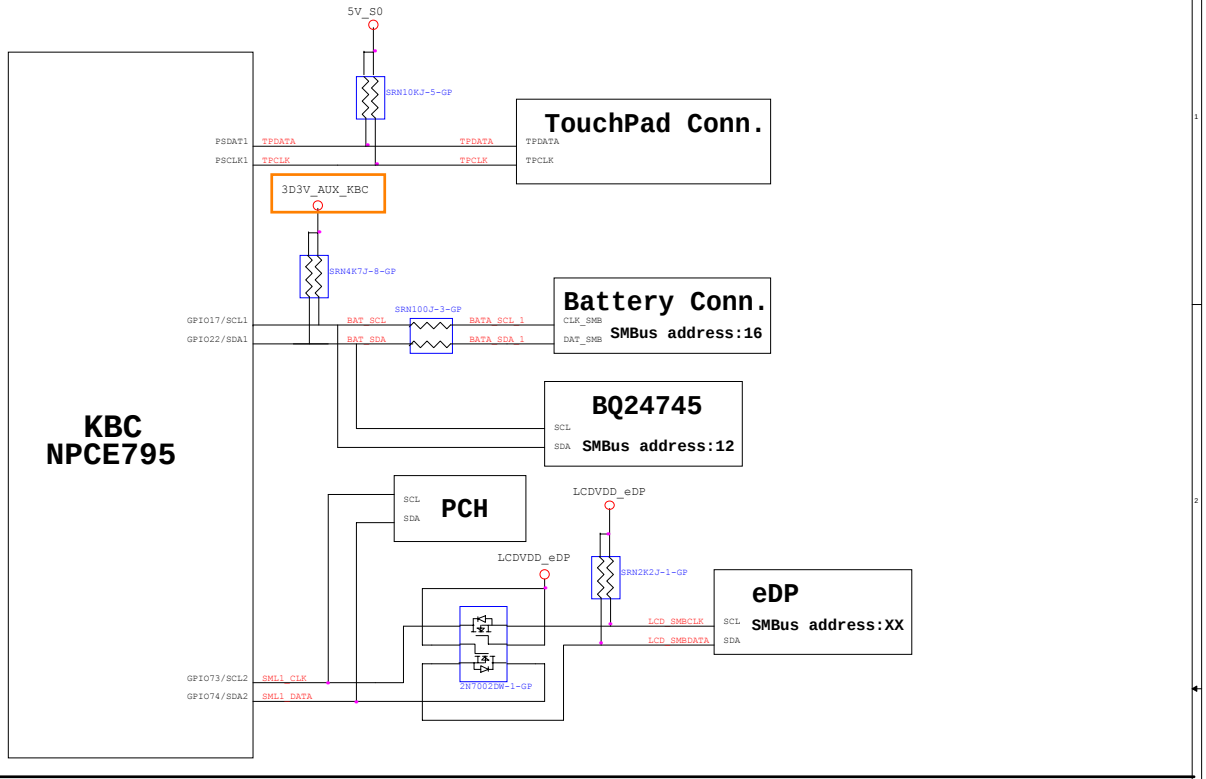


Title		
Size	Document Number	Rev
Date:		Sheet

PCH SMBus Block Diagram

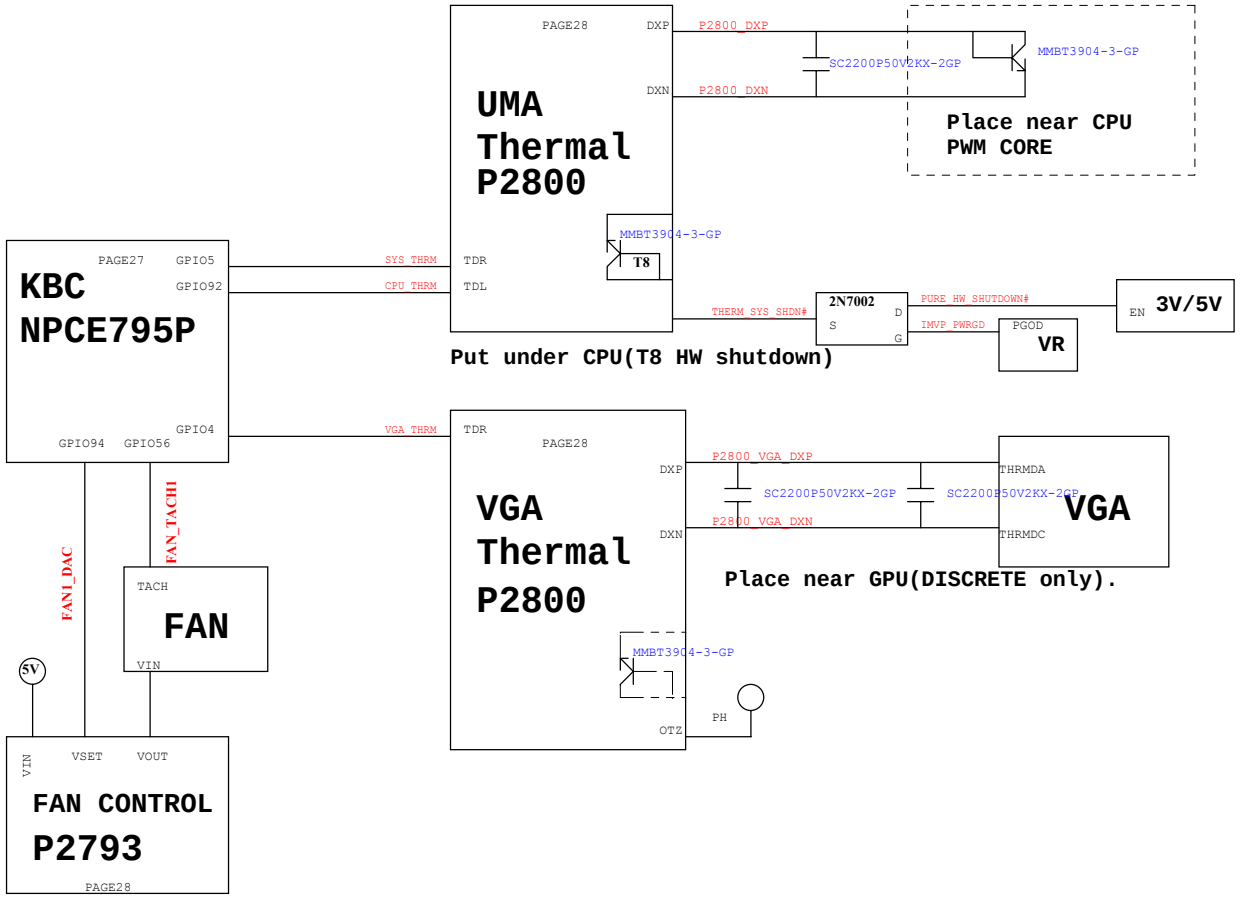


KBC SMBus Block Diagram

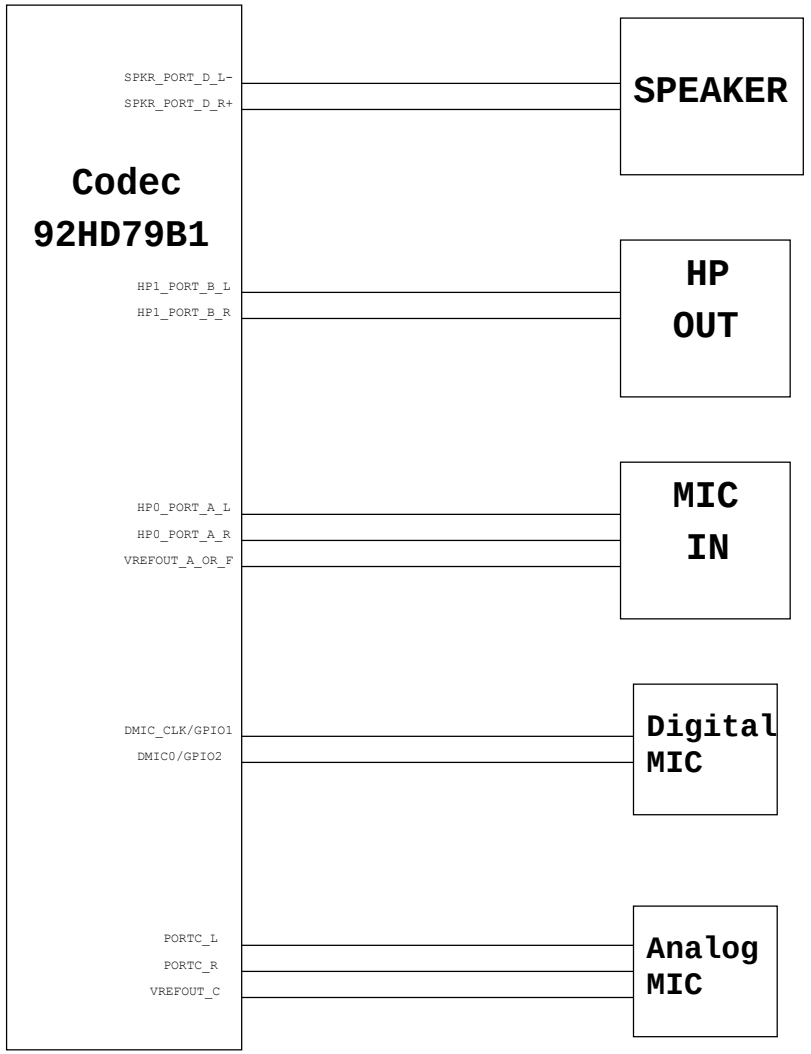


Title		
Size	Document Number	Rev
Date:	Sheet	

Thermal Block Diagram



Audio Block Diagram



Title		
Size	Document Number	Rev
Date:	Sheet	