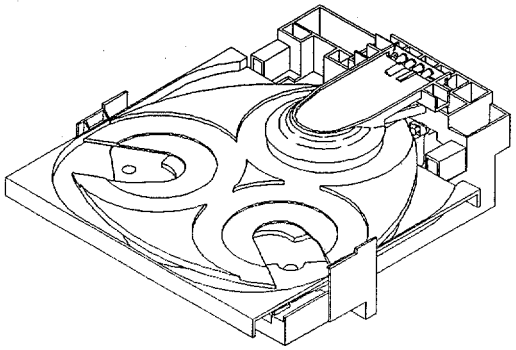
aiwa

aiwa SERVICE

4ZG-1
4ZG-1A
4ZG-1B
4ZG-1Z

SERVICE MANUAL



CD MECHANISM

• BASIC CD MECHANISM: KSM-2 131 BAM
3ZG-2 C1 / 3ZG-2 C2 / 3ZG-2 C5

•TYPE: English

BASIC NAME		DERIVATION NAME							
4ZG-1	*1	–	–	–	–	WR	–	–	–
	*2	G	D	F	R	–	V3L	V4L	V5
4ZG-1A		G	D	–	–	–	–	–	–
4ZG-1B		G	D	–	–	–	–	–	–
4ZG-1Z		–	D	–	–	–	–	–	–

●*1,*2, have the same BASIC NAME but the board structures are different. The CD BLOCK,VCD BLOCK of the WR are shown on the SERVICE MANUAL of each DERIVATION NAME .

●This mechanism has various derivation. Derivation name is indicated by the Service Manual for eath model.

●For different version of mechanism that may be introduced since the issue of this manual, only the new or modified points be discussed.

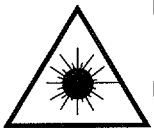
S/M Code No. 09-965-128-10T

TABLE OF CONTENTS

PROTECTION OF EYES FROM LASER BEAM DURING SERVICING

This set employs laser. Therefore, be sure to follow carefully the instructions below when servicing.

WARNING!
WHEN SERVICING, DO NOT APPROACH THE LASER EXIT WITH THE EYE TOO CLOSELY. IN CASE IT IS NECESSARY TO CONFIRM LASER BEAM EMISSION. BE SURE TO OBSERVE FROM A DISTANCE OF MORE THAN 30cm FROM THE SURFACE OF THE OBJECTIVE LENS ON THE OPTICAL PICK-UP BLOCK.



- Caution: Invisible laser radiation when open and interlocks defeated avoid expo-sure to beam.
- Advarsel: Usynlig laserståling ved åbning, når sikkerhedsafbrydere er ude af funktion. Undgå udsættelse for stråling.

VAROITUS!
Laiteen Käyttäminen muulla kuin tässä käyttöohjeessa mainit-ulla tavalla saattaa altistaa käyt-täjän turvallisuusluokan 1 ylit-tävälle näkymättömälle lasersäteilylle.

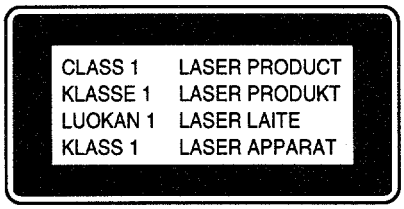
VARNING!
Om apparaten används på annat sätt än vad som specificeras i denna bruksanvising, kan användaren utsättas för osynling laserstrålning, som överskrider gränsen för laserklass 1.

CAUTION
Use of controls or adjustments or performance of procedures other than those specified herein may result in hazardous radi-ation exposure.

ATTENTION
L'utilisation de commandes, réglages ou procédures autres que ceux spécifiés peut entraîner une dangereuse exposition aux radiations.

ADVARSEL!
Usynlig laserståling ved åbning, når sikkerhedsafbrydereer ude af funktion. Undgå udsættelse for stråling.

This Compact Disc player is classified as a CLASS 1 LASER product.
The CLASS 1 LASER PRODUCT label is located on the rear exterior.



This is the SERVICE MANUAL for the BASIC CD MECHANISM of BASIC NAME: 4ZG-1. This BASIC NAME includes the following models as shown under the SUFFIX name: DERIVATION NAME. Please use this manual with the separate SERVICE MANUAL for DERIVATION NAME.

BASIC CD MECHANISM: 4ZG-1 AGD

SUFFIX
(DERIVATION NAME)

BASIC NAME: 4ZG-1 (ORIGINAL MODEL)
4ZG-1A (SONY IC MODEL)
4ZG-1B (TOSHIBA IC MODEL)
4ZG-1Z (SANYO IC MODEL)

BASIC NAME	DERIVATION NAME							
4ZG-1 *1	—	—	—	—	WR	—	—	—
4ZG-1 *2	G	D	F	R	—	V3L	V4L	V5
4ZG-1A	G	D	—	—	—	—	—	—
4ZG-1B	G	D	—	—	—	—	—	—
4ZG-1Z	—	D	—	—	—	—	—	—

NOTE:
- *1 and *2 have the same BASIC NAME but the board structures are different.
- The CD BLOCK, VCD BLOCK of the WR is shown on the SERVICE MANUAL of each DERIVATION NAME.
- Model 4ZG-1 A, B and Z has "F" as the standard installation.

BOARD NAME / BASIC NAME	3CD C.B	LED C.B	T-T C.B	MOTOR C.B	MAIN VCD C.B	CD MECHA C.B	VCD C.B	DRIVE C.B
4ZG-1 *1	—	—	○	—	—	—	—	○
4ZG-1 *2	—	○	○	—	○	○	○ (EXCEPT V5)	—
4ZG-1A	○	○	○	○	—	—	—	—
4ZG-1B	○	○	○	○	—	—	—	—
4ZG-1Z	○	○	○	—	—	—	—	○

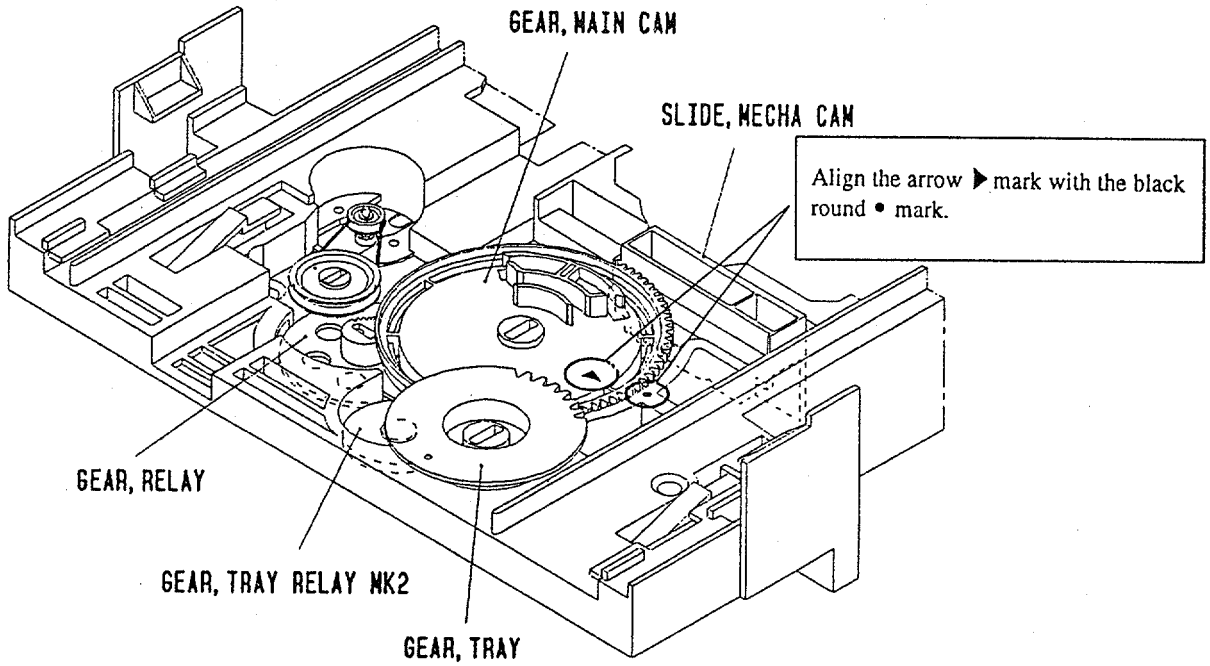
DERIVATION NAME

G: Supporting the CD graphic feature
D: Digital output function
F: CD WINDOW Flash function (LED: AMBER/GREEN)
R: Round Tray
WR: With out Video CD and CD graphic board.
V3L: Supporting the video CD function PAL
V4L: Supporting the video CD function PAL
V5: Supporting the video CD function

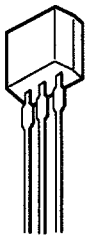
How to Adjust the Rotating Phase of the Gear, Main Cam

1) Push down the hooking catch of the CHAS. MECH, and remove the TRAY.
2) Align the arrow mark of the Gear, Main Cam with the black round mark of the CHAS, MECHA as shown below.
3) Confirm that the Slide, Mech Cam is located in the right position, then insert the TRAY gently.

Caution: If the rotating phase of the Gear, Main Cam is incorrectly adjusted, the chucking operation and tray movement will have malfunction.

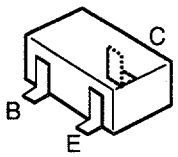


TRANSISTOR ILLUSTRATION



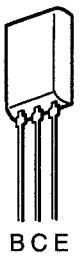
2SA933

2SA1296
2SA1318
2SC1815
2SC2001
2SD655
2SD2172

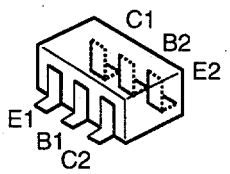


2SA1037
2SA1162
2SA1362
2SA1576
2SC2712
2SC3326
2SC4081
2SD1383

DTA123JK
DTA144TK
DTC114TK
DTC123JK
DTC124XK
DTC143TK
RN1441



2SD2005



HN1C03

4ZG-1

ELECTRICAL MAIN PARTS LIST

DESCRIPTION で判断できない物は “REFERENCE NAME LIST” を参照してください。
If can't understand for Description please kindly refer to “REFERENCE NAME LIST”.

REF. NO.	PART NO.	カンリ NO.	DESCRIPTION
IC			
	SC-L48-000-000		IC,CL480<V3L>
	S4-730-42X-010		IC,HD6473042F16(5EULF6)<V4L>
	SC-XD1-178-Q00		IC,CXD1178Q<V3L>
	SA-T27-C51-2R1		IC,AT27C512R-15JC<V3L>
	SX-D11-86X-010		IC,CXD1186CR(5EUNFC)<V4L>
	SC-008-K81-R10		IC,BR6265AF-10LL(5EUMFS)<V4L>
	ST-C51-425-6BJ		IC,TC514256BJ-70<V3L>
	SC-032-K81-MA0		IC,M5M5256CFP-70LL(5EUMFS)<V4L>
	87-001-948-080		IC,PST572CMT(5EUBFP)<V4L>
	SD-493-07X-010		IC,HD49307(5EUNFH)<V4L>
	SM-C68-MC7-05C		IC,MC68HC705C8ACP<V3L>
	87-002-259-080		IC,uPD6376GS<V3L>
	87-001-607-080		IC,BA4558F<V3L>
	82-NV1-628-080		IC,CXA1645M(5EUBFC)<V3L,V4L>
	SP-D63-210-010		IC,UPD63210GT-E1(5EUNFU)<V4L>
	SS-N74-HCU-04D		IC,SN74HCU04DR<V3L>
	S1-010-XXX-010		IC,UPD61010AGD-LBD(5EULF6)<V4L>
	SC-170-CXX-010		IC,TC170C100AF-001(5EUKFT)<V4L>
	SC-256-KG1-T10		IC,TC514260BJ-70(5EULMD)<V4L>
	SC-000-002-000		IC,TC514260BJ-70(5EULMD)<V4L>
	SL-C29-32X-010		IC,TLC2932IPW(5EUNFT)<V4L>
	87-017-745-019		IC,CXA1782BQ<EXCEPT V5,WR>
	87-002-783-110		IC,CXD2500BQ<EXCEPT WR>
	87-A20-257-049		IC,BA6791FP<V5>
	87-070-120-049		IC,BA6897 FP<EXCEPT V5,WR>
	87-070-429-019		IC,NJM2244L<EXCEPT V5,WR>
	87-002-532-019		IC,PQ05RF11<V5>
	87-017-825-019		IC,GP1F32T<D,V5>
	87-001-873-019		IC,LB1644<V5>
	84-ZG1-639-010		C-IC,MB89627<V5>
	ST-C74-HC2-570		IC,TC74HC257<V3L>
	83-NFT-618-010		IC,UPD78044BGF<V3L>
	85-MAR-614-010		IC,UPD78044BGF-025<V4L>
	87-070-430-019		IC,LA6530<EXCEPT V5,WR>
	87-017-543-089		IC,PST 600D<V5>
	87-A20-255-049		C-IC,SN74LV373NS<V5>
	87-A20-251-049		C-IC,BR6265BF-N10SL<V5>
	87-A20-252-049		C-IC,SN74LV00NS<V5>
	87-A20-253-049		C-IC,SN74LV04NS<V5>
	87-A20-254-049		C-IC,SN74LV32NS<V5>
	87-A20-244-010		C-IC,CL484<V5>
	87-020-881-089		IC,NJM78L05A<EXCEPT V5,WR>
	87-A20-200-040		C-IC,HM514260CJ7/CLJ7<V5>
	87-017-888-089		IC,NJM4558MD<V4L>
	84-ZG1-640-049		C-IC,LH5317<V5>
	87-A20-256-049		C-IC,PQ20VZ5U<V5>
	87-A20-247-019		C-IC,BU1417AK<V5>
	87-017-802-010		IC,LC7872E<G>
	87-A20-248-049		C-IC,BU2173F<V5>
	87-017-803-010		IC,LC32464P-80<G>
	87-A20-258-040		C-IC,SM5877AM<V5>
TRANSISTOR			
	SC-408-1XX-010		TR,2SC4081(5EQQ2S)<V4L>
	S1-441-XXX-010		TR,RN1441-A(5EQQRN)<V4L>
	SA-157-6XX-010		TR,2SA1576(5EQQ2S)<V4L>
	89-111-625-089		C-TR,2SA1162GR<EXCEPT V5,WR>
	87-026-237-089		C-TR,DTC124XK<EXCEPT WR>
	87-327-125-089		C-TR,2SC2712 GR<V5>
	89-113-625-089		C-TR 2SA 1362 GR(TAPG)<V5>
	89-327-125-089		C-TR,2SC2712GR<EXCEPT WR>
	89-112-965-089		TR,2SA1296GR<EXCEPT WR>
	87-026-608-089		C-TR,DTC 123 JK<F>
	89-324-585-010		TR,2SC2458<V3L>
	89-333-266-089		C-TR,2SC3326B<EXCEPT V5,WR>
	87-026-580-089		C-TR,DTA123JK<EXCEPT WR>
	87-026-470-089		TR,HN1C03 F B<V5>
	89-318-155-089		TR,2SC1815 GR<V5>
DIODE			
	S0-041-480-000		DIODE,1N4148<V3L>
	S1-305-700-283		DIODE,DA115(5EDQDD)<V4L>
	S0-240-010-000		DIODE,1N4001<V3L>
	SA-P20-2UX-010		DIODE,DAP202U(5EDQDD)<V4L>
	87-002-608-089		DIODE,DSF10TC<V4L>
	87-017-430-090		DIODE,RK14<V3L>
	87-020-465-089		DIODE,ISS133<EXCEPT V5,WR>
	SM-TZ2-7B0-000		ZENER,MTZ2.7B<V3L>
	87-020-027-089		C-DIODE 1SS184<V5>
	87-A40-180-049		C-DIODE SB07-015 C<V5>
	87-A40-196-089		C-ZENER UDZ6.2 B<V5>
MAIN VCD C.B<V3L,V4L>			
C101	87-012-140-089		C-CAP,S 470P-50 CH<EXCEPT WR>
C102	87-010-194-089		C-CAP,S 0.047-25 F
C103	87-010-178-089		C-CAP,S 1000P-50 B
C104	87-012-156-089		C-CAP,S 220P-50 CH
C105	87-010-384-089		CAP,E 100-25 SME
C106	87-010-196-089		C-CAP,S 0.1-25 F
C107	87-010-314-089		C-CAP,S 22P-50 CH
C108	87-010-314-089		C-CAP,S 22P-50 CH
C110	87-010-221-089		CAP,E 470-10 11L
C111	87-010-320-089		C-CAP,S 68P-50 CH
C112	87-010-196-089		C-CAP,S 0.1-25 F<V4L>
C112	87-016-463-089		C-CAP,S 0.33-16 B<V3L>
C113	87-010-260-089		CAP,E 47-25 SME
C114	87-010-498-049		CAP,E 10-16 GAS
C115	87-010-498-049		CAP,E 10-16 GAS<G>
C116	87-010-196-089		C-CAP,S 0.1-25 F
C117	87-010-197-089		C-CAP,S 0.01-25 B
C118	87-010-553-049		CAP,E 47-16 GAS<V4L>
C119	87-010-553-049		CAP,E 47-16 GAS
C120	87-010-197-089		C-CAP,S 0.01-25 B
C121	87-010-384-089		CAP,E 100-25 SME<V4L>
C122	87-010-320-089		C-CAP,S 68P-50 CH<D>
C123	87-010-401-089		CAP,E 1-50 SME
C124	87-A10-011-019		CAP,E 2200-25 SMG
C125	87-010-322-089		C-CAP,S 100P-50 CH
C126	87-010-178-089		C-CAP,S 1000P-50 B
C127	87-010-314-089		C-CAP,S 22P-50 CH<G>
C128	87-010-320-089		C-CAP,S 68P-50 CH
C129	87-010-263-089		CAP,E 100-10 SME<D>
C130	87-010-197-089		C-CAP,S 0.01-25 B<D>
C131	87-010-197-089		C-CAP,S 0.01-25 B
C132	87-010-196-089		C-CAP,S 0.1-25 F
C133	87-010-196-089		C-CAP,S 0.1-25 F
C134	87-010-196-089		C-CAP,S 0.1-25 F
C135	87-010-196-089		C-CAP,S 0.1-25 F
C136	87-010-154-089		C-CAP,S 10P-50 CH<V4L>
C201	87-010-382-089		CAP,E 22-25 SME
C202	87-010-197-089		C-CAP,S 0.01-25 B

REF. NO.	PART NO.	カンリ NO.	DESCRIPTION
C203	87-010-382-089		CAP,E 22-25 SME
C204	87-010-381-089		CAP,E 330-16 SME
C205	87-010-196-089		C-CAP,S 0.1-25 F
C206	87-010-196-089		C-CAP,S 0.1-25 F
C207	87-010-498-049		CAP,E 10-16 GAS<F>
C208	87-010-405-089		CAP,E 10-50 SME
C301	87-010-197-089		C-CAP,S 0.01-25 B
C306	87-010-381-089		CAP,E 330-16 SME<V4L>
C307	87-010-553-049		CAP,E 47-16 GAS
C308	87-010-498-049		CAP,E 10-16 GAS
C309	87-010-404-089		CAP,E 4.7-50 SME<V4L>
C310	87-010-404-089		CAP,E 4.7-50 SME<V4L>
C311	87-012-140-089		C-CAP,S 470P-50 CH<V4L>
C312	87-012-140-089		C-CAP,S 470P-50 CH<V4L>
C313	87-010-384-089		CAP,E 100-25 SME<V4L>
C315	87-010-404-089		CAP,E 4.7-50 SME<V4L>
C316	87-010-404-089		CAP,E 4.7-50 SME<V4L>
C317	87-010-197-089		C-CAP,S 0.01-25 B
C318	87-010-197-089		C-CAP,S 0.01-25 B
C401	87-010-405-089		CAP,E 10-50 SME<G>
C402	87-010-314-089		C-CAP,S 22P-50 CH<G>
C403	87-010-315-089		C-CAP,S 27P-50 CH<G>
C406	87-010-384-089		CAP,E 100-25 SME<G>
C407	87-010-384-089		CAP,E 100-25 SME<G>
C408	87-010-196-089		C-CAP,S 0.1-25 F<G>
C409	87-010-196-089		C-CAP,S 0.1-25 F<G>
CON6	83-NFT-628-019		CONN ASSY,8P<V3L>
EM101	87-008-474-089		F-BEAD,EMI BL02RN1
EM102	87-008-474-089		F-BEAD,EMI BL02RN1
FC1	85-NFT-612-019		FF-CABLE,30P-1.0<V4L>
FC2	88-912-131-219		FF-CABLE,12P 1.25
FC3	85-MAR-617-019		FF-CABLE,6P-1.25
J101	87-009-502-019		JACK,PIN 1PY EARTH
L101	87-003-149-089		COIL,47UH
L102	87-003-149-089		COIL,47UH
L103	87-003-143-089		COIL,4.7UH
L401	87-003-149-089		COIL,47UH<G>
L402	87-003-149-089		COIL,47UH<G>
M401	87-045-305-019		MOTOR, RF-500TB
PR101	87-026-689-089		PROTECTOR,1A 60V 491
SW201	87-036-109-019		SW,PUSH SPPB 61
SW202	87-036-109-019		SW,PUSH SPPB 61
X101	87-030-270-089		VIB,XTAL 16.9344MHZ
X201	89-MX1-704-089		CERA LOCK(MU)3.9MHZ
X401	80-JUC-602-089		VIB,XTAL 17.73MHZ<G>

MAIN VCD C.B<V5>

REF. NO.	PART NO.	カンリ NO.	DESCRIPTION
C101	87-010-197-089		C-CAP,S 0.01-25 B
C102	87-010-550-049		CAP,E 100-6.3 GAS
C103	87-010-318-089		C-CAP,S 47P-50 CH
C104	87-010-197-089		C-CAP,S 0.01-25 B
C105	87-010-318-089		C-CAP,S 47P-50 CH
C106	87-010-549-049		CAP,E 47-6.3 GAS
C107	87-012-156-089		C-CAP,S 220P-50 CH
C108	87-010-184-089		C-CAP,S 3300P-50 B
C109	87-010-194-089		C-CAP,S 0.047-25 F
C110	87-012-140-089		C-CAP,S 470P-50 CH
C111	87-010-197-089		C-CAP,S 0.01-25 B
C112	87-016-461-089		C-CAP,S 0.47-16 F
C113	87-010-196-089		C-CAP,S 0.1-25 F
C114	87-010-550-049		CAP,E 100-6.3 GAS
C115	87-010-197-089		C-CAP,S 0.01-25 B
C116	87-010-561-049		CAP,E 100-16 GAS
C117	87-010-562-049		CAP,E 220-10 GAS
C118	87-010-553-049		CAP,E 47-16 GAS
C119	87-010-197-089		C-CAP,S 0.01-25 B
C120	87-010-555-089		CAP,E 100-10 GAS
C121	87-010-197-089		C-CAP,S 0.01-25 B
C201	87-010-499-049		CAP,E 22-6.3 GAS
C202	87-010-197-089		C-CAP,S 0.01-25 B
C203	87-010-196-089		C-CAP,S 0.1-25 F
C204	87-010-316-089		C-CAP,S 33P-50 CH
C205	87-010-316-089		C-CAP,S 33P-50 CH
C206	87-010-499-049		CAP,E 22-6.3 GAS
C207	87-010-197-089		C-CAP,S 0.01-25 B
C208	87-010-197-089		C-CAP,S 0.01-25 B
C209	87-010-197-089		C-CAP,S 0.01-25 B
C210	87-010-197-089		C-CAP,S 0.01-25 B
C211	87-010-197-089		C-CAP,S 0.01-25 B
C212	87-010-318-089		C-CAP,S 47P-50 CH
C301	87-010-549-049		CAP,E 47-6.3 GAS
C302	87-010-549-049		CAP,E 47-6.3 GAS
C304	87-010-197-089		C-CAP,S 0.01-25 B
C305	87-010-197-089		C-CAP,S 0.01-25 B
C306	87-010-197-089		C-CAP,S 0.01-25 B
C307	87-010-197-089		C-CAP,S 0.01-25 B
C308	87-010-197-089		C-CAP,S 0.01-25 B
C309	87-010-197-089		C-CAP,S 0.01-25 B
C310	87-010-197-089		C-CAP,S 0.01-25 B
C311	87-010-197-089		C-CAP,S 0.01-25 B
C312	87-010-197-089		C-CAP,S 0.01-25 B
C313	87-010-318-089		C-CAP,S 47P-50 CH
C314	87-010-196-089		C-CAP,S 0.1-25 F
C315	87-010-196-089		C-CAP,S 0.1-25 F
C316	87-010-549-049		CAP,E 47-6.3 GAS
C317	87-010-314-089		C-CAP,S 22P-50 CH
C319	87-010-314-089		C-CAP,S 22P-50 CH
C320	87-010-196-089		C-CAP,S 0.1-25 F
C321	87-010-550-049		CAP,E 100-6.3 GAS
C322	87-010-197-089		C-CAP,S 0.01-25 B
C323	87-010-550-049		CAP,E 100-6.3 GAS
C324	87-010-197-089		C-CAP,S 0.01-25 B
C401	87-010-197-089		C-CAP,S 0.01-25 B
C402	87-010-550-049		CAP,E 100-6.3 GAS
C403	87-010-197-089		C-CAP,S 0.01-25 B
C404	87-012-140-089		C-CAP,S 470P-50 CH
C405	87-010-322-089		C-CAP,S 100P-50 CH
C406	87-012-140-089		C-CAP,S 470P-50 CH
C407	87-016-350-049		CAP,E 470-4 MA GAS
C408	87-010-196-089		C-CAP,S 0.1-25 F
C409	87-010-197-089		C-CAP,S 0.01-25 B
C410	87-010-197-089		C-CAP,S 0.01-25 B
C411	87-010-550-049		CAP,E 100-6.3 GAS
C412	87-010-197-089		C-CAP,S 0.01-25 B
C413	87-010-314-089		C-CAP,S 22P-50 CH
C414	87-010-316-089		C-CAP,S 33P-50 CH
C415	87-010-499-049		CAP,E 22-6.3 GAS
C416	87-010-197-089		C-CAP,S 0.01-25 B
C418	87-010-197-089		C-CAP,S 0.01-25 B
C420	87-010-196-089		C-CAP,S 0.1-25 F
C421	87-012-140-089		C-CAP,S 470P-50 CH
C422	87-010-184-089		C-CAP,S 3300P-50 B
C422	87-010-184-089		C-CAP,S 3300P-50 B
C423	87-010-175-089		C-CAP,S 560P-50 SL
C424	87-010-317-089		C-CAP,S 39P-50 CH
C425	87-012-140-089		C-CAP,S 470P-50 CH
C501	87-010-549-049		CAP,E 47-6.3 GAS
C502	87-010-196-089		C-CAP,S 0.1-25 F
C503	87-010-318-089		C-CAP,S 47P-50 CH
C505	87-010-313-089		C-CAP,S 18P-50 CH
C506	87-010-313-089		C-CAP,S 18P-50 CH
C507	87-010-197-089		C-CAP,S 0.01-25 B
C508	87-010-178-089		C-CAP,S 1000P-50 B
C509	87-010-178-089		C-CAP,S 1000P-50 B
C510	87-010-178-089		C-CAP,S 1000P-50 B
C511	87-010-178-089		C-CAP,S 1000P-50 B
C512	87-010-498-049		CAP,E 10-16 GAS
C513	87-010-498-049		CAP,E 10-16 GAS
C514	87-010-318-089		C-CAP,S 47P-50 CH
C515	87-010-318-089		C-CAP,S 47P-50 CH
C516	87-010-196-089		C-CAP,S 0.1-25 F
C599	87-010-196-089		C-CAP,S 0.1-25 F
C601	87-010-561-049		CAP,E 100-16 5L
C602	87-010-432-049		CAP,E 10-16 OS

REF. NO.	PART NO.	カンリ NO.	DESCRIPTION
C603	87-010-196-089		C-CAP,S 0.1-25 F
C604	87-010-196-089		C-CAP,S 0.1-25 F
C605	87-A10-222-049		CAP,E 22-10 OS
C606	87-010-196-089		C-CAP,S 0.1-25 F
C607	87-012-140-089		C-CAP,S 470P-50 CH
C608	87-010-196-089		C-CAP,S 0.1-25 F
J401	87-009-502-019		JACK,PIN 1PY EARTH
L101	87-005-781-089		C-COIL,47UH FLC32C
L201	87-005-781-089		C-COIL,47UH FLC32C
L202	87-005-781-089		C-COIL,47UH FLC32C
L301	87-005-781-089		C-COIL,47UH FLC32C
L302	87-005-781-089		C-COIL,47UH FLC32C
L303	87-005-781-089		C-COIL,47UH FLC32C
L401	87-005-196-089		COIL,10UH
L402	87-005-781-089		C-COIL,47UH FLC32C
L404	87-005-190-089		COIL,3.3UH
L405	87-005-189-089		COIL,2.7UH
L501	87-005-781-089		C-COIL,47UH FLC32C
L601	87-005-469-089		COIL,4.7UH
L602	87-A50-095-019		COIL,68UH
M201	87-045-305-019		MOTOR, RF-500TB
S101	87-036-109-019		SW,PUSH SPPB 61
S102	87-036-109-019		SW,PUSH SPPB 61
S201	87-A90-162-019		SW,SL 1-1-3 SSSU
X201	87-A70-027-089		VIB,XTAL 8MHZ 100PPM
X401	87-A70-026-089		VIB,XTAL 13.5MHZ 50PPM
X501	87-030-270-089		VIB,XTAL 16.9344MHZ

CD MECHA C.B<V3L,V4L,V5>

C101	87-010-154-089		C-CAP,S 10P-50 CH<EXCEPT V5>
C101	87-010-334-080		C-CAP,S 12P-50 CH<V5>
C102	87-010-193-089		C-CAP,S 0.033-25 F<V5>
C102	87-010-184-089		C-CAP,S 3300P-50 B<EXCEPT V5>
C103	87-010-197-089		C-CAP,S 0.01-25 B<EXCEPT V5>
C103	87-010-993-089		C-CAP,S 0.056-25<V5>
C104	87-010-193-089		C-CAP,S 0.033-25 F<EXCEPT V5>
C104	87-010-993-089		C-CAP,S 0.056-25<V5>
C105	87-010-197-089		C-CAP,S 0.01-25 B
C107	87-010-197-089		C-CAP,S 0.01-25 B<V5>
C107	87-010-182-089		C-CAP,S 2200P-50 B<EXCEPT V5>
C108	87-010-805-089		C-CAP,S 1-16F
C109	87-010-322-089		C-CAP,S 100P-50 CH
C110	87-010-198-089		C-CAP,S 0.022-25 B<EXCEPT V5>
C110	87-010-993-089		C-CAP,S 0.056-25<V5>
C111	87-010-551-089		CAP ELECT 33-10V SRE<EXCEPT V5>
C111	87-010-499-049		CAP,E 22-6.3 GAS<V5>
C112	87-010-322-089		C-CAP,S 100P-50 CH
C113	87-010-196-089		C-CAP,S 0.1-25 F
C114	87-010-197-089		C-CAP,S 0.01-25 B
C115	87-010-196-089		C-CAP,S 0.1-25 F<EXCEPT V5>
C115	87-012-141-089		C-CAP,S 0.22-16 F<V5>
C116	87-010-182-089		C-CAP,S 2200P-50 B
C117	87-010-196-089		C-CAP,S 0.1-25 F<EXCEPT V5>
C117	87-012-141-089		C-CAP,S 0.22-16 F<V5>
C118	87-010-196-089		C-CAP,S 0.1-25 F
C119	87-010-193-089		C-CAP,S 0.033-25 F<V5>
C119	87-010-196-089		C-CAP,S 0.1-25 F<EXCEPT V5>
C120	87-010-549-089		CAP ELECT 47-6.3V
C121	87-010-549-089		CAP ELECT 47-6.3V
C122	87-010-495-089		CAP,E 2.2-35 5L<V5>
C122	87-010-497-089		CAP,E 4.7-35 5L<EXCEPT V5>
C123	87-010-549-089		CAP ELECT 47-6.3V
C125	87-010-553-089		CAP,E 47-16
C127	87-010-553-089		CAP,E 47-16
C127	87-010-549-089		CAP,E 47-6.3 GAS
C128	87-010-549-089		CAP ELECT 47-6.3V
C129	87-010-182-089		C-CAP,S 2200P-50 B
C131	87-010-196-089		C-CAP,S 0.1-25 F
C133	87-010-196-089		C-CAP,S 0.1-25 F
C134	87-010-196-089		C-CAP,S 0.1-25 F
C135	87-010-196-089		C-CAP,S 0.1-25 F

REF. NO.	PART NO.	カンリ NO.	DESCRIPTION
C136	87-010-197-089		C-CAP,S 0.01-25 B
C137	87-010-805-089		C-CAP,S 1-16F
C138	87-010-178-089		C-CAP,S 1000P-50 B
C140	87-010-805-089		C-CAP,S 1-16F<EXCEPT V5>
FC4	85-NFT-611-119		FF-CABLE,16P-1.0
M101	87-045-356-019		MOT,RF-310T A 30
M102	87-045-358-019		MOT,RF-310T A 43
R140	87-022-364-089		C-RES,S82K-1/10WF
R141	87-022-363-089		C-RES,S 68K-1/10W F
R142	87-022-363-089		C-RES,S 68K-1/10W F
R143	87-022-363-089		C-RES,S 68K-1/10W F
R144	87-022-363-089		C-RES,S 68K-1/10W F
R145	87-022-364-089		C-RES,S82K-1/10WF
SFR101	87-024-175-089		SFR,47K DIA6 V
SFR102	87-024-176-089		SFR,100K DIA6 V
SFR103	87-024-175-089		SFR,47K DIA6 V
SW101	87-036-340-019		SW,LEAF LSA-1121

T-T C.B

C401	87-018-214-089		CAP TC U 0.1-50 F
FC401	84-ZG1-614-119		CABLE FFC 5P-1.25
M401	87-045-364-019		MOTOR,(BCH3B14)
PS401	87-026-573-019		P-SNSR,GP1S53V

LED C.B<F>

LED101	87-070-200-089		LED,SLP636C-81-S-T1<F>
LED102	87-017-350-080		LED,SEL1550CM<F>
LED103	87-017-350-080		LED,SEL1550CM<F>
LED104	87-070-200-089		LED,SLP636C-81-S-T1<F>

VCD C.B<V3L>

C2	87-010-378-010		CAP,E 10-16
C3	87-010-378-010		CAP,E 10-16
C4	87-010-374-010		CAP,E 47-10
C5	87-010-374-010		CAP,E 47-10
C9	87-010-378-010		CAP,E 10-16
C10	87-010-378-010		CAP,E 10-16
C11	87-010-378-010		CAP,E 10-16
C12	87-010-374-010		CAP,E 47-10
C13	87-010-378-010		CAP,E 10-16
C17	87-010-248-010		CAP,E 220-10
C22	87-010-374-010		CAP,E 47-10
C23	87-010-374-010		CAP,E 47-10
C32	87-010-378-010		CAP,E 10-16
C47	87-010-248-010		CAP,E 220-10
C49	87-010-378-010		CAP,E 10-16
C52	87-010-248-010		CAP,E 220-10
C101	87-010-378-010		CAP,E 10-16
L1	SL-AL0-4NA-100		COIL,10UH
L2	SL-AL0-4NA-472		COIL,4.7UH
X1	SS-KY4-05M-000		X'TAL,40.5MHz
X2	SS-KY4-M00-000		X'TAL,4MHz
X3	SS-KY4-433-616		X'TAL,4.433616MHz

VCD C.B<V4L>

C13	87-010-367-080		CAP,E 4.7-25V(5ECEC1)
C38	87-010-075-040		CAP,E 10-16V(5ECEC1)
C40	87-010-549-010		CAP,E 47-6.3V(5ECEC0)
C44	87-010-549-010		CAP,E 47-6.3V(5ECEC0)
C47	87-010-549-010		CAP,E 47-6.3V(5ECEC0)
C48	87-010-549-010		CAP,E 47-6.3V(5ECEC0)
C51	87-010-549-010		CAP,E 47-6.3V(5ECEC0)
C54	87-010-549-010		CAP,E 47-6.3V(5ECEC0)
C56	87-010-076-810		CAP,E 22-6.3V(5ECEC0)
C58	87-010-076-810		CAP,E 22-6.3V(5ECEC0)
C81	87-016-155-010		CAP,E 1000-6.3V5ECER0)
C128	87-010-549-010		CAP,E 47-6.3V(5ECEC0)
C133	87-010-053-810		CAP,E 1-50V(5ECEC1)
C150	87-010-075-040		CAP,E 10-16V(5ECEC1)

REF. NO.	PART NO.	カンリ NO.	DESCRIPTION
C151	87-010-549-010		CAP,E 47-6.3V(5ECEC0)
C152	87-016-155-010		CAP,E 1000-6.3V5ECER0)
C157	87-010-075-040		CAP,E 10-16V(5ECEC1)
CT1	S2-130-007-010		CAP,TRIMMER 30PF(5ECT04)
L1	S7-001-XXX-100		C-COIL,47UH(5ELQE4)
X1	S0-120-003-010		X'TAL,12.0000MHZ(5EXMA4)
X2	S0-177-343-010		X'TAL,17.73447MHZ(5EXMA4)

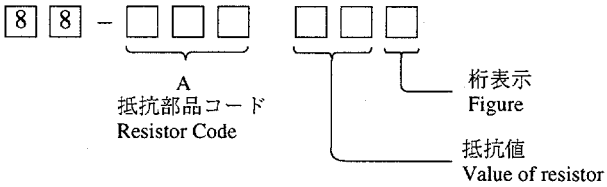
SUB C.B<V3L>

DRIVE C.B<WR>

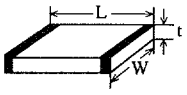
M1	87-045-358-019		MOT,RF-310TA 43
M2	87-045-356-019		MOT,RF-310TA 30
SW1	87-A90-042-019		SW,LEAF MSW 17310 MVPO

○ チップ抵抗部品コード／CHIP RESISTOR PART CODE

チップ抵抗部品コードの成り立ち
Chip Resistor Part Coding

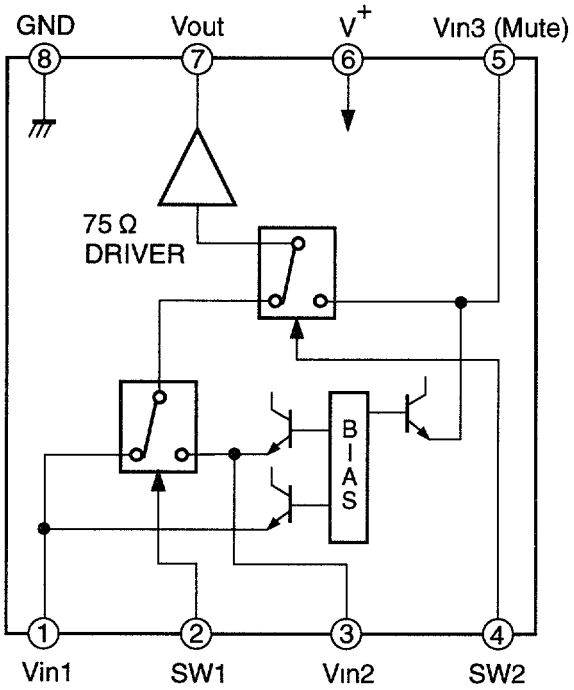


チップ抵抗
Chip resistor

容量 Wattage	種類 Type	許容誤差 Tolerance	記号 Symbol	寸法／Dimensions (mm) 外形／Form	L	W	t	抵抗コード ：A Resistor Code: A
1／16W	1608	±5%	CJ		1.6	0.8	0.45	108
1／10W	2125	±5%	CJ		2	1.25	0.45	118
1／8W	3216	±5%	CJ		3.2	1.6	0.55	128

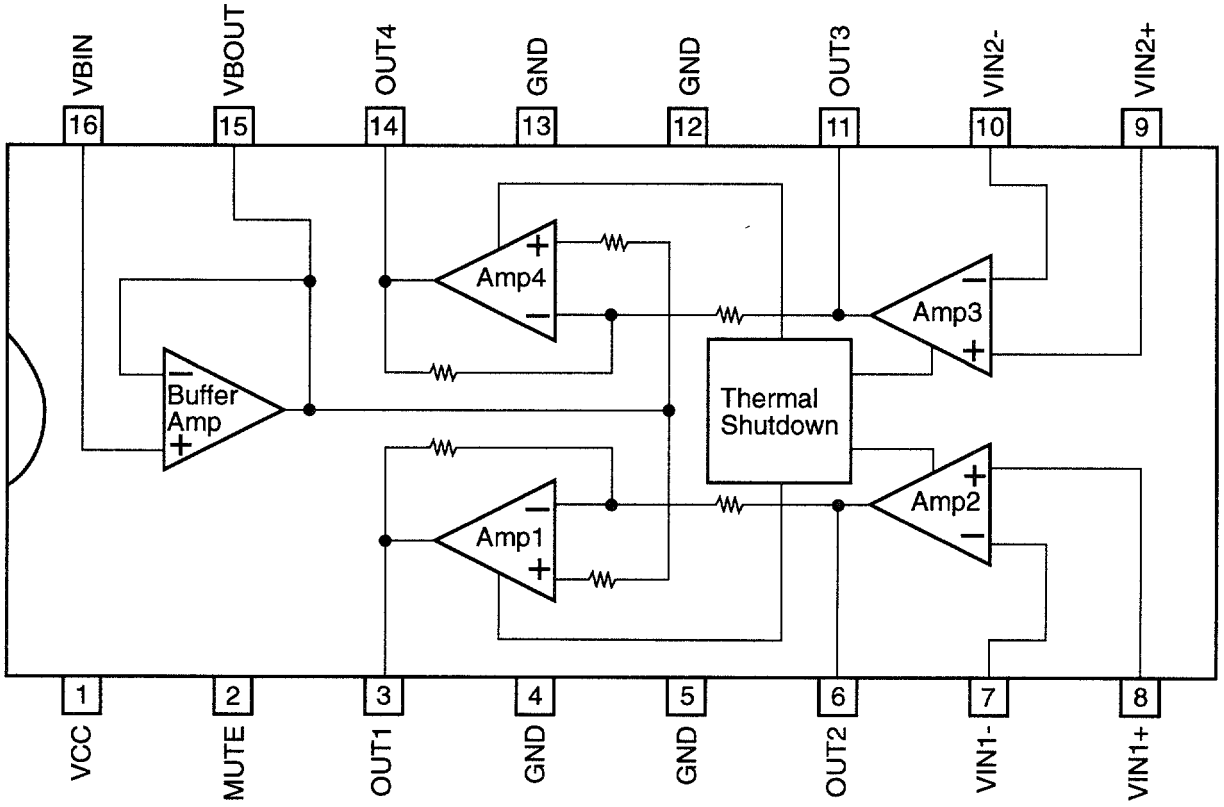
IC BLOCK DIAGRAM

IC, NJM2244L

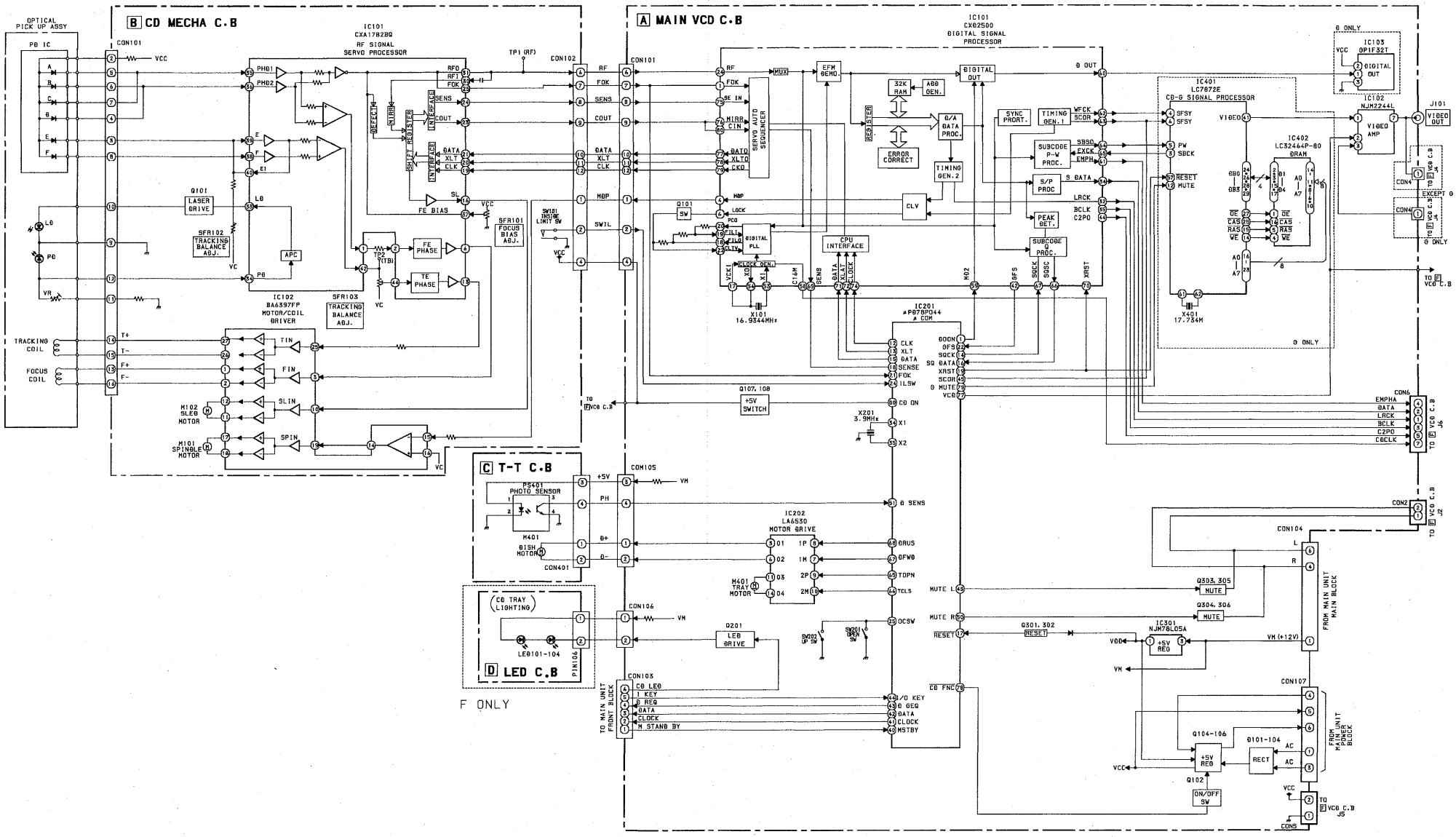


SW1	SW2	OUTPUT SIGNAL
L	L	Vin1
H	L	Vin2
L/H	H	Vin3

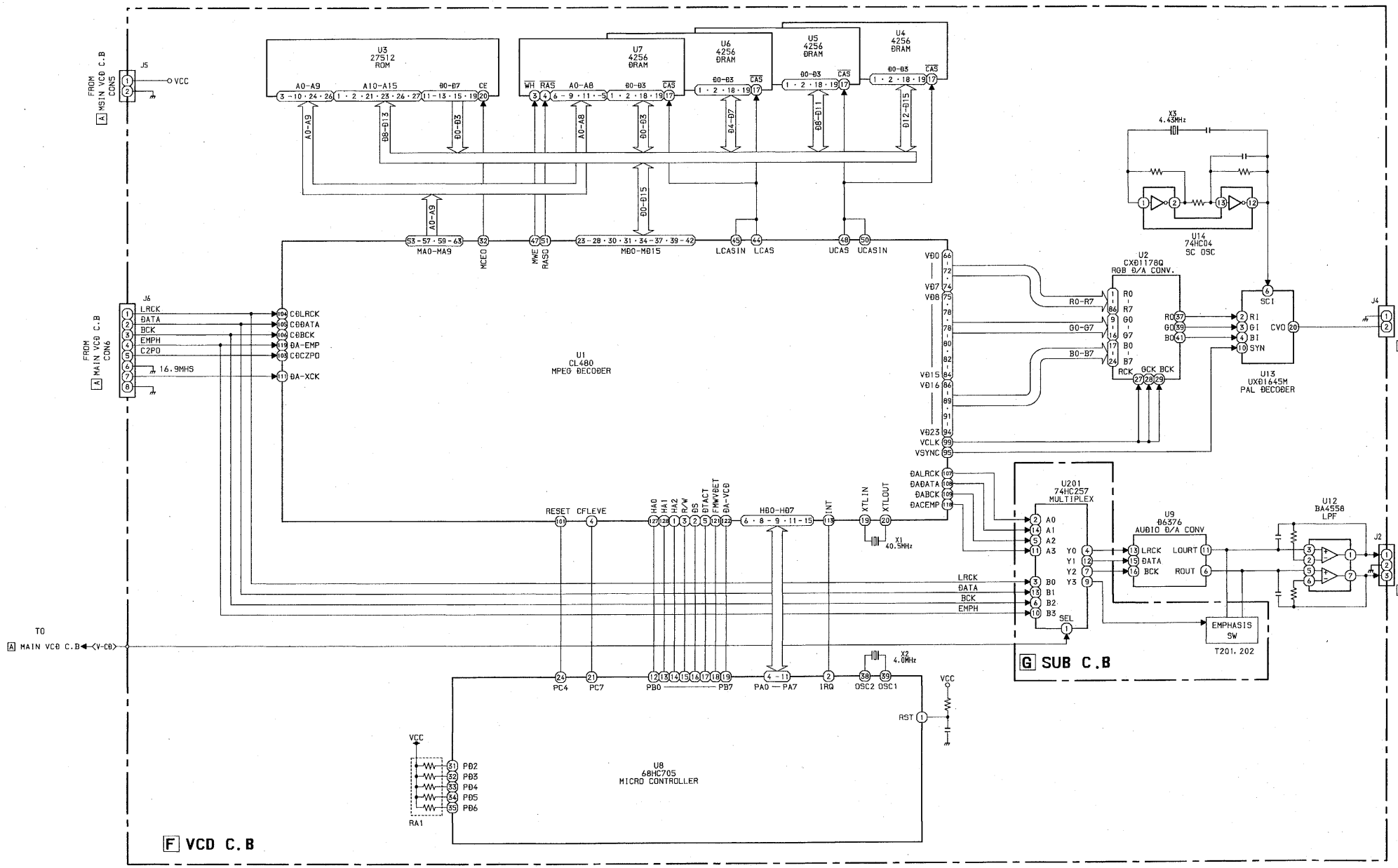
IC, LA6530



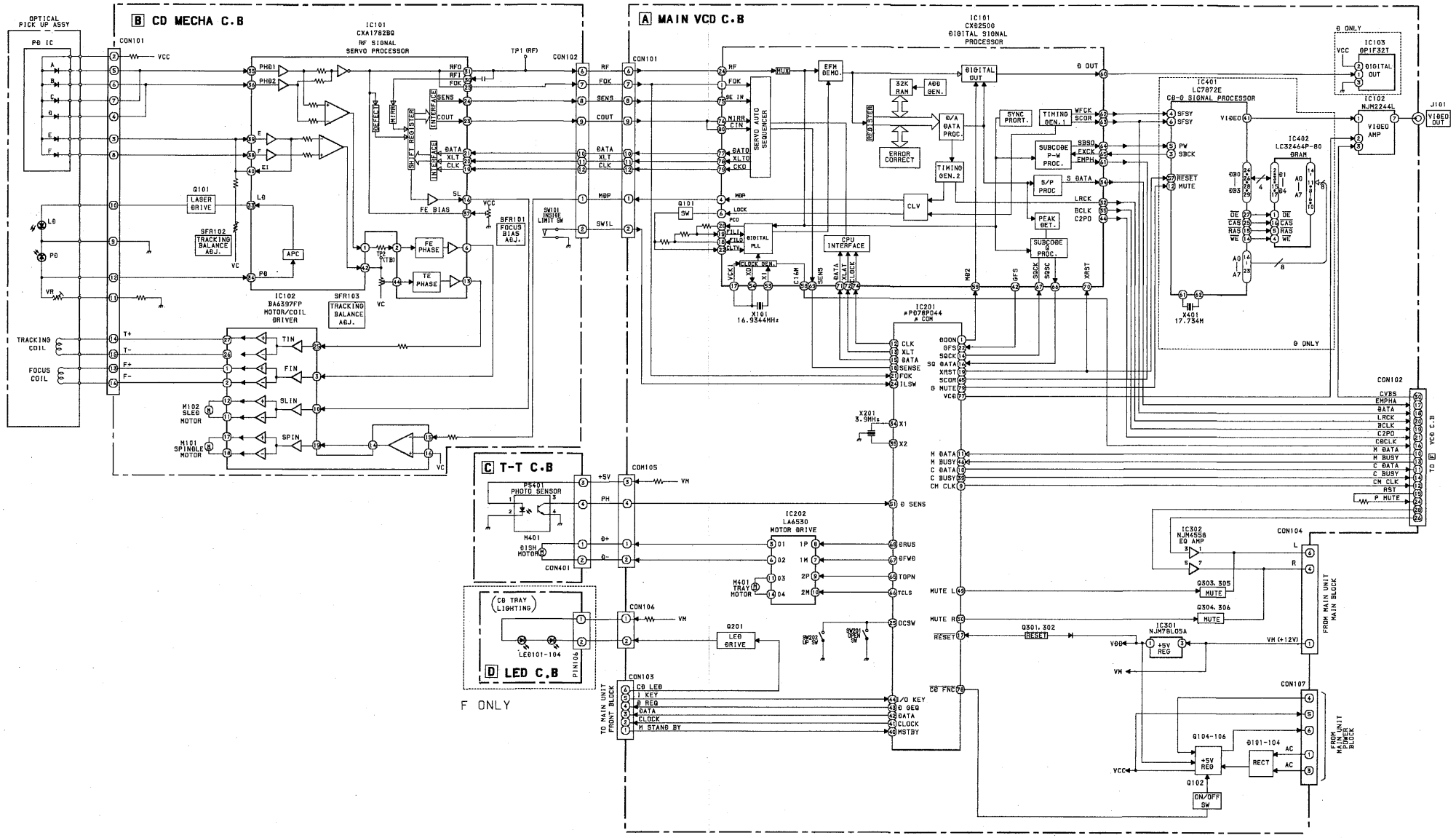
BLOCK DIAGRAM-1 (V3L: MAIN VCD ／ CD MECHA)



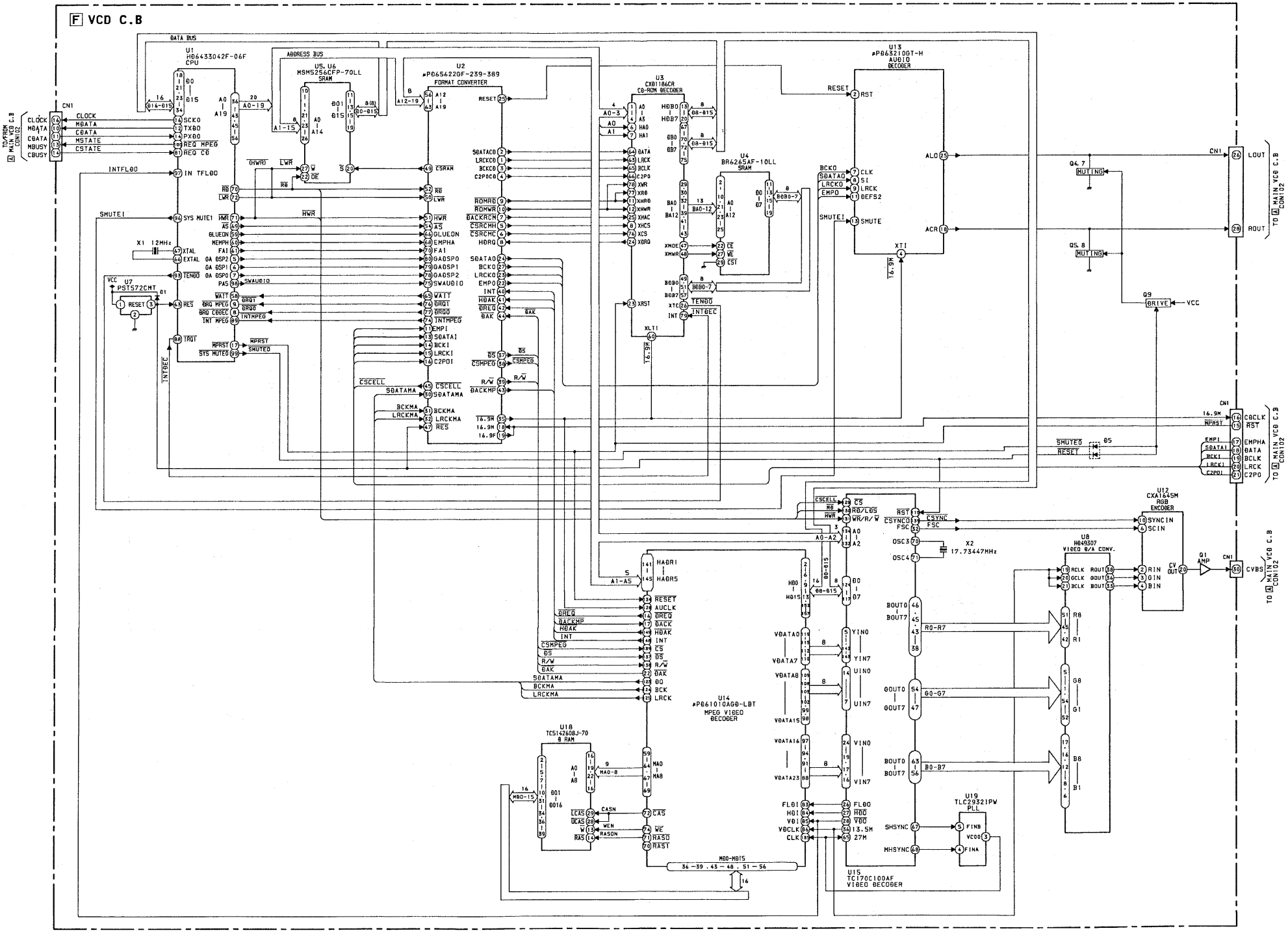
BLOCK DIAGRAM-2 (V3L: VCD)



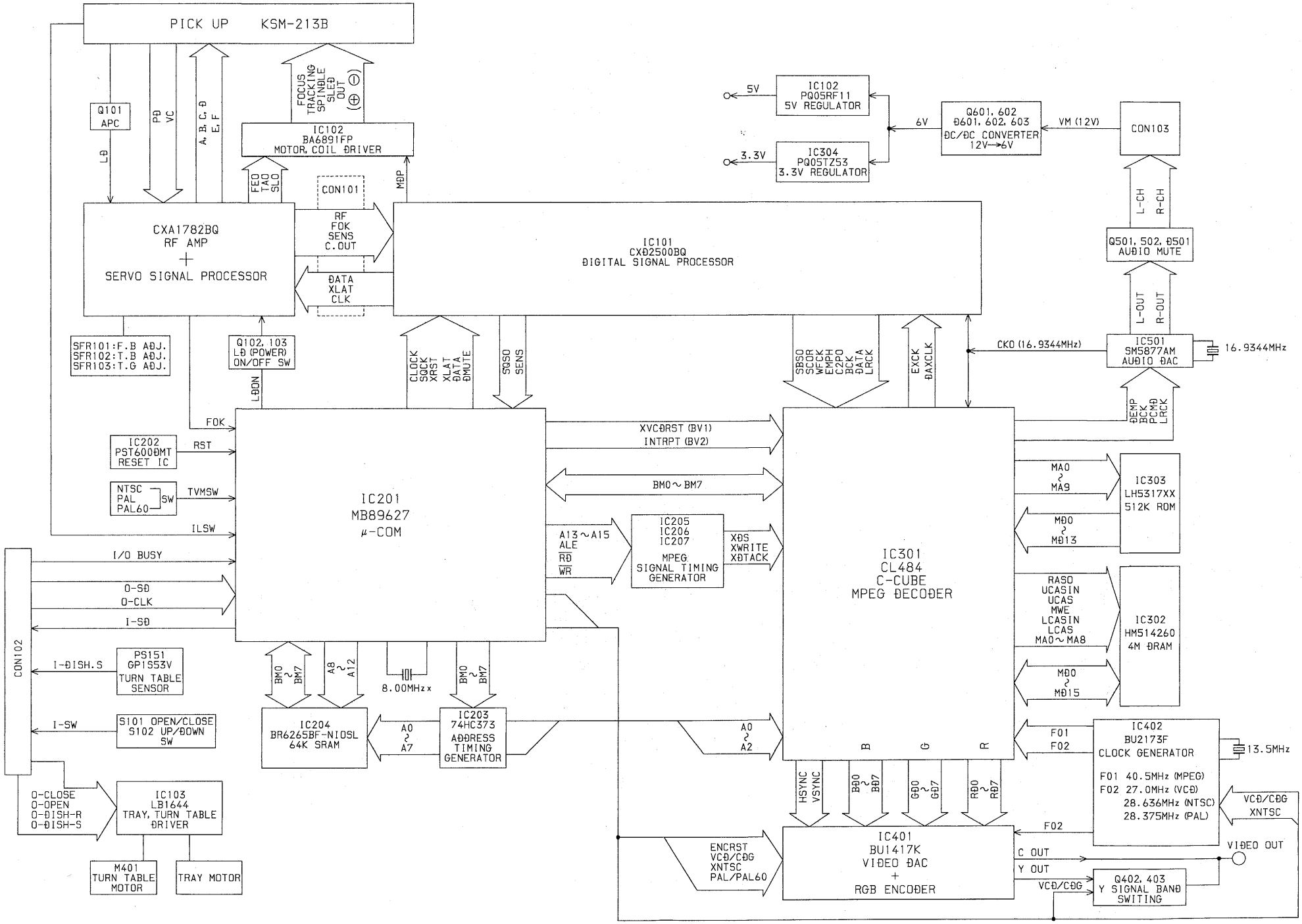
BLOCK DIAGRAM-3 (V4L: MAIN VCD ／ CD MECHA)

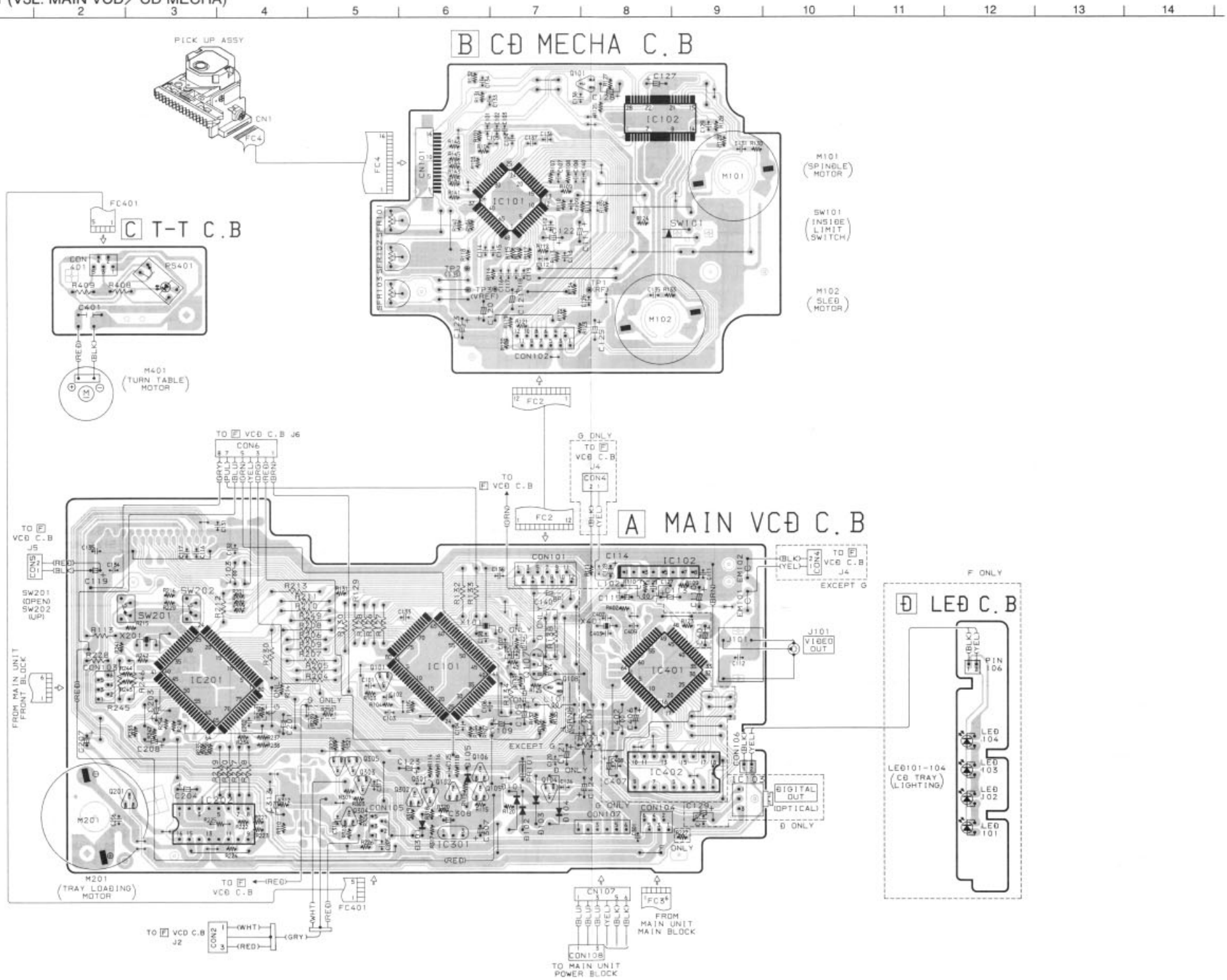


BLOCK DIAGRAM-4 (V4L: VCD)

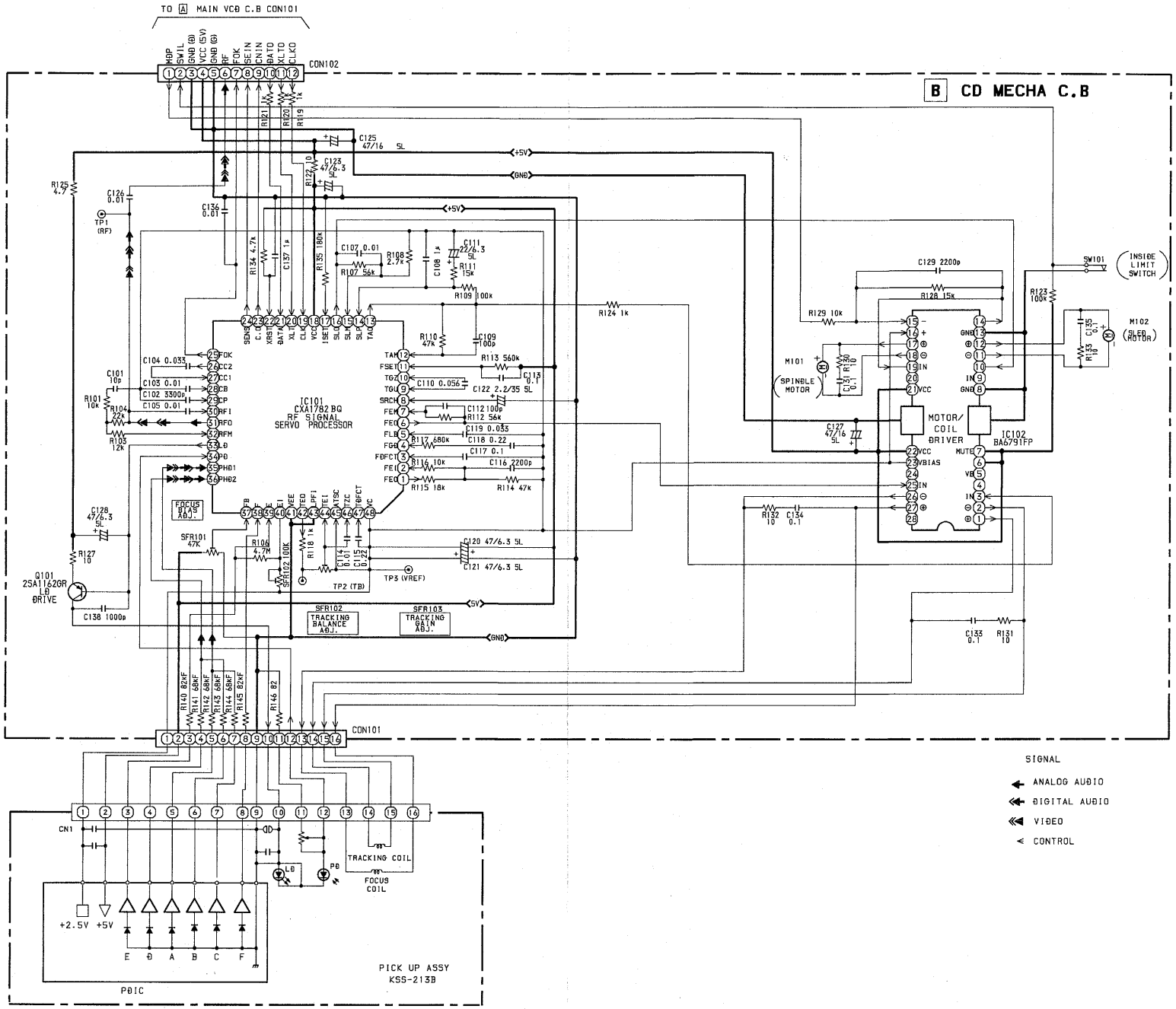


BLOCK DIAGRAM-5 (V5)

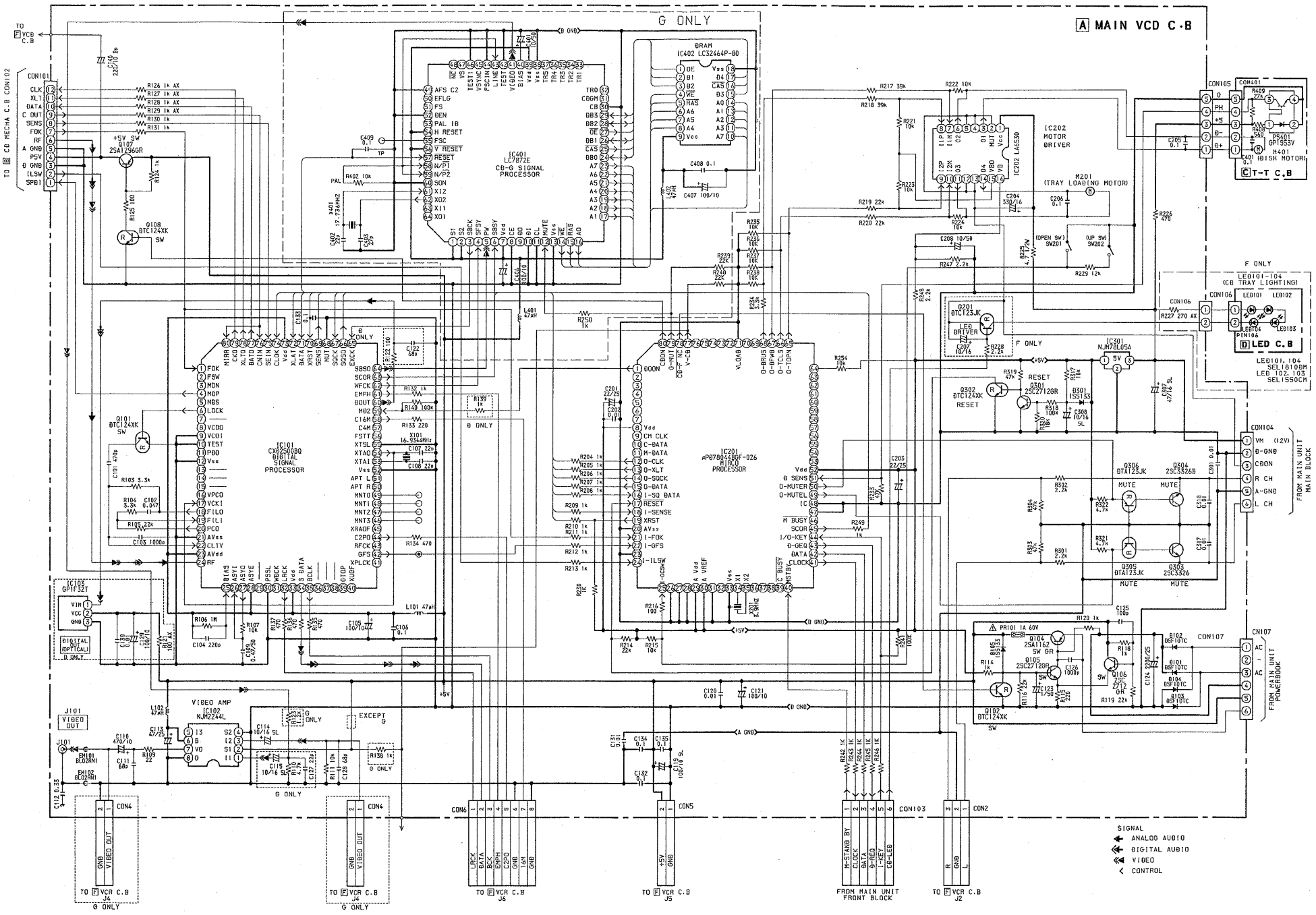


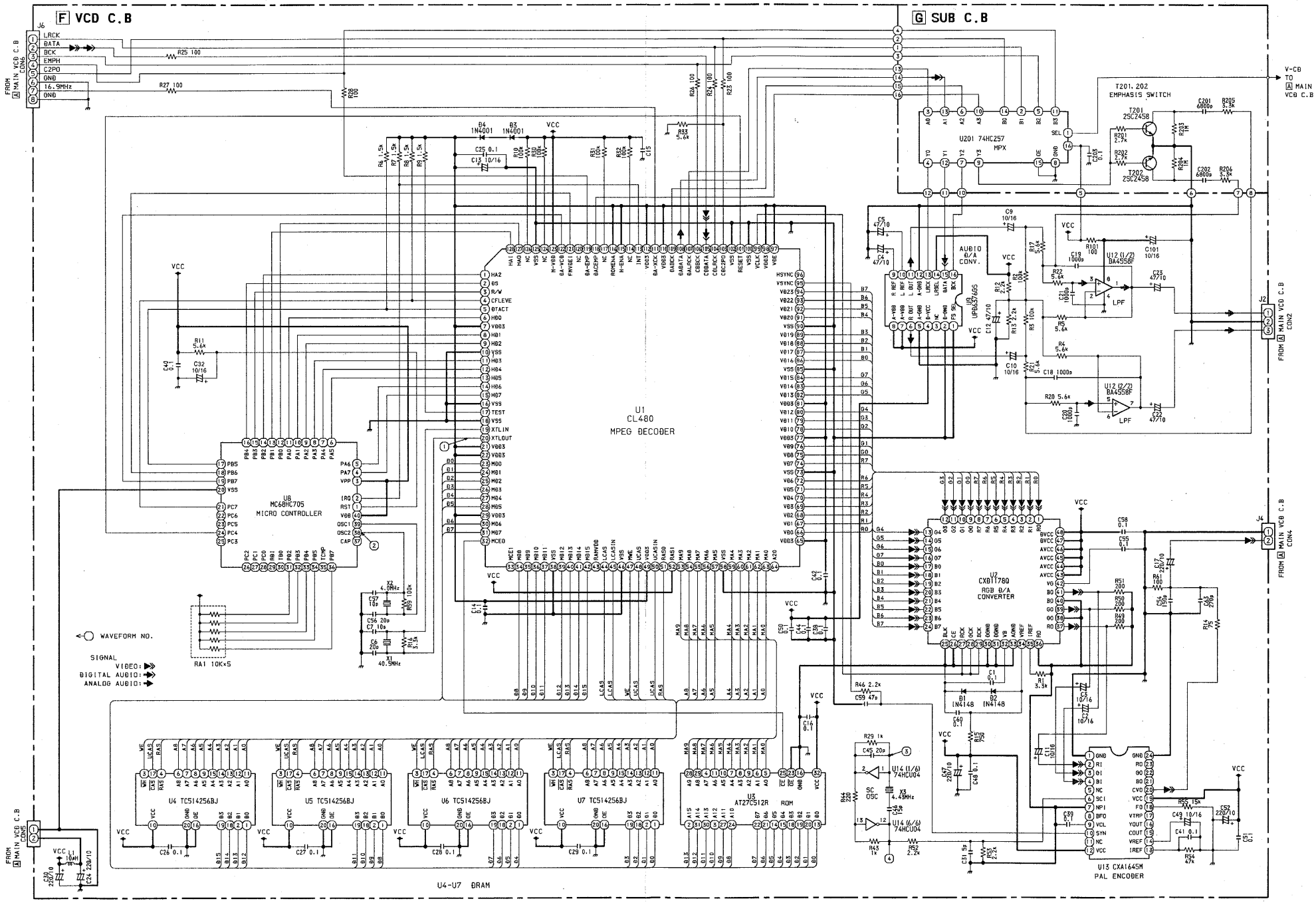

B CD MECHA C.B
PICK UP ASSY
CN1
FC4
IC102
IC101
M101
(SPINDLE MOTOR)
SW101
(INSIDE LIMIT SWITCH)
M102
(SLED MOTOR)
CON102
FC2
C T-T C.B
FC401
CON 401
RS401
R409
R408
C401
M401
(TURN TABLE MOTOR)
TO F VCD C.B J6
CON6
TO F VCD C.B
G ONLY
TO F VCD C.B J4
CON4
A MAIN VCD C.B
IC201
IC401
IC402
IC301
CON101
CON105
CON106
CON107
CON108
SW201
SW202
J5
CONS
J101
VIDEO OUT
EXCEPT G
F ONLY
D LED C.B
LED104
LED103
LED102
LED101
PIN 106
LED101-104
(CD TRAY LIGHTING)
DIGITAL OUT (OPTICAL)
D ONLY
M201
(TRAY LOADING MOTOR)
FROM MAIN UNIT FRONT BLOCK
FROM MAIN UNIT MAIN BLOCK
TO MAIN UNIT POWER BLOCK
TO F VCD C.B J2
CON2

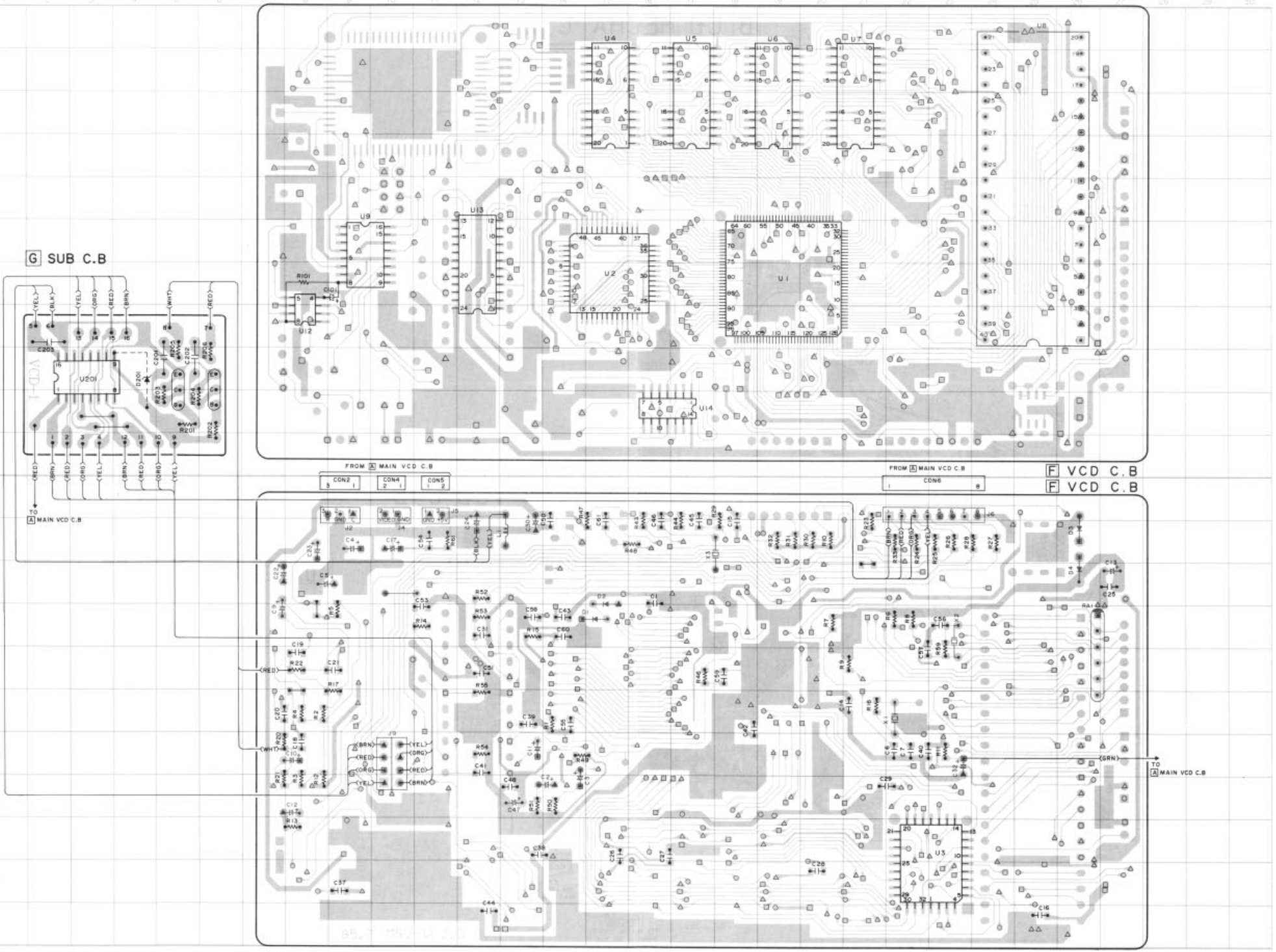
SCHEMATIC DIAGRAM-1 (V3L: CD MECHA)



SCHEMATIC DIAGRAM-2 (V3L: MAIN VCD)



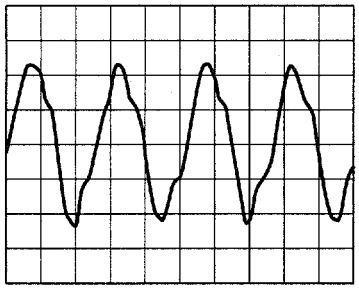

F VCD C.B
G SUB C.B
U1
CL480
MPEG DECODER
U8
MC68HC705
MICRO CONTROLLER
U2
CXD1780
RGB D/A
CONVERTER
U13 CXA1645M
PAL ENCODER
U4 TC514256BJ
U5 TC514256BJ
U6 TC514256BJ
U7 TC514256BJ
U3
AT27C512R
ROM
U4-U7 DRAM
U201 74HC257
MPX
T201, 202
EMPHASIS SWITCH
T201
2SC2458
T202
2SC2458
AUDIO
D/A
CONV.
U9
UPD63705
U12 (1/2)
BA4558F
U12 (2/2)
BA4558F
LPF
LPF
U14 (1/6)
74HCU04
U14 (6/6)
74HCU04
RA1 10K×5
WAVEFORM NO.
SIGNAL
VIDEO:
DIGITAL AUDIO:
ANALOG AUDIO:
FROM A MAIN VCB C.B CON6
V-CB TO A MAIN VCB C.B
FROM A MAIN VCB C.B CON2
FROM A MAIN VCB C.B CON4
FROM A MAIN VCB C.B CON1
LRCK
BATA
BCK
EMPH
C2PO
GNB
16.9MHz
GNB
R25 100
R27 100
VCC


G SUB C.B
F VCD C.B
F VCD C.B
FROM A MAIN VCD C.B
CON2
CON4
CON5
FROM A MAIN VCD C.B
CON6
TO A MAIN VCD C.B
TO A MAIN VCD C.B
U1
U2
U3
U4
U5
U6
U7
U8
U9
U12
U13
U14
U201

WAVE FORM

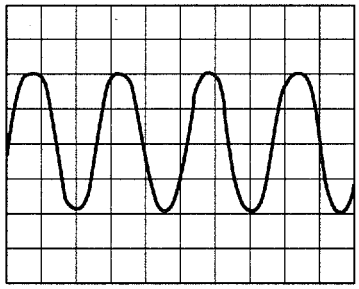
① U1 Pin ⑳ (XLT OUT)

VOLT/DIV: 1V
TIME/DIV: 10nS



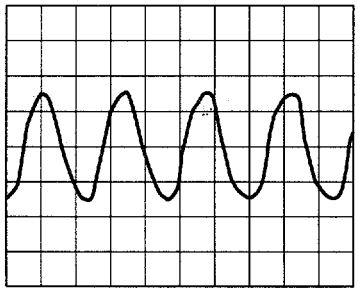
② U8 Pin ㊳ (OSC2)

VOLT/DIV: 1V
TIME/DIV: 100nS



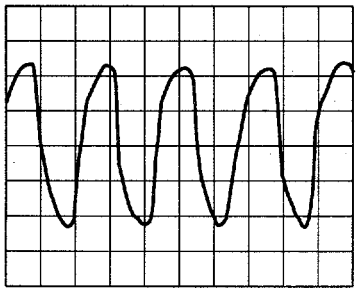
③ U14 Pin ①

VOLT/DIV: 1V
TIME/DIV: 100nS

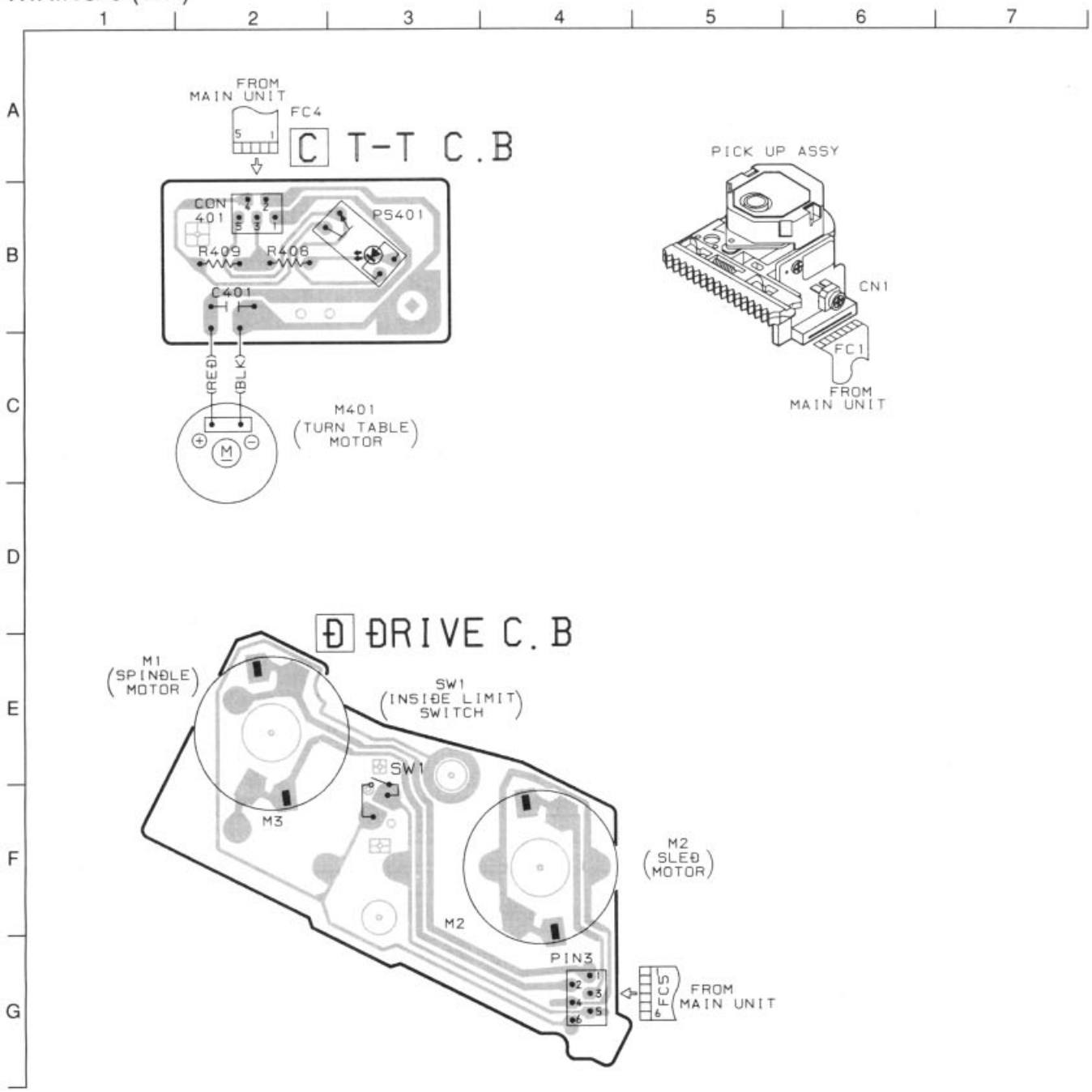


④ U14 Pin ⑫

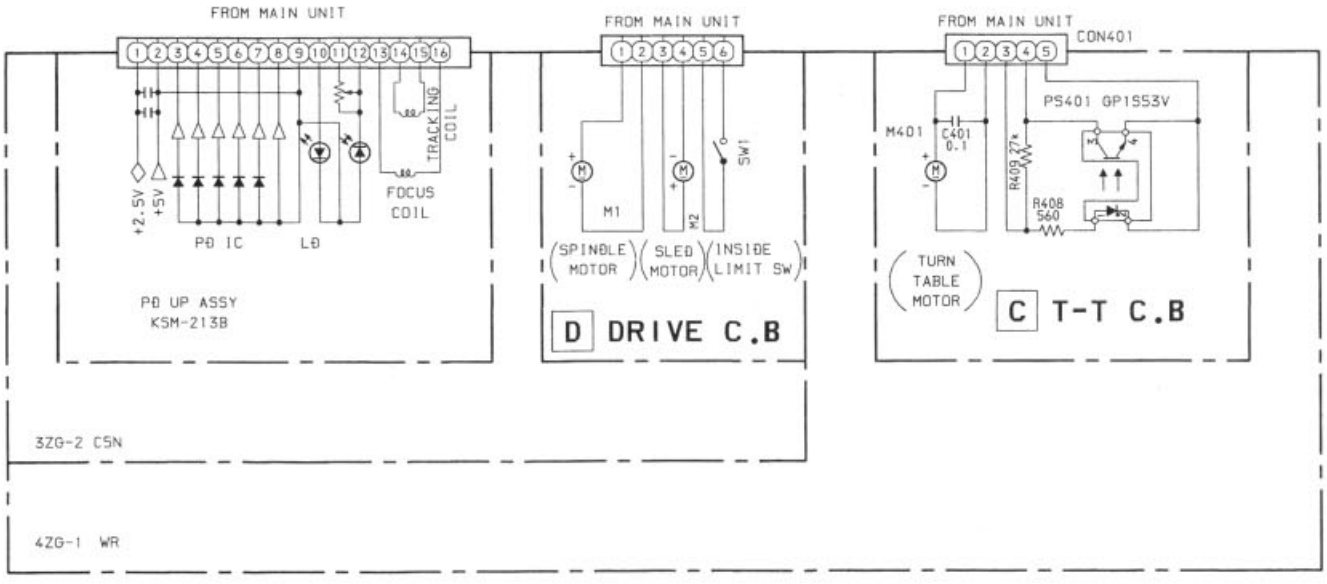
VOLT/DIV: 1V
TIME/DIV: 100nS



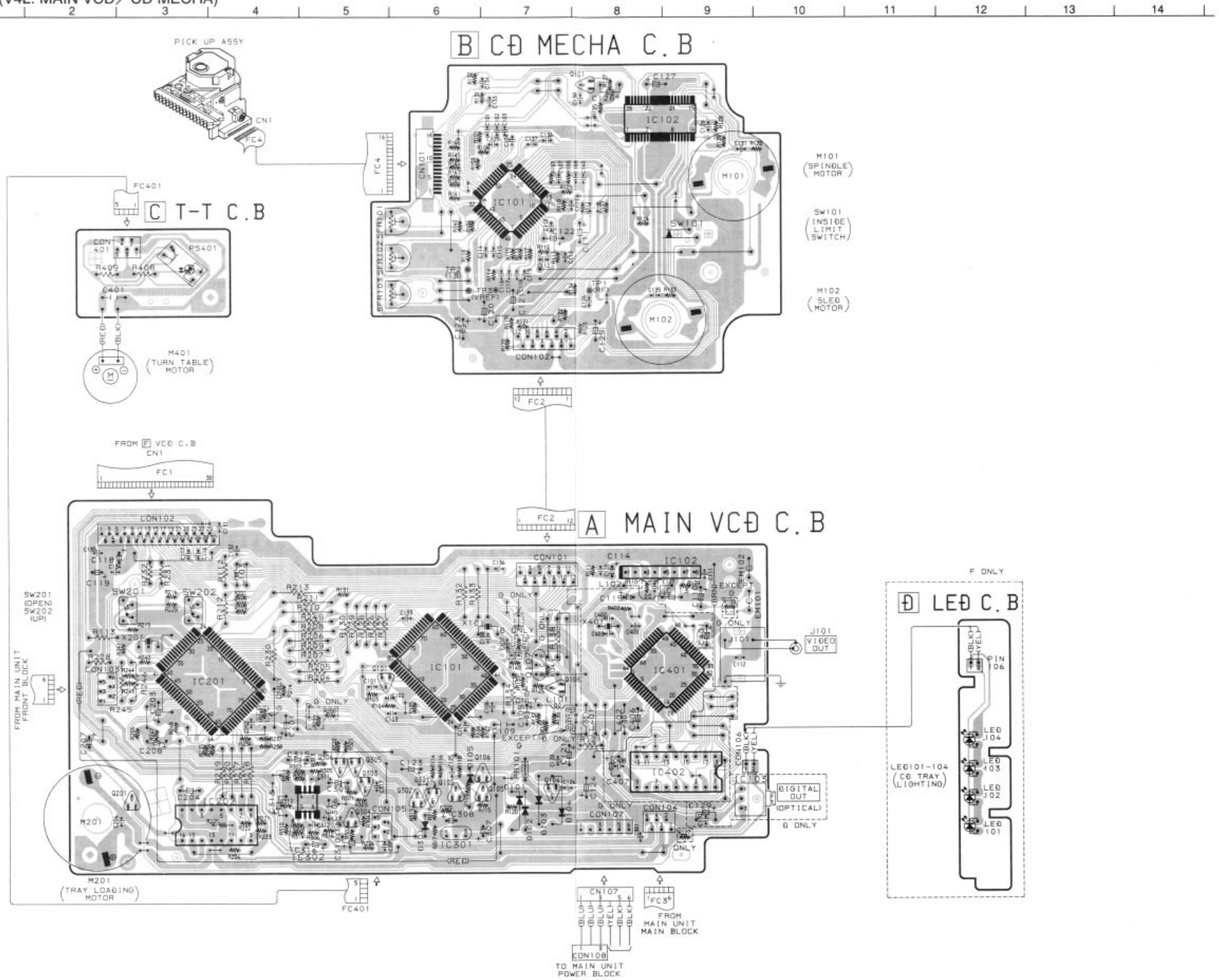
WIRING-3 (WR)



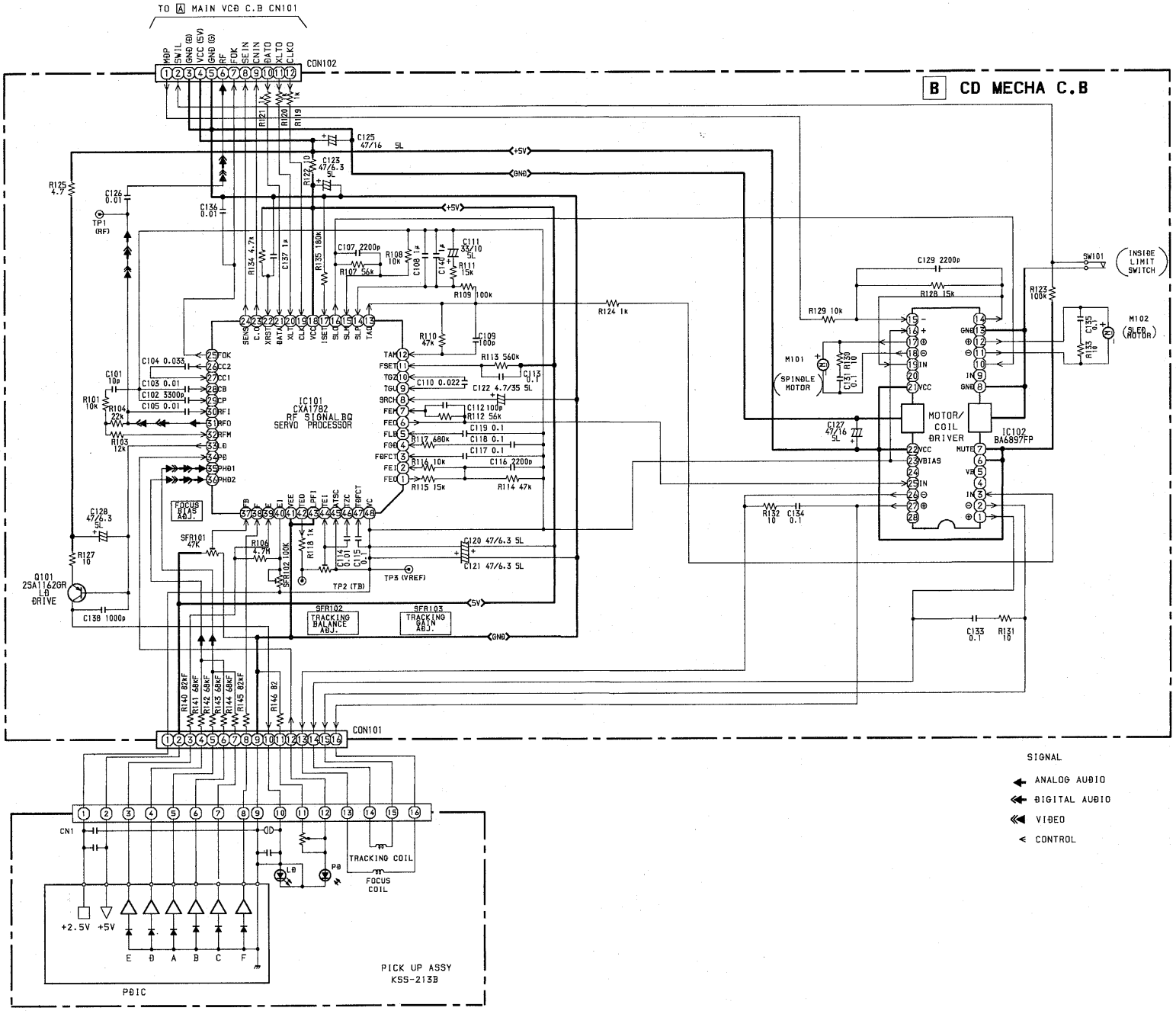
SCHEMATIC DIAGRAM-4 (WR)



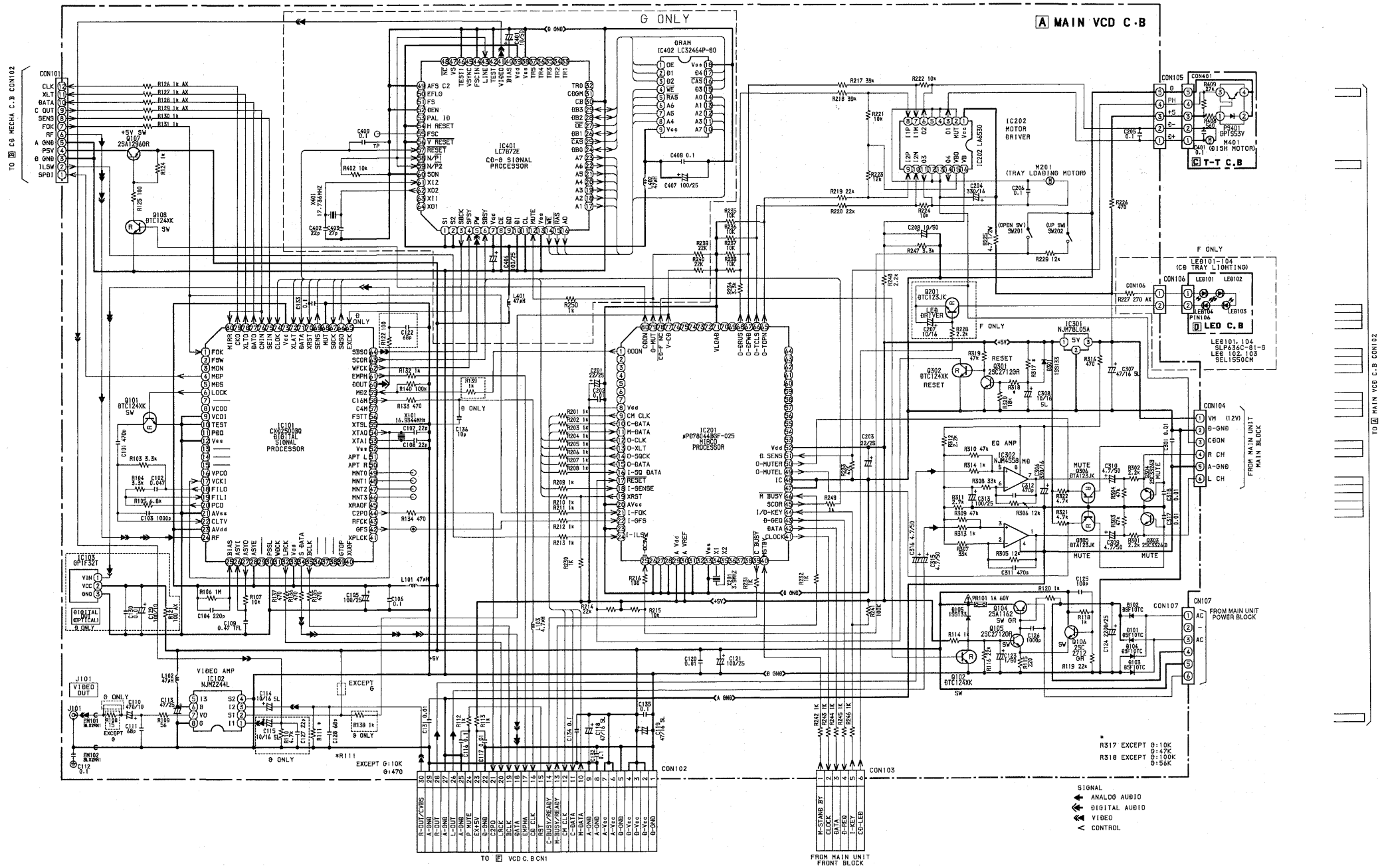
WIRING-4 (V4L: MAIN VCD／CD MECHA)

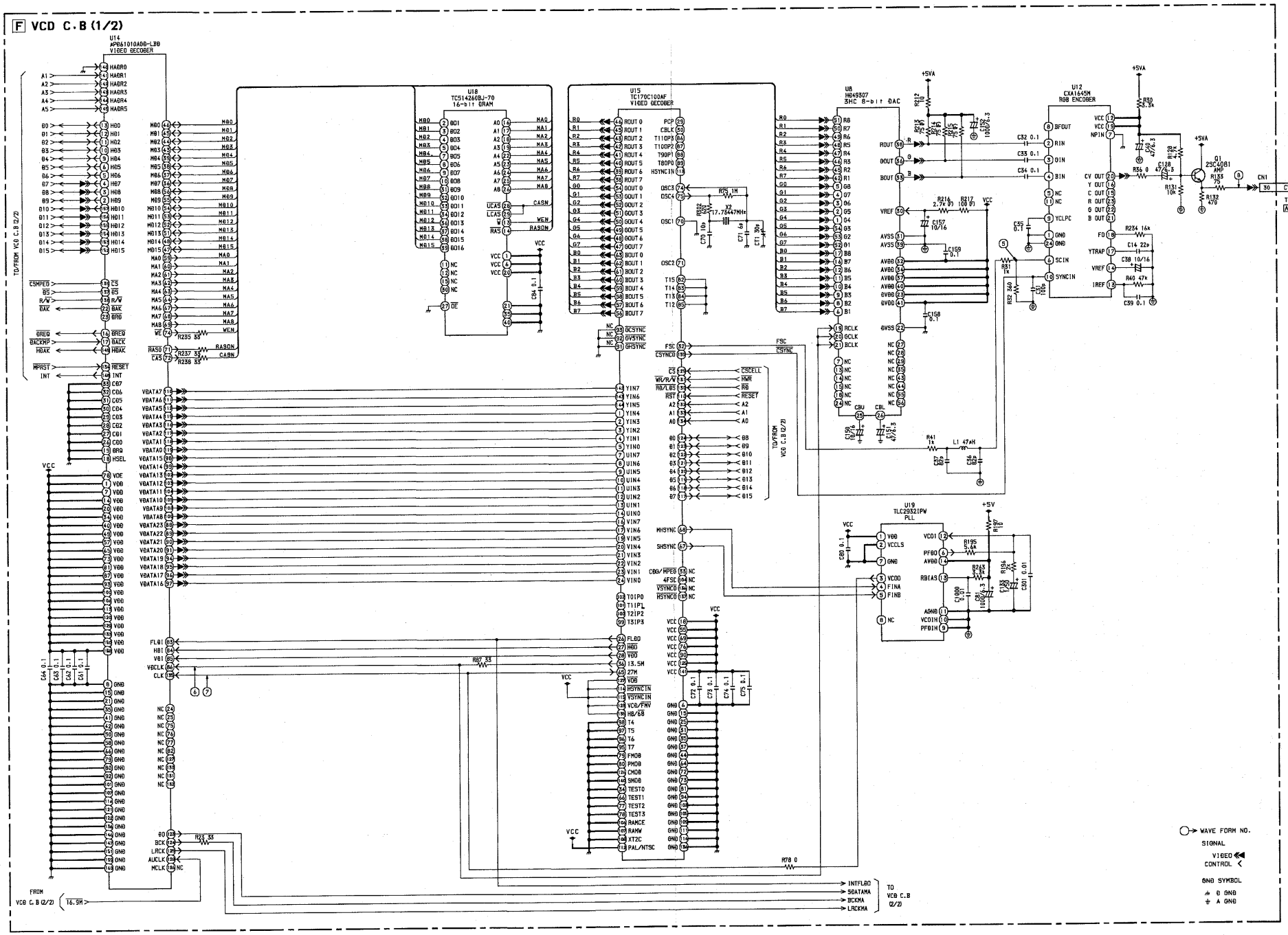


SCHEMATIC DIAGRAM-5 (V4L: CD MECHA)

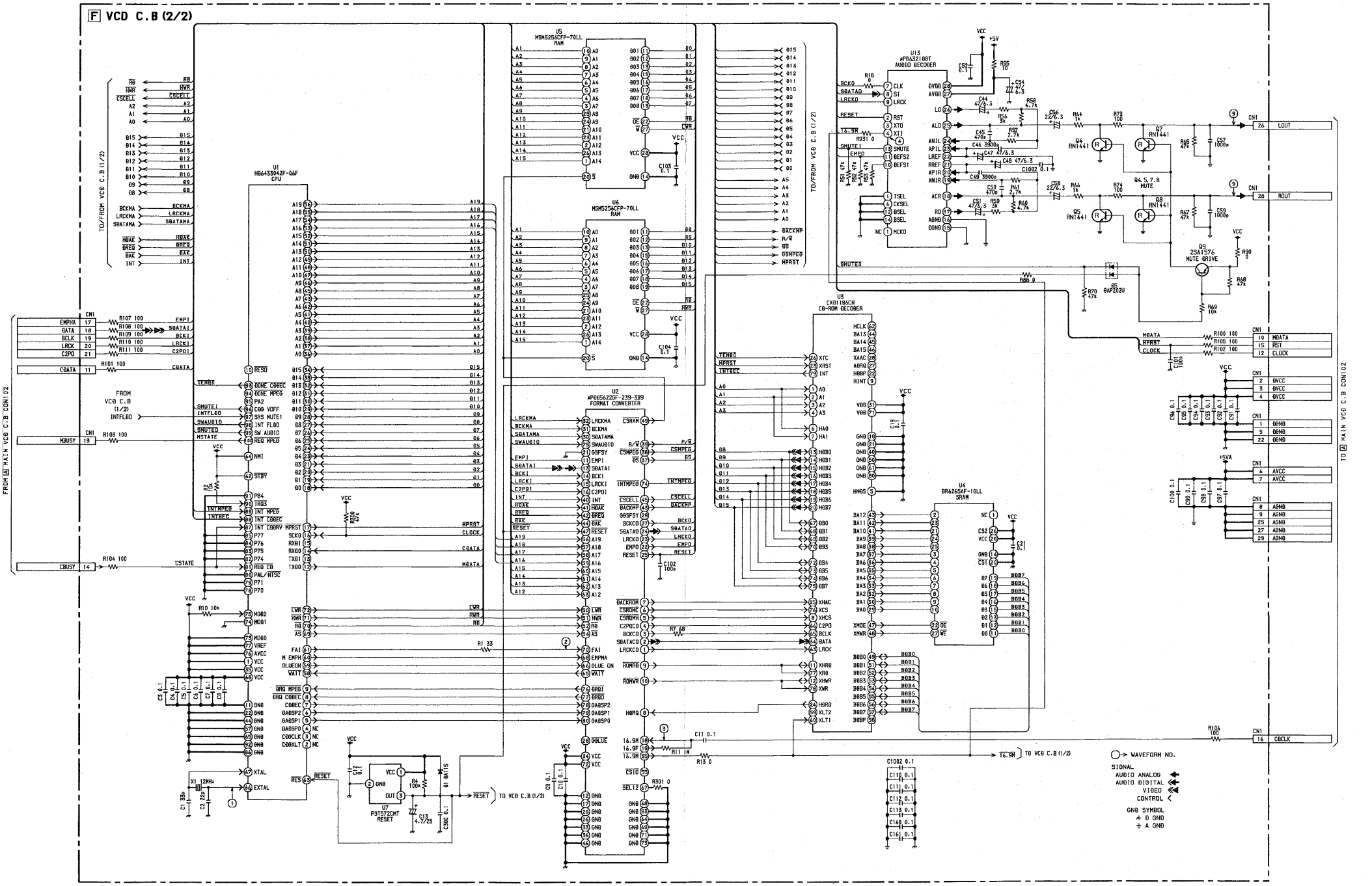


SCHEMATIC DIAGRAM-6 (V4L: MAIN VCD)



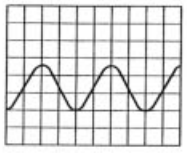

F VCD C.B (1/2)
U14
APB61010AGB-LBB
VIDEO DECODER
U18
TC514260BJ-70
16-bit DRAM
U15
TC170C100AF
VIDEO DECODER
U8
HD49507
3HC 8-bit DAC
U12
CXA1645M
RGB ENCODER
U19
TLC2932IPW
PLL
Q1
2SC4081
AMP
CN1
CVBS 00
TO
A MAIN VCD C.B
CON102
TO/FROM VCD C.B (2/2)
TO/FROM
VCD C.B (2/2)
FROM
VCD C.B (2/2)
T6.9M
INTFLB0
SDATAMA
BCKMA
LRCKMA
TO
VCD C.B
(2/2)
WAVE FORM NO.
SIGNAL
VIDEO
CONTROL
GND SYMBOL
B GND
A GND

SCHEMATIC DIAGRAM-8 (V4L: VCD 2/2)



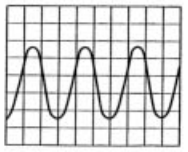
WAVE FORM

① U1 Pin ㉖ (EXTAL) VOLT/DIV: 1V TIME/DIV: 20nS



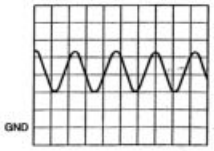
② U2 Pin ㉙ (FAI) VOLT/DIV: 1V TIME/DIV: 20nS

③ U2 Pin ⑲ (16.9M) VOLT/DIV: 1V TIME/DIV: 20nS



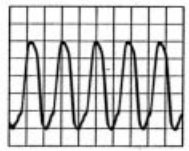
④ U13 Pin ④ (XTI) VOLT/DIV: 1V TIME/DIV: 20nS

⑤ U12 Pin ⑤ (SC IN) VOLT/DIV: 1.0V TIME/DIV: 0.1μS

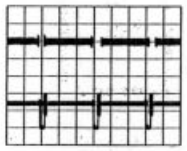


⑥ U14 Pin ㊽ (VD CLK) VOLT/DIV: 1V TIME/DIV: 20nS

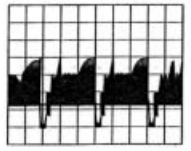
⑦ U14 Pin ㊾ (CLK) VOLT/DIV: 1V TIME/DIV: 20nS



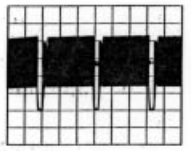
⑧ CN1 Pin ㊿ (CVBS R) VOLT/DIV: 200mV TIME/DIV: 20μS
WHITE



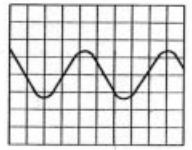
KARAOKE VOLT/DIV: 200mV TIME/DIV: 20μS



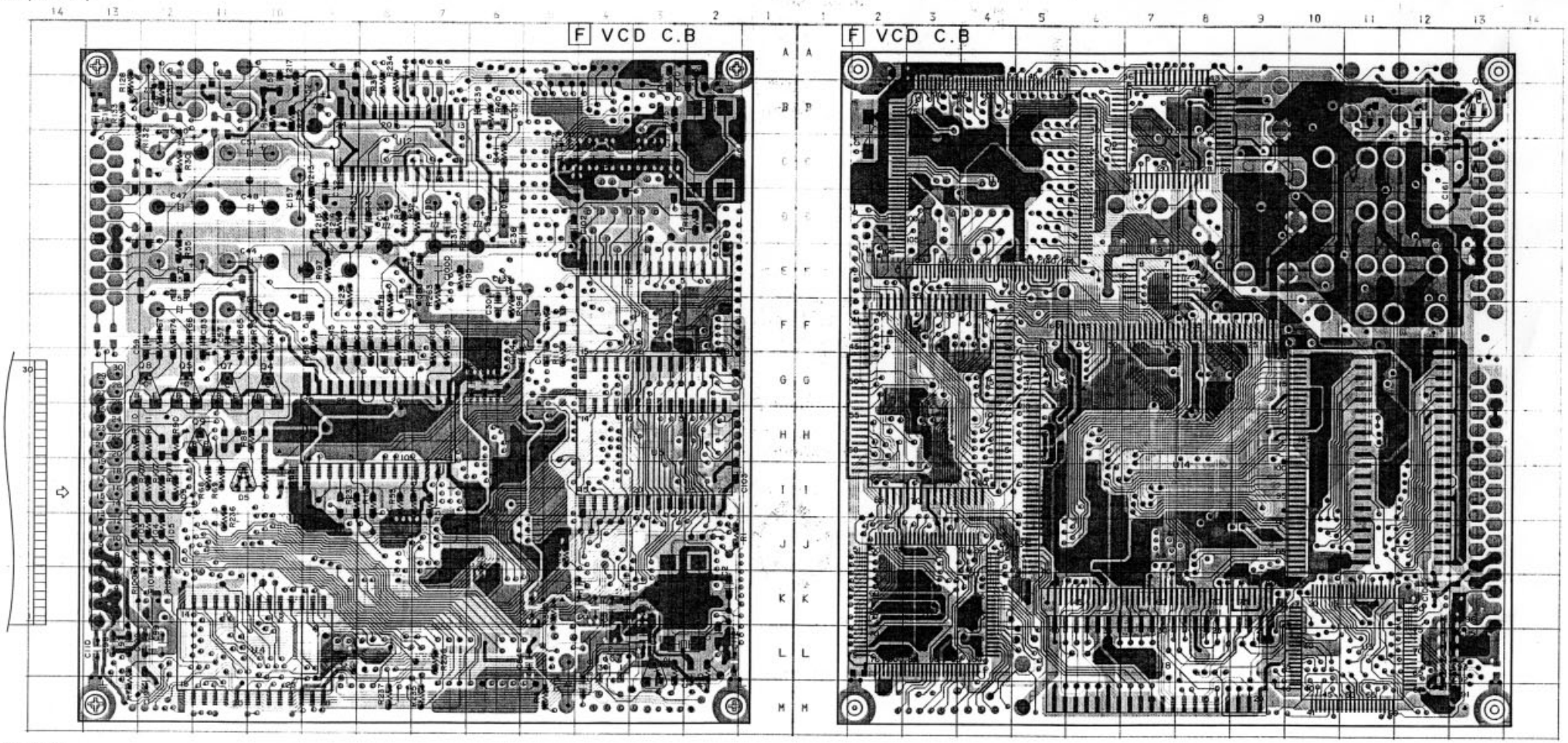
BLUE VOLT/DIV: 100mV TIME/DIV: 20μS



⑨ CN1 Pin ㊷ (L OUT) VOLT/DIV: 1.0V
CN1 Pin ㊸ (R OUT) TIME/DIV: 0.2mS
1kHz OUTPUT

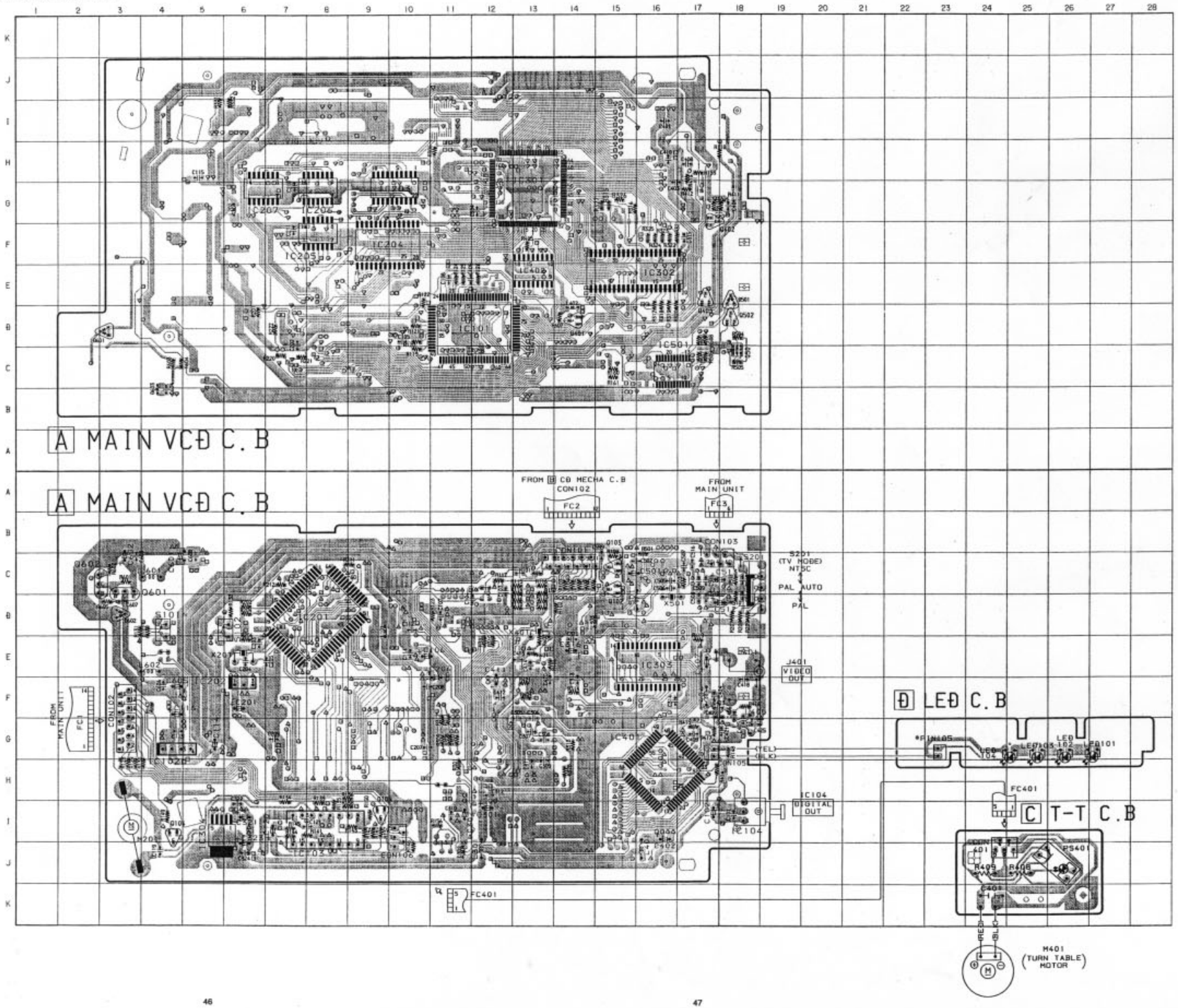


WIRING-5 (V4L: VCD)

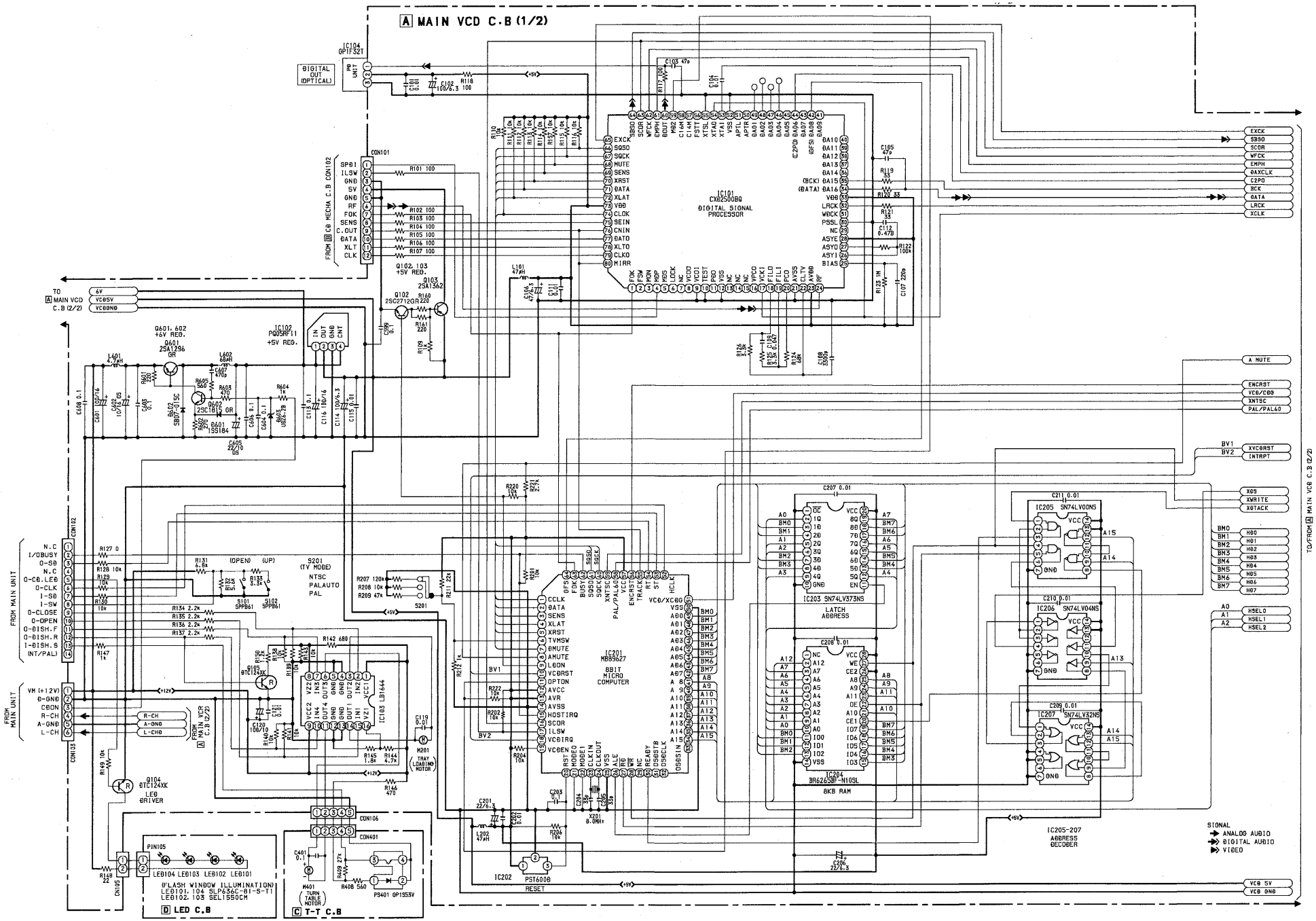


Through-Hole Note

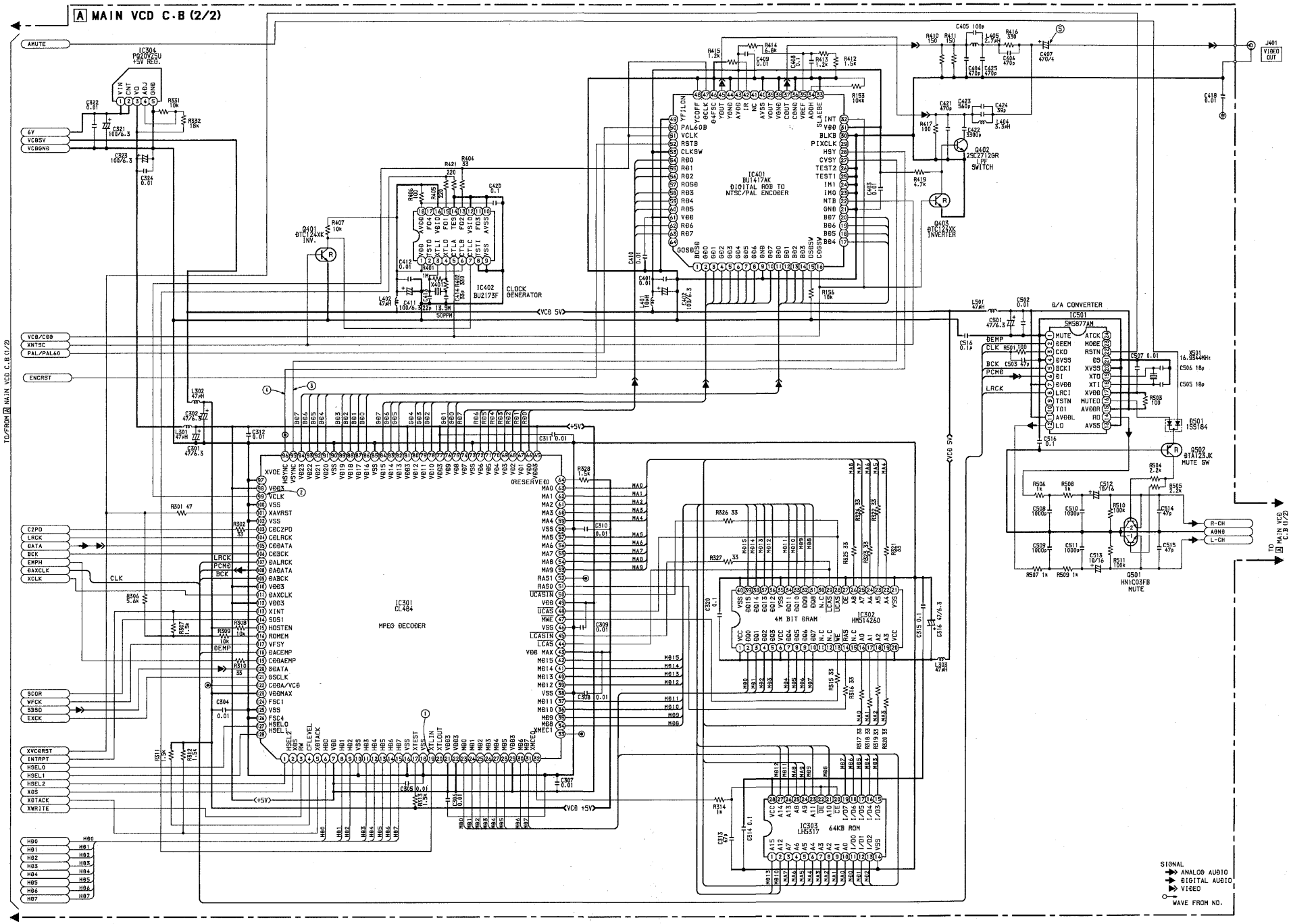
SIGNAL	VCC	+5V	A GND	D GND
○	▲	▲	●	●


A MAIN VCÐ C.B
A MAIN VCÐ C.B
FROM B CD MECHA C.B
CON102
FC2
FROM
MAIN UNIT
FC3
S201
(TV MODE)
NTSC
PAL AUTO
PAL
J401
VIDEO
OUT
IC104
DIGITAL
OUT
FROM
MAIN UNIT
FC1
CON102
FC401
Ð LEÐ C.B
LED
LED101
FC401
C T-T C.B
M401
(TURN TABLE)
MOTOR

SCHEMATIC DIAGRAM-9 (V5: MAIN VCD 1/2)



SCHEMATIC DIAGRAM-10 (V5: MAIN VCD 2/2)

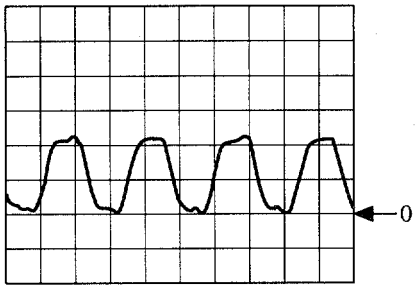


WAVE FORM

①

IC301 Pin ⑲ (GCK)
40.5MHz
VCD PLAY
TV MODE: • NTSC
• PAL
• PAL AUTO

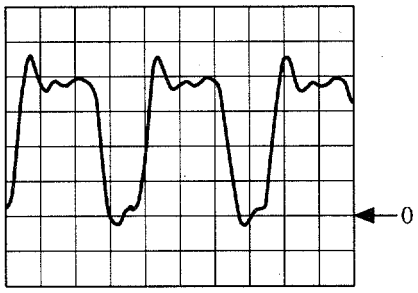
VOLT/DIV: 1V
TIME/DIV: 10nS



②

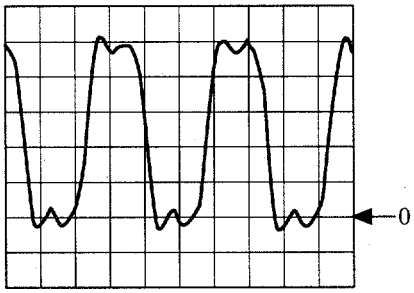
IC301 Pin ㊾ (VCLK)
27MHz±1350Hz
VCD PLAY
TV MODE: • NTSC
• PAL
• PAL AUTO

VOLT/DIV: 1V
TIME/DIV: 10nS



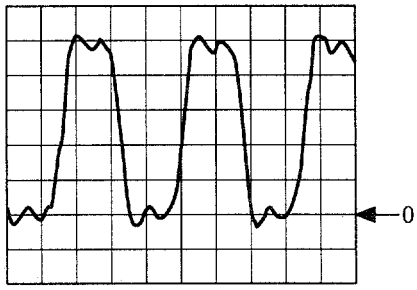
28.375MHz
CDG PLAY
TV MODE: • PAL
• PAL AUTO

VOLT/DIV: 1V
TIME/DIV: 10nS



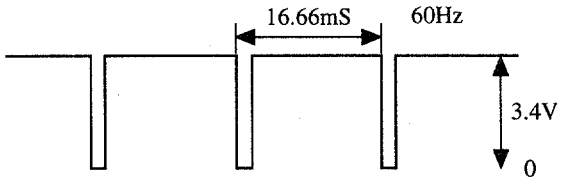
28.6363MHz
CDG PLAY
TV MODE: • NTSC

VOLT/DIV: 1V
TIME/DIV: 10nS

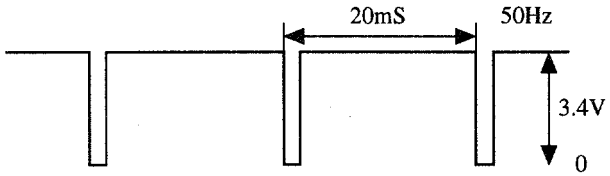


③

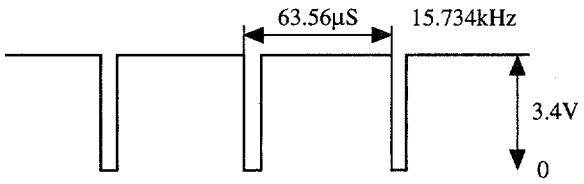
IC301 Pin ㊺ (V SYNC)
VCD, CDG PLAY
TV MODE: • NTSC
• PAL AUTO



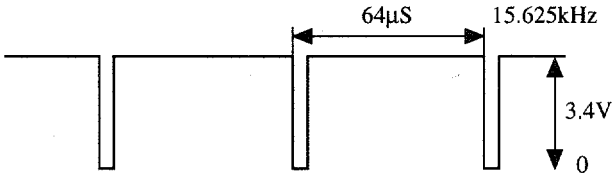
VCD, CDG PLAY
TV MODE: PAL



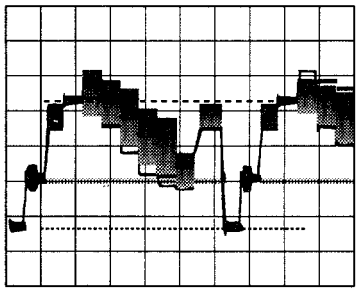
④ IC301 Pin ㊻ (H SYNC)
VCD, CDG PLAY
TV MODE: • NTSC
• PAL AUTO



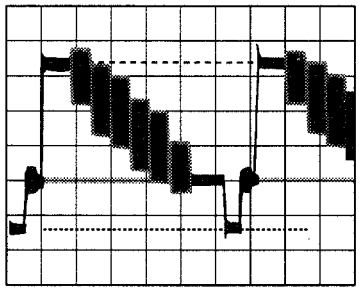
VCD, CDG PLAY
TV MODE: PAL

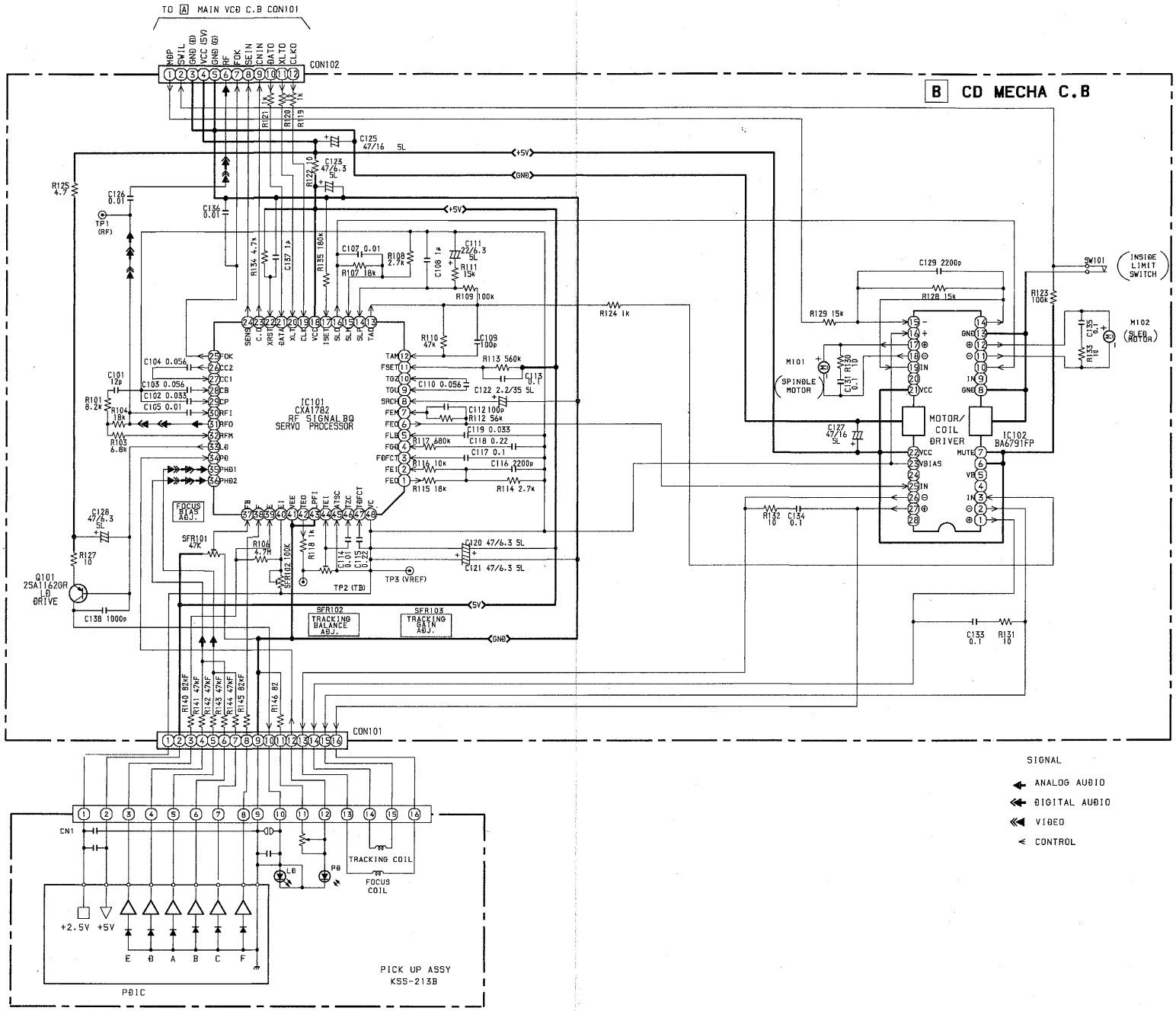


⑤ VIDEO OUT
C407 ⊖ side
CDG PLAY: CD-T03 TRACK2
TV MODE:• NTSC
VOLT/DIV: 200mV
TIME/DIV: 10µS

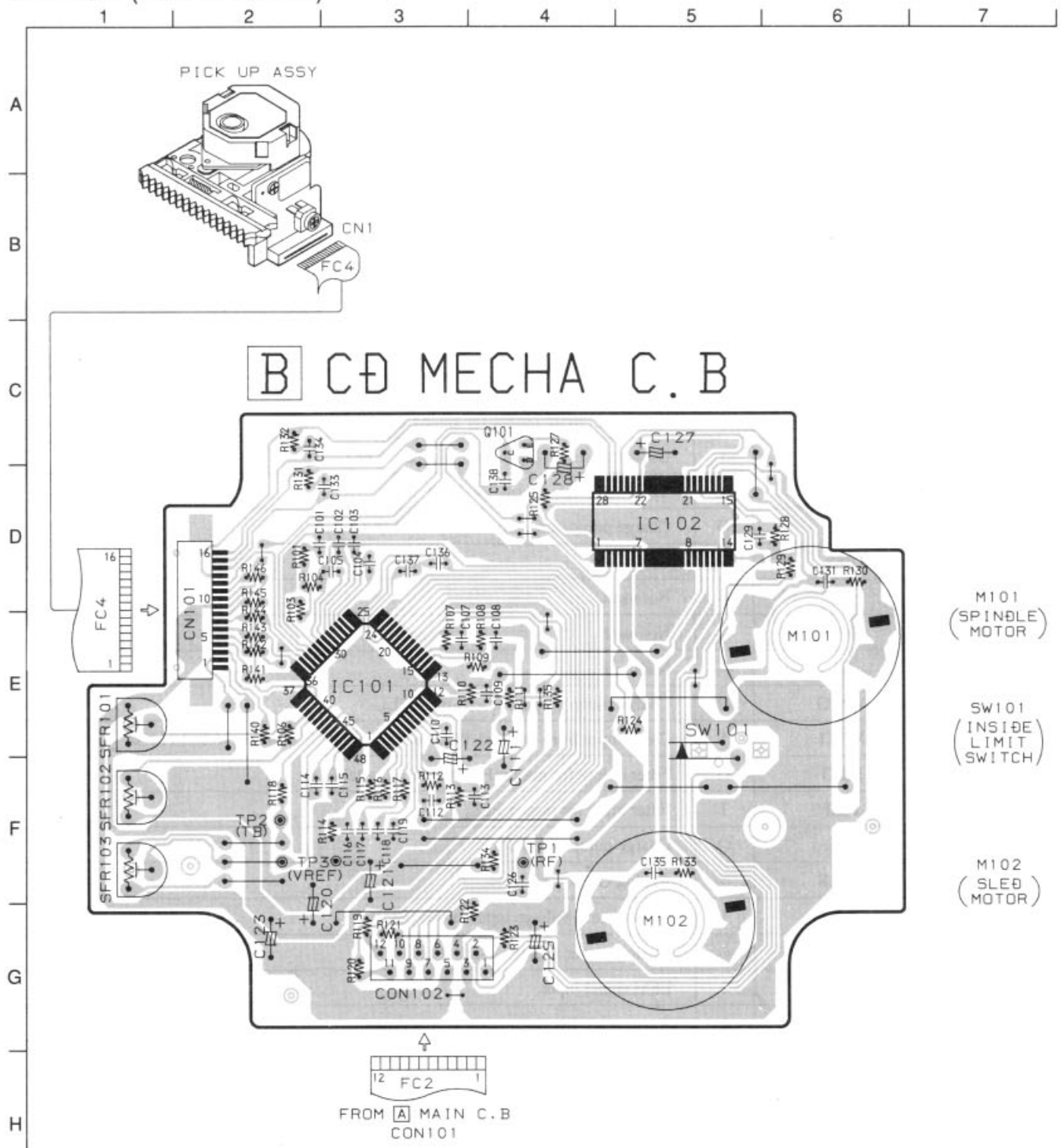


VCD PLAY: CD-T05 TRACK4
TV MODE:• NTSC
VOLT/DIV: 200mV
TIME/DIV: 10µS




TO A MAIN VCD C.B CON101
CON102
B CD MECHA C.B
IC101
CXA1782
RF SIGNAL BQ
SERVO PROCESSOR
IC102
BA6791FP
MOTOR/
COIL
DRIVER
SPINDLE
MOTOR
SLED
MOTOR
INSIDE
LIMIT
SWITCH
FOCUS
BIAS
ADJ.
SFR101
SFR102
TRACKING
BALANCE
ADJ.
SFR103
TRACKING
GAIN
ADJ.
TP1
(RF)
TP2 (TB)
TP3 (VREF)
Q101
2SA1162GR
LD
DRIVE
CON101
CN1
TRACKING COIL
FOCUS
COIL
LD
PD
+2.5V
+5V
E
D
A
B
C
F
PD IC
PICK UP ASSY
KSS-213B
SIGNAL
ANALOG AUDIO
DIGITAL AUDIO
VIDEO
CONTROL

WIRING-7 (V5: CD MECHA)



IC DESCRIPTION

IC, CXD2500BQ

Pin No.	Pin Name	I/O	Description
1	FOK	I	Focus OK input terminal. Used for SENS output and servo auto sequencer.
2	FSW	O	Spindle motor output filter selection output.
3	MON	O	Spindle motor ON-OFF control output.
4	MDP	O	Spindle motor servo control.
5	MDS	O	Spindle motor servo control.
6	LOCK	O	H output when GFS is sampled at 460 Hz and GFS is H. L output when L is continuously 8 times.
7	NC	—	Not used.
8	VCOO	O	Oscillator circuit output for analog EFM PLL.
9	VCOI	I	Oscillator circuit input for analog EFM PLL. fLOCK = 8.6436 MHz.
10	TEST	I	TEST terminal. Normally GND.
11	PDO	O	Charge pump output for analog EFM PLL.
12	VSS	—	GND.
13	NC	—	Not used.
14	NC	—	Not used.
15	NC	—	Not used.
16	VPCO	O	Charge pump output for vari-pitch PLL.
17	VCKI	I	Clock input from external VCO for vari-pitch. fc center = 16.9344 MHz.
18	FILO	O	Filter output for master PLL (slave = digital PLL).
19	FILI	I	Filter input for master PLL.
20	PCO	O	Charge pump output for
21	AVSS	—	Analog GND.
22	CLTV	I	VCO control voltage input for master.
23	AVDD	—	Analog power supply. (+3.5 V)
24	RF	I	EFM signal input.
25	BIAS	I	Asymmetry circuit constant current input.
26	ASYI	I	Asymmetry comparate voltage input.
27	ASYO	O	EFM full swing output (L = Vss, H = VDD.)
28	ASYE	I	L: asymmetry circuit OFF, H: asymmetry circuit ON.
29	NC	—	Not used.
30	PSSL	I	Audio data output mode selection input. Serial output at L, parallel output at H.
31	WDCK	O	D/A interface for 48-bit slot. Word clock f = 2 Fs.
32	LRCK	O	D/A interface for 48-bit slot. LR clock f = Fs.
33	VDD		Power supply. (+3.5 V)
34	S DATA	O	DA16 (MSB) output when PSSL = H. 48-bit slot serial data when PSSL = L. (2's COMP, MSB first).
35	BCLK	O	DA15 output when PSSL = H. 48-bit slot bit clock when PSSL = L.
36	NC	O	DA14 output when PSSL = H. 64-bit slot serial data when PSSL = L. (2's COMP, MSB first).
37	NC	O	DA13 output when PSSL = H. 64-bit slot bit clock when PSSL = L.
38	NC	O	DA12 output when PSSL = H. 64-bit slot LR clock when PSSL = L.

Pin No.	Pin Name	I/O	Description
39	GTOP	O	DA11 output when PSSL = H. GTOP output when PSSL = L.
40	XUGF	O	DA10 output when PSSL = H. XUGF output when PSSL = L.
41	XPLCK	O	DA09 output when PSSL = H. XPLCK output when PSSL = L.
42	GFS	O	DA08 output when PSSL = H. GFS output when PSSL = L.
43	RFCK	O	DA07 output when PSSL = H. RFCK output when PSSL = L.
44	C2PO	O	DA06 output when PSSL = H. C2P0 output when PSSL = L.
45	XRAOF	O	DA05 output when PSSL = H. XRAOFoutput when PSSL = L.
46	MNT3	O	DA04 output when PSSL = H. MNT3 output when PSSL = L.
47	MNT2	O	DA03 output when PSSL = H. MNT2 output when PSSL = L.
48	MNT1	O	DA02 output when PSSL = H. MNT1 output when PSSL = L.
49	MNT0	O	DA01 output when PSSL = H. MNT0 output when PSSL = L.
50	APTR	O	Aperture correction control output. H when R channel.
51	APTL	O	Aperture correction control output. H when L channel.
52	VSS	—	GND.
53	XTAI	I	Input to 16.9344 MHz X'tal oscillator circuit. or 33.8688 MHz input.
54	XTAO	O	16.9344 MHz X'tal oscillator output.
55	XTSL	I	X'tal selection input. L when X'tal is 16.9344 MHz. H when 33.8688 MHz.
56	FSTT	O	2/3 divider output of the pins 53 and 54. Does not change with vari-pitch.
57	C4M	O	4.2336 MHz output. When vari-pitch is performed, it changes too.
58	C16M	O	16.2336 MHz output. When vari-pitch is performed, it changes too.
59	MD2	I	Digital-out ON/OFF control. ON at H, OFF at L.
60	DOUT	O	Digital-out terminal.
61	EMPH	O	H output when the playback disc has emphasis. L output without emphasis.
62	WFCK	O	WFCK (Write Frame Clock) output.
63	SCOR	O	H output when S0 or S1 of the subcode sync is detected.
64	SBSO	O	Serial output of Sub P to W.
65	EXCK	I	Clock input for SBSO read out.
66	SQSO	O	SubQ 8-bit and PCM peak level data. 16-bit output.
67	SQCK	I	Clock input for SQSO readout.
68	MUTE	I	Mute at H. Release at L.
69	SENS	O	SENS output. Output to CPU.
70	XRST	I	System reset. Reset at L.
71	DATA	I	Serial data input from CPU.
72	XLAT	I	Latch input from CPU. Latches serial data at fall-down edge.
73	VDD	—	Power supply (+3.5 V).
74	CLOK	I	Serial data transfer clock input from CPU.
75	SEIN	I	Sensor input from SSP.
76	CNIN	I	Track jump number counted signal input.
77	DATO	O	Serial data output to SSP.
78	XLTO	O	Serial data latch output to SSP. Latches at fall-down edge.
79	CLKO	O	Serial data transfer clock output to SSP.
80	MIRR	I	Mirror signal input. Used for jump of 128 track or more at auto sequencer.

IC, μPD78044BGF

Pin No.	Pin Name	I/O	Description
1	DO ON	O	Digital output. ON/OFF output.
2~7	NC	—	Not used.
8	VDD	—	PWR. +5 V power supply.
9	CM CLK	I/O	Serial clock I/O.
10	C DATA	O	Serial data output.
11	M DATA	I	Serial data input.
12	O-CLK	O	DSP serial clock output.
13	O-XLT	O	DSP serial latch output.
14	O-SQCLK	O	DSP sub Q read-out clock output.
15	O-DATA	O	DSP serial data output.
16	I-SQDATA	I	DSP sub Q data input.
17	$\overline{\text{RESET}}$	I	System reset input.
18	I-SENS	I	DSP SENS input.
19	XRST	O	CD system reset output.
20	AVSS	—	PWR. GND potential of A/D converter input.
21	I-FOK	I	ASP FOK input.
22	I-GFS	I	DSP GFS input.
23	—	—	Connected GND.
24	I-ILSW	I	Pickup limit switch input.
25	I-OCSW	I	Tray OPEN/CLOSE switch input.
26~28	—	—	Connected GND.
29	AVDD	—	PWR. Analog power supply of A/D converter input.
30	AVREF	I	PWR. Reference voltage input of A/D converter input.
31	—	—	Connected GND.
32	NC	—	Open terminal.
33	VSS	—	PWR. GND potential.
34	X1	I	CLK. Terminal for 4.19 MHz clock oscillator.
35	X2	O	CLK. Terminal for 4.19 MHz clock oscillator.
36~38	NC	—	Not used.
39	$\overline{\text{C-BUSY}}$	O	MPEG status output.
40	MSTBY	I	Main microprocessor status input.
41	CLOCK	O	Main microprocessor serial clock output.
42	DATA	O	Main microprocessor serial data output.
43	D-REQ	O	Main microprocessor status output.
44	I-KEY	I	Main microprocessor serial data input.
45	SCOR	I	DSP SCOR input.
46	$\overline{\text{M-BUSY}}$	I	MPEG status signal input.
47	—	—	Connected GND.
48	IC	—	PWR. Connected to Vss.
49	MUTE L	O	L channel analog mute output.
50	MUTE R	O	R channel analog mute output.

Pin No.	Pin Name	I/O	Description
51	DSENS	I	Turntable sensor input.
52	VDD	—	PWR. +5 V power supply.
53～64	NC	—	Not used.
65	O-TOPN	O	Tray OPEN output.
66	O-CLS	O	Tray CLOSE output.
67	O-DFWD	O	Turntable forward rotation output.
68	O-DRVS	O	Turntable reverse rotation output.
69, 70	NC	—	Not used.
71	VLOAD	—	PWR. -27 V power supply for FL pull-down.
72～76	NC	—	Not used.
77	VCD	O	VIDEO CD selection output.
78	$\overline{\text{CD FUNC}}$	O	CD function selection output.
79	G-MUT	O	CDG mute output.
80	CD ON	O	FL. Digit output for FL display.

IC, LC7872E

Pin No.	Pin name	I/O	Description
1, 2	S1, S2	—	DSP select pin for CD. (Connected to VDD)
3	SBCK	O	Subcode read/write clock.
4	SFSY	I	Subcode frame sync signal.
5	PW	I	Subcode read/write data.
6	SBSY	I	Subcode block sync signal.
7	VDD1	—	Power supply for digital block. (Connected to +5V)
8	CE	I	Control pin when serial input or serial output. (Connected to GND)
9	DO	O	Serial data output. (Connected to GND)
10	DI	I	Serial data input. (Connected to GND)
11	CL	I	Clock when inputting/outputting serial data. (Connected to GND)
12	MUTE	I	Control signal disabling the subcode.
13	VSS1	—	GND for digital block.
14	$\overline{WE}$	O	DRAM control pin.
15	$\overline{RAS}$	O	DRAM control pin.
16～23	A0～A7	O	DRAM address pin.
24	DB0	I/O	DRAM data pin.
25	$\overline{CAS}$	O	DRAM control pin.
26	DB1	I/O	DRAM data pin.
27	$\overline{DE}$	O	DRAM control pin.
28	DB2	I/O	DRAM data pin.
29	DB3	I/O	DRAM data pin.
30	CE	I	"L": Normal mode "H": Color bar output (Not used)
31	CDGM	O	"H" output when CDG disk. (Not used)
32	TRANS0	O	Transparency digital output. (Not used)
33	TRANS1	O	Transparency digital output. (Not used)
34	TRANS2	O	Transparency digital output. (Not used)
35	TRANS3	O	Transparency digital output. (Not used)
36	TRANS4	O	Transparency digital output. (Not used)
37	TRANS5	O	Transparency digital output. (Not used)
38	VSS2	—	Composite video DAC GND pin.
39	VDD2	—	Composite video DAC power supply pin. (Connected to +5V)
40	BIAS	O	Capacitor connecting pin for eliminating ripple.
41	VIDEO	O	Composite video output pin (8-bit DAC output).
42	TEST	I	Test pin. Set to "L" normally. (Connected to GND)
43	LINE	I	When NP2 pin is "H": H: 263H L: 262H When NP2 pin is "L": H: 312H L: 314H (Not used)
44	FSCIN	I	Subcarrier clock input pin. (feedback resistor is built in) (Connected to GND)
45	VSYNC	O	Vertical sync signal output pin. (Not used)
46	TEST1	I	Test pin. Set to "L" normally. (Connected to GND)
47	YS	O	Superimpose control output. (Not used)
48	$\overline{CSTNC}$	O	Composite sync signal output. (Not used)

Pin No.	Pin name	I/O	Description
49	GND	—	GND.
50	EFLG	O	Error status monitor pin. (Not used)
51	FSX	O	For error status monitor trigger. (Not used)
52	DEN	I	Disk information display enable. H: BGC L: Enable (Connected to GND)
53	PALID	I	External control pin when superimposing with PAL (pull-up resistor is built in). (Not used)
54	VDD3	—	Digital power supply (+5V)
55	FSC	O	Subcarrier clock output. NTSC mode: 3.579545 MHz PAL mode: 4.433619 MHz (Not used)
56	VDD4	—	Digital power supply (+5V)
57	$\overline{\text{RESET}}$	I	Reset input pin.
58	N/$\overline{\text{P}}$1	I	NTSC/PAL selection pin. (RGB encoder) "H": NTSC "L": PAL
59	N/$\overline{\text{P}}$2	I	NTSC/PAL selection pin. (CD-G decoder) "H": NTSC "L": PAL
60	SON	I	Superimpose ON/OFF pin. (Connected to GND)
61	XIN2	I	Crystal oscillator 17.734476 MHz. (for PAL)
62	XOUT2	O	Crystal oscillator 17.734476 MHz. (for PAL)
63	XIN1	I	Crystal oscillator connection 14.31818 MHz. (for NTSC)
64	XOUT1	O	Crystal oscillator connection 14.31818 MHz. (for NTSC)

IC, CXA1782BQ

Pin No.	Pin name	I/O	Description
1	FEO	O	Focus error amplifier output pin. This pin is connected to the FZC comparator input internally.
2	FEI	I	Focus error input pin.
3	FDFCT	I	Capacitor connection pin for time constant used when there is defect.
4	FGD	I	This pin is connected to GND via capacitor when high frequency gain of the focus servo is attenuated.
5	FLB	I	This is a pin where the time constant is externally connected to raise the low frequency gain of the focus servo.
6	FEO	O	Focus drive output.
7	FEM	I	Focus amplifier inverted input pin.
8	SRCH	I	This is a pin where the time constant is externally connected to generate the focus search waveform.
9	TGU	I	This is a pin where the selection time constant is externally connected to set the tracking servo the high frequency gain.
10	TG2	I	This is a pin where the selection time constant is externally connected to set the tracking high frequency gain.
11	FSET	I	Pin for setting peak of the phase compensator of the focus tracking.
12	TAM	I	Tracking amplifier inverted input pin.
13	TAO	O	Tracking drive output.
14	SLP	I	Sled amplifier non-inverted input pin.
15	SLM	I	Sled amplifier inverted input pin.
16	SLO	O	Sled drive output.
17	ISET	I	The current which determines height of the focus search, track jump and sled kick is input.
18	VCC	—	+ 5 V power supply pin.
19	CLK	I	Serial data transfer clock input from CPU.
20	XLT	I	Latch input from CPU.
21	DATA	I	Serial data input from CPU .
22	XRST	I	Reset input pin. Reset at L.
23	COUT	O	Signal output to count the number of tracks.
24	SENS	O	FZC, DFCT, TZC, Gain or BAL is output depending on the command from CPU .
25	FOK	O	Output pin of the focus OK comparator.
26	CC2	O	Input pin where the DEFECT bottom hold output is capacitance coupled.
27	CC1	I	DEFECT bottom hold output pin.
28	CB	I	This is a pin where the DEFECT bottom hold capacitor is connected.
29	CP	I	This is a pin where the MIRR hold capacitor is connected and MIRR comparator non-inverted signal is input.
30	RFI	I	Input pin where the RF summing amplifier output is capacitance coupled.
31	RFO	O	RF summing amplifier output pin. (Eye pattern check point)
32	RFM	I	RF summing amplifier inverted input pin. Gain of RF amplifier is determined by the resistor connected between RFO and this pin.

Pin No.	Pin name	I/O	Description
33	LD	O	APC amplifier output pin.
34	PHD	I	APC amplifier input pin.
35~36	PHD1~2	I	RF I-V amplifier inverted input pin. These pins are connected to the A+C and B+D pins of the optical pickup.
37	FE BIAS	I	Bias adjustment pin of the focus error amplifier.
38~39	F~E	I	F and E IV amplifier non-inverted input pins. These pins are connected to the F and E of the optical pickup.
40	EI	—	Gain adjustment pin of the I-V amplifier E.
41	VEE	—	GND connection pin
42	TEO	O	Tracking error amplifier output pin. E-F signal is output.
43	LPFI	I	BAL adjustment comparator input pin.
44	TEI	I	Tracking error input pin.
45	ATSC	I	Window comparator input pin for detecting ATSC.
46	TZC	I	Tracking zero-cross comparator input pin.
47	TDFCT	I	Capacitor connection pin for the time constant used when there is defect.
48	VC	O	DC voltage output pin of VREF. (VDD/2)

IC, CL480

Pin No.	Pin Name	I/O	Description
1	HSEL2	I	Host address bus.
2	-DS	I	Data strobe.
3	R/-W	I	Read/write.
4	CFLEVEL	O	Coded data FIFO level status. Open drain.
5	-DACK	O	Host data acknowledge. Open drain.
6	HD0	I/O	Host data bus.
7	VDD3	—	Power supply pin. Used in 3.3 V.
8, 9	HD1, HD2	I/O	Host data bus.
10	VSS	—	GND.
11~15	HD3~HD7	I/O	Host data bus.
16	VSS	—	GND.
17	-TEST	I	Test terminal. Normally fixed to High.
18	VSS	—	GND.
19	XTL IN	I	Global clock. 40.5 MHz.
20	XTL OUT	O	Global clock. 40.5 MHz.
21, 22	VDD3	—	Power supply pin. Used in 3.3 V.
23~28	MD0~MD5	I/O	Memory data bus.
29	VDD3	—	Power supply pin. Used in 3.3 V.
30, 31	MD6, MD7	I/O	Memory data bus.
32, 33	-MCE0, -MCE1	O	Chip enable.
34~37	MD8~MD11	I/O	Memory data bus.
38	VSS	—	GND.
39~42	MD12~MD15	I/O	Memory data bus.
43	VDDMAX	—	Power supply pin. Used in 5.0 V.
44	-LCAS	O	Lower digit, column address strobe.
45	-LCASIN	I	Lower digit, data latch enable.
46	VSS	—	GND.
47	-MWE	O	Write enable.
48	-UCAS	O	Higher digit, column address strobe.
49	VDD3	—	Power supply pin. Used in 3.3 V.
50	-UCASIN	I	Higher digit, data latch enable.
51, 52	RAS0, RAS1	O	Lower address strobe.
53~57	MA9~MA5	O	Memory address bus.
58	VSS	—	GND.
59~63	MA4~MA0	O	Memory address bus.
64	RESERVED	—	Reserved.
65	VDD3	—	Power supply pin. Used in 3.3 V.
66~72	VD0~VD6	O	Pixel data bus. RGB or YCbCr format.
73	VSS		GND.
74~76	VD7~VD9	O	Pixel data bus. RGB or YCbCr format.
77	VDD3	—	Power supply pin. Used in 3.3 V.

Pin No.	Pin Name	I/O	Description
78~80	VD10~VD12	O	Pixel data bus. RGB or YCbCr format.
81	VDD3		Power supply pin. Used in 3.3 V.
82~84	VD13~VD15	O	Pixel data bus. RGB or YCbCr format.
85	VSS	—	GND.
86~89	VD16~VD19	O	Pixel data bus. RGB or YCbCr format.
90	VSS	—	GND.
91~94	VD20~VD23	O	Pixel data bus. RGB or YCbCr format.
95	-VSYNC or CSY	I/O	Vertical sync signal.
96	-HSYNC	I/O	Horizontal sync signal.
97	-VOE	I	Video output enable.
98	VDD3	—	Power supply pin. Used in 3.3 V.
99	VCLK	I/O	Video clock.
100	VSS	—	GND.
101	-RESET	I	Hardware reset.
102	VSS	—	GND.
103	CD-C2PO	I	Data error. Used during CD-ROM data input.
104	CD-LRCK	I	LR clock.
105	CD-DATA	I	Serial data input from CD-DSP.
106	CD-BCK	I	Bit clock from CD decoder.
107	DA-LRCK	O	LR clock.
108	DA-DATA	O	Bit serial audio sample signal.
109	DA-BCK	O	Audio bit clock.
110	VDD3	—	Power supply pin. Used in 3.3 V.
111	DA-XCLK	I	External audio frequency clock.
112	VDD3	—	Power supply pin. Used in 3.3 V.
113	-INT	O	Interrupt request.
114	RESERVED	—	Reserved.
115	HOST_ENA	I	Host enable.
116	RAM_ENA	I	Boot ROM enable.
117	RESERVED	—	Reserved.
118	DAC_EMP	O	Output emphasis flag.
119	CDDA_EMP	I	Input emphasis flag.
120	RESERVED	—	Reserved.
121	-FMV_DET	O	FMV detection. L: FMV detected.
122	CDDA/VCD	O	Input data identification. H: CDDA. L: video CD.
123	VDDMAX	I	Power supply pin. Used in 5.0 V.
124	RESERVED	—	Reserved.
125	VSS	—	GND.
126	RESERVED	—	Reserved.
127, 128	HSEL0, HSEL1	I	Host address bus.

IC, CXD1178Q

Pin No.	Pin Name	I/O	Description
1~8	R0~R7	I	Digital input.
9~16	G0~G7		
17~24	B0~B7		
25	BLK	I	Blanking pin. No signal at "H" (Output 0V). Output condition at "L".
26	$\overline{CE}$	I	Chip enable pin. No signal (Output 0V) at "H" and minimizes power consumption.
27	RCK	I	Clock pin. Moreover all input pins are TTL-CMOS compatible.
28	GCK		
29	BCK		
30, 31	DVSS	—	Digital GND.
32	VB	O	Connect a capacitor of about 0.1μF.
33	AVSS	—	Analog GND.
34	VREF	I	Set full scale output value.
35	IREF	I	Connect a resistance 16 times "16R" that of output resistance value "R".
36	$\overline{RO}$	O	Inverted current output pin. Normally dropped to analog GND.
37	RO	O	Current output pin. Voltage output can be obtained by connecting a resistance.
38	$\overline{GO}$	O	Inverted current output pin. Normally dropped to analog GND.
39	GO	O	Current output pin. Voltage output can be obtained by connecting a resistance.
40	$\overline{BO}$	O	Inverted current output pin. Normally dropped to analog GND.
41	BO	O	Current output pin. Voltage output can be obtained by connecting a resistance.
42	VG	I	Connect a capacitor of about 0.1μF.
43~46	AVDD	—	Analog VDD.
47, 48	DVDD	—	Digital VDD.

IC, MC68HC705

Pin No.	Pin Name	I/O	Description
1	RST	I	Reset.
2	IRQ	I	MPEG DECODER request signal.
3	VPP	—	ROM write power.
4~11	PA7~PA0	I/O	MPEG DECODER data bus 7~0.
12~14	PB0~PB2	O	MPEG DECODER register select 0~2.
15	PB3	O	MPEG DECODER data R/W select.
16	PB4	O	MPEG DECODER data strobe.
17	PB5	I	MPEG DECODER data acknowledge.
18	PB6	I	CD-I bit stream detect.
19	PB7	I	CD DA/VCO select.
20	VSS	—	Power ground.
21	PC7	I	MPEG DECODER FIFO status.
22, 23	PC6, PC5	—	Not used.
24	PC4	O	MPEG DECODER reset signal.
25, 26	PC3, PC2	—	Not used.
27, 28	PC1, PC0	O	Key scan out 1, 0.
29	RDI	—	Not used.
30	TDO		
31~34	PD2~PD5	I	Key scan input 0~3.
35	TCMP	O	Remote data out.
36	PD7	—	Not used.
37	CAP	I	Remote data in.
38, 39	OSC2, OSC1	I	X_tal in.
40	VDD	—	Power 5V.

IC, μPD6376

Pin No.	Pin Name	I/O	Description
1	FS-SEL	I	As this terminal is "Low" or open, L-ch data and R-ch data are inputted for serial data by the pin 15. As this terminal is "High", L-ch data is inputted by the pin 15, R-ch data is inputted by the pin 14. (Pull-downed by the 100 kΩ resistance in IC.)
2	D. GND	—	Ground terminal for the logic circuit.
3	NC	—	—
4	D. VDD	—	Power supply terminal for the logic circuit .
5	A. GND	—	Ground terminal for the analog circuit.
6	R. OUT	O	Output terminal for the right analog signal.
7, 8	A. VDD	—	Power supply terminal for the analog circuit.
9, 10	R. REF, L. REF	—	Operational Amplifier reference bias terminal. Normally connected to A.GND via a capacitor.
11	L. OUT	O	Output terminal for the left analog signal.
12	A. GND	—	Ground terminal for the analog circuit.
13	LRCK	I	As the pin 1 is "Low" or open, this is input terminal for left/right identification signal. As the pin 1 is "High", this is input terminal for word identification signal of input data.
14	LRSEL	I	As the pin 1 is "Low" or open, this is left/right selection terminal for LRCK signal. At "High" of LRCK signal, set LRSEL pin at "Low" for L-ch DATA input. At "Low" of LRCK signal, set LRSEL pin at "High" for L-ch DATA input. As the pin 1 is "High", this is input terminal for R-ch serial data.
15	DATA	I	As the pin 1 is "Low" or open, this is input terminal for L-ch and R-ch serial data. As the pin 1 is "High", this is input terminal for L-ch serial data.
16	BCK	I	Input terminal for read clock of serial input data.

IC, CXA1645M

Pin No.	Pin Name	I/O	Description
1	GND	—	GND.
2	RIN	I	Analog RGB input terminals.
3	GIN		
4	BIN		
5	NC	—	N. C.
6	SCIN	I	Subcarrier input terminal.
7	NPIN	I	NTSC, PAL mode select terminal. NTSC: Vcc, PAL: GND.
8	BFOUT	O	Output terminal to monitor the BF pulse. Unable to drive 75 Ω load.
9	YCLPC	—	External time constant for Y signal clamp is connected to this terminal.
10	SYNCIN	I	Composite sync signal input terminal. Input at TTL level. SYNC period at L (≦ 0.8 V). H (≧ 2.0 V).
11	NC	—	N. C.
12	VCC	—	Power supply terminal.
13	IREF		Terminal which determines internal reference current.
14	VREF	—	Internal reference voltage terminal.
15	COUT	O	Chroma signal output terminal.
16	YOUT	O	Y signal output terminal.
17	YTRAP	I	Terminal to reduce cross-color due to subcarrier frequency component included in the Y signal.
18	FO	I	fo adjustment terminal of internal filter. The following resistor is connected between GND depending upon NTSC or PAL mode. NTSC: 20 kΩ (±1%) PAL: 16 kΩ (±1%).
19	VCC	—	Power supply terminal.
20	CVOUT	O	Composite video signal output terminal.
21	BOUT	O	Analog RGB signal output terminal
22	GOUT		
23	ROUT		
24	GND	—	GND.

IC, HD6433042F06F

Pin No.	Pin Name	I/O	Description
1	VCC	I	Power supply.
2	CDG DIN	O	CD-G decoder serial data signal.
3	CDG XLT	O	CD-G decoder latch signal.
4	CDG CLK	O	CD-G decoder clock signal.
5~7	GADSP0~2	O	Gate array DSP format 0~2.
8	$\overline{\text{DRQ CDDEC}}$	I	CD-ROM decoder data request signal.
9	$\overline{\text{DRQ MPEG}}$	I	MPEG decoder data request signal.
10	$\overline{\text{RESO}}$	O	External reset output.
11	GND	I	GND.
12	TXD0	O	Serial interface (RXD).
13	TXD1	O	CXD for test.
14	RXD0	I	Serial interface (RXD).
15	RXD1	I	RXD for test.
16	SCK0	I/O	Serial interface (SCK).
17	$\overline{\text{MPRST}}$	O	Peripheral reset. L: RESET ON.
18~21	D0~D3	I/O	Data bus 0~3.
22	GND	I	GND.
23~34	D4~D15	I/O	Data bus 4~15.
35	VCC	I	Power supply.
36~43	A0~A7	O	Address bus 0~7.
44	GND	I	GND.
45~56	A8~A19	O	Address bus 8~19.
57	GND	I	GND.
58	$\overline{\text{WAIT}}$	I	External wait signal.
59	GLUE ON	O	DMA glue circuit enable 0: OFF. 1: ON.
60	M EMPH	O	MPEG AUDIO emphasis 0: OFF. 1: ON.
61	FAI	O	System clock output.
62	$\overline{\text{STBY}}$	I	Standby. (Hardware standby mode at low level).
63	$\overline{\text{RES}}$	I	Reset input. (Reset at low).
64	NMI	I	Non-maskable interrupt. (Non-maskable interrupt is requested).
65	GND	I	GND.
66	EXTAL	I	External crystal is connected to this pin.
67	XTAL	I	External crystal is connected to this pin.
68	VCC	I	Power supply.
69	$\overline{\text{AS}}$	O	Address strobe signal.
70	$\overline{\text{RD}}$	O	External address read enable signal.
71	$\overline{\text{HWR}}$	O	External address high write enable signal.
72	$\overline{\text{LWR}}$	O	External address low write enable signal.
73~75	MOD0~MOD2	I	Mode terminal. Operating mode is set using this terminal.
76	AVCC	I	Power supply terminal of A/D converter and D/A converter.
77	VREF	I	Reference voltage input to A/D converter and D/A converter.

Pin No.	Pin Name	I/O	Description
78, 79	P70, P71	I	IN port 0, 1 for test.
80	PAL/$\overline{\text{NTSC}}$	I	PAL/NTSC status 0: NTSC. 1: PAL.
81	$\overline{\text{REQ CD}}$	I	Serial interface (REQ_CD).
82~85	P74~P77	I	Reserve.
86	AGND	I	GND terminal of A/D converter and D/A converter.
87	$\overline{\text{INT CDDRV}}$	I	Serial interface interrupt.
88	$\overline{\text{INT CDDEC}}$	I	CD-ROM decoder interrupt.
89	$\overline{\text{INT MPEG}}$	I	MPEG decoder interrupt.
90	$\overline{\text{IRQ3}}$	I	Reserve.
91	P84	I	Reserve.
92	GND	I	GND.
93	$\overline{\text{DONE CDDEC}}$	O	CD-ROM decoder DONE signal.
94	$\overline{\text{DONE MPEG}}$	O	MPEG decoder DONE signal.
95	CDG VOFF	O	CD-G decoder video OFF signal. 1: VOFF.
96	SYS MUTE1	O	Audio mute 1 signal. 1: mute ON.
97	INTFLDO	I	EVEN/OFF input signal. 0: EVEN. 1: 0DD.
98	SW AUDIO	O	Audio select signal. 0: CD-G/DA. 1: MPEG.
99	$\overline{\text{SYS MUTE0}}$	O	Audio mute 0 signal. 0: mute on.
100	$\overline{\text{REQ MPEG}}$	O	Serial interface (REQ MPEG)

IC, µPD65622GF-239-3B9

Pin No.	Pin Name	I/O	Description
1	LRCKCD	O	Main data signal to CXD1186.
2	SDATACD	O	
3	BCKCD	O	
4	C2POCD	O	
5	$\overline{\text{CSROMH}}$	O	Chip select signal to CXD1186 (host side).
6	$\overline{\text{CSROMC}}$	O	Chip select signal to CXD1186 (CPU side).
7	$\overline{\text{DACKROM}}$	O	DMA acknowledge signal to CXD1186.
8	HDRQ	I	Data transfer request signal from CXD1186. This signal is active high.
9	$\overline{\text{ROMRD}}$	O	Read/write signal to CXD1186.
10	$\overline{\text{ROMWR}}$	O	Read/write signal to CXD1186.
11	EMPHI	I	This signal allows inputting the main data from the CD drive.
12	GND	—	GND.
13	SDATAI	I	This signal allows inputting the main data from the CD drive.
14	BCKI	I	
15	LRCKI	I	
16	C2POI	I	
17	GND	—	GND.
18	16.9M	I	16.9344 MHz oscillator circuit input signal.
19	16.9F	O	16.9344 MHz oscillator circuit output signal.
20	GND	—	GND.
21	GSFSY	I	Write frame clock signal used to input the sub data from CD drive.
22	EMPO	O	Main data signal to CXD1186.
23	LRCKO	O	Audio data signal to audio DAC.
24	SDATAO	O	Audio data signal to audio DAC.
25	RESET	O	Active high reset signal.
26	GND	—	GND.
27	BCKCO	O	Audio data signal to audio DAC.
28	$\overline{\text{GGLUE}}$	I	The input signal which makes the glue circuit valid from GSFSY input.
29	$\overline{\text{GGSFSY}}$	O	Not used.
30	SDATAMA	I	Audio data signal from µPD61010.
31	BCKMA	I	
32	LRCKMA	I	
33	GND	—	GND.
34	VCC	—	Vcc.
35	$\overline{\text{16.9M}}$	O	16.9344 MHz output signal.
36	GND	—	GND.
37	$\overline{\text{DS}}$	O	Control signal to µPD61010.
38	$\overline{\text{CSMPEG}}$	O	Chip select signal to CXD1186.
39	$\overline{\text{R/W}}$	O	Control signal to µPD61010.
40	INT	I	Interrupt request signal from µPD61010. This signal is active high.
41	$\overline{\text{HDAK}}$	I	Data acknowledge signal from µPD61010.

Pin No.	Pin Name	I/O	Description
42	$\overline{\text{DREQ}}$	I	DRAM data transfer request signal from μPD61010.
43	$\overline{\text{DACKMP}}$	O	DMA acknowledge signal to μPD61010.
44	$\overline{\text{DAK}}$	I	Bit stream data transfer request signal from μPD61010.
45	$\overline{\text{CSCELL}}$	O	Chip select signal to standard cell.
46	GND	—	GND.
47	$\overline{\text{RESET}}$	I	System reset signal.
48	GND	—	GND.
49	$\overline{\text{CSRAM}}$	O	Chip select signal to the system RAM.
50	$\overline{\text{LWR}}$	I	Lower data write signal from CPU.
51	$\overline{\text{HWR}}$	I	Upper data write signal from CPU.
52	$\overline{\text{RD}}$	I	Data read signal from CPU.
53	GND	—	GND.
54	$\overline{\text{AS}}$	I	Address strobe signal from CPU.
55	$\overline{\text{CSIO}}$	O	Optional chip select signal.
56～63	A19～A12	I	Address signal from CPU.
64	GND	—	GND.
65	$\overline{\text{WAIT}}$	O	Wait signal to CPU.
66	GLUEON	I	This signal makes the glue logic valid in order to prevent CPU DMAC from trouble. This circuit is made valid at high.
67	$\overline{\text{SEL12}}$	I	Input signal to select 12 MHz or 16 MHz CPU clock.
68	EMPMA	I	Audio data signal from μPD61010.
69	GND	—	GND.
70	FAI	I	Basic clock signal (12 MHz) from CPU.
71	GND	—	GND.
72	VCC	—	Vcc.
73	GND	—	GND.
74	$\overline{\text{INTMPEG}}$	O	Interrupt request signal to CXD1186.
75	SWAUDIO	I	Selection signal between MPEG audio and CD-DA audio signals.
76	$\overline{\text{DRQ1}}$	O	DMA transfer request signal to μPD61010.
77	$\overline{\text{DRQ0}}$	O	DMA transfer request signal to CXD1186.
78～80	GADSP2～0	I	Format select signal to convert format of the main data from CD drive.

IC, CXD1186CR

Pin No.	Pin Name	I/O	Description
1~4	A0~A3	I	CPU address signal.
5	HMDS	I	Host mode select signal.
6, 7	HA0, HA1	I	Host address signal.
8	XHCS	I	Chip select negative logic signal from the host.
9	HINT	O	Interrupt request negative logic signal to the host.
10	GND	—	GND.
11	XHRD	I/O	Data read strobe signal from the host or to the SCSI control IC.
12	XHWR	I/O	Data write strobe signal from the host or to the SCSI control IC.
13~20	HDB0~HDB7	I/O	Host data bus.
21	GND	—	GND.
22	HDBP	I/O	Error flag. Host data bus.
23	XRST	I	Reset negative logic signal.
24	HDRQ	O	Data request positive logic signal to the host. Or DMA acknowledge negative logic signal to the SCSI control IC.
25	XHAC	I	DMA acknowledge negative logic signal from the host Or data request positive logic signal from the SCSI control.
26	XTC	I	Terminal count negative logic signal.
27	ADRQ	I	DMA request positive logic signal from ADP.
28	XAAC	O	DMA acknowledge negative logic signal to ADP.
29, 30	BA0, BA1	O	Buffer memory address.
31	VDD	—	Power supply (+5 V) terminal.
32~39	BA2~BA9	O	Buffer memory address.
40	GND	—	GND.
41~46	BA10~BA15	O	Buffer memory address.
47	XMOE	O	Buffer memory output enable negative logic signal.
48	XMWR	O	Buffer memory write negative logic signal.
49	BDB0	I/O	Buffer memory data bus.
50	GND	—	GND.
51~57	BDB1~BDB7	I/O	Buffer memory data bus.
58	BDBP	I/O	Buffer memory pointer data bus.
59	XTL2	O	X'TAL oscillator circuit output terminal.
60	XTL1	I	X'TAL oscillator input terminal.
61	GND	—	GND.
62	HCLK	O	X'TAL 1 divided-by-2 clock signal.
63	LRCK	I	LR clock from CD player.
64	DATA	I	Serial data from CD player.
65	BCLK	I	Bit clock from CD player.
66	C2P0	I	C2 pointer from CD player.
67~70	DB0~DB3	I/O	CPU data bus.
71	VDD	—	Power supply (+5 V) terminal.
72~75	DB4~DB7	I/O	CPU data bus.

Pin No.	Pin Name	I/O	Description
76	XCS	I	Chip select negative logic signal from CPU.
77	XRD	I	IC internal register read-out strobe negative logic signal from CPU.
78	XWR	I	IC internal register write strobe negative logic signal from CPU.
79	INT	O	Interrupt request signal to CPU.
80	GND	—	GND.

IC, TLC29321PW

Pin No.	Pin Name	I/O	Description
1	VDD	—	Power supply terminal to the internal logic circuit.
2	VCO LS	I	VCO output frequency divide-by-2 divider select terminal. The VCO output frequency can be divided by 2 and output as this terminal is controlled by external logic.
3	VCOO	O	VCO output terminal. Goes to low level during inhibit.
4, 5	FIN-A, FIN-B	I	2 input terminal for edge difference detection between the reference frequency (fREF-IN) and the frequency from external counter. The fREF-IN is input to the FIN-A terminal normally, and the divided or multiplied frequency from external counter is input to the FIN-B terminal.
6	PFDO	O	PFD output terminal.
7	GND	—	Internal logic circuit GND terminal.
8	NC	—	N.C.
9	PFDIH	I	PFD inhibit function control terminal.
10	VCOIH	I	VCO inhibit function control terminal.
11	A GND	—	VCO GND.
12	VCOI	I	VCO control voltage input. The VCO oscillator control voltage is input from an external low-pass filter to form PLL.
13	RBIAS	I	External resistor is connected to this terminal for setting the VCO oscillation frequency. A bias resistor is connected between this terminal and power supply line to supply bias for internal VCO oscillation and for setting and adjusting the oscillating frequency.
14	A VDD	—	VCO power supply voltage terminal.

IC, HD49307

Pin No.	Pin No.	I/O	Description
1~5	G4~G8	I	Digital input terminal.
6	B1	—	N. C.
7	NC	I	Digital input terminal.
8~12	B2~B6	I	Digital input terminal.
13~15	NC	—	N. C.
16, 17	B7, B8	I	Digital input terminal.
18	NC	—	N. C.
19	RCLK	I	R channel clock input.
20	GCLK	I	G channel clock input.
21	BCLK	I	B channel clock input.
22	DVSS	—	Digital GND.
23	DVDD	—	Digital power supply.
24	NC	—	N. C.
25	CBU	—	External phase compensation capacitance connection terminal.
26	CBL	—	Bypass capacitance connection terminal.
27~29	NC	—	N. C.
30	VRREF	I	Reference voltage input terminal.
31	AVSS	—	Analog GND.
32	AVDD	—	Analog power supply.
33	BOUT	O	B channel analog signal output terminal.
34	AVDD	—	Analog power supply.
35	NC	—	N. C.
36	GOUT	O	G channel analog signal output terminal.
37	AVDD	—	Analog power supply.
38	ROUT	O	R channel analog signal output terminal.
39	AVSS	—	Analog GND.
40	AVDD	—	Analog power supply.
41	DVDD	—	Digital power supply.
42	R1	I	Digital input terminal.
43~44	NC	—	N. C.
45~51	R2~R8	I	Digital input terminal.
52~54	G1~G3	I	Digital input terminal.
55, 56	NC	—	N. C.

IC, μPD61010

Pin No.	Pin Name	I/O	Description
1	VDD	—	+5 V power supply.
2~6	HD9~5	I/O	Host data bus.
7	VDD	—	+5 V power supply.
8	GND	—	GND.
9~13	HD4~0	I/O	Host data bus.
14	VDD	—	+5 V power supply.
15	GND	—	GND.
16	$\overline{\text{DREQ}}$	O	DMA request signal.
17	$\overline{\text{DACK}}$	I	DMA acknowledge signal.
18	HSEL	I	Signal to select the host CPU access method.
19	DRQ	I	Data input request for bit stream input from CD-ROM decoder.
20	VDD	—	+5 V power supply.
21	GND	—	GND.
22	$\overline{\text{DAK}}$	O	Data input response for bit stream input from CD-ROM decoder, or DMA input request for code input.
23	$\overline{\text{DRD}}$	O	Bit stream input approval signal.
24, 25	NC	—	N. C.
26~33	CD0~7	I	Data bus for bit stream input from CD-ROM decoder.
34	VDD	—	+5 V power supply.
35	GND	—	GND.
36~39	MD7~4	I/O	DRAM data bus.
40	VDD	—	+5 V power supply.
41, 42	GND	—	GND.
43~46	MD3~0	I/O	DRAM data bus.
47, 48	MD15, 14	I/O	DRAM data bus.
49	VDD	—	+5 V power supply.
50	GND	—	GND.
51~56	MD13~8	I/O	DRAM data bus.
57	VDD	—	+5 V power supply.
58	GND	—	GND.
59~64	MA0~5	O	DRAM address bus.
65	VDD	—	+5 V power supply.
66	GND	—	GND.
67~69	MA6~8	O	DRAM address bus.
70	$\overline{\text{RAS 1}}$	O	DRAM RAS signal.
71	$\overline{\text{RAS 0}}$	O	DRAM RAS signal.
72	$\overline{\text{CAS}}$	O	DRAM CAS signal.
73	VDD	—	+5 V power supply.
74	$\overline{\text{WE}}$	O	Write enable to DRAM.
75~77	NC	—	N. C.
78	VOE	I	Video data output enable.

Pin No.	Pin Name	I/O	Description
79, 80	GND	—	GND.
81	VDD	—	+5 V power supply.
82	NC	—	N. C.
83	FLDI	I	Field signal (odd/even)
84	HDI	I	Horizontal sync signal.
85	VDI	I	Vertical sync signal.
86	VDCLK	I	Video data output clock (13.5 MHz).
87	VDD	—	+5 V power supply.
88~91	VDATA23~20	O	Video data output bus.
92	GND	—	GND.
93	VDD	—	+5 V power supply.
94~97	VDATA19~16	O	Video data output bus.
98, 99	VDATA15, 14	O	Video data output bus.
100	VDD	—	+5 V power supply.
101	GND	—	GND.
102~105	VDATA13~10	O	Video data output bus.
106	VDD	—	+5 V power supply.
107	GND	—	GND.
108~112	VDATA9~5	O	Video data output bus.
113	VDD	—	+5 V power supply.
114	GND	—	GND.
115~119	VDATA4~0	O	Video data output bus.
120	VDD	—	+5 V power supply.
121, 122	GND	—	GND.
123	DO	O	Video data output bus.
124	BCK	O	Video data output clock.
125	LRCK	O	L/R channel identification signal.
126	MCLK	O	Audio master clock.
127	NC	—	N. C.
128	AUCLK	I	Internal audio decoder system clock.
129	VDD	—	+5 V power supply.
130~132	NC	—	N. C.
133	VDD	—	+5 V power supply.
134	$\overline{\text{RESET}}$	I	Reset signal.
135	CLK	I	System clock (27 MHz)
136	GND	—	GND.
137	$\overline{\text{DS}}$	I	Data strobe signal.
138	R/$\overline{\text{W}}$	I	Read/write select.
139	$\overline{\text{CS}}$	I	Chip select.
140~145	HADR0~5	I	Host address bus.
146, 147	GND	—	GND.

Pin No.	Pin Name	I/O	Description
148	INT	O	Interrupt signal.
149	$\overline{\text{HDAK}}$	O	Bus cycle response signal.
150	VDD	—	+5 V power supply.
151	GND	—	GND.
152~157	HD15~10	I/O	Host data bus.
158	VDD	—	+5 V power supply.
159, 160	GND	—	GND.

IC, μPD63210GT

Pin No.	Pin Name	I/O	Description
1	TSEL	I	Test selection input.
2	RST	I	Reset input.
3	XTO	O	External crystal oscillator is connected to this pin.
4	XTI	I	External crystal oscillator is connected to this pin.
5	MCKO	O	Master clock output.
6	CKSEL	I	Clock selection input.
7	CLK	I	Bit clock input.
8	SI	I	Data input.
9	LRCK	I	LR clock input.
10	DEFS1	I	Deemphasis selection input 1.
11	DEFS2	I	Deemphasis selection input 2.
12	DSEL	I	Double speed playback selection input..
13	SMUTE	I	Soft mute selection input.
14	BSEL	I	Data bit length selection input.
15	DGND	—	Digital GND.
16	AGND	—	Analog GND.
17	RO	O	D/A converter output (R channel).
18	AOR	O	Filter amplifier output (R channel).
19	ANIR	I	Filter amplifier (-) input (R channel).
20	APIR	I	Filter amplifier (+) input (R channel).
21	RREF	—	Reference (R channel).
22	LREF	—	Reference (L channel).
23	APIL	I	Filter amplifier (+) input (L channel).
24	ANIL	I	Filter amplifier (-) input (L channel).
25	AOL	O	Filter amplifier output (L channel).
26	LO	O	D/A converter output (L channel).
27	AVDD	—	Analog power supply.
28	DVDD	—	Digital power supply.

IC, TC170C100AF

Pin No.	Pin Name	I/O	Description
1~5	YIN4~0	I	Y signal from MPEG chip.
6	GND	—	GND.
7~14	UIN7~0	I	U signal from MPEG chip.
15	GND	—	GND.
16, 17	VIN7, 6	I	V signal from MPEG chip.
18	VCC	—	Power supply terminal.
19~24	VIN5~0	I	V signal from MPEG chip.
25	GND	—	GND.
26	FLDO	O	Odd/even signal output of a field.
27	$\overline{\text{HDO}}$	O	$\overline{\text{HSYNC}}$ signal to MPEG chip.
28	$\overline{\text{VDO}}$	O	$\overline{\text{VSYNC}}$ signal to MPEG chip.
29	PCP	O	Clamp signal output.
30	CBLK	O	Blanking signal output (used depending upon type of DAC).
31	GND	—	GND.
32	FSC	O	Sub carrier output (Divided-by-four of NTSC: 14.31818 MHz. PAL: 17.734475 MHz).
33	CDG/$\overline{\text{MPEG}}$	O	CD-G or MPEG play selector signal to external RGB video selector.
34	TEST0	I	Operation mode setting terminal.
35	GND	—	GND.
36	13.5M	O	13.5 MHz output.
37	GND	—	GND.
38~43	R OUT7~2	O	Y/R signal output (Output format can be selectable in Y/R).
44	GND	—	GND.
45, 46	R OUT1, 0	O	Y/R signal output (Output format can be selectable in Y/R).
47~54	G OUT7~0	O	U/G signal output (Output format can be selectable in U/G).
55	VCC	—	Power supply terminal.
56~63	B OUT7~0	O	V/B signal output (Output format can be selectable in V/B).
64	GND	—	GND.
65	27M	I	27 MHz input.
66	TEST1	I	Operation mode setting terminal.
67	SHSYNC	O	Comparison clock for PLL synchronizing CLK.
68	MHSYNC	O	Reference clock for PLL synchronizing CLK.
69	VCC	—	Power supply terminal.
70	OSC1	I	14.31818 MHz input port (crystal oscillation) when supporting NTSC.
71	OSC2	O	NTSC: 14.31818 MHz crystal oscillation output terminal.
72, 73	GND	—	GND.
74	OSC3	I	17.734475 MHz input port (crystal oscillation) when supporting PAL.
75	OSC4	O	17.734475 MHz crystal oscillation output terminal.
76	VCC	—	Power supply terminal.
77, 78	TEST2, 3	I	Operation mode setting terminal.
79	FMOD	I	FLD0 output HL inversion selection signal.
80	PMOD	I	PCP output HL inversion selection signal.

Pin No.	Pin Name	I/O	Description
81	GND	—	GND.
82～85	T15～T12	I	RAM data input terminals 15 - 12 during RAM check.
86	T11OP3	I/O	OUT port terminals 3 - 0 (address 4). RAM data input terminals 11 - 8 during RAM check.
87	T10OP2	I/O	OUT port terminals 3 - 0 (address 4). RAM data input terminals 11 - 8 during RAM check.
88	T9OP1	I/O	OUT port terminals 3 - 0 (address 4). RAM data input terminals 11 - 8 during RAM check.
89	T8OP0	I/O	OUT port terminals 3 - 0 (address 4). RAM data input terminals 11 - 8 during RAM check.
90	VCC	—	Power supply terminal.
91	$\overline{\text{GHSYNC}}$	I	$\overline{\text{HSYNC}}$ signal from CD-G decoder.
92	$\overline{\text{GVSYNC}}$	I	$\overline{\text{VSYNC}}$ signal from CD-G decoder.
93	$\overline{\text{GCSYNC}}$	I	$\overline{\text{CSYNC}}$ signal from CD-G decoder.
94	GND	—	GND.
95～98	T7～4	I	RAM data input terminals 7 - 4 during RAM check.
99	T3IP3	I	IN port terminals 3 - 0 (address 5). RAM data input terminals 3 - 0 during RAM check.
100	T2IP2	I	IN port terminals 3 - 0 (address 5). RAM data input terminals 3 - 0 during RAM check.
101	T1IP1	I	IN port terminals 3 - 0 (address 5). RAM data input terminals 3 - 0 during RAM check.
102	T0IP0	I	IN port terminals 3 - 0 (address 5). RAM data input terminals 3 - 0 during RAM check.
103	GND	—	GND.
104	4FSC	O	104 NTSC: 14.31818 MHz. PAL: 17.734475 MHz buffer output.
105	GND	—	GND.
106	RAMCE	I	Chip enable signal for checking internal RAM and ROM check. (Fixed to low normally).
107	RAMW	I	Read/write signal for checking internal RAM and ROM check. (Fixed to low normally).
108	XT2C	I	XT2C input (used for HYNC DL delay).
109	GND	—	GND.
110	$\overline{\text{RST}}$	I	Input port of the reset signal.
111	GND	—	GND.
112	PAL/$\overline{\text{NTSC}}$	I	PAL/NTSC selector port.
113	HSYNCIN	O	Inverted output of $\overline{\text{HYNSC}}$ IN.
114	$\overline{\text{HSYNCIN}}$	I	$\overline{\text{SYNC}}$ signal from VST (only when supporting FMV engine).
115	$\overline{\text{VSYNCIN}}$	I	$\overline{\text{VSYNC}}$ from VSC. (only when supporting FMV engine).
116	GND	—	GND.
117～124	D7～0	I/O	CPU data bus signal.

Pin No.	Pin Name	I/O	Description
125	VCC	—	Power supply terminal.
126	CMOD	I	CLBK output HL inversion selection signal.
127	$\overline{\text{VOD}}$	I	Video output disable.
128	VCD/$\overline{\text{FMV}}$	I	VIDEO CD/DMV engine selection port.
129	$\overline{\text{CS}}$	I	Chip select signal.
130	$\overline{\text{RD/LDS}}$	I	READ signal from CPU $\overline{\text{RD}}$ (when supporting H8). $\overline{\text{LD}}$ (when supporting 680009).
131	$\overline{\text{WR/R/W}}$	I	$\overline{\text{WRITE}}$ signal from CPU $\overline{\text{WR}}$ (when supporting H8). R/W (when supporting 680009).
132～134	A2～0	I	Address signal from CPU.
135	H8/$\overline{68}$	I	CPU H8-325/68000 selection port.
136	GND	—	GND.
137	$\overline{\text{HSYNCO}}$	O	Horizontal sync output.
138	$\overline{\text{VSYNCO}}$	O	Vertical sync output.
139	$\overline{\text{CSYNCO}}$	O	Composite sync output. $\overline{\text{CSYNC}}$ signal from video encoder.
140	SMOD	I	13.5 MHz ↑ ↓ selection of SYNC signal output. Selection is possible at the final stage of $\overline{\text{HDO}}$, $\overline{\text{VDO}}$, $\overline{\text{HSYNCO}}$, $\overline{\text{VSYNCO}}$, $\overline{\text{CSYNCO}}$, SHYNC, PCP, CBLK, FLDO. (However, $\overline{\text{HSYNCO}}$, $\overline{\text{VSYNCO}}$, $\overline{\text{CSYNCO}}$ are supported during SYNC output of the CD-G decoder.)
141	VCC	—	Power supply terminal.
142～144	YIN7～5	I	Y signal from MPEG chip.

IC, MB89627

Pin No.	Pin Name	I/O	Description
1	CCLK	O	SSP, DSP Control Clock.
2	DATA	O	SSP, DSP Control Data.
3	SENS	I	SSP, DSP Status.
4	XLAT	O	SSP, DSP Command Latch.
5	XRST	O	SSP, DSP Reset.
6	TVMSW	O	OFF/NTSC/PAL/PAL60/PAL AUTO/AUTO/TEST. *NOTE
7	DMUTE	O	Digital Mute.
8	AMUTE	O	Analog Mute.
9	LDON	O	Servo PCB Power on.
10	VCDRST	O	Video CD Reset.
11	OPTON	O	Optical Digital Output ON.
12	VCC	—	A/D Converter VCC.
13	VCC	—	A/D Converter VREF.
14	VSS	—	A/D Converter VSS.
15	HOSTIRQ	I	Host CPU Interrupt Request.
16	SCOR	I	Subcode Sync 0. (Subcode IRQ)
17	ILSW	I	Inter Limit Switch.
18	VCDIRQ	I	Video CD Decoder Interrupt Request.
19	N. C.	I	Not used.
20	RST	I	CPU Reset.
21	MODE0	I	CPU MODE. (Pull-down)
22	MODE1	I	CPU MODE. (Pull-down)
23	CLKIN	O	8MHz System Clock.
24	CLKOUT	I	8MHz System Clock.
25	VSS	—	GND.
26	ALE	O	Address Latch Strobe.
27	RD	O	Data Read Strobe.
28	WR	O	Data Write Strobe.
29	CLK	O	Clock out.
30	READY	I	Video CD Decoder Ready.
31	OSDCS	O	OSDC Enable.
32	OSDCLK	O	OSDC Data Clock.
33	OSDSIN	O	OSDC Data.
34~41	A8~A15	O	Address Bus 8~15.
42~49	AD0~AD7	I/O	Address/Data Bus 0~7.
50	VSS	—	GND.
51	VCD/CDG	O	Video CD/CDG Switch.
52	HCLK	I	Host CPU Control Clock.
53	ST	O	Host CPU Control Send Data.
54	RT	I	Host CPU Control Receive Data.
55	TRACK	I	Travase Counter.

Pin No.	Pin Name	I/O	Description
56	ENCRST	O	Video Encoder Reset.
57	DVCC	—	DVCC.
58	PAL/PAL60	O	PAL/PAL60 Switch.
59	XNTSC	O	PAL/NTSC Switch.
60	SQCK	O	Subcode Q Read Clock.
61	SQSO	I	Subcode Q Serial Data.
62	BUSY	I/O	Host CPU I/F Busy Signal.
63	FOK	I	Focus Servo OK Detect.
64	GFS	I	Frame Sync Detect.

Note

- Analog input (TVMSW: 6 pin) of the microprocessor is divided into 7, then controlled.
- The output are the command setting (Set Video Format) to the two ports of PAL/PAL60 (58 pin), XNTSC (59 pin) and IC301 (CL484).

TVMSW (6 pins)		DISC encoding system	TV output mode	PAL/PAL60 (58 pins)	XNTSC (59 pins)	Set Video Format
Volt (V)	Mode					
5.00	OFF	—	Not used (NTSC output mode).			
4.58	NTSC	—	NTSC	H	L	NTSC
3.75	PAL	—	PAL	H	H	PAL
2.92	PAL60	—	PAL60	L	H	NTSC
2.08	PAL AUTO	NTSC	PAL60	L	H	NTSC
		PAL	PAL	H	H	PAL
1.25	AUTO	NTSC	NTSC	H	L	NTSC
		PAL	PAL	H	H	PAL
0.42	TEST	—	For servo circuit adjustment (NTSC output mode).			
0.00						

*1 As to identification of the disc encoding system, it is identified from the V_SIZE (1A1h/word) of the MPEG data.

*2 "For servo circuit adjustment" is the process during adjustment (when variable resistor is operated by service engineer) that the microprocessor enters the emergency process routine if the servo system goes extremely out of the servo range.

*3 In addition to the above, ENCRST (56 pin) is the reset signal for TV encoder, issues the active "L" pulse when each of the input port of CDGSW, NTB, CVSY, HSY, PIXCLK, GCLK, PAL60B and VCLK of IC401 (BU1417AK) has changed as follows:

① When the power is supplied to the circuit boards of the CD block,

② When starting to reach TOC.

③ The modes have changed as follows:

- TVMSW is switched.
- Switching of encoding system owing to exchange of video CD disc
- Exchange of video CD disc with the CD-DA or CD-G.

IC, CL484

Pin No.	Pin Name	I/O	Description
1	HSEL2	I	Host address bus.
2	-DS	I	Data strobe.
3	R/-W	I	Read/write.
4	CFLEVEL	O	Coded data FIFO level status. Open drain.
5	-DACK	O	Host data acknowledge. Open drain.
6	HD0	I/O	Host data bus.
7	VDD3	—	Power supply pin. Used in 3.3 V.
8, 9	HD1, HD2	I/O	Host data bus.
10	VSS	—	GND.
11~15	HD3~HD7	I/O	Host data bus.
16	VSS	—	GND.
17	-TEST	I	Test terminal. Normally fixed to High.
18	VSS	—	GND.
19	XTL IN	I	Global clock. 40.5 MHz.
20	XTL OUT	O	Global clock. 40.5 MHz.
21, 22	VDD3	—	Power supply pin. Used in 3.3 V.
23~28	MD0~MD5	I/O	Memory data bus.
29	VDD3	—	Power supply pin. Used in 3.3 V.
30, 31	MD6, MD7	I/O	Memory data bus.
32, 33	-MCE0, -MCE1	O	Chip enable.
34~37	MD8~MD11	I/O	Memory data bus.
38	VSS	—	GND.
39~42	MD12~MD15	I/O	Memory data bus.
43	VDDMAX	—	Power supply pin. Used in 5.0 V.
44	-LCAS	O	Lower digit, column address strobe.
45	-LCASIN	I	Lower digit, data latch enable.
46	VSS	—	GND.
47	-MWE	O	Write enable.
48	-UCAS	O	Higher digit, column address strobe.
49	VDD3	—	Power supply pin. Used in 3.3 V.
50	-UCASIN	I	Higher digit, data'latch enable.
51, 52	RAS0, RAS1	O	Lower address strobe.
53~57	MA9~MA5	O	Memory address bus.
58	VSS	—	GND.
59~63	MA4~MA0	O	Memory address bus.
64	RESERVED	—	Reserved.
65	VDD3	—	Power supply pin. Used in 3.3 V.
66~72	VD0~VD6	O	Pixel data bus. RGB or YCbCr format.
73	VSS	—	GND.
74~76	VD7~VD9	O	Pixel data bus. RGB or YCbCr format.
77	VDD3	—	Power supply pin. Used in 3.3 V.

Pin No.	Pin Name	I/O	Description
78~80	VD10~VD12	O	Pixel data bus. RGB or YCbCr format.
81	VDD3	—	Power supply pin. Used in 3.3 V.
82~84	VD13~VD15	O	Pixel data bus. RGB or YCbCr format.
85	VSS	—	GND.
86~89	VD16~VD19	O	Pixel data bus. RGB or YCbCr format.
90	VSS	—	GND.
91~94	VD20~VD23	O	Pixel data bus. RGB or YCbCr format.
95	-VSYNC or CSY	I/O	Vertical sync signal.
96	-HSYNC	I/O	Horizontal sync signal.
97	-VOE	I	Video output enable.
98	VDD3	—	Power supply pin. Used in 3.3 V.
99	VCLK	I/O	Video clock.
100	VSS	—	GND.
101	-RESET	I	Hardware reset.
102	VSS	—	GND.
103	CD-C2PO	I	Data error. Used during CD-ROM data input.
104	CD-LRCK	I	LR clock.
105	CD-DATA	I	Serial data input from CD-DSP.
106	CD-BCK	I	Bit clock from CD decoder.
107	DA-LRCK	O	LR clock.
108	DA-DATA	O	Bit serial audio sample signal.
109	DA-BCK	O	Audio bit clock.
110	VDD3	—	Power supply pin. Used in 3.3 V.
111	DA-XCLK	I	External audio frequency clock.
112	VDD3	—	Power supply pin. Used in 3.3 V.
113	-INT	O	Interrupt request.
114	CDG-S0S1	I	Block start sync.
115	HOST_ENA	I	Host enable.
116	RAM_ENA	I	Boot ROM enable.
117	CDG-VFSY	I	Frame start or composite sync.
118	DAC_EMP	O	Output emphasis flag.
119	CDDA_EMP	I	Input emphasis flag.
120	CDG-SDATA	I	Subcode data.
121	CDG-SCLK	I/O	Subcode data clock.
122	CDDA/VCD	O	Input data identification. H: CDDA. L: video CD.
123	VDDMAX	I	Power supply pin. Used in 5.0 V.
124	FSC1	O	Output generated by dividing-by-4 the pin-126 input CLK.
125	VSS	—	GND.
126	FSC4	I	Frequency divider input.
127, 128	HSEL0, HSEL1	I	Host address bus.

IC, BU1417AK

Pin No.	Pin Name	I/O	Description
1	BOSD	I	OSD Blue Data input.
2	GD0	I	Green Data Bit 0. (LSB)
3~8	GD1~GD6	I	Green Data Bit 1~6.
9	GND	—	Digital ground.
10	GD7	I	Green Data Bit 7. (MSB)
11	BD0	I	Blue Data Bit 0. (LSB)
12~14	BD1~BD3	I	Blue Data Bit 1~3.
15	OSDSW	I	OSD input enable.
16	CDGSWB	I	Select Video-CD/$\overline{\text{CD-G}}$.
17~19	BD4~BD6	I	Blue Data Bit 4~6.
20	BD7	I	Blue Data Bit 7. (MSB)
21	GND	—	Digital ground.
22	NTB	I	Select $\overline{\text{NTSC}}$/PAL mode.
23, 24	IM0, IM1	I	Input mode set Bit 0, 1.
25, 26	TEST1, TEST2	I	Normally pulldown to GND.
27	CVSY	I	C-SYNC or V-SYNC input.
28	HSY	I	H-SYNC input.
29	PIXCLK	O	1/2 Freq. of internal CL.
30	BLKB	I	Data blanking $\overline{\text{ENABLE}}$.
31	VDD	—	Digital VDD.
32	INT	I	INTERLACE/$\overline{\text{NON-INTERLACE}}$.
33	SLABEB	I	Set mode MASTER/$\overline{\text{SLABE}}$.
34	ADDH	I	ADD One_line at Non-inter.
35	VREF	I	Reference voltage. (1.29V)
36	CGND	—	Chroma output ground.
37	COUT	O	Chroma output.
38	VGND	—	Composite output ground.
39	VOUT	O	Composite output.
40	AVSS	—	Analog (DAC, VREF) ground.
41	NC	—	Not used.
42	IR	I	Reference resistor. (1.2K)
43	AVDD	—	Analog (DAC, REF) VDD.
44	YGND	—	Luminance output ground.
45	YOUT	O	Luminance output.
46	G4FSC	I	Pulldown to GND.
47	GCLK	I	Video clock input for CD-G.
48	YCOFF	I	DAC (YOUT, COUT) off.
49	YFILON	I	Pulldown to GND.
50	PAL60B	I	$\overline{\text{PAL60 ON}}$ at NTB=HIGH.
51	VCLK	I	Video clock input for VCD.
52	RSTB	I	Logic part initial reset.

Pin No.	Pin Name	I/O	Description
53	CLKSW	I	Divide input CLK $\overline{\text{ENABLE}}$.
54	RD0	I	Red data Bit 0. (LSB)
55, 56	RD1, RD2	I	Red data Bit 1, 2.
57	ROSD	I	OSD Red data input.
58~60	RD3~RD5	I	Red data Bit 3~5.
61	VDD	—	Digital VDD.
62	RD6, RD7	I	Red data Bit 6, 7.
63	GOSD	I	OSD green data input.

IC, BU2173AF

Pin No.	Pin Name	I/O	Description
1	VDD	—	Digital VDD.
2	TSTO	O	Open during normal mode. (Used in test mode.)
3	XTALI	I	Reference oscillator input.
4	XTALO	O	Reference oscillator output.
5	CTRLA	I	CD-G/VCD clock selector terminal.
6	CTRLB	I	Fixed to "H" during normal mode.
7	CTRLC	I	CD-G PAL/NTSC clock selector terminal.
8	TSTI	I	Connected to Vss during normal mode. (Used in test mode.)
9	VSS	—	Digital GND.
10	AVSS	—	Analog GND.
11	FOUT3	O	Not used. Open during normal mode.
12	VSSIO	—	I/O GND.
13	FOUT2	O	Clock output (2).
14	TEST	—	Test mode setting. Connected to Vss during normal mode.
15	FOUT1	O	Clock output (1).
16	VDDIO	—	I/O VDD.
17	FOUT4	O	Clock output (4).
18	AVDD	—	Analog VDD.

TEST MODE

1. How to Activate CD Test Mode
   Insert the AC plug while pressing the function CD button.
   All FL display tubes will light up, and the test mode will be activated.

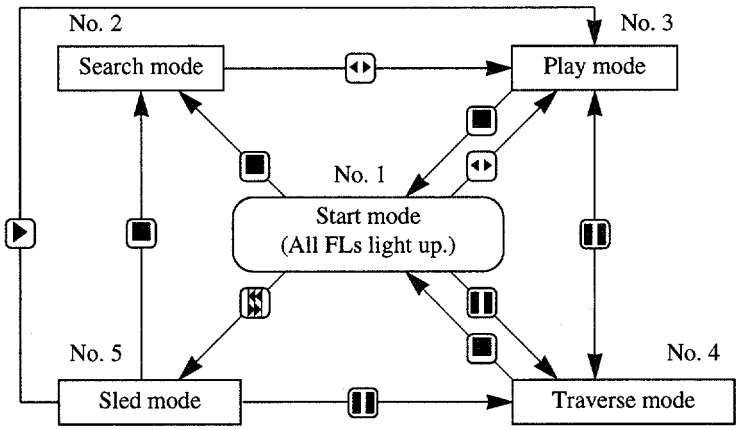
2. How to Cancel CD Test Mode
   Either one of the following operations will cancel the CD test mode.
   - Press the function button. (except CD function button)
   - Press the power switch button.
   - Disconnect the AC plug

3. CD Test Mode Functions
   When test mode is activated, the following mode functions from No.1 to No.5 can be used by pressing the operation keys.

Mode/No.	Operation	FL display	Operation	Contents
Start mode No.1	Activation	All lamps light	• Test mode is activated. • Laser diode turns always ON. (CD block power is ON.)	• FL display check (All displays light.) • APC circuit check • Laser current measurement (Laser current control. Across a resistor connected between emitter and GND.)
Search mode No.2	■ key	CD--	• Continual focus search (The pickup lens repeats the full-swing up-down motion.) * Avoid continual searches that last for more than 10 minutes. * NOTE 1	FOCUS SERVO • Check focus search waveform • Check focus error waveform (FOK/FZC are not monitored in the search mode)
Play mode No.3	◀▶ key	CD 1	• Normal playback • Focus search is continued if TOC cannot be read. * NOTE 1	FOCUS SERVO/TRACKING SERVO CLV SERVO/SLED SERVO Check FOK/FZC
Traverse mode No.4	▮▮ key	CD 1	• During normal disc playback Press once; tracking servo OFF Press twice; tracking servo ON * NOTE 2	TRACKING SERVO ON/OFF Tracking balance (traverse) adjustment
Sled mode No.5	⏮ key ⏭	All lamps light	• Pickup moves to the outermost track • Pickup moves to the innermost track * NOTE 3 (During playback, machine operates normally.)	SLED SERVO Check SLED mechanism operation

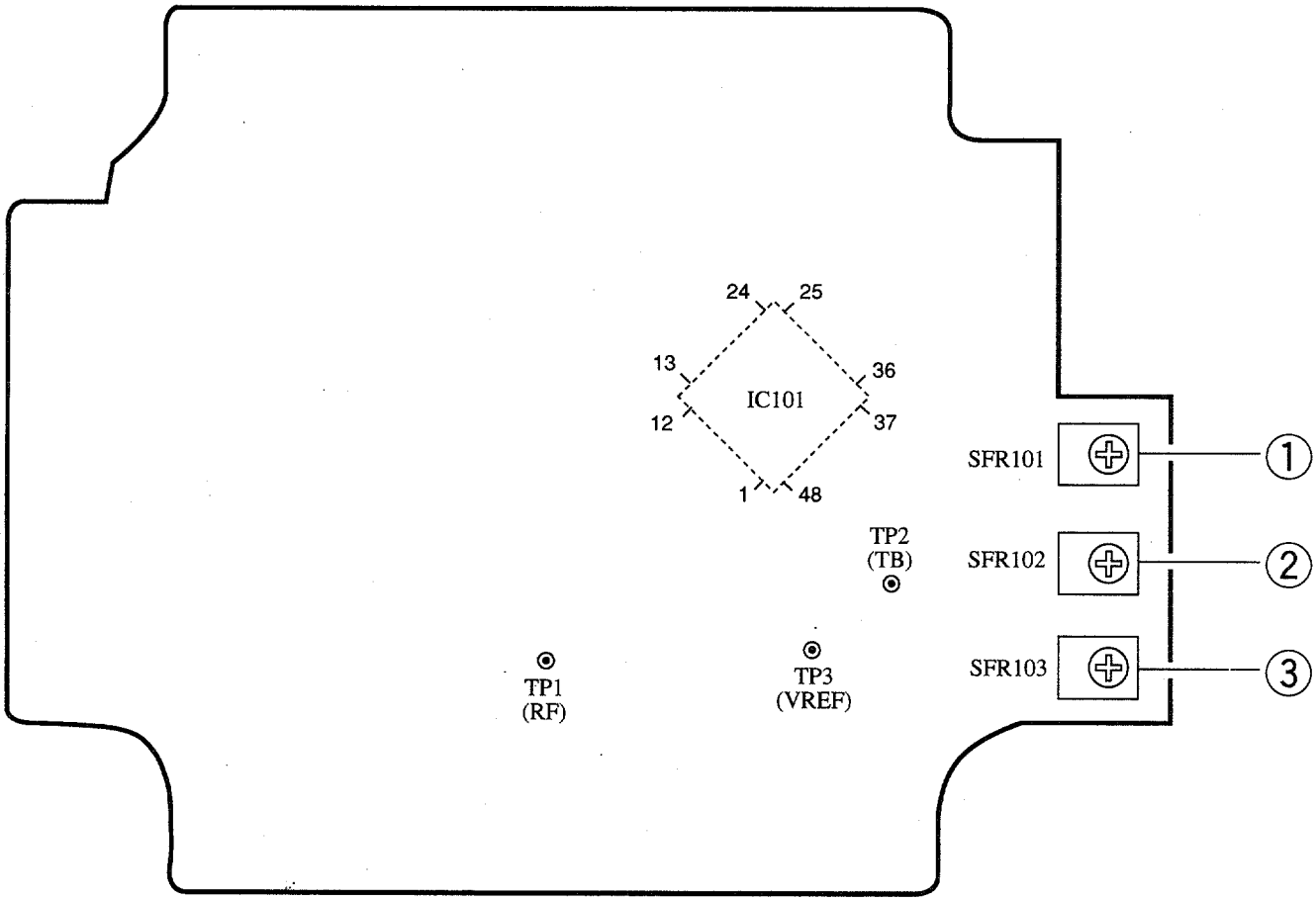
* NOTE 1: There are cases when the tracking servo cannot be locked owing to the protection circuit being operated when heat builds up in the driver IC if the focus search is operated continually for more than 10 minutes. In these cases the power supply should be switched off for 10 minutes until heat has been reduced and then re-started.
* NOTE 2: Do not press the ⏮ or ⏭ keys when the machine is in the ▮▮ status is active. If they are pressed, playback will not be possible after the ▮▮ status has been canceled. If the ⏮ or ⏭ keys are pressed in the ▮▮ status, press the ■ key and return to the start mode (No.1).
* NOTE 3: When pressing the ⏮ or ⏭ keys, take care to avoid damage to the gears. Because the sled motor is activated when the ⏮ or ⏭ keys are pressed, even when the pick-up is at the outermost or innermost track.

4. Operation Outline
   The operation of each mode is carried out in the direction of the arrows from the start mode as indicated in the following illustration.



If the DISC DIRECT PLAY button is pressed, the machine performs the same operation as the PLAY button is pressed as shown. If the tray is opened by pressing OPEN/CLOSE button during Play mode or Traverse mode, the machine returns to the Start mode.

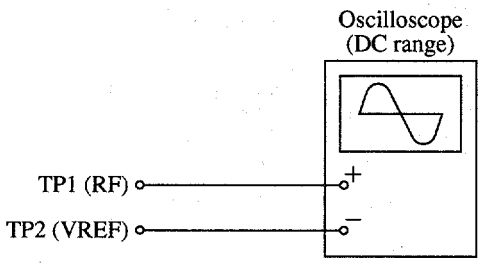
B CD MECHA C.B


24
25
13
36
IC101
12
37
1
48
SFR101
1
TP2
(TB)
SFR102
2
TP1
(RF)
TP3
(VREF)
SFR103
3

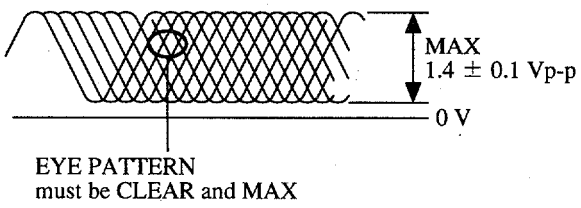
Note: Connect a probe (10: 1) of the oscilloscope or the frequency counter to a test point.

1. Focus Bias Adjustment

Make the focus bias adjustment when replacing and repairing the optical block.

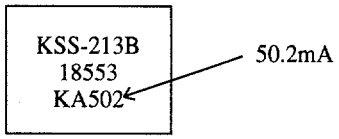


1) Connect an oscilloscope to test points TP1 (RF) and TP2 (VREF).
2) Turn on the power switch.
3) Insert test disc TCD-782 (YEDS-18) and play back the second composition.
4) Adjust SFR101 so that RF signal of test point TP1 (RF) is MAX and CLEARREST.



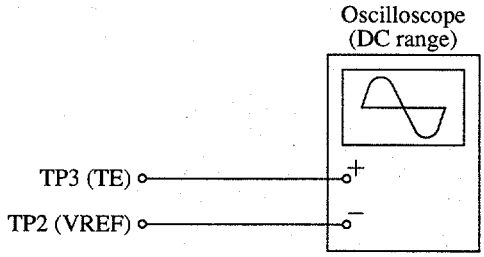
VOLT/DIV : 50mV
TIME/DIV : 0.5μS

Note: The current of the laser signal can be checked with the voltages on both sides of R127 (10Ω). The difference for the specified value shown on the lavel must be within ± 6.0mA.

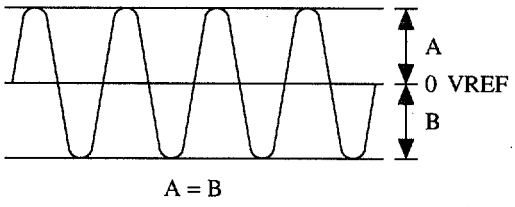


$$\text{Laser current Iop} = \frac{\text{Voltage across R127}}{10\Omega}$$

2. Tracking Balance Adjustment



1) Connect an oscilloscope to test points TP3 (TE) and TP2 (VREF).
2) Turn on the power switch.
3) Insert test disc TCD-782 (YEDS-18) and press the PLAY button.
4) Adjust SFR103 to decrease the tracking gain.
5) Adjust SFR102 so that the waveform on the oscilloscope is vertically symmetrical as shown in the figure below.
6) After the adjustment is completed, remove the connected lead wires from the terminals.



VOLT/DIV : 20mV
TIME/DIV : 1mS

3. Tracking Gain Adjustment

A servo analyzer is necessary in order to perform this adjustment exactly. However, this gain has a margin, so even if it is slightly off, there is no problem. Therfore, do not perform this adjustment.
Focus/tracking gain determines the pick-up follow-up (vertical and horizontal) relative to mechanical noise and mechanical shock when 2-axis device operates. However, as these reciprocate, the adjustment is at the point where both are satisfied.

- When gain is raised, the noise increases when the 2-axis device operates.
- When gain is lowered, it is more susceptible to mechanical shock and skipping occurs more easily.

When the gain adjustment is off, the symptoms below appear.

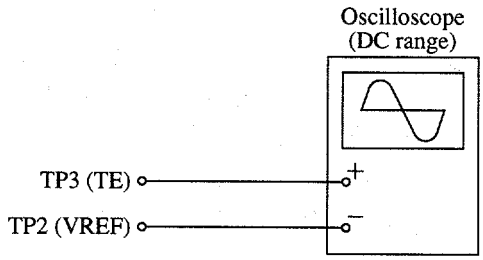
Symptoms \ Gain	(Focus)	Tracking
● The time until music starts becomes longer for STOP→▶PLAY or automatic selection (⏮, ⏭ buttons pressed.) (Normally takes about 2 seconds.)	low	low or high
● Music does not start and disc continues to rotate for STOP →▶PLAY or automatic selection (⏮, ⏭ buttons pressed.)	—	low
● Disc stops to rotate shortly after STOP→▶PLAY.	low or high	—
● Sound is interrupted during PLAY. Or time counter display stops.	—	low
● More noises during the 2-axis device operation.	high	high

The following is simple adjustment method.

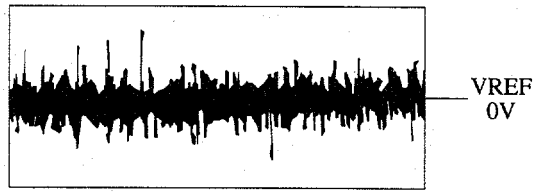
— Simple adjustment —

Note: Since the exact adjustment cannot be performed, remember the positions of the controls before the performing the adjustment. If the positions after the simple adjustment are only a little different, return the controls to the original position.

Procedure:



1) Keep the set horizontal. (If the set is not kept horizontally, this adjustment cannot be performed due to the gravity against the 2-axis device.)
2) Insert test disc TCD-782 (YEDS-18) and play back the second composition.
3) Connect an oscilloscope to TP3 (TE), TP2 (VREF) of the CD MECHA C.B.
4) Adjust SFR103 so that the waveform appears as shown in the figure below. (tracking gain adjustment)

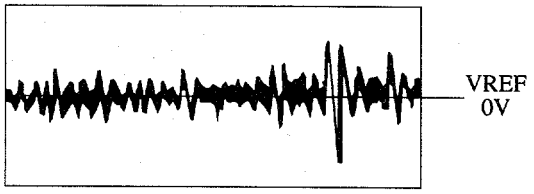


VOLT/DIV: 50 mV
TIME/DIV: 1mS

● Incorrect example

Low tracking gain

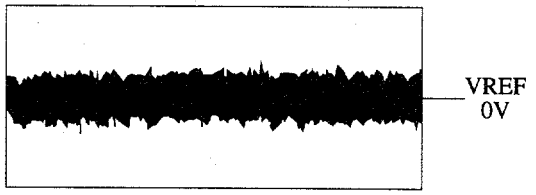
The fundamental wave appears as compared with the waveform adjusted.



VOLT/DIV: 50 mV
TIME/DIV: 1mS

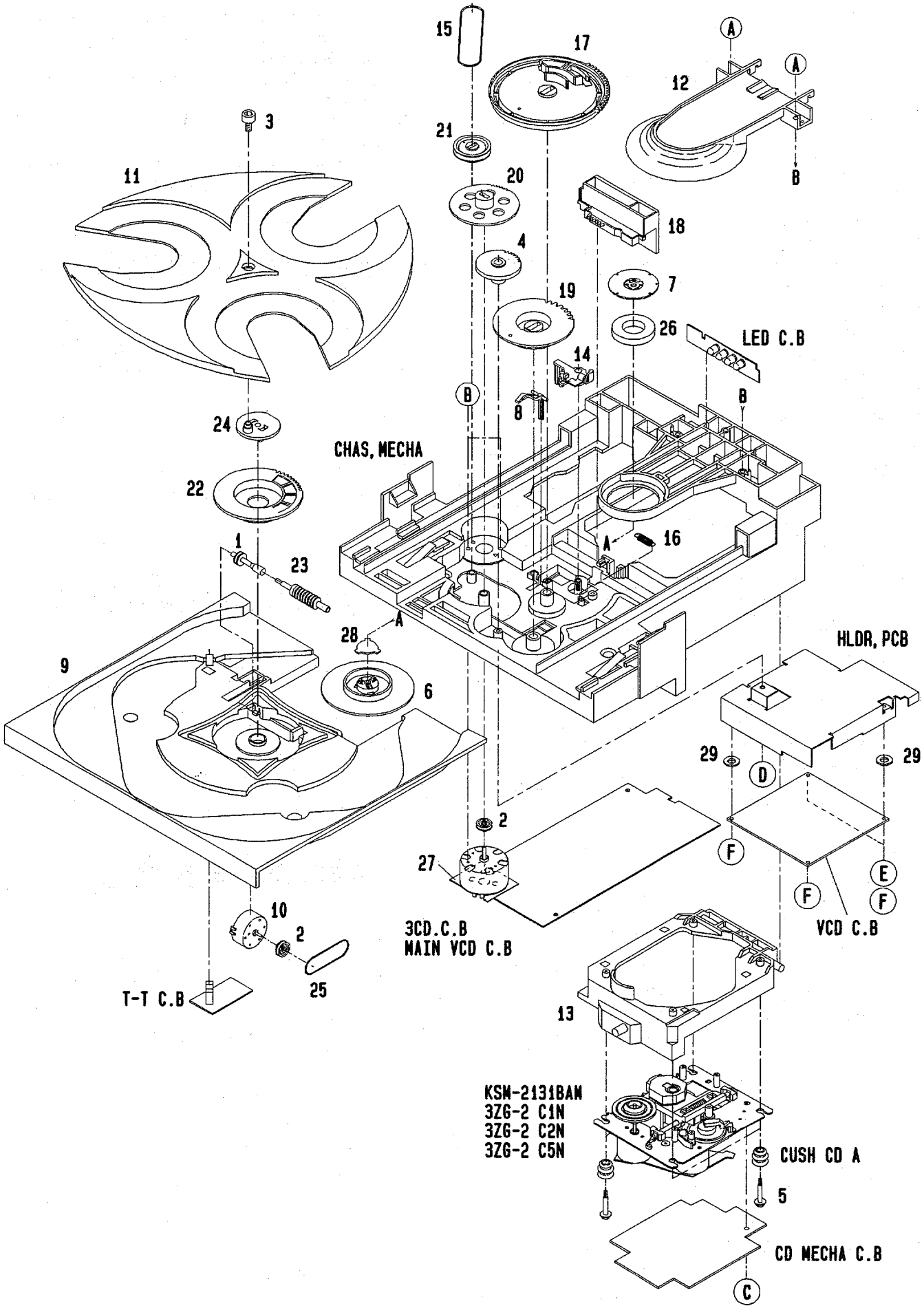
High tracking gain

The frequency of the fundamental wave is higher than that in low gain.



VOLT/DIV: 50 mV
TIME/DIV: 1mS

MECHANICAL EXPLODED VIEW 1 / 1

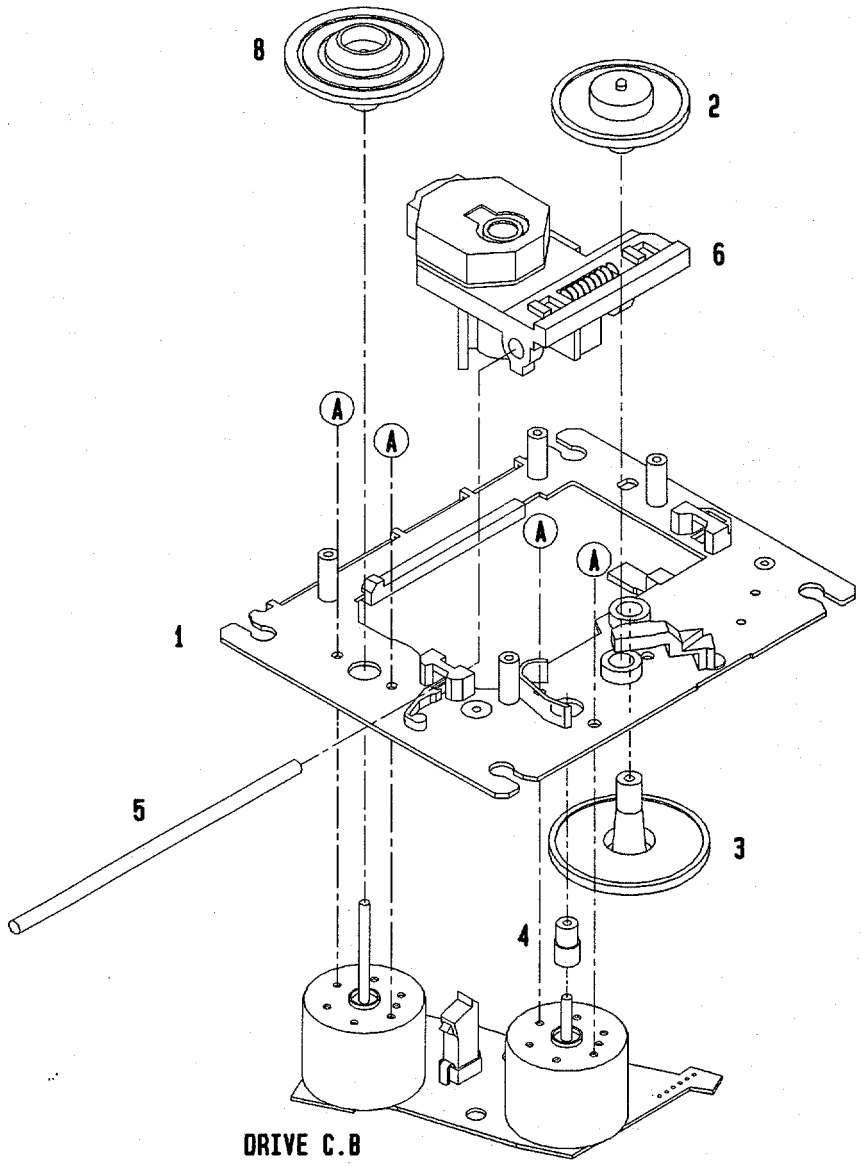


MECHANICAL PARTS LIST 1 ／ 1

DESCRIPTIONで判断できない物は “REFERENCE NAME LIST” を参照してください。
If can't understand for Description please kindly refer to “REFERENCE NAME LIST”.

REF. NO	PART NO.	カンリ NO.	DESCRIPTION
1	84-ZG1-239-11K		PULLY,WORM N
2	81-ZG1-212-01K		PULLY,LOAD MO
3	81-ZG1-239-019		S-SCREW,TT
4	81-ZG1-291-019		GEAR,TRAY RELAY NO3
5	81-ZG1-271-019		S-SCREW,MECH REAR
6	81-ZG1-277-219		HLDR,MAGNET N
7	81-ZG1-255-119		PLATE,MAGNET MK2
8	83-ZG3-213-019		LVR,SW
9	84-ZG1-003-219		TRAY,NO2-B
10	87-045-364-019		MOTOR,(BCH3B14)
11	84-ZG1-005-119		TURNTABLE,NO1
12	84-ZG1-010-019		IND,CD N<V3L,V4L>
12	84-ZG1-011-019		REFLECTOR,CD<A,B,Z,V5>
13	84-ZG1-212-119		HLDR,MECHA NO2
14	84-ZG1-208-019		LEVER,CAM
15	84-ZG1-209-010		BELT,SQ1.8-117.7
16	84-ZG1-211-019		SPR-E CAM S
17	84-ZG1-215-219		GEAR,MAIN CAM BLU
18	84-ZG1-216-219		SLIDE,MECHA CAM YEL
19	84-ZG1-205-119		GEAR,TRAY
20	84-ZG1-206-119		GEAR,RELAY
21	84-ZG1-219-019		PULLY,RELAY BGE
22	84-ZG1-221-019		GEAR,MAIN TT
23	84-ZG1-238-01K		GEAR,WORM N
24	84-ZG1-224-019		LEVER,TT
25	84-ZG1-225-010		BELT,SQ1.0-63.3
26	87-036-326-010		MAGNET,CLAMPER 93<A,B,Z,WR,V5>
26	83-ZG3-602-010		RING,MAG<V3L,V4L>
27	80-CD3-214-019		CUSH CD A
28	84-ZG1-248-019		SPR-C,WORM
29	82-DW1-220-019		SPACER,DIA 3.6-8-0.24<V3L>
A	87-067-703-019		BVT2+3-10 (W/O SLOT)<EXCEPT WR>
B	87-251-070-419		U+2.6-3<Z>
C	87-342-036-219		UT2+2-8<V3L,V4L,V5>
D	87-067-579-019		BVT 2+3-8 W/O SLOT<V3L,V4L>
E	81-557-598-010		UTT+2-5 C-TITE<V4L>
F	87-067-767-019		BVTT+2.6-6<V3L>
G	87-067-058-019		FW,3.2-8-0.5<V4L>

CD MECHANISM EXPLODED VIEW 1 ／ 1 (3ZG-2 C5N <WR>)

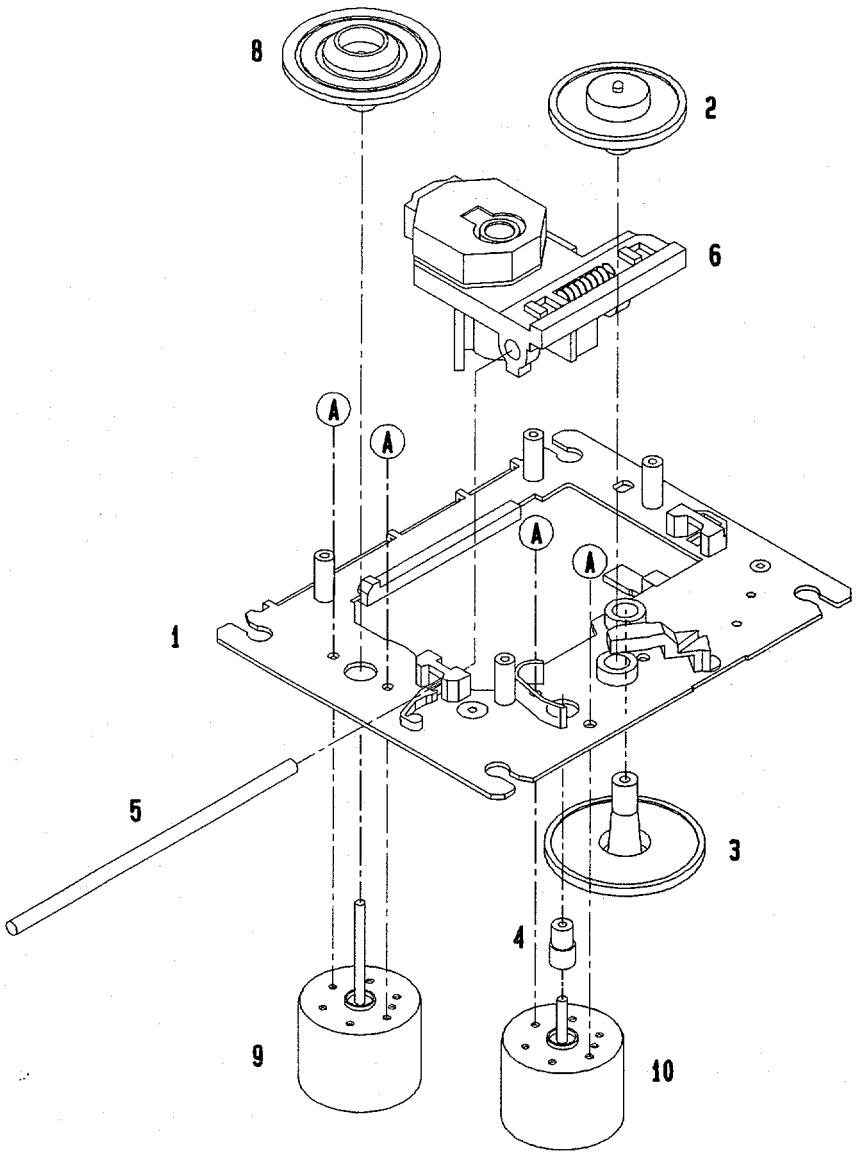


CD MECHANISM PARTS LIST 1 ／ 1 (3ZG-2 C5N <WR>)

DESCRIPTIONで判断できない物は "REFERENCE NAME LIST" を参照してください。
If can't understand for Description please kindly refer to "REFERENCE NAME LIST".

REF. NO	PART NO.	カンリ NO.	DESCRIPTION
1	83-ZG2-202-71K		O-SERT S ASSY,S
2	83-ZG2-204-419		GEAR,A
3	83-ZG2-205-219		GEAR,B
4	83-ZG2-220-01K		GEAR MOTOR 2
5	83-ZG2-207-119		SHAFT,SLIDE
6	87-070-445-010		PICK-UP,KSS-213B
8	83-ZG2-227-01K		TURN TABLE,C1
A	87-261-032-219		SCREW V+2-3

CD MECHANISM EXPLODED VIEW 1 ／ 1 (3ZG-2 C1N <V3L/V4L/V5>)



CD MECHANISM PARTS LIST 1 ／ 1 (3ZG-2 C1N <V3L/V4L/V5>)

DESCRIPTIONで判断できない物は "REFERENCE NAME LIST" を参照してください。
If can't understand for Description please kindly refer to "REFERENCE NAME LIST".

REF. NO	PART NO.	ｶﾝﾘ NO.	DESCRIPTION
1	83-ZG2-202-71K		O-SERT S ASSY,S
2	83-ZG2-204-419		GEAR,A
3	83-ZG2-205-219		GEAR,B
4	83-ZG2-220-01K		GEAR MOTOR 2
5	83-ZG2-207-119		SHAFT,SLIDE
6	87-070-445-010		PICK-UP,KSS-213B
8	83-ZG2-233-019		TURN TABLE,A5
9	87-045-358-019		MOT,RF-310T A 43
10	87-045-356-019		MOT,RF-310T A 30
A	87-261-032-219		SCREW V+2-3

4ZG-1A

ELECTRICAL MAIN PARTS LIST

DESCRIPTION で判断できない物は "REFERENCE NAME LIST" を参照してください。
If can't understand for Description please kindly refer to "REFERENCE NAME LIST".

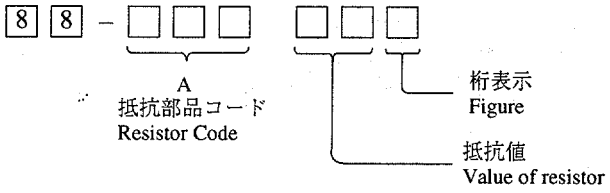
REF. NO.	PART NO.	カンリ NO.	DESCRIPTION
IC			
	87-070-294-019		IC,CXD2508AQ
	87-017-745-019		IC,CXA1782BQ
	87-017-888-089		IC,NJM4558MD
	87-070-305-019		IC,BA6897S
	87-001-982-019		IC,TA7291S
	87-017-802-010		IC,LC7872E<G>
	87-017-803-010		IC,LC32464P-80<G>
TRANSISTOR			
	87-026-239-089		C-TR,DTC114TK
	89-110-373-089		C-TR,2SA1037 S
	89-420-052-089		TR 2SD2005Q (T105)
	89-421-722-389		TR,2SD2172 V/W
	89-320-011-089		TR,2SC2001K
	87-026-223-089		C-TR,DTC143TK
	89-113-187-089		TR,2SA1318TU
	87-026-608-089		C-TR,DTC 123 JK
	89-406-555-089		TR,2SD655E<G>
	87-A30-039-040		C-TR,2SD1383K<D>
DIODE			
	87-020-465-089		DIODE,1SS133
	87-020-330-089		C-DIODE,DAP202K
3CD C.B			
C101	87-010-194-089		C-CAP,S 0.047-25 F
C102	87-010-180-089		C-CAP,S 1500P-50 B
C103	87-018-134-089		CAP,TC-U 0.01-16 Y
C104	87-012-156-089		C-CAP,S 220P-50 CH
C105	87-015-698-049		CAP,E 4.7-50 7L
C106	87-010-060-049		CAP,E 100-16 7L
C107	87-010-197-089		C-CAP,S 0.01-25 B
C108	87-016-461-089		C-CAP,S 0.47-16 F
C109	87-010-197-089		C-CAP,S 0.01-25 B
C115	87-010-318-089		C-CAP,S 47P-50 CH
C116	87-010-318-089		C-CAP,S 47P-50 CH
C117	87-010-197-089		C-CAP,S 0.01-25 B
C118	87-010-260-089		CAP,E 47-25 SME
C119	87-018-134-089		CAP,TC-U 0.01-16 Y<EXCEPT G>
C120	87-018-209-080		CAP,TC-U 0.1-50 F
C121	87-018-134-089		CAP,TC-U 0.01-16 Y
C151	87-010-182-089		C-CAP,S 2200P-50 B
C152	87-010-196-089		C-CAP,S 0.1-25 F
C153	87-010-196-089		C-CAP,S 0.1-25 F
C154	87-010-196-089		C-CAP,S 0.1-25 F
C155	87-010-404-089		CAP,E 4.7-50 SME
C156	87-010-193-089		C-CAP,S 0.033-25 F
C157	87-010-197-089		C-CAP,S 0.01-25 B
C158	87-010-401-089		CAP,E 1-50 SME
C159	87-010-382-089		CAP,E 22-25 SME
C160	87-010-213-089		C-CAP,S 0.015-25 B
C161	87-018-134-089		CAP,TC-U 0.01-16 Y
C162	87-010-263-089		CAP,E 100-10 SME 5X11
C163	87-010-197-089		C-CAP,S 0.01-25 B
C164	87-010-193-089		C-CAP,S 0.033-25 F
C165	87-010-197-089		C-CAP,S 0.01-25 B
C166	87-010-193-089		C-CAP,S 0.033-25 F
C167	87-010-197-089		C-CAP,S 0.01-25 B
C169	87-010-150-089		C-CAP,S 6P-50 CH
C170	87-010-263-089		CAP,E 100-10 SME 5X11
C171	87-010-178-089		C-CAP,S 1000P-50 B
C172	87-010-198-089		C-CAP,S 0.022-25 B
C173	87-010-196-089		C-CAP,S 0.1-25 F
C174	87-010-197-089		C-CAP,S 0.01-25 B
C175	87-010-263-089		CAP,E 100-10 SME 5X11
C176	87-010-248-089		CAP,E 220-10 SME
C177	87-010-197-089		C-CAP,S 0.01-25 B
C178	87-010-260-089		CAP,E 47-25 SME
C179	87-010-196-089		C-CAP,S 0.1-25 F
C180	87-010-196-089		C-CAP,S 0.1-25 F
C201	87-010-318-089		C-CAP,S 47P-50 CH
C202	87-010-318-089		C-CAP,S 47P-50 CH
C203	87-010-321-089		C-CAP,S 82P-50 CH
C204	87-010-321-089		G-CAP,S 82P-50 CH
C205	87-010-321-089		C-CAP,S 82P-50 CH
C206	87-010-321-089		C-CAP,S 82P-50 CH
C207	87-012-153-089		C-CAP,S 120P-50 CH
C208	87-012-153-089		C-CAP,S 120P-50 CH
C209	87-012-153-089		C-CAP,S 120P-50 CH
C210	87-012-153-089		C-CAP,S 120P-50 CH
C211	87-010-405-049		CAP,E 10-50 SME
C212	87-010-405-049		CAP,E 10-50 SME
C213	87-010-186-089		C-CAP,S 4700P-50 B
C214	87-010-186-089		C-CAP,S 4700P-50 B
C231	87-010-112-089		CAP,E 100-16 11L
C232	87-010-060-049		CAP,E 100-16 7L
C301	87-010-196-089		C-CAP,S 0.1-25 F
C302	87-010-260-089		CAP,E 47-25 SME
C501	87-010-221-049		CAP,E 470-10 SME
C502	87-010-197-089		C-CAP,S 0.01-25 B
C503	87-010-263-089		CAP,E 100-10 SME 5X11
C504	87-010-196-089		C-CAP,S 0.1-25 F
C505	87-010-196-089		C-CAP,S 0.1-25 F
C506	87-010-196-089		C-CAP,S 0.1-25 F
C507	87-010-196-089		C-CAP,S 0.1-25 F
C508	87-010-221-049		CAP,E 470-10 SME
C509	87-010-196-089		C-CAP,S 0.1-25 F
C510	87-010-196-089		C-CAP,S 0.1-25 F
C511	87-010-185-089		C-CAP,S 3900P-50 B
C601	87-010-197-089		C-CAP,S 0.01-25 B
C602	87-010-381-089		CAP,E 330-16 SME
C603	87-010-196-089		C-CAP,S 0.1-25 F
C604	87-010-137-080		CAP,E,22-16 BP
C701	87-010-322-089		C-CAP,S 100P-50 CH
C702	87-010-322-089		C-CAP,S 100P-50 CH
C703	87-010-318-089		C-CAP,S 47P-50 CH
C704	87-010-178-089		C-CAP,S 1000P-50 B
C705	87-010-178-089		C-CAP,S 1000P-50 B
C712	87-010-982-049		CAP,E 33-25 GAS
C801	87-010-197-089		C-CAP,S 0.01-25 B<G>
C802	87-010-260-089		CAP,E 47-25 SME<G>
C803	87-010-194-089		C-CAP,S 0.047-25 F<G>
C804	87-010-260-089		CAP,E 47-25 SME<G>
C805	87-018-134-089		CAP,TC-U 0.01-16 Y<G>
C806	87-010-260-089		CAP,E 47-25 SME<G>
C807	87-010-405-089		CAP,E 10-50 SME<G>
C808	87-010-197-089		C-CAP,S 0.01-25 B<G>
C809	87-010-405-049		CAP,E 10-50 SME<G>
C810	87-010-313-089		C-CAP,S 18P-50 CH<G>
C811	87-010-314-089		C-CAP,S 22P-50 CH<G>
C812	87-010-313-089		C-CAP,S 18P-50 CH<G>
C813	87-010-315-089		C-CAP,S 27P-50 CH<G>

REF. NO.	PART NO.	カンリ NO.	DESCRIPTION
C814	87-010-197-089		C-CAP,S 0.01-25 B<G>
C815	87-010-260-049		CAP,E 47-25 SME<G>
C816	87-010-404-089		CAP,E 4.7-50 SME<G>
C817	87-010-221-089		CAP,E 470-10<G>
C818	87-010-196-089		C-CAP,S 0.1-25 F<G>
C819	87-010-321-089		C-CAP,S 82P-50 CH<G>
C820	87-010-178-089		C-CAP,S 1000P-50 B<G>
C821	87-010-196-089		C-CAP,S 0.1-25 F<G>
C822	87-010-197-089		C-CAP,S 0.01-25 B<G>
C901	87-010-260-089		CAP,E 47-25 SME<D>
C902	87-010-196-089		C-CAP,S 0.1-25 F<D>
CON2	84-ZG1-616-019		CONN ASSY,6P H
EMI801	87-008-474-089		F-BEAD,EMI BL02RN1<G>
EMI802	87-008-474-089		F-BEAD,EMI BL02RN1<G>
FC1	85-NFT-611-119		FF-CABLE,16P-1.0
FC4	84-ZG1-614-219		CABLE,FFC 5P-1.25
J801	87-009-502-010		JACK,PIN 1PY EARTH<G>
LED901	87-A40-123-019		LED,SLZ-8128A-01-B<D>
M601	87-045-305-019		MOTOR, RF-500TB
R177	87-022-365-089		C-RES,S 100K-1/10W F
R178	87-022-363-089		C-RES,S 68K-1/10W F
R179	87-022-363-089		C-RES,S 68K-1/10W F
R180	87-022-363-089		C-RES,S 68K-1/10W F
R181	87-022-363-089		C-RES,S 68K-1/10W F
R182	87-022-365-089		C-RES,S 100K-1/10W F
R401	87-022-186-089		C-RES,82-1/4W J
R403	87-022-186-089		C-RES,82-1/4W J
SFR151	87-024-175-089		SFR,47K DIA6 V
SFR152	87-024-176-089		SFR,100K DIA6 V
SFR153	87-024-176-089		SFR,100K DIA6 V

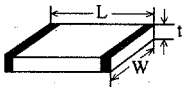
REF. NO.	PART NO.	カンリ NO.	DESCRIPTION
SW701	87-036-109-019		SW,PUSH SPPB 61
SW702	87-036-109-019		SW,PUSH SPPB 61
X101	87-030-402-089		VIB,XTAL 16.9344 MHZ
X801	80-JUC-602-089		VIB,XTAL 17.73MHZ<G>
X802	80-JUC-601-089		VIB,XTAL 14.31MHZ<G>
LED C.B			
LED701	87-070-200-089		LED,SLP636C-81-S-T1
LED702	87-017-350-080		LED,SEL1550CM
LED703	87-017-350-080		LED,SEL1550CM
LED704	87-070-200-089		LED,SLP636C-81-S-T1
T-T C.B			
C401	87-018-214-089		CAP TC U 0.1-50 F
M401	87-045-364-019		MOTOR,(BCH3B14)
PS401	87-026-573-019		P-SNSR,GP1S53V
MOTOR C.B			
M2	9X-262-513-210		SLED MOTOR ASSY
PIN3	91-564-722-110		CONNECTOR 6P
SW1	91-572-085-110		LEAF SW

○ チップ抵抗部品コード／CHIP RESISTOR PART CODE

チップ抵抗部品コードの成り立ち
Chip Resistor Part Coding



チップ抵抗
Chip resistor

容量 Wattage	種類 Type	許容誤差 Tolerance	記号 Symbol	寸法／Dimensions (mm) 外形／Form	L	W	t	抵抗コード：A Resistor Code: A
1／16W	1608	±5%	CJ		1.6	0.8	0.45	108
1／10W	2125	±5%	CJ		2	1.25	0.45	118
1／8W	3216	±5%	CJ		3.2	1.6	0.55	128

Refer to the following pages for the 4ZG-1 and the common sections.

■ IC DESCRIPTION

CXA1782BQ ..... See page 64

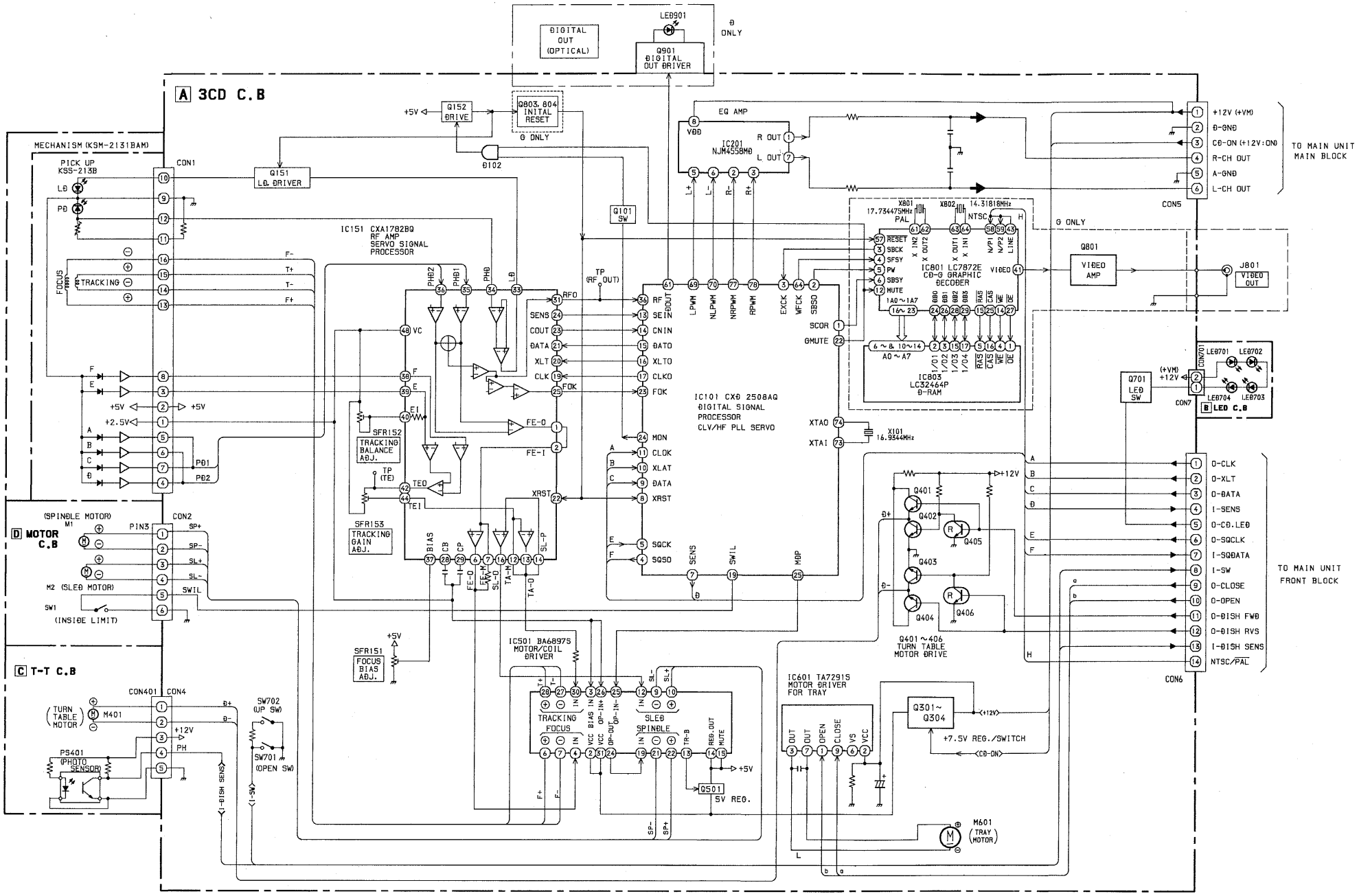
LC7872E ..... See page 62

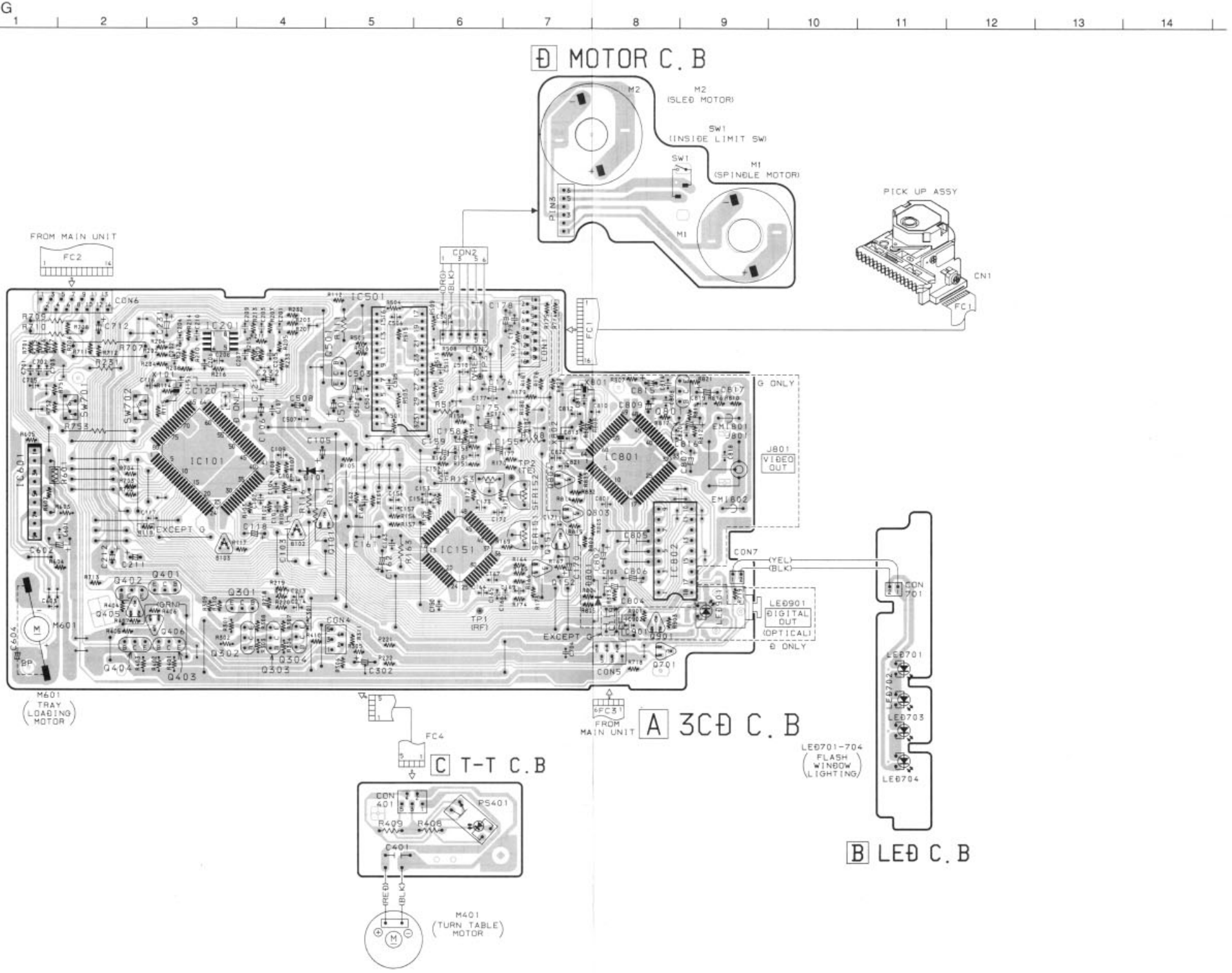
■ MECHANICAL EXPLODED VIEW 1 ／ 1

See page 95

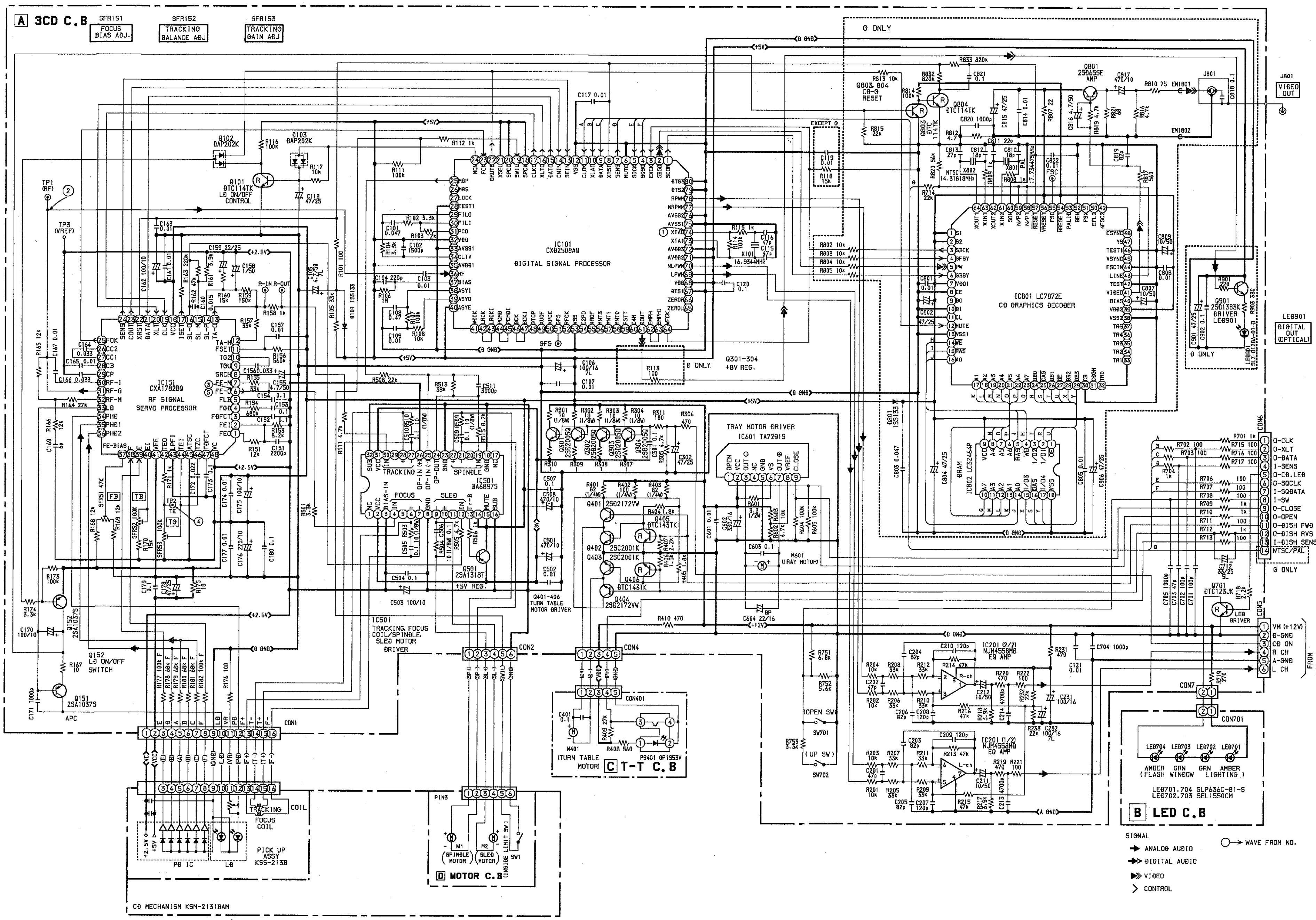
■ MECHANICAL PARTS LIST 1 ／ 1

See page 96


A 3CD C.B
DIGITAL OUT (OPTICAL)
LED901
Q901 DIGITAL OUT DRIVER
ONLY
MECHANISM (KSM-213BAM)
PICK UP KSS-213B
CON1
Q151 LD DRIVER
Q152 DRIVE
Q803, 804 INITAL RESET
G ONLY
D102
Q101 SW
IC151 CXA1782BQ RF AMP SERVO SIGNAL PROCESSOR
IC101 CXD 2508AQ DIGITAL SIGNAL PROCESSOR CLV/HF PLL SERVO
EQ AMP
IC201 NJM4558MD
R OUT
L OUT
X801 17.734475MHz PAL
X802 14.31818MHz NTSC
IC801 LC7872E CD-G GRAPHIC DECODER
IC803 LC32464P D-RAM
Q801 VIDEO AMP
J801 VIDEO OUT
X101 16.9344MHz
Q701 LED SW
LED701 LED702 LED703 LED704
B LED C.B
CON5
CON6
CON7
+12V (+VM)
D-GND
CD-ON (+12V:ON)
R-CH OUT
A-GND
L-CH OUT
TO MAIN UNIT MAIN BLOCK
D-CLK
D-XLT
D-DATA
I-SENS
D-CD.LED
D-SQCLK
I-SQDATA
I-SW
D-CLOSE
D-OPEN
D-DISH FWD
D-DISH RVS
I-DISH SENS
NTSC/PAL
TO MAIN UNIT FRONT BLOCK
D MOTOR C.B
(SPINDLE MOTOR) M1
M2 (SLED MOTOR)
SW1 (INSIDE LIMIT)
CON2
C T-T C.B
CON401
CON4
(TURN TABLE MOTOR) M401
PS401 (PHOTO SENSOR)
SW702 (UP SW)
SW701 (OPEN SW)
SFR151 FOCUS BIAS ADJ.
SFR152 TRACKING BALANCE ADJ.
SFR153 TRACKING GAIN ADJ.
IC501 BA68975 MOTOR/COIL DRIVER
TRACKING
FOCUS
SLED
SPINDLE
Q501 5V REG.
IC601 TA7291S MOTOR DRIVER FOR TRAY
Q301~Q304
+7.5V REG./SWITCH
M601 (TRAY MOTOR)
Q401~406 TURN TABLE MOTOR DRIVE
Q401
Q402
Q403
Q404
Q405
Q406
+12V
+5V
+2.5V
TRACKING
FOCUS

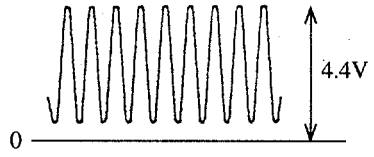

Ð MOTOR C. B
M2
(SLED MOTOR)
SW1
(INSIDE LIMIT SW)
SW1
M1
(SPINDLE MOTOR)
PIN3
PICK UP ASSY
CN1
FC1
FROM MAIN UNIT
FC2
CON2
(ORG)
(BLK)
G ONLY
J801
VIDEO
OUT
EXCEPT G
CON7
(YEL)
(BLK)
LEÐ901
ÐIGITAL
OUT
(OPTICAL)
Ð ONLY
CON
701
LEÐ701
LEÐ702
LEÐ703
LEÐ704
LEÐ701-704
(FLASH
WINÐOW
LIGHTING)
B LEÐ C. B
M601
(TRAY
LOADING
MOTOR)
FC4
C T-T C. B
CON
401
PS401
R409
R406
C401
(RED)
(BLK)
M401
(TURN TABLE)
MOTOR
FROM
MAIN UNIT
FC3
A 3CÐ C. B

SCHEMATIC DIAGRAM

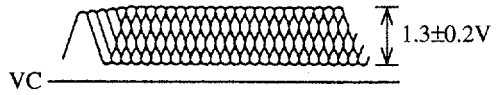


WAVE FORM

① SYSTEM CLOCK
IC101 Pin ㉔ (XTAO)
f=16.9344MHz
VOLT/DIV: 2V
TIME/DIV: 0.1μS

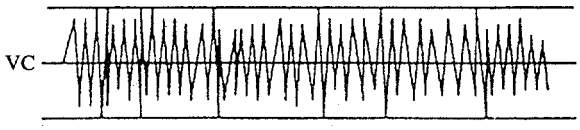


② RF
TP1 (RF)
VOLT/DIV: 500mV
TIME/DIV: 0.5μS

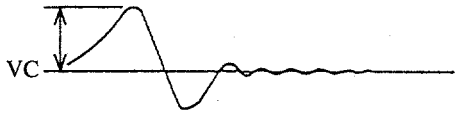


③ Focus
IC151 Pin ⑥ (FE-O)
VOLT/DIV: 200mV
TIME/DIV: 2mS

④ Tracking
TP2 (TE)
TIME/DIV: 1mS

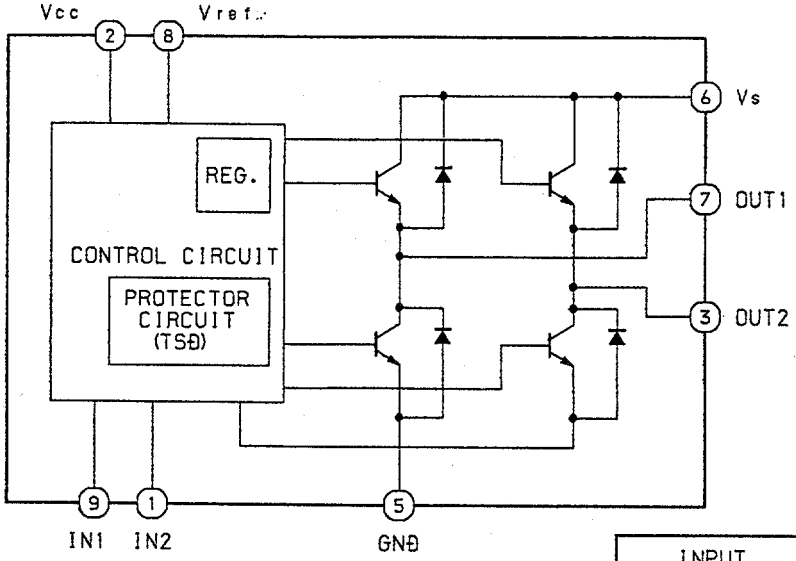


⑤ Focus Search
IC151 Pin ⑥ (FE-O)



IC BLOCK DIAGRAM

IC, TA7291



INPUT		OUTPUT		MODE
IN1	IN2	OUT1	OUT2	
0	0	∞	∞	STOP
1	0	H	L	CW
0	1	L	H	CCW
1	1	L	L	BRAKE

∞ : HI IMPEDANCE
NOTE : INPUT "H" ACTIVE

IC DESCRIPTION

IC, CXD2508AQ

Pin No.	Pin name	I/O	Description
1	SCOR	O	1H when the subcode sync S0 or S1 is detected.
2	SBSO	O	SUBP~W serial output.
3	EXCK	I	Clock input for SBSO read out.
4	SQSO	O	SUBQ 80-bit serial output.
5	SQCK	I	Clock input for SQSO read out.
6	MUTE	I	H to mute. L to cancel.
7	SENS	O	SENS signal output to CPU.
8	XRST	I	System reset. L to reset.
9	DATA	I	Serial data input from CPU .
10	XLAT	I	Latch input from CPU. Latching serial data at fall down.
11	CLOK	I	Clock input from CPU to transfer serial data.
12	VSS	—	GND.
13	SEIN	I	SENS input from SSP.
14	CNIN	I	Numbers of track jump are counted and input.
15	DATO	O	Serial data output to SSP.
16	XLTO	O	Serial data latched output to SSP. Latched at fall down edge.
17	CLKO	O	Clock input from SSP to transfer serial data.
18, 20	SPOA, C	I	Microprocessor expansion interface.
19	XTSL	I	X'tal selection input terminal. "L" at 16.9344MHz X'tal. "H" at 33.86888MHz.
22	XLON	O	Microprocessor expansion interface.
23	FOK	I	Focus OK input pin. Used for SENS output and servo auto sequencer.
24	MON	O	Spindle motor ON/OFF control output.
25	MDP	O	Spindle motor servo control output.
26	MDS	O	Spindle motor servo control output.
27	LOCK	O	GFS is sampled by 460Hz. H output when GFS is H. L output when GFS is L for 8 consecutive times.
28	TEST1	I	TEST. (Connected to GND)
29	FILO	O	Filter output to master PLL. (slave=digital PLL)
30	FILI	I	Filter input to master PLL.
31	PCO	O	Charge-pump output to master PLL.
32	VDD	—	Power supply input. (+5V)
33	AVSS1	—	GND.
34	CLTV	I	VCO control voltage input to master PLL.
35	AVDD1	—	Power supply input. (+5V)
36	RF	I	EFM signal input.
37	BIAS	I	Constant current input to asymmetry correction circuit.
38	ASYI	I	Comparate voltage input to asymmetry correction circuit.
39	ASYO	O	EFM full swing output. (L=VSS, H=VDD)
40	ASYE	I	L: asymmetry correction OFF. H: asymmetry correction ON
41	WDCK	O	D/A interface, word clock (2Fs) for 48-bit slot.
42	LRCK	O	D/A interface, LR clock (Fs) for 48-bit slot.

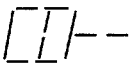
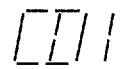
Pin No.	Pin name	I/O	Description
43	LRCKI	I	LR clock input to DAC. (48-bit slot)
44	PCMD	O	D/A interface, serial data. (2's complement, MSB first)
45	PCMDI	I	Audio data input to DAC. (48-bit slot)
46	BCK	O	D/A interface, bit clock.
47	BCKI	I	Bit clock input to DAC. (48-bit slot)
48	GTOP	O	GTOP output.
49	XUGF	O	XUFG output.
50	XPCK	O	XPLCK output.
51	GFS	O	GFS output.
52	RFCK	O	RFCK output.
53	VSS	—	GND.
54	C2PO	O	C2PO output.
55	XROF	O	XRAOF output.
56	MNT3	O	MNT3 output.
57	MNT1	O	MNT1 output.
58	MNT0	O	MNT0 output.
59	FSTT	O	Pins-73 and -74 divided-by 2/3 output.
60	C4M	O	4.2336MHz output.
61	DOUT	O	Digital Out connector output signal.
62	EMPH	O	H when the playback disc has emphasis. L when it does not.
63	EMPHI	I	DAC emphasis ON/OFF. H when ON. L when OFF
64	WFCK	O	WFCK (WRITE FRAME CLOCK) output.
65	ZEROL	O	No sound data detection output. H (L-ch) when no sound data is detected.
66	ZEROR	O	No sound data detection output. H (R-ch) when no sound data is detected.
67	DTSI	I	TEST for DAC. (Normally "L")
68	VDD	—	Power supply input. (+5V)
69	NLPWM	O	L-ch PWM output. (reversed polarity)
70	LPWM	O	L-ch PWM output. (normal polarity)
71	AVDD2	—	Power supply input to L-ch PWM driver. (Connected to +5V)
72	AVDD3	—	Power supply input to X'tal. (Connected to +5V)
73	XTAI	I	X'tal input to 33.8688MHz oscillator circuit.
74	XTAO	O	33.8688MHz X'tal oscillator circuit output.
75	AVSS1	—	GND input to X'tal. (Connected GND)
76	AVSS2	—	GND input to PWM driver. (Connected to GND)
77	NRPWM	O	R-ch PWM output. (reversed phase)
78	RPWM	O	R-ch PWM output. (normal phase)
79	DTS2	I	TEST-2 for DAC. (Normally "L")
80	DTS3	I	TEST-3 for DAC. (Normally "L")

TEST MODE

1. How to Activate CD Test Mode
   Insert the AC plug while pressing the function CD button.
   All FL display tubes will light up, and the test mode will be activated.

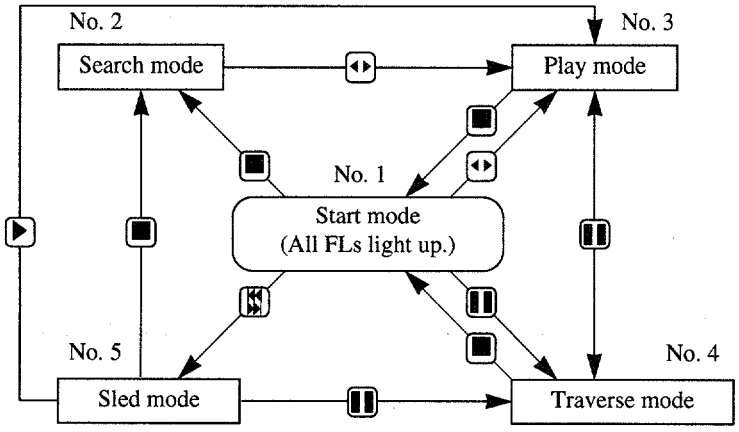
2. How to Cancel CD Test Mode
   Either one of the following operations will cancel the CD test mode.
   - Press the function button. (except CD function button)
   - Press the power switch button.
   - Disconnect the AC plug

3. CD Test Mode Functions
   When test mode is activated, the following mode functions from No.1 to No.5 can be used by pressing the operation keys.

Mode/No.	Operation	FL display	Operation	Contents
Start mode No.1	Activation	All lamps light	• Test mode is activated. • Laser diode turns always ON. (CD block power is ON.)	• FL display check (All displays light.) • APC circuit check • Laser current measurement (Laser current control. Across a resistor connected between emitter and GND.)
Search mode No.2	■ key		• Continual focus search (The pickup lens repeats the full-swing up-down motion.) * Avoid continual searches that last for more than 10 minutes. * NOTE 1	FOCUS SERVO • Check focus search waveform • Check focus error waveform (FOK/FZC are not monitored in the search mode)
Play mode No.3	◀ ▶ key		• Normal playback • Focus search is continued if TOC cannot be read. * NOTE 1	FOCUS SERVO/TRACKING SERVO CLV SERVO/SLED SERVO Check FOK/FZC
Traverse mode No.4	❚❚ key		• During normal disc playback Press once; tracking servo OFF Press twice; tracking servo ON * NOTE 2	TRACKING SERVO ON/OFF Tracking balance (traverse) adjustment
Sled mode No.5	⏮ key ⏭	All lamps light	• Pickup moves to the outermost track • Pickup moves to the innermost track * NOTE 3 (During playback, machine operates normally.)	SLED SERVO Check SLED mechanism operation

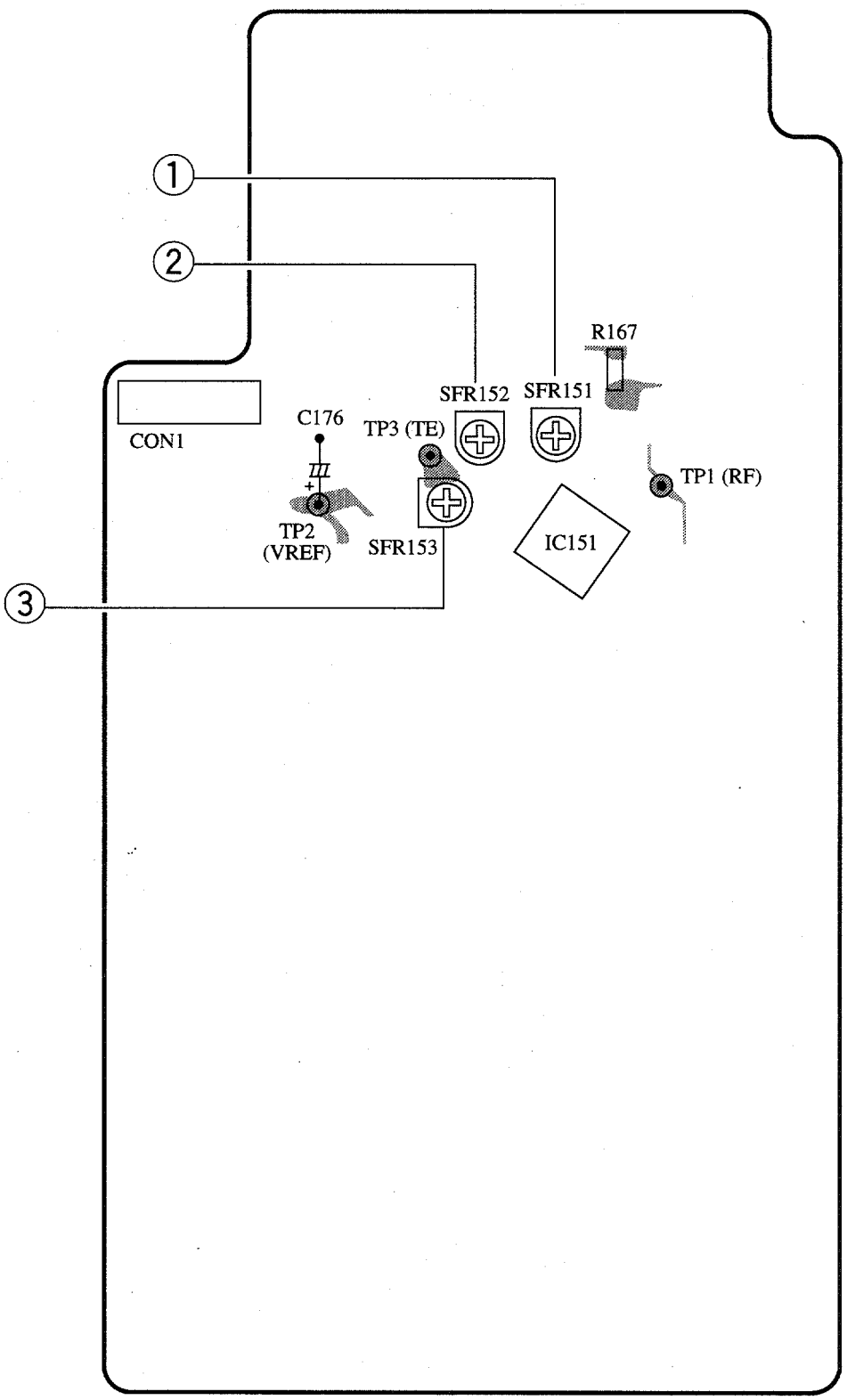
* NOTE 1: There are cases when the tracking servo cannot be locked owing to the protection circuit being operated when heat builds up in the driver IC if the focus search is operated continually for more than 10 minutes. In these cases the power supply should be switched off for 10 minutes until heat has been reduced and then re-started.
* NOTE 2: Do not press the ⏮ or ⏭ keys when the machine is in the ❚❚ status is active. If they are pressed, playback will not be possible after the ❚❚ status has been canceled. If the ⏮ or ⏭ keys are pressed in the ❚❚ status, press the ■ key and return to the start mode (No.1).
* NOTE 3: When pressing the ⏮ or ⏭ keys, take care to avoid damage to the gears. Because the sled motor is activated when the ⏮ or ⏭ keys are pressed, even when the pick-up is at the outermost or innermost track.

4. Operation Outline
   The operation of each mode is carried out in the direction of the arrows from the start mode as indicated in the following illustration.



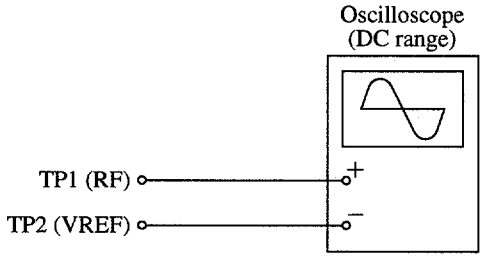
If the DISC DIRECT PLAY button is pressed, the machine performs the same operation as the PLAY button is pressed as shown. If the tray is opened by pressing OPEN/CLOSE button during Play mode or Traverse mode, the machine returns to the Start mode.

A 3CD C.B (PATTERN SIDE)

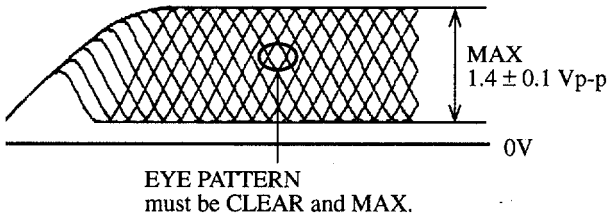


Note: • Connect a probe (10: 1) of the oscilloscope or the frequency counter to a test point.
• During adjustment, connect (⊖) pin of an oscilloscope to TP2 (VREF).

1. Focus Bias Adjustment
Make the focus bias adjustment when replacing and repairing the optical block.

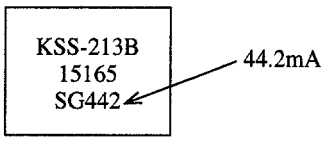


1) Connect an oscilloscope to test points TP1 (RF) and TP2 (VREF).
2) Turn on the power switch.
3) Insert test disc TCD-782 (YEDS-18) and play back the second composition.
4) Adjust SFR151 so that RF signal of test point TP1 (RF) is MAX and CLEARREST.



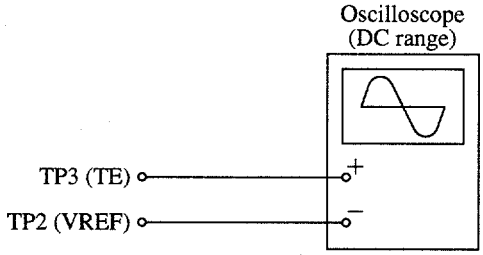
VOLT/DIV: 0.5 V
TIME/DIV: 0.5μS

Note: The current of the laser signal can be checked with the voltages on both sides of R167 (10Ω). The difference for the specified value shown on the lavel must be within±6.0mA.

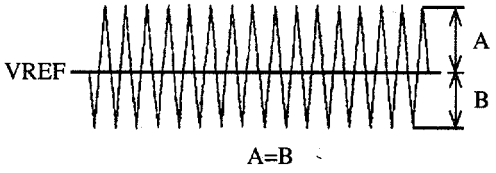


$$\text{Laser current Iop} = \frac{\text{Voltage across R167}}{10\Omega}$$

2. Tracking Balance Adjustment



1) Connect an oscilloscope to test points TP3 (TE) and TP2 (VREF).
2) Turn on the power switch.
3) Insert test disc TCD-782 (YEDS-18) and press the PLAY button.
4) Adjust SFR153 to reduce the tracking gain.
5) Adjust SFR152 so that the traverse waveform on an oscilloscope is vertically symmetrical as shown in the figure below.



VOLT/DIV: 20mV
TIME/DIV: 1mS

3. Tracking Gain Adjustment

A servo analyzer is necessary in order to perform this adjustment exactly. However, this gain has a margin, so even if it is slightly off, there is no problem. Therfore, do not perform this adjustment.
Focus/tracking gain determines the pick-up follow-up (vertical and horizontal) relative to mechanical noise and mechanical shock when 2-axis device operates. However, as these reciprocate, the adjustment is at the point where both are satisfied.

- When gain is raised, the noise increases when the 2-axis device operates.
- When gain is lowered, it is more susceptible to mechanical shock and skipping occurs more easily.

When the gain adjustment is off, the symptoms below appear.

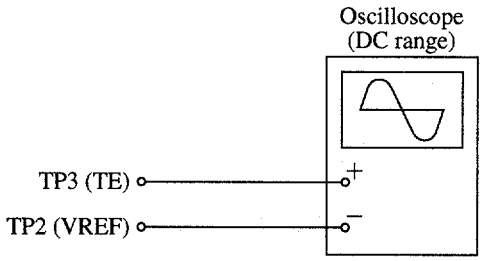
Gain / Symptoms	(Focus)	Tracking
● The time until music starts becomes longer for STOP→▶PLAY or automatic selection (⏮, ⏭ buttons pressed.) (Normally takes about 2 seconds.)	low	low or high
● Music does not start and disc continues to rotate for STOP→▶PLAY or automatic selection (⏮, ⏭ buttons pressed.)	———	low
● Disc stops to rotate shortly after STOP→▶PLAY.	low or high	———
● Sound is interrupted during PLAY. Or time counter display stops.	———	low
● More noises during the 2-axis device operation.	high	high

The following is simple adjustment method.

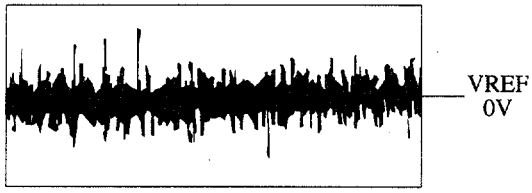
— Simple adjustment —

Note: Since the exact adjustment cannot be performed, remember the positions of the controls before the performing the adjustment. If the positions after the simple adjustment are only a little different, return the controls to the original position.

Procedure:



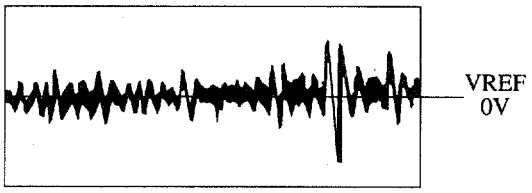
1) Keep the set horizontal. (If the set is not kept horizontally, this adjustment cannot be performed due to the gravity against the 2-axis device.)
2) Insert test disc TCD-782 (YEDS-18) and play back the second composition.
3) Connect an oscilloscope to TP3 (TE), TP2 (VREF) of the CD C.B.
4) Adjust SFR153 so that the waveform appears as shown in the figure below. (tracking gain adjustment)



VOLT/DIV: 50mV
TIME/DIV: 1mS

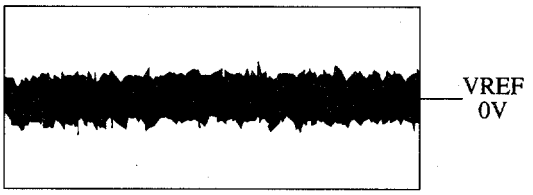
● Incorrect example

Low tracking gain
(The fundamental wave appears as compared with the waveform adjusted.)



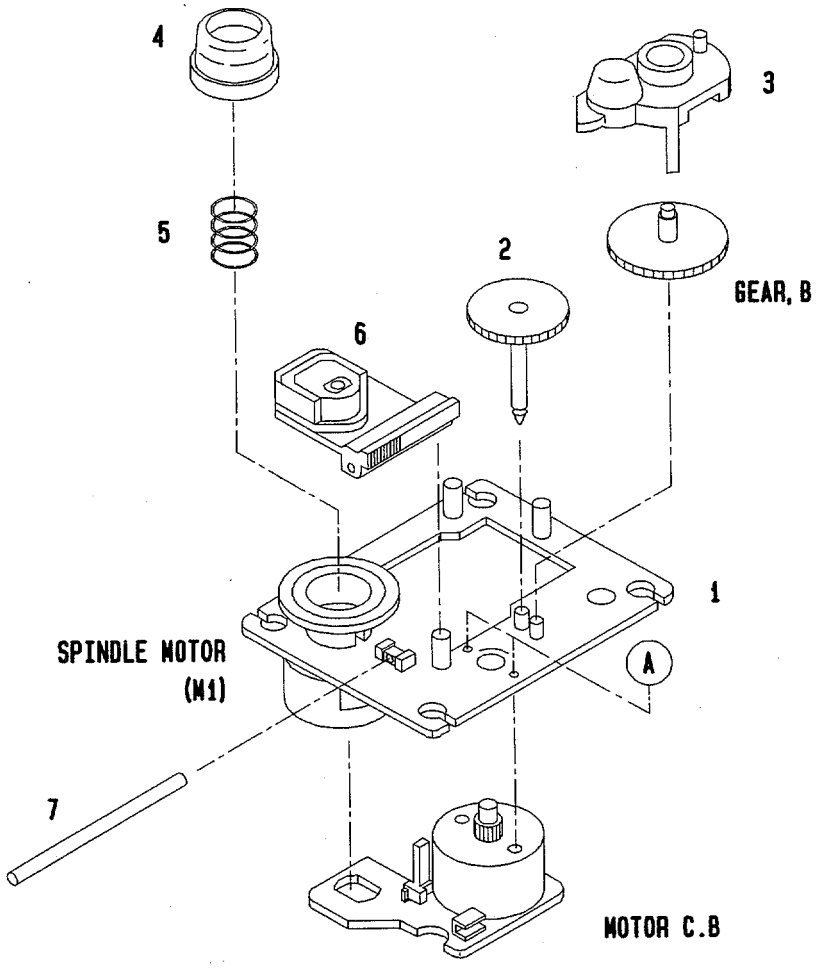
VOLT/DIV: 50mV
TIME/DIV: 1mS

High tracking gain
(The frequency of the fundamental wave is higher than that in low gain.)



VOLT/DIV: 50mV
TIME/DIV: 1mS

CD MECHANISM EXPLODED VIEW 1 ／ 1 (KSM-2131BAM <A, B>)



CD MECHANISM PARTS LIST 1 ／ 1 (KSM-2131BAM <A, B>)

DESCRIPTIONで判断できない物は "REFERENCE NAME LIST" を参照してください。
If can't understand for Description please kindly refer to "REFERENCE NAME LIST".

REF. NO	PART NO.	カンリ NO.	DESCRIPTION
1	- - -		MOTOR CHASSIS ASSY
2	92-625-188-020		GEAR(A)
3	92-625-544-010		COVER
4	92-625-186-020		RING CENTER C
5	92-625-191-010		SPRING COMPRESSION
6	87-070-445-010		OPTICAL PICK UP KSS-213B
7	94-917-565-010		SHAFT SLED
A	87-261-032-210		V+2-3

4ZG-1B

ELECTRICAL MAIN PARTS LIST

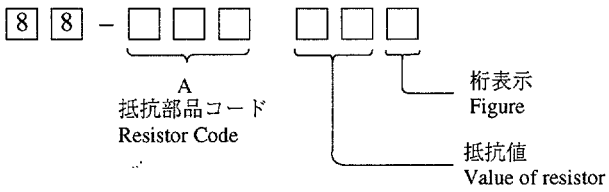
DESCRIPTION で判断できない物は “REFERENCE NAME LIST” を参照してください。
If can't understand for Description please kindly refer to “REFERENCE NAME LIST”.

REF. NO.	PART NO.	カンリ NO.	DESCRIPTION
IC			
	87-070-336-019		IC,TC 9284 BF
	87-002-407-019		IC TA8191F
	87-017-888-089		IC,NJM4558MD
	87-070-305-019		IC,BA6897S
	87-001-982-019		IC,TA7291S
	87-017-802-010		IC,LC7872E<G>
	87-017-803-010		IC,LC32464P-80<G>
TRANSISTOR			
	87-026-297-089		C-TR,DTA144TK
	89-110-373-089		C-TR,2SA1037 S
	89-420-052-089		TR 2SD2005Q (T105)
	89-421-722-389		TR,2SD2172 V/W
	89-320-011-089		TR,2SC2001K
	87-026-223-089		C-TR,DTC143TK
	89-113-187-089		TR,2SA1318TU
	87-026-608-089		C-TR,DTC 123 JK
	89-406-555-089		TR,2SD655E<G>
	87-026-239-089		C-TR,DTC114TK<G>
	89-327-125-089		C-TR,2SC2712GR<D>
DIODE			
	87-020-465-089		DIODE,1SS133
3CD C.B			
C101	87-015-819-089		CHIP CAP 0.01
C102	87-015-819-089		CHIP CAP 0.01
C103	87-015-676-089		CAP,E 47-6.3 7L
C104	87-015-676-089		CAP,E 47-6.3 7L
C106	87-010-197-089		C-CAP,S 0.01-25 B
C107	87-010-404-089		CAP,E 4.7-50 SME
C108	87-010-197-089		C-CAP,S 0.01-25 B
C109	87-010-248-049		CAP,E 220-10 SME
C110	87-010-263-049		CAP,E 100-10
C111	87-010-309-089		C-CAP,1000P-50 CH
C112	87-010-197-089		C-CAP,S 0.01-25 B
C113	87-010-184-089		C-CAP,S 3300P-50 B
C114	87-010-060-049		CAP,E 100-16 7L
C115	87-010-197-089		C-CAP,S 0.01-25 B
C116	87-010-197-089		C-CAP,S 0.01-25 B
C117	87-010-322-089		C-CAP,S 100P-50 CH
C120	87-010-314-089		C-CAP,S 22P-50 CH
C121	87-010-314-089		C-CAP,S 22P-50 CH
C123	87-010-197-089		C-CAP,S 0.01-25 B
C124	87-010-184-089		C-CAP,S 3300P-50 B
C125	87-010-805-089		C-CAP,S 1-16F
C126	87-018-134-089		CAP,TC-U 0.01-16 Y<EXCEPT G>
C127	87-010-196-089		C-CAP,S 0.1-25 F
C152	87-010-196-089		C-CAP,S 0.1-25 F
C153	87-010-154-089		C-CAP,S 10P-50 CH
C154	87-010-322-089		C-CAP,S 100P-50 CH
C155	87-010-263-089		CAP,E 100-10 SME 5X11
C156	87-010-197-089		C-CAP,S 0.01-25 B
C157	87-012-141-089		C-CAP,S 0.22-16 F
C158	87-010-545-049		CAP E 0.22-50 SME
C159	87-015-683-080		CAP,E 33-16 7L
C160	87-010-193-089		C-CAP,S 0.033-25 F
C161	87-010-197-089		C-CAP,S 0.01-25 B
C162	87-010-248-089		CAP,E 220-10 SME
C163	87-010-260-089		CAP,E 47-25 SME
C164	87-010-403-089		CAP,E 3.3-50 SME
C165	87-010-213-089		C-CAP,S 0.015-25 B
C166	87-010-187-089		C-CAP,S 5600P-50 B
C167	87-012-365-089		C-CAP,S 0.027-25V BK
C168	87-010-189-089		C-CAP,S 8200P-50 B
C169	87-015-883-089		C-CAP 0.022-25BK
C170	87-010-320-089		C-CAP,S 68P-50 CH
C171	87-010-382-089		CAP,E 22-25 SME
C172	87-010-197-089		C-CAP,S 0.01-25 B
C173	87-010-263-089		CAP,E 100-10 SME 5X11
C174	87-010-178-089		C-CAP,S 1000P-50 B
C175	87-010-805-089		C-CAP,S 1-16F
C201	87-010-318-089		C-CAP,S 47P-50 CH
C202	87-010-318-089		C-CAP,S 47P-50 CH
C203	87-010-321-089		C-CAP,S 82P-50 CH
C204	87-010-321-089		C-CAP,S 82P-50 CH
C205	87-010-321-089		C-CAP,S 82P-50 CH
C206	87-010-321-089		C-CAP,S 82P-50 CH
C207	87-012-153-089		C-CAP,S 120P-50 CH
C208	87-012-153-089		C-CAP,S 120P-50 CH
C209	87-012-153-089		C-CAP,S 120P-50 CH
C210	87-012-153-089		C-CAP,S 120P-50 CH
C211	87-010-405-049		CAP,E 10-50 SME
C212	87-010-405-049		CAP,E 10-50 SME
C213	87-010-186-089		C-CAP,S 4700P-50 B
C214	87-010-186-089		C-CAP,S 4700P-50 B
C231	87-010-112-089		CAP,E 100-16
C232	87-010-060-049		CAP,E 100-16 7L
C301	87-010-196-089		C-CAP,S 0.1-25 F
C302	87-010-260-089		CAP,E 47-25 SME
C501	87-010-221-049		CAP,E 470-10 SME
C502	87-010-197-089		C-CAP,S 0.01-25 B
C503	87-010-263-089		CAP,E 100-10 SME 5X11
C504	87-010-196-089		C-CAP,S 0.1-25 F
C505	87-010-196-089		C-CAP,S 0.1-25 F
C506	87-010-196-089		C-CAP,S 0.1-25 F
C507	87-010-196-089		C-CAP,S 0.1-25 F
C508	87-010-221-049		CAP,E 470-10 SME
C509	87-010-196-089		C-CAP,S 0.1-25 F
C510	87-010-196-089		C-CAP,S 0.1-25 F
C601	87-010-197-089		C-CAP,S 0.01-25 B
C602	87-010-381-089		CAP,E 330-16 SME
C603	87-010-196-089		C-CAP,S 0.1-25 F
C701	87-010-322-089		C-CAP,S 100P-50 CH
C702	87-010-322-089		C-CAP,S 100P-50 CH
C703	87-010-318-089		C-CAP,S 47P-50 CH
C704	87-010-178-089		C-CAP,S 1000P-50 B
C705	87-010-178-089		C-CAP,S 1000P-50 B
C712	87-010-982-049		CAP,E 33-25 GAS
C801	87-010-197-089		C-CAP,S 0.01-25 B<G>
C802	87-010-260-089		CAP,E 47-25 SME<G>
C803	87-010-194-089		C-CAP,S 0.047-25 F<G>
C804	87-010-260-089		CAP,E 47-25 SME<G>
C805	87-018-134-089		CAP,TC-U 0.01-16 Y<G>
C806	87-010-260-089		CAP,E 47-25 SME<G>
C807	87-010-405-089		CAP,E 10-50 SME<G>
C808	87-010-197-089		C-CAP,S 0.01-25 B<G>
C809	87-010-405-049		CAP,E 10-50 SME<G>
C810	87-010-313-089		C-CAP,S 18P-50 CH<G>
C811	87-010-314-089		C-CAP,S 22P-50 CH<G>
C812	87-010-313-089		C-CAP,S 18P-50 CH<G>

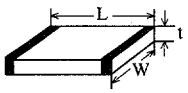
REF. NO.	PART NO.	カンリ NO.	DESCRIPTION
C813	87-010-315-089		C-CAP,S 27P-50 CH<G>
C814	87-010-197-089		C-CAP,S 0.01-25 B<G>
C815	87-010-260-049		CAP,E 47-25 SME<G>
C816	87-010-404-089		CAP,E 4.7-50 SME<G>
C817	87-010-221-089		CAP,E 470-10<G>
C818	87-010-196-089		C-CAP,S 0.1-25 F<G>
C819	87-010-321-089		C-CAP,S 82P-50 CH<G>
C820	87-010-178-089		C-CAP,S 1000P-50 B<G>
C821	87-010-196-089		C-CAP,S 0.1-25 F<G>
C822	87-010-403-089		CAP,E 3.3-50 SME<G>
C824	87-018-134-089		CAP,TC-U 0.01-16 Y
C901	87-010-260-089		CAP,E 47-25 SME<D>
C902	87-010-196-089		C-CAP,S 0.1-25 F<D>
CON2	84-ZG1-616-019		CONN ASSY,6P H
EMI801	87-008-474-089		F-BEAD,EMI BL02RN1<G>
EMI802	87-008-474-089		F-BEAD,EMI BL02RN1<G>
FC1	85-NFT-611-119		FF-CABLE,16P-1.0
FC4	84-ZG1-614-219		CABLE,FFC 5P-1.25
J801	87-009-502-010		JACK,PIN 1PY EARTH<G>
LED901	87-A40-123-019		LED,SLZ-8128A-01-B<D>
M601	87-045-305-019		MOTOR, RF-500TB
R184	87-022-361-089		C-RES,S 47K-1/10W F
R185	87-022-361-089		C-RES,S 47K-1/10W F
R186	87-022-361-089		C-RES,S 47K-1/10W F
R187	87-022-361-089		C-RES,S 47K-1/10W F
R188	87-022-361-089		C-RES,S 47K-1/10W F
R189	87-022-361-089		C-RES,S 47K-1/10W F
R401	87-022-186-089		C-RES,82-1/4W J
R403	87-022-186-089		C-RES,82-1/4W J
SFR151	87-024-176-089		SFR,100K DIA6 V
SFR152	87-024-171-089		SFR 4.7K DIA6 V
SW701	87-036-109-019		SW,PUSH SPPB 61
SW702	87-036-109-019		SW,PUSH SPPB 61
X101	87-030-402-089		VIB,XTAL 16.9344 MHZ
X801	80-JUC-602-089		VIB,XTAL 17.73MHZ<G>
X802	80-JUC-601-089		VIB,XTAL 14.31MHZ<G>
LED C.B			
LED701	87-070-200-089		LED,SLP636C-81-S-T1
LED702	87-017-350-080		LED,SEL1550CM
LED703	87-017-350-080		LED,SEL1550CM
LED704	87-070-200-089		LED,SLP636C-81-S-T1
T-T C.B			
C401	87-018-214-089		CAP TC U 0.1-50 F
M401	87-045-364-019		MOTOR,(BCH3B14)
PS401	87-026-573-019		P-SNSR,GP1S53V
MOTOR C.B			
M2	9X-262-513-210		SLED MOTOR ASSY
PIN3	91-564-722-110		CONNECTOR 6P
SW1	91-572-085-110		LEAF SW

○ チップ抵抗部品コード／CHIP RESISTOR PART CODE

チップ抵抗部品コードの成り立ち
Chip Resistor Part Coding



チップ抵抗
Chip resistor

容量 Wattage	種類 Type	許容誤差 Tolerance	記号 Symbol	寸法／Dimensions (mm) 外形／Form	L	W	t	抵抗コード ：A Resistor Code: A
1／16W	1608	±5%	CJ		1.6	0.8	0.45	108
1／10W	2125	±5%	CJ		2	1.25	0.45	118
1／8W	3216	±5%	CJ		3.2	1.6	0.55	128

Refer to the following pages for the 4ZG-1 and the common sections.

■ IC DESCRIPTION

LC7872E ..... See page 62

■ MECHANICAL EXPLODED VIEW 1 ／ 1

See page 95

■ MECHANICAL PARTS LIST 1 ／ 1

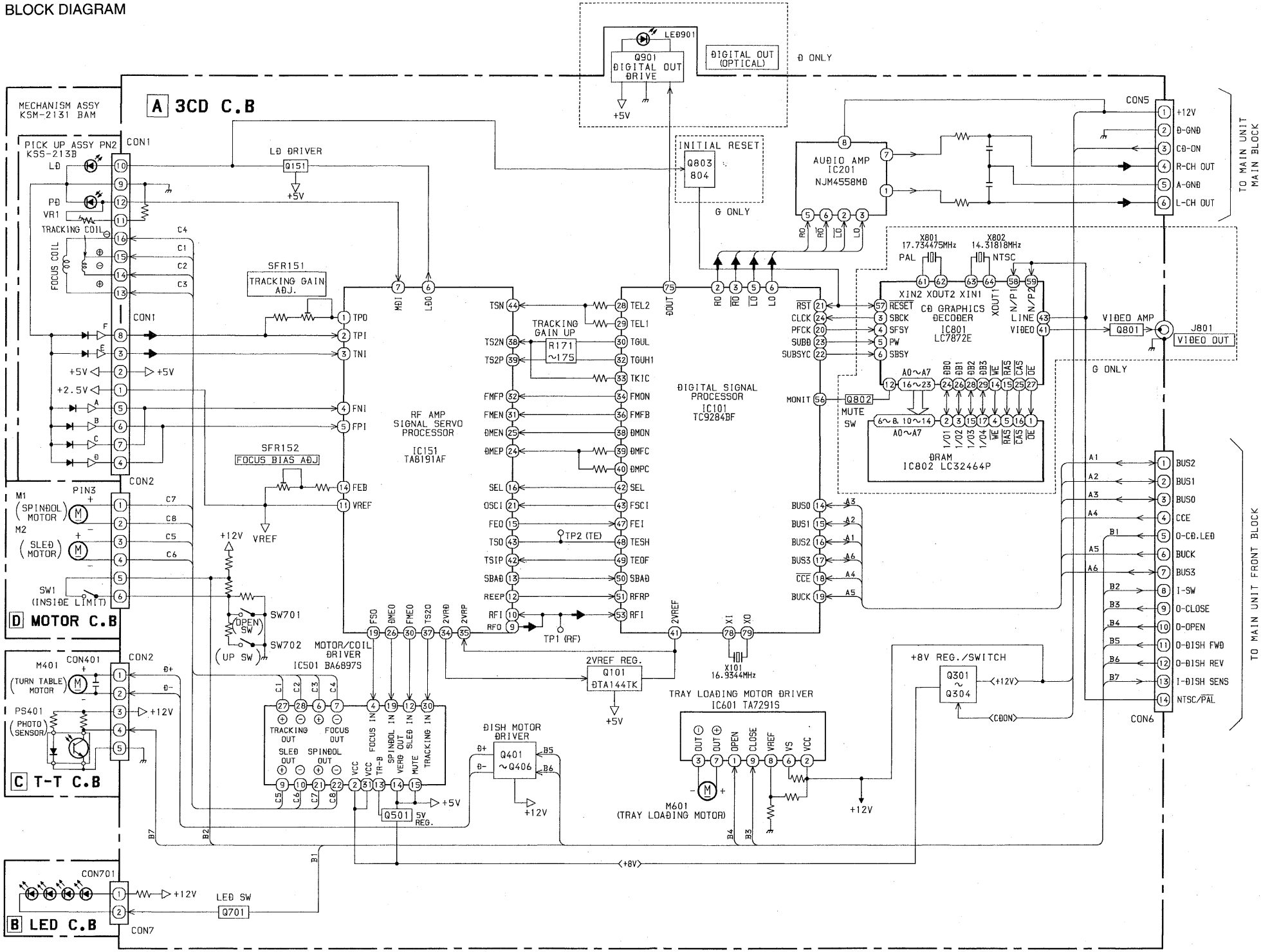
See page 96

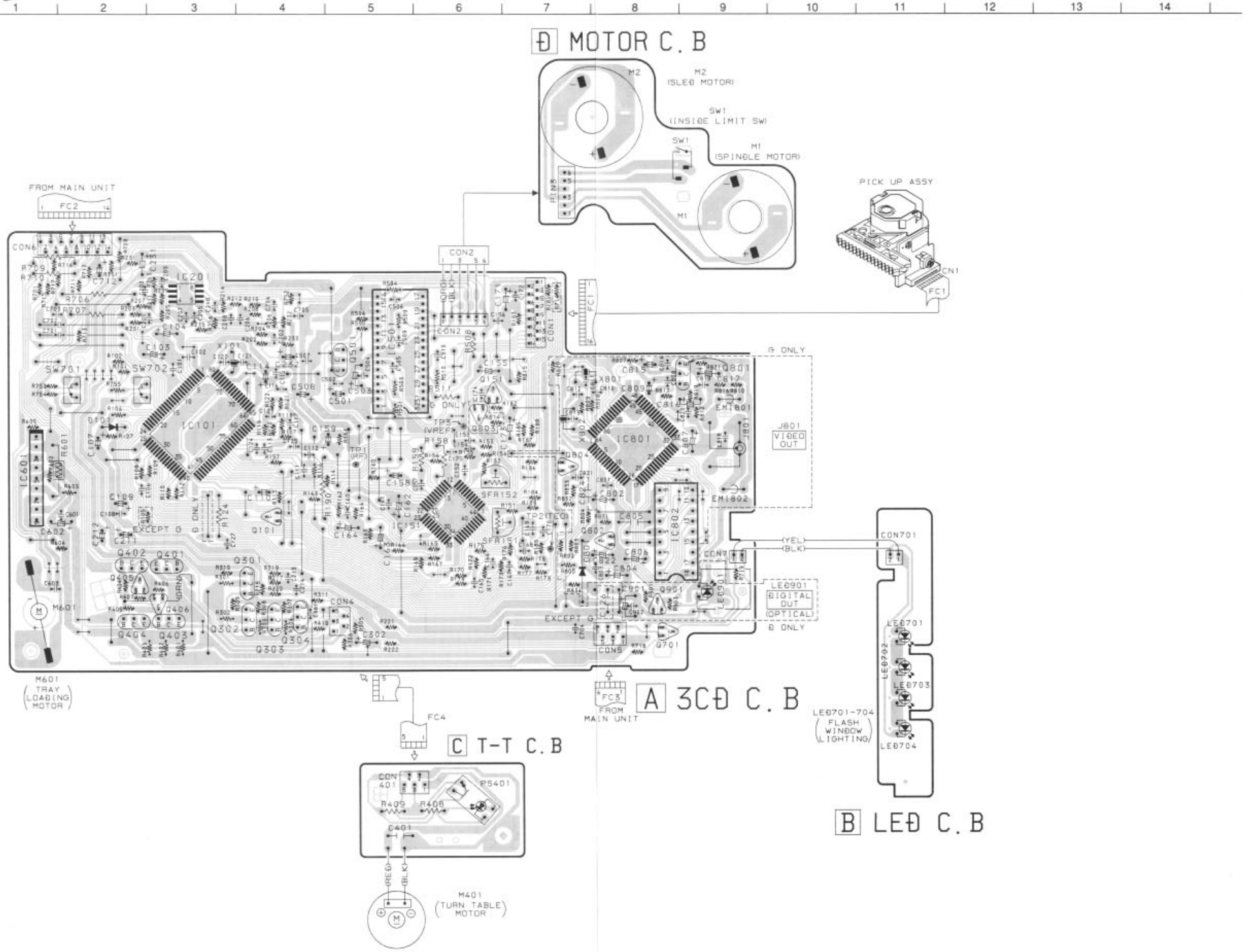
■ CD MECHANISM EXPLODED VIEW 1 ／ 1

See page 114

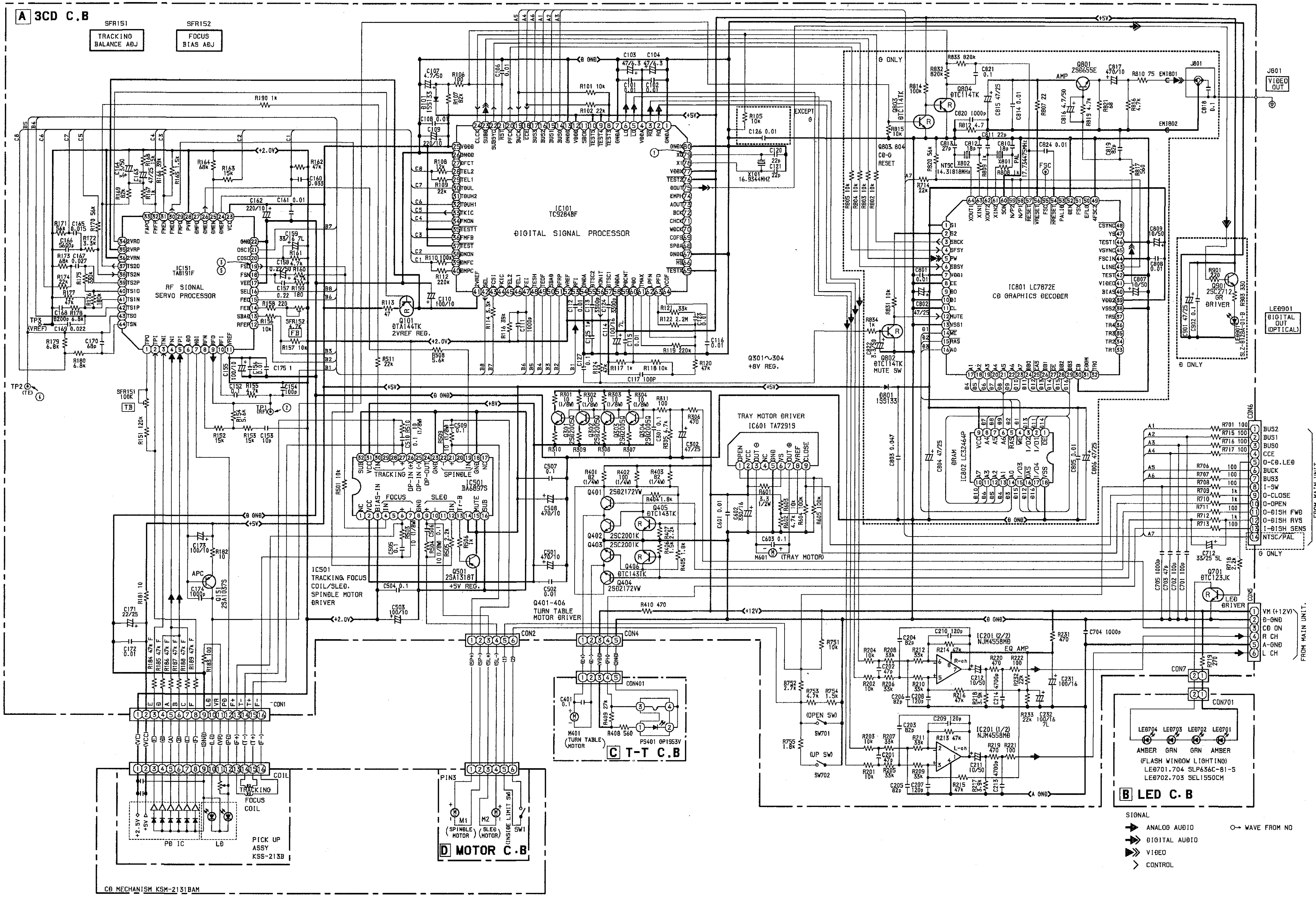
■ CD MECHANISM PARTS LIST 1 ／ 1

See page 114


A 3CD C.B
MECHANISM ASSY KSM-2131 BAM
PICK UP ASSY PN2 KSS-213B
CON1
LD
PD
VR1
TRACKING COIL
FOCUS COIL
LD DRIVER
Q151
+5V
SFR151
TRACKING GAIN ADJ.
SFR152
FOCUS BIAS ADJ
CON2
M1 SPINDOL MOTOR
M2 SLED MOTOR
SW1 (INSIDE LIMIT)
D MOTOR C.B
VREF
+12V
SW701 (OPEN SW)
SW702 (UP SW)
MOTOR/COIL DRIVER IC501 BA6897S
M401 TURN TABLE MOTOR
CON401
PS401 PHOTO SENSOR
C T-T C.B
CON701
LED SW
Q701
B LED C.B
CON7
LED901
Q901 DIGITAL OUT DRIVE
DIGITAL OUT (OPTICAL)
D ONLY
INITIAL RESET
Q803 804
G ONLY
AUDIO AMP IC201 NJM4558MD
CON5
+12V
D-GND
CD-ON
R-CH OUT
A-GND
L-CH OUT
TO MAIN UNIT MAIN BLOCK
X801 17.734475MHz
X802 14.31818MHz
PAL
NTSC
XIN2 XOUT2 XIN1
CD GRAPHICS DECODER IC801 LC7872E
VIDEO AMP Q801
J801 VIDEO OUT
Q802 MUTE SW
DRAM IC802 LC32464P
RF AMP SIGNAL SERVO PROCESSOR IC151 TA8191AF
TRACKING GAIN UP
R171 ~175
DIGITAL SIGNAL PROCESSOR IC101 TC9284BF
TP2 (TE)
TP1 (RF)
2VREF REG. Q101 DTA144TK
X101 16.9344MHz
+8V REG./SWITCH Q301 ~ Q304
CDON
TRAY LOADING MOTOR DRIVER IC601 TA7291S
M601 (TRAY LOADING MOTOR)
DISH MOTOR DRIVER Q401 ~Q406
Q501 5V REG.
TRACKING OUT
FOCUS OUT
SLED OUT
SPINDOL OUT
FOCUS IN
SPINDOL IN
SPINDOL OUT
SLED IN
MUTE
TRACKING IN
TO MAIN UNIT FRONT BLOCK
CON6
BUS2
BUS1
BUS0
CCE
D-CD.LED
BUCK
BUS3
I-SW
D-CLOSE
D-OPEN
D-DISH FWD
D-DISH REV
D-DISH SENS
NTSC/PAL

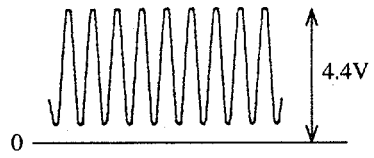

Ð MOTOR C. B
M2
(SLEÐ MOTOR)
SW1
(INSIÐE LIMIT SW)
SW1
M1
(SPINÐLE MOTOR)
PICK UP ASSY
CN1
FC1
FROM MAIN UNIT
FC2
CON2
G ONLY
JB01
VIÐEO
OUT
EXCEPT G
Ð ONLY
(YEL)
(BLK)
CON701
LEÐ901
ÐIGITAL
OUT
(OPTICAL)
LEÐ701
LEÐ702
LEÐ703
LEÐ704
LEÐ701-704
(FLASH
WINÐOW
LIGHTING)
B LEÐ C. B
M601
(TRAY
LOAÐING
MOTOR)
FC4
C T-T C. B
CON
401
P5401
R409
R408
C401
(RED)
(BLK)
M401
(TURN TABLE)
MOTOR
FC3
FROM
MAIN UNIT
A 3CÐ C. B

SCHEMATIC DIAGRAM

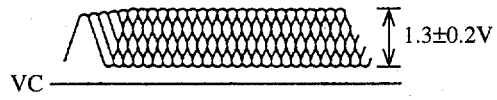


WAVE FORM

① SYSTEM CLOCK
IC101 Pin ⑲ (XO)
f=16.9344MHz
VOLT/DIV: 2V
TIME/DIV: 0.1μS

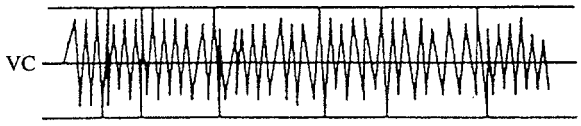


② RF
TP1 (RF)
VOLT/DIV: 500mV
TIME/DIV: 0.5μS

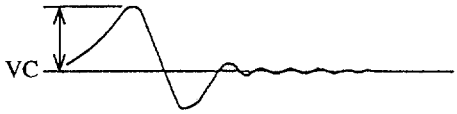


③ Focus
IC151 Pin ⑲ (FSO)
VOLT/DIV: 200mV
TIME/DIV: 2mS

④ Tracking
TP2 (TE)
TIME/DIV: 1mS

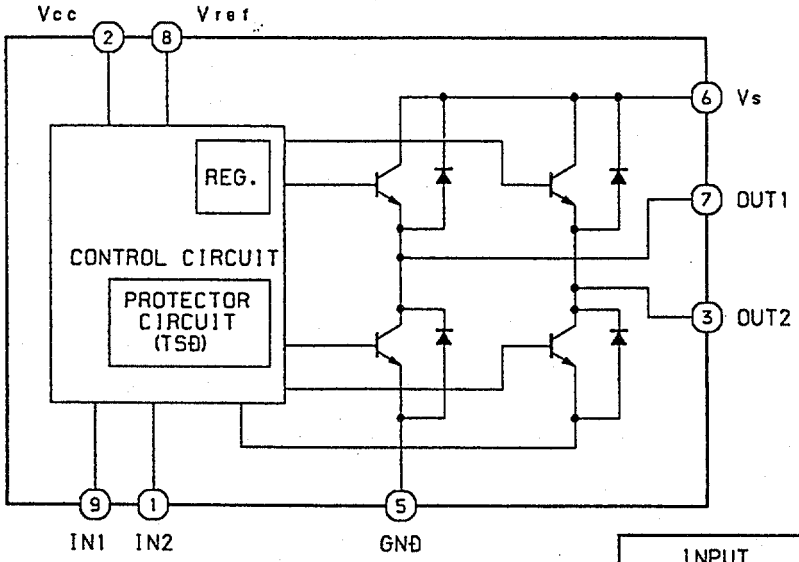


⑤ Focus Search
IC151 Pin ⑲ (FSO)



IC BLOCK DIAGRAM

IC, TA7291



INPUT		OUTPUT		MODE
IN1	IN2	OUT1	OUT2	
0	0	∞	∞	STOP
1	0	H	L	CW
0	1	L	H	CCW
1	1	L	L	BRAKE

∞ : HI IMPEDANCE
NOTE : INPUT "H" ACTIVE

IC DESCRIPTION

IC, TC9284BF

Pin No.	Pin name	I/O	Description
1	GNDA	—	D/A converter R-channel analog GND.
2	RO	O	R-channel data positive output.
3	$\overline{RO}$	O	R-channel data inverted output.
4	VDA	—	D/A converter power supply.
5	$\overline{LO}$	O	L-channel data inverted output.
6	LO	O	L-channel data positive output.
7	GNDA	—	D/A converter L-channel analog GND.
8～10	$\overline{TEST3}$～$\overline{TEST5}$	I	TEST pin. Normally "H" or open.
11	SBOK	O	Sub code Q data CRCC judgment result output. Judgment result OK: H
12	VDDD	—	Digital power supply. (+5 V)
13	GNDD	—	Digital GND.
14～17	BUS0～BUS3	I/O	μprocessor interface, data input/output.
18	CCE	I	μprocessor interface, chip enable signal input. When "L" : BUS 3～0 are active
19	BUCK	I	μprocessor interface, clock input.
20	PFCK	O	PB frame sync output.
21	$\overline{RST}$	I	Reset signal input. "L" at reset.
22	SUBSYC	O	Sub code block sync output. When sub code is detected,"H" at S1 position.
23	SUBD	O	Sub code P～W output.
24	CLCK	I	Sub code P～W data read clock input.
25	VDDD	—	Digital power supply. (+5 V)
26	GNDD	—	Digital GND.
27	DFCT	O	Defect detection signal output. When defect is detected: "VREF", normally "HiZ".
28	TEL2	O	Tracking gain adjustment analog switch output. "VREF" , or "HiZ".
29	TEL1	O	Tracking gain adjustment analog switch output. "VREF" , or "HiZ".
30	TGUL	O	Analog switch output for tracking servo gain up. Polarity in gain-up mode and normal mode can be selected by command.
31	TGUH2	O	Analog switch output for tracking servo gain up. "HiZ" for gain-up, normally "VREF". TGUH1 during normal playback. TGUH2: not used
32	TUGH1	O	
33	TKIC	O	Tracking actuator kick signal output. NKICx and CKICx are used for kick during tracking gain adjustment. "VREF" for outermost track."O" for moving toward inner track. Normally "HiZ".
34	FMON	O	Analog switch output to turn ON/OFF the feed servo. "HiZ" to turn ON servo. "VREF" to turn OFF servo.
35	$\overline{TEST1}$	I	TEST pin. Normally "H" or open.
36	FMFB	O	Feed motor FWD/BWD direction control signal output."2VREF" for outmost track. "O" for moving toward inner track. Normally "HiZ".
37	$\overline{TEST}$	I	TEST pin. Normally "H" or open.
38	DMON	O	Analog switch output to select gain of the disc motor drive circuit. "HiZ" for CLV servo OFF, "HiZ" or "VREF" can be selected by command.

<table>
<tr><th>Pin No.</th><th>Pin name</th><th>I/O</th><th>Description</th></tr>
<tr><td>39</td><td>DMPC</td><td>O</td><td>Disc motor CLV servo AFC signal output.
<table>
<tr><th>Operation</th><th>Command</th><th>DMFC output</th></tr>
<tr><td>Motor acceleration</td><td>DMFK</td><td>“2VREF”</td></tr>
<tr><td>CLV servo ON</td><td>DMSV</td><td>AFC signal (PWM)</td></tr>
<tr><td>Motor brake</td><td>DMBK</td><td>“L”</td></tr>
<tr><td>CLV servo OFF</td><td>DMOFF</td><td>“VREF”</td></tr>
</table></td></tr>
<tr><td>40</td><td>DMPC</td><td>O</td><td>Disc motor CLV servo APC signal output.</td></tr>
<tr><td>41</td><td>2VREF</td><td>—</td><td>Analog power supply. (twice the “VREF” voltage)</td></tr>
<tr><td>42</td><td>SEL</td><td>O</td><td>Servo mode select output. It turns ON/OFF the laser diode (LD) and focus servo.
<table>
<tr><th>SEL output</th><th>LD</th><th>Focus servo</th><th>Operating mode</th></tr>
<tr><td>“L”</td><td>OFF</td><td>OFF</td><td>LD OFF</td></tr>
<tr><td>“HiZ”</td><td>ON</td><td>OFF</td><td>Focus search</td></tr>
<tr><td>“H”</td><td>ON</td><td>ON</td><td>Focus ON (normal play)</td></tr>
</table></td></tr>
<tr><td>43</td><td>FCSI</td><td>O</td><td>Focus actuator drive signal output during focus search mode. “VDDA” to move the lens far from disc. “L” to move the lens closer to disc. Normally “HiZ”.</td></tr>
<tr><td>44</td><td>FKIC</td><td>O</td><td>Focus actuator drive signal output during focus adjustment mode.ÅgVDDAÅhto move the lens far from disc. “L” to move the lens closer to disc. Normally “HiZ”.</td></tr>
<tr><td>45, 46</td><td>FEL1, FEL2</td><td>O</td><td>Focus gain adjustment analog switch output. “VREF” or “HiZ”.</td></tr>
<tr><td>47</td><td>FEI</td><td>I</td><td>Focus error signal input.</td></tr>
<tr><td>48</td><td>TESH</td><td>I</td><td>Analog switch input to track error signal sample-and-hold.</td></tr>
<tr><td>49</td><td>TEOF</td><td>O</td><td>Focus gain adjustment analog switch output.“VREF” when tracking servo off.</td></tr>
<tr><td>50</td><td>SBAD</td><td>I</td><td>Sub beam added signal input.</td></tr>
<tr><td>51</td><td>RFRP</td><td>I</td><td>RF ripple signal input.</td></tr>
<tr><td>52</td><td>VREF</td><td>—</td><td>Analog power supply.</td></tr>
<tr><td>53</td><td>RFI</td><td>I</td><td>RF signal input.</td></tr>
<tr><td>54</td><td>GNDA</td><td>—</td><td>Analog GND.</td></tr>
<tr><td>55</td><td>DTSC2</td><td>O</td><td>Data slice control EFM signal inverted output.</td></tr>
<tr><td>56</td><td>MONI T</td><td>O</td><td>Internal signal monitored output. EFMO, PLCK or LOCK signals can be selected by command. Can be muted. (Not used)</td></tr>
<tr><td>57</td><td>DTSC 1</td><td>O</td><td>Data slice control EFM signal positive polarity output.</td></tr>
<tr><td>58</td><td>VDDA</td><td>—</td><td>Analog power supply.</td></tr>
<tr><td>59</td><td>PDCNT</td><td>I</td><td>PDO output control signal input. “L” to fix to “HiZ” forcibly. “H” : normal output.</td></tr>
<tr><td>60</td><td>PDO</td><td>O</td><td>Phase error signal between EFM and PLCK signals is output.</td></tr>
<tr><td>61</td><td>TMAX</td><td>O</td><td>TMAX detected result output.
<table>
<tr><th>TMAX detected result</th><th>TMAX output</th></tr>
<tr><td>Longer than specified cycle</td><td>“L”</td></tr>
<tr><td>Shorter than specified cycle</td><td>“VREF”</td></tr>
<tr><td>Within specified cycle</td><td>“HiZ”</td></tr>
</table></td></tr>
<tr><td>62</td><td>LPFN</td><td>I</td><td>Low-pass filter amplifier inverted input.</td></tr>
</table>

Pin No.	Pin name	I/O	Description
63	LPFO	O	Low-pass filter amplifier output.
64	VCOF	O	VCO filter output.
65	TESTX	I	TEST pin. Normally "H" or "L" .(Connected to +5 V)
66	$\overline{HS}$	O	Double speed mode output. "H" : normal speed. "L" : double speed
67	GNDD	—	Digital GND.
68	SPDA	O	Processor status signal output.
69	COFS	O	Correction circuit frame clock (7.35 kHz) output.
70	WDCK	O	Word clock (88.2 kHz) output. SUBQ, BUF0V or 1PF can be selected by the µprocessor command. (Not used)
71	CHCK	O	Channel clock (44.1 kHz) output. "L"for L-channel. "H" for R-channel.
72	BCK	O	Bit clock (1.4112 MHz) output.
73	AOUT	O	Audio data output. (Not used)
74	EMPH	O	Emphasis ON/OFF select signal. "H" : emphasis ON. "L" for emphasis OFF
75	DOUT	O	DIGITAL SIGNAL output.
76	$\overline{TEST2}$	I	TEST pin. Normally "H".
77	VDDX	—	Crystal oscillator circuit power supply.
78	XI	I	External crystal oscillator is connected. (Crystal oscillator frequency 16.9344 MHz)
79	XO	O	External crystal oscillator is connected. (Crystal oscillator frequency 16.9344 MHz)
80	GNDX	—	Crystal oscillator GND.

IC, TA8191F

Pin No.	Pin Name	I/O	Description
1	TPO	O	Sub beam I-V amplifier (TA Amp) output terminal.
2	TPI	I	Sub beam I-V amplifier (TA Amp) input terminal.
3	TNI	I	Sub beam I-V amplifier (TA Amp) input terminal.
4	FNI	I	Main beam I-V amplifier (FN Amp) input terminal.
5	FPI	I	Main beam I-V amplifier (FP Amp) input terminal.
6	LDO	O	Laser diode amplifier (LD Amp) output terminal.
7	MDI	I	Monitor photo diode amplifier (MD Amp) input terminal.
8	RFN	I	RF amplifier reversed phase input terminal.
9	RFO	O	RF amplifier output terminal.
10	RFI	I	RF ripple signal generator circuit input terminal.
11	VREF	O	Reference voltage output terminal (+2.1 V).
12	RFRP	O	RF ripple signal output terminal.
13	SBAD	O	Scar detection signal output terminal.
14	FEB	I	Focus error balance adjustment input terminal.
15	FEO	O	Focus error amplifier (FE Amp) output terminal.
16	SEL	I	Analog switch control signal input terminal.
17	VEE	—	Power supply terminal. (TA8190F; -5 V, TA8191F; GND)
18	FSN	I	Focus output amplifier (FS Amp) reversed phase input terminal.
19	FSO	O	Focus output amplifier (FS Amp) output terminal.
20	COSC	O	External capacitor to generate focus search signal is connected to this terminal.
21	OSCI	I	External input to control the built-in power supply to generate focus search signal is connected to this terminal.
22	GND	—	GND.
23	VCC	I	Power supply terminal (+5 V).
24	DMEP	I	Disc motor amplifier (DM Amp) positive phase input terminal.
25	DMEN	I	Disc motor amplifier (DM Amp) reversed phase input terminal.
26	DMEO	O	Disc motor amplifier (DM Amp) output terminal.
27	DMPO	O	Disc motor drive amplifier (DMP Amp) output terminal. (Not used).
28	PVR	I	Drive amplifier reference voltage input terminal.
29	FMPO	O	Feed motor drive amplifier (FMP Amp) output terminal. (Not used).
30	FMEO	O	Feed motor amplifier (FM Amp) output terminal.
31	FMEN	I	Feed motor amplifier (FM Amp) reversed phase input terminal.
32	FMEP	O	Feed motor amplifier (FM Amp) positive phase input terminal.
33	FAPO	O	Focus actuator drive amplifier (FAP Amp) output terminal. (Not used).
34	2VRO	I	2 V REF amplifier (2 V REF Amp) output terminal.
35	2VRP	I	2 V REF amplifier (2 V REF Amp) positive phase input terminal.
36	2VRN	I	2 V REF amplifier (2 V REF Amp) reversed phase input terminal.
37	TS2O	O	Tracking servo amplifier 2 (TS2 Amp) output terminal.
38	TS2N	I	Tracking servo amplifier 2 (TS2 Amp) reversed phase input terminal.
39	TS2P	I	Tracking servo amplifier 2 (TS2 Amp) positive phase input terminal.
40	TS1O	O	Tracking servo amplifier 1 (TS1 Amp) output terminal.

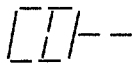
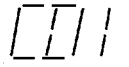
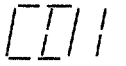
Pin No.	Pin Name	I/O	Description
41	TS1N	I	Tracking servo amplifier 1 (TS1 Amp) reversed phase input terminal.
42	TS1P	I	Tracking servo amplifier 1 (TS1 Amp) positive phase input terminal.
43	TSO	O	Tracking output amplifier (TS Amp) output terminal.
44	TSN	I	Tracking output amplifier (TS Amp) reversed phase input terminal.

TEST MODE

1. How to Activate CD Test Mode
   Insert the AC plug while pressing the function CD button.
   All FL display tubes will light up, and the test mode will be activated.

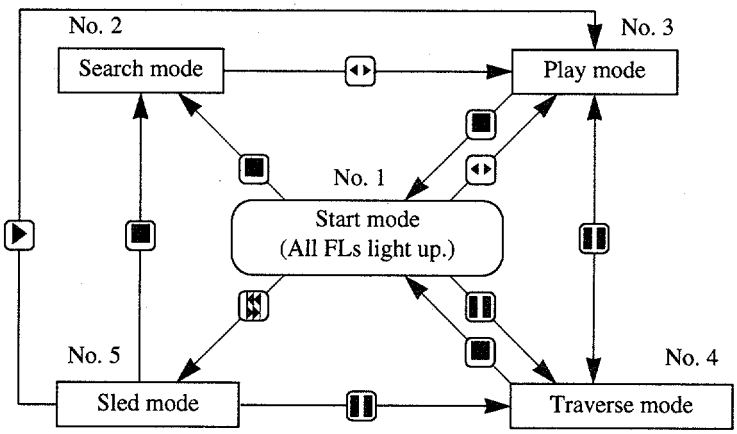
2. How to Cancel CD Test Mode
   Either one of the following operations will cancel the CD test mode.
   - Press the function button. (except CD function button)
   - Press the power switch button.
   - Disconnect the AC plug

3. CD Test Mode Functions
   When test mode is activated, the following mode functions from No.1 to No.5 can be used by pressing the operation keys.

Mode/No.	Operation	FL display	Operation	Contents
Start mode No.1	Activation	All lamps light	• Test mode is activated.	• FL display check (All displays light.)
Search mode No.2	■ key		• Laser diode turns always ON. (CD block power is ON.) • Continual focus search (The pickup lens repeats the full-swing up-down motion.) * Avoid continual searches that last for more than 10 minutes. * NOTE 1	• APC circuit check • Laser current measurement (Laser current control. Across a resistor connected between emitter and GND.) FOCUS SERVO • Check focus search waveform • Check focus error waveform (FOK/FZC are not monitored in the search mode)
Play mode No.3	◀▶ key		• Normal playback • Focus search is continued if TOC cannot be read. * NOTE 1	FOCUS SERVO/TRACKING SERVO CLV SERVO/SLED SERVO Check FOK/FZC
Traverse mode No.4	▮▮ key		• During normal disc playback Press once; tracking servo OFF Press twice; tracking servo ON * NOTE 2	TRACKING SERVO ON/OFF Tracking balance (traverse) adjustment
Sled mode No.5	⏮ key ⏭	All lamps light	• Pickup moves to the outermost track • Pickup moves to the innermost track * NOTE 3 (During playback, machine operates normally.)	SLED SERVO Check SLED mechanism operation

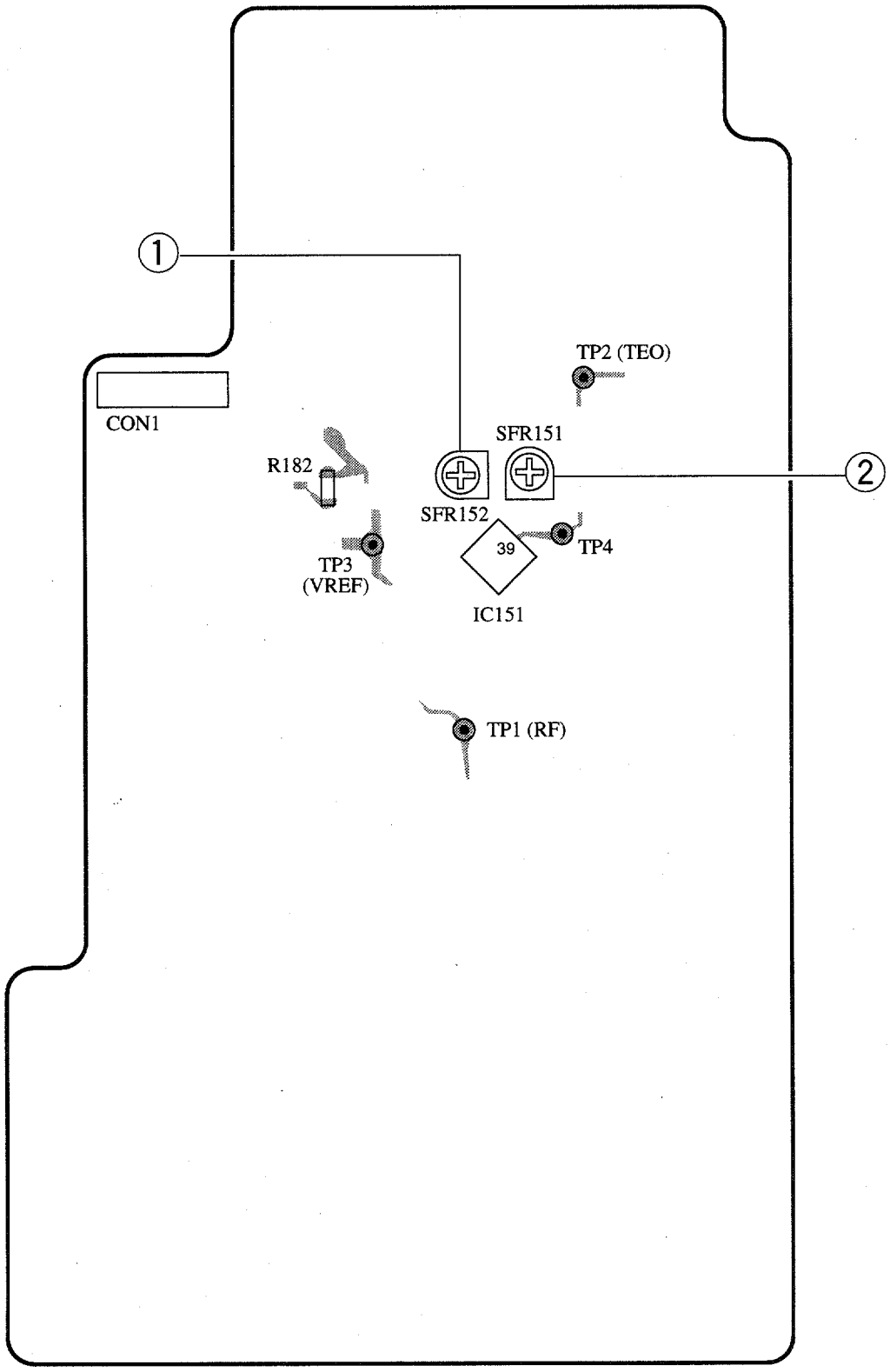
* NOTE 1: There are cases when the tracking servo cannot be locked owing to the protection circuit being operated when heat builds up in the driver IC if the focus search is operated continually for more than 10 minutes. In these cases the power supply should be switched off for 10 minutes until heat has been reduced and then re-started.
* NOTE 2: Do not press the ⏮ or ⏭ keys when the machine is in the ▮▮ status is active. If they are pressed, playback will not be possible after the ▮▮ status has been canceled. If the ⏮ or ⏭ keys are pressed in the ▮▮ status, press the ■ key and return to the start mode (No.1).
* NOTE 3: When pressing the ⏮ or ⏭ keys, take care to avoid damage to the gears. Because the sled motor is activated when the ⏮ or ⏭ keys are pressed, even when the pick-up is at the outermost or innermost track.

4. Operation Outline
   The operation of each mode is carried out in the direction of the arrows from the start mode as indicated in the following illustration.



If the DISC DIRECT PLAY button is pressed, the machine performs the same operation as the PLAY button is pressed as shown. If the tray is opened by pressing OPEN/CLOSE button during Play mode or Traverse mode, the machine returns to the Start mode.

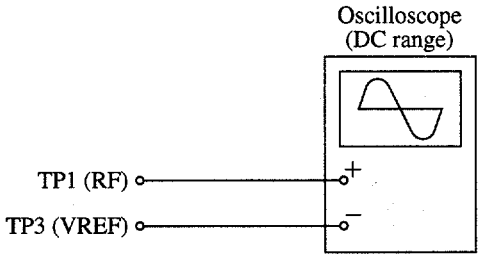
A 3CD C.B (PATTERN SIDE)



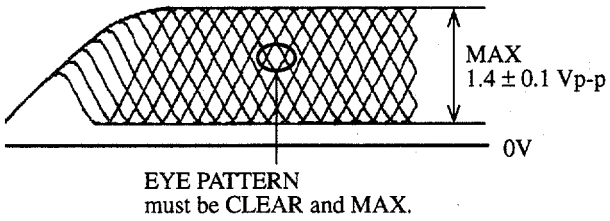
Note: • Connect a probe (10: 1) of the oscilloscope or the frequency counter to a test point.
• During adjustment, connect (⊖) pin of an oscilloscope to TP3 (VREF).

1. Focus Bias Adjustment

Make the focus bias adjustment when replacing and repairing the optical block.

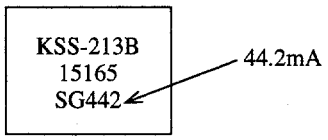


1) Connect an oscilloscope to test points TP1 (RF) and TP3 (VREF).
2) Turn on the power switch.
3) Insert test disc TCD-782 (YEDS-18) and play back the second program.
4) Adjust SFR152 so that RF signal of the test point TP2 (RF) is MAX and CLEARREST.



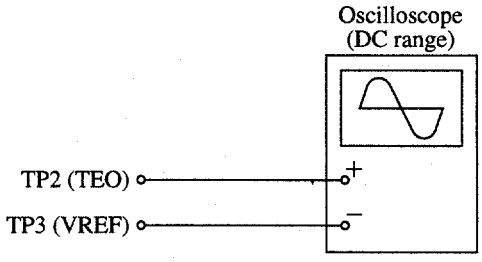
VOLT/DIV: 0.5V
TIME/DIV: 0.5μS

Note : The current of the laser signal can be checked with the voltages on both sides of R182 (voltage across 10Ω). The difference for the specified value shown on the label must be within ± 6.0mA.

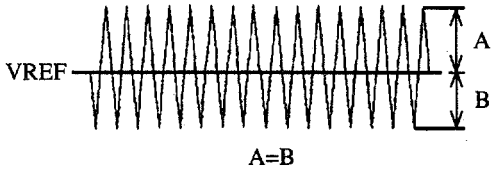


$$\text{Laser current Iop} = \frac{\text{Voltage across R182}}{10\Omega}$$

2. Tracking Balance Adjustment



1) Short circuit between TP3 (VREF) and TP4.
2) Connect an oscilloscope to test points TP2 (TEO) and TP3 (VREF).
3) Turn on the power switch.
4) Insert test disc TCD-782 (YEDS-18) and press the PLAY (▶) button.
5) Adjust SFR151 so that the waveform on the oscilloscope is vertically symmetrical as shown in the figure below.
6) After the adjustment is completed, remove the connected lead wires from the test point TP3 (VREF) and TP4.



VOLT/DIV: 20mV
TIME/DIV: 2mS

4ZG-1Z

ELECTRICAL MAIN PARTS LIST

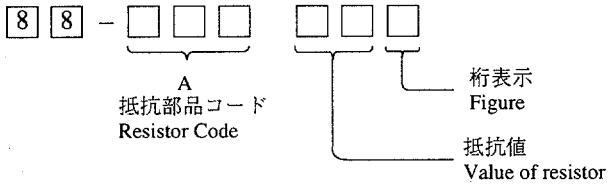
DESCRIPTION で判断できない物は “REFERENCE NAME LIST” を参照してください。
If can't understand for Description please kindly refer to “REFERENCE NAME LIST”.

REF. NO.	PART NO.	カンリ NO.	DESCRIPTION
IC			
	87-A20-165-010		C-IC,LA9230M
	87-A20-164-010		C-IC,LC78630E-T
	87-017-888-089		IC,NJM4558MD
	87-070-305-019		IC,BA6897S
	87-001-982-019		IC,TA7291S
TRANSISTOR			
	87-026-463-089		TR, 2SA933S (RS)
	89-406-555-089		TR,2SD655E
	89-320-011-089		TR,2SC2001K
	87-026-223-089		C-TR,DTC143TK
	89-113-187-089		TR,2SA1318TU
	87-026-470-089		TR,HN1C03 F B
	87-026-608-089		C-TR,DTC 123 JK
	89-327-125-089		C-TR,2SC2712GR<D>
DIODE			
	87-020-465-089		DIODE,1SS133
3CD C.B			
C11	87-016-081-089		C-CAP,S 0.1-16 RK
C12	87-012-157-089		C-CAP,S 330P-50 CH
C13	87-016-369-089		C-CAP,S 0.033-25 B K
C14	87-016-081-089		C-CAP,S 0.1-16 RK
C15	87-010-596-089		C-CAP,S 0.047-16 RK
C16	87-010-956-089		C-CAP,S 0.068-25 B
C17	87-010-182-089		C-CAP,S 2200P-50 B
C18	87-016-369-089		C-CAP,S 0.033-25 B K
C19	87-010-213-089		C-CAP,S 0.015-25 B
C20	87-010-178-089		C-CAP,S 1000P-50 B
C21	87-012-393-089		C-CAP,S 0.22-16,R,K
C22	87-016-083-089		C-CAP,S 0.15-16 RK
C23	87-010-197-089		C-CAP,S 0.01-25 B
C24	87-010-186-089		C-CAP,S 4700P-50 B
C25	87-015-694-089		CAP E 0.47-50-7L
C26	87-010-322-089		C-CAP,S 100P-50 CH
C27	87-015-686-089		CAP,E 22-25 7L
C28	87-015-697-089		CAP,E 3.3-50 7L
C29	87-010-184-089		C-CAP,S 3300P-50 B
C30	87-010-146-089		C-CAP,S 2P-50 CH
C31	87-010-186-089		C-CAP,S 4700P-50 B
C32	87-010-148-089		C-CAP,S 4P-50 CH
C33	87-016-081-089		C-CAP,S 0.1-16 RK
C35	87-010-196-089		C-CAP,S 0.1-25 F
C37	87-010-405-089		CAP,E 10-50 SME
C38	87-010-263-089		CAP,E 100-10 SME
C39	87-010-197-089		C-CAP,S 0.01-25 B
C40	87-010-401-089		CAP,E 1-50 SME
C41	87-016-463-089		C-CAP,S 0.33-16 B
C42	87-010-263-089		CAP,E 100-10 SME
C43	87-018-134-089		CAP,TC-U 0.01-16 Y
C44	87-010-263-089		CAP,E 100-10 SME
C46	87-010-196-089		C-CAP,S 0.1-25 F
C47	87-015-684-010		CAP,E 47-16 7L
C48	87-010-196-089		C-CAP,S 0.1-25 F
C50	87-010-197-089		C-CAP,S 0.01-25 B
C51	87-010-263-089		CAP,E 100-10 SME
C101	87-016-081-089		C-CAP,S 0.1-16 RK
C102	87-016-081-089		C-CAP,S 0.1-16 RK
C103	87-012-149-089		C-CAP, S 30P-50 CH
C105	87-010-196-089		C-CAP,S 0.1-25 F
C106	87-010-196-089		C-CAP,S 0.1-25 F
C108	87-010-154-089		C-CAP,S 10P-50 CH
C109	87-010-154-089		C-CAP,S 10P-50 CH
C111	87-010-196-089		C-CAP,S 0.1-25 F
C112	87-010-404-089		CAP,E 4.7-50 SME
C113	87-010-196-089		C-CAP,S 0.1-25 F
C114	87-010-263-089		CAP,E 100-10 SME
C201	87-010-318-089		C-CAP,S 47P-50 CH
C202	87-010-318-089		C-CAP,S 47P-50 CH
C203	87-010-321-089		C-CAP,S 82P-50 CH
C204	87-010-321-089		C-CAP,S 82P-50 CH
C205	87-010-321-089		C-CAP,S 82P-50 CH
C206	87-010-321-089		C-CAP,S 82P-50 CH
C207	87-010-318-089		C-CAP,S 47P-50 CH
C208	87-010-318-089		C-CAP,S 47P-50 CH
C209	87-010-318-089		C-CAP,S 47P-50 CH
C210	87-010-318-089		C-CAP,S 47P-50 CH
C211	87-010-403-089		CAP,E 3.3-50 SME
C212	87-010-403-089		CAP,E 3.3-50 SME
C213	87-010-186-089		C-CAP,S 4700P-50 B
C214	87-010-186-089		C-CAP,S 4700P-50 B
C215	87-010-555-049		CAP,E 100-10 GAS
C216	87-010-384-089		CAP,E 100-25 SME
C301	87-010-196-089		C-CAP,S 0.1-25 F
C302	87-010-260-089		CAP,E 47-25 SME
C501	87-010-221-089		CAP,E 470-10 11L
C502	87-010-197-089		C-CAP,S 0.01-25 B
C504	87-010-196-089		C-CAP,S 0.1-25 F
C505	87-010-196-089		C-CAP,S 0.1-25 F
C506	87-010-196-089		C-CAP,S 0.1-25 F
C507	87-010-196-089		C-CAP,S 0.1-25 F
C509	87-010-196-089		C-CAP,S 0.1-25 F
C510	87-010-196-089		C-CAP,S 0.1-25 F
C601	87-010-197-089		C-CAP,S 0.01-25 B
C602	87-010-381-089		CAP,E 330-16 SME
C603	87-010-196-089		C-CAP,S 0.1-25 F
C701	87-010-322-089		C-CAP,S 100P-50 CH
C702	87-010-322-089		C-CAP,S 100P-50 CH
C703	87-010-322-089		C-CAP,S 100P-50 CH
C704	87-010-322-089		C-CAP,S 100P-50 CH
C705	87-018-131-089		CAP,TC-U 1000P-50 B
C901	87-010-260-089		CAP,E 47-25 SME<D>
C902	87-010-196-089		C-CAP,S 0.1-25 F<D>
FC1	85-NFT-611-119		FP-CABLE,16P-1.0
FC4	84-ZG1-614-219		CABLE,FFC 5P-1.25
FC5	84-ZG1-630-019		CABLE FFC 6P-1.25
L11	87-003-102-089		COIL,10UH
LED901	87-A40-123-019		LED,SLZ-8128A-01-B<D>
M601	87-045-383-019		MOT,M9I T2
R102	87-022-345-089		C-RES,S 1.2K-1/10W F
SW701	87-036-109-019		SW,PUSH SPPB 61
SW702	87-036-109-019		SW,PUSH SPPB 61
X101	87-030-402-089		VIB,XTAL 16.9344 MHZ
LED C.B			
LED701	87-070-200-089		LED,SLP636C-81-S-T1
LED702	87-017-350-080		LED,SEL1550CM
LED703	87-017-350-080		LED,SEL1550CM
LED704	87-070-200-089		LED,SLP636C-81-S-T1

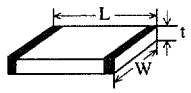
REF. NO.	PART NO.	カンリ NO.	DESCRIPTION
T-T C.B			
C401	87-018-214-089		CAP TC U 0.1-50 F
M401	87-045-364-019		MOTOR,(BCH3B14)
PS401	87-026-573-019		P-SNSR,GP1S53V
DRIVE C.B			
M1	87-045-358-019		MOT,RF-310TA 43
M2	87-045-356-019		MOT,RF-310TA 30
SW1	87-A90-042-019		SW,LEAF MSW 17310 MVPO

○ チップ抵抗部品コード／CHIP RESISTOR PART CODE

チップ抵抗部品コードの成り立ち
Chip Resistor Part Coding



チップ抵抗
Chip resistor

容量 Wattage	種類 Type	許容誤差 Tolerance	記号 Symbol	寸法／Dimensions (mm) 外形／Form	L	W	t	抵抗コード ：A Resistor Code: A
1／16W	1608	±5%	CJ		1.6	0.8	0.45	108
1／10W	2125	±5%	CJ		2	1.25	0.45	118
1／8W	3216	±5%	CJ		3.2	1.6	0.55	128

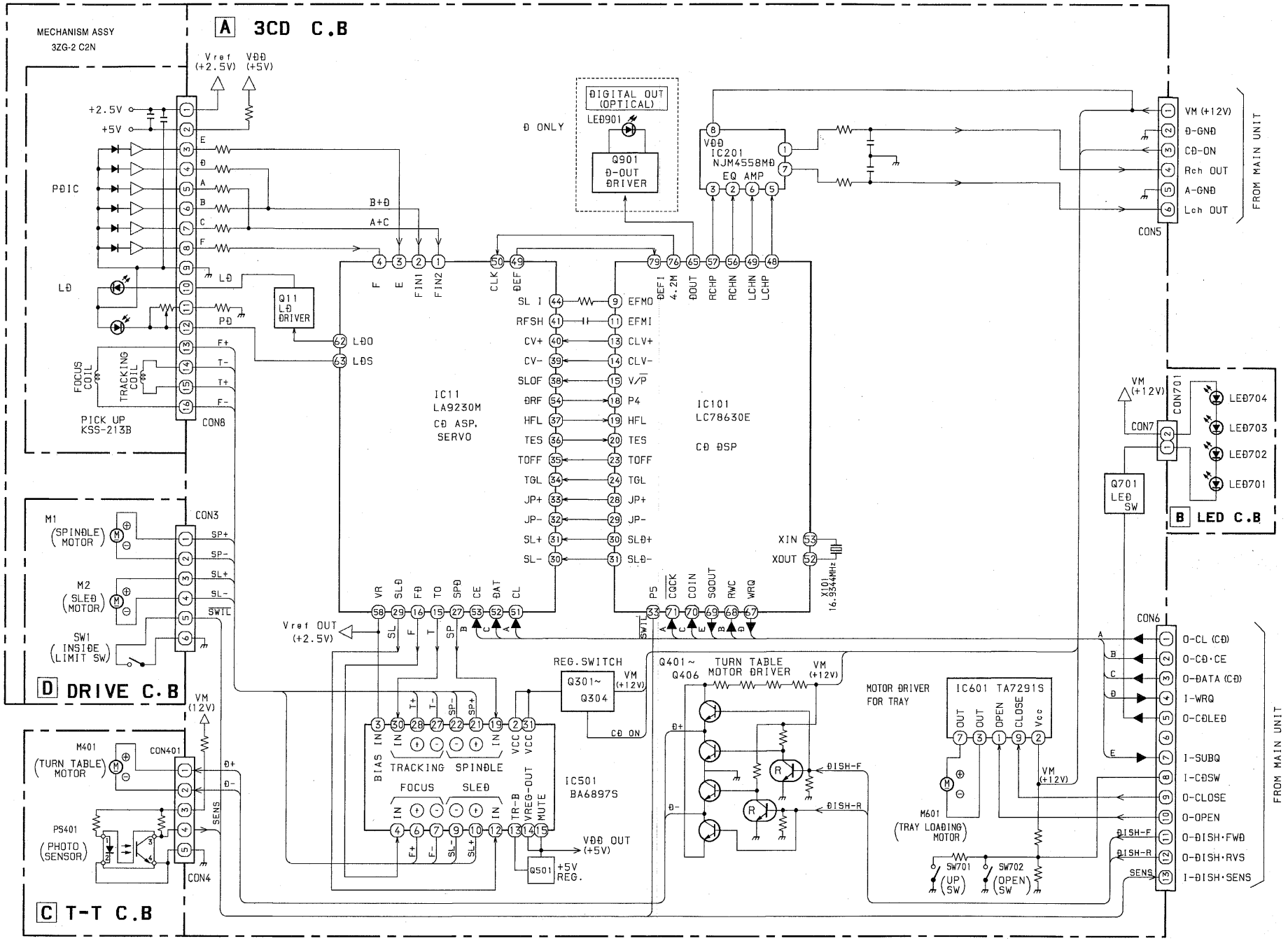
Refer to the following pages for the 4ZG-1 and the common sections.

■ MECHANICAL EXPLODED VIEW 1 ／ 1

See page 95

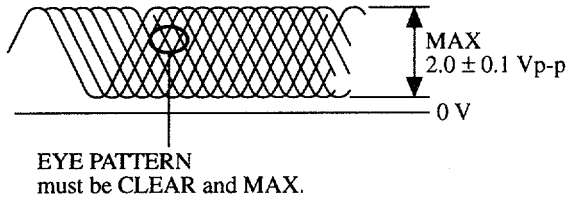
■ MECHANICAL PARTS LIST 1 ／ 1

See page 96


MECHANISM ASSY
3ZG-2 C2N
A 3CD C.B
Vref (+2.5V)
VDD (+5V)
+2.5V
+5V
PDIC
LD
FOCUS COIL
TRACKING COIL
PICK UP KSS-213B
CON8
Q11 LD DRIVER
B+D
A+C
LDO
LDS
IC11 LA9230M CD ASP. SERVO
IC101 LC78630E CD DSP
DIGITAL OUT (OPTICAL)
LED901
D ONLY
Q901 D-OUT DRIVER
VDD
IC201 NJM4558MD
EQ AMP
CON5
FROM MAIN UNIT
VM (+12V)
D-GND
CD-ON
Rch OUT
A-GND
Lch OUT
CON701
CON7
LED704
LED703
LED702
LED701
Q701 LED SW
B LED C.B
M1 (SPINDLE MOTOR)
M2 (SLED MOTOR)
SW1 (INSIDE LIMIT SW)
CON3
D DRIVE C.B
Vref OUT (+2.5V)
REG.SWITCH
Q301~ Q304
CD ON
Q401~ Q406
TURN TABLE MOTOR DRIVER
MOTOR DRIVER FOR TRAY
IC601 TA7291S
M401 (TURN TABLE MOTOR)
CON401
PS401 (PHOTO SENSOR)
CON4
BIAS IN
TRACKING
SPINDLE
FOCUS
SLED
IC501 BA6897S
VREG-OUT
MUTE
Q501 +5V REG.
VDD OUT (+5V)
DISH-F
DISH-R
M601 (TRAY LOADING MOTOR)
SW701 (UP SW)
SW702 (OPEN SW)
CON6
O-CL (CD)
O-CD·CE
O-DATA (CD)
I-WRQ
O-CDLED
I-SUBQ
I-CDSW
O-CLOSE
O-OPEN
O-DISH·FWD
O-DISH·RVS
I-DISH·SENS
C T-T C.B

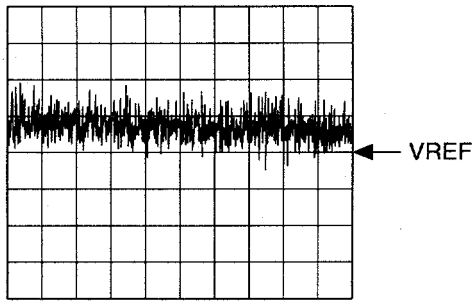
WAVE FORM

① IC11 Pin ㊶ (RFSM) VOLT/DIV: 0.5V TIME/DIV: 1μS

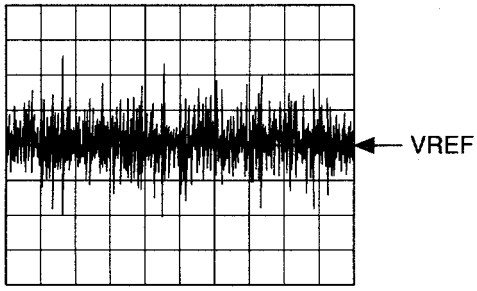


EYE PATTERN
must be CLEAR and MAX.

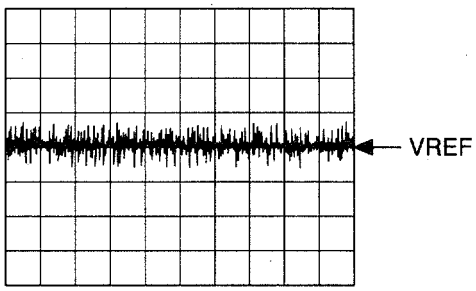
② IC11 Pin ⑯ (FD) VOLT/DIV: 100mV TIME/DIV: 1mS



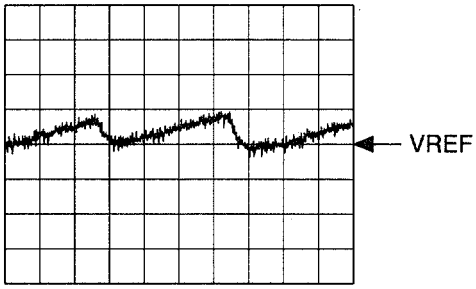
③ IC11 Pin ⑮ (TO) VOLT/DIV: 100mV TIME/DIV: 1mS



④ IC11 Pin ㉗ (SPD) VOLT/DIV: 100mV TIME/DIV: 1mS

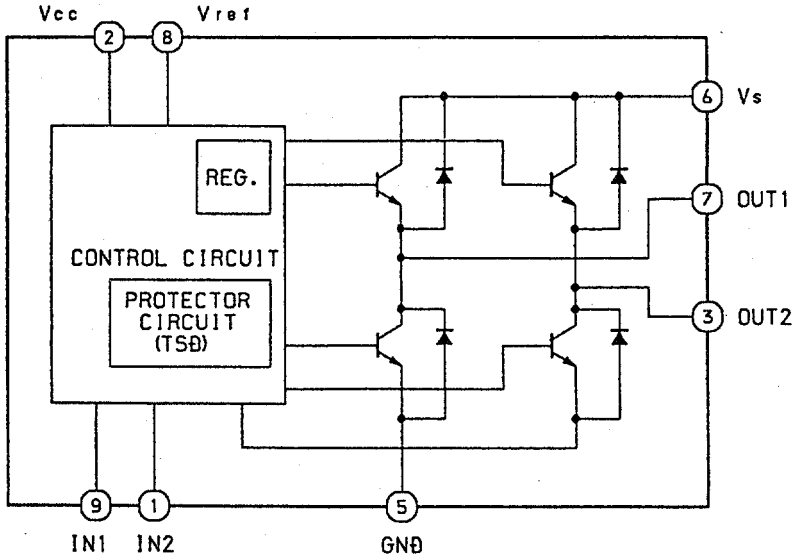


⑤ IC11 Pin ㉙ (SLD) VOLT/DIV: 200mV TIME/DIV: 2S



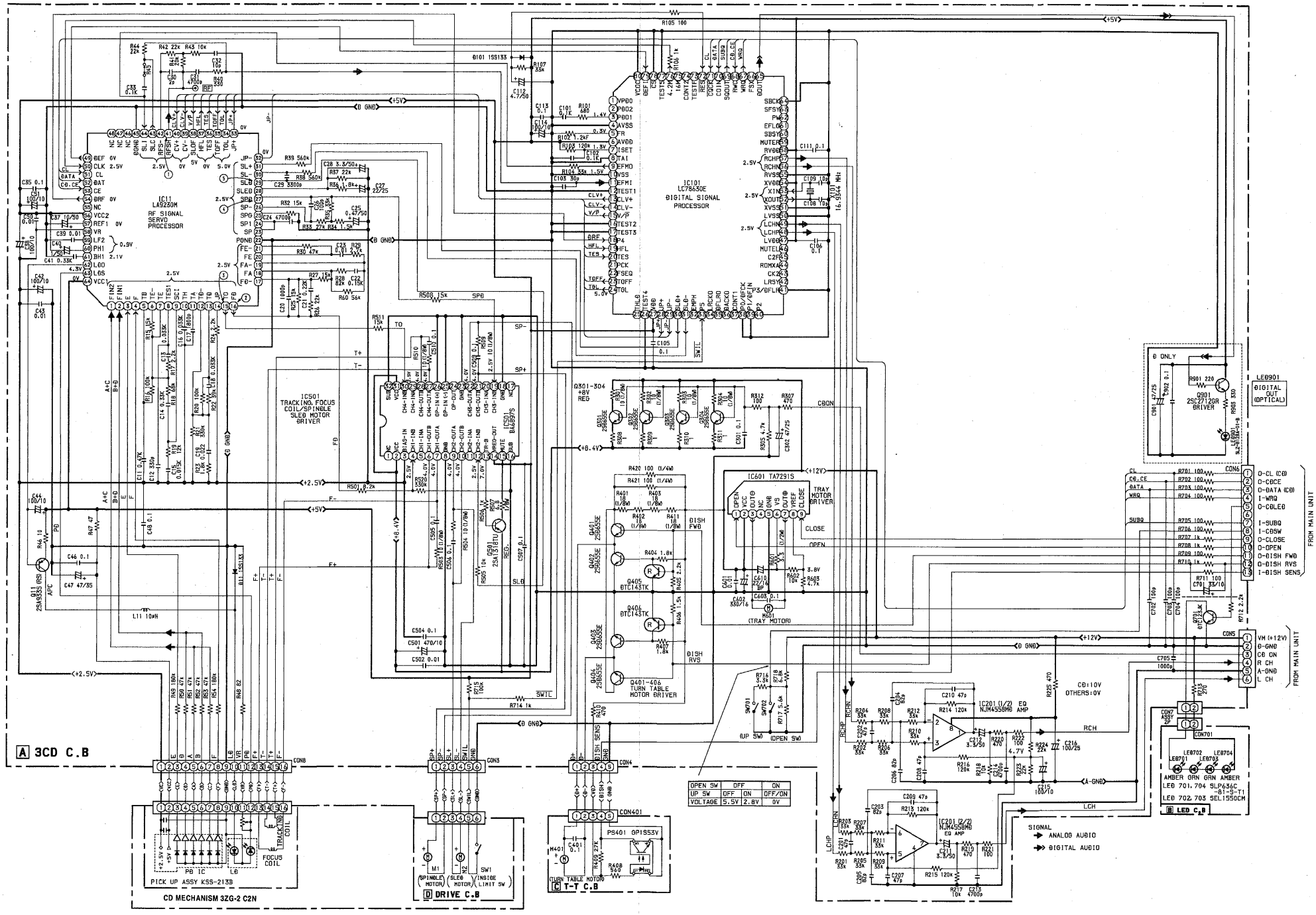
IC BLOCK DIAGRAM

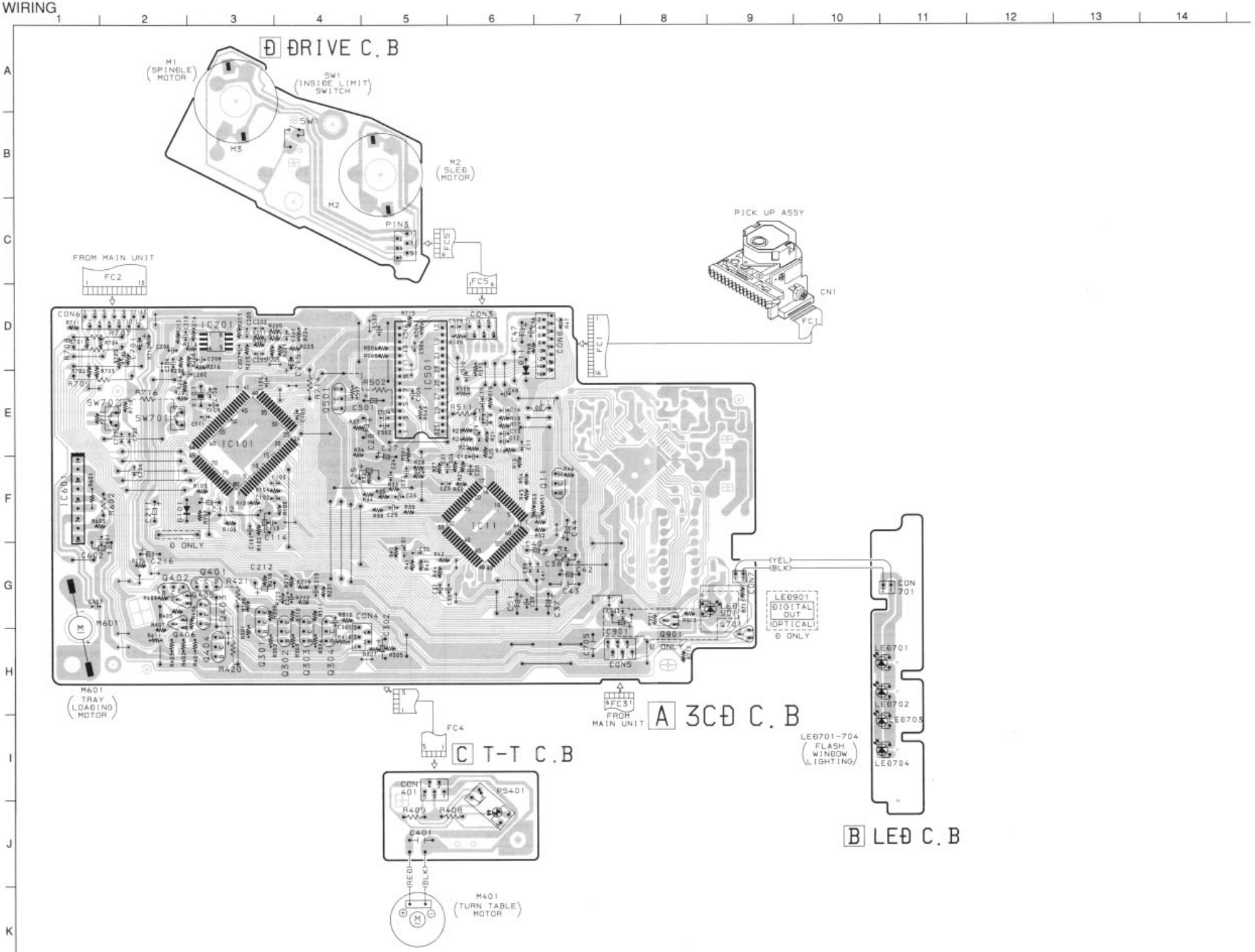
IC, TA7291



INPUT		OUTPUT		MODE
IN1	IN2	OUT1	OUT2	
0	0	∞	∞	STOP
1	0	H	L	CW
0	1	L	H	CCW
1	1	L	L	BRAKE

∞ : HI IMPEDANCE
NOTE : INPUT "H" ACTIVE


A 3CD C.B
IC11 LA9280M RF SIGNAL SERVO PROCESSOR
IC101 LC78630E DIGITAL SIGNAL PROCESSOR
IC501 TRACKING, FOCUS COIL/SPINDLE SLED MOTOR DRIVER
IC601 TA7291S TRAY MOTOR DRIVER
IC201 (1/2) EQ NJM4558MB EQ AMP
IC201 (2/2) NJM4558MB EQ AMP
Q301-304 +8V REG
Q401-406 TURN TABLE MOTOR DRIVER
Q901 2SC2712GR DRIVER
PICK UP ASSY KSS-213B
CD MECHANISM 3ZG-2 C2N
B LED C.B
C T-T C.B
D DRIVE C.B
FROM MAIN UNIT
SIGNAL
ANALOG AUDIO
DIGITAL AUDIO
OPEN SW
UP SW
VOLTAGE
5.5V
2.8V
0V
OFF/ON


Đ ĐRIVE C.B
M1 (SPINĐLE MOTOR)
SW1 (INSIĐE LIMIT SWITCH)
SW1
M3
M2 (SLEĐ MOTOR)
M2
PIN3
FC5
FC5
FROM MAIN UNIT
FC2
PICK UP ASSY
CN1
FC1
FC1
IC201
IC101
IC11
IC601
SW702
SW701
Đ ONLY
M601
M601 (TRAY LOADING MOTOR)
FC4
C T-T C.B
CON 401
PS401
R409
R408
C401
(RED)
(BLK)
M401 (TURN TABLE MOTOR)
FC3
FROM MAIN UNIT
A 3CĐ C.B
(YEL)
(BLK)
CON7
LEĐ901 DIGITAL OUT (OPTICAL)
Đ ONLY
CON 701
LEĐ701
LEĐ702
LEĐ703
LEĐ704
LEĐ701-704 (FLASH WINĐOW LIGHTING)
B LEĐ C.B

IC DESCRIPTION

IC, LC78630E

Pin No.	Pin Name	I/O	Description
1	VPDO	O	Vari-pitch PLL charge pump output pin. This pin must be open when not used.
2	PDO2	O	Bit clock playback PLL charge pump output pin during 2 times and 4 times speed. This pin must be open when not used.
3	PDO1	O	Bit clock playback PLL charge pump output pin during normal speed.
4	AVSS	—	Analog system GND. Normally 0V.
5	FR	I	An external resistor to set built-in VCO frequency range is connected to this pin.
6	AVDD	—	Analog system GND.
7	ISET	I	An external resistor set PD01 and PD02 output current is connected to this pin.
8	TAI	I	Test input pin with built-in pull-down resistor.
9	EFMO	O	EFM signal output pin.
10	VSS	—	Digital system GND. Normally 0V.
11	EFMI	I	EFM signal input pin.
12	TEST1	I	Test input pin with built-in pull-down resistor.
13	CLV+	O	Spindle servo control output pin. Acceleration when CLV+ is "H".
14	CLV-	O	Deceleration when CLV- is "H".
15	V/$\overline{P}$	O	Rough servo/phase control automatic selection monitoring output pin. Rough servo at "H". Phase control mode at "L".
16, 17	TEST2, TEST3	I	Test input pin with built-in pull-down resistor.
18	P4	I/O	Input/output port.
19	HFL	I	Tracking detection signal input pin. Schmitt input.
20	TES	I	Tracking error signal input pin. Schmitt input.
21	PCK	O	EFM data playback bit clock monitoring pin. 4.3218 MHz when phase is locked during normal speed playback.
22	FSEQ	O	Sync signal detection output pin. When the sync signal detected from the EFM signal agrees with the internally generated sync signal, "H" output.
23	TOFF	O	Tracking OFF output pin.
24	TGL	O	Tracking gain selector output pin. Gain is increased at "L".
25	THLD	O	Tracking hold output pin.
26	TEST4	I	Test input pin with built-in pull-down resistor.
27	VDD	—	Digital system GND.
28, 29	JP+, JP-	O	Tracking jump output pin. JP+ "H" occurs at acceleration during jump toward outside or decelerator toward inside. JP- "H" occurs at acceleration during jump toward inside or deceleration toward outside.
30, 31	SLD+, SLD-	O	Sled output pin. Four different level can be set using commands.
32	EMPH	O	Emphasis monitoring output. "H" indicates that emphasis disc is being played back.
33	P5	I/O	Input/output.
34	LRCKO	O	Digital filter output. LR clock output pin.
35	DFLRO	O	Digital filter output. LR data output pin. DF is turned OFF with the DFOFF command.
36	DACKO	O	Digital filter output. Bit clock output pin.
37	CONT1	O	Output port.

Pin No.	Pin Name	I/O	Description
38	P0/DFCK	I/O	Input/output port. The DF bit clock input pin during the anti-shock mode.
39	P1/DFIN	I/O	Input/output port. The DF data input pin during the anti-shock mode.
40	P2	I/O	Input/output port. Deemphasis filter ON/OFF selection input pin during the anti-shock mode. Deemphasis filter ON at "H".
41	P3/DFLR	I/O	Input/output port. The DF LR clock input pin during the anti-shock mode.
42	LRSY	O	For ROMXA • LR clock output pin.
43	CK2	O	For ROMXA • Bit clock output pin. Polarity inversion by the CK2CON command.
44	ROMXA	O	For ROMXA • Interpolation data output pin. The un-interpolated data is output with the ROMXA command.
45	C2F	O	For ROMXA • C2 flat output pin.
46	MUTEL	O	For 1-bit DAC • L-channel mute output pin.
47	LVDD	—	For 1-bit DAC • L-channel power supply.
48	LCHP	O	For 1-bit DAC • L-channel P output pin.
49	LCHN	O	For 1-bit DAC • L-channel N output pin.
50	LVSS	—	For 1-bit DAC • L-channel GND. Normally 0 V.
51	XVSS	—	Crystal oscillator GND. Normally 0 V.
52	XOUT	O	An external 16.9344 MHz crystal oscillator is connected to this pin.
53	XIN	I	33.8688 MHz crystal oscillator is connected during 4 time speed playback.
54	XVDD	—	Crystal oscillator GND.
55	RVSS	—	For 1-bit DAC • R-channel GND. Normally 0 V.
56	RCHN	O	For 1-bit DAC • R-channel N output pin.
57	RCHP	O	For 1-bit DAC • R-channel P output pin.
58	RVDD	—	For 1-bit DAC • R-channel power supply.
59	MUTER	O	For 1-bit DAC • R-channel mute output pin.
60	SBSY	O	Subcode block sync signal output pin.
61	EFLG	O	C1 and C2 error correction monitoring pin.
62	PW	O	ubcode P, Q, R, S, T, U, V and W output pin.
63	SFSY	O	Subcode frame sync signal output pin. The level falls down when the subcode is in standby.
64	SBCK	I	Subcode read clock input pin. Schmitt input. This pin must be connected GND when not used.
65	DOUT	O	Digital output pin.
66	FSX	O	7.35 kHz sync signal divided from the crystal oscillator is output to this pin.
67	WRQ	O	Subcode Q output standby output pin.
68	RWC	I	Read/write control input pin.
69	SQOUT	O	Subcode Q output pin.
70	COIN	I	Microprocessor command input pin.
71	$\overline{\text{CQCK}}$	I	Command input read clock or subcode read clock input from SQOUT. Schmitt input.
72	$\overline{\text{RES}}$	I	Chip reset input pin. This pin goes to "L" once when the main power is turned on.
73	TESTF	O	Test output pin.
74	CONT2	O	Output port.

Pin No.	Pin Name	I/O	Description
75	16M	O	16.9344 MHz crystal output pin. 33.8688 MHz is output during 4 times speed playback.
76	4.2M	O	4.2336 MHz output pin.
77	TEST5	I	Test input pin with built-in pull-down resistor.
78	$\overline{CS}$	I	Chip select input pin with built-in pull-down resistor.
79	DEFI	I	Defect detection signal input pin. This pin must be connected GND when not used.
80	VCOC	I	Vari-pitch VCO control input pin. This pin must be connected GND when not used.

IC, LA9230M

Pin No.	Pin Name	I/O	Description
1	FIN2	I	Photo diode of pickup is connected to this pin. This signal is added to the FIN1 pin signal to produce the RF signal and subtracted to produce the FE signal.
2	FIN1	I	Photo diode of pickup is connected to this pin.
3	E	I	Photo diode of pickup is connected to this pin. This signal is subtracted from the F pin signal to produce the FE signal.
4	F	I	Photo diode of pickup is connected to this pin.
5	TB	I	DC component of the TE signal is input to this pin.
6	TE-	I	The TE signal gain adjustment resistor is connected between this pin and the TE pin.
7	TE	O	The TE signal output pin.
8	TESI	I	TES (Track Error Sense) comparator input pin. The TE signal is input after passing through band-pass filter.
9	SCI	I	Shock sense input signal is connected to this pin.
10	TH	I	Tracking gain time constant setting pin.
11	TA	O	TA amplifier output pin.
12	TD-	I	An external tracking phase compensation constant is connected between the TD and VR pins.
13	TD	I	An external tracking phase compensation setting pin.
14	JP	I	Tracking jump signal (kick pulse) amplitude setting pin.
15	TO	O	Tracking control signal output pin.
16	FD	O	Focusing control signal output pin.
17	FD-	I	A focusing phase compensation constant is connected between the FD and FA pins.
18	FA	I	A focusing phase compensation constant is connected between the FD- and FA- pins.
19	FA-	I	A focusing phase compensation constant is connected between the FA and FE pins.
20	FE	O	FE signal output pin.
21	FE-	I	An external FE signal gain setting resistor is connected between the TE and this pins.
22	AGND	—	Analog signal GND.
23	SP	O	Single-ended output of the CV+ and CV- pin input signal.
24	SPI	I	Spindle amplifier input.
25	SPG	I	An external spindle gain in 12 cm mode setting resistor is connected to this pin.
26	SP-	I	An external spindle phase compensation constant together with the SPD pin, is connected to this pin.
27	SPD	O	Spindle control signal output pin.
28	SLEQ	I	Sled phase compensation constant is connected to this pin.
29	SLD	O	Sled control signal output pin.
30, 31	SL-, SL+	I	Sled advance signal input pin from microprocessor.
32, 33	JP-, JP+	I	Tracking jump signal input pin from DSP.
34	TGL	I	Tracking gain control signal input pin from DSP. Gain low when TGL = "H".
35	TOFF	I	Tracking off control signal input pin from DSP. Tracking off when TGL = "H".
36	TES	O	The TES signal is output from this pin to DSP.
37	HFL	I	The (HIGH FREQUENCY LEVEL) is used to judge whether the main beam is positioned above the bits or mirror.

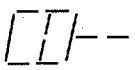
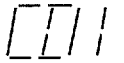
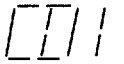
Pin No.	Pin Name	I/O	Description
38	SLOF	I	Sled servo off control input pin.
39, 40	CV-, CV+	I	CLV error signal input pin from DSP.
41	RFSM	O	RF output pin.
42	RFS-	I	RF gain setting and 3T compensation constant setting pin together with RFSM pin.
43	SLC	O	The (SLICE LEVEL CONTROL) is the signal which control the data slice level of the RF waveform with DSP. The (SLICE LEVEL CONTROL) is from this pin.
44	SLI	I	The input signal which controls the data slice level with DSP, is connected to this pin.
45	DGND	—	Digital system GND.
46	NC [FSC]	—	No connection. (Output pin for focus search smoothing capacity.)
47, 48	NC	—	No connection.
49	DEF	O	Disc defect detection output pin.
50	CLK	I	Reference clock input pin. The DSP 4.23 MHz is input to this pin.
51	CL	I	Microprocessor command clock input pin.
52	DAT	I	Microprocessor command data input pin.
53	CE	I	Microprocessor command chip enable input pin.
54	DRF	O	(DETECT RF) RF level detection output.
55	NC	—	No connection.
56	VCC2	—	Servo system and digital system Vcc pin.
57	REFI	I	A bypass capacitor for reference voltage is connected to this pin.
58	VR	O	Reference voltage output pin.
59	LF2	I	An external disc defect detection constant is connected to this pin.
60	PH1	I	An external RF signal peak holding capacitor is connected to this pin.
61	BH1	I	An external RF signal bottom holding capacitor is connected to this pin.
62	LDD	O	APC circuit output pin.
63	LDS	I	APC circuit input pin.
64	VCC1	—	RF system Vcc pin.

TEST MODE

1. How to Activate CD Test Mode
   Insert the AC plug while pressing the function CD button.
   All FL display tubes will light up, and the test mode will be activated.

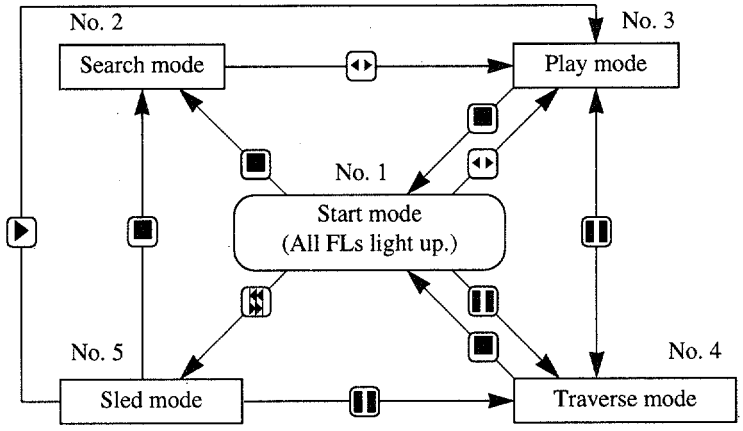
2. How to Cancel CD Test Mode
   Either one of the following operations will cancel the CD test mode.
   - Press the function button. (except CD function button)
   - Press the power switch button.
   - Disconnect the AC plug

3. CD Test Mode Functions
   When test mode is activated, the following mode functions from No.1 to No.5 can be used by pressing the operation keys.

Mode/No.	Operation	FL display	Operation	Contents
Start mode No.1	Activation	All lamps light	• Test mode is activated. • CD block power is ON.	• FL display check (All displays light.)
Search mode No.2	■ key		• Laser diode turns always ON. • Continual focus search (The pickup lens repeats the full-swing up-down motion.) * Avoid continual searches that last for more than 10 minutes. * NOTE 1	• APC circuit check • Laser current measurement (Laser current control. Across a resistor connected between emitter and GND.) FOCUS SERVO • Check focus search waveform • Check focus error waveform (FOK/FZC are not monitored in the search mode)
Play mode No.3	◀▶ key		• Normal playback • Focus search is continued if TOC cannot be read. * NOTE 1	FOCUS SERVO/TRACKING SERVO CLV SERVO/SLED SERVO Check DRF
Traverse mode No.4	▮▮ key		• During normal disc playback Press once; tracking servo OFF Press twice; tracking servo ON * NOTE 2	TRACKING SERVO ON/OFF Tracking balance (traverse) check
Sled mode No.5	⏮ key ⏭	All lamps light	• Pickup moves to the outermost track • Pickup moves to the innermost track * NOTE 3 (During playback, machine operates normally.)	SLED SERVO Check SLED mechanism operation

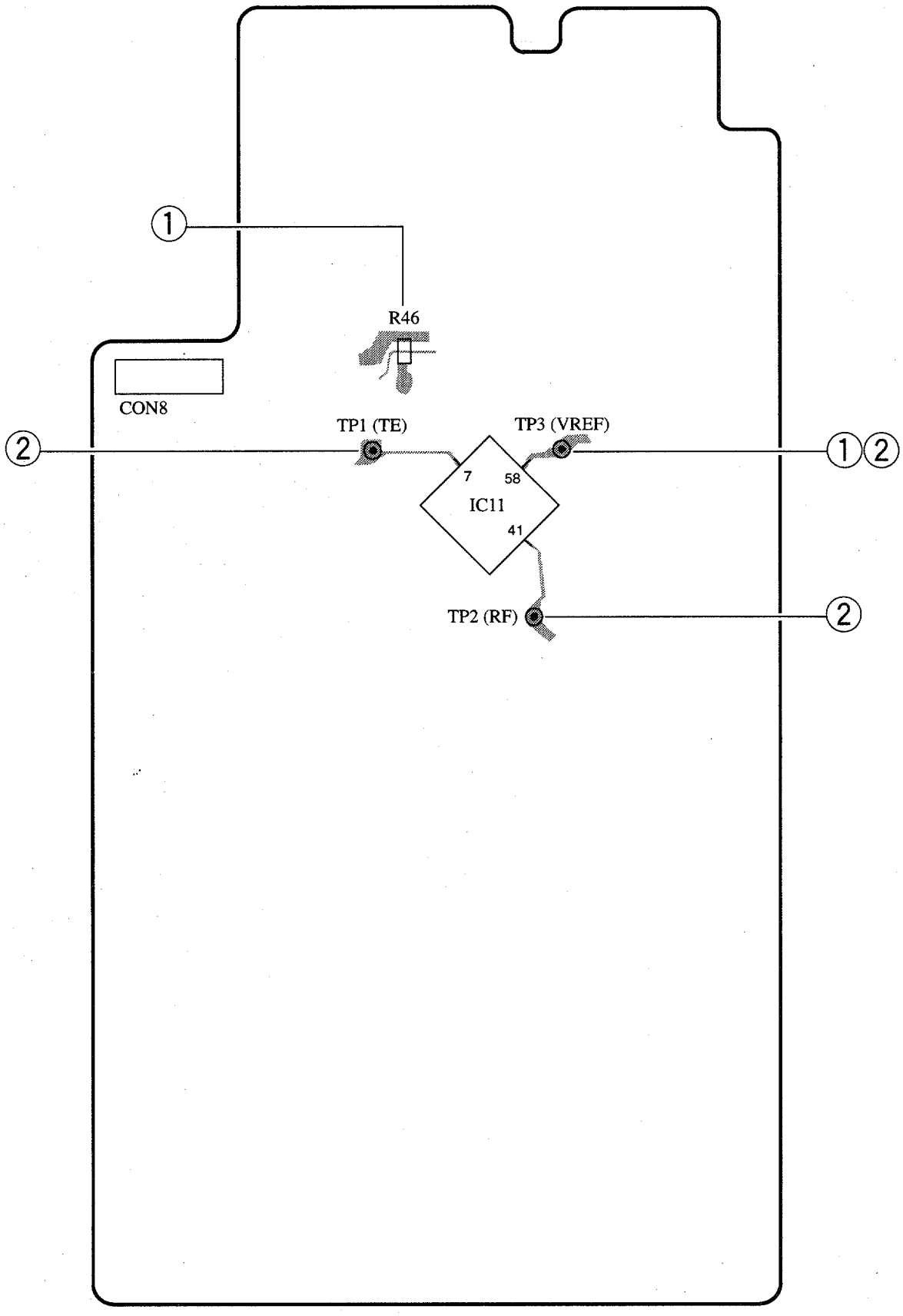
* NOTE 1: There are cases when the tracking servo cannot be locked owing to the protection circuit being operated when heat builds up in the driver IC if the focus search is operated continually for more than 10 minutes. In these cases the power supply should be switched off for 10 minutes until heat has been reduced and then re-started.
* NOTE 2: Do not press the ⏮ or ⏭ keys when the machine is in the ▮▮ status is active. If they are pressed, playback will not be possible after the ▮▮ status has been canceled. If the ⏮ or ⏭ keys are pressed in the ▮▮ status, press the ■ key and return to the start mode (No.1).
* NOTE 3: When pressing the ⏮ or ⏭ keys, take care to avoid damage to the gears. Because the sled motor is activated when the ⏮ or ⏭ keys are pressed, even when the pick-up is at the outermost or innermost track.

4. Operation Outline
   The operation of each mode is carried out in the direction of the arrows from the start mode as indicated in the following illustration.



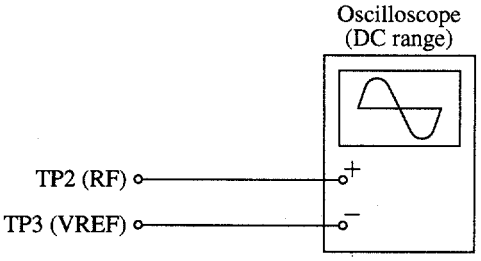
If the DISC DIRECT PLAY button is pressed, the machine performs the same operation as the PLAY button is pressed as shown. If the tray is opened by pressing OPEN/CLOSE button during Play mode or Traverse mode, the machine returns to the Start mode.

A 3CD C.B (PATTERN SIDE)

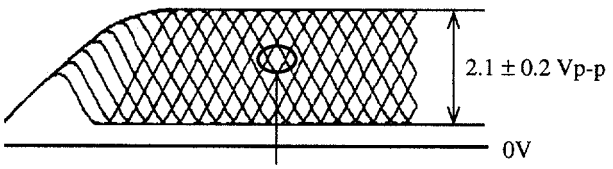


Note:
- Connect a probe (10: 1) of the oscilloscope or the frequency counter to a test point.
- During adjustment, connect (⊖) pin of an oscilloscope to TP3 (VREF).

1. RF waveform Check



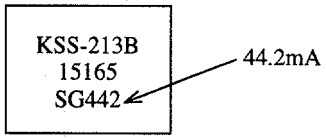
1) Connect an oscilloscope to test points TP2 (RF) and TP3 (VREF).
2) Turn on the power switch.
3) Insert test disc TCD-782 (YEDS-18) and play back the second program.
4) Confirm that the waveform at oscilloscope has amplitude of 2.1 Vp-p, and clear wedge area in its center.



EYE PATTERN
must be CLEAR and MAX.

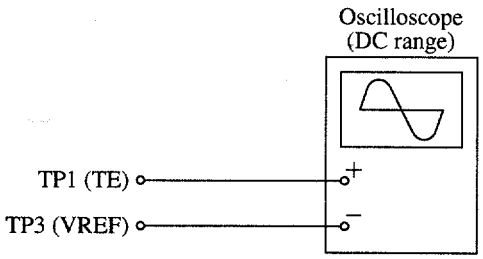
VOLT/DIV: 50mV
TIME/DIV: 0.5μS

Note: The current of the laser signal can be checked with the voltages on both sides of R46 (voltage across 10Ω). The difference for the specified value shown on the label must be within ± 6.0mA.

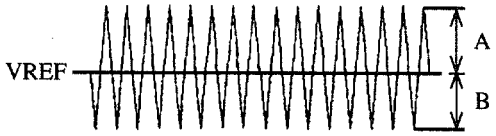


$$\text{Laser current Iop} = \frac{\text{Voltage across R46}}{10\Omega}$$

2. Tracking Balance Check



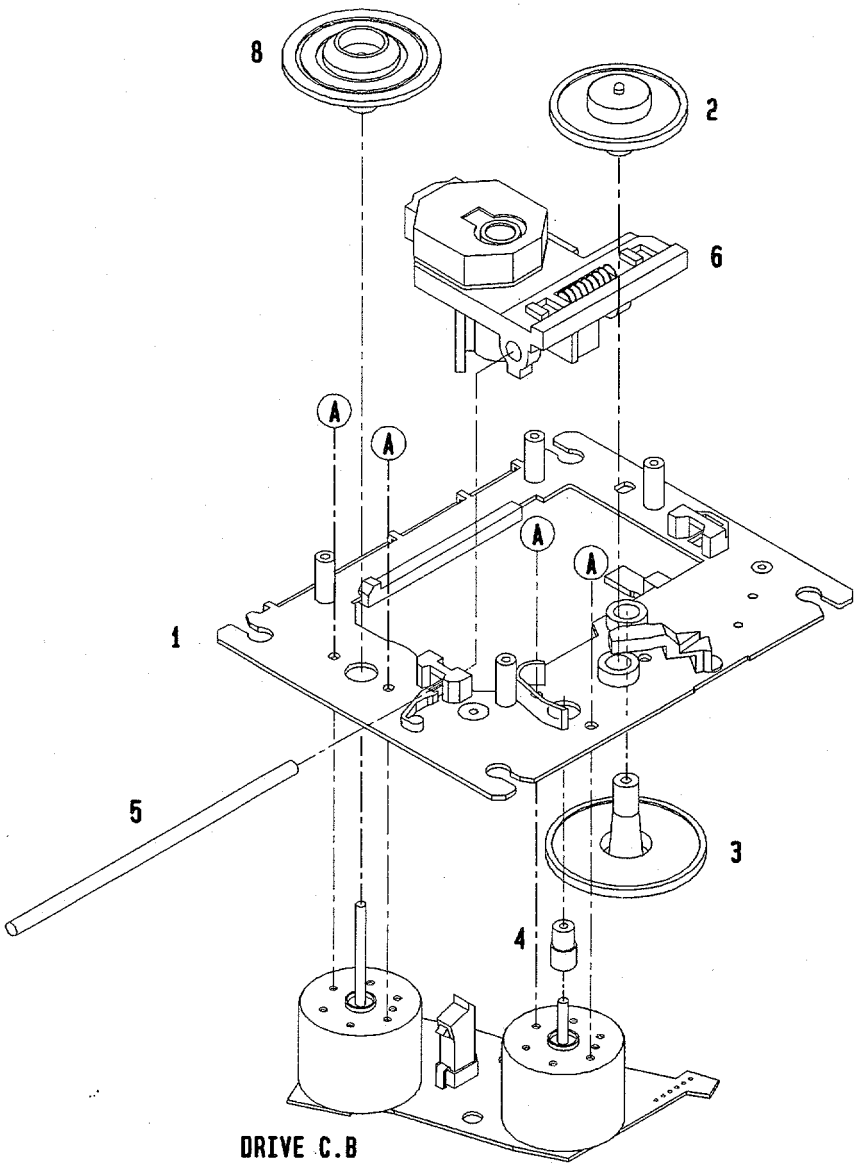
1) Connect an oscilloscope to test points TP1 (TE) and TP3 (VREF).
2) Start up the CD test mode.
3) Insert the test disc TCD-782(YEDS-18) and enter the traverse mode of the CD test mode.
4) Confirm that the traverse waveform on an oscilloscope is vertically symmetrical as shown in the figure below.
5) After confirming the waveform, release the CD test mode.



A=B

VOLT/DIV: 20mV
TIME/DIV: 1mS

CD MECHANISM EXPLODED VIEW 1 ／ 1 (3ZG-2 C2N <Z>)



CD MECHANISM PARTS LIST 1 ／ 1 (3ZG-2 C2N <Z>)

DESCRIPTIONで判断できない物は "REFERENCE NAME LIST" を参照してください。
If can't understand for Description please kindly refer to "REFERENCE NAME LIST".

REF. NO	PART NO.	カンリ NO.	DESCRIPTION
1	83-ZG2-202-71K		O-SERT S ASSY,S
2	83-ZG2-204-419		GEAR,A
3	83-ZG2-205-219		GEAR,B
4	83-ZG2-220-01K		GEAR MOTOR 2
5	83-ZG2-207-119		SHAFT,SLIDE
6	87-070-445-010		PICK-UP,KSS-213B
8	83-ZG2-233-019		TURN TABLE,A5
A	87-261-032-219		SCREW V+2-3

USE MODEL LIST

CX-NAV70 (NSX-AV70)
CX-NAV700 (NSX-AV700)
CX-NAV71 (NSX-AV71)
CX-NAV80 (NSX-AV80)
CX-NAV800 (NSX-AV800)
CX-NAV90 (NSX-AV90)
CX-NAV900 (NSX-AV900)
CX-NK300 (NSX-K300)
CX-NK700 (NSX-K700)
CX-NK77 (NSX-K77)
CX-NK80 (NSX-K80)
CX-NK90 (NSX-K90)
CX-NV300 (NSX-V300)
CX-NV3000 (NSX-V3000)
CX-NV3001 (NSX-V3001)
CX-NV390 (NSX-V390)
CX-NV500 (NSX-V500)
CX-NV700 (NSX-V700)
CX-NV705 (NSX-V705)
CX-NV710 (NSX-V710)
CX-NV715 (NSX-V715)
CX-NV720 (NSX-V720)
CX-NV770 (NSX-V770)
CX-NV800 (NSX-V800)
CX-NV8000 (NSX-V8000)
CX-NV8080 (NSX-V8080)
CX-NV820 (NSX-V820)
CX-NV900 (NSX-V900)
CX-NV9000 (NSX-V9000)
CX-NV9090 (NSX-V9090)
CX-NV915 (NSX-V915)
CX-NV929 (NSX-V929)
FD-NAKH8 (NSX-AKH8)
FD-NH8 (NSX-AVH8)
FD-NH8 (NSX-AVH8)
FD-NH80 (NSX-AVH80)
FD-NH9 (NSX-AVH9)
FD-NH9 (NSX-AVH9)
FD-NH90 (NSX-AVH90)
FD-SNAKH8 (NSX-AKH8)
FD-SNH9 (NSX-AVH9)

REFERENCE NAME LIST

ELECTRICAL SECTION

DESCRIPTION	REFERENCE NAME
ANT	ANTENNAS
C-	CHIP
C-CAP	CAP, CHIP
C-CAP TN	CAP, CHIP TANTALUM
C-COIL	COIL, CHIP
C-DI	DIODE, CHIP
C-DIODE	DIODE, CHIP
C-FET	FET, CHIP
C-FOTR	FILTER, CHIP
C-JACK	JACK, CHIP
C-LED	LED, CHIP
C-RES	RES, CHIP
C-SFR	SFR, CHIP
C-SLIDE SW	SLIDE SWITCH, CHIP
C-SW	SWITCH, CHIP
C-TR	TRANSISTOR, CHIP
C-VR	VOLUME, CHIP
C-ZENER	ZENER, CHIP
CAP, CER	CAP, CERA-SOL
CAP, E	CAP, ELECT
CAP, M/F	CAP, FILM
CAP, TC	CAP, CERA-SOL
CAP, TC-U	CAP, CERA-SOL SS
CAP, TN	CAP, TANTALUM
CERA FIL	FILTER, CERAMIC
CF	FILTER, CERAMIC
DL	DELAY LINE
E/CAP	CAP, ELECT
FILT	FILTER
FLTR	FILTER
FUSE RES	RES, FUSE
MOT	MOTOR
P-DIODE	PHOTO DIODE
P-SNSR	PHOTO SENSER
P-TR	PHOTO TRANSISTOR
POLY VARI	VARIABLE CAPACITOR
PPCAP	CAP, PP
PT	POWER TRANSFORMER
PTR, RES	PTR, MELF
RC	REMOTE CONTROLLER
RES NF	RES, NON-FLAMMABLE
RESO	RESONATOR
SHLD	SHIELD
SOL	SOLENOID
SPKR	SPEAKER
SW, LVR	SWITCH, LEVER
SW, RTRY	SWITCH, ROTARY
SW, SL	SWITCH, SLIDE
TC CAP	CAP, CERA-SOL
THMS	THERMISTOR
TR	TRANSISTOR
TRIMMER	CAP, TRIMMER
TUN-CAP	VARIABLE CAPACITOR
VIB, CER	RESONATOR, CERAMIC
VIB, XTAL	RESONATOR, CRYSTAL
VR	VOLUME
ZENER	DIODE, ZENER
サージサプレッサ	SERGESUPPRESSOR
セラコン	CAP,CERA

MECHANICAL SECTION

DESCRIPTION	REFERENCE NAME
ADHESHIVE	SHEET ADHESHIVE
AZ	AZIMUTH
BAR-ANT	BAR-ANTENNA
BAT	BATTERY
BATT	BATTERY
BRG	BEARING
BTN	BUTTON
CAB	CABINET
CASS	CASSETTE
CHAS	CHASSIS
CLR	COLLAR
CONT	CONTROL
CRSR	CURSOR
CU	CUSHION
CUSH	CUSHION
DIR	DIRECTION
DUBB	DUBBING
FL	FRONT LOADING
FLY-WHL	FLYWHEEL
FR	FRONT
FUN	FUNCTION
G-CU	G-CUSHION
HDL	HANDOL
HIMERON	CLOTH
HINGE, BAT	HINGE, BATTERY
HLDR	HOLDER
HT-SINK	HEAT SINK
IB	INSTRUCTION BOOKLET
IDLE	IDLER
IND, L-R	INDICATOR, L-R
KEY, CONT	KEY, CONTROL
KEY, PRGM	KEY, PROGRAM
KNOB, SL	KNOB, SLIDE
LBL	LABEL
LID, BATT	LID, BATTERY
LID, CASS	LID, CASSETTE
LVR	LEVER
P-SP	P-SPRING
PANEL, CONT	PANEL, CONTROL
PANEL, FR	PANEL, FRONT
PRGM	PROGRAM
PULLY, LOAD MO	PULLY, LOAD MOTOR
RBN	RIBBON
S-	SPECIAL
SEG	SEGMENT
SH	SHEET
SHLD-SH	SHIELD-SHEET
SL	SLIDE
SP	SPRING
SP-SCREW	SPECIAL-SCREW
SPACER, BAT	SPACER, BATTERY
SPR	SPRING
SPR-P	P-SPRING
SPR-PC-PUSH	P-SPRING, C-PUSH
T-SP	T-SPRING
TERM	TERMINAL
TRIG	TRIGGER
TUN	TUNING
VOL	VOLUME
W	WASHER
WHL	WHEEL
WORM-WHL	WORM-WHEEL
ジグアーム	ARM,SHAFT
ジグガイド	GUIDE,SHAFT
ストラップ	STRAP
トクナベ	S-SCREW
ヒンジ	HINGE
ヒンジビス	S-SCREW
ビスセレート	SCREW,SERRART

サービス技術ニュース	
番 号	連絡内容
G－　－	
G－　－	
G－　－	

アイワ株式会社
AIWA CO.,LTD.

912162, 750038

Tokyo Japan

〒110 東京都台東区池之端１－２－11　☎ 03 (3827) 3111 （代表）

Printed in Singapore