Primary-Side PWM Power Switch with CV/CC Operation

VER. 00

General Description

The LD7922 integrates a 700V power MOSFET and a primary-side feedback PWM controller with CV/CC operation in a DIP-7 package. The LD7922 is designed for low power adapter/charger and LED lighting applications. It minimizes the components counts and is available in tiny packages. Those make it an ideal design for low cost applications.

The LD7922 provides constant voltage, constant current (CV/CC) operation requiring neither photo-coupler nor secondary control circuit. Also, the LD7922 features OTP (Over Temperature Protection) and OVP (Over Voltage Protection) to prevent the circuit from being damaged under abnormal conditions.

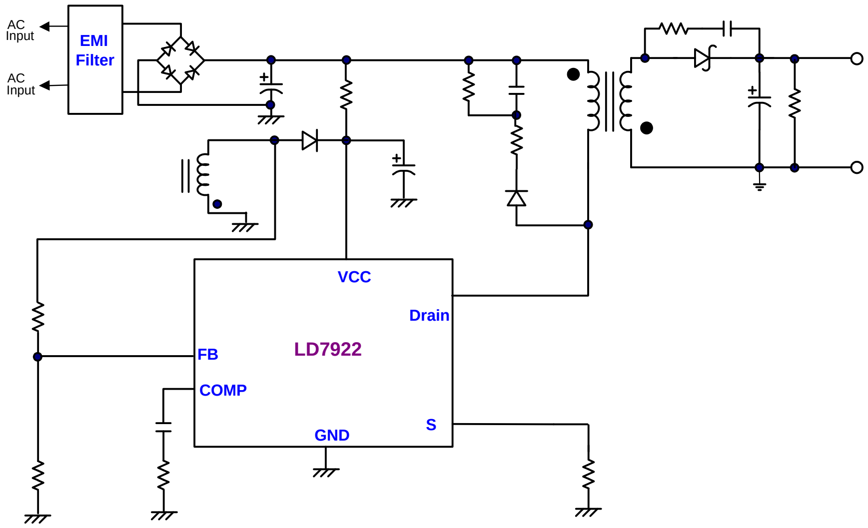
Features

- Built-in 700V Power MOSFET
- Primary-side Feedback Control
- Constant Current Control
- Built-in Load Regulation Compensation
- Built-in Primary Winding Inductance Compensation
- Low Startup Current (<16μA)
- Current Mode Control with Cycle-by-Cycle Current Limit
- Green Mode Control
- UVLO (Under Voltage Lockout)
- LEB (Leading-Edge Blanking) on CS Pin
- OVP (Over Voltage Protection) on Vcc
- OTP (Over Temperature Protection)

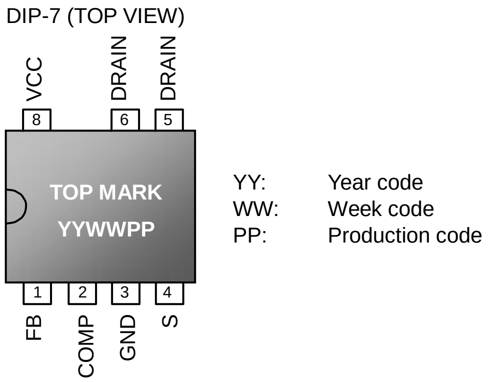
Applications

- AC-DC Adapter and Charger
- AC-DC LED Lighting

Typical Application



Pin Configuration



Ordering Information

Part number	Package	Top Mark	Shipping
LD7922 GM7	DIP-7	LD7922GM7	3600/ Tube/ Carton

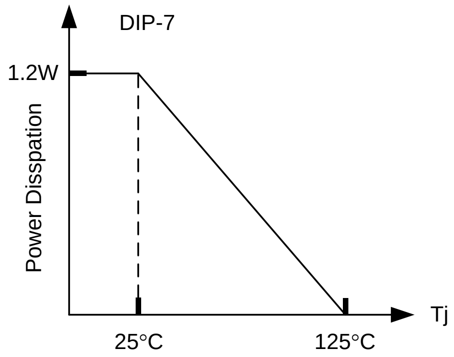
The LD7922 is green packaged.

Pin Descriptions

DIP-7 PIN	NAME	FUNCTION
1	FB	Voltage Feedback Sense. This pin detects the output voltage information based on voltage of auxiliary winding.
2	COMP	Output of the error amplifier for voltage compensation
3	GND	Ground of the controller
4	S	Source of internal power MOSFET, connecting a sense resistor to ground.
5	Drain	Drain terminal of the internal power MOSFET
6	Drain	Drain terminal of the internal power MOSFET
8	VCC	Power supply to Vcc

Output Power Table & De-rating Curve

Product	Drain Current	Rds(on) *	230VAC ± 15% **		90~264VAC **	
			Adapter	Open Frame	Adapter	Open Frame
LD7922	2A	6Ω	11~13W	13~14W	9~11W	11~12W



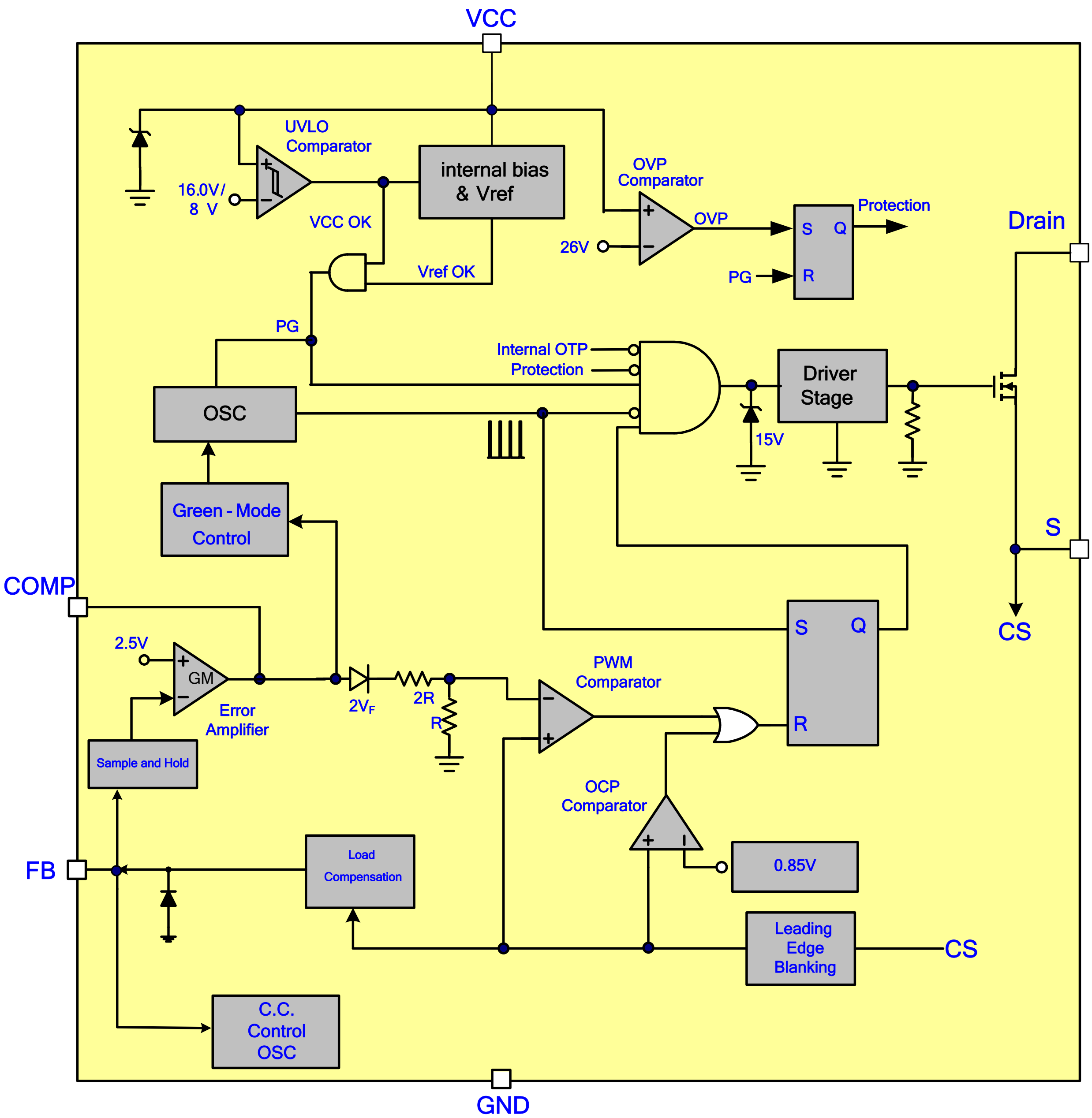
*Typ.@25°C, V_{CC}=12V Drain Current=0.5A

**Calculated maximum Input Power Rating at Ta=25°C

Recommended Operating Conditions

Item	Min.	Max.	Unit
Supply Voltage Vcc	9	24	V
Start-up capacitor	2.2	22	μF

Block Diagram



Absolute Maximum Ratings

Supply Voltage VCC,	-0.3 ~29V
Drain	-0.3~700V
COMP, FB, S	-0.3 ~6V
Maximum Junction Temperature	150°C
Peak Pulse drain current1, TC=25°C	2.0A
Total Power Dissipation of DIP-7, Ta=25°C	1.2W
Package thermal resistance (DIP-7), θ_{JA}	80°C/W[2]
Operating Ambient Temperature	-40°C to 85°C
Operating Junction Temperature	-40°C to 125°C
Storage Temperature Range	-65°C to 150°C
Lead temperature (Soldering, 10sec)	260°C
ESD Voltage Protection, Human Body Model (Exclusive Drain Pin)	2.5 KV
ESD Voltage Protection, Machine Model (Exclusive Drain Pin)	250 V

1. Repetitive rating: Pulse width limited by maximum junction temperature
2. w/o heat-sink, under natural convection

Caution:

Stress exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stress above Recommended Operating Conditions may affect device reliability

Electrical Characteristics

(T_A = +25°C unless otherwise stated, V_{CC}=15.0V)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage (Vcc Pin)					
Startup Current			10	16	μA
Operating Current	V_{COMP}=0V		1.8		mA
	V_{COMP}=3.6V,		2.1		mA
	OVP tripped	0.5	0.65	0.74	mA
UVLO (off)		7.0	8	9	V
UVLO (on)		15	16	17	V
V_{CC} OVP Level		25	26	27	V
Error Amplifier (CV mode, Comp pin, FB pin)					
Reference Voltage, V_{REF}		2.47	2.500	2.53	V
Transconductance		110	150	190	μmho
Output Sink Current	V_{FB}=3.2V, V_{COMP}=2.5V	64	75	96	μA
Output Source Current	V_{FB}=1.8V, V_{COMP} =2.5V	-96	-75	-64	μA
Output Upper Clamp Voltage	V_{FB}=2.3V	4.0	4.1	4.3	V
Load Compensation Current	V_{CS}=0.75V	11	13.5	16	μA
Load Compensation Cut-off Voltage	Load compensation current=0μA		0.2		V
Sample and Hold					
Sampling Delay Time	*		1.8		μs
Sampling Time	*		0.4		μs
Current Sensing (CS Pin)					
Maximum Input Voltage, V_{CS}(off)		0.83	0.85	0.87	V
V_{CS}-min	V_{COMP} < 1.8V	0.17	0.2	0.22	V
Leading Edge Blanking Time		380	430	510	ns
Input impedance		1			MΩ

*These parameters are guaranteed by design only.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Oscillator for Switching Frequency (CV mode, COMP Pin)					
Frequency	COMP=3.6V	61	65	69	kHz
Green Mode Frequency		18	20	24	kHz
Minimum Frequency		0.9	1.4	1.7	kHz
Trembling Frequency	COMP=3.6V		± 4		kHz
Temp. Stability	(-20°C ~125°C)*		5		%
Voltage Stability	(V_{CC}=9V-24V)*		1		%
Maximum Frequency Mode Threshold VCOMP, V_{SMAX}	*		3.0		V
Green Mode Threshold V_{COMP1}, V_{SG1}	*		2.7		V
Green Mode Threshold V_{COMP2}, V_{SG2}	*		1.9		V
Minimum Frequency V_{COMP}, V_{SMIN}	*		1.6		V
Maximum duty		57	60	63	%
Oscillator for Switching Frequency (CC mode)					
Max. Frequency		61	65	69	kHz
Minimum Frequency		17.5	20	24	kHz
Trembling Frequency			± 6		%
On Chip OTP (Over Temperature)					
OTP Level	*		140		°C
OTP Hysteresis	*		40		°C

*These parameters are guaranteed by design only.

Electrical Characteristics for MOSFET

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage					
Breakdown Voltage BV_{DSS}	V_{CC}=0V, COMP=0V, I_D=250μA	700			V
Drain Leakage Current					
Drain-Source Leakage Current	V_{DS}=700V, Vcc=0V, T_J=25°C	0		1	μA
	V_{DS}=560V, Vcc=0V, T_J=125°C	0		10	μA
Drain on Resistance					
Drain to S pin On-Resistance	I_D=0.5A; V_{CC}=15V; Tj=25°C		6		Ω

Typical Performance Characteristics

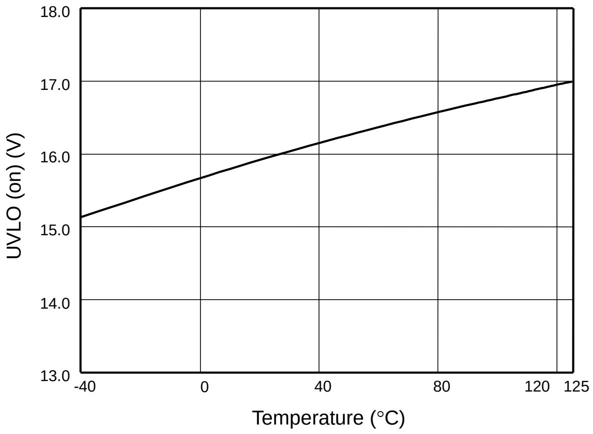


Fig. 1 UVLO (on) vs. Temperature

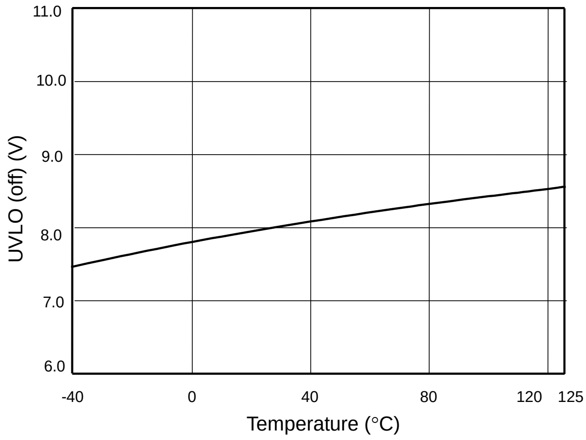


Fig. 2 UVLO (off) vs. Temperature

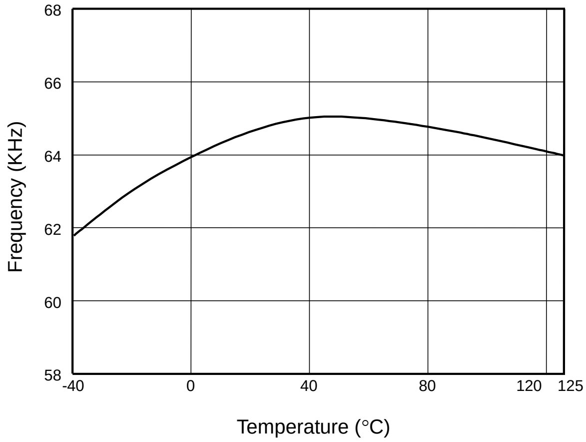


Fig. 3 Frequency vs. Temperature

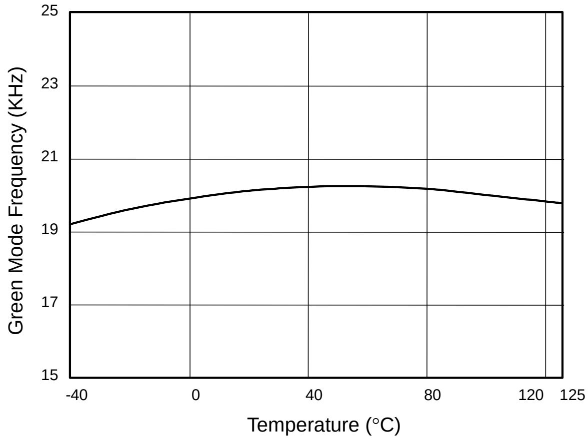


Fig. 4 Green Mode Frequency vs. Temperature

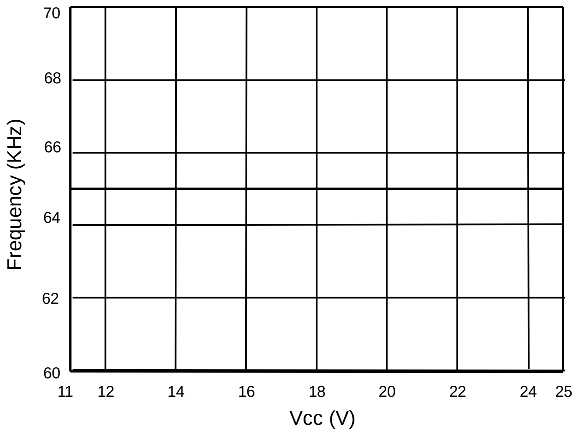


Fig. 5 Frequency vs. Vcc

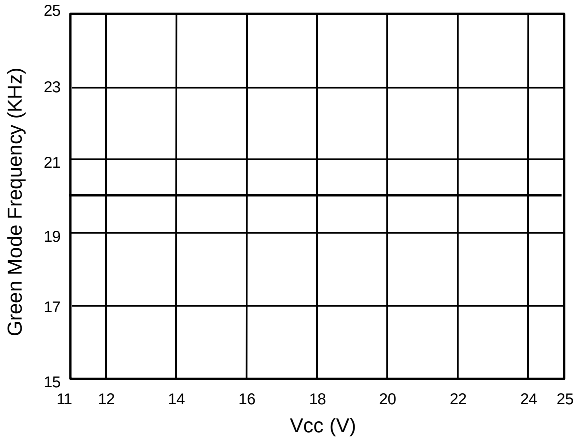


Fig. 6 Green Mode Frequency vs. Vcc

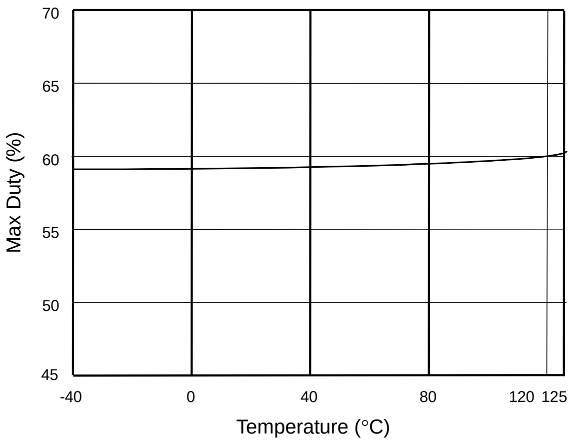


Fig. 7 Max Duty vs. Temperature

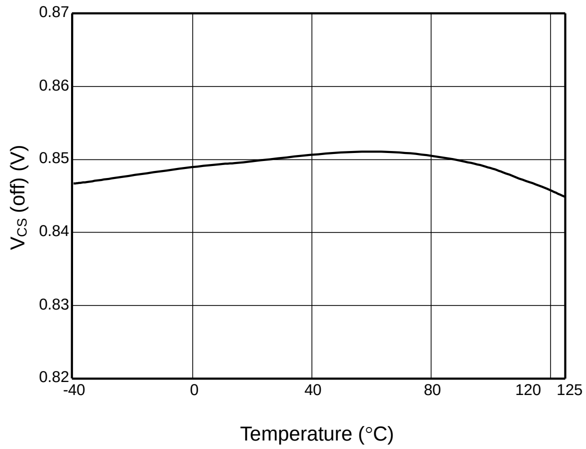


Fig. 8 V_{CS} (off) vs. Temperature

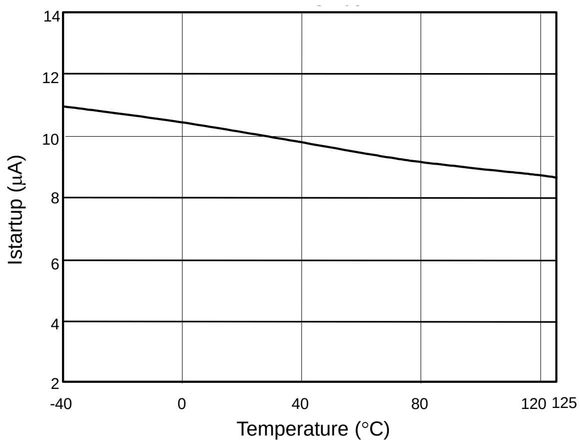


Fig. 9 Startup Current (Istartup) vs. Temperature

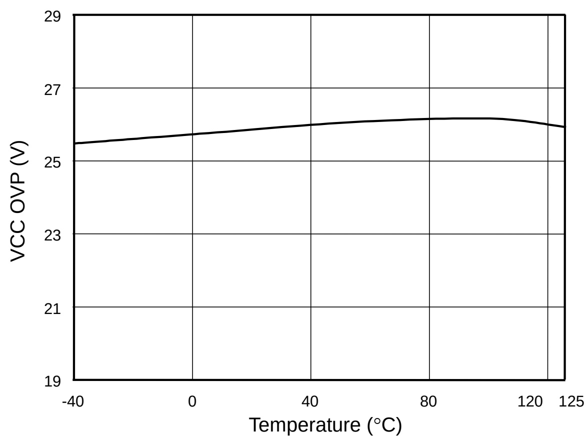


Fig. 10 VCC OVP vs. Temperature

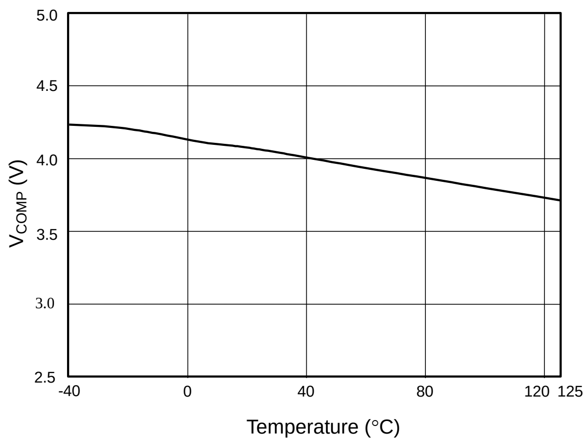


Fig. 11 V_{COMP} open loop voltage vs. Temperature

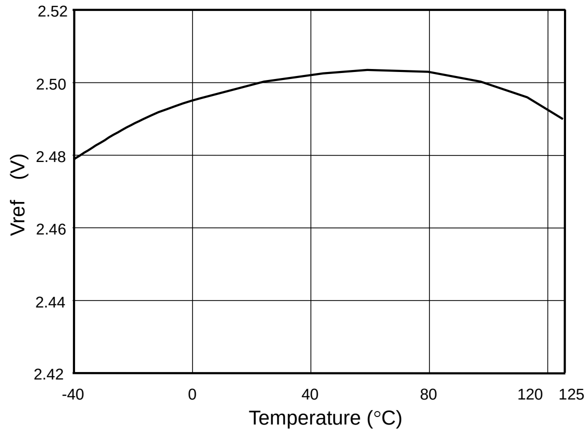


Fig. 12 Vref vs. Temperature

Application Information

Operation Overview

The LD7922 integrates a 700V power MOSFET and a primary-side feedback PWM controller with CV/CC operation in a DIP-7 package. The LD7922 is designed for low power adapter/charger and LED lighting applications. It meets the green-power requirement and is intended for the use in those modern switching power suppliers and linear adaptors that demand higher power efficiency and power-saving. Its major features are described as below.

Under Voltage Lockout (UVLO)

An UVLO comparator is implemented to detect the voltage on VCC pin. It would assure the supply voltage enough to turn on the LD7922 PWM controllers and further to drive the power MOSFET. As shown in Fig. 13, a hysteresis is built in to prevent shutdown from the voltage dip during startup.

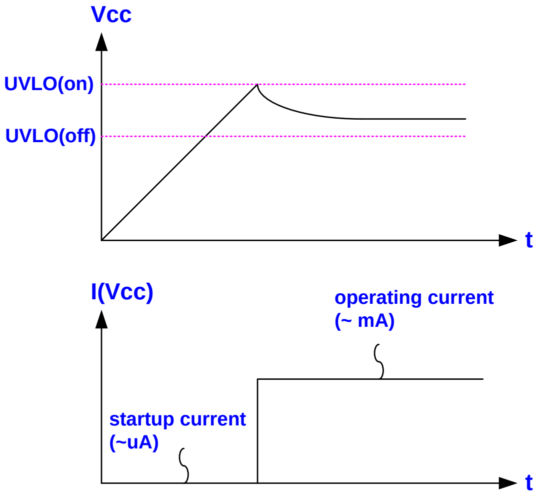


Fig. 13

Startup Current and Startup Circuit

The typical startup circuit to generate the LD7922 Vcc is shown in Fig. 14. During the startup transient, the Vcc is below UVLO threshold thus there is no gate pulse produced from LD7922 to drive power MOSFET. Therefore, the current through R1 will provide the startup current and to charge the capacitor C1. When the Vcc voltage is large enough to turn on the LD7922 and further to deliver the gate drive signal, the supply current is provided from the auxiliary winding of the transformer. Requirement for lower startup current on the PWM controller will help to increase the value of R1 and then reduce the power consumption on R1. In using CMOS process and the special circuit design, LD7922 requires 10µA (Typ.) only for the maximum startup current. If a greater resistor R1 is chosen, it usually takes more time to start up. To carefully select the value of R1 and C1 will optimize the power consumption and startup time. If less start-up time is required, a two-step start-up circuit is recommended for it, as shown in Fig. 15. In this circuit example, a smaller capacitor C1 can be used to minimize startup time. The energy for the controller after start-up is mainly from a larger capacitor C2.

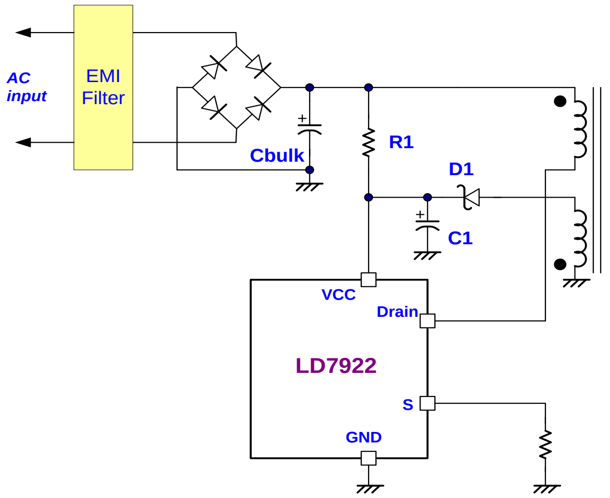


Fig. 14

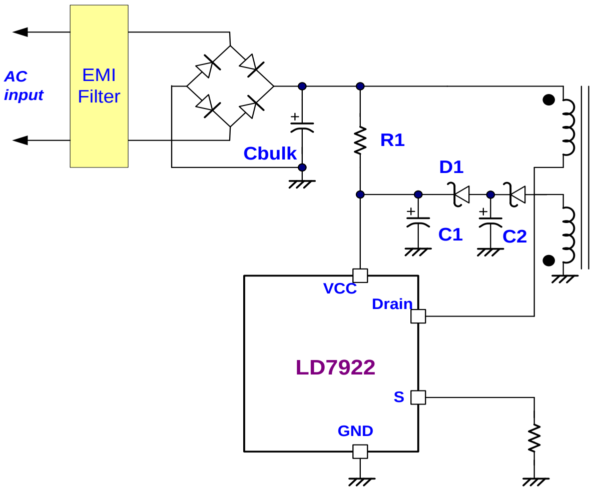


Fig. 15

Principle of CV Operation

In the DCM flyback converter, the output voltage can be sensed by the auxiliary winding. LD7922 samples the auxiliary winding on the primary-side to regulate the output voltage, as shown in the Fig 16. The voltage induced in the auxiliary winding is a reflection of the secondary winding voltage while the MOSFET is in off state. Via a resistor divider connected between the auxiliary winding and FB pin, the auxiliary voltage is sampled after the sample delay time and will be hold until the next sampling. The sampled voltage is compared with internal reference V_{REF} (2.5V) and the error will be amplified. The error amplifier output COMP reflects the load condition and controls the duty cycle to regulate the output voltage, thus constant output voltage can be achieved. The output voltage is given as:

$$V_{OUT} = 2.5V(1+\frac{Ra}{Rb})(\frac{Ns}{Na}) - V_f$$

Where V_F indicates the drop voltage of the output Diode, Ra and Rb are values for top and bottom feedback resistor, Ns and Na are the turns of transformer secondary and auxiliary.

In case that the output voltage is sensed through the auxiliary winding; the leakage inductance will induce ringing to affect output regulation. Optimizing the drain voltage clamp circuit to minimize the high frequency ringing will achieve the best regulation. Fig. 17 shows the desired drain voltage waveform in compare to Fig. 18 with a large undershoot due to the leakage inductance induced ring. This will cause error to the sample and inferior performance to the output voltage regulation. A proper selection for resistor R_S, in series with the clamp diode, may reduce any large undershoot, as shown in Fig. 19.

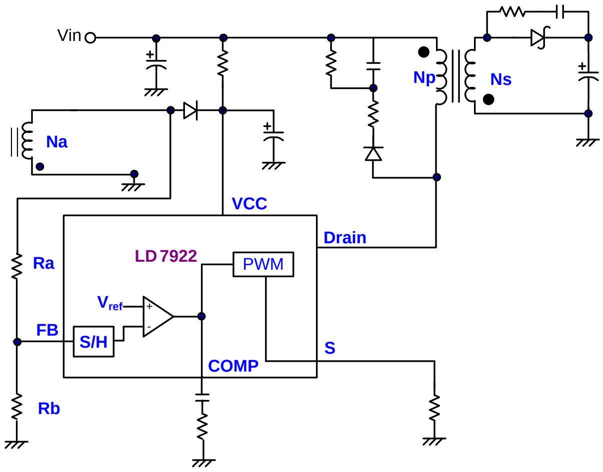


Fig.16

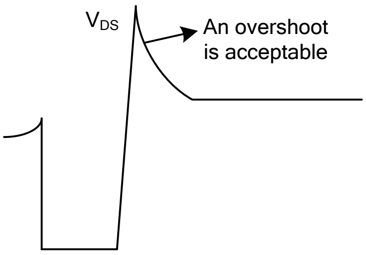


Fig.17

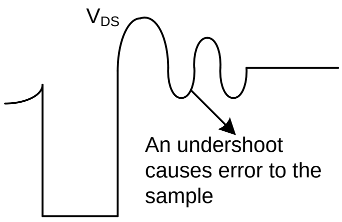


Fig.18

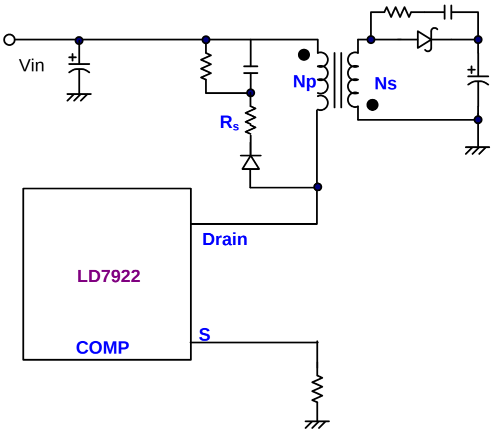


Fig.19

Load Regulation Compensation

In LD7922, load regulation compensation is implemented to compensate the cable voltage droop and to achieve a better voltage regulation. An offset voltage is generated at FB by an internal sink current source flowing into the FB during the sample period. The built-in sink current source is proportional to the peak value of Vcs. As a result, it is proportional to the output load current, thus the drop due to the cable loss can be compensated. As the load current decreases from full-load to no-load, the offset voltage at FB will decrease. It can also be programmed by adjusting the resistance of the divider to compensate the drop for various cable lines used. The equation of internal sink current source is shown as:

$$I_{FB} = (V_{CS,pk} - 0.2) * 24.5\,(\mu A)$$

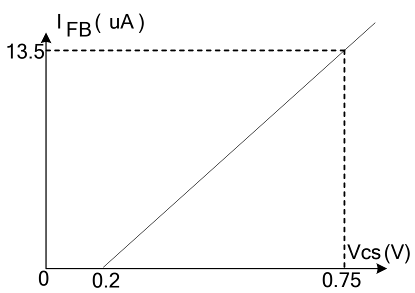


Fig. 20

Principle of C.C. Operation

To support with the proprietary CC/CV control of the LD7922, a system designed in DCM mode is required for flyback converter, as shown in Fig. 21. The output current Io can be expressed as:

$$I_O = \frac{1}{2}\frac{i_{S,PK} \times T_{DIS}}{T_S}$$
$$= \frac{1}{2}\frac{N_P}{N_S} \times i_{P,PK} \times \frac{T_{DIS}}{Ts}$$
$$= \frac{1}{2}\frac{N_P}{N_S} \times \frac{V_{CS} - OFF}{R_S} \times \frac{T_{DIS}}{T_S}$$

As a result, the output current Io can be controlled by the Vcs-off and Ts. In the C.C. mode, Vcs-off will be controlled as a constant, 0.85V and the ratio of T_{DIS}/Ts will be modulated as a constant (T_{DIS}/Ts=0.4). In order to set Tdis/Ts=0.4, the switching frequency will be programmed according to T_{DIS}, as shown as below.

$$f_S = \frac{1}{T_S} = \frac{0.4}{T_{DIS}}$$

The C.C. point and maximum output power can be externally adjusted through external current sense resistor Rs of CS pin. The greater Rs, the smaller CC point is, and the smaller output power becomes, and vice versa as shown in Fig. 22.

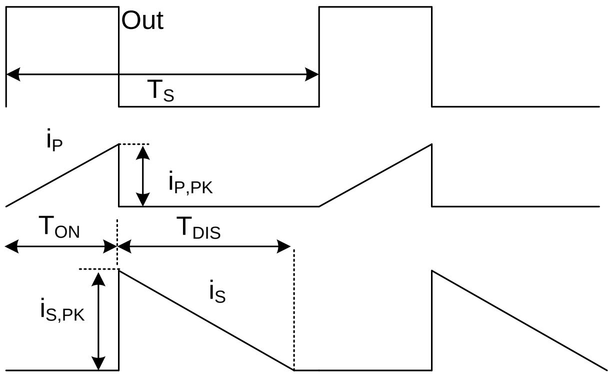


Fig. 21

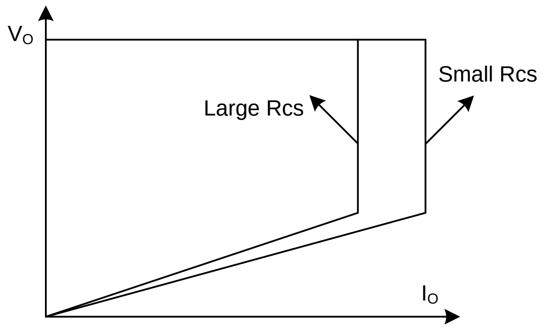


Fig. 22

Current Sensing, load compensation, and Leading-edge Blanking

The typical current mode of PWM controller feeds back with current signal and voltage signal to close the control loop and achieves regulation. The LD7922 detects the primary MOSFET current from the CS pin for the peak current mode control and the pulse-by-pulse current limit. The maximum voltage threshold of the current sensing pin is set at 0.85V. From above, the MOSFET peak current can be obtained as below.

$$I_{PEAK(MAX)} = \frac{0.85V}{R_S}$$

A leading-edge blanking (LEB) time is included in the input of CS pin to prevent the false-trigger from current spike.

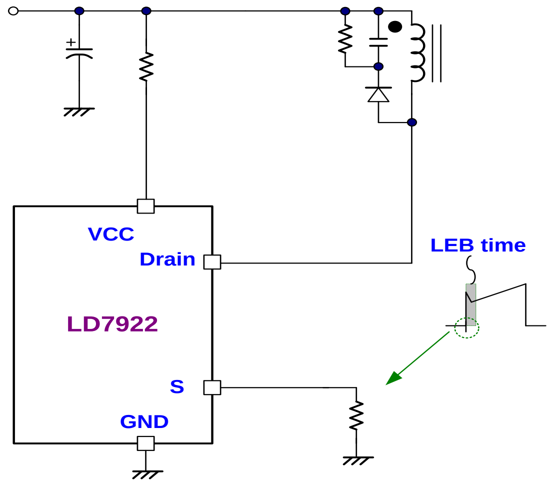


Fig. 23

Oscillator and Switching Frequency (CV Mode)

The switching frequency of LD7922 is various to provide the optimized operations either in heavy load or light load. In heavy load, the switching frequency is fixed at 65 kHz. In light load conditions, the LD7922 operates at a lower frequency to reduce the switching loss. Fig. 15 shows the characteristics of the switching frequency vs. the comp pin voltage (V_{COMP}). In heavy load conditions, the V_{COMP} is higher than V_{SMAX} and the switching frequency will start to linearly increase from 20kHz to 65kHz. In light load conditions, the V_{COMP} is lower than V_{SG2} and the switching frequency will start to linearly decrease from 20kHz to 1.4 kHz. The switching frequency is reduced to a minimum frequency of 1.4kHz, enhancing power saving to meet requirements for international power conservation.

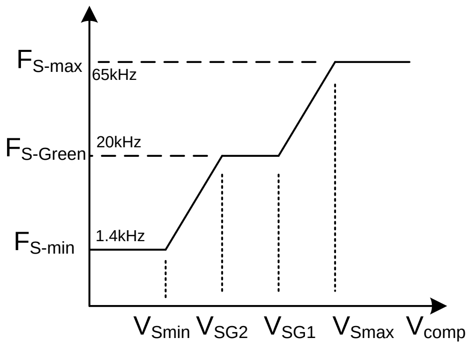


Fig. 24

Frequency Swapping (LD property)

The LD7922 is built-in with frequency swapping function, which enables the power supply designers to optimize EMI performance and system cost. The swapping frequency was internally set between ±6% of switching frequency.

Maximum Duty-Cycle

The maximum duty-cycle of LD7922 is limited for 60% (V_{COMP} > 3.0V) to avoid the transformer saturation.

OVP (Over Voltage Protection) on Vcc

The V_{GS} ratings of the nowadays power MOSFETs are often limited up to max. 30V. To prevent the V_{GS} from being damaged due to fault condition, LD7922 is implemented with OVP function on Vcc. If the Vcc voltage rises above the OVP voltage threshold, the output gate drive circuit will be shutdown simultaneously and to stop the switching of the power MOSFET until the next UVLO(on). The Vcc OVP function of LD7922 is an auto-recovery type protection. The Fig. 25 shows its operation. As soon as OVP condition is removed, the Vcc level will resume to normal and the output will automatically return to the normal operation.

Over-Temperature Protection (OTP)

An internal OTP circuit is embedded in the LD7922 to provide the worst-case protection for this controller. When the chip temperature rises above trip OTP level, the output will be disabled until the chip is cooled down below the hysteresis window.

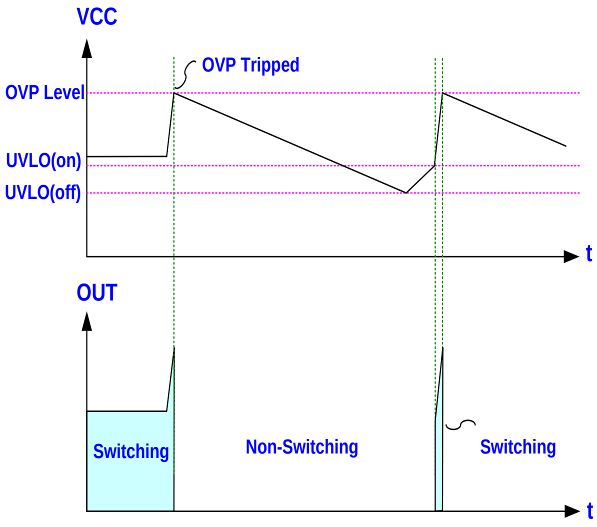
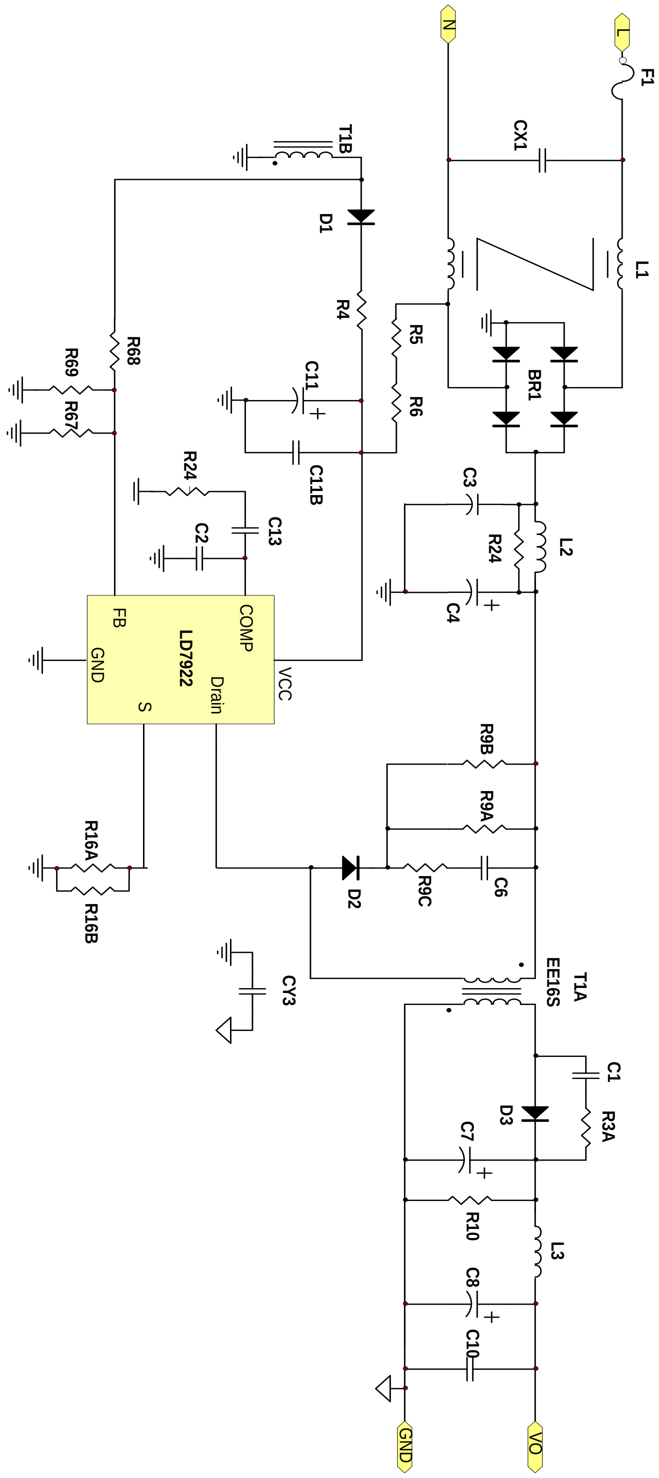


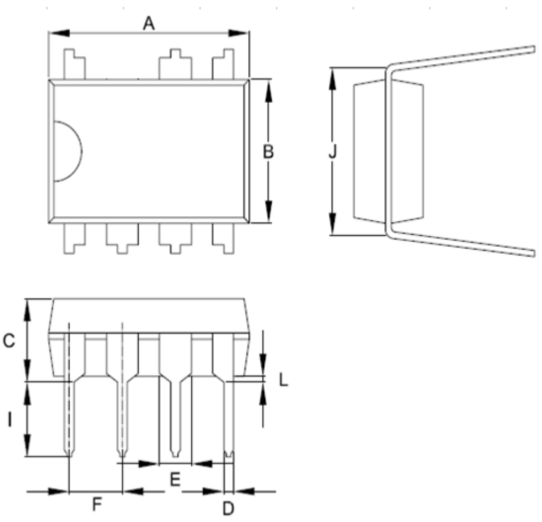
Fig. 25

Reference Application Circuit --- 9.8W (14V/700mA)



Package Information

DIP-7



	Dimension in Millimeters		Dimensions in Inches	
Symbol	**Min**	**Max**	**Min**	**Max**
A	9.017	10.160	0.355	0.400
B	6.096	7.112	0.240	0.280
C	-----	5.334	------	0.210
D	0.356	0.584	0.014	0.023
E	1.143	1.778	0.045	0.070
F	2.337	2.743	0.092	0.108
I	2.921	3.556	0.115	0.14
J	7.366	8.255	0.29	0.325
L	0.381	------	0.015	--------

Important Notice

Leadtrend Technology Inc. reserves the right to make changes or corrections to its products at any time without notice. Customers should verify the datasheets are current and complete before placing order.

Revision History

Rev.	Date	Change Notice
00	8/2/2012	Original Specification