DATA SHEET

TDA4780
RGB video processor with automatic cut-off control and gamma adjust

Product specification
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Philips
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RGB video processor with automatic cut-off control and gamma adjust

TDA4780

FEATURES

- Gamma adjust
- Dynamic black control (adaptive black)
- All input signals clamped on black-levels
- Automatic cut-off control, alternative: output clamping on fixed levels
- Three adjustable reference voltage levels via the I²C-bus for automatic cut-off control
- Luminance/colour difference interface
- Two luminance input levels allowed
- Two RGB interfaces controlled by either fast switches or by the I²C-bus
- Two peak drive limiters, selection via the I²C-bus
- Blue stretch; selection via the I²C-bus
- Luminance output for Scan Velocity Modulation (SCAVEM)
- Extra luminance output; same pin can be used as hue control output e.g. for the TDA4650 and TDA4655
- Non standard operations like 50 Hz vertical at 32 kHz horizontal are also possible
- Either 2 or 3 level sandcastle pulse applicable
- High bandwidth for 32 kHz application
- White point adjusts via the I²C-bus
- Average beam current and improved peak drive limiting
- Two switch-on delays to prevent discoloration during start-up
- All functions and features programmable via the I²C-bus
- PAL/SECAM or NTSC matrix selection.

GENERAL DESCRIPTION

The TDA4780 is a monolithic integrated circuit with a luminance and a colour difference interface for video processing in TV receivers. Its primary function is to process the luminance and colour difference signals from a colour decoder which is equipped e.g. with the multistandard decoder TDA4655 or TDA9160 plus delay line TDA4661 or TDA4665 and the Picture Signal Improvement (PSI) IC TDA467X or from a feature module.

The required input signals are:

- Luminance and negative colour difference signals
- 2 or 3-level sandcastle pulse for internal timing pulse generation
- I²C-bus data and clock signals.

Two sets of analog RGB colour signals can also be inserted, e.g. one from a peritelevision connector (SCART plug) and the other one from an On-Screen Display (OSD) generator. The TDA4780 has I²C-bus control of all parameters and functions with automatic cut-off control of the picture tube cathode currents. It provides RGB output signals for the video output stages. In clamped output mode it can also be used as an RGB source.

The main differences with the sister type TDA4680 are:

- Additional features; namely gamma adjust, adaptive black, blue stretch and two different peak drive limiters
- The measurement lines are triggered by the trailing edge of the vertical component of the sandcastle pulse
- I²C-bus receiver only; automatic white level control is not provided; the white levels are determined directly by the I²C-bus data
- The TDA4780 is pin compatible (except pin 18) with the TDA4680. The I²C-bus slave address can be used for both ICs. When a function of the TDA4780 is not included in the TDA4680, the I²C-bus command is not executed. Special commands (except control bit FSWL) for the TDA4680 will be ignored by the TDA4780.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage (pin 5)		7.2	8.0	8.8	V
I_P	supply current (pin 5)		80	100	120	mA
$V_{8(p-p)}$	input signal (composite signal; VBS; peak-to-peak value)	adaption to two signal levels				
		bit YHI = 0	–	0.45	–	V
		bit YHI = 1	–	1.43	–	V
$V_{6(p-p)}$	–(B – Y) input signal (peak-to-peak value)		–	1.33	–	V
$V_{7(p-p)}$	–(R – Y) input signal (peak-to-peak value)		–	1.05	–	V
V_{14}	required voltage range for sandcastle pulse	three-level				
		H + V	2.0	2.5	3.0	V
		H	4.0	4.5	4.9	V
		BK	6.1	–	V_P + 5.8	V
		two-level				
		H + V	2.0	2.5	3.0	V
		BK	4.0	–	V_P + 5.8	V
$V_{i(p-p)}$	RGB input signals at pins 2, 3, 4, 10, 11 and 12 (peak-to-peak value)		–	0.7	–	V
$V_{24,22,20(nom)}$	nominal signal amplitude for RGB output at pins 24, 22 and 20 (black-white)		1.7	2.0	2.3	V
T_{amb}	ambient temperature		–20	–	+70	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA4780	DIP28	plastic dual in-line package; 28 leads (600 mil)	SOT117-1

BLOCK DIAGRAM

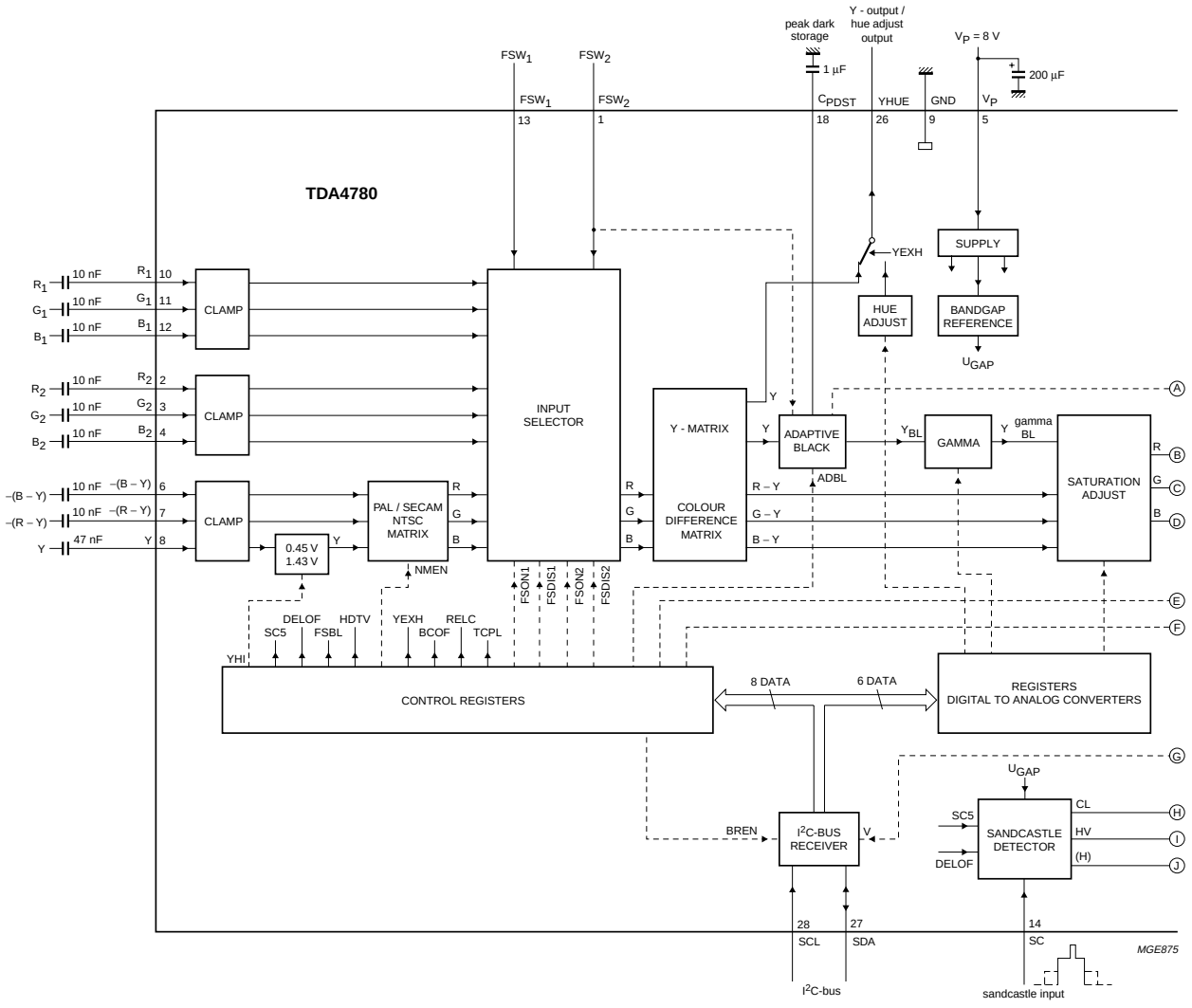


Fig.1 Block diagram (continued in Fig.2).

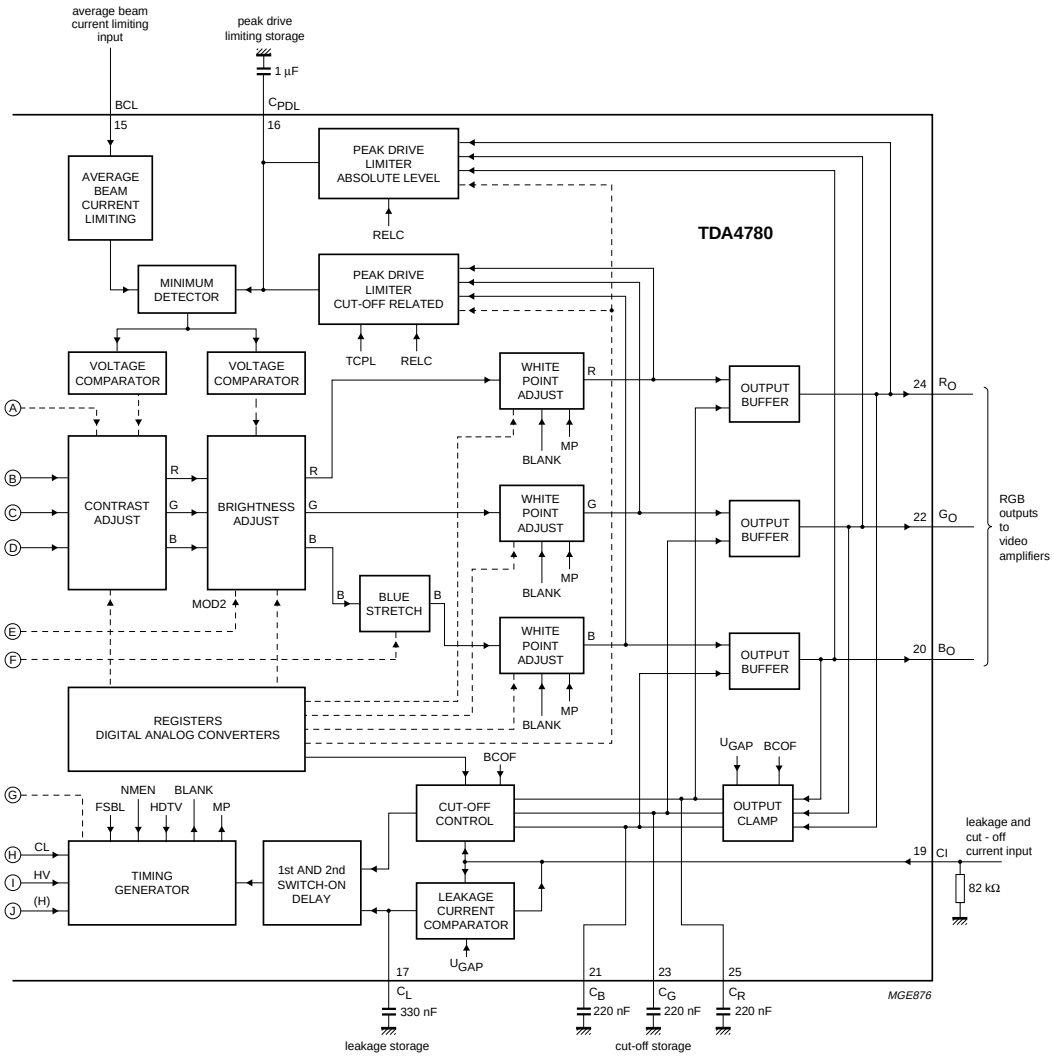


Fig.2 Block diagram (continued from Fig.1).

PINNING

SYMBOL	PIN	DESCRIPTION
FSW_2	1	fast switch 2 input
R_2	2	red input 2
G_2	3	green input 2
B_2	4	blue input 2
V_P	5	supply voltage
–(B – Y)	6	colour difference input –(B – Y)
–(R – Y)	7	colour difference input –(R – Y)
Y	8	luminance input
GND	9	ground
R_1	10	red input 1
G_1	11	green input 1
B_1	12	blue input 1
FSW_1	13	fast switch 1 input
SC	14	sandcastle pulse input
BCL	15	average beam current limiting input
C_{PDL}	16	storage capacitor for peak drive limiting
C_L	17	storage capacitor for leakage current compensation
C_{PDST}	18	storage capacitor for peak dark
CI	19	cut-off measurement input
B_O	20	blue output
C_B	21	blue cut-off storage capacitor
G_O	22	green output
C_G	23	green cut-off storage capacitor
R_O	24	red output
C_R	25	red cut-off storage capacitor
YHUE	26	Y-output or hue adjust output
SDA	27	I^2C-bus serial data input or acknowledge output
SCL	28	I^2C-bus serial clock input

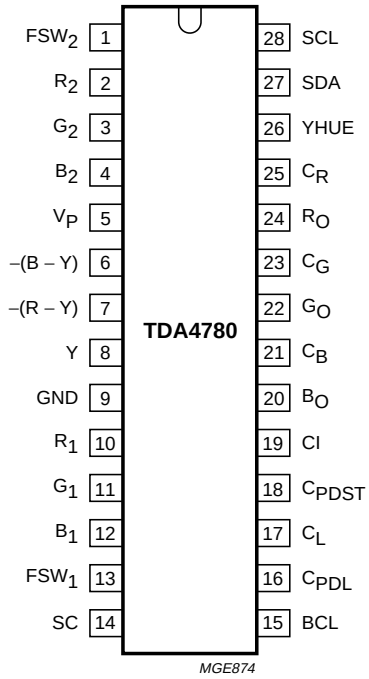


Fig.3 Pin configuration.

FUNCTIONAL DESCRIPTION

Signal input stages

The TDA4780 contains 3 sets of input signal stages for:

1. Luminance and colour difference signals:
   a) Y: 0.45 V (p-p) VBS or 1.43 V (p-p) VBS; selectable via the I^2C-bus
   b) –(R – Y): 1.05 V (p-p)
   c) –(B – Y): 1.33 V (p-p).

   The capacitively coupled signals are matrixed to RGB signals by either a PAL/SECAM or NTSC matrix (selected via the I^2C-bus).
2. $(RGB)_1$ signals: 0.7 V (p-p) VB; capacitively coupled (e.g. from external source)
3. $(RGB)_2$ signals: 0.7 V (p-p) VB; capacitively coupled (e.g. video text and OSD).

All input signals are clamped in order to have the same black levels at the signal switch input. Displayed signals must be synchronous with the sandcastle pulse.

Signal switches

Both fast signal switches can be operated by switching pins (e.g. SCART facilities) or set via the I^2C-bus. With pin FSW_1 the luminance and colour difference signals or the $(RGB)_1$ signals can be selected and with pin FSW_2 the above selected signals or the $(RGB)_2$ signals are enabled. During the vertical and horizontal blanking time an artificial black level equal to the clamped black level is inserted in order to clip off the sync pulse of the luminance signal and to suppress hum during the cut-off measurement time and eliminate noise during these intervals.

Saturation, contrast and brightness

Saturation, contrast and brightness adjustments are controlled via the I^2C-bus and act on luminance and colour difference signals as well as on RGB input signals. Gamma acts on the luminance content of the input signals.

Gamma adjust stage

The gamma adjust stage has a non-linear transmission characteristic according to the formula $y = x^{gamma}$, where x represents the input and y the output signal. If gamma is smaller than unity, the lower parts of the signal are amplified with higher gain.

Adaptive black (ADBL)

The adaptive black stage detects the lowest voltage of the luminance component of the internal RGB signals during the scanning time and shifts it to the nominal black level. In order to keep the nominal white level the contrast is increased simultaneously.

Blue stretch (BLST)

The blue stretch channel gets additional amplification if the blue signal is greater than 80% of the nominal signal amplitude. In this event the white point is shifted towards higher colour temperature so that white parts of a picture seem to be brighter.

Measurement pulse and blanking stage

During the vertical and horizontal blanking time and the measurement period the signals are blanked to an ultra black level, so that the leakage current of the picture tube can be measured and automatically compensated for.

During the cut-off measurement lines (one line period for each R, G or B) the output signal levels are at cut-off measurement level.

The vertical blanking period is timed by the sandcastle pulse. The measurement pulses (leakage, R, G and B) are triggered by the negative going edge of the vertical pulse of the sandcastle pulse and start after the following horizontal pulse.

The IC is prepared for $2f_H$ (32 kHz) application.

Output amplifier and white adjust potentiometer

The RGB signals are amplified to nominal 2 V (p-p), the DC-levels are shifted according to cut-off control. The nominal signal amplitude can be varied by ±50% by the white point adjustment via the I^2C-bus (individually for RGB respectively).

Automatic cut-off control

During the leakage measurement time the leakage current is compensated in order to get a reference voltage at the cut-off measurement information pin. This compensation value is stored in an external capacitor. During cut-off current measurement times for the R, G and B channels, the voltage at this pin is compared with the reference voltage, which is individually adjustable via the I^2C-bus for each colour channel. The control voltages that are derived in this way are stored in the external feedback capacitors. Shift stages add these voltages to the corresponding output signals. The automatic cut-off control may be disabled via the I^2C-bus. In this mode the output voltage is clamped to 2.5 V. Clamping periods are the same as the cut-off measurement periods.

Signal limiting

The TDA4780 provides two kinds of signal limiting. First, an average beam limiting, that reduces the signal level if a certain average is exceeded. Second, a peak drive limiting, that is activated if one of the RGB signals even shortly exceeds a via the I^2C-bus adjusted threshold. The latter can be either referenced to the cut-off measurement level of the outputs or to ground.

When signal limiting occurs, the contrast is reduced, and at minimum contrast the brightness is reduced additionally.

Sandcastle decoder and timer

A 3-level detector separates the sandcastle pulse into combined line and field pulses, line pulses, and clamping pulses. The timer contains a line counter and controls the cut-off control measurement.

Application with a 2-level 5 V sandcastle pulse is possible.

Switch-on delay circuit

After switch-on all signals are blanked and a warm-up test pulse is fed to the outputs during the cut-off measurement lines. If the voltage at the cut-off measurement input exceeds an internal level the cut-off control is enabled but the signal remains still blanked. In the event of output clamping, the cut-off control is disabled and the switch-on procedure will be skipped.

Y output and hue adjust

The TDA4780 contains a digital-to-analog converter for hue adjust. The analog information can be fed, e.g. to the multistandard decoder TDA4650 or TDA4655. This output pin may be switched to a Y output signal, which can be used for scan velocity modulation. The Y output is the Y input signal or the matrixed (RGB) input signal according to the switch position of the fast switch.

I^2C-bus

The TDA4780 contains an I^2C-bus receiver for control functions.

ESD protection

The pins are provided with protection diodes to ground and supply voltage (see Chapter “Internal pin configuration”). I^2C-bus input pins do not shunt the I^2C-bus signals in the event of missing supply voltage.

EMC

The pins are protected against electromagnetic radiation.

I²C-BUS RECEIVER

Table 1 Slave address; note 1

A6	A5	A4	A3	A2	A1	A0	$\overline{W}$
1	0	0	0	1	0	0	0

Note

1. Explanation for the cell contents of the table:
   a) W means write.

Table 2 Slave receiver format (write mode; bit BREN = 0); see Figs 4 to 6; note 1

S	SLAVE ADDRESS	A	SUBADDRESS(2)	A	DATA BYTE n data bytes with auto-increment of subaddresses	A	P

Notes

1. Explanation for the cell contents of the table:
   a) S means START condition.
   b) P means STOP condition.
   c) A means acknowledge.
2. All subaddresses within the range 00H to 0FH are automatically incremented. The subaddress counter wraps around from 0FH to 00H. Only in this event 0FH will be acknowledged. Subaddresses outside the range 00H to 0EH are not acknowledged by the device and neither auto-increment nor any other internal operation takes place. All eight bits of the subaddress have to be decoded by the device.

Table 3 Slave receiver format (write mode; bit BREN = 1); see Figs 4 and 5; note 1

S	SLAVE ADDRESS	A	SUBADDRESS	A	DATA BYTE(2)	A	P

Notes

1. Explanation for the cell contents of the table:
   a) S means START condition.
   b) P means STOP condition.
   c) A means acknowledge.
2. Auto-increment is not possible.

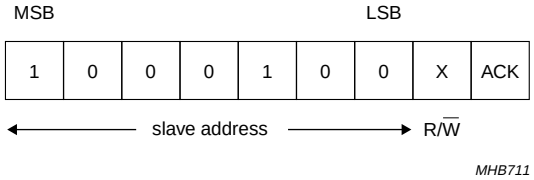
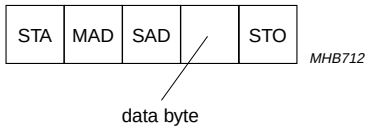


Fig.4 Slave address byte.



STA = START.
MAD = main address.
SAD = subaddress.
STO = STOP

Fig.5 Data transmission without auto-increment (bit BREN = 0 or 1).

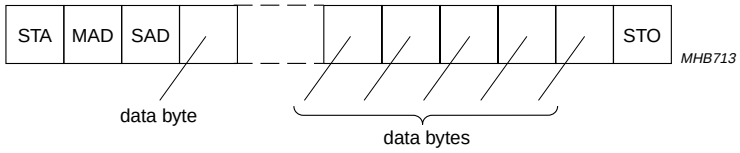


Fig.6 Data transmission with auto-increment (bit BREN = 0).

Table 4 Signal input selection and effect on adaptive black measurements by fast source switches and I²C-bus; note 1

I²C-BUS CONTROLLED BITS				ANALOG SWITCH		SELECTED SIGNALS			
FSON2	**FSDIS2**	**FSON1**	**FSDIS1**	**FSW2 (pin 1)**	**FSW1 (pin 13)**	**RGB_2 (pins 2, 3 and 4)**	**ADBL**	**RGB_1 (pins 10, 11 and 12)**	**TV (pins 6, 7 and 8)**
0	0	0	0	L	L	–	active	–	ON
				L	H	–	active	ON	–
				H	X	ON	inactive	–	–
0	0	0	1	L	X	–	active	–	ON
				H	X	ON	inactive	–	–
0	0	1	X	L	X	–	active	ON	–
				H	X	ON	inactive	–	–
0	1	0	0	X	L	–	active	–	ON
				X	H	–	active	ON	–
0	1	0	1	X	X	–	active	–	ON
0	1	1	X	X	X	–	active	ON	–
1	0	X	X	L	X	ON	active	–	–
				H	X	ON	inactive	–	–
1	1	X	X	X	X	ON	active	–	–

Note

1. Explanation for the cell contents of the table:
   a) H = analog switch (pins 1 and 13) to >0.9 V.
   b) L = analog switch (pins 1 and 13) to <0.4 V.
   c) X = don't care.
   d) ON = this signal is selected.

Table 5 Crosstalk

FSW1	FSW2	CROSSTALK	AT 4 MHz MAXIMUM VALUE (dB)	AT 8 MHz MAXIMUM VALUE (dB)	AT 13 MHz MAXIMUM VALUE (dB)
L	L	$(RGB)_1 \rightarrow$ Y and colour difference	–58	–55	–50
		$(RGB)_2 \rightarrow$ Y and colour difference	–58	–55	–50
L	H	Y and colour difference $\rightarrow (RGB)_1$	–51	–50	–47
		$(RGB)_2 \rightarrow (RGB)_1$	–58	–55	–50
L	H	Y and colour difference $\rightarrow (RGB)_2$	–51	–50	–47
		$(RGB)_1 \rightarrow (RGB)_2$	–58	–55	–50
H	H	Y and colour difference $\rightarrow (RGB)_2$	–51	–50	–47
		$(RGB)_1 \rightarrow (RGB)_2$	–58	–55	–50

Table 6 Subaddress byte and data byte format; notes 1 and 2

FUNCTION	SUBADDRESS	MSB			DATA BYTE				LSB
		D7	D6	D5	D4	D3	D2	D1	D0
Brightness	00H	0	0	A05	A04	A03	A02	A01	A00
Saturation	01H	0	0	A15	A14	A13	A12	A11	A10
Contrast	02H	0	0	A25	A24	A23	A22	A21	A20
Hue	03H	0	0	A35	A34	A33	A32	A31	A30
Red gain	04H	0	0	A45	A44	A43	A42	A41	A40
Green gain	05H	0	0	A55	A54	A53	A52	A51	A50
Blue gain	06H	0	0	A65	A64	A63	A62	A61	A60
Red level reference	07H	0	0	A75	A74	A73	A72	A71	A70
Green level reference	08H	0	0	A85	A84	A83	A82	A81	A80
Blue level reference	09H	0	0	A95	A94	A93	A92	A91	A90
Peak drive limit	0AH	0	0	AA5	AA4	AA3	AA2	AA1	AA0
Gamma	0BH	0	0	AB5	AB4	AB3	AB2	AB1	AB0
Control register 1	0CH	SC5	DELOF	BREN	X	NMEN	X	X	X
Control register 2	0DH	X	HDTV	FSBL	BCOF	FSDIS2	FSON2	FSDIS1	FSON1
Control register 3	0EH	ADBL	YHI	MOD2	BLST	YEXH	RELC	TCPL	0

Notes

1. Explanation for the cell contents of the table:
   a) X = don’t care, but for software compatibility with further video ICs with the same slave address, it is recommended to set all these bits to logic 0.
2. After Power-on reset all alignment registers are set to 01H.

Table 7 RGB processor mode bits control register

SYMBOL	PARAMETER	CONDITIONS
Control register 1		
SC5	sandcastle pulse 5 V	0 = 3-level sandcastle pulse
		1 = 2-level sandcastle pulse
DELOF	delay of leading edge of clamping pulse switched off	0 = delay
		1 = no delay
BREN	buffer register enable	0 = new data are executed just after reception
		1 = data is held in a latch (buffer register) and will be transferred to their destination register within the next vertical blanking interval; the device does not acknowledge any new data transfer until the internal transfer to the destination register has been completed
NMEN	NTSC matrix enable; note 1	0 = PAL matrix
		1 = NTSC matrix; hue position set on −2 degrees

SYMBOL	PARAMETER	CONDITIONS
Control register 2		
HDTV	HDTV or progressive scan for ADBL line counter	0 = 272 (PAL) or 224 (NTSC) lines
		1 = 544 (PAL) or 448 (NTSC) lines
FSBL	full screen black level, e.g. for optical measurement	0 = normal mode
		1 = cut-off measurement level during full field, brightness inactive
BCOF	internal black level control off	0 = automatic cut-off control active
		1 = RGB outputs clamped to fixed DC levels
FSDIS2	fast switch 2 disable	see Table 4
FSON2	fast switch 2 on	
FSDIS1	fast switch 1 disable	
FSON1	fast switch 1 on	
Control register 3		
ADBL	adaptive black	0 = off
		1 = on
YHI	Y high level	0 = input = 0.315 V (p-p) (black-white)
		1 = input = 1.0 V (p-p) (black-white)
MOD2	modus 2	0 = inactive; bit BCOF = 0 AND bit MOD2 = 1 is senseless (no output stabilization)
		1 = output clamp without brightness adjust; brightness remains active e.g. for blue stretch
BLST	blue stretch	0 = off
		1 = on
YEXH	Y exclusive hue	0 = pin 26 is switched to hue adjust output
		1 = pin 26 is switched to Y output
RELC	relative to cut-off	0 = peak drive limit to absolute output
		1 = peak drive limit relative to cut-off
TCPL	time constant peak drive limiter	0 = $2f_H$
		1 = $1f_H$

Note

1. Matrix coefficients should be tested by comparing RGB output signals with a reference RGB colour bar, which is fed in at $(RGB)_1$ or $(RGB)_2$ inputs. In the event of bit NMEN = 1 (NTSC) at minimum saturation the Y output and RGB output signals are not identical to the Y input signal.
   a) PAL/SECAM signals are matrixed by the equation: $V_{G-Y} = -0.51V_{R-Y} - 0.19V_{B-Y}$
   b) NTSC signals are matrixed by the equations (hue phase shift of –2 degrees):
      $V_{R-Y^*} = 1.39V_{R-Y} - 0.07V_{B-Y}$
      $V_{G-Y^*} = -0.46V_{R-Y} - 0.15V_{B-Y}$
      $V_{B-Y^*} = V_{B-Y}$
   c) For the demodulation axis see Fig.11.
   d) In the matrix equations: V_{R-Y} and V_{B-Y} are conventional PAL demodulation axes and amplitudes at the output of the demodulator and V_{R-Y^*}, V_{G-Y^*} and V_{B-Y^*} are the NTSC-modified colour-difference signals.

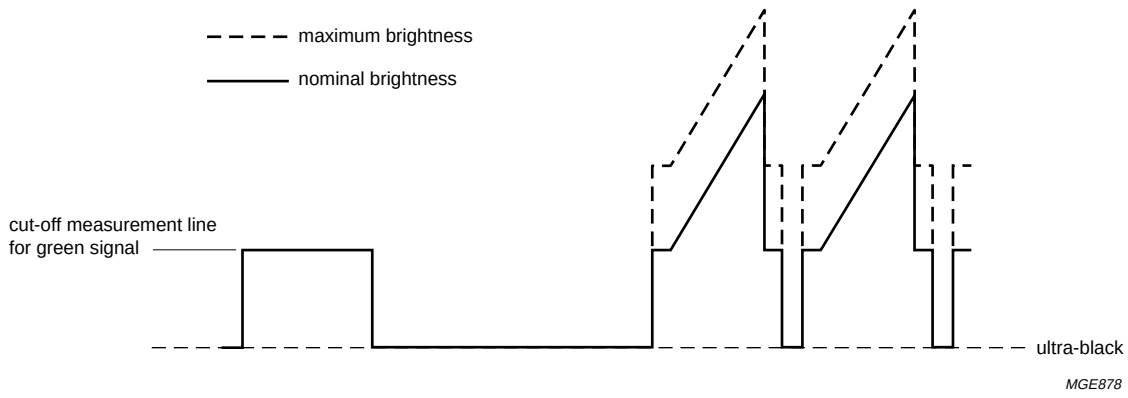


Fig.7 Cut-off measurement pulses.

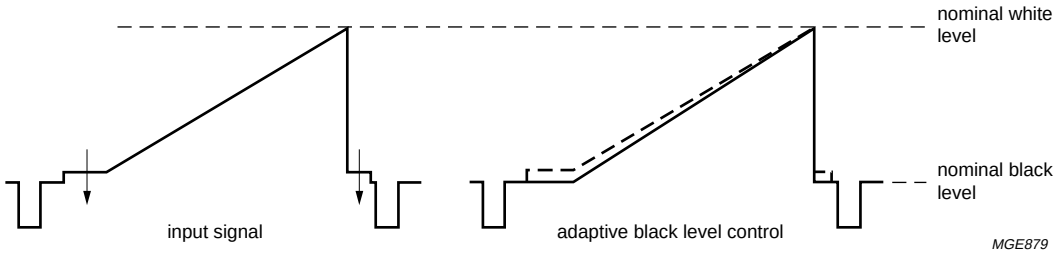


Fig.8 Principle of adaptive black control.

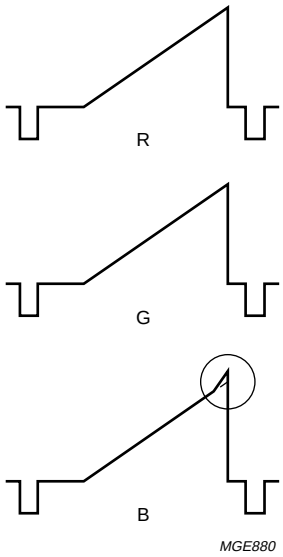
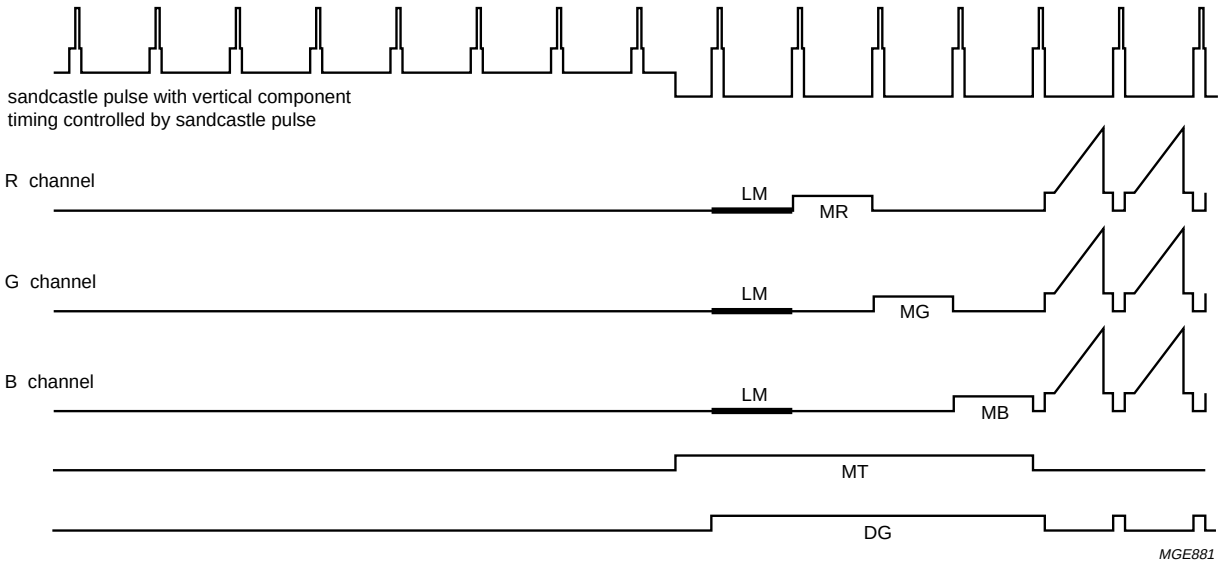


Fig.9 Principle of blue stretch.



LM = leakage current measurement time.
MR, MG, MB = R, G, B cut-off measurement pulses.
MT = measurement time.
DG = internal blanking.

Fig.10 Pulse diagram.

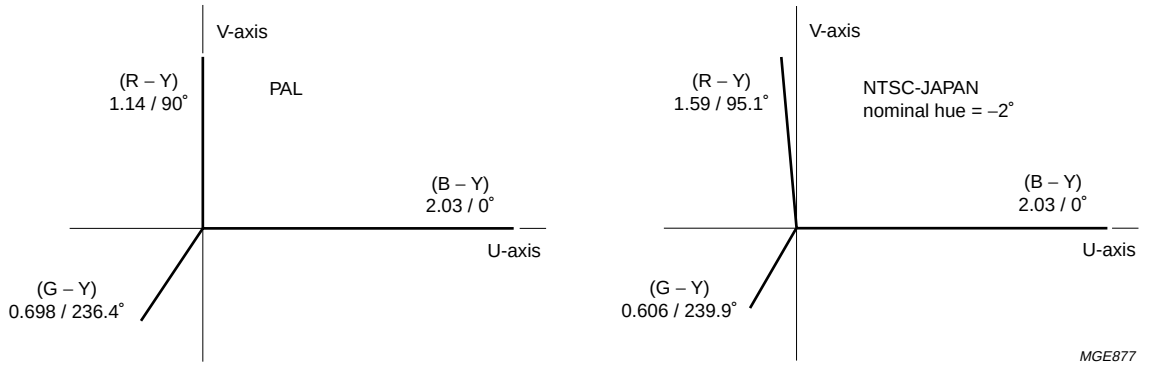


Fig.11 Demodulation axes.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_P	supply voltage		–0.1	+9.0	V
$V_{10,11,12}$	$(RGB)_1$ input voltage	with respect to GND	–0.1	V_P	V
$V_{2,3,4}$	$(RGB)_2$ input voltage	with respect to GND	–0.1	V_P	V
$V_{8,7,6}$	Y and colour difference input voltage	with respect to GND	–0.1	V_P	V
$V_{13,1}$	switch 1 and switch 2 input voltage	with respect to GND	–0.1	V_P	V
$V_{25,23,21,17}$	black level, leakage storage voltage	with respect to GND	–0.1	V_P	V
V_{14}	sandcastle voltage	with respect to GND	–0.7	V_P + 5.8	V
V_{15}	average current information voltage	with respect to GND	–0.7	V_P + 0.7	V
V_{16}	peak drive storage voltage	with respect to GND	–0.1	V_P	V
V_{18}	peak dark storage voltage	with respect to GND	–0.1	V_P	V
V_{19}	cut-off control input voltage	with respect to GND	–0.7	V_P + 0.7	V
$V_{27,28}$	I^2C-bus: SDA and SCL voltage	with respect to GND	–0.1	V_P	V
$I_{24,22,20}$	output peak current		–20	–	mA
$I_{24,22,20}$	output average current		–10	–	mA
I_{26}	Y output or hue adjust current		–8	–	mA
P_{tot}	total power dissipation		–	1200	mW
T_{amb}	ambient temperature		–20	+70	°C
T_{stg}	storage temperature		–20	+150	°C
V_{es}	electrostatic discharge voltage	note 1	–500	+500	V

Note

1. Charge device model class A: discharging a 200 pF capacitor through a 0 Ω series resistor.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	47	K/W

QUALITY SPECIFICATION

In accordance with URV-4-2-59/601. The number of the quality specification can be found in the *"Quality reference handbook"*. The handbook can be ordered using the code 9397.750.04888.

CHARACTERISTICS

V_P = 8 V; T_{amb} = 25 °C; V_{nom}: nominal signal amplitude (black-white) 2000 mV (p-p) at output pins; maximum gamma = 00H; adaptive black inactive; brightness, contrast, saturation and white balance at nominal settings; no beam current or peak drive limiting; all voltages are related to ground (pin 9) and measured in Fig.12; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_P	supply voltage (pin 5)		7.2	8.0	8.8	V
I_P	supply current (pin 5)		80	100	120	mA
Colour-difference inputs [–(B – Y): pin 6, –(R – Y): pin 7; capacitively coupled to a low-ohmic source; recommendation: maximum 600 Ω]						
$V_{6(p-p)}$	–(B – Y) input signal (peak-to-peak value)	75% colour bar signal	–	1.33	–	V
$V_{7(p-p)}$	–(R – Y) input signal (peak-to-peak value)	75% colour bar signal	–	1.05	–	V
$V_{6,7}$	internal bias voltage during clamping		–	4.0	–	V
$I_{6,7}$	DC input current between clamping pulses		–	–	0.1	µA
$I_{6,7(clamp)(max)}$	maximum input current during clamping		100	180	260	µA
$R_{6,7}$	AC input signal resistance		10.0	–	–	MΩ
Y input (pin 8; capacitively coupled to a low-ohmic source; recommendation: maximum 600 Ω)						
$V_{8(p-p)}$	input signal (composite signal; VBS; peak-to-peak value)	adaption to two signal levels:				
		bit YHI = 0	–	0.45	–	V
		bit YHI = 1	–	1.43	–	V
V_8	internal bias voltage during clamping	bit YHI = 0	–	3.7	–	V
		bit YHI = 1	–	4.6	–	V
I_8	DC input current between clamping pulses		–	–	0.1	µA
$I_{8(clamp)(max)}$	maximum input current during clamping		100	180	260	µA
R_8	AC input resistance		10.0	–	–	MΩ
RGB input 1 [pin 10 (R_1), pin 11 (G_1), pin 12 (B_1); capacitively coupled to a low-ohmic source; recommendation: maximum 600 Ω]; note 1						
$V_{10,11,12(p-p)}$	input signal (peak-to-peak value)		–	0.7	–	V
$V_{10,11,12}$	internal bias voltage during clamping		–	5.1	–	V
$I_{10,11,12}$	DC input current between clamping pulses		–	–	0.1	µA
$I_{10,11,12(clamp)(max)}$	maximum input current during clamping		100	180	260	µA
$R_{10,11,12}$	AC input resistance		10.0	–	–	MΩ

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
RGB input 2 [pin 2 (R_2), pin 3 (G_2), pin 4 (B_2); capacitively coupled to a low-ohmic source; recommendation: maximum 600 Ω]; note 1						
$V_{2,3,4(p\text{-}p)}$	input signal (peak-to-peak value)		–	0.7	–	V
$V_{2,3,4}$	internal bias voltage during clamping		–	5.1	–	V
$I_{2,3,4}$	DC input current between clamping pulses		–	–	0.1	µA
$I_{2,3,4(clamp)(max)}$	maximum input current during clamping		100	180	260	µA
$R_{2,3,4}$	AC input resistance		10.0	–	–	MΩ
Fast signal switches and blanking [fast signal switch 1 (pin 13); Y and colour difference or $(RGB)_1$; control bits FSDIS1 and FSON1]						
V_{13}	voltage to select Y and colour difference		–	0	0.4	V
V_{13}	voltage range to select $(RGB)_1$		0.9	1.0	5.5	V
R_{13}	internal resistance to ground		3.3	3.8	4.8	kΩ
CROSSTALK (SEE TABLE 5)						
$t_s - t_i$	difference between transit times for signal switching and signal insertion		–	–	10	ns
Fast signal switch 2 [pin 1; Y and colour difference or $(RGB)_1$ or $(RGB)_2$; control bits FSDIS2 and FSON2]						
V_1	voltage to select Y and colour difference or $(RGB)_1$		–	0	0.4	V
V_1	voltage range to select $(RGB)_2$		0.9	1.0	5.5	V
V_1	required minimal voltage to switch off the ADBL measurement		–	0.87	1.0	V
R_1	internal resistance to ground	$R_1 > R_{13}$	2.8	4.2	6.0	kΩ
CROSSTALK (SEE TABLE 5)						
$t_s - t_i$	difference between transit times for signal switching and signal insertion		–	–	10	ns
Adjust stages (adaptive black, gamma, contrast, saturation, brightness and white point adjust, blue stretch)						
ADAPTIVE BLACK [DETECTORS INACTIVE STATUS DUE TO ACTION OF FAST SWITCH 2 (PIN 1); see Table 4; see Fig.8; note 2]						
$I_{18(dch)}$	discharge current of peak dark storage capacitor	outside active measurement window	–1.0	0.0	+1.0	µA
		inside active measurement window	1.5	2.5	3.5	µA
$I_{18(ch)}$	charge current of peak dark storage capacitor		–360	–300	–250	µA
$d_{bl(max)}$	maximum level shift: Δ black level in percent of nominal signal amplitude		10	13	16	%
$d_{bl(nom)}$	difference between nominal black and adaptive black in percent of nominal signal amplitude		–3	0	+3	%

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
t_{dibb}	detectors inactive time before blanking		2.3	3.1	4.0	µs
t_{diab}	detectors inactive time after blanking		2.3	2.5	3.4	µs
GAMMA ADJUST [ACTS ON INTERNAL Y SIGNAL; Y MATRIX SEE Y OUTPUT; I²C-BUS CONTROLLED POTENTIOMETER (SUBADDRESS 0BH); RESOLUTION 6 BIT; note 3]						
d_g	range of gamma					
	minimum (3FH)		–	0.7	–	
	maximum (00H)		–	1.0	–	
G_{max}	maximum gain at minimum gamma	near nominal black	5	6	7	dB
SATURATION ADJUST [ACTS ON RGB SIGNALS; Y MATRIX SEE Y OUTPUT; I²C-BUS CONTROLLED POTENTIOMETERS (SUBADDRESS 01H); RESOLUTION 1.5% OF MAXIMUM SATURATION]						
$d_{s(max)}$	maximum saturation	I²C-bus data 3FH; measured at 100 kHz; relative to nominal saturation; note 4	4.7	5.2	5.8	dB
$d_{s(min)}$	minimum saturation	I²C-bus data 00H; measured at 100 kHz; relative to typical value of maximum saturation	–	–	–50	dB
CONTRAST ADJUST [ACTS ON RGB SIGNALS; I²C-BUS CONTROLLED POTENTIOMETERS (SUBADDRESS 02H); RESOLUTION 1.5% OF MAXIMUM CONTRAST]						
$d_{c(max)}$	maximum contrast	I²C-bus data 3FH; limiters inactive; relative to nominal contrast; note 5	–	4.5	5.5	dB
$d_{c(min)}$	minimum contrast	I²C-bus data 00H; relative to maximum contrast	–28	–22	–16	dB
BRIGHTNESS ADJUST [ACTS ON RGB SIGNALS; I²C-BUS CONTROLLED POTENTIOMETERS (SUBADDRESS 00H); RESOLUTION 1.5% OF RANGE; Δ BLACK LEVEL IN PERCENT OF NOMINAL SIGNAL AMPLITUDE REFERRED TO CUT-OFF MEASURING LEVEL]						
$d_{br(max)}$	maximum brightness: Δ black level	I²C-bus data 3FH				
		normal	23	30	37	%
		control bits BCOF = 1 and MOD2 = 0	23	30	37	%
$d_{br(nom)}$	nominal brightness: Δ black level	I²C-bus data 29H	–7	0	+7	%
$d_{br(min)}$	minimum brightness: Δ black level	I²C-bus data 00H				
		normal	–58	–50	–42	%
		control bits BCOF = 1 and MOD2 = 0	–58	–50	–42	%
BLUE STRETCH (BLUE STRETCH IS ACTIVATED BY I²C-BUS CONTROL BIT BLST = 1; see Fig.9)						
G_{bs}	increase of small signal gain	100% of nominal signal amplitude and at 1 MHz	15	20	25	%

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
DIFFERENCES OF BLACK LEVEL STEPS [DIFFERENCES FROM CHANNEL TO CHANNEL OF THE RATIO OF THE DIFFERENCE (BLACK LEVEL CUT-OFF MEASUREMENT LEVEL) TO ACTUAL NOMINAL SIGNAL AMPLITUDE $V_{24(nom)}$, $V_{22(nom)}$ AND $V_{20(nom)}$ OVER THE WHOLE CONTRAST, BRIGHTNESS AND SATURATION RANGE, SWITCHING MATRIX OR SWITCHING FAST SWITCHES, MAXIMUM GAMMA = 00H, BIT BLST = 0 AND BIT ADBL = 0]						
$\Delta V/V_{nom}$	static deviation	ripple on pin 5 during clamping ≤1 mV; notes 6 and 7	–1.0	–	+1.0	%
		at nominal saturation	–0.5	–	+0.5	%
RGB outputs [output for positive RGB signals; pin 24 (R), pin 22 (G), pin 20 (B); following data without external load]						
$R_{24,22,20}$	differential output resistance		–	25	30	Ω
$I_{24,22,20(max)}$	maximum output current		4.0	5.0	–	mA
$V_{24,22,20(min)}$	minimum output voltage	note 8	–	–	0.8	V
$V_{24,22,20(max)}$	maximum output voltage	$R_L \geq 2$ kΩ	6.3	7.0	–	V
$V_{24,22,20(max)(p-p)}$	maximum signal amplitude (black-white) due to internal limits (peak-to-peak value)		3.3	–	–	V
$V_{24,22,20(nom)}$	nominal signal amplitude (black-white)	at nominal white adjust, contrast and saturation setting; maximum gamma = 00H; nominal input signals	1.7	2.0	2.3	V
$V_{24,22,20}$	cut-off measurement level	note 8	1.0	–	5.0	V
$V_{24,22,20}$	recommended cut-off measurement level		–	3.0	–	V
OUTPUT CLAMPING (RGB)						
$V_{24,22,20}$	clamp voltage black level	control bit BCOF = 1	2.3	2.5	2.7	V
WHITE POTENTIOMETERS						
$\Delta G_{v(inc)(max)}$	maximum increase of AC gain	I^2C-bus data 3FH; relative to nominal setting; note 9	40	50	60	%
$\Delta G_{v(dec)(max)}$	maximum decrease of AC gain	I^2C-bus data 00H; relative to nominal setting; note 9	40	50	60	%

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
OVERALL WHITE POINT DEVIATION						
$\Delta V/V_{nom}$	white point deviation	input: $(RGB)_{1,2}$; differences from channel to channel of the ratio of the difference (signal white level cut-off measurement level) to actual nominal signal amplitude [$V_{24(nom)}$, $V_{22(nom)}$ and $V_{20(nom)}$] over the whole saturation range at nominal contrast, brightness and nominal input signals; ripple on pin 5 during clamping ≤1 mV; notes 6 and 7	–2.0	–	+2.0	%
Frequency behaviour						
BETWEEN THE Y INPUT (PIN 8) AND THE RGB OUTPUTS (PINS 24, 22 AND 20)						
ΔG	decrease in gain	R_L = 1 MΩ; C_L = 20 pF; f = 13 MHz	–	–	3	dB
BETWEEN THE COLOUR-DIFFERENCE INPUTS (PINS 7 AND 6) AND THE CORRESPONDING R AND B OUTPUTS (PINS 24 AND 20)						
ΔG	decrease in gain	f = 13 MHz	–	–	3	dB
BETWEEN THE $(RGB)_{1,2}$ INPUTS (PINS 10, 11 AND 12 OR 2, 3 AND 4) AND THE RGB OUTPUTS (PINS 24, 22 AND 20)						
ΔG	decrease in gain	f = 22 MHz	–	–	3	dB
Sandcastle input (pin 14; control bit SC5); note 10						
I_{14}	input current	V_{14} < 0.5 V	–100	–	–	µA
C_{14}	input capacitance	referenced to ground	–	–	10	pF
V_{14}	required voltage range					
	for horizontal and vertical blanking pulses	bit SC5 = 0 or bit SC5 = 1	2.0	2.5	3.0	V
	for horizontal pulses (line count)	bit SC5 = 0	4.0	4.5	4.9	V
	for burst key pulses	bit SC5 = 0	6.1	–	V_P + 5.8	V
	for burst key pulses and line count	bit SC5 = 1	4.0	–	V_P + 5.8	V
CLAMP PULSE DELAY						
$t_{d(clamp)}$	delay of leading edge of clamping pulse	nominal sandcastle pulse				
		bit DELOF = 0	1.2	1.5	1.8	µs
		bit DELOF = 1	–	0	–	µs
REQUIRED MINIMAL BURST GATE PULSE WIDTH						
t_W	pulse width	bit DELOF = 0; line frequency is 16 kHz	3	–	–	µs
		bit DELOF = 1; line frequency is 32 kHz	1.5	–	–	µs

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Generation of measurement lines and blanking; note 11						
$\Delta V/V_{nom}$	difference between ultra black level (VUB) and measurement level (VCL) in percent of nominal signal amplitude	ΔV = VCL – VUB; no clipping; independent of white point adjust	25	35	45	%
WARM-UP TEST PULSE DURING TIME MT (see Fig.10)						
V_{WU}	warm-up level	$V_{WU} = V_{PL} - 1$ V; V_{PL} = peak drive level (see also signal limiting) given by the I^2C-bus subaddress 0AH; no warm-up test pulse in the event of output clamping (bit BCOF = 1)	–	–	–	
$V_{WU(max)}$	maximum warm-up level	I^2C-bus data 3FH; bit RELC = 0	6.3	6.6	6.9	V
$V_{WU(fixed)}$	fixed warm-up level	bit RELC = 1	5.0	5.2	5.4	V
THRESHOLD FOR POWER-ON RESET (POR) DURING TIME DG (see Fig.10)						
$V_{20,22,24(POR)}$	output voltage to cause POR	bit RELC = 0	–	V_{PL}	–	V
		bit RELC = 1	–	5.7	–	V
Y output (pin 26); note 12						
$V_{26(nom)(p-p)}$	nominal signal amplitude (black-white; independent of gamma, adaptive black, saturation, contrast and brightness; peak-to-peak value)	bit YEXH = 1; hue DAC (subaddress 03H) set to >28H	0.85	1.0	1.15	V
V_{26}	black level	bit YEXH = 1; I^2C-bus data 3FH	–	4.0	–	V
		bit YEXH = 1; I^2C-bus data 20H	–	2.0	–	V
a_r	Y matrix coefficients	$Y = a_rR + a_gG + a_bB$	0.27	0.30	0.33	
a_g	Y matrix coefficients	$Y = a_rR + a_gG + a_bB$	0.53	0.59	0.65	
a_b	Y matrix coefficients	$Y = a_rR + a_gG + a_bB$	0.10	0.11	0.12	
R_{26}	differential output resistance		–	190	230	Ω
$\Delta\tau_{26}$	group delay time	between RGB outputs and Y output	20	25	30	ns
f_g	3 dB bandwidth		11	15	–	MHz
Automatic cut-off control (pin 19; measurement periods see beam information on pin 19)						
V_{19}	permissible voltage (also during scanning period)		–	–	$V_P - 1.4$	V
V_{REF0}	internally controlled voltage on pin 19	during leakage measurement time LM	2.4	2.7	3.0	V
$I_{19(max)}$	maximum output current		–350	–	–250	μA
$I_{19(max)}$	maximum input current		250	–	350	μA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
R_{19}	input resistance for measurement input		1	–	–	MΩ
I_{19}	additional input current	only during warm-up	–	0.5	–	mA
V_{19}	threshold of warm-up detector	active in line MG	4.3	4.5	4.7	V
V_{MEAS}	difference between input voltage for cut-off and V_{REF0}	adjustable via the I^2C-bus (subaddresses for reference R: 07H, G: 08H and B: 09H)				
	maximum V_{MEAS}	I^2C-bus data 3FH	1.45	1.6	1.75	V
	nominal V_{MEAS}	I^2C-bus data 20H	0.9	1.0	1.1	V
	minimum V_{MEAS}	I^2C-bus data 00H	0.4	0.45	0.5	V
Storage of cut-off control voltage/output clamping voltage (pins 25, 23 and 21)						
$I_{25,23,21}$	input current of storage input outside of the measurement time		–	–	0.1	µA
$\lvert I_{25,23,21(max)} \rvert$	maximum charge/discharge current during measurement time		0.2	0.3	0.4	mA
G_{stg}	gain from storage pins 25, 23 and 21 to outputs		–	1.7	–	
Storage of leakage information (pin 17)						
I_{17}	maximum charge/discharge current at time LM		300	400	–	µA
I_{17}	discharge current	peak limiting during time MK active	–	4	–	mA
I_{17}	leakage current	outside time LM	–	–	0.1	µA
V_{17}	voltage to reset the IC to switch-on conditions		–	–	2.3	V
V_{17}	voltage to avoid reset		3.0	–	–	V
Signal limiting (the limitation acts on contrast and at low contrast on brightness)						
AVERAGE BEAM CURRENT LIMITING (PIN 15)						
V_{15}	start of contrast reduction		–	4	–	V
ΔV_{15}	input range for full contrast reduction		–	–2	–	V
V_{15}	start of brightness reduction		–	2.5	–	V
ΔV_{15}	input range for full brightness reduction		–	–1.6	–	V
I_{15}	input current		–	–	–0.5	µA
PEAK SIGNAL LIMITING OF OUTPUT SIGNALS [PIN 16; THE LIMITATION ACTS 1H DELAYED; LIMITING LEVEL ADJUSTABLE BY I^2C-BUS (SUBADDRESS 0AH0; CONTROL BIT RELC = 0]						
$V_{24,22,20(max)}$	maximum limiting level	extrapolated from 2FH	6.8	–	7.2	V
$V_{24,22,20(min)}$	minimum limiting level	I^2C-bus data 00H	–	2.3	3	V
$I_{16(max)}$	maximum discharge current at peak drive	bit RELC = 0	4	–	6	mA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
PEAK SIGNAL LIMITING [PIN 16; LIMITING LEVEL (V_{LiL}) ADJUSTABLE BY I^2C-BUS (SUBADDRESS 0AH); CONTROL BIT RELC = 1]						
V_{LiL}	limiting level	equal gain in white point adjust; signal only in one output channel; peak drive limiting starts, if the maximum of the RGB signals after white point adjustment exceeds a threshold				
	maximum level	I^2C-bus data 3FH	3.2	3.5	4.0	V
	minimum level	I^2C-bus data 00H	1.2	1.5	1.8	V
DISCHARGE CURRENTS (CUT-OFF MEASUREMENT LEVEL MX = MR OR MB OR MG)						
$I_{16(dch)(tot)}$	total discharge current	$I_{16} = I_{16(1)} + I_{16(2)} + I_{16(3)}$	–	–	–	
Threshold 1 (TH1)						
$I_{16(1)(dch)(max)}$	maximum discharge current	TH1 = MX + V_{LiL}; 1 line delayed and low-pass filtered	4.5	6	7.5	mA
S	steepness		–	15	–	mA/V
Low-pass filter, control bit TCPL						
t_{DPDL}	time constant low-pass filter	bit RELC = 1				
		at $1f_H$ (bit TCPL = 1)	0.9	1.2	1.5	µs
		at $2f_H$ (bit TCPL = 0)	0.4	0.6	0.8	µs
Threshold 2 (TH2)						
$I_{16(2)(dch)(max)}$	maximum discharge current	TH2 = MX + 1.10V_{LiL}; 1 line delayed	4.5	6	7.5	mA
S	steepness		–	15	–	mA/V
Threshold 3 (TH3)						
$I_{16(3)(dch)(max)}$	maximum discharge current	TH3 = MX + V_{LiL}; undelayed	0.45	0.6	0.75	mA
S	steepness		–	1.5	–	mA/V
CHARGE CURRENT						
I_{16}	charge current		–2	–1	–0.5	µA
V_{16}	start of contrast reduction		–	4	–	V
ΔV_{16}	input range for full contrast reduction		–	–2	–	V
V_{16}	start of brightness reduction		–	2.5	–	V
ΔV_{16}	input range for full brightness reduction		–	–1.6	–	V
$V_{16(max)}$	maximum voltage by internal limitation		4.5	–	–	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Hue adjust output (pin 26); note 13						
$V_{26(min)}$	minimum output voltage	bit YEXH = 0; I^2C-bus data 00H	0.5	–	1.0	V
$V_{26(nom)}$	nominal output voltage	bit YEXH = 0; I^2C-bus data 20H	3.0	3.2	3.4	V
$V_{26(max)}$	maximum output voltage	bit YEXH = 0; I^2C-bus data 3FH	4.8	–	5.6	V
I_{26}	current of internal emitter follower		500	700	–	µA
I^2C-bus						
INPUTS						
f_{28}	clock frequency range		0	–	100	kHz
$t_{SU;DAT}$	data set-up time		250	–	–	ns
t_H	clock pulse HIGH		4	–	–	µs
t_L	clock pulse LOW		4.7	–	–	µs
t_r	rise time		–	–	1	µs
t_f	fall time		–	–	0.3	µs
INPUT LEVELS (PINS 27 AND 28)						
V_{IL}	LOW-level input voltage		–	–	1.5	V
V_{IH}	HIGH-level input voltage		3.0	–	5.5	V
I_I	input current	V_{27} = 0.4 V; V_{28} = 0.4 V	–10	–	–	µA
		$V_{27} = 0.9V_P$; $V_{28} = 0.9V_P$	–	–	10	µA
OUTPUT LEVEL (PIN 27)						
V_{OL}	LOW-level output voltage		–	–	0.4	V
I_O	output current	V_{27} = 0.4 V	3.0	–	–	mA

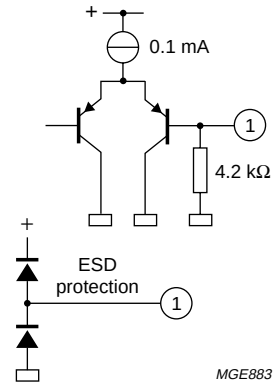
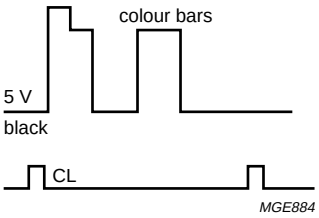
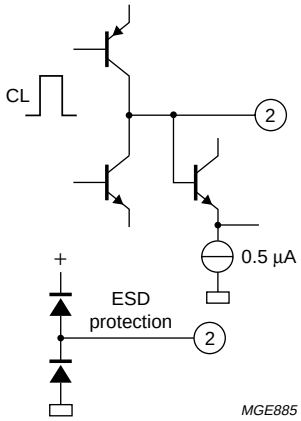
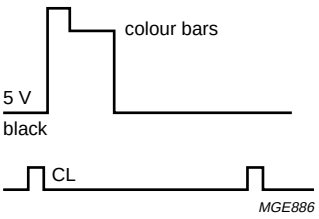
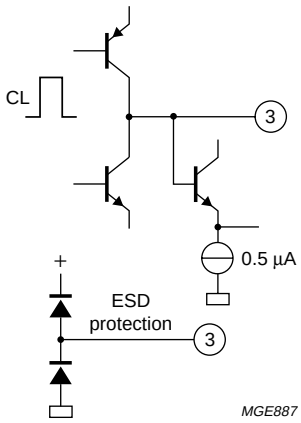
Notes

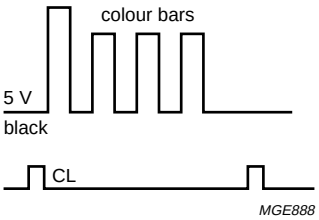
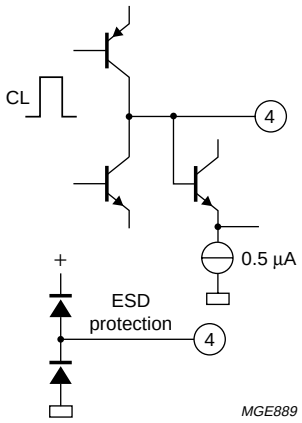
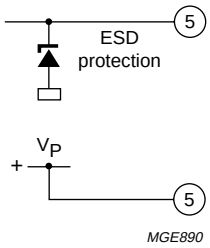
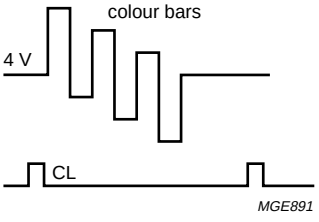
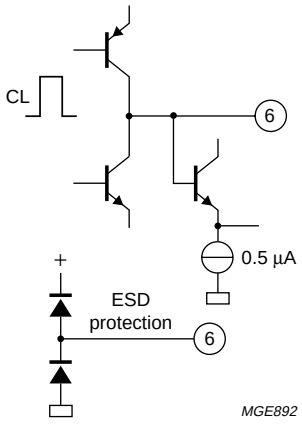
1. RGB signals controlled by saturation, adaptive black, contrast and brightness. Gamma affects the Y component of the internal RGB signals.
2. Adaptive black control acts on Y signal, which is either Y input or Y output from the RGB matrix. Negative set-up is not affected. The level shift value is determined by the peak dark detector, operation selected by the control bit ADBL. The peak dark detector is inactive during blanking. Peak dark detector activated by internal line counter, which starts after the end of the vertical blank of the sandcastle. Active from line 16 (after end of vertical sandcastle) to line 224 (NTSC mode, bit NMEN = 1) or line 272 (PAL mode, bit NMEN = 0). It is recommended to increase the contrast value (subaddress 02H) by 15% if bit ADBL = 1. The line numbers are doubled if bit HDTV = 1.
3. At minimum gamma (3FH) any differences in black level steps are amplified by 6 dB.
4. For nominal saturation the range of values is:
   a) 1FH is the minimum value that can be used
   b) 20H is the typical value that can be used
   c) 21H is the maximum value that can be used.

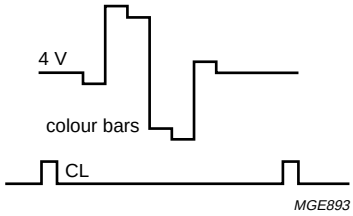
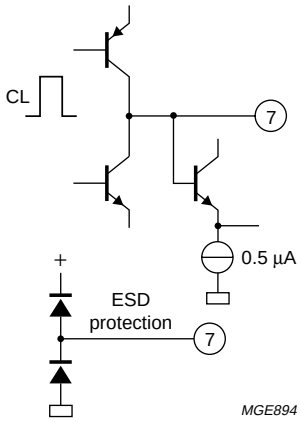
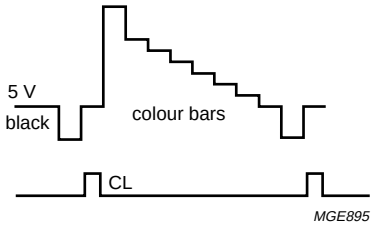
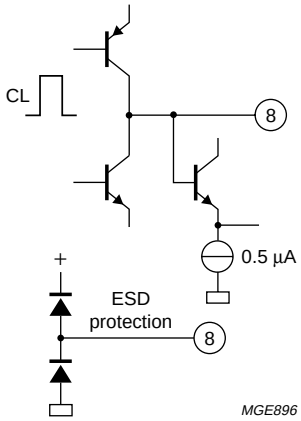
5. For nominal contrast the range of values is:
   a) 20H is the minimum value that can be used
   b) 22H is the typical value that can be used
   c) 24H is the maximum value that can be used.
6. $\frac{\Delta V}{V_{nom}} = \frac{\Delta V_{24}}{V_{24(nom)}} - \frac{\Delta V_{22}}{V_{22(nom)}} = \frac{\Delta V_{24}}{V_{24(nom)}} - \frac{\Delta V_{20}}{V_{20(nom)}} = \frac{\Delta V_{22}}{V_{22(nom)}} - \frac{\Delta V_{20}}{V_{20(nom)}}$ For meaning of actual nominal signal see chapter “Characteristics”.
7. Series resistance in supply voltage line should be less than 0.3 Ω.
8. At 1.0 V cut-off measurement level the function of the cut-off control loop is not guaranteed because the blanking level is limited to the minimum output voltage. For proper working a guide number for the minimum cut-off measurement level is 1.3 V (see also Fig.7).
9. For nominal AC gain settings the range of values is:
   a) 21H is the minimum value that can be used
   b) 22H is the typical value that can be used
   c) 23H is the maximum value that can be used.
10. The sandcastle pulse is compared with 3 internal threshold levels (bit SC5 = 0) or 2 internal threshold levels (bit SC5 = 1) to separate the various pulses. The internal pulses are generated while the input is higher than the thresholds. The thresholds are independent of supply voltage and temperature.
11. Blanking to ultra black level occurs during time DG except time MR in R-channel, time MG in G-channel and time MB in B-channel (see Fig.10).
    a) Leakage current measuring time: time LM will start after the end of vertical sandcastle.
    b) Vertical blanking period and cut-off measurement lines. The vertical component will be identified if it contains 2 or more burst key pulses in the event of bit SC5 = 1 or two or more line pulses (H) in the event of bit SC5 = 0. The line counter is triggered by the leading edge. The blanking time is valid for a vertical pulse detected by the sandcastle decoder. The internal blank pulse is OR gated with the sandcastle vertical pulse and the end of the measurement pulses.
    c) Insertion time: full line period.
    d) Measurement time: line period minus horizontal period (50 or 60 Hz).
    e) Line sequence of measuring lines. First line after end of horizontal pulse which followed the end of vertical pulse: leakage measurement LM. First line after leakage measurement pulse: red measurement MR. Second line after leakage measurement pulse: green measurement MG. Third line after leakage measurement pulse: blue measurement MB.
12. Y output can be switched to hue adjust output via the I^2C-bus control bit YEXH. Output without sync pulse. Recommendation: hue adjust DAC set to 3FH. Black level adjustable via hue adjust DAC.
13. Output can be switched to Y output via the I^2C-bus control bit YEXH (via the I^2C-bus, resolution 6-bit, bus subaddress 03H).

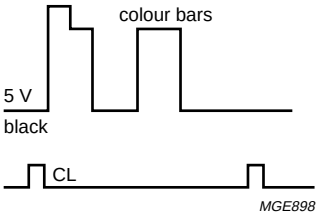
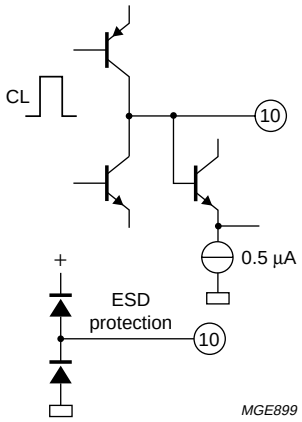
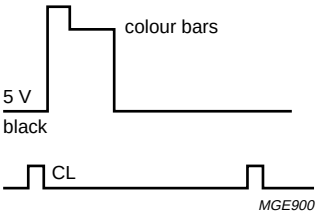
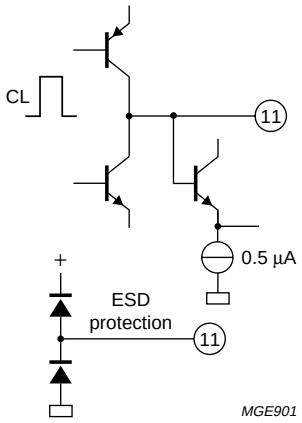
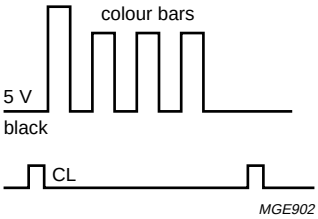
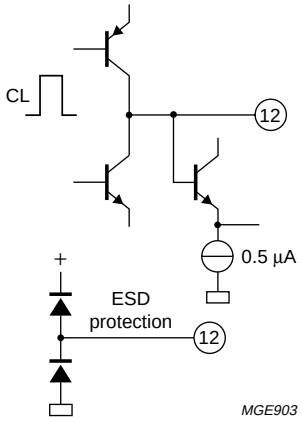
INTERNAL PIN CONFIGURATION

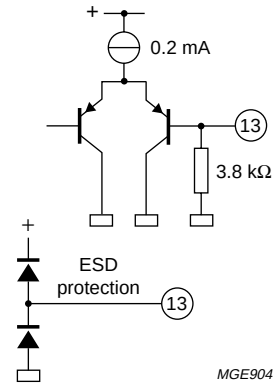
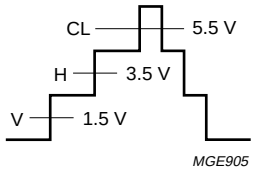
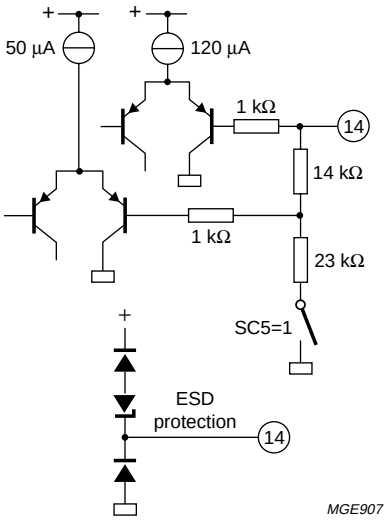
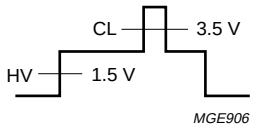
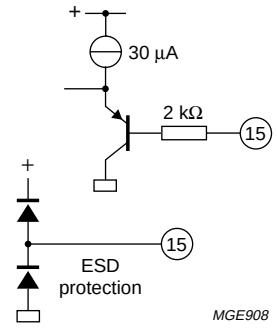
Used abbreviations: OB = open base and CL = clamp pulse.

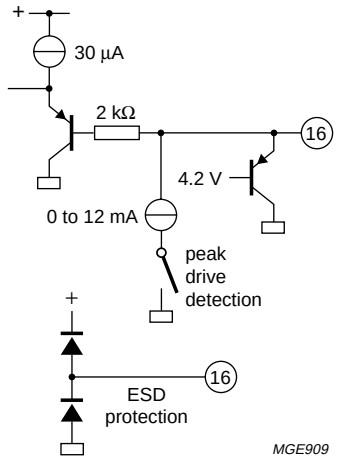
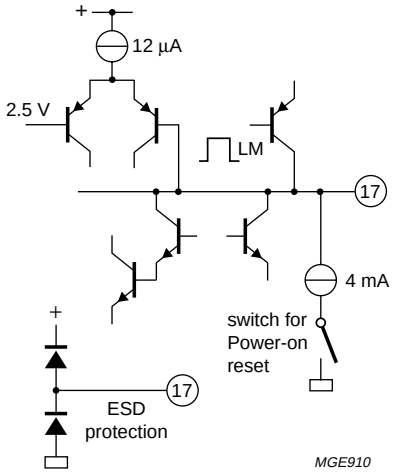
PIN	DESCRIPTION	WAVEFORM	I or Z	INTERNAL CIRCUIT
1	fast switch 2 input			
2	red input 2		100 µA/OB	
3	green input 2		100 µA/OB	

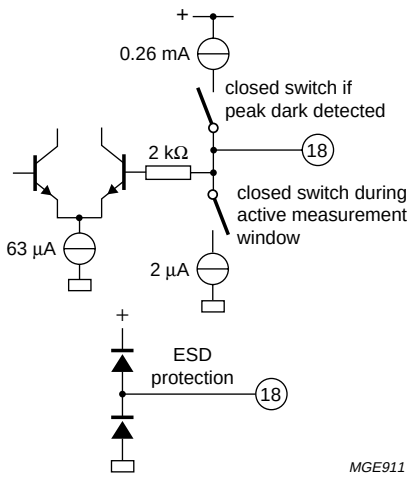
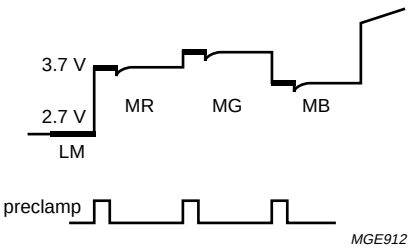
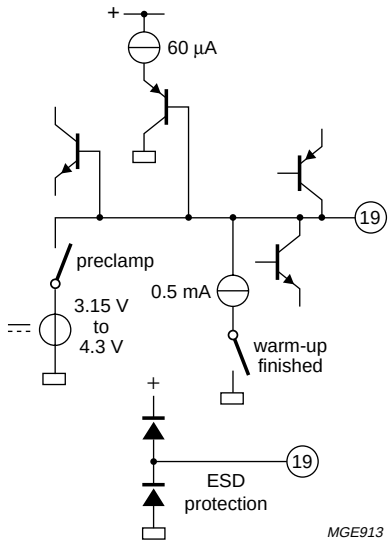
PIN	DESCRIPTION	WAVEFORM	I or Z	INTERNAL CIRCUIT
4	blue input 2		100 µA/OB	
5	supply voltage			
6	colour difference input −(B − Y)		100 µA/OB	

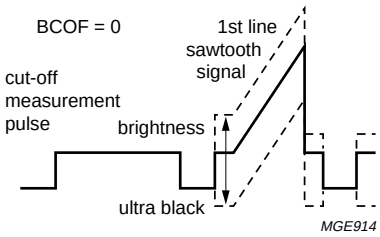
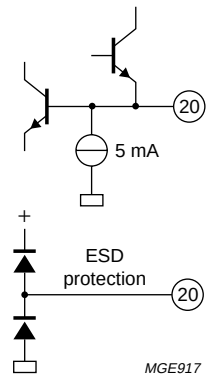
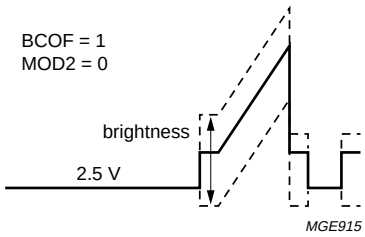
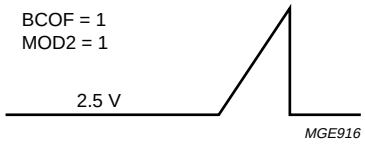
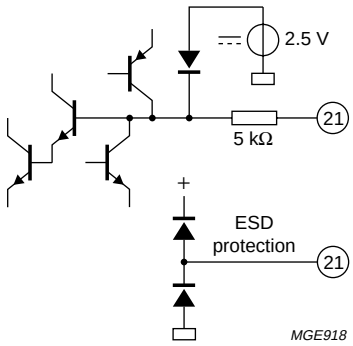
PIN	DESCRIPTION	WAVEFORM	I or Z	INTERNAL CIRCUIT
7	colour difference input –(R – Y)		100 μA/OB	
8	luminance input		100 μA/OB	
9	ground			 no ESD protection circuit for ground pin

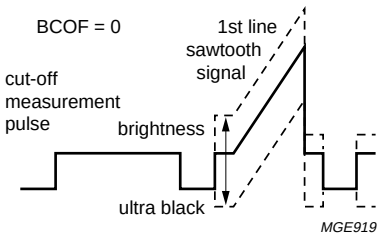
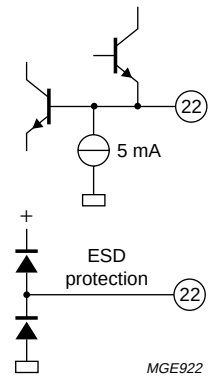
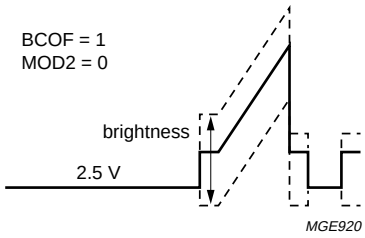
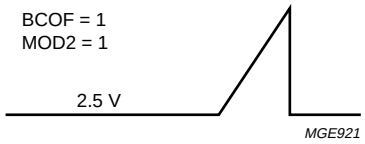
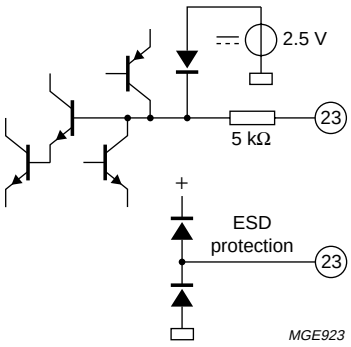
PIN	DESCRIPTION	WAVEFORM	I or Z	INTERNAL CIRCUIT
10	red input 1		100 µA/OB	
11	green input 1		100 µA/OB	
12	blue input 1		100 µA/OB	

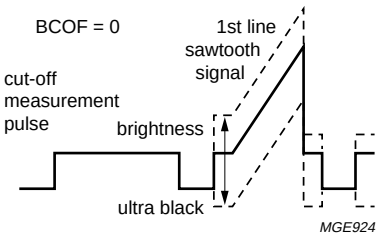
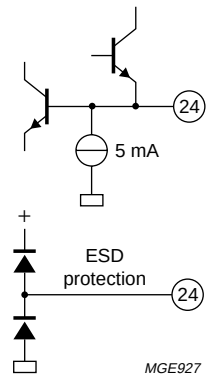
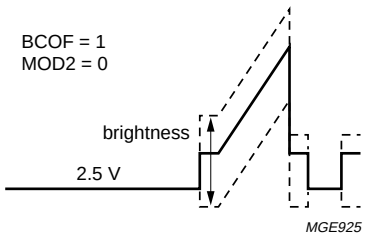
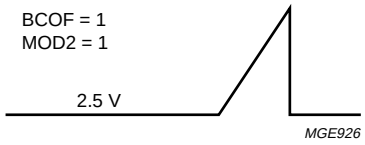
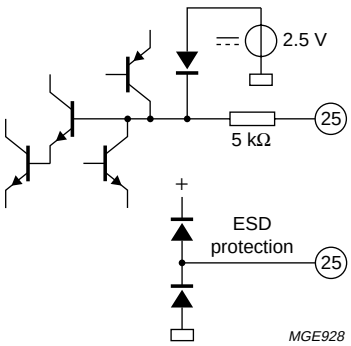
PIN	DESCRIPTION	WAVEFORM	I or Z	INTERNAL CIRCUIT
13	fast switch 1 input			
14	sandcastle pulse input	3-level sandcastle 	37 kΩ (bit SC5 = 0)	
		2-level sandcastle 	OB (bit SC5 = 1)	
15	average beam current limiting input		OB	

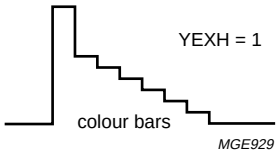
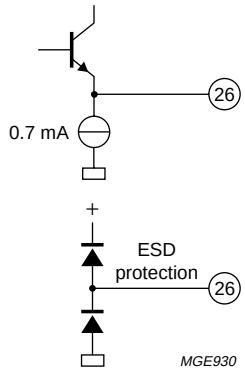
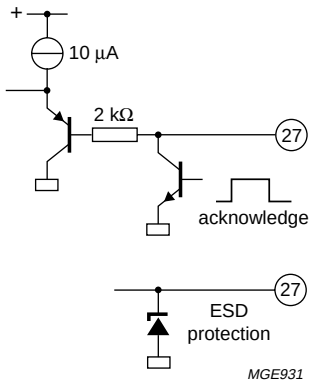
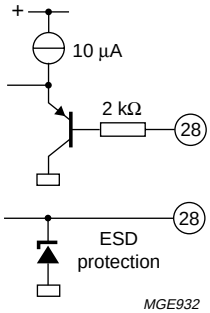
PIN	DESCRIPTION	WAVEFORM	I or Z	INTERNAL CIRCUIT
16	storage capacitor for peak limiting	outside peak drive	OB	
		during peak drive (bit RELC = 1)	0 to 12 mA	
		during peak drive (bit RELC = 0)	5 mA	
17	storage capacitor for leakage current compensation	outside leakage current measurement	OB	
		during leakage current measurement	–400 µA to +400 µA	
		automatic switch to Power-on reset	4 mA	

PIN	DESCRIPTION	WAVEFORM	I or Z	INTERNAL CIRCUIT
18	storage capacitor for peak dark		0.26 mA/OB	
19	cut-off measurement input		−300 µA to +300 µA	

PIN	DESCRIPTION	WAVEFORM	I or Z	INTERNAL CIRCUIT
20	blue output		5 mA	
			5 mA	
			5 mA	
21	blue cut-off storage capacitor	during cut-off control or during output clamping	OB −300 µA to +300 µA	

PIN	DESCRIPTION	WAVEFORM	I or Z	INTERNAL CIRCUIT
22	green output		5 mA	
			5 mA	
			5 mA	
23	green cut-off storage capacitor	during cut-off control or during output clamping	OB −300 µA to +300 µA	

PIN	DESCRIPTION	WAVEFORM	I or Z	INTERNAL CIRCUIT
24	red output		5 mA	
			5 mA	
			5 mA	
25	red cut-off storage capacitor	during cut-off control or during output clamping	OB –300 µA to +300 µA	

PIN	DESCRIPTION	WAVEFORM	I or Z	INTERNAL CIRCUIT
26	Y output or hue adjust output	 bit YEXH = 0; DC 0.8 V to 5.0 V	0.7 mA 0.7 mA	
27	I^2C-bus serial data input/acknowledge output	outside acknowledge during acknowledge	OB less than 0.1 V up to 4 mA due to external pull-up resistor	
28	I^2C-bus serial clock input		OB	

APPLICATION INFORMATION

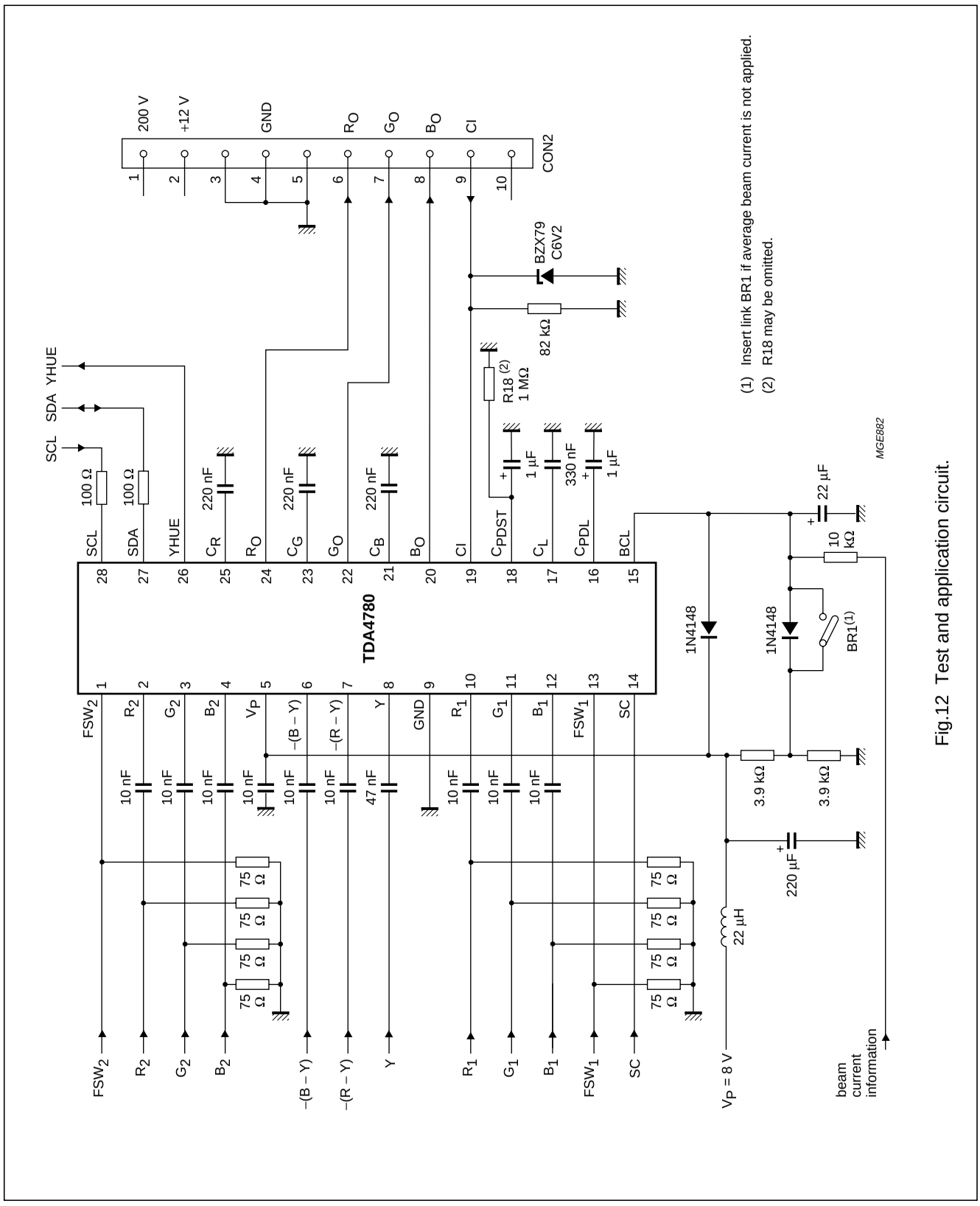
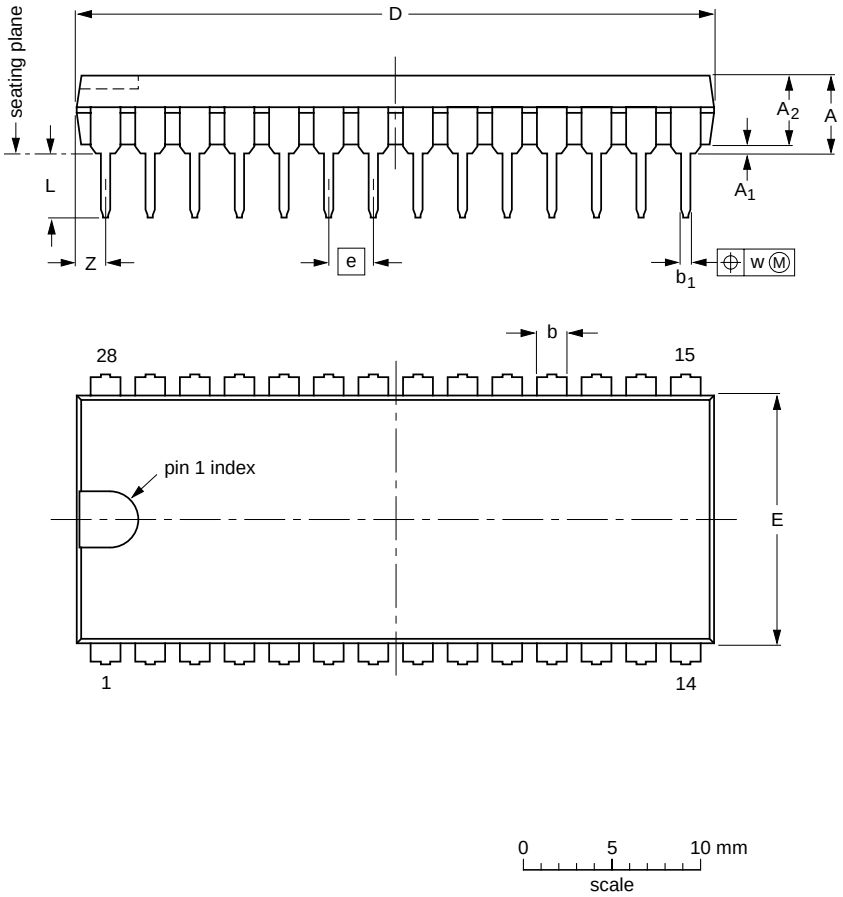


Fig.12 Test and application circuit.

PACKAGE OUTLINE

DIP28: plastic dual in-line package; 28 leads (600 mil) **SOT117-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	5.1	0.51	4.0	1.7 1.3	0.53 0.38	0.32 0.23	36.0 35.0	14.1 13.7	2.54	15.24	3.9 3.4	15.80 15.24	17.15 15.90	0.25	1.7
inches	0.20	0.020	0.16	0.066 0.051	0.020 0.014	0.013 0.009	1.41 1.34	0.56 0.54	0.10	0.60	0.15 0.13	0.62 0.60	0.68 0.63	0.01	0.067

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT117-1	051G05	MO-015	SC-510-28			~~95-01-14~~ 99-12-27

SOLDERING

Introduction to soldering through-hole mount packages

This text gives a brief insight to wave, dip and manual soldering. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

Wave soldering is the preferred method for mounting of through-hole mount IC packages on a printed-circuit board.

Soldering by dipping or by solder wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joints for more than 5 seconds.

The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg(max)}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

Manual soldering

Apply the soldering iron (24 V or less) to the lead(s) of the package, either below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

Suitability of through-hole mount IC packages for dipping and wave soldering methods

PACKAGE	SOLDERING METHOD	
	DIPPING	WAVE
DBS, DIP, HDIP, SDIP, SIL	suitable	suitable[1]

Note

1. For SDIP packages, the longitudinal axis must be parallel to the transport direction of the printed-circuit board.

DATA SHEET STATUS

DATA SHEET STATUS	PRODUCT STATUS	DEFINITIONS (1)
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

Note

1. Please consult the most recently issued data sheet before initiating or completing a design.

DEFINITIONS

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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