Green-Mode PWM Controller with Latch off Protections

REV: 00

General Description

LD7532 is specifically designed for a low cost system by integrating in a SOT-26 package many functions, protections, and EMI-improved solution which usually need a lot of extra components or circuits on a system design.

Furthermore, CT pin latch-off function triggered by a high voltage above 3.1V provides power circuit designers to easily deal with protection schemes, such as OVP and OTP, and to minimize component cost and developing time.

In order to satisfy different designs, the OVP trig level is adjustable by user adding a Zener diode from VCC pin to CT pin.

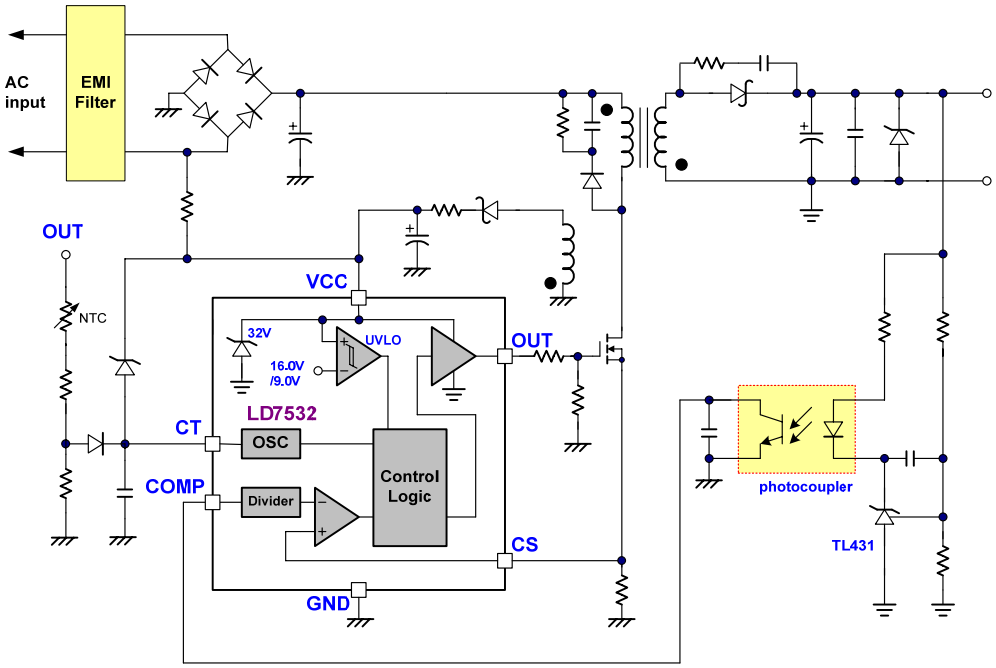
Features

- High-Voltage CMOS Process with ESD protection
- Very Low Startup Current (<20μA)
- Current Mode Control
- Non-audible-noise Green Mode Control
- UVLO (Under Voltage Lockout) on VCC Pin
- LEB (Leading-Edge Blanking) on CS Pin
- Programmable OLP Delay Time
- Internal Slope Compensation
- External OVP Latch-off Protection
- OLP (Over Load Protection) Auto-recovery Mode
- External OTP Latch-off Protection
- 300mA Driving Capability

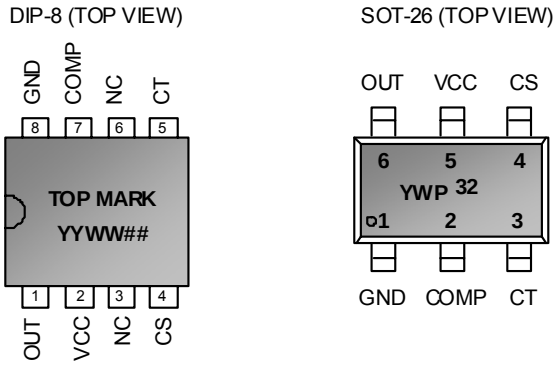
Applications

- Switching AC/DC Adaptor and Battery Charger
- Open Frame Switching Power Supply

Typical Application



Pin Configuration



YY, Y : Year code (D: 2004, E: 2005.....)
WW, W: Week code
P : LD75..
(Product family code)
: Production code

Ordering Information

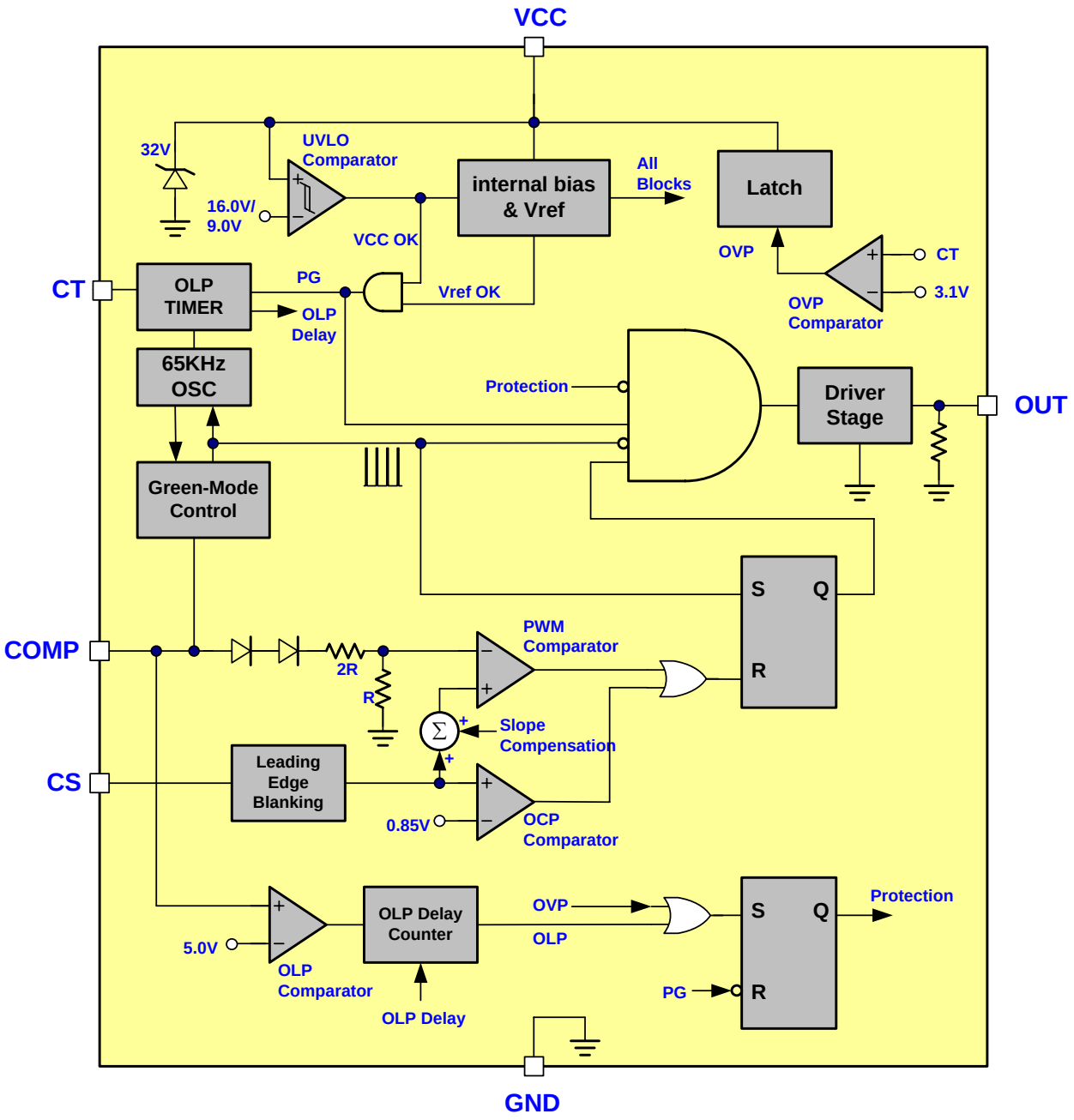
Part number	Package		TOP MARK	Shipping
LD7532 GL	SOT-26	Green Package	YWP/32	3000 /tape & reel
LD7532 GN	DIP-8	Green Package	LD7532GN	3600 /tube /Carton

The LD7532 is RoHS compliant.

Pin Descriptions

PIN SOT-26	PIN DIP-8	NAME	FUNCTION
1	8	GND	Ground
2	7	COMP	Voltage feedback pin (same as the COMP pin in UC384X). Connecting a photo-coupler to this pin closes the control loop and achieves the regulation.
3	5	CT	Connecting a capacitor to ground sets the frequency of a timer for OLP. Another function of this pin provides latch off control
4	4	CS	Current sense pin, connected to sense external MOSFET current.
5	2	VCC	Supply voltage pin
6	1	OUT	Gate drive output to drive an external MOSFET

Block Diagram



Absolute Maximum Ratings

Supply Voltage VCC	30V
COMP, CT, CS	-0.3 ~7V
OUT	-0.3 ~VCC+0.3V
Junction Temperature	150°C
Operating Ambient Temperature	-20°C to 85°C
Storage Temperature Range	-65°C to 150°C
Package Thermal Resistance (SOT-26)	250°C/W
Package Thermal Resistance (DIP-8)	100°C/W
Power Dissipation (SOT-26, at Ambient Temperature of 85°C)	250mW
Power Dissipation (DIP-8, at Ambient Temperature of 85°C)	650mW
Lead temperature (Soldering, 10sec)	260°C
ESD Voltage Protection, Human Body Model	3.0 KV
ESD Voltage Protection, Machine Model	300 V
Gate Output Current	300mA

Caution:

Stresses beyond the ratings specified in “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Recommended Operating Conditions

Item	Min.	Max.	Unit
Supply Voltage Vcc	11	25	V
CT Value	0.047	0.1	μF
Comp pin Parallel Capacitor	0.001	0.1	μF
Startup Resister	540K	--	Ω

Electrical Characteristics

(T_A = +25°C unless otherwise stated, V_{CC}=15.0V)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage (Vcc Pin)					
Startup Current			12	20	μA
Operating Current (with 1nF load on OUT pin)	V_{COMP}=0V		2.5		mA
	V_{COMP}=3V		3.0		mA
	Protection tripped mode		0.45		mA
UVLO (off)		9.0	10.0	11.0	V
UVLO (on)		15.0	16.0	17.0	V
Voltage Feedback (Comp Pin)					
Short Circuit Current	V_{COMP}=0V		1.5		mA
Open Loop Voltage	COMP pin open		6.0		V
OLP Current	COMP pin open		0.45		mA
Green Mode Threshold VCOMP			2.35		V
Burst Mode Threshold VCOMP			1.4		V
Current Sensing (CS Pin)					
Maximum Input Voltage, Vcs(off)		0.80	0.85	0.90	V
Leading Edge Blanking Time			220		nS
Input impedance		1			MΩ
Delay to Output			100		nS
Oscillator for Switching Frequency					
Frequency		60	65	70	KHz
Green Mode Frequency			20		KHz
Temp. Stability	(-40°C ~105°C)		5		%
Voltage Stability	(VCC=11V-25V)		1		%
FM Oscillator (CT pin)					
Timer Frequency	CT=0.047μF		220		Hz
OVP trigger level (Latch)		2.9	3.1	3.3	V
Holding Current	Vcc=7V(latched),		250		uA
Gate Drive Output (OUT Pin)					
Output Low Level	VCC=15V, Io=20mA			1.0	V
Output High Level	VCC=15V, Io=20mA	8			V
Rising Time	Load Capacitance=1000pF		180	360	nS
Falling Time	Load Capacitance=1000pF		50	100	nS
Max. Duty	Load Capacitance=1000pF		75		%
OLP (Over Load Protection)					
OLP Trip Level	Vcomp(OLP)		5.0		V
OLP Delay time	CT=0.047μF		45		mS

Typical Performance Characteristics

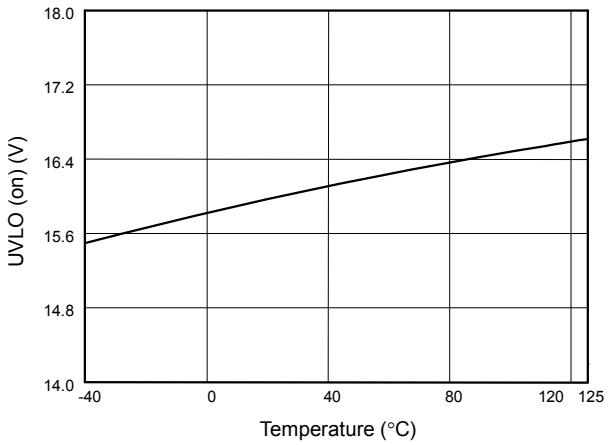


Fig. 1 UVLO (on) vs. Temperature

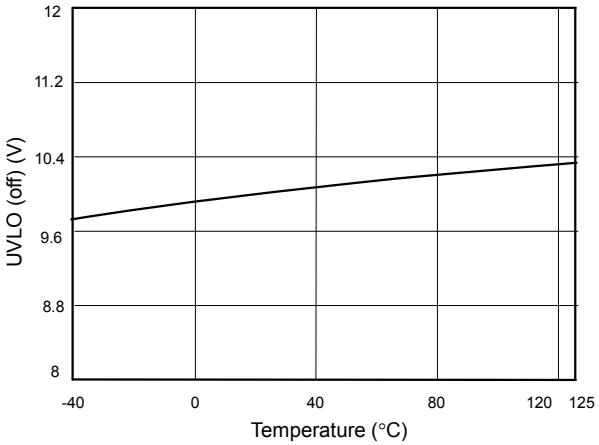


Fig. 2 UVLO (off) vs. Temperature

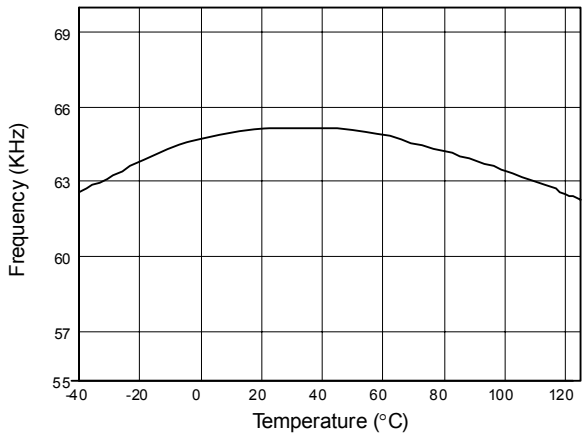


Fig. 3 Frequency vs. Temperature

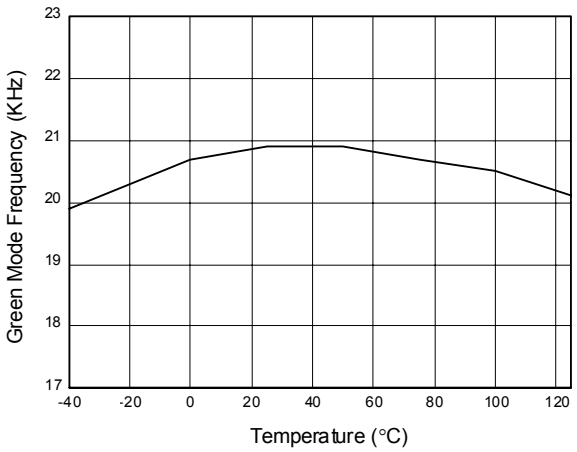


Fig. 4 Green Mode Frequency vs. Temperature

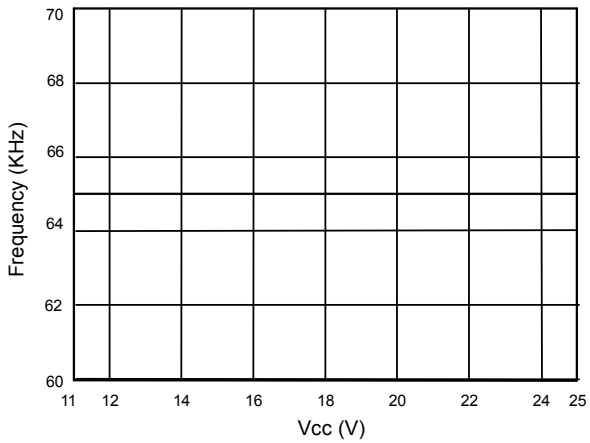


Fig. 5 Frequency vs. Vcc

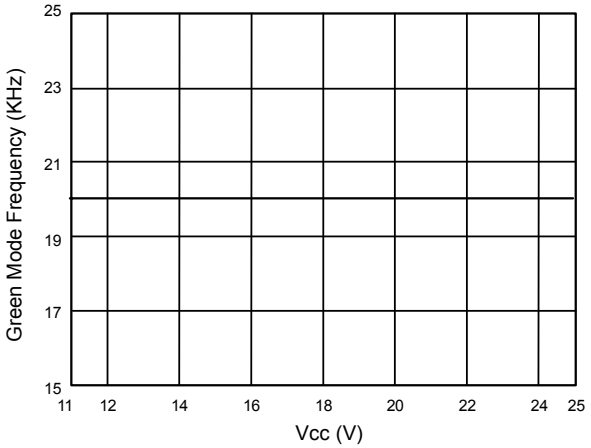


Fig. 6 Green Mode Frequency vs. Vcc

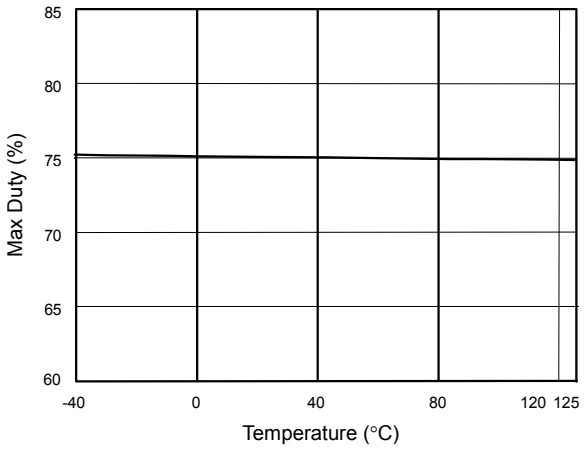


Fig. 7 Max Duty vs. Temperature

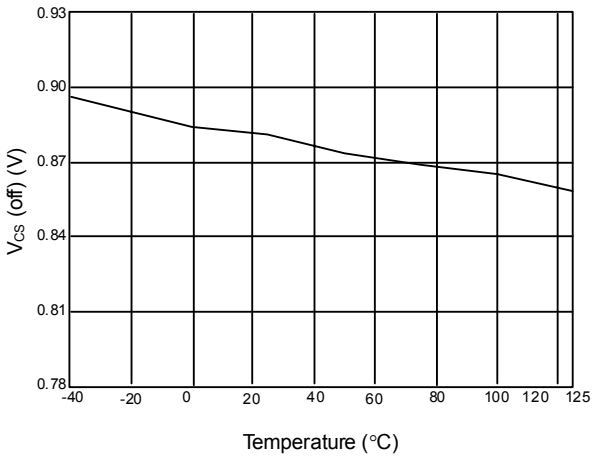


Fig. 8 V_{CS} (off) vs. Temperature

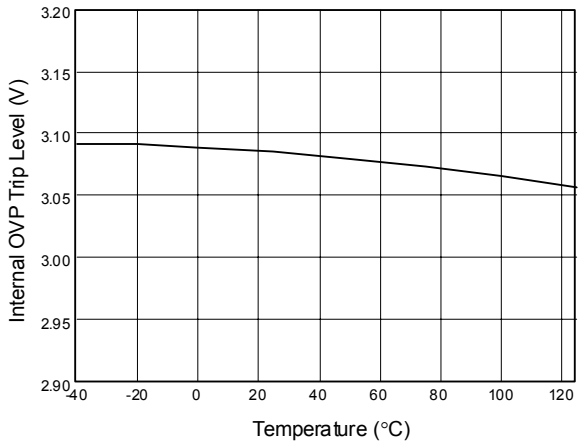


Fig. 9 Internal OVP Trip Level vs. Temperature (°C)

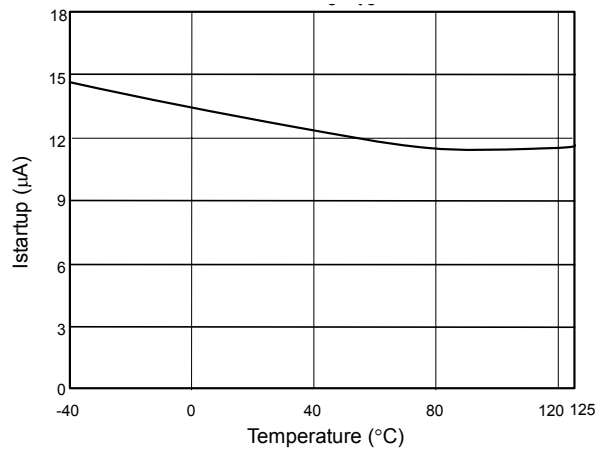


Fig. 10 Startup Current (Istartup) vs. Temperature

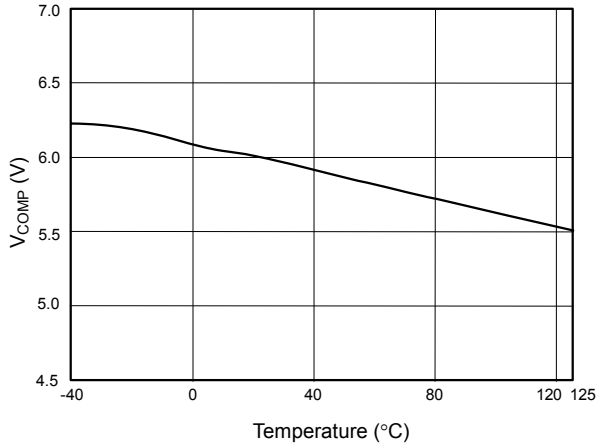


Fig. 11 V_{COMP} open loop voltage vs. Temperature

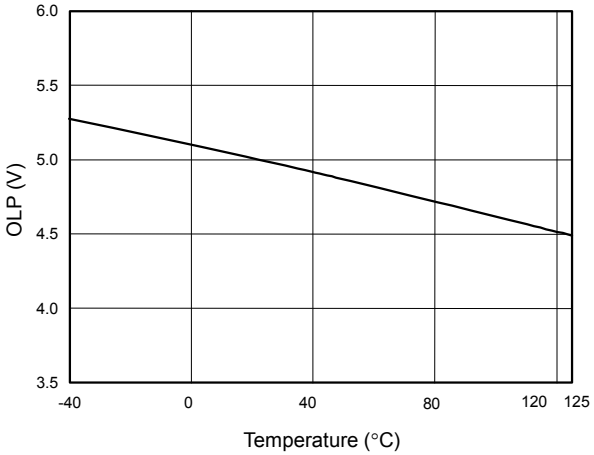


Fig. 12 OLP-Trip Level vs. Temperature

Application Information

Operation Overview

LD7532 meets green-power requirement and is intended for the use in those modern switching power suppliers and adaptors which demand higher power efficiency and power-saving. It integrates more functions to reduce external component counts and the resulted system size. Its major features are described as below.

Under Voltage Lockout (UVLO)

An UVLO comparator is implemented in it to detect the voltage on the VCC pin. It would assure the supply voltage high enough to turn on PWM controllers in LD7532 and further to drive the power MOSFET. As shown in Fig. 13, a hysteresis is provided to UVLO to prevent the shutdown from the voltage dip during startup. The turn-on and turn-off threshold levels are set as 16.0V and 10.0V, respectively.

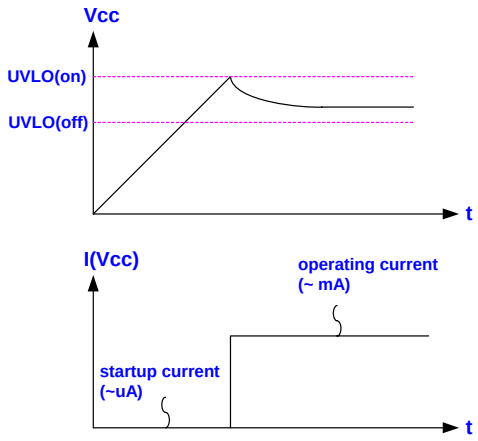


Fig. 13

Startup Current and Startup Circuit

The typical startup circuit to generate the LD7532 Vcc is shown in Fig. 14. During the startup transient, the Vcc is lower than the UVLO threshold, thus there is no gate pulse produced from LD7532 to drive power MOSFET. Therefore, the current through R1 will provide the startup current, charging the capacitor C1. Whenever the Vcc voltage is high enough to turn on the LD7532 and further to deliver the gate drive signal, the supply current is provided from the auxiliary winding of the transformer. Lower startup current required for the PWM controller will help to increase the value of R1 and then reduce the power consumption on R1. By using CMOS process and the special circuit design, the maximum startup current of LD7532 is as low as 20μA.

The higher the resistance value of the R1, the longer the startup time. Careful selection of the values of R1 and C1 will optimize the power consumption and the startup time.

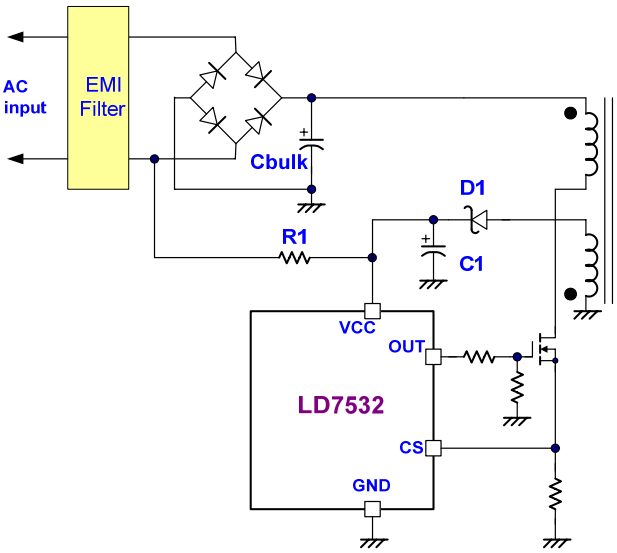


Fig. 14

Current Sensing and Leading-edge Blanking

The typical current mode of PWM controller feeds back both current and voltage signals to close the control loop and achieve regulation. As shown in Fig. 15, LD7532 detects the external MOSFET current from the CS pin, which is not only for the peak current mode control but also for the pulse-by-pulse current limit. The maximum voltage threshold of the current sensing pin is set at 0.85V. From above, the MOSFET peak current can be obtained from below.

$$I_{PEAK(MAX)} = \frac{0.85V}{R_S}$$

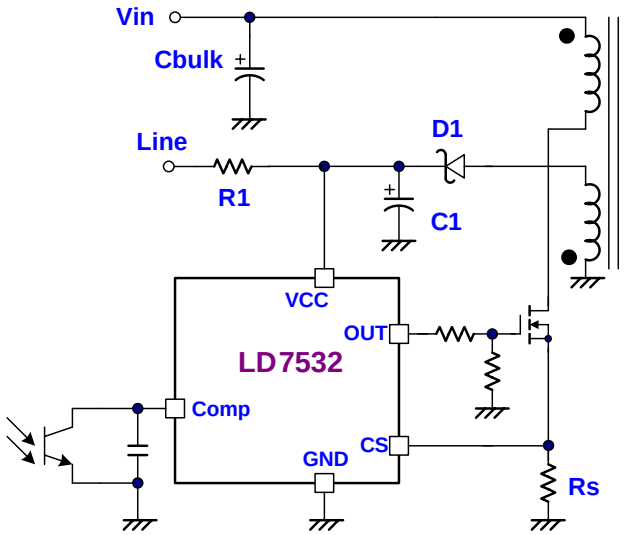


Fig. 15

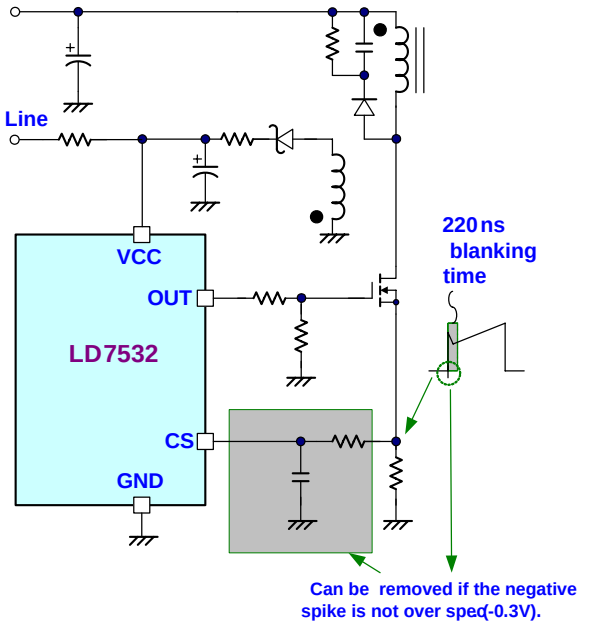


Fig. 16

A 220nS leading-edge blanking (LEB) time is included in the input of CS pin to prevent the false-trigger from the current spike. In the low power application, if the total pulse width of the turn-on spikes is less than 220nS and the negative spike on the CS pin is not under -0.3V, the R-C filter connected to CS pin as shown in figure 16 could be removed. Nevertheless, as shown in figure 16, it is strongly recommended to adopt a smaller R-C filter at the CS pin for higher power applications to avoid the CS pin from being damaged by an over-negative turn-on spike.

Output Stage and Maximum Duty-Cycle

An output stage of a CMOS buffer, with typical 300mA driving capability, is incorporated to drive a power MOSFET directly. And the maximum duty-cycle of LD7532 is limited to 75% to avoid transformer saturation.

Voltage Feedback Loop

The voltage feedback signal is provided from the TL431 at the secondary side through the photo-coupler to the COMP pin of LD7532. Similar to UC3842, LD7532 would carry a two-diode voltage offset at the stage to feed the voltage divider at the ratio of 1/3, that is,

$$V_{-(PWM_{COMPARATOR})} = \frac{1}{3} \times (V_{COMP} - 2V_F)$$

A pull-high resistor is embedded internally, eliminating the necessity of an external pull-high resistor..

Oscillator and Switching Frequency

The switching frequency of LD7532 is substantially fixed as 65 KHz internally to provide the optimized operations in respect with EMI performance, thermal treatment, component sizes and transformer design.

Internal Slope Compensation

In conventional applications, stability is a critical issue for current mode control, especially when it operates in higher than 50% of the duty-cycle. As UC384X, LD7532 implements slope compensation by internally injecting the ramp signal of the RT/CT pin through a coupling capacitor, and, therefore, requires no external design.

Dual-Oscillator Green-Mode Operation

Many different topologies have been implemented in different chips for the green-mode or power saving requirements such as “burst-mode control”, “skipping-cycle mode”, “variable off-time control “…etc. The basic operation theory of all these approaches intends to reduce the switching cycles under light-load or no-load condition either by skipping some switching pulses or reducing the switching frequency.

What LD7532 uses to implement the power-saving operation is Leadtrend Technology’s own IP. In such approaching, as shown in the block diagram, there are 2

oscillators implemented in LD7532. The first oscillator is to set the normal switching frequency, which can be set by the CT pin through an external capacitor. In such normal operation mode, as shown in Fig. 17, the 2nd oscillation (green-mode oscillator) does not activate. Therefore, the rising-time and the falling-time of the internal ramp will be constant to achieve good stability over all temperature range. Under the normal operation, the first oscillator dominates the switching frequency.

The green-mode oscillator will detect the signal of COMP pin to determine if it meets a certain requirement. When the signal of V- is lower than the green-mode threshold V_{GREEN}, the green-mode oscillator activates. The green-mode oscillator, implemented by a VCO (voltage controlled oscillator), is a variable frequency oscillator.

By using this dual-oscillator control, the green-mode frequency can be well controlled and further to avoid the generation of audible noise.

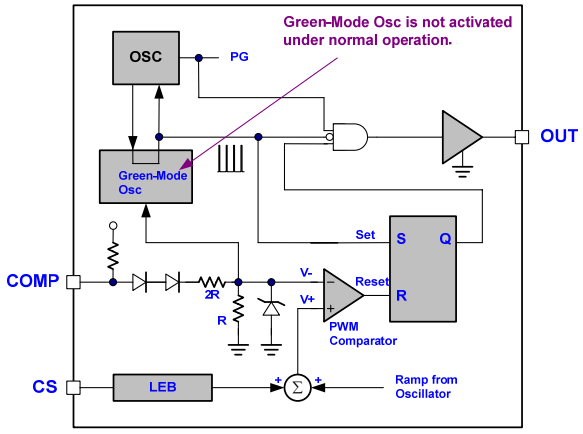


Fig. 17

Latch Off Control

LD7532 can be latched off by injecting the CT pin a voltage signal higher than 3.1V. The gate output pin of the LD7532 will be disabled immediately under such condition. This latch-off can't be released unless the VCC voltage goes under a de-latch level by, for example, recycled the input power.

OVP/OTP Implementation on CT Pin

The OVP function could be implemented by adding a Zener diode from VCC pin to CT pin. The protection is a latch type. If the OVP condition occurs, usually caused by the feedback loop opened, the Vcc trips over the OVP level (Vz+3.1V) and shutdowns the output. The Vcc will be discharged to a low level for easily reset again. Figure 18 shows its operation.

OTP function could be implemented by connecting from OUT pin to CT PIN a simple divider circuit composed of a proper N.T.C. While temperature is rising and causing the resistance down, the CT pin voltage is over pulled to trigger the IC into latch-off, which could be released by recycling the input power same as the OVP behavior.

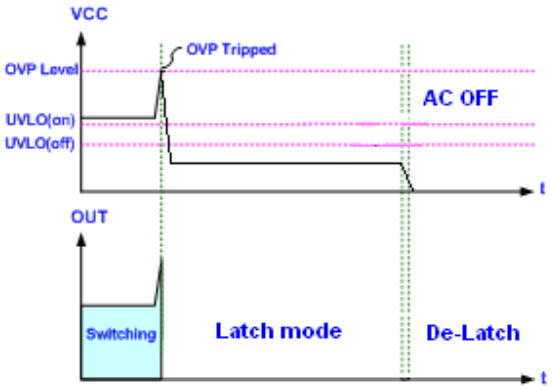


Fig. 18

Over Load Protection (OLP)

To protect the circuit from being damaged under over load condition or short condition, a smart OLP function is implemented in the LD7532. Figure 19 shows the waveforms of the OLP operation. In the beginning of the OLP operation, the feedback system forces the voltage loop proceed toward saturation and pulls up the voltage on COMP pin (V_{COMP}). Whenever the V_{COMP} trips up to the OLP threshold, 5V, and stays longer than the OLP delay time, OLP activates and turns off the gate output, stopping the switching of power circuit. The OLP delay time, set by CT pin, is to prevent the false trigger from the power-on and turn-off transients. The higher the CT value, the longer the OLP delay time. For instance, the OLP delay time is around 85mS when CT=0.1μF and will be around 40mS if CT=0.047μF.

By such protection mechanism, the average input power can be reduced to a very low level so that the component temperature and stress can be controlled within a safe operating area.

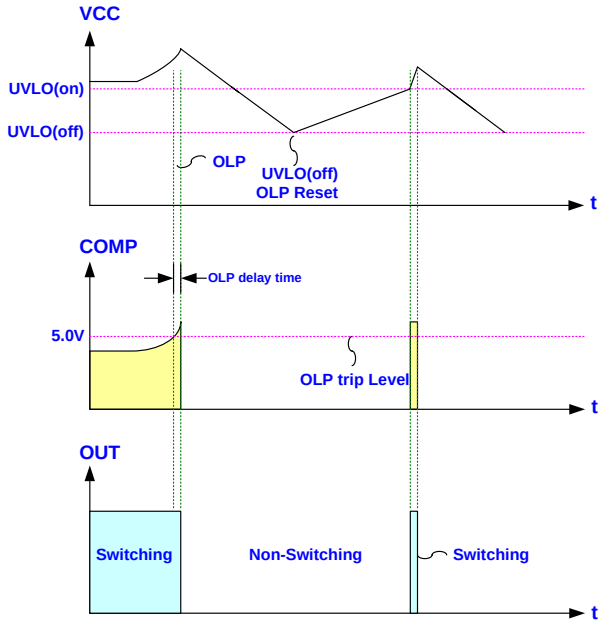
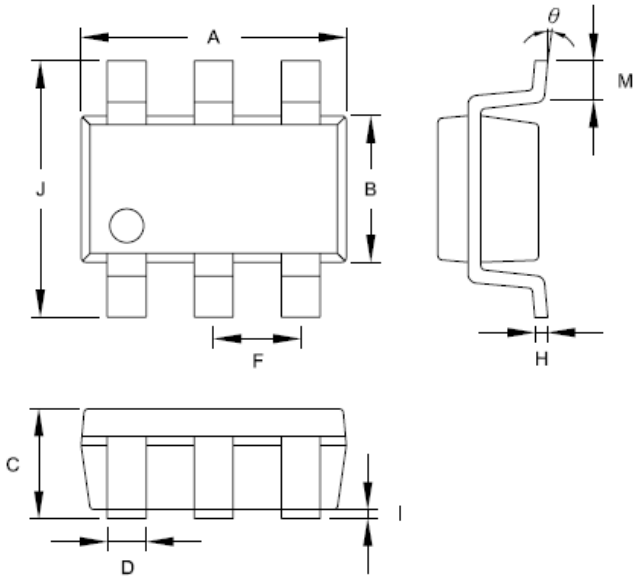

VCC
UVLO(on)
UVLO(off)
OLP
UVLO(off)
OLP Reset
t
COMP
OLP delay time
5.0V
OLP trip Level
t
OUT
Switching
Non-Switching
Switching
t

Fig. 19

Package Information

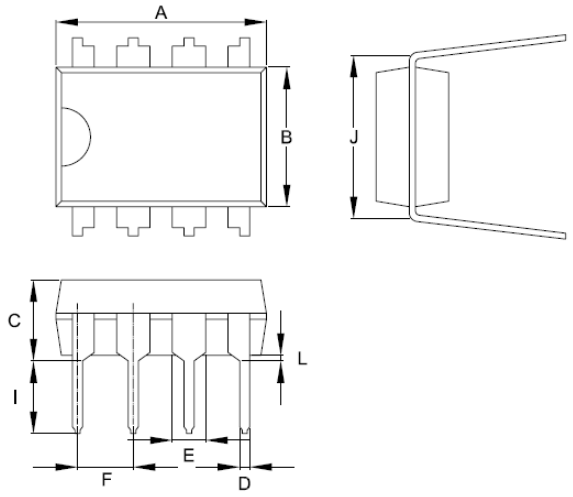
SOT-26



Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min	Max	Min	Max
A	2.692	3.099	0.106	0.122
B	1.397	1.803	0.055	0.071
C	-------	1.450	-------	0.058
D	0.300	0.550	0.012	0.022
F	0.838	1.041	0.033	0.041
H	0.080	0.254	0.003	0.010
I	0.050	0.150	0.002	0.006
J	2.600	3.000	0.102	0.118
M	0.300	0.600	0.012	0.024
θ	0°	10°	0°	10°

Package Information

DIP-8



Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min	Max	Min	Max
A	9.017	10.160	0.355	0.400
B	6.096	7.112	0.240	0.280
C	-----	5.334	------	0.210
D	0.356	0.584	0.014	0.023
E	1.143	1.778	0.045	0.070
F	2.337	2.743	0.092	0.108
I	2.921	3.556	0.115	0.140
J	7.366	8.255	0.290	0.325
L	0.381	------	0.015	--------

Important Notice

Leadtrend Technology Corp. reserves the right to make changes or corrections to its products at any time without notice. Customers should verify the datasheets are current and complete before placing order.

Revision History

Rev.	Date	Change Notice
00	6/16/2008	Original Specification