NCP1212

Current Mode PWM Controller for Both Forward and Flyback Converters

NCP1212 is a high performance current mode PWM controller specifically designed for off−line and dc−to−dc converter applications. The device requires very few external components and offers designer additional protection for better system reliability. The device features a trimmed oscillator for precise duty−cycle control, accurate bandgap voltage reference, high gain error amplifier, current sensing comparator and a high current totem pole output gate driver that ideally drives the external power MOSFET. Additionally, the device has built−in programmable Brownout Detect and Soft−Start features to enhance system reliability. Also, the 48%/82% selectable maximum turn on duty−cycle control and external programmable switching frequency capabilities make this device an ideal controller for both forward and flyback configurations. This device is available in both PDIP−8 and space saving SO−8 packages.

Features

- Trimmed Oscillator Charge and Discharge Current for Precise Duty−Cycle Control
- Internal High Accuracy Bandgap Voltage Reference
- Current Mode Operation up to 200 kHz
- Inherent Feed Forward Compensation
- Latching PWM for Cycle−by−Cycle Current Limiting
- High Current Totem Pole Output Gate Driver
- Low Startup and Operating Current
- Internal Undervoltage Lockout with Hysteresis
- Internal Leading Edge Blanking for Current Feedback
- Direct Interface with Optocoupler for Secondary Sensing
- Built−in Soft−Start Function, Programmable by External Capacitor
- User Programmable 48%/82% Maximum Duty−Cycle Selection
- Output Overvoltage Protection Against Open Loop
- AC Line Brownout Detect Protection
- Output Overload Protection Irrespective of Auxiliary Voltage Level

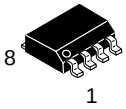
Typical Applications

- ATX PC Power Supply
- Universal Input Wall Mount Adaptors
- CRT Monitor
- All Flyback and Forward SMPS Systems

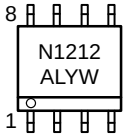
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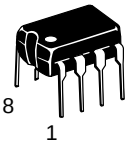
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MARKING DIAGRAMS

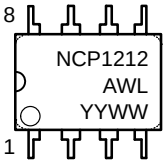


SO−8
D SUFFIX
CASE 751



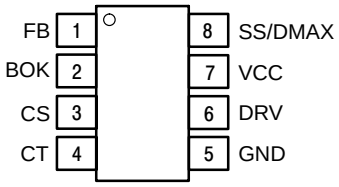


PDIP−8
P SUFFIX
CASE 626



A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Package	Shipping
NCP1212DR2	SO−8	2500 Tape & Reel
NCP1212P	PDIP−8	50 Units/Rail

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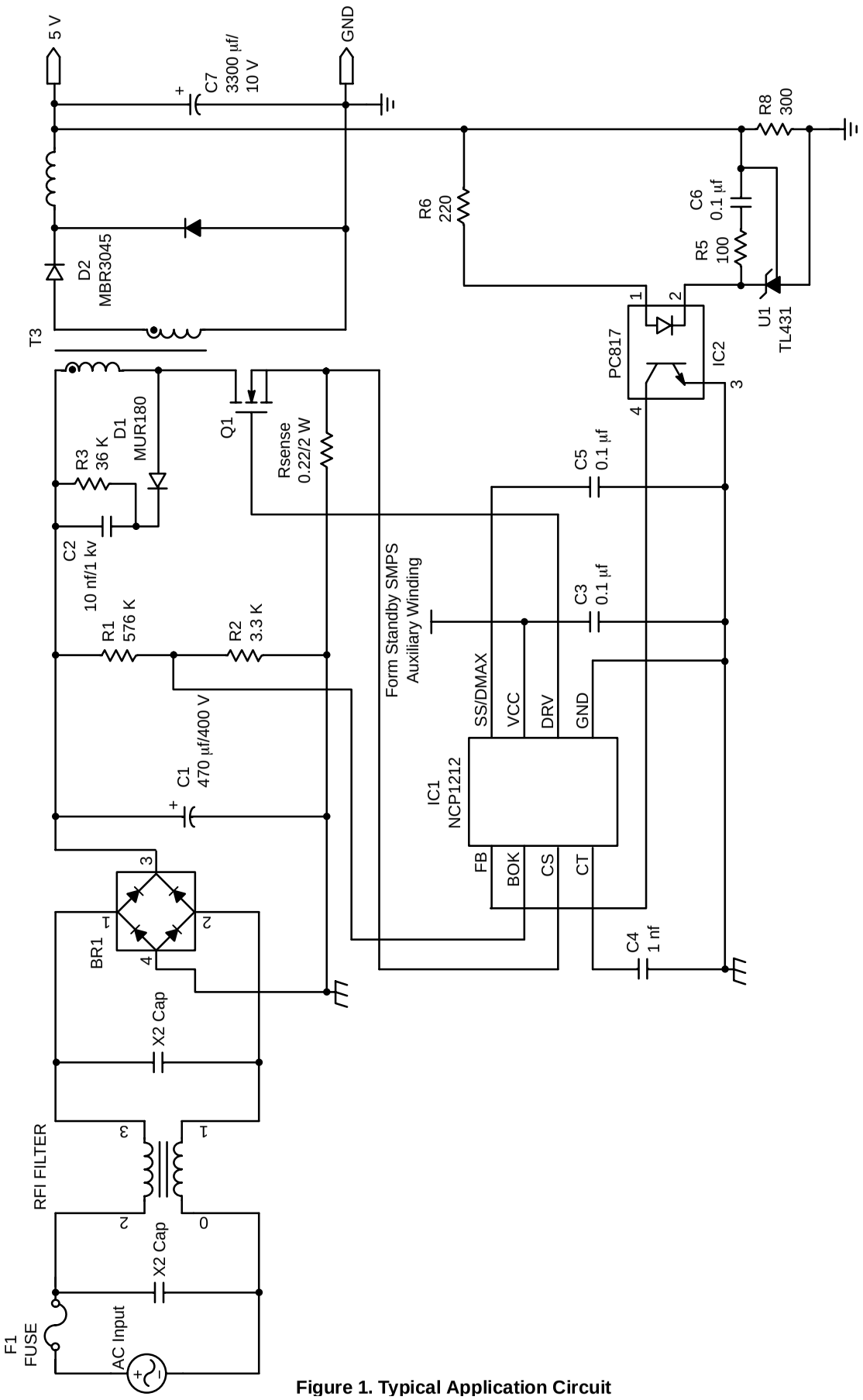


Figure 1. Typical Application Circuit

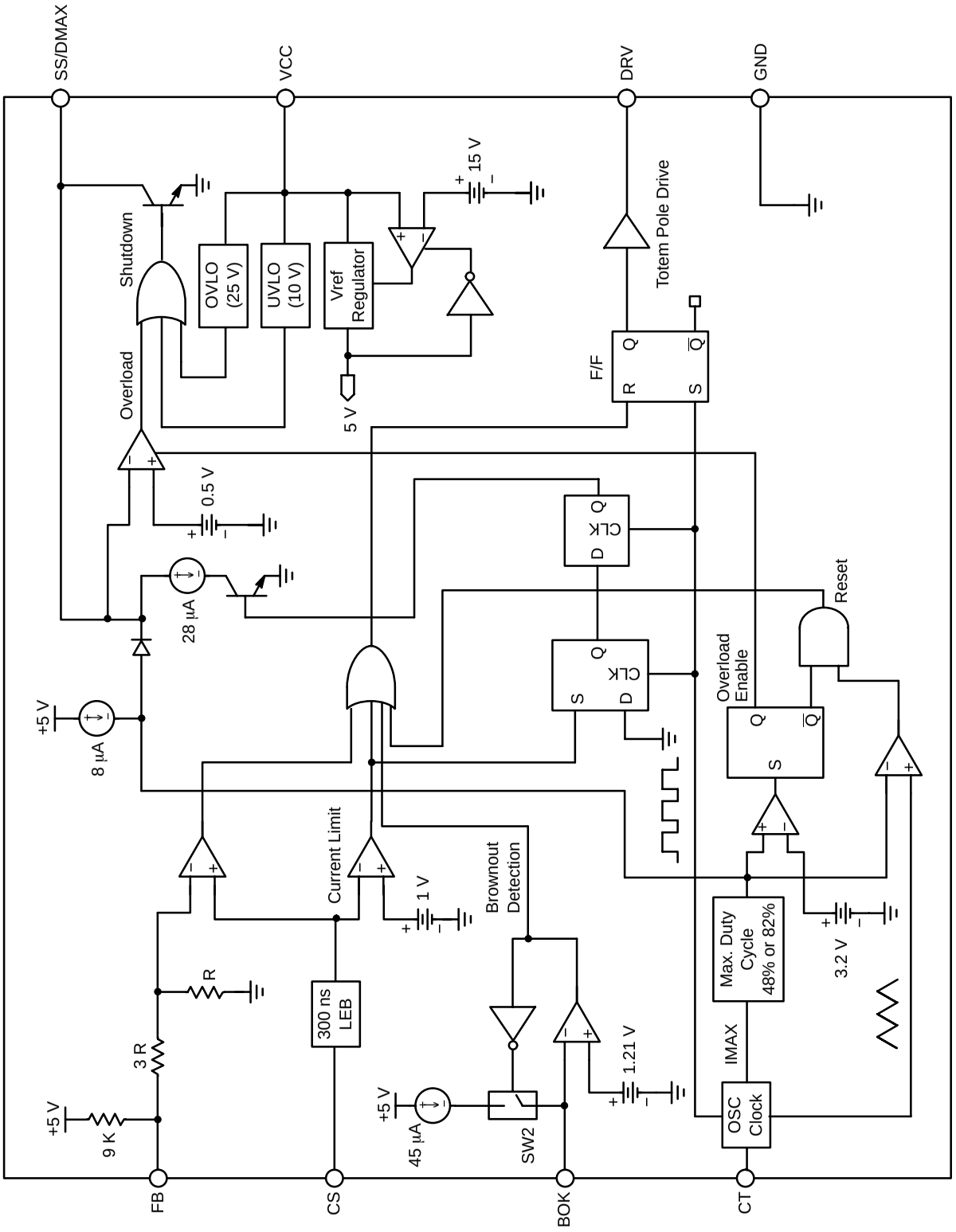


Figure 2. Simplified Functional Block Diagram

PIN FUNCTION DESCRIPTION

Pin	Name	Function	Description
1	FB	Feedback Input	This pin detects voltage feedback from output, can be connected directly to the optocoupler collector pin.
2	BOK	Brownout Detect with Hysteresis	This is the inverting input of the brownout detect comparator. The brownout detect comparator has a detect threshold voltage of 1.21 V. This pin senses the voltage of the bulk capacitor through a resistor divider network to determine the brownout event. The hysteresis band is provided by a 45 μA current flows out of this pin to the resistor network.
3	CS	Current Sense Input	During output on–time of the power switch, this pin receives a voltage proportional to power switch current set by the current sensing resistor. The information is utilized to terminate output switch conduction by PWM action or overcurrent limit circuitry.
4	CT	Programmed Oscillator Frequency	Connecting a capacitor from CT pin to ground programs the internal oscillator frequency. The oscillator can operate up to 200 kHz.
5	GND	IC Ground	−
6	DRV	Gate Driver Output	This is a high current totem pole output. The PWM driving control is provided by this pin. The current and slew rate capability of this pin are suitable to drive a Power MOSFET.
7	VCC	Positive Supply to IC	This pin is the positive supply of the IC. The driver output gets disabled when the voltage becomes higher than 25 V and the operating range is between 10 V and 25 V. The startup voltage is set at 15 V.
8	SS/DMAX	Soft−Start Time Programming and Maximum Duty−Cycle Selection	This is a multi−function pin. Soft−start effect is provided during startup with a capacitor connected to this pin. After soft−start period elapsed, the capacitor is used for timing control to determine output overload. If only a capacitor is connected to this pin, its final voltage is ~4.3 V and maximum turn−on duty−cycle DMAX is set at 82%. Connect a resistor in parallel with the capacitor can alter the final voltage of this pin. 48% DMAX is selected if this pin stays at 2.1 V to 2.8 V after soft−start period.

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage (Pin 7)	V_{CC}	−0.3, 28	V
Input/Output Pins (Pins 1, 2, 3, 4, 8)	V_{IO}	−0.3, 6.5	V
Gate Driver Output Pin (Pin 6)	V_{DRV}	−0.3, 14	V
Power Dissipation and Thermal Characteristics Thermal Resistance, Junction−to−Air, PDIP−8 Version Thermal Resistance, Junction−to−Air, SO−8 Version	$R_{\theta J-A}$	 100 178	°C/W
Output Current, Source or Sink	I_{DRV}	1.0	A
Operating Junction Temperature Range	T_J	−40 to +150	°C
Operating Ambient Temperature Range	T_A	−25 to +105	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C
ESD Capability, HBM (All pins except V_{CC} pin) (Note 1)	−	2.0	kV
ESD Capability, Machine Model (All pins except V_{CC} pin) (Note 1)	−	200	V

1. This device series contains ESD protection and exceeds the following tests:
   Human Body Model (HBM) ≤ 2.0 kV per JEDEC standard: JESD22−A114.
   Machine Model (MM) ≤ 200 V per JEDEC standard: JESD22−A115.
2. Latch−up Current Maximum Rating: ± 150 mA per JEDEC standard: JESD78.

ELECTRICAL CHARACTERISTICS (For typical values T_J = 25°C, DMAX = 48%, for min/max values T_J = −25°C to +105°C, V_{CC} = 16 V unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OSCILLATOR SECTION					
Oscillation Frequency, T_J = 25°C (DMAX = 48%, C_T = 1.0 nF)	F_{OSC-48}	81	90	99	kHz
Oscillation Frequency, T_J = 25°C (DMAX = 82%, C_T = 1.0 nF)	F_{OSC-82}	72	80	88	kHz
Frequency Change against Supply Voltage (V_{CC} = 13 V to 25 V, T_J = 25°C)	ΔF_{OSC-V}	−	0.02	−	%
Frequency Change against Temperature (V_{CC} = 16 V, T_J = −25°C to 105°C)	ΔF_{OSC-T}	−	5.0	−	%
CURRENT SENSE SECTION					
Maximum Current Sense Input Threshold	V_{CS}	0.96	1.0	1.16	V
Propagation Delay (Current Sense to Gate after LEB Blanking)	T_{PLH}	−	150	200	ns
Leading Edge Blanking Time	T_{LEB}	−	300	−	ns
SOFT−START SECTION					
Soft−Start Charge Current	I_{SS}	5.0	8.0	11	μA
Overload Timing Discharge Current (Note 3)	$I_{SD}-I_{SS}$	15	20	26	μA
48% Duty−Cycle Selection Input Voltage Threshold	V_{D48}	−	2.5	−	V
82% Duty−Cycle Selection Input Voltage Threshold	V_{D82}	−	3.0	−	V
GATE DRIVER SECTION					
Gate Drive Sink Capability, V_{CC} = 15 V, V_{DRV} = 1.0 V	I_{OL}	−	100	−	mA
Gate Drive Source Capability, V_{CC} = 15 V, V_{DRV} = 5.0 V (Note 4)	I_{OH}	−	300	−	mA
Gate Drive Voltage (From 1.0 V to 11 V) Rise Time (C_L = 1.0 nF, T_J = 25°C)	T_r	−	25	50	ns
Gate Drive Voltage (From 11 V to 1.0 V) Fall Time (C_L = 1.0 nF, T_J = 25°C)	T_f	−	25	50	ns
IC POWER SUPPLY SECTION					
V_{CC} Start−Up Threshold Voltage	VCC_{TH}	13.5	15	16.5	V
V_{CC} Overvoltage Lockout Threshold	VCC_{OVLO}	22.5	25	27.5	V
V_{CC} Undervoltage Lockout Threshold	VCC_{UVLO}	8.5	10	11.5	V
Power Supply Current, before Start−up (V_{CC} = 12 V)	I_{C1}	−	0.15	0.26	mA
Power Supply Current, Operating	I_{C2}	−	3.0	5.0	mA
Power Supply Current, Shutdown (V_{CC} = 15 V)	I_{C3}	−	3.0	−	mA
BROWNOUT DETECT SECTION (BOK)					
Brownout Input Threshold Voltage	V_{BOK}	1.14	1.21	1.27	V
Brownout Hysteresis Current	I_{BOK}	38	45	54	μA
MAXIMUM DUTY−CYCLE SECTION					
Maximum Duty−Cycle at Soft−Start Pin Voltage between 2.1 V and 2.8 V (2.1 V ≤ V_{DMAX} ≤ 2.8 V)	$DMAX_{48}$	47	48	50	%
Maximum Duty−Cycle at Soft−Start Pin Voltage Higher than 3.0 V (V_{DMAX} ≥ 3.0 V)	$DMAX_{82}$	79	82	88	%

3. I_{SD} is an internal current source not accessible externally.
4. The output voltage is internally clamped by 13.5 V Zener.

TYPICAL CHARACTERISTICS

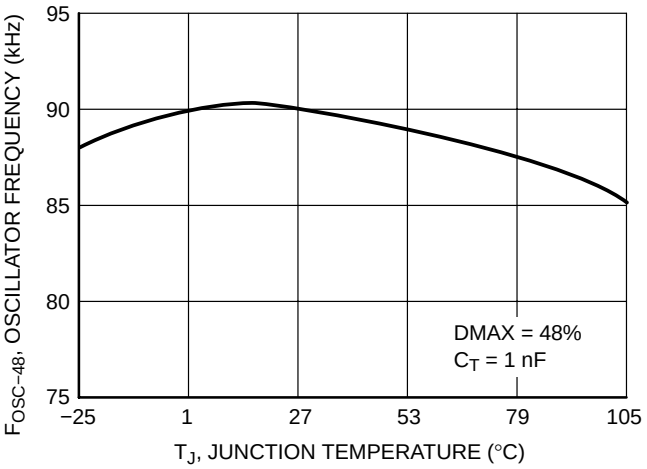


Figure 3. Oscillator Frequency with 48% Duty−Cycle vs. Junction Temperature

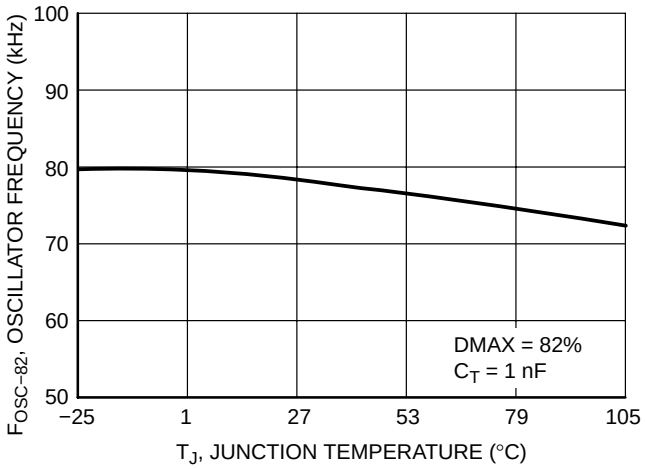


Figure 4. Oscillator Frequency with 82% Duty−Cycle vs. Junction Temperature

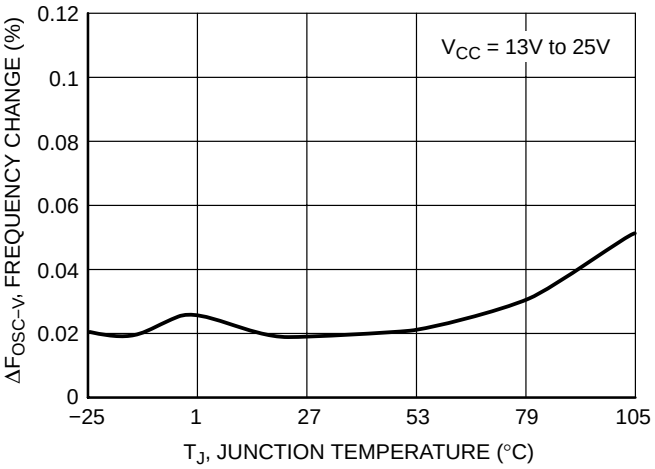


Figure 5. Frequency Change against Supply Voltage vs. Junction Temperature

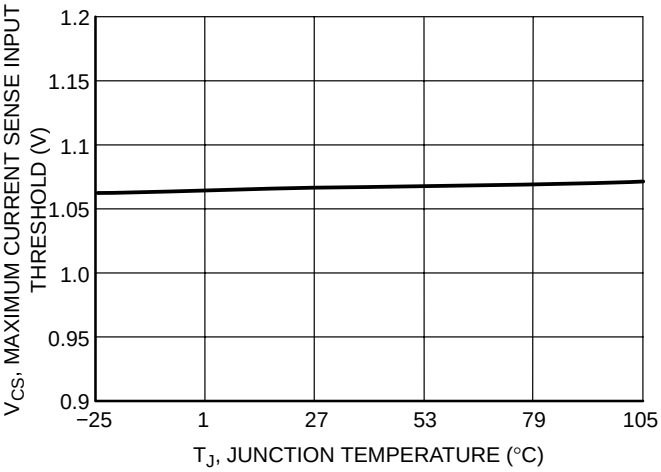


Figure 6. Maximum Current Sense Input Threshold Voltage vs. Junction Temperature

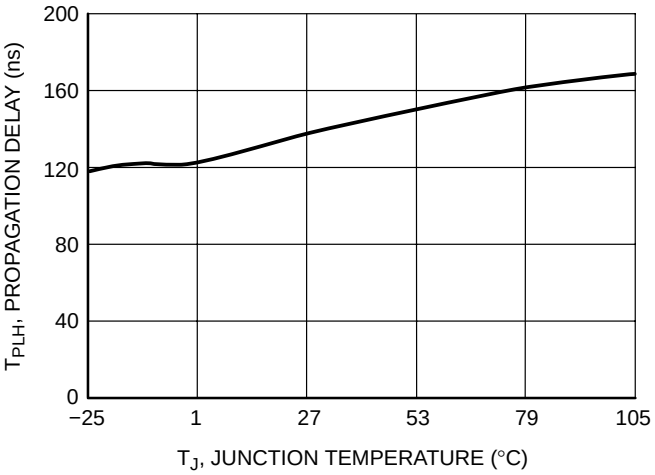


Figure 7. Propagation Delay vs. Junction Temperature

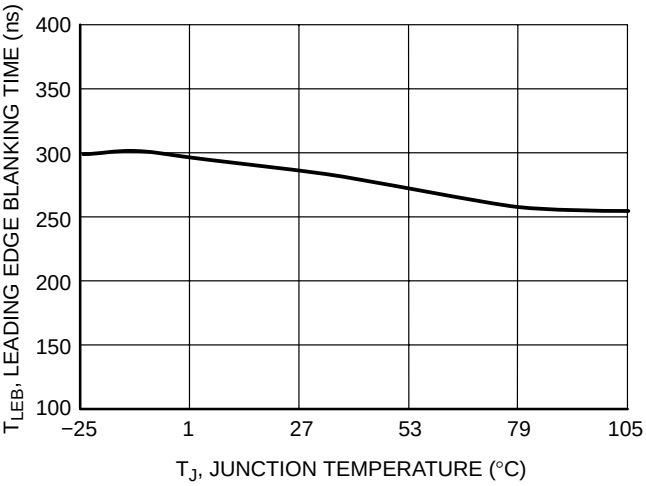


Figure 8. Leading Edge Blanking Time vs. Junction Temperature

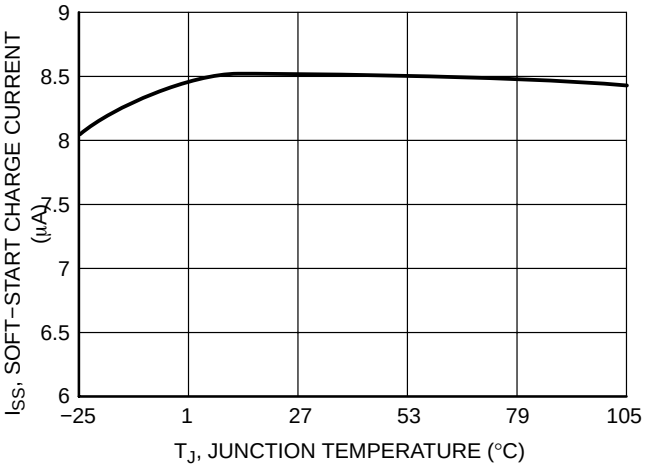


Figure 9. Soft−Start Charge Current vs. Junction Temperature

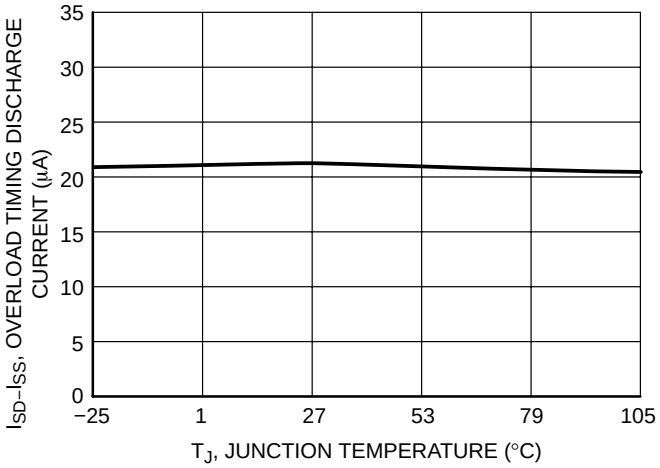


Figure 10. Overload Timing Discharge Current vs. Junction Temperature

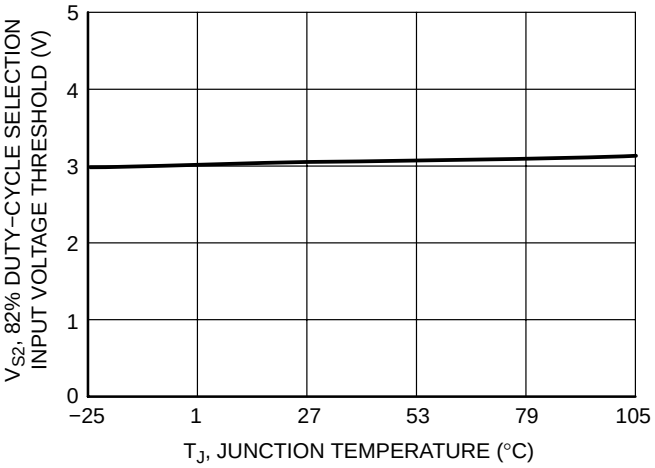


Figure 11. 82% Duty−Cycle Selection Input Voltage Threshold vs. Junction Temperature

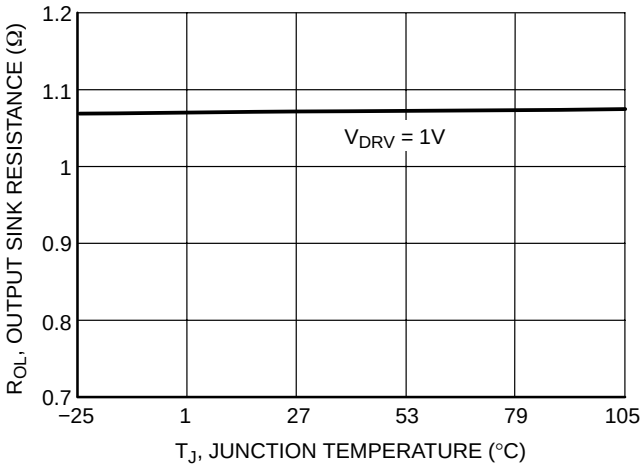


Figure 12. Output Sink Resistance vs. Junction Temperature

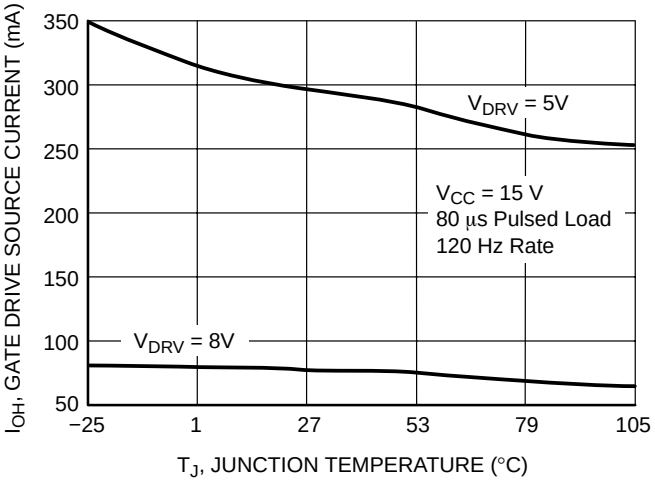


Figure 13. Gate Drive Source Capability vs. Junction Temperature

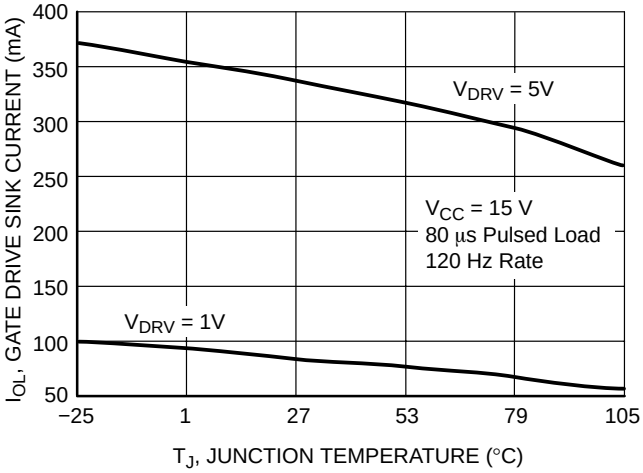


Figure 14. Gate Drive Sink Capability vs. Junction Temperature

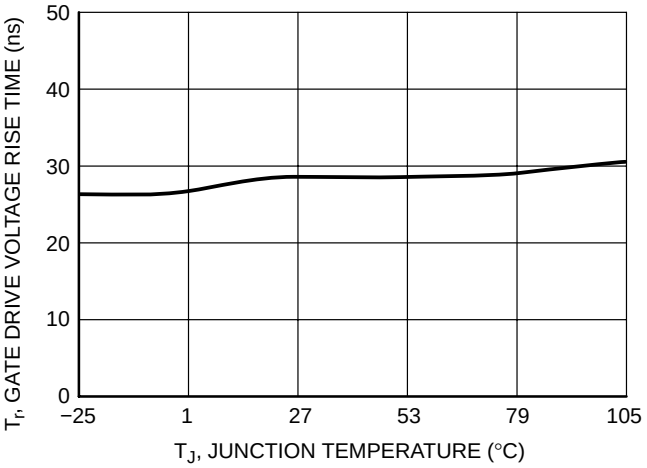


Figure 15. Gate Drive Voltage Rise Time vs. Junction Temperature

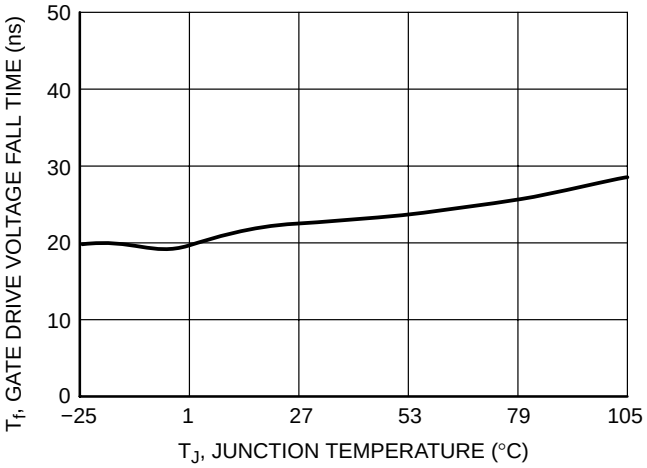


Figure 16. Gate Drive Voltage Fall Time vs. Junction Temperature

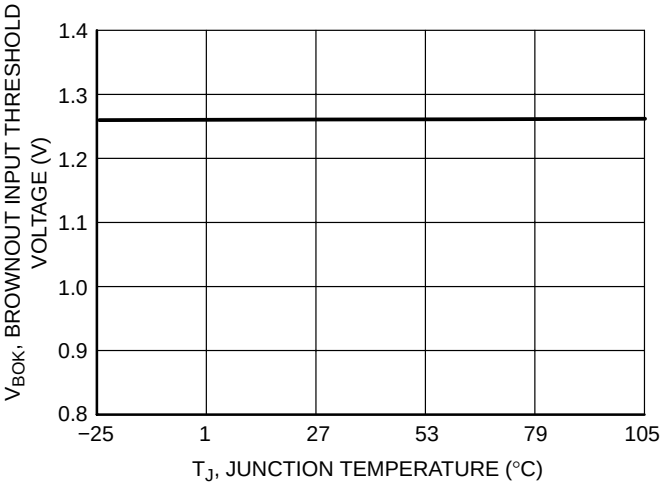


Figure 17. Brownout Input Threshold Voltage vs. Junction Temperature

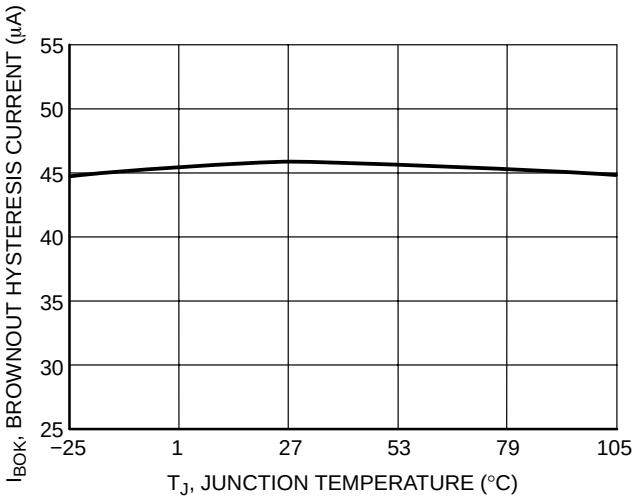


Figure 18. Brownout Hysteresis Current vs. Junction Temperature

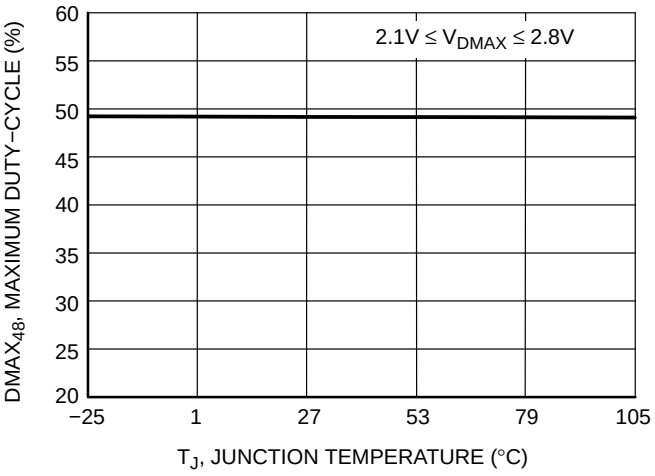


Figure 19. Maximum Duty−Cycle, $DMAX_{48}$ vs. Junction Temperature

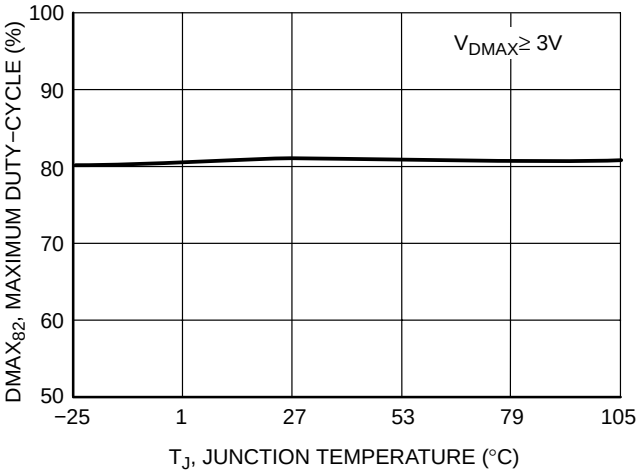


Figure 20. Maximum Duty−Cycle, $DMAX_{82}$ vs. Junction Temperature

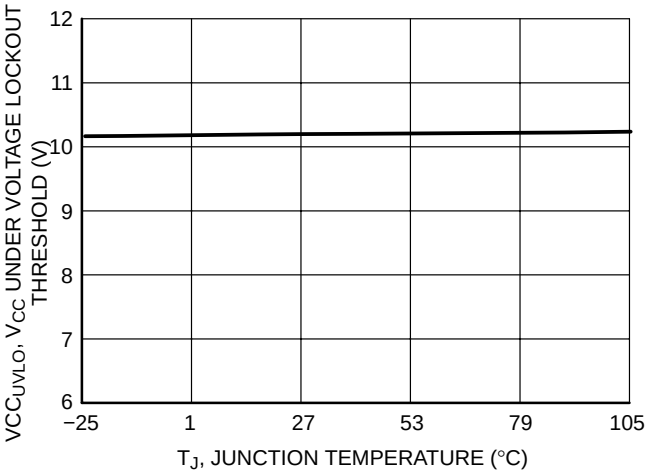


Figure 21. V_{CC} Under Voltage Lockout Threshold vs. Junction Temperature

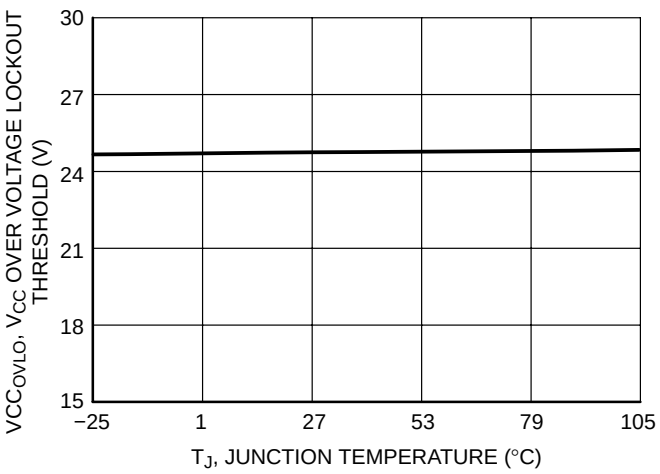


Figure 22. V_{CC} Over Voltage Lockout Threshold vs. Junction Temperature

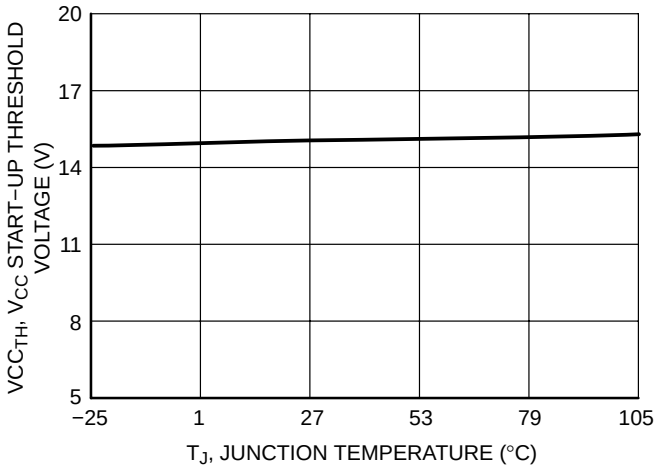


Figure 23. V_{CC} Start−up Threshold Voltage vs. Junction Temperature

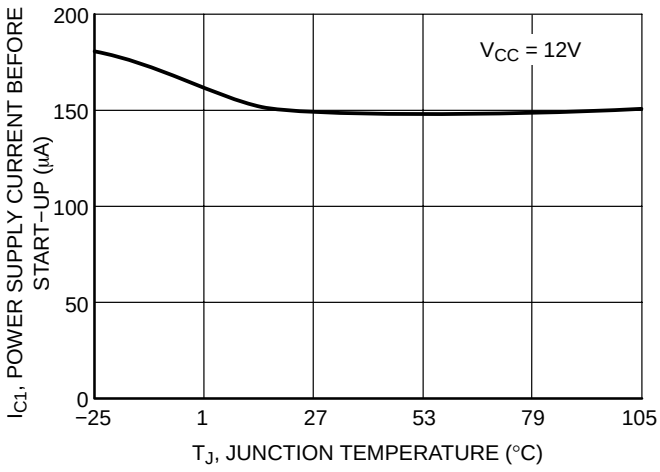


Figure 24. Power Supply Current Start−up vs. Junction Temperature

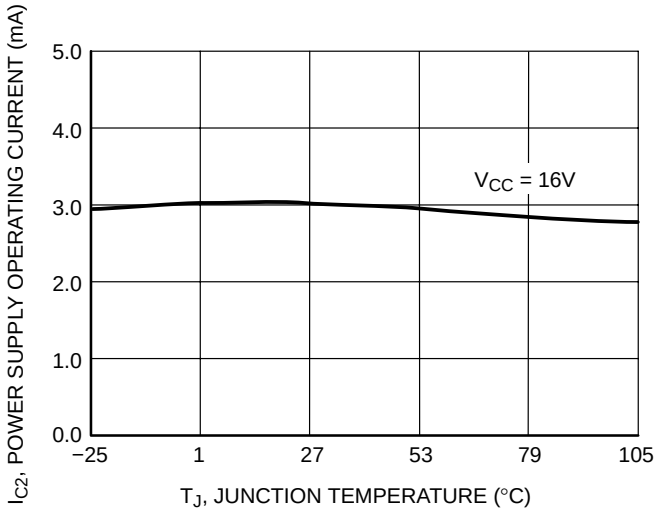


Figure 25. Power Supply Operating Current vs. Junction Temperature

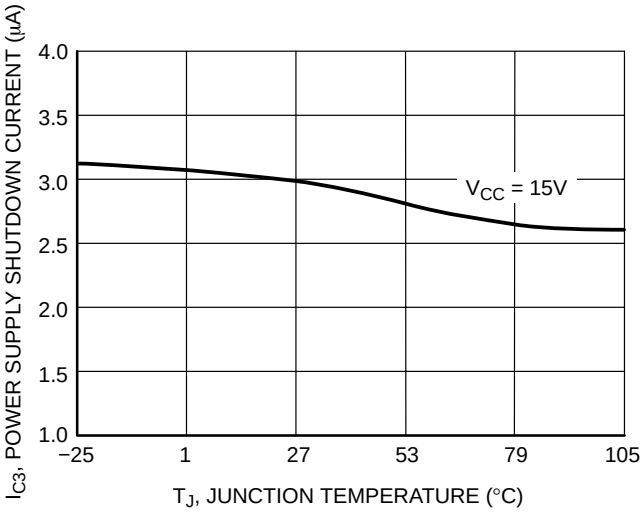


Figure 26. Power Supply Shutdown Current vs. Junction Temperature

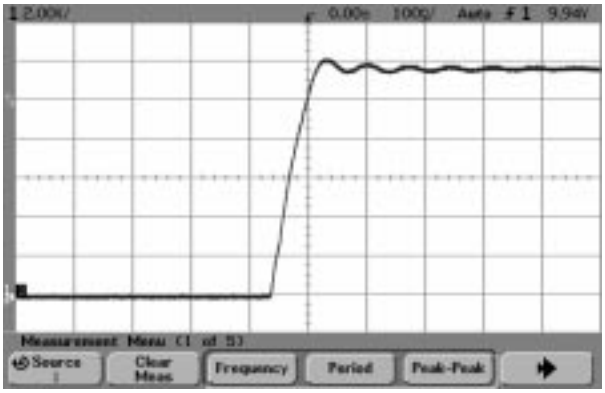


Figure 27. Rise Time of Gate Drive Waveform (C_L = 1 nF)

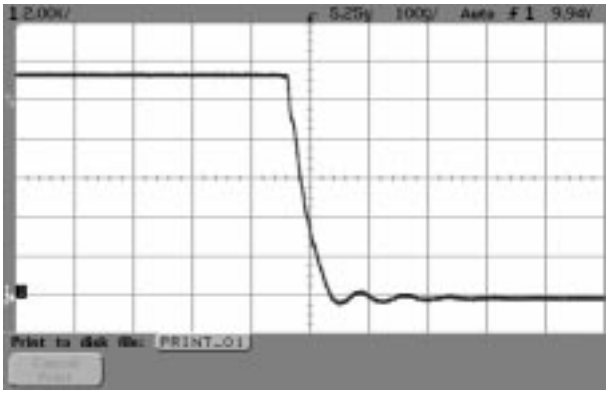


Figure 28. Fall Time of Gate Drive Waveform (C_L = 1 nF)

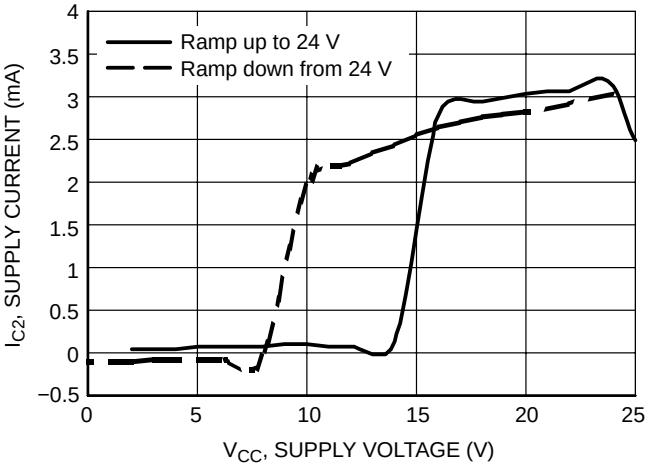


Figure 29. Supply Current vs. Supply Voltage (Duty−Cycle = 82% and Output Load = 1 nF)

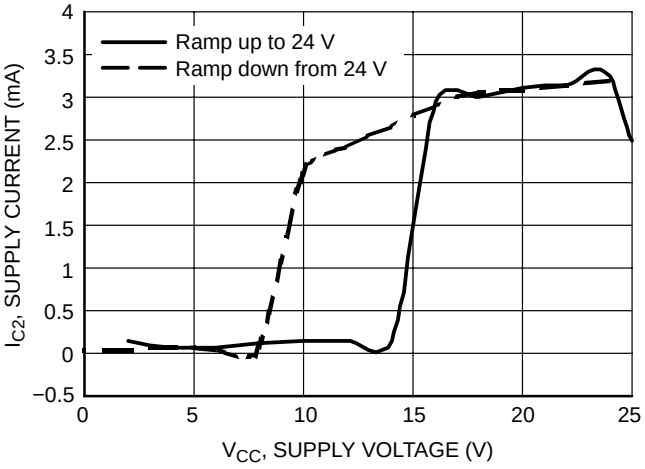


Figure 30. Supply Current vs. Supply Voltage (Duty−Cycle = 48% and Output Load = 1 nF)

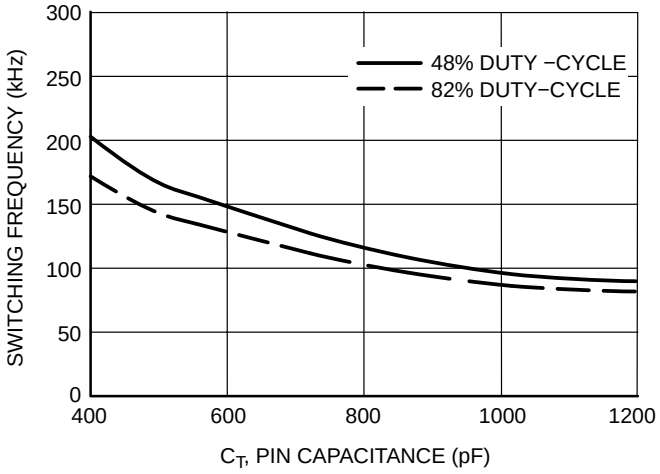


Figure 31. Switch Frequency vs. C_T Pin Capacitance

DETAILED OPERATING DESCRIPTIONS

INTRODUCTION

The NCP1212 implements a standard current mode architecture where the switch−off time is dictated by the peak current set point. This device represents an ideal candidate where low external part−count is the key system requirement. Additionally, the device provides extensive value−added functions, Soft−Start, Brownout Detect, etc., that can be applied to low−cost AC/DC adaptor applications. The NCP1212 incorporates all the necessary functions normally needed in UC384X based power supply systems: Oscillator section, PWM Latch section, Current Sense section, Brownout Detect protection, Soft−Start and Maximum Duty−Cycle Selection. With all those functions, this device becomes a good alternative to UC384X that can help to improve both performance and system cost. Also, the innovative Maximum Duty−Cycle Selection feature allows the device applied to both forward and fly−back mode configurations. Detailed functions of individual internal blocks are described in below and a simplified functional block diagram is shown in Figure 2.

Oscillator Section

The oscillator frequency is programmed by the capacitor connected to C_T pin. The capacitor is charged by a constant current source to 3.8 V and 2.5 V for 82% and 48% maximum duty−cycle condition respectively. Once the selected voltage is reached, C_T is then discharged by another constant current source down to 1.0 V and this charging and discharging action will carry on perpetually. Desirable switching frequency can be selected by choosing proper value of timing capacitor, C_T. The C_T pin waveform is shown in Figure 32.

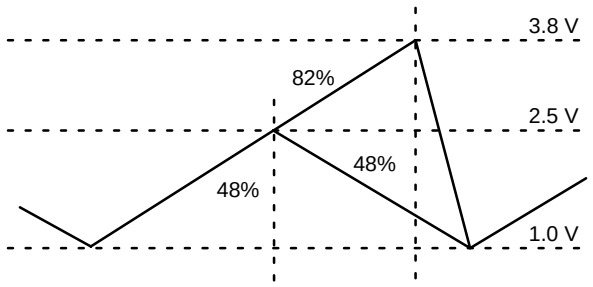


Figure 32. C_T Pin Waveform for Oscillator

PWM Latch Section

NCP1212 works in current mode. The power switch current is converted to a positive voltage by inserting a sensing resistor R_{sense} between the power switch source and the ground. The power switch peak current is compared with the level shifted control input voltage on a cycle−by−cycle basis. Figure 27 illustrated the internal blocks of the function. The PWM latch is initialized by the Oscillator set signal and is terminated by the current sense comparator when the current exceeds the value dictated by the control input or current limit level. The current sense Comparator Latch configuration used ensures that only a single pulse appears at the output during any given oscillator cycle.

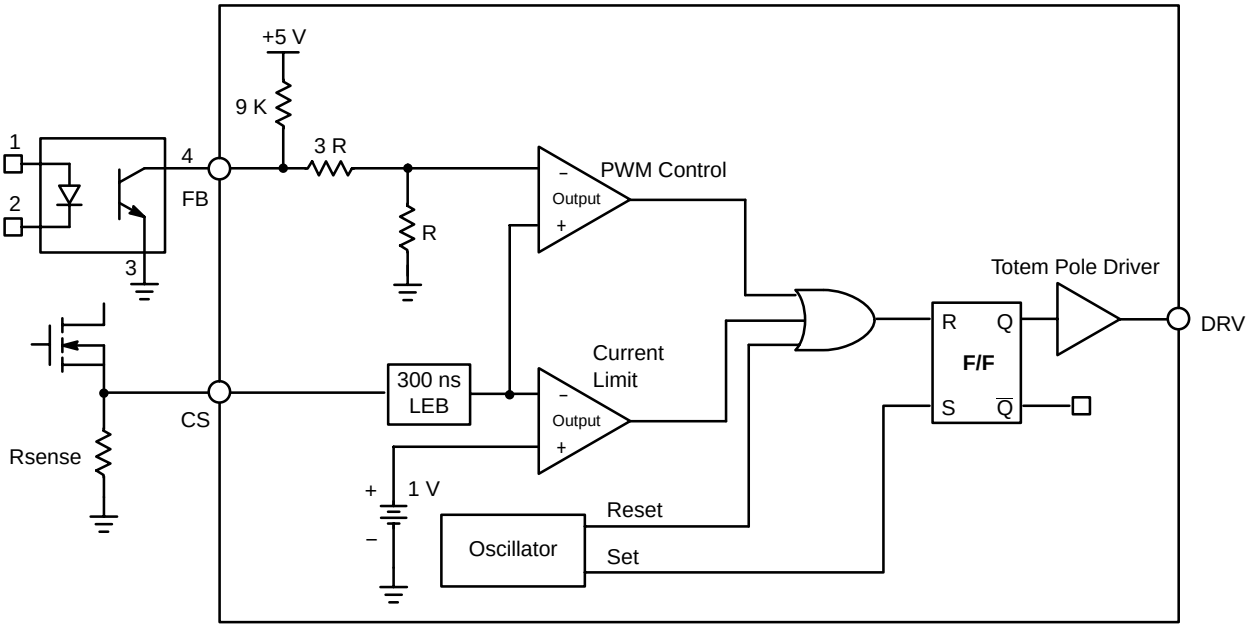


Figure 33. PWM Latch Function

Current Sense Section

The current sense pin, CS detects the voltage drop across a current sensing resistor, R_{sense} connected in between the power MOSFET and Ground. In most cases, a narrow spike on the leading edge of the current waveform can be observed and may cause the power supply to exhibit an instability when the output is lightly loaded. The spike is due to the power transformer inter−winding capacitance and output rectifier recovery time which are unavoidable. NCP1212 provides a 300 ns Leading Edge Blanking block to shield off the spike. With the Leading Edge Blanking function, the CS pin is not sensitive to the power switch turn−on noise and spikes, practically in most applications, no filtering network is required.

In normal operation, voltage developed at the current sense input is compared with the level shifted control input voltage and an internal Current Limit Threshold, V_{CS}. In case the CS input exceeds the Current Limit Threshold, which is 1.0 V (typ.) in NCP1212, the gate driver output will be forced to turn off immediately. Thus the maximum allowable peak current is given by the following equation:

$$I_{pk(max)} = \frac{1\ V}{R_{sense}}$$

Soft−Start and Maximum Duty Selection

NCP1212 includes an internal Soft−Start function to simplify designer's job hence make this device easy to use. During the start−up phase, a constant current source of 8.0 μA flows out of the SS/DMAX pin once V_{CC} attains the minimum startup voltage. The capacitor connected at SS/DMAX pin is slowly charged up and the voltage developed plus one diode drop, V_{SST} is compared with the saw−tooth waveform, C_T from the internal oscillator as shown in Figure 34. Whenever C_T voltage is higher than V_{SST}, gate driver output will be turned off. Since V_{SST} rises slowly and it controls the output duty gradually increases as shown in Figure 35. The minimum C_T voltage is at 1.0 V, hence there is no output before SS/DMAX pin attains about 0.4 V (1.0 V–1 diode drop). Soft−Start block will have no effect to the PWM operation once V_{SST} reaches 3.2 V.

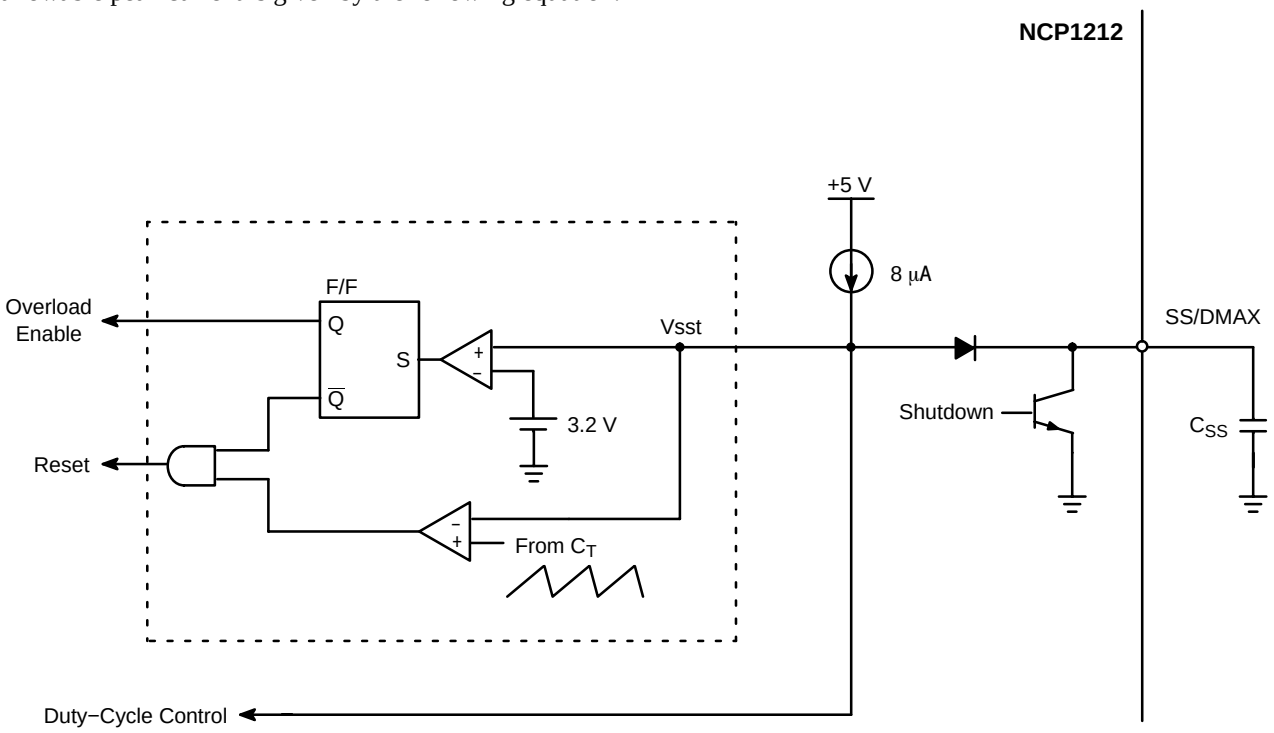


Figure 34. Soft−Start Operation

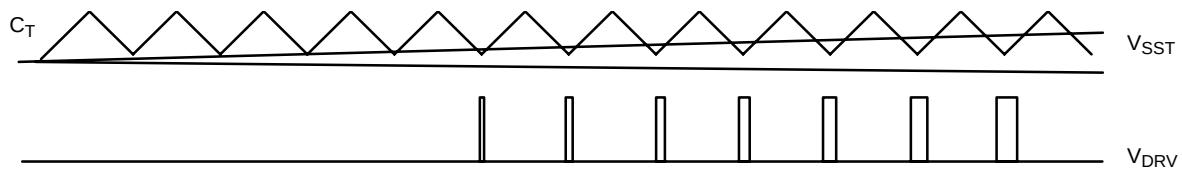


Figure 35. Output Pulse Duty−Cycle Depends on the SS/DMAX Pin Voltage

SS/DMAX pin is also used for the selection of maximum turn on Duty−Cycle. The oscillator circuit is designed to operate in either 82% or 48% charging time that corresponds to either 82% or 48% maximum PWM turn on Duty−Cycle. As discussed in the Oscillator Section, saw−tooth waveform at C_T pin is different for 82% and 48% maximum turn on Duty−Cycle and it is shown in Figure 32.

The final voltage at SS/DMAX pin determines the maximum turn on Duty−Cycle. If 82% maximum turn on duty is desired, simply connect a capacitor from SS/DMAX pin to ground as shown in Figure 36 and the final voltage on the capacitor will be 5.0 V minus one diode drop (~4.3 V).

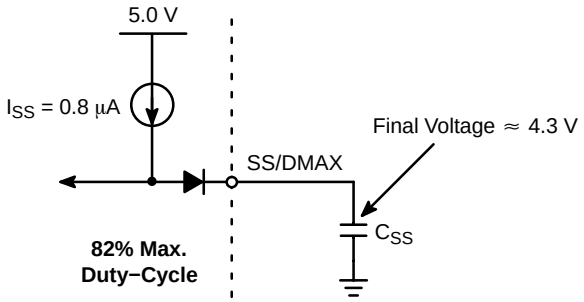


Figure 36. 82% Maximum Duty−Cycle Selection

For 48% maximum Duty−Cycle selection, we need to adjust the final voltage at SS/DMAX to lower than 3.2 V minus one diode drop (~2.5 V). This can be achieved by connecting a resistor in parallel with C_{SS} as shown in Figure 37. The value of this parallel resistor is given by the equation in below:

$$R_{duty} = \frac{2.5\ V}{8\ \mu A}$$

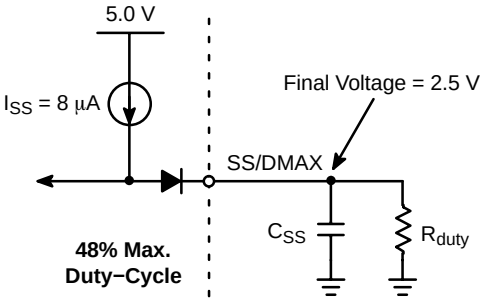


Figure 37. 48% Maximum Duty−Cycle Connection

Overload Detection

During output overload or short circuit condition, the PWM controller will pump as much energy as possible to the secondary side and the power only limited by the cycle−by−cycle current limit setting. Components in the power supply circuit such as the power MOSFET and output rectifier may be damaged by this continuous stress. Theoretically, fly−back converter has inherent short circuit protection provided that the PWM controller is supplied by a fly−back auxiliary winding and it has UVLO function. Unluckily, it is quite common that the supply will experience very high leaky voltage spike that prevents the V_{CC} voltage to fall below UVLO level during short circuit.

NCP1212 is equipped with an integrated overload detection mechanism, which is irrespective of auxiliary winding voltage level. Overload shutdown is no longer bothered by leakage spike hence a reliable overload protection system can be easily constructed by NCP1212 for both forward and fly−back configuration. Overload detection block is shown in Figure 38. Overload condition is signified by current sense voltage hitting the maximum allowable voltage, 1.0 V. To avoid false trigger that may happen during transient load changes, C_{SS} starts to discharge by 20 μA (I_{SD}−I_{SS}). If overload condition persists, V_{SST} voltage level drops to 0.5 V and triggers the overload shutdown. Overload shutdown is only enabled after the soft−start period**.**

Due to the overload detection mechanism, it is mandatory to connect a capacitor at the SS/DMAX pin. Otherwise overload shutdown may be triggered during startup phase.

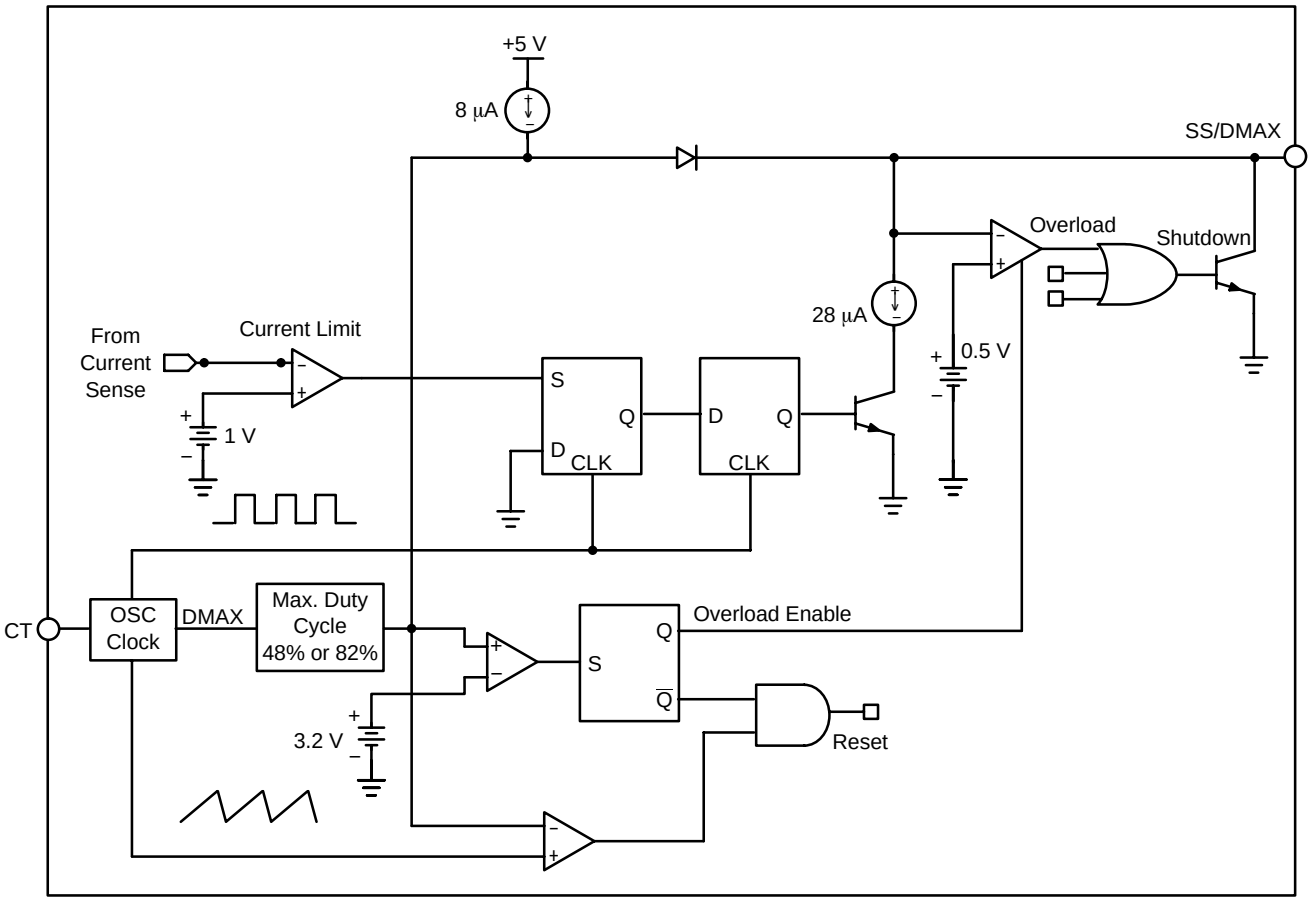


Figure 38. Overload Detection Block Diagram

Brownout Protection

NCP1212 has a built−in comparator for brownout detection as shown in Figure 39. Positive terminal of the comparator is connected to a +1.21 V bandgap reference. The IC is prohibited from switching until Brownout Detect pin exceeds 1.21 V. Once the brownout detect threshold is exceeded, 45 μA flows out of the pin and the voltage at this pin is further pushed up to provide hysteresis effect. The Brownout voltage setting is determined by the potential divider formed with R_{Upper} and R_{Lower}. Equations to calculate the resistors are shown below:

$$R_{Upper} + R_{Lower} = \frac{(V_{Bulk_H} - V_{Bulk_L})}{45\ \mu A}$$

$$R_{Lower} = \frac{[1.21\ V(V_{Bulk_H} - V_{Bulk_L})]}{(45\ \mu A \times V_{Bulk_H})}$$

Where V_{Bulk_H} and V_{Bulk_L} are the desired upper and lower bulk capacitor voltage for brownout detection.

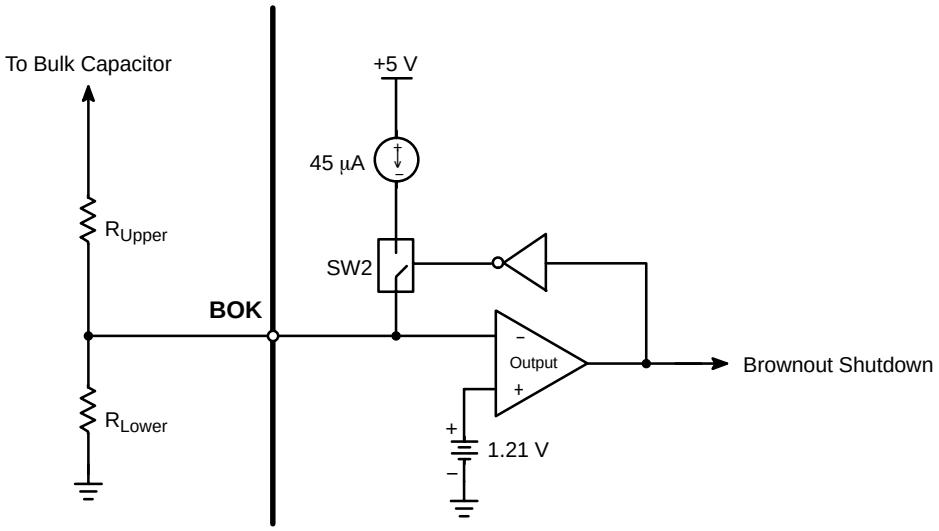


Figure 39. Brownout Detect Block Diagram

Internal 5.0 V Regulator

A low current 5.0 V regulator is available internally for the device operation and reference voltages generation. This voltage not accessible externally and is designed to operate with no external bypass capacitor.

Totem Pole Output Driver

NCP1212 contains a single totem pole output stage that was specifically designed for direct drive of power MOSFETs. It is capable of up to 300 mA peak drive current and has a typical rise time and fall time of 25 ns with 1.0 nF load.

Over Voltage Protection and Under Voltage Lockout

NCP1212 starts operation once V_{CC} reaches 15 V. Over Voltage Protection (OVP) will be triggered if V_{CC} exceeds 25 V and on the other hand, Under Voltage Lockout (UVLO) will take place if V_{CC} drops below 10 V. NCP1212 continues to draw 3.0 mA typical after overload or over voltage shutdown is triggered. If the startup resistance connected to V_{CC} pin is large enough such that V_{CC} voltage keeps on dropping after shutdown, NCP1212 will restart once V_{CC} drops below UVLO threshold. If the fault condition persists, NCP1212 will enter hi−cup operation. In case system latch−off is required in fault conditions, a smaller startup resistance can be used to sustain the device operation. NCP1212 will remain in shutdown mode as long as V_{CC} is maintained above UVLO threshold after fault is detected.

APPLICATION INFORMATION AND TYPICAL WAVEFORMS

The NCP1212 is an ideal choice for next generation isolated fix switching frequency forward mode converters that only need few external components to complete the system. Converting your existing application from using UC384X controllers to NCP1212 is easy and simple. In below is a description on how to determine external components value for a typical application example. For the schematic of the application, please refer to Figure 1 in this data sheet.

Finding the external component values can be broken down into several steps as introduced below:

1. Select the maximum duty−cycle for forward mode operation and calculate the Soft−Start time.

   Select the system, operate in forward mode with 82% maximum duty−cycle. Only a capacitor is required at SS/DMAX pin and the Soft−Start time is determined by the capacitor, C_{SS}. Its value is given by the equation below:

$$C_{SS} = \frac{I \times T_{SS}}{V_1 - V_2}$$

   where:

   I is an 8.0 μA constant current source flow out of the SS/DMAX pin;

   T_{SS} is the required Soft−Start time;

   V_1 is the Upper Threshold Voltage in the oscillator block and which is effectively controlling the PWM maximum duty−cycle at gate driver output. Soft−start block will have no effect to the PWM operation once SS/DMAX pin voltage reaches this threshold. This threshold voltage is 2.5 V with 48% maximum duty−cycle;

   V_2 is about 0.4 V (1.0 V minus one diode drop) which is the Lower Voltage Threshold for the PWM operation. There will be no PWM gate driver output before SS/DMAX pin voltage attains this threshold.

   For example, the required Soft−Start time is 50 ms, the timing capacitor, C_{SS} can be calculated as:

$$C_{SS} = \frac{8\ \mu A \times 50\ ms}{2.5\ V - 0.4\ V} = 0.182\ \mu F$$

   In this case, a 0.22 μF capacitor is used for this application and the Soft−Start time is calculated as 57.75 ms. The charging waveform at SS/DMAX pin is shown in Figure 40. From the captured waveform, the charge time from 0 V to 4.0 V is 115.2 ms and for the voltage charging up to 2.5 V, i.e. hitting the Upper Threshold Voltage, the elapsed time is about 70 ms that matched with the theoretical calculation closely.

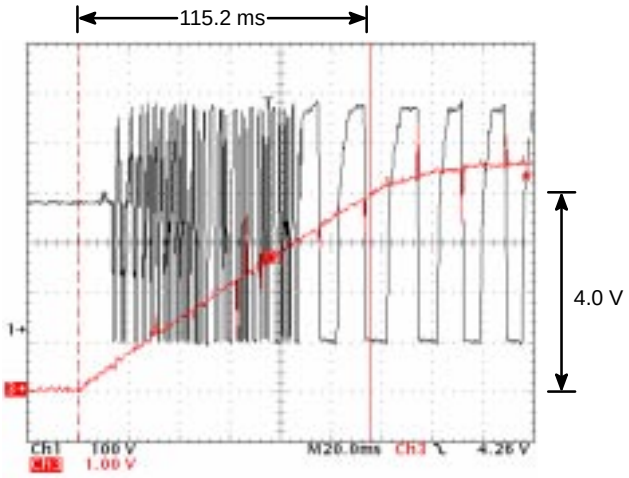


Figure 40. SS/DMAX Pin Charging Waveform

Overload condition is signified by current sense input voltage hitting the Maximum Current Sense Threshold, V_{CS}. To avoid false trigger that may happen during transient load change, C_{SS} starts to discharge by an internal current source of 20 μA, I_{SD}−I_{SS} and the overload protection will only be issued until the voltage at SS/DMAX pin falls below 0.5 V. The discharging time, T_{DIS} for 0.22 μF Soft−Start capacitor is given by:

$$T_{DIS} = \frac{C_{SS} \times (V_{ref} - V_D - V_{OL})}{I_{SD} - I_{SS}}$$

where:

C_{SS} is the Soft−Start timing capacitor;

V_{ref} is the internal reference voltage, 5.0 V typical;

V_D is the internal diode forward voltage on between the reference voltage and SS/DMAX pin in IC internal, is 0.6 V typical;

V_{OL} is the overload threshold voltage. Refer to Figure 39 Overload Detection Block Diagram, the over−load threshold voltage is 0.5 V typical;

$I_{SD}-I_{SS}$ is the internal current source for C_{SS} discharging, 20 μA typical.

The discharging time for 0.22 μF Soft−Start capacitor is:

$$T_{DIS} = \frac{0.22\ \mu F \times (5.0\ V - 0.6\ V - 0.5\ V)}{20\ \mu A} = 42.9\ ms$$

The discharging waveform on SS/DMAX pin is shown in Figure 41. The discharging time from 4.0 V to 0.6 V is measured as 36 ms from Figure 41. By interpolation, discharging time can be estimated as about 41.3 ms when output is overload which agreed with the calculated result.

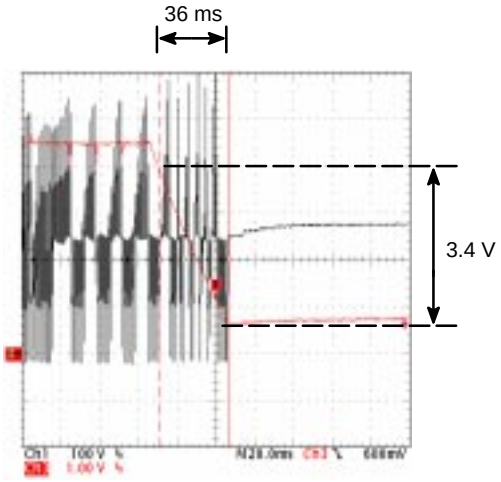


Figure 41. SS/DMAX Pin Discharging Waveform

2. Determine the PWM Switching Frequency

   The switching waveform is generated by the action of charging and discharging by internal current sources to a capacitor connected at C_T, pin 4. The relationship of the switching frequency and the value of C_T is governed by the equation below:

$$F_{SW} = \frac{I_{chg} \times D}{C_T \times (V_{th} - 1)}$$

   where:

   I_{chg} is the charging current to C_T, 278 μA typical;

   D is the selected Maximum Duty−Cycle, 48% or 82%;

   C_T is the capacitor connected to C_T pin;

   V_{th} is the threshold voltage for different Maximum Duty−Cycle selection, 2.5 V for 48% Maximum Duty−Cycle and 3.8 V for 82% Maximum Duty−Cycle.

The Switching Frequency against C_T is shown in Figure 31 to help the designers to determine the capacitance for their selected switching frequency.

3. Determine the BOK Thresholds

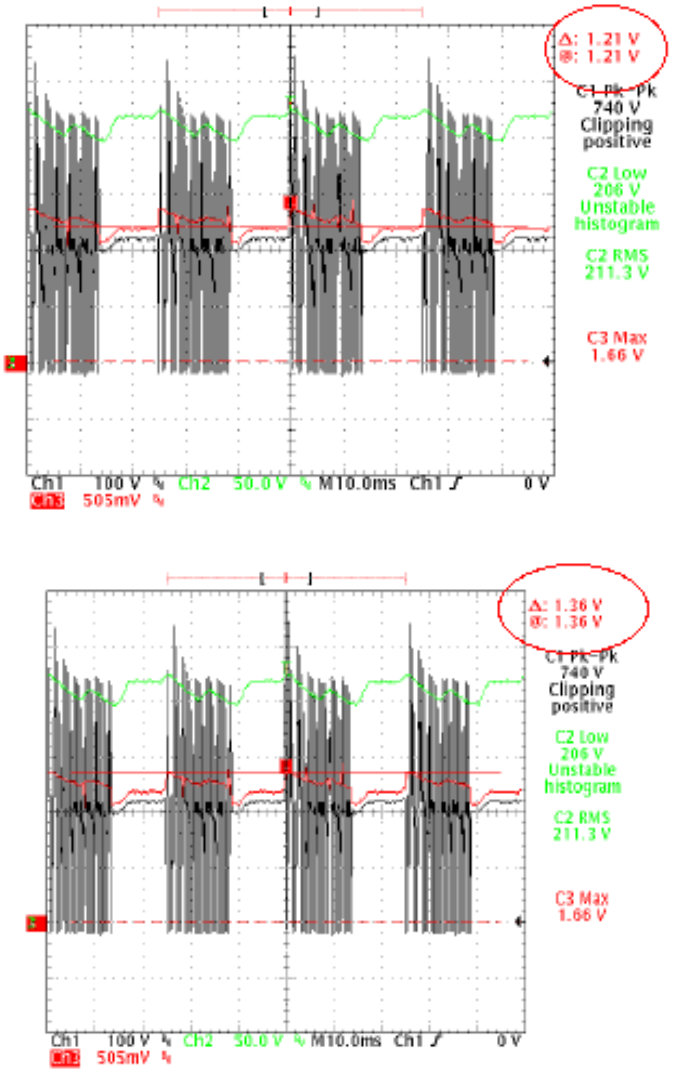
   Brownout detect thresholds are determined by a resistors network that monitors part of the bulk capacitor voltage at BOK pin. Equations below illustrate the calculation of the resistors value for the network.

$$R_{Upper} + R_{Lower} = \frac{(V_{Bulk_H} - V_{Bulk_L})}{45\ \mu A}$$

$$R_{Lower} = \frac{[1.21\ V(V_{Bulk_H} - V_{Bulk_L})]}{(45\ \mu A \times V_{Bulk_H})}$$

   Where V_{Bulk_H} and V_{Bulk_L} are the desired upper and lower bulk capacitor voltage for brownout detection.

   Assume V_{Bulk_H} = 212 Vdc and V_{Bulk_L} = 186 Vdc, select 3.3 kΩ for R_{Lower} then R_{Upper} can be calculated to be 576 kΩ.



Channel 1: The MOSFET's V_{DS} Switching Waveform
Channel 2: Primary Bulk Capacitor Voltage
Channel 3: BOK Pin Voltage

Figure 42. Brownout Detect Waveforms

Experimental results for the Brownout action were shown in Figure 42. From the captured waveforms, it can be noted that the Brownout Input Threshold Voltage is 1.21 V and Brownout Hysteresis Voltage is 1.36 V at BOK pin.

4. Improving Light Load and No Load Regulation for High Power Applications

   For high power applications, limited by the dynamic range of the control circuitry, i.e. the control feedback is limited by the swing of the optocoupler. When V_{FB} reaches about 0.1 V at light load conditions, it no longer has the means to further reduce that voltage because of the saturation of the optocoupler. At light load or no load conditions, the primary current is very small and as the current sensing resistor is also small for high power applications, the current sense feedback voltage will be much smaller than 0.1 V. Consequently, the control will force to acquire maximum duty−cycle operation and the output will increase without control.

   In order to improve the poor regulation at light load, a small circuit is added as shown in Figure 43. With the additional circuitry, when V_{FB} falls below 0.1 V, Q2 will drive additional offset current to CS pin and modify the current sensing voltage, V_{CS}. For V_{FB} higher than 0.1 V at normal load operation, Q2 will be turned off due to limited V_{be}.

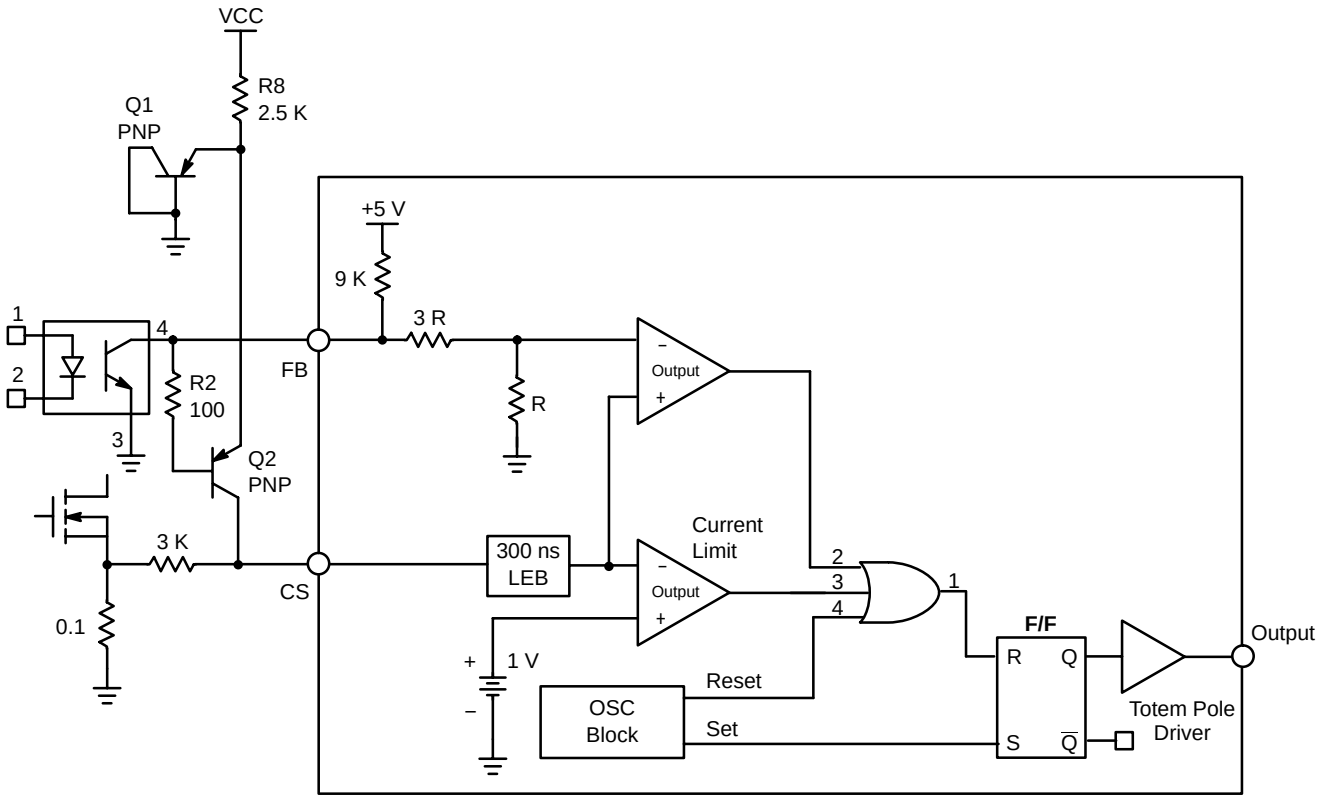


Figure 43. Suggested Solution for Better Light Load Regulation

The skip mode operation waveform at light load is shown in Figure 44. Where Channel 1 is the gate drive pin waveform and Channel 2 is the CS input pin waveform.

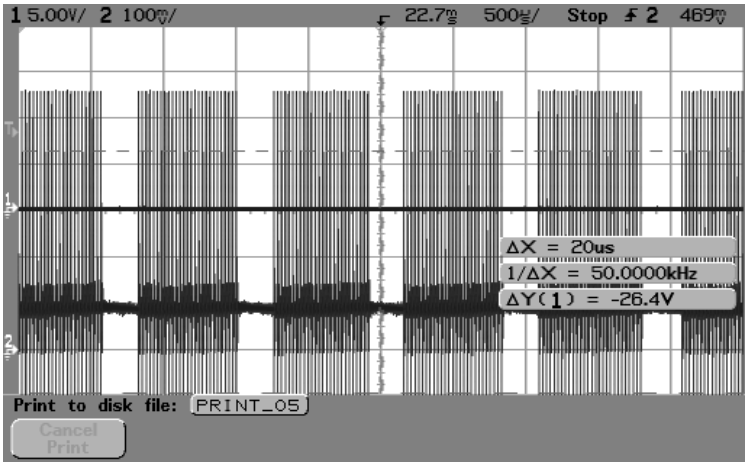
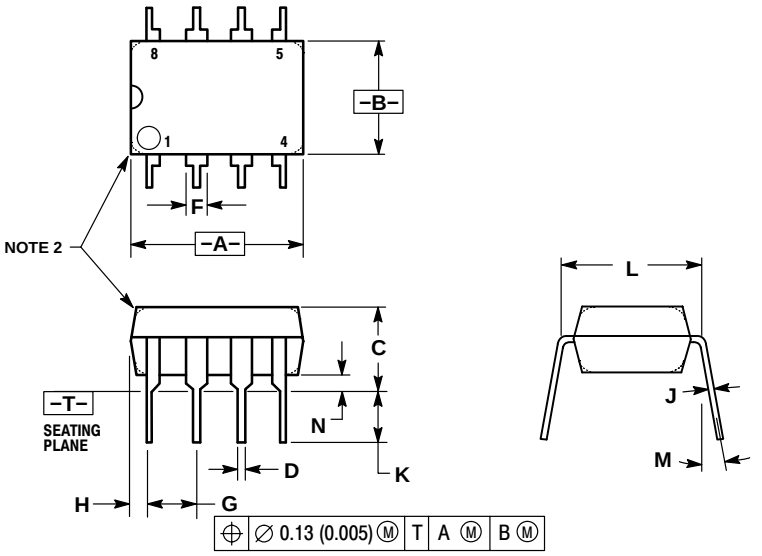


Figure 44. Skip Mode Switching Waveform at Light Load

PACKAGE DIMENSIONS

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CASE 626−05
ISSUE L

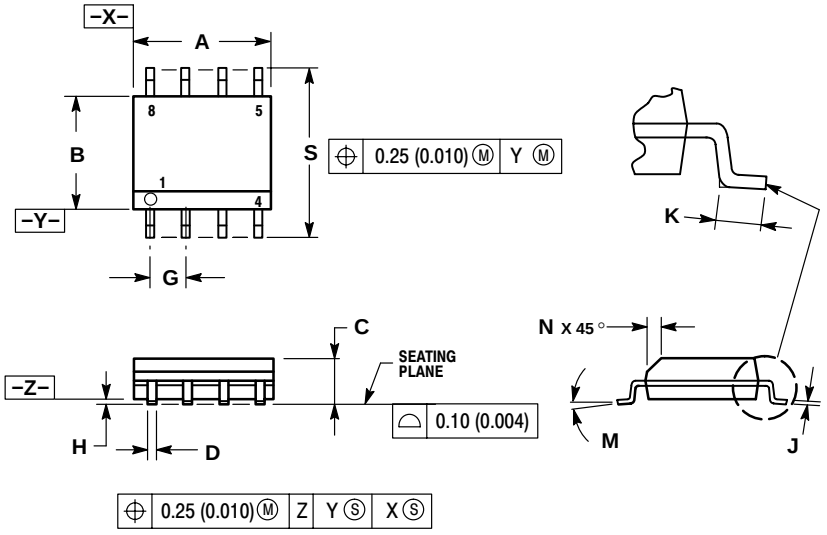


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3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.40	10.16	0.370	0.400
B	6.10	6.60	0.240	0.260
C	3.94	4.45	0.155	0.175
D	0.38	0.51	0.015	0.020
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	0.76	1.27	0.030	0.050
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	---	10°	---	10°
N	0.76	1.01	0.030	0.040

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SOIC−8
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	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

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