

P-Channel Enhancement Mode MOSFET

◆ DESCRIPTION

The MT3401 is the P-Channel logic enhancement mode power field effect transistor is produced using high cell density, DMOS trench technology.

This high-density process is especially tailored to minimize on-state resistance.

These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other Battery powered circuits, and low in-line power loss are needed in a very small outline surface mount package.

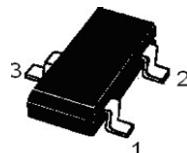
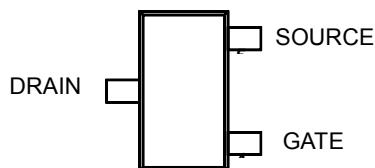
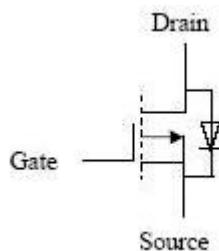
◆ FEATURES

- -30V/-4.0A, $R_{DS(ON)} = 58 \text{ m}\Omega$ @ $V_{GS} = -10\text{V}$
- -30V/-3.2A, $R_{DS(ON)} = 65 \text{ m}\Omega$ @ $V_{GS} = -4.5\text{V}$
- -30V/-1.2A, $R_{DS(ON)} = 85 \text{ m}\Omega$ @ $V_{GS} = -2.5\text{V}$
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability
- SOT-23-3L package design

◆ APPLICATIONS

- POWER Management in Note
- Portable Equipment
- Battery Powered System
- DC/DC Converter
- Load Switch
- DSC

◆ PIN CONFIGURATION



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◆ ABSOLUTE MAXIMUM RATINGS

($T_A=25^\circ\text{C}$ Unless Otherwise Noted)

Parameter	Symbol	Maximum	Unit
Drain-Source Voltage	V_{DS}	-30	V
Gate-Source Voltage	V_{GS}	± 12	V
Continuous Drain Current $T_A = 25^\circ\text{C}$	I_D	-4.0	A
$T_A = 70^\circ\text{C}$		-3.2	
Pulsed Drain Current	I_{DM}	-15	A
Continuous Source Current (Diode Conduction)	I_S	-1.0	A
Power Dissipation $T_A = 25^\circ\text{C}$	P_D	1.25	W
$T_A = 70^\circ\text{C}$		0.8	
Operating junction temperature range	T_J	150	$^\circ\text{C}$
Storage temperature range	T_{STG}	- 55 to 150	$^\circ\text{C}$

◆ THERMAL RESISTANCE RATINGS

Thermal Resistance	Symbol	Maximum	Unit
Junction-to-Ambient	$R_{\theta JA}$	120	$^\circ\text{C}/\text{W}$

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◆ ELECTRICAL CHARACTERISTICS

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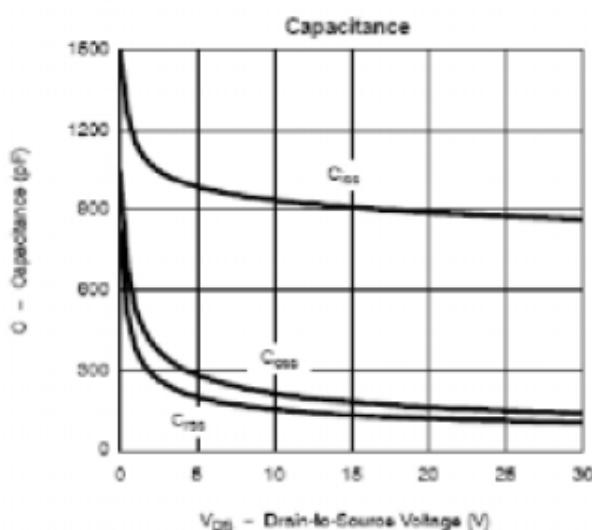
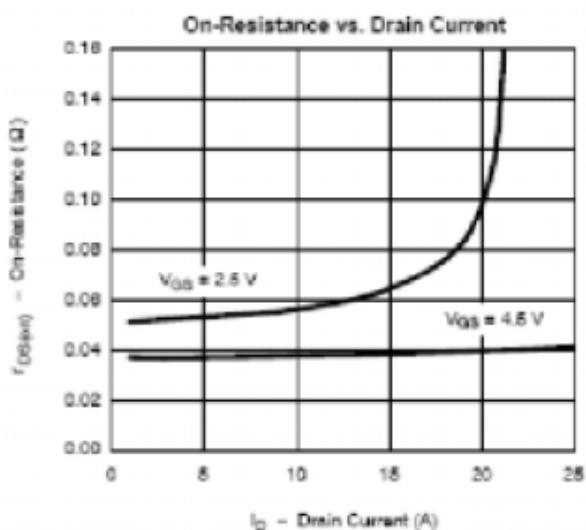
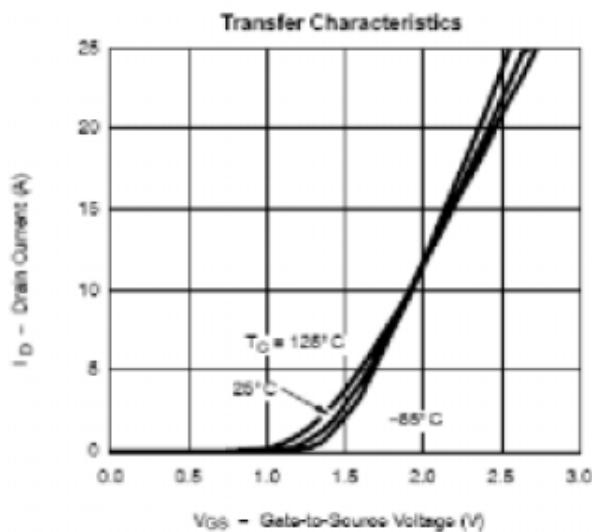
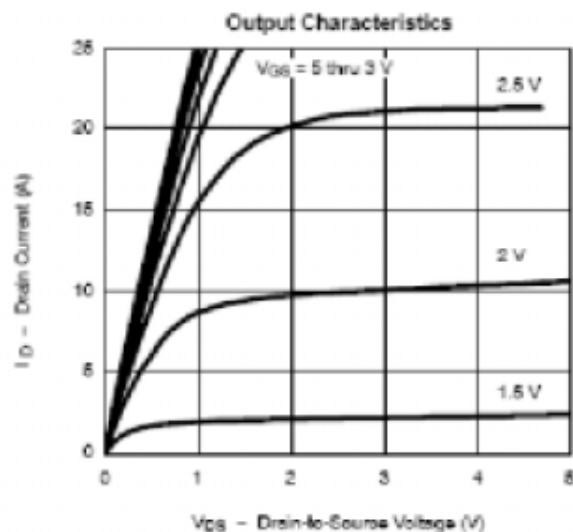
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static Parameters						
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0V, I _D = -250μA	-30	-	-	V
Gate Threshold Voltage	V _{GS(th)}	V _{GS} = V _{DS} , I _D = -250μA	-0.4	-	-1.2	V
Gate Current	I _{GSS}	V _{DS} = 0V, V _{GS} = ±12V	-	-	±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = -24V, V _{GS} = 0V	-	-	-1	μA
		V _{DS} = -24V, V _{GS} = 0V, T _J = 55 °C	-	-	-10	
Forward Trans conductance	g _{fs}	V _{DS} = -5V, I _D = -4.0A	-	10	-	S
On-State Drain Current	I _{D(ON)}	V _{DS} ≤ -5V, V _{GS} = -10V	-10	-	-	A
Drain-Source On Resistance	R _{DS(ON)}	V _{GS} = -10V, I _D = -4.0A	-	45	58	mΩ
		V _{GS} = -4.5V, I _D = -3.2A	-	50	65	
		V _{GS} = -2.5V, I _D = -1.2A	-	60	85	
Diode Forward Voltage	V _{SD}	I _S = -1.0A, V _{GS} = 0V	-	-0.8	-1.2	V
Dynamic Parameters						
Input Cap.	C _{iss}	V _{DS} = -15V, V _{GS} = 0V, F = 1MHz	-	540		pF
Output Cap.	C _{oss}		-	131		
Reverse Transfer Cap.	C _{rss}		-	105		
Total Gate Charge	Q _g	V _{DS} = -15V, V _{GS} = -10V I _D = -4.0A	-	14	21	nC
Gate-Source Charge	Q _{gs}		-	1.9		
Gate-Drain Charge	Q _{gd}		-	3.7		
Turn-On Time	T _{D(ON)}	V _{DS} = -15V, R _L = 15Ω, I _D = -1A, V _{GEN} = -10V, R _G = 6Ω	-	10	15	nS
	t _r		-	15	25	
Turn-Off Time	T _{D(OFF)}		-	31	50	
	T _f		-	20	30	



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◆ TYPICAL CHARACTERISTICS

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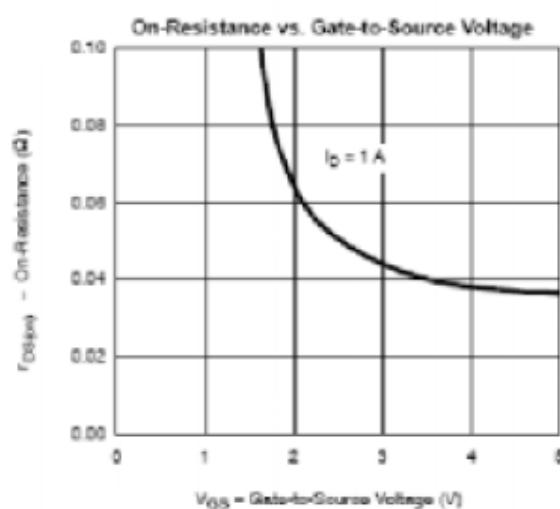
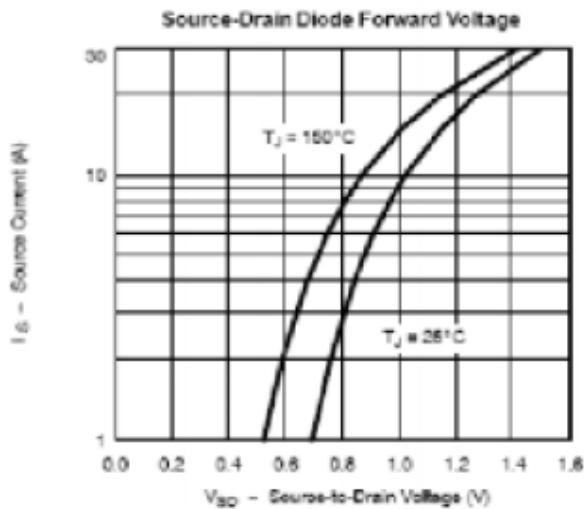
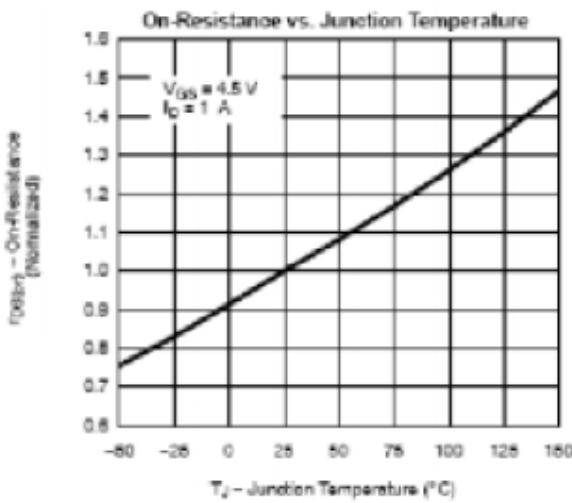
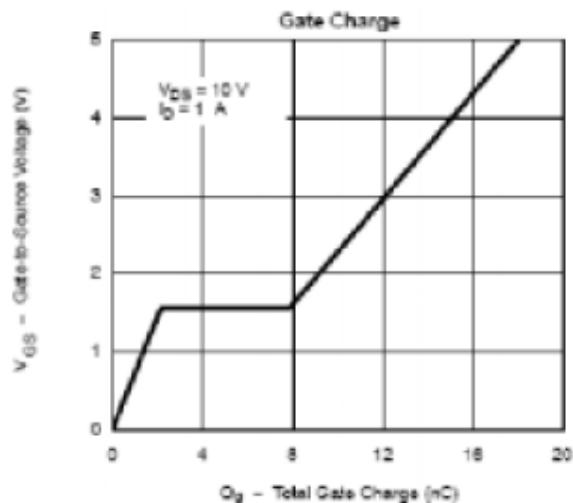




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◆ TYPICAL CHARACTERISTICS

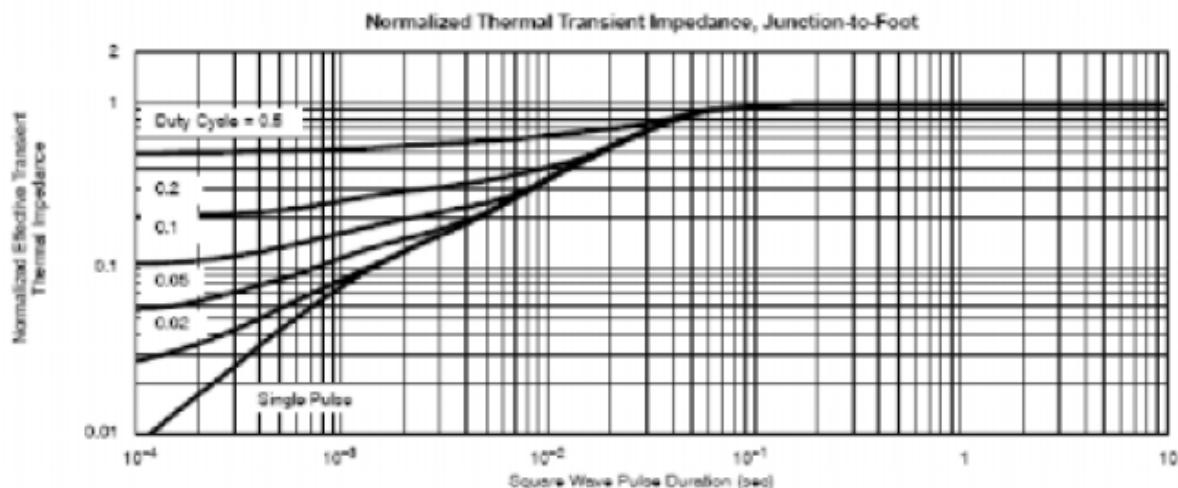
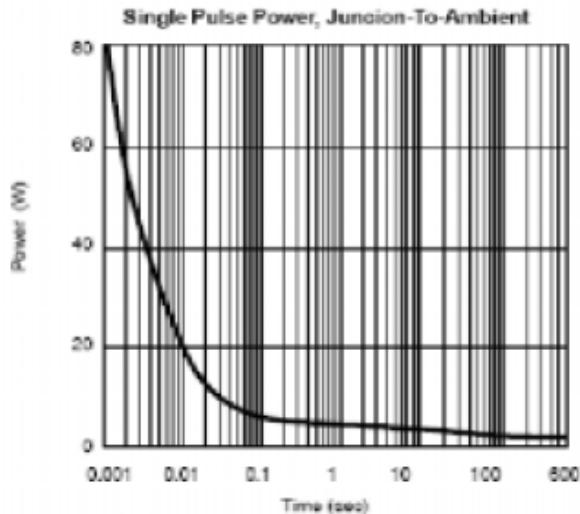
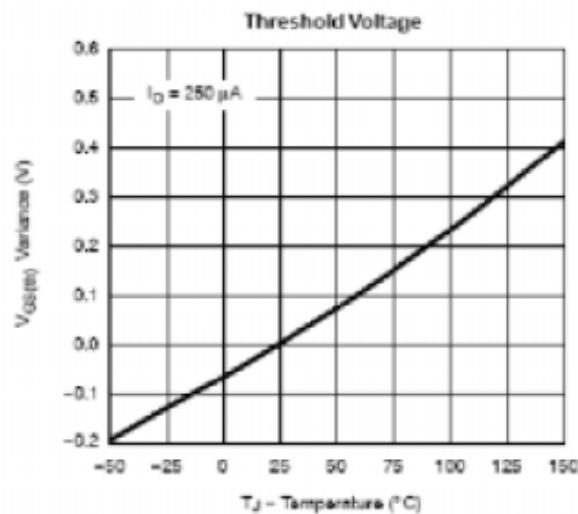
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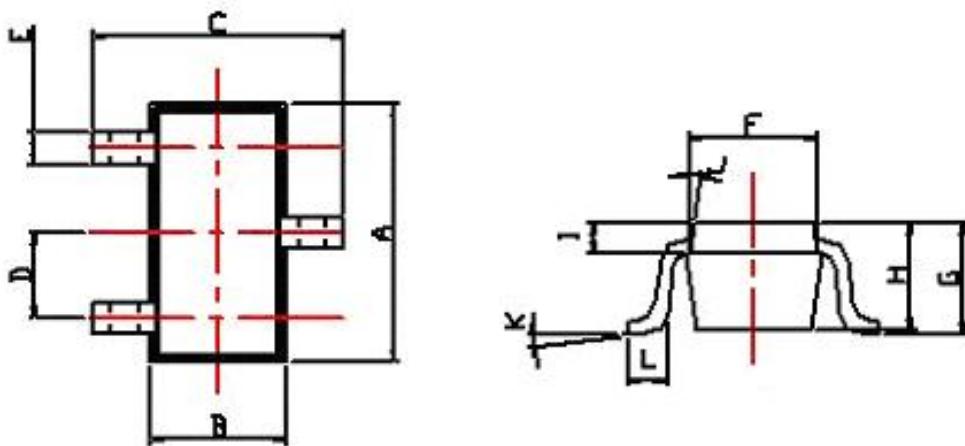
◆ TYPICAL CHARACTERISTICS

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**◆ PHYSICAL DIMENSIONS:**

3-Pin surface Mount SOT-23(S)



REF.	Millimeter		REF.	Millimeter	
	Min.	Max.		Min.	Max.
A	2.70	3.10	G	0.9	1.4
B	1.20	1.66	H	0.8	1.30
C	2.37	2.90	I	0.25	0.7
D	0.85	1.15	J	$7 \pm 2^\circ$.	
E	$0.350 + 0.15/-0.05$		K	$0 \sim 10^\circ$.	
F	1.07	1.53	L	0.2 (MIN)	