SANYO	8-BIT SINGLE CHIP MICROCONTROLLER
Preliminary	LC86F3548A

LC86F3548A

8-bit Single Chip Microcontroller with on-chip 64K-byte Flash Memory (ROM 48K -byte + CGROM 16K-byte), on-chip 640-byte RAM and 176 × 9 bit OSD RAM

Overview

The LC86F3548A is a CMOS 8-bit single chip microcontroller with flash memory for the LC863500 series.
This microcontroller contains the following on-chip functional blocks:

- CPU : Operable at a minimum bus cycle time of 0.424µs
- On-chip ROM capacity : 64K bytes Flash Memory
  - Program ROM : 48K bytes
  - CGROM : 16K bytes
- On-chip RAM capacity : 640 bytes
- OSD RAM : 176 × 9 bits
- On-screen display controller
- Four channels × 6-bit AD Converter
- Three channels × 7-bit PWM
- Two 16-bit timer/counters, 14-bit base timer
- IIC-bus compliant serial interface circuit (Multi-master type)
- ROM correction function
- 12-source 8-vectored interrupt system
- Integrated system clock generator and display clock generator
  - Only one X'tal oscillator (32.768kHz) for PLL reference is used for both generators

All of the above functions are fabricated on a single chip.
The program is rewritable by using the on-board writing system after the LSI has been installed on the application board.

Note : This product includes the IIC bus interface circuit. If you intend to use the IIC bus interface, please notify us of this in advance of our receiving your program ROM code order.
Purchase of SANYO IIC components conveys a license under the Philips IIC Patents Rights to use these components in an IIC system, provided that the system conforms to the IIC Standard Specification as defined by Philips.

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This catalog provides information as of February 2001. Specifications and information herein are subject to change without notice.

SANYO Electric Co., Ltd. Semiconductor Company
SYSTEM-LSI Div. System-Microcomputer Development Dep.
1-1-1, Sakata Oizumi-Machi, Gunma, JAPAN

Features

(1) Built-in Flash Memory :
64K bytes
- Program ROM 48K bytes
- Character ROM 16K bytes
- Rewritable in page units 128 bytes / page
- Page erase / program cycle 100 cycle per page

(2) Built-in Random Access Memory (RAM) : 640 × 8 bits (including 128 bytes for ROM correction function)
176 × 9 bits (for CRT display)

The LC86F3548A consists of 48K of ROM space and 640 bytes of RAM space. For this microcontroller, the usable program ROM capacity and RAM capacity are the same size for the mask ROM version.

Mask ROM versions compatible with the LC86F3548A	Program ROM limit set for the LC86F3548A	RAM limit set for the LC86F3548A (including 128 bytes for the ROM correction function)
LC863548	49152 bytes	640 bytes
LC863540	40960 bytes	640 bytes
LC863532	32768 bytes	512 bytes
LC863528	28672 bytes	512 bytes
LC863524	24576 bytes	512 bytes
LC863520	20480 bytes	512 bytes
LC863516	16384 bytes	512 bytes

When using on-board rewriting system is selected by the option, the rewriting program (loader program) is allocated in the last 2K-byte of the memory ,following to 46k-byte (B800h)

(3) OSD functions
- Screen display : 36 characters × 16 lines (by software)
- RAM : 176 words (9 bits per word)
  - Display area : 36 words × 4 lines
  - Control area : 8 words × 4 lines
- Characters
  - Up to 252 kinds of 16 × 32 dot character fonts
    (4 characters including 1 test character are not programmable)
  - Each font can be divided into two parts and used as two fonts (Ex. 16 × 16 dot font ×2)
- Various character attributes
  - Character colors : 16 colors (analog mode: lv_{p-p} output) / 8 colors (digital mode)
  - Character background colors : 16 colors (analog mode: lv_{p-p} output) / 8 colors (digital mode)
  - Fringe / shadow colors : 16 colors (analog mode: lv_{p-p} output) / 8 colors (digital mode)
  - Full screen colors : 16 colors (analog mode: lv_{p-p} output) / 8 colors (digital mode)
- Attribute can be changed without spacing
- Vertical display start line number can be set for each row independently (Rows can be overlapped)
- Horizontal display start position can be set for each row independently
- Horizontal pitch (bit 9 - 16)[*1] and vertical pitch (bit-32) can be set for each row independently
- Different display modes can be set for each row independently
  - Caption • Text mode / OSD mode 1 / OSD mode 2 (Quarter size) / Simplifed graphic mode
- Ten character sizes [*1]
  - Horiz. × Vert. = (1 × 1), (1 × 2), (2 × 2), (2 × 4), (0.5 × 0.5)
    (1.5 × 1), (1.5 × 2), (3 × 2), (3 × 4), (0.75 × 0.5)
- Shuttering and scrolling on each row
- Simplified Graphic Display

*1 Note : range depends on display mode : refer to the manual for details.

(4) Bus Cycle Time / Instruction-Cycle Time

Bus cycle time	Instruction cycle time	Clock divider	System clock oscillation	Oscillation Frequency	Voltage
0.424µs	0.848µs	1/2	Internal VCO	14.156MHz	4.5V to 5.5V
7.5µs	15.0µs	1/2	Internal RC	800kHz	4.5V to 5.5V
91.55µs	183.1µs	1/1	Crystal	32.768kHz	4.5V to 5.5V
183.1µs	366.2µs	1/2	Crystal	32.768kHz	4.5V to 5.5V

(5) Ports

- Input / Output Ports : 4 ports (24 terminals)
  Data direction programmable in nibble units : 1 port (8 terminals)
  (If the N-ch open drain output is selected by option, the corresponding port data can be read in output mode.)
  Data direction programmable for each bit individually : 3 ports (16 terminals)

(6) AD converter

4 channels × 6-bit AD converters

(7) Serial interfaces

- IIC-bus compliant serial interface (Multi-master type)
  Consists of a single built-in circuit with two I/O channels.
  The two data lines and two clock lines can be connected internally.

(8) PWM output

- 3 channels × 7-bit PWM

(9) Timer

- Timer 0 : 16-bit timer/counter
  With 2-bit prescaler + 8-bit programmable prescaler
  Mode 0 : Two 8-bit timers with a programmable prescaler
  Mode 1 : 8-bit timer with a programmable prescaler + 8-bit counter
  Mode 2 : 16-bit timer with a programmable prescaler
  Mode 3 : 16-bit counter
  The resolution of timer is 1 tCYC.
- Timer 1 : 16-bit timer/PWM
  Mode 0 : Two 8-bit timers
  Mode 1 : 8-bit timer + 8-bit PWM
  Mode 2 : 16-bit timer
  Mode 3 : Variable bit PWM (9 to 16 bits)
  In mode0/1,the resolution of Timer1/PWM is 1 tCYC
  In mode2/3,the resolution is selectable by program; tCYC or 1/2 tCYC
- Base timer
  Generate every 500ms overflow for a clock application (using 32.768kHz crystal oscillation for the base timer clock)
  Generate every 976µs, 3.9ms, 15.6ms, 62.5ms overflow (using 32.768kHz crystal oscillation for the base timer clock)
  Clock for the base timer is selectable from 32.768kHz crystal oscillation, system clock or programmable prescaler output of Timer 0

(10) Remote control receiver circuit (connected to the P73/INT3/T0IN terminal)

- Noise rejection function
- Polarity switching

(11) Watchdog timer

External RC circuit is required
Interrupt or system reset is activated when the timer overflows

(12) ROM correction function
Max 128 bytes / 2 addresses

(13) Interrupts
- 12 source 8 vectored interrupts
  1. External Interrupt INT0
  2. External Interrupt INT1
  3. External Interrupt INT2, Timer/counter T0L (Lower 8 bits)
  4. External Interrupt INT3, base timer
  5. Timer/counter T0H (Upper 8 bits)
  6. Timer T1H,T1L
  7. Vertical synchronous signal interrupt ($\overline{VS}$), scan line
  8. IIC
- Interrupt priority control

  Three interrupt priorities are supported (low, high and highest) and multi-level nesting is possible. Low or high priority can be assigned to the interrupts from 3 to 8 listed above. For the external interrupt INT0 and INT1, low or highest priority can be set.

(14) Sub-routine stack level
- A maximum of 128 levels (stack is built in the internal RAM)

(15) Multiplication/division instruction
- 16 bits × 8 bits (7 instruction cycle times)
- 16 bits / 8 bits (7 instruction cycle times)

(16) 3 oscillation circuits
- Built-in RC oscillation circuit used for the system clock
- Built-in VCO circuit used for the system clock and OSD
- X'tal oscillation circuit used for base timer, system clock and PLL reference

(17) Standby function
- HALT mode

  The HALT mode is used to reduce the power dissipation. In this operation mode, the program execution is stopped. This mode can be released by the interrupt request or the system reset.
- HOLD mode

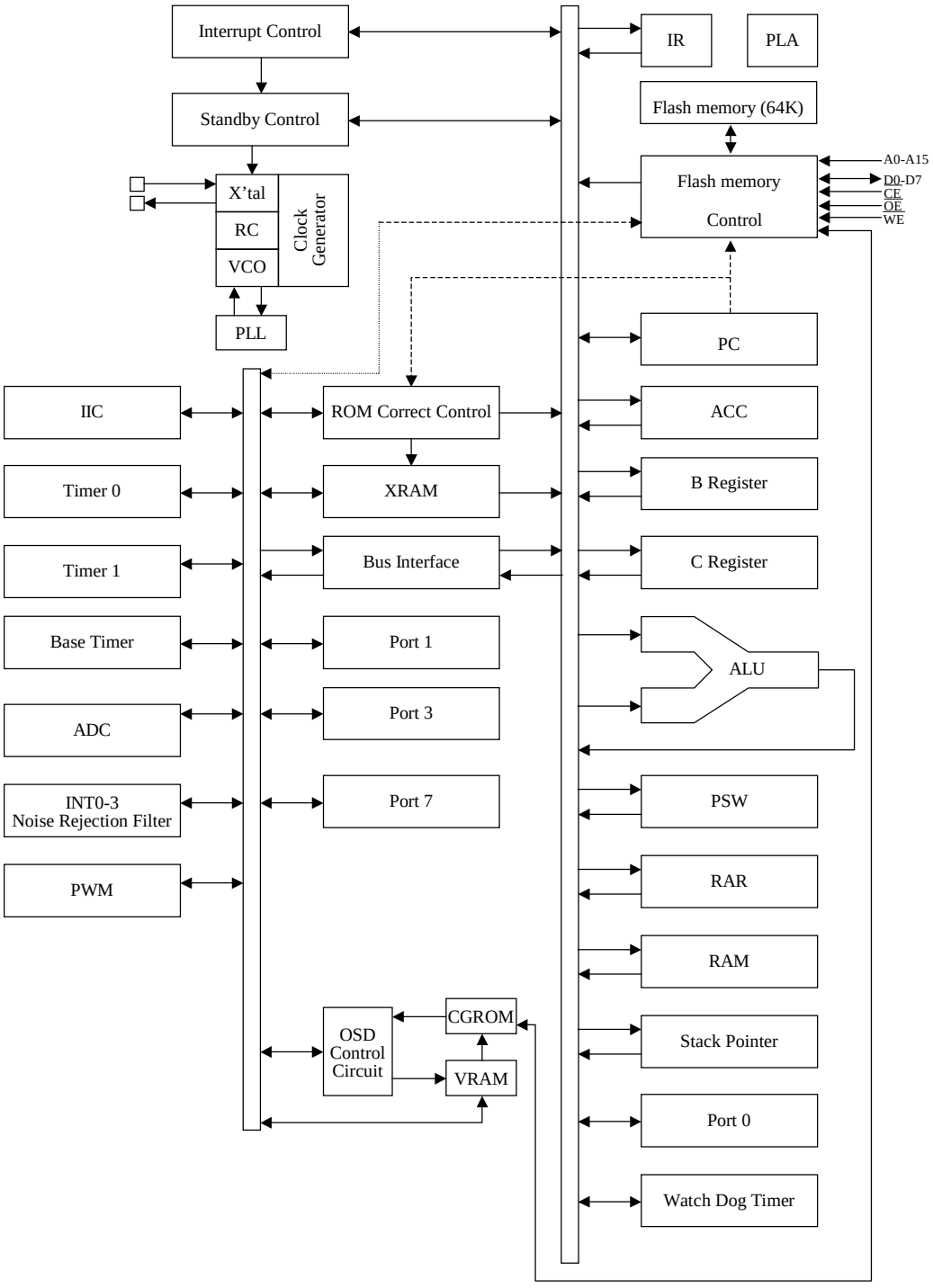
  The HOLD mode is used to stop the oscillations; RC (internal), VCO, and X'tal oscillations. This mode can be released by the following conditions.
  - Pull the reset terminal ($\overline{RES}$) to low level.
  - Feed the selected level to either P70/INT0 or P71/INT1.

(18) Package
- MFP36S
- DIP36S

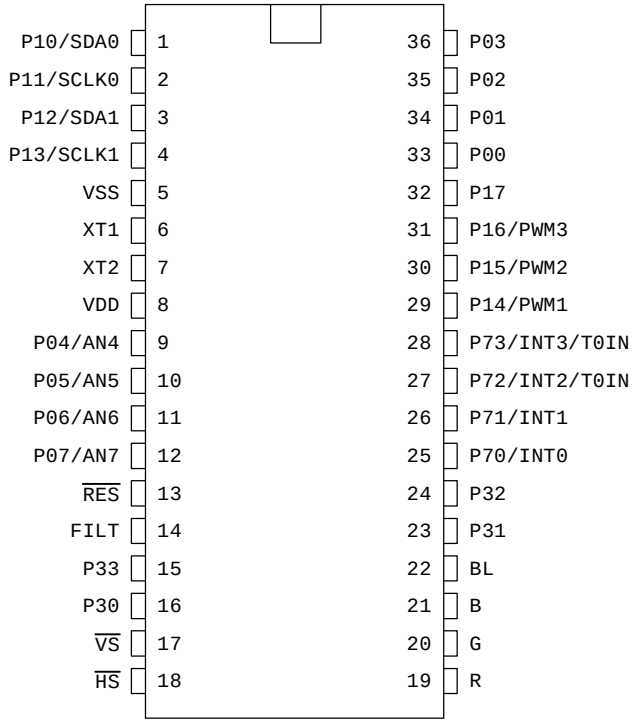
(19) Development tools
- Evaluation chip: LC863096
- Emulator: EVA86000 (main) + ECB863400 (evaluation chip board)
  + POD36-CABLE (cable)
  + POD36-DIP (for DIP36S)
  or POD36-MFP (for MFP36S)

Write Flash Memory
SANYO provides special services including writing data to Flash Memory and stamping.
There is a charge for these services.
Please feel free to ask our sales persons for details.

System Block Diagram



Pin Assignment



Pin Description

Pin Description Table

Terminal	I/O	Function Description	Option	Flash memory mode (Parallel input/ output mode)
VSS	-	Negative power supply		
XT1	I	Input terminal for crystal oscillator		
XT2	O	Output terminal for crystal oscillator		
VDD	-	Positive power supply		
$\overline{RES}$	I	Reset terminal		Input to set up mode
FILT	O	Filter terminal for PLL		
$\overline{VS}$	I	Vertical synchronization signal input terminal		Input to set up mode
$\overline{HS}$	I	Horizontal synchronization signal input terminal		
R	O	Red (R) output terminal of RGB image output		Address input A8
G	O	Green (G) output terminal of RGB image output		Address input A9
B	O	Blue (B) output terminal of RGB image output		Address input A10
BL	O	Fast blanking control signal Switch TV image signal and OSD image signal		Address input A11
Port 0 P00 - P07	I/O	•8-bit input/output port, Input/output can be specified in nibble unit •Other functions Interrupt input	Pull-up resistor provided/not provided Output Format CMOS/Nch-OD	Address input A0 to A7
Port 1 P10 - P17	I/O	•8-bit input/output port Input/output can be specified in a bit (programmable pull-up resister provided) •Other functions P10: IIC0 data I/O P11: IIC0 clock output P12: IIC1 data I/O P13: IIC1 clock output P14: PWM1 output P15: PWM2 output P16: PWM3 output P17: Timer1 (PWM) output	Output Format CMOS/Nch-OD	Data input/output D0 to D7
Port 3 P30 – P33	I/O	•4-bit input/output port Input/output can be specified in a bit (CMOS output/input with programmable pull-up resister)		control signal $\overline{WE}$ control signal $\overline{OE}$ control signal $\overline{CE}$

<table>
<tr><th>Terminal</th><th>I/O</th><th>Function Description</th><th>Option</th></tr>
<tr><td>Port 7
P70
P71 - P73</td><td>I/O</td><td>•4-bit input/output port
Input or output can be specified for each bit
P70: I/O provided programmable pull-up resister
P71 to P73: CMOS output/input with programmable pull-up resister
•Other function
<table>
<tr><td>P70</td><td>INT0 input/HOLD release input/
Nch-Tr. output for watchdog timer</td></tr>
<tr><td>P71</td><td>INT1 input/HOLD release input</td></tr>
<tr><td>P72</td><td>INT2 input/Timer 0 event input</td></tr>
<tr><td>P73</td><td>INT3 input (noise rejection filter connected)/
Timer 0 event input</td></tr>
</table>
Interrupt receiver format, vector addresses
<table>
<tr><th></th><th>rising</th><th>falling</th><th>rising/
falling</th><th>H level</th><th>L level</th><th>vector</th></tr>
<tr><td>INT0</td><td>enable</td><td>enable</td><td>disable</td><td>enable</td><td>enable</td><td>03H</td></tr>
<tr><td>INT1</td><td>enable</td><td>enable</td><td>disable</td><td>enable</td><td>enable</td><td>0BH</td></tr>
<tr><td>INT2</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td><td>13H</td></tr>
<tr><td>INT3</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td><td>1BH</td></tr>
</table></td><td>Address input
A12 to A15</td></tr>
</table>

Note: A capacitor of at least 10μF must be inserted between VDD and VSS when using this IC.

- Output form and existence of pull-up resistor for all ports can be specified for each bit.
- Programmable pull-up resistor is always connected regardless of port option, CMOS or N-ch open drain output in port 1.

User options

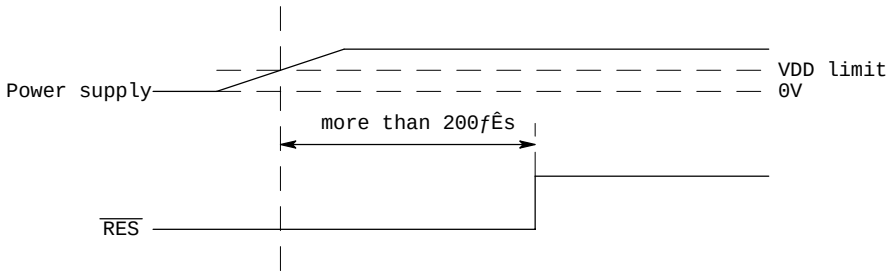
User options can be changed using Flash Memory data.

A kind of option	Pin, Circuits	
Input/output form of input/output ports	Port 0 (Specified in a bit)	1. Input : Without pull-up MOS Tr. Output : N-channel open drain 2. Input : With pull-up MOS Tr. Output : CMOS
	Port 1 (Specified in a bit)	1. Input : With programmable pull-up MOS Tr. Output : N-channel open drain 2. Input : With programmable pull-up MOS Tr. Output : CMOS

Notice for use

- Input level of terminal $\overline{\text{RES}}$ at power on

  Terminal $\overline{\text{RES}}$ must be held low for at least 200µs after the supply voltage exceeds the power supply lower limit.



-difference between the Mask version and Flash version(LC86F3548A)

1. the operation after release of reset : the mask version operates the program from the address 0 in the program counter as soon as detecting the H level on the reset port. the flash version operates the program from the address 0 in the program counter after setting the option.
2. Current dissipation : The current dissipation of the flash version is bigger than that of the mask version. please refer to the latest semiconductor news.

- Conditions during reset and after release of reset

  Port options are set using Flash Memory data.

  Port options are set internally within approximately 3ms after logic HIGH is applied to the RESET terminal. The configuration of the port outputs change over the duration of this period. Then the Program Counter is set to 0 and program execution begins.

  During reset, and in the few hundred milliseconds after reset is released, the port options on certain of the ports will not yet have been set. The conditions of the various ports during reset or on release of reset have been collected in the following table. Please refer to it when analyzing circuits where these conditions apply.

Pins	Options	Condition during and on release of reset
P0	Input : Without pull up MOS transistor Output : N-channel open drain	Output -off Input mode : High impedance
	Input : With pull up MOS transistor Output : CMOS	Output-off Flash version: During reset and in the first few hundred µs after reset is released, the pull-up MOS transistor is OFF. Thereafter, set to input mode with pull-up MOS Tr. ON Mask version: During reset the pull-up MOS transistor is OFF. After soon, set to input mode with pull-up MOS Tr. ON
P1	Input : With programmable pull up MOS transistor Output : N-channel open drain	Output-off Input mode : High impedance
	Input : With programmable pull up MOS transistor Output : CMOS	
P3	No options Input : With programmable pull up MOS transistor Output : CMOS	Output -off Input mode : High impedance
P7	No options Input : With programmable pull up MOS transistor Output : With pull up MOS (P70) CMOS (P71 - P73)	Output-off Input mode : High impedance

On-board writing system

The LC86F3548A has the On-board writing system. The program is renewable by using SANYO Flash On-board
System after the LSI has been installed on the application board.
This system is composed of 4 types divided by the combination of mode setting pin and communication pin.
Each type system has to connect the 6 pins (VDD,VSS,RES, communication pins) with the interface board of SANYO Flash On-board system.
It is necessary that the pins to be used for the rewriting system should be able to be separated from the application board properly.
The system type is selected by the option setting program (Su86K.exe).

types	mode setting pin	communication pins
type1	RES pin (high voltage(12V) applied)	P30(DATA1),P31(DATA0),P32(CLK)
type2	RES pin (high voltage(12V) applied)	P30(DATA1),P11(DATA0),P10(CLK)
type3	P30 pin (High level voltage (5V)applied)	P30(ENA/DATA1),P31(DATA0),P32(CLK)
type4	P30 pin (High level voltage (5V)applied)	P30(ENA/DATA1),P11(DATA0),P10(CLK)

- Type 3 or 4 is selected : P30 is exclusive for the on-board system. This pin must always be pulled-down, so this pin can't be used for other applications.

- The loader program must be written into the ROM to use On-board writing system.
  The loader program should be written into the ROM before the LSI has been installed on the board by the the general purpose ROM programs.
  When the option setting selects the this system to use, the loader program automatically links on the user program linking.

Please ask to our sales persons before using On-board writing system.

Use of PROM Conversion board

When reading or writing data to the LC86F3548A using our exclusive conversion board (W86F3448D, W86F3448M) general purpose PROM programs can be used.

(1) Name of conversion boards
- W86F3448D • • • DIP36S purpose
- W86F3448M • • • MFP36S purpose

(2) Available PROM programmers

The LC86F3548A does not support a silicon signature feature. Do not use the feature (automatic device type selection) when programming this device. To avoid erasing the program, confirm the setting of the protection for written program is active before using .

Single word write

Manufacture	Name of device	version	applicable device (code)	Data protection setting after write operation
Minato Electronics	MODEL 1890A + OU-910	V4.1	SST Co., Ltd. 29EE512 (D617)	Protected
Ando	AF-9708	01.00	SST Co., Ltd. 29EE512 (47100)	Protected
Data I. O.	ChipLab	V5.3	SST Co., Ltd. 29EE512	Selectable

Write multiple words

Manufacture	Name of device	version	applicable device (code)	Data protection setting after write operation
Minato Electronics	MODEL 1892 + TYPE9102A	V4.1	SST Co., Ltd. 29EE512 (D617)	Protected

(3) Notes

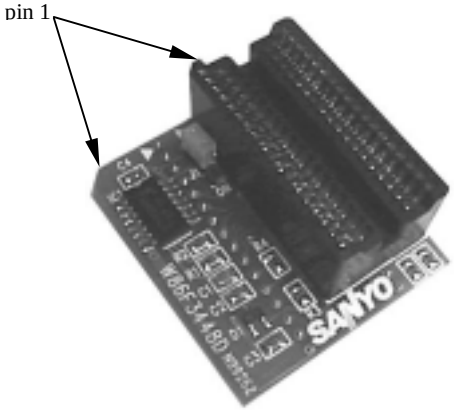
When using the conversion board, all of the jumper SW must be set to the OFF position. If set to the ON position, read/write operations will not perform correctly.

(4) Location of pin 1

Pin 1 of the conversion board should be located as indicated below.

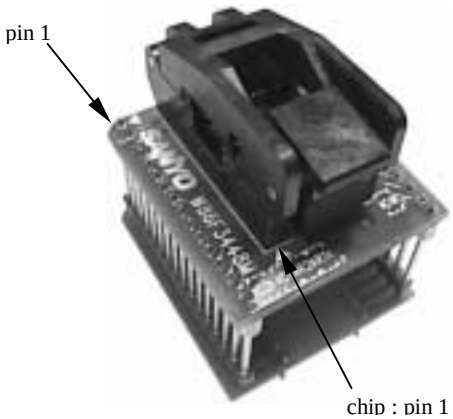
W86F3448D : when viewing from the edge closest to jumper SW, pin 1 is located on the upper left of both the chip and conversion board.

W86F3448M : when viewing from the edge closest to jumper SW, pin 1 of the chip is located on the lower left while pin 1 of the conversion board is located on the upper left.



Set jumper SW to OFF

W86F3448D



Set jumper SW to OFF

W86F3448M

1. Absolute maximum ratings / VSS=0V and Ta=25°C

Parameter		Symbol	Pins	Conditions	Limits				
					VDD[V]	min.	typ.	max.	unit
Supply voltage		VDDMAX	VDD			-0.3		+6.0	V
Input voltage		VI(1)	• $\overline{RES}$, $\overline{HS}$, $\overline{VS}$			-0.3		VDD+0.3	
Output voltage		VO(1)	R, G, B, BL, FILT			-0.3		VDD+0.3	
Input/output voltage		VIO	•Ports 0, 1, 3, 7			-0.3		VDD+0.3	
High level output current	Peak output current	IOPH(1)	•Ports 0, 1, 3, 7	•CMOS output •For each pin.		-4			mA
		IOPH(2)	R, G, B, BL	•CMOS output •For each pin.		-5			
	Total output current	∑IOAH(1)	•Ports 0, 1	The total of all pins.		-20			
		∑IOAH(2)	Ports 3,7	The total of all pins.		-10			
		∑IOAH(3)	R, G, B, BL	The total of all pins.		-12			
Low level output current	Peak output current	IOPL(1)	Ports 0, 1, 3,7	For each pin.				20	
		IOPL(2)	Port 7	For each pin.				15	
		IOPL(3)	R, G, B, BL	For each pin.				5	
	Total output current	∑IOAL(1)	Ports 0, 1	The total of all pins.				40	
		∑IOAL(2)	Ports 3, 7	The total of all pins.				30	
		∑IOAL(3)	R, G, B, BL	The total of all pins.				15	
Maximum power dissipation		Pdmax	MFP36S	Ta=-10 to +70°C				380	mW
			DIP36S					560	
Operating temperature range		Topg				-10		+70	℃
Storage temperature range		Tstg				-55		+125	

2. Recommended operating range / Ta=-10°C to +70°C, VSS=0V

Parameter	Symbol	Pins	Conditions	Limits				
				VDD[V]	min.	typ.	max.	unit
Operating supply voltage range	VDD(1)	VDD	0.844µs ≤ tCYC ≤ 0.852µs		4.5		5.5	V
	VDD(2)		4µs ≤ tCYC ≤ 400µs		4.5		5.5	
Hold voltage	VHD	VDD	RAMs and the registers data are kept in HOLD mode.		2.0		5.5	
High level input voltage	VIH(1)	Port 0	Output disable	4.5 - 5.5	0.6VDD		VDD	
	VIH(2)	•Ports 1,3 (Schumitt) •Port 7 (Schumitt) port input/interrupt • $\overline{HS}$, $\overline{VS}$, $\overline{RES}$ (Schumitt)	Output disable	4.5 - 5.5	0.75VDD		VDD	
	VIH(3)	Port 70 Watchdog timer input	Output disable	4.5 - 5.5	VDD-0.5		VDD	
Low level input voltage	VIL(1)	Port 0 (Schumitt)	Output disable	4.5 - 5.5	VSS		0.2VDD	
	VIL(2)	•Ports 1,3 (Schumitt) •Port 7 (Schumitt) port input/interrupt • $\overline{HS}$, $\overline{VS}$, $\overline{RES}$ (Schumitt)	Output disable	4.5 - 5.5	VSS		0.25VDD	
	VIL(3)	Port 70 Watchdog timer input	Output disable	4.5 - 5.5	VSS		0.6VDD	
Operation cycle time	tCYC(1)		•All functions operating	4.5 - 5.5	0.844	0.848	0.852	µs
	tCYC(2)		•AD converter operating •OSD is not operating	4.5 - 5.5	0.844		30	
	tCYC(3)		•OSD and AD converter are not operating	4.5 - 5.5	0.844		400	
Oscillation frequency range	FmRC		Internal RC oscillation	4.5 - 5.5	0.4	0.8	3.0	MHz

3. Electrical characteristics / Ta=-10°C to +70°C, VSS=0V

Parameter	Symbol	Pins	Conditions	Limits				
				VDD[V]	min.	typ.	max.	unit
High level input current	IIH(1)	Ports 0, 1, 3, 7	•Output disable •Pull-up MOS Tr. OFF •VIN=VDD (including the off-leak current of the output Tr.)	4.5 - 5.5			1	µA
	IIH(2)	• $\overline{RES}$ • $\overline{HS}$, $\overline{VS}$	•VIN=VDD	4.5 - 5.5			1	
Low level input current	IIL(1)	Ports 0, 1, 3, 7	•Output disable •Pull-up MOS Tr. OFF •VIN=VSS (including the off-leak current of the output Tr.)	4.5 - 5.5	-1			
	IIL(2)	• $\overline{RES}$ • $\overline{HS}$, $\overline{VS}$	VIN=VSS	4.5 - 5.5	-1			
High level output voltage	VOH(1)	•CMOS output of ports 0, 1, 3, 71 - 73	IOH=-1.0mA	4.5 - 5.5	VDD-1			V
	VOH(2)	R, G, B, BL	IOH=-0.1mA RGB: digital mode	4.5 - 5.5	VDD-0.5			
Low level output voltage	VOL(1)	Ports 0, 1, 3, 71 - 73	IOL=10mA	4.5 - 5.5			1.5	
	VOL(2)	Ports 0, 3, 71 - 73	IOL=1.6mA	4.5 - 5.5			0.4	
	VOL(3)	•R, G, B, BL •Port 1	IOL=3.0mA RGB: digital mode	4.5 - 5.5			0.4	
	VOL(4)	Port 70	IOL=1mA	4.5 - 5.5			0.4	
Pull-up MOS Tr. resistance	Rpu	•Ports 0, 1, 3, 7	VOH=0.9VDD	4.5 - 5.5	13	38	80	kΩ
Bus terminal short circuit resistance (SCL0-SCL1, SDA0-SDA1)	RBS	•P10-12 •P11-13		4.5 - 5.5			130	Ω
Hysteresis voltage	VHIS	•Ports 1, 3, 7 • $\overline{RES}$ • $\overline{HS}$, $\overline{VS}$	Output disable	4.5 - 5.5		0.1VDD		V
Pin capacitance	CP	All pins	•f=1MHz •Every other terminals are connected to VSS. •Ta=25°C	4.5 - 5.5		10		pF

4. IIC input/output conditions / Ta=-10°C to +70°C, VSS=0V

Parameter	Symbol	Standard		High speed		unit
		min.	max.	min.	max.	
SCL Frequency	fSCL	0	100	0	400	kHz
BUS free time between stop - start	tBUF	4.7	-	1.3	-	µs
HOLD time of start, restart condition	tHD;STA	4.0	-	0.6	-	µs
L time of SCL	tLOW	4.7	-	1.3	-	µs
H time of SCL	tHIGH	4.0	-	0.6	-	µs
Set-up time of restart condition	tSU;STA	4.7	-	0.6	-	µs
HOLD time of SDA	tHD;DAT	0	-	0	0.9	µs
Set-up time of SDA	tSU;DAT	250	-	100	-	ns
Rising time of SDA, SCL	tR	-	1000	20+0.1Cb	300	ns
Falling time of SDA, SCL	tF	-	300	20+0.1Cb	300	ns
Set-up time of stop condition	tSU;STO	4.0	-	0.6	-	µs

Refer to figure 7

(Note) Cb : Total capacitance of all BUS (unit : pF)

5. Pulse input conditions / Ta=-10°C to +70°C, VSS=0V

Parameter	Symbol	Pins	Conditions	Limits				
				VDD[V]	min.	typ.	max.	unit
High/low level pulse width	tPIH(1) tPIL(1)	•INT0, INT1 •INT2/T0IN	•Interrupt acceptable •Timer0-countable	4.5 - 5.5	1			tCYC
	tPIH(2) tPIL(2)	INT3/T0IN (1 tCYC is selected for noise rejection clock.)	•Interrupt acceptable •Timer0-countable	4.5 - 5.5	2			
	tPIH(3) tPIL(3)	INT3/T0IN (16 tCYC is selected for noise rejection clock.)	•Interrupt acceptable •Timer0-countable	4.5 - 5.5	32			
	tPIH(4) tPIL(4)	INT3/T0IN (64 tCYC is selected for noise rejection clock.)	•Interrupt acceptable •Timer0-countable	4.5 - 5.5	128			
	tPIL(5)	$\overline{RES}$	Reset acceptable	4.5 - 5.5	200			µs
	tPIH(6) tPIL(6)	$\overline{HS}$, $\overline{VS}$	•Display position controllable (Note) •The active edge of $\overline{HS}$ and $\overline{VS}$ must be apart at least 1 tCYC. •Refer to figure 4.	4.5 - 5.5	8			
Rising/falling time	tTHL tTLH	$\overline{HS}$	Refer to figure 4.	4.5 - 5.5			500	ns

6. AD converter characteristics / Ta=-10°C to + 70°C, VSS=0V

Parameter	Symbol	Pins	Conditions	Limits				
				VDD[V]	min.	typ.	max.	unit
Resolution	N			4.5 – 5.5		6		bit
Absolute precision	ET		(Note)				±1	LSB
Conversion time	tCAD	Vref selection to conversion finish	1 bit conversion time = 2 × Tcyc			1.69		µs
Analog input voltage range	VAIN	AN4 - AN7			VSS		VDD	V
Analog port input current	IAINH		VAIN=VDD				1	µA
	IAINL		VAIN=VSS		-1			

(Note) Absolute precision does not include quaritizing error (1/2LSB).

7. Analog mode RGB characteristics / Ta=-10°C to +70°C, VSS=0V

Parameter	Symbol	Pins	Conditions	Limits				
				VDD[V]	min.	typ.	max.	unit
Analog output voltage		R.G.B Analog output mode	Low level output	5.0	0.45	0.5	0.55	V
			Intensity output		0.90	1.0	1.10	
			Hi lebel output		1.35	1.5	1.65	
Time setting		R.G.B	70% 10pf load				50	ns

8. Sample current dissipation characteristics / Ta=-10°C to +70°C, VSS=0V

The sample current dissipation characteristics is the measurement result of Sanyo provided evaluation board when the recommended circuit parameters shown in the sample oscillation circuit characteristics are used externally. The currents through the output transistors and the pull-up MOS transistors are ignored.

Parameter	Symbol	Pins	Conditions		Limits			
				VDD[V]	min.	typ.	max.	unit
Current dissipation during basic operation	IDDOP(1)	VDD	•FmX'tal=32.768kHz X'tal oscillation •System clock : VCO •VCO for OSD operating • OSD : digital mode •Internal RC oscillation stops	4.5 - 5.5		27	44	mA
	IDDOP(2)	VDD	•FmX'tal=32.768kHz X'tal oscillation •System clock : VCO • VCO for OSD operating • OSD : analog mode •Internal RC oscillation stops	4.5 - 5.5		35	55	µA
	IDDOP(3)	VDD	•FmX'tal=32.768kHz X'tal oscillation •System clock : X'tal •VCO for system VCO for OSD, internal RC oscillation stop • AD converters stop	4.5 - 5.5		100	300	µA
Current dissipation in HALT mode	IDDHALT(1)	VDD	•HALT mode •FmX'tal=32.768kHz X'tal oscillation •System clock : VCO •VCO for OSD stops •Internal RC oscillation stops	4.5 - 5.5		6	10	mA
	IDDHALT(2)	VDD	•HALT mode •FmX'tal=32.768kHz X'tal oscillation •VCO for system stops •VCO for OSD stops •System clock : Internal RC	4.5 - 5.5		430	1000	µA
	IDDHALT(3)	VDD	•HALT mode •FmX'tal=32.768kHz X'tal oscillation •VCO for system stops •VCO for OSD stops •System clock : X'tal	4.5 - 5.5		60	200	
Current dissipation in HOLD mode	IDDHOLD	VDD	•HOLD mode •All oscillation stops.	4.5 - 5.5		0.05	20	µA

(Note 3) The currents of the output transistors and the pull-up MOS transistors are ignored.

Recommended Oscillation Circuit and Sample Characteristics

The sample oscillation circuit characteristics in the table below is based on the following conditions:

- Recommended circuit parameters are verified by an oscillator manufacturer using a Sanyo provided oscillation evaluation board.
- Sample characteristics are the result of the evaluation with the recommended circuit parameters connected externally.

Recommended oscillation circuit and sample characteristics (Ta = -10 to +70°C)

Frequency	Manufacturer	Oscillator	Recommended circuit parameters				Operating supply voltage range	Oscillation stabilizing time		Notes
			C1	C2	Rf	Rd		typ.	max	
32.768kHz	Seiko Epson	C-002RX	18pF	18pF	open	390k•	4.5 – 5.5V	1.00s	1.50s	

Notes The oscillation stabilizing time period is the time until the VCO oscillation for the internal system becomes stable after the following conditions. (Refer to Figure 2.)

1. The VDD becomes higher than the minimum operating voltage after the power is supplied.
2. The HOLD mode is released.

The sample oscillation circuit characteristics may differ applications. For further assistance, please contact with oscillator manufacturer with the following notes in your mind.

- Since the oscillation frequency precision is affected by wiring capacity of the application board, etc., adjust the oscillation frequency on the production board.
- The above oscillation frequency and the operating supply voltage range are based on the operating temperature of -10°C to +70°C. For the use with the temperature outside of the range herein, or in the applications requiring high reliability such as car products, please consult with oscillator manufacturer.
- When using the oscillator which is not shown in the sample oscillation circuit characteristics, please consult with Sanyo sales personnel.

Since the oscillation circuit characteristics are affected by the noise or wiring capacity because the circuit is designed with low gain in order to reduce the power dissipation, refer to the following notices.

- The distance between the clock I/O terminal (XT1 terminal XT2 terminal) and external parts should be as short as possible.
- The capacitors' VSS should be allocated close to the microcontroller's GND terminal and be away from other GND.
- The signal lines with rapid state changes or with large current should be allocated away from the oscillation circuit.

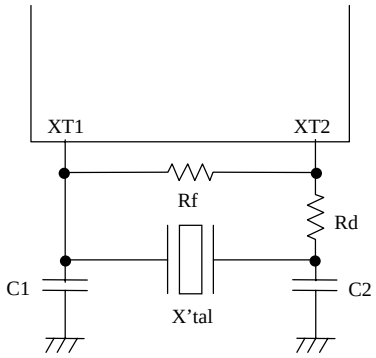


Figure 1 Recommended oscillation circuit.

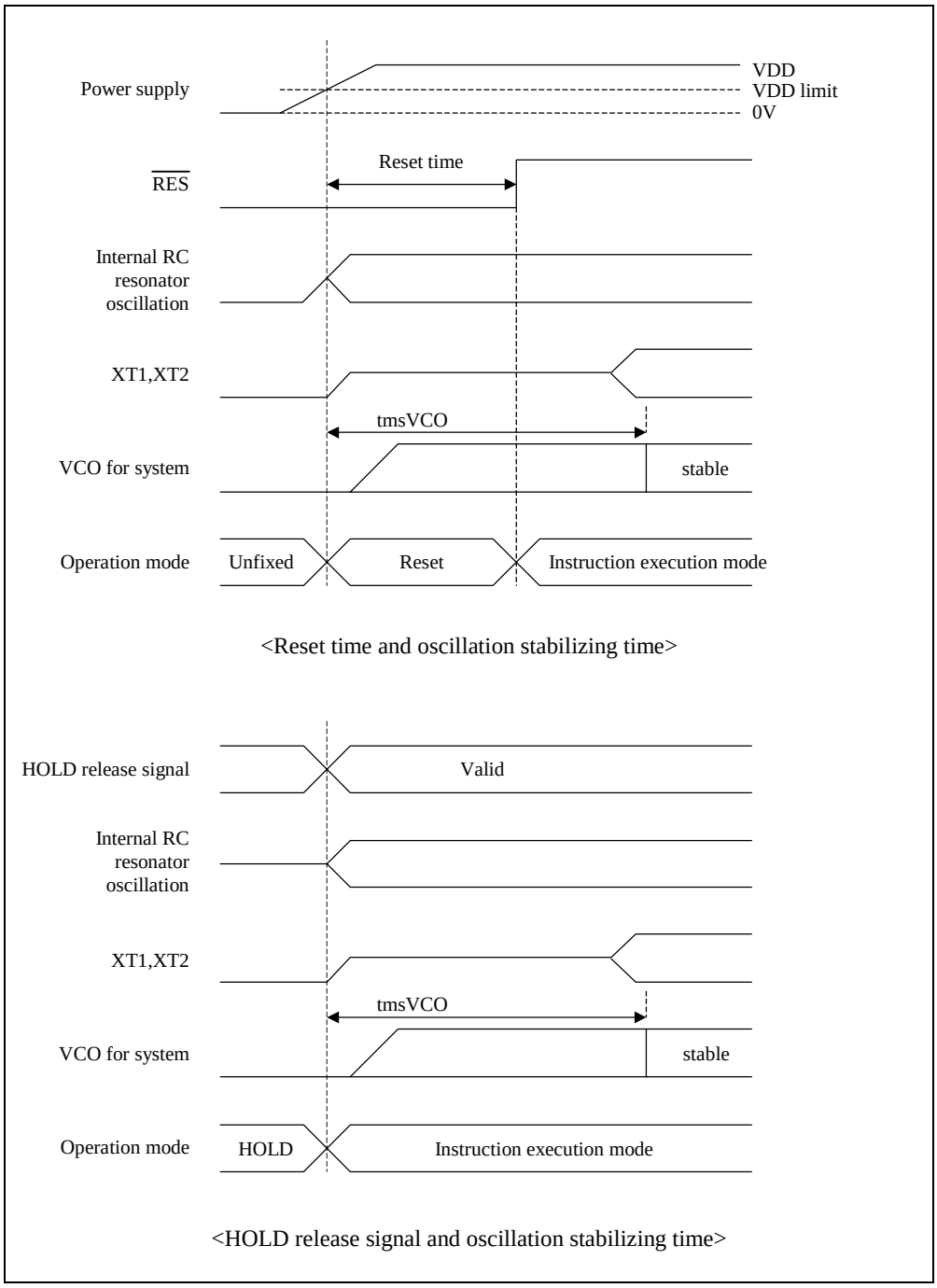


Figure 2 Oscillation stabilizing time

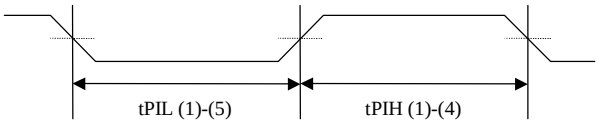


Figure 3 Pulse input timing condition – 1

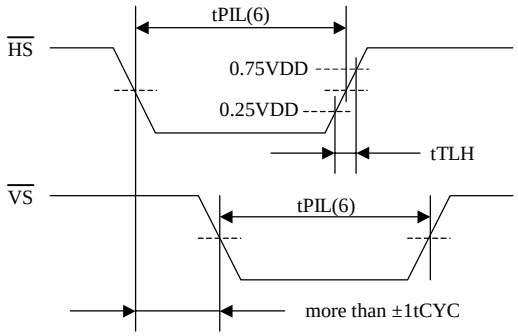


Figure 4 Pulse input timing condition - 2

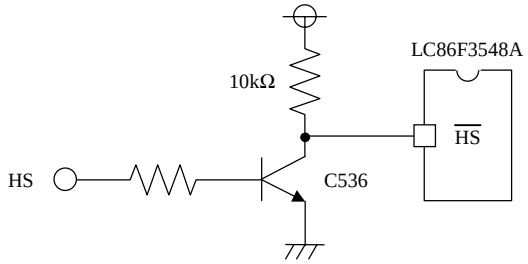


Figure 5 Recommended Interface circuit

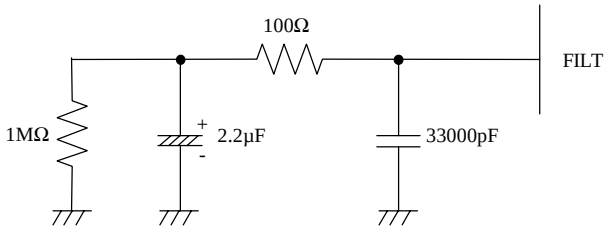
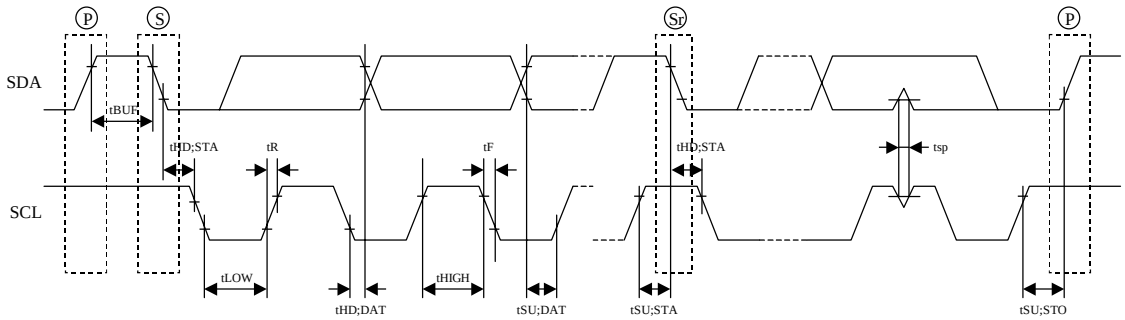


Figure 6 FILT recommended circuit

(Note) Place FILT parts on board as close to the microcontroller as possible.



S : start condition
P : stop condition
Sr : restart condition

tsp : Spike suppression

Standard mode : not exist
High speed mode : less than 50ns

Figure 7 IIC timing

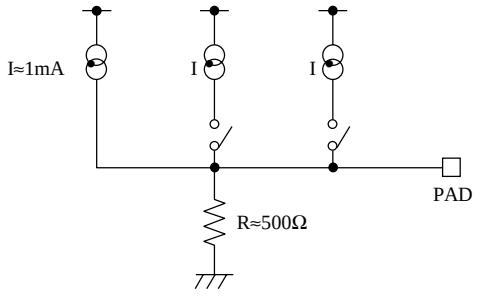


Figure 8 R.G.B. analog output equivalent circuit