

## **Product Specification**

### **GENERAL DESCRIPTION**

OB2278 is a highly integrated current mode PWM control IC optimized for high performance, low standby power and cost effective offline flyback converter applications.

PWM switching frequency at normal operation is externally programmable and trimmed to tight range. At no load or light load condition, the IC operates in extended 'burst mode' to minimize switching loss. Lower standby power and higher conversion efficiency is thus achieved.

VDD low startup current and low operating current contribute to a reliable power on startup design with OB2278. A large value resistor could thus be used in the startup circuit for reduced power loss.

The internal slope compensation improves system large signal stability and reduces the possible sub-harmonic oscillation at high PWM duty cycle output. Leading-edge blanking on current sense input removes the signal glitch due to snubber circuit diode reverse recovery and greatly reduces the external component count and system cost in the design.

OB2278 comprehensive offers protection including coverage Cycle-by-Cycle current limiting(OCP), **VDD** Under Voltage Lockout(UVLO). **VDD** Over Voltage Protection(OVP), VDD Clamp, Gate Clamp, Over Load protection(OLP) and Over Temperature protection (OTP), etc.

Different latch shutdown options are offered on OB2278 in different device version. T version supports both OVP and OTP latch shutdown. L version provides all OVP, OTP and OLP latch shutdown control.

Excellent EMI performance is achieved with soft switching control at the totem pole gate drive output.

OB2278 is offered in SOP-8 and DIP-8 packages.

#### **FEATURES**

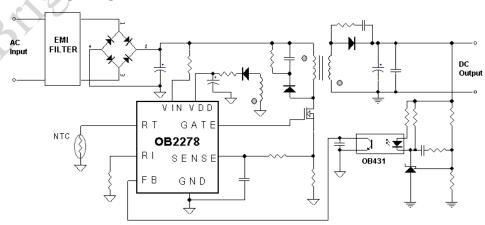
- Power On Soft Start
- Extended Burst Mode Control For Improved Efficiency and Minimum Standby Power Design
- Audio Noise Free Operation
- External Programmable PWM Switching Frequency
- Internal Synchronized Slope Compensation
- Low VIN/VDD Startup Current(3uA) and Low Operating Current (2.3mA)
- Leading Edge Blanking on Current Sense Input
- Complete Protection Coverage with selective protections for Latch Shutdown
  - VDD Over Voltage Protection(OVP) Latch Shutdown
  - Over Temperature Protection(OTP) Latch Shutdown
  - Over Load Protection. (OLP) Auto recovery or Latch Shutdown
  - VDD Under Voltage Lockout with Hysteresis (UVLO)
  - Gate Output Voltage Clamp (16.5V)
  - Built-in OCP Compensation to Achieve Minimum OPP Variation over Universal AC Input Range.

## **APPLICATIONS**

Offline AC/DC flyback converter for

- Adaptor
- Notebook Adaptor
- LCD Monitor/TV/PC/Set-Top Box Power Supplies
- Open-frame SMPS
- Printer Power

## TYPICAL APPLICATION

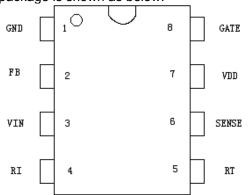




## **GENERAL INFORMATION**

## **Pin Configuration**

The pin map of OB2278 in DIP8 and SOP8 package is shown as below.



**Ordering Information** 

Part Number	Description
OB2278AP-T	DIP8, tube package, T version with OVP/OTP latch
OB2278AP-L	DIP8, tube package, L version with OVP/OTP/OLP latch
OB2278CP-T	SOP8, tube package, T version with OVP/OTP latch
OB2278CPA-T	SOP8, taping package, T version with OVP/OTP latch
OB2278CP-L	SOP8, tube package, L version with OVP/OTP/OLP latch
OB2278CPA-L	SOP8, taping package, L version with OVP/OTP/OLP latch

**Note:** All Devices are offered in Pb-free Package if not otherwise noted.

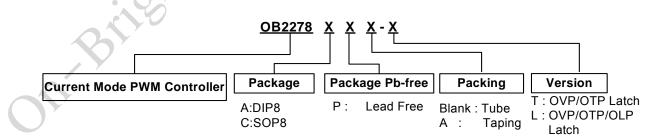
**Package Dissipation Rating** 

Package	RθJA (℃/W)		
DIP8	90		
SOP8	150		

**Absolute Maximum Ratings** 

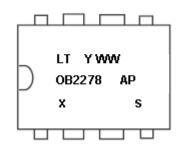
Parameter	Value	
VDD Clamp Voltage (V <sub>clamp</sub> )	35 V	
VDD Clamp Continuous Current	10 mA	
VIN / VDD Input Voltage	-0.3V to V <sub>clamp</sub>	
FB Input Voltage	-0.3 to 7V	
Sense Input Voltage	-0.3 to 7V	
RT Input Voltage	-0.3 to 7V	
RI Input Voltage	-0.3 to 7V	
Min/Max Operating Junction Temperature T <sub>J</sub>	-20 to 150 ℃	
$\begin{array}{c} \text{Min/Max Storage Temperature} \\ \text{T}_{\text{stg}} \end{array}$	-55 to 150 ℃	
Lead Temperature (Soldering, 10 seconds)	260 ℃	

**Note:** Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum-rated conditions for extended periods may affect device reliability.

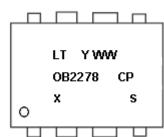


## **Marking Information**

DIP8



SOP8



A: DIP8 Package P: Pb-free Package Y: Year Code(0-9) WW: Week Code(01-52)

X: Version s: Internal Code

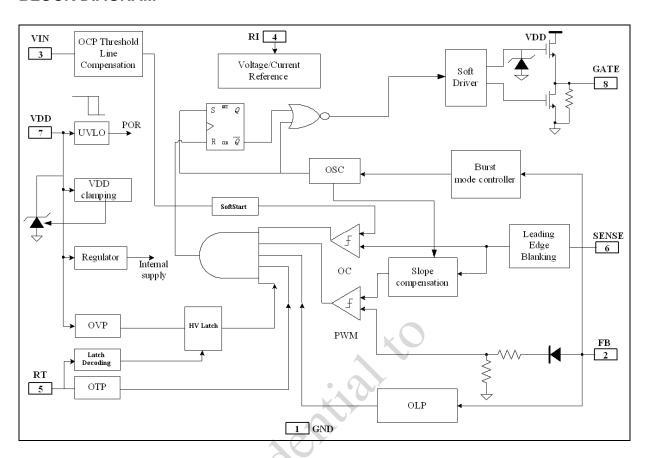
C: SOP8 Package P: Pb-free Package Y: Year Code(0-9) WW: Week Code(01-52)

X: Version s: Internal Code

## **TERMINAL ASSIGNMENTS**

Pin Num	Pin Name	1/0	Description	
1	GND	Р	Ground	
2	FB	I	Feedback input pin. PWM duty cycle is determined by voltage level into this pin and current-sense signal level at Pin 6.	
3	VIN	I	Connected through a large value resistor to rectified line input for startup and line voltage sensing.	
4	RI	1	Internal oscillator frequency setting pin. A resistor connected between RI and GND sets the PWM frequency.	
5	RT	1	Dual function pin. Either connected through a NTC resistor to GND for over temperature shutdown control or used as latch shutdown control input.	
6	SENSE	1	Current sense input pin. Connected to MOSFET current sensing resistor node.	
7	VDD	Р	DC power supply pin.	
8	GATE	0	Totem-pole gate drive output for power MOSFET.	
S. I. Z. J.				
30				

## **BLOCK DIAGRAM**



## RECOMMENDED OPERATING CONDITION

Symbol	Parameter	Min	Max	Unit	
VDD	VDD Supply Voltage	11.5	25	V	
T <sub>A</sub>	Operating Ambient Temperature	-20	85	$^{\circ}$	
n Bi					



## **ELECTRICAL CHARACTERISTICS**

(TA =  $25^{\circ}$ C, RI=100K ohm, VDD=16V, if not otherwise noted)

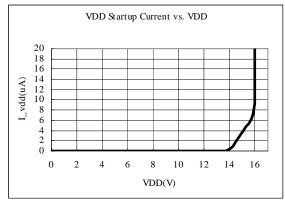
Symbol	Parameter	Test Conditions	Min	Тур	Max	Unit	
Supply Voltage	(VDD)						
I_VDD_Startup	VDD Start up Current	VDD =15V Measure current into VDD		3	20	uA	
I_VDD_Ops	Operation Current	V <sub>FB</sub> =3V		2.3		mA	
UVLO(Enter)	VDD Under Voltage Lockout Enter		8.8	9.8	10.8	٧	
UVLO(Exit)	VDD Under Voltage Lockout Exit (Startup)		15.5	16.5	17.5	V	
OVP(Latch)	VDD Over Voltage Latch Trigger		26.5	28	29.5	V	
OVP(De-Latch)	VDD Latch Release Voltage Threshold			7.5		V	
I(Vdd)_latch	VDD bleeding current at latch shutdown when VDD = 9V			45		uA	
T <sub>D</sub> OVP	VDD OVP Debounce time			80		uSec	
V <sub>DD</sub> _Clamp	V <sub>DD</sub> Zener Clamp Voltage	$I(V_{DD}) = 5 \text{ mA}$		35		V	
T_Softstart	Soft Start Time			3		mSec	
Feedback Input			1		1		
A <sub>VCS</sub>	PWM Input Gain	$\Delta V_{FB}/\Delta V_{cs}$		2.8		V/V	
V <sub>FB</sub> _Open	V <sub>FB</sub> Open Voltage			6.2		V	
I <sub>FB</sub> _Short	FB pin short circuit current	Short FB pin to GND, measure current		0.75		mA	
V <sub>TH</sub> _0D	Zero Duty Cycle FB Threshold Voltage				0.95	V	
V <sub>TH</sub> _BM	Burst Mode FB Threshold Voltage			1.6		V	
V <sub>TH</sub> _PL	Power Limiting FB Threshold Voltage			4.4		<b>\</b>	
T <sub>D</sub> _PL	Power limiting Debounce Time			80		mSec	
Z <sub>FB</sub> _IN	Input Impedance			9.0		Kohm	
<b>Current Sense In</b>							
T_blanking	Sense Input Leading Edge Blanking Time			300		nSec	
Z <sub>SENSE</sub> _IN	Sense Input Impedance			30		Kohm	
T <sub>D</sub> OC	Over Current Detection and Control Delay	CL=1nf at GATE,		70		nSec	
V <sub>TH</sub> _OC_0	Current Limiting Threshold at No Compensation	I(VIN) = 0uA	0.85	0.90	0.95	V	
V <sub>TH</sub> _OC_1	Current Limiting Threshold at Compensation	I(VIN) = 150uA		0.80		V	
Oscillator							
F <sub>OSC</sub>	Normal Oscillation Frequency		60	65	70	KHZ	
Δf_Temp	Frequency Temperature Stability	-20℃ to 100 ℃		3		%	
Δf_VDD	Frequency Voltage Stability	VDD = 12-28V,		3		%	

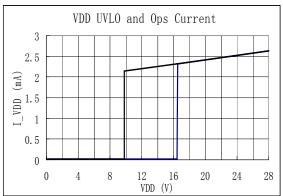


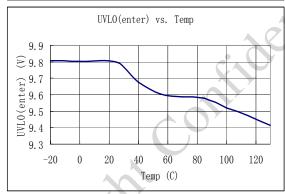
RI_range	Operating RI Range		50	100	250	Kohm	
V_RI_open	RI open voltage			2.0		V	
F_BM	Burst Mode Base Frequency			20		KHZ	
Gate Drive Out	put						
VOL	Output Low Level	lo = 20 mA			0.3	V	
VOH	Output High Level	Io = 20 mA	11			V	
VG_Clamp	Output Clamp Voltage Level			16.5		٧	
T_r	Output Rising Time	CL = 1nf		120		nSec	
T_f	Output Falling Time	CL = 1nf		50		nSec	
Over Temperat	Over Temperature Protection						
I_RT	Output Current of RT pin			70		uA	
V <sub>TH</sub> _OTP	OTP Threshold Voltage		1.015	1.065	1.115	V	
T <sub>D</sub> OTP	OTP De-bounce Time			100		uSec	
V RT Open	RT Pin Open Voltage			3.7		V	

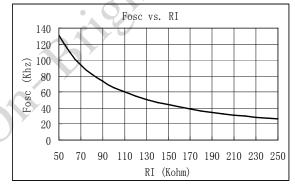


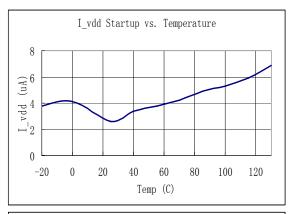
## **CHARACTERIZATION PLOTS**

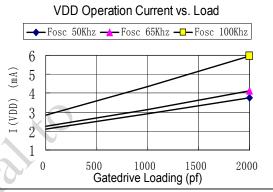


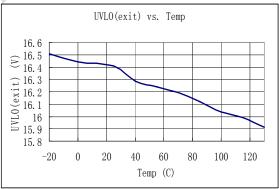


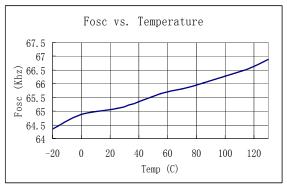




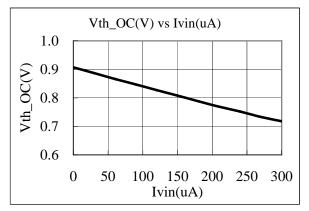


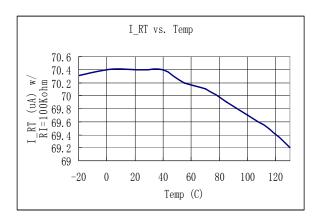


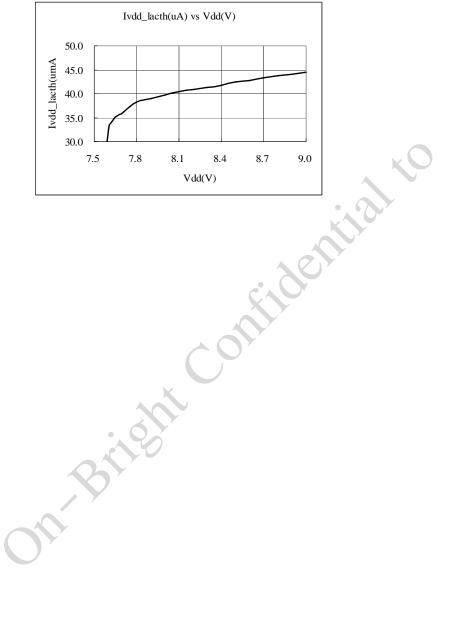














## **OPERATION DESCRIPTION**

OB2278 is a highly integrated PWM controller IC optimized for offline flyback converter applications with requirement in latch shutdown or auto recovery. The extended burst mode control greatly reduces the standby power consumption and helps the design easily meet the international power conservation requirements.

#### Startup Current and Start up Control

Startup current of OB2278 is designed to be very low so that VDD could be charged up above UVLO(exit) threshold level and device starts up quickly. A large value startup resistor can therefore be used to minimize the power loss yet reliable startup in application. For a typical AC/DC adaptor with universal input range design, a 2 M $\Omega$ , 1/8 W startup resistor could be used together with a VDD capacitor to provide a fast startup and yet low power dissipation design solution.

#### Operating Current

The Operating current of OB2278 is low at 2.3mA. Good efficiency is achieved with OB2278 low operating current together with extended burst mode control schemes.

## Burst Mode Operation

At zero load or light load condition, most of the power dissipation in a switching mode power supply is from switching loss of the MOSFET transistor, the core loss of the transformer and the loss in the snubber circuit. The magnitude of power loss is in proportion to the number of switching events within a fixed period of time. Reducing switching events leads to the reduction on the power loss and thus conserves the energy. OB2278 self adjusts the switching mode according to the loading condition. At no load or light load condition, the FB input drops below burst mode threshold level. Device enters Burst Mode control. The Gate drive output switches only when VDD voltage drops below a preset level and FB input is actived to output an on state. Otherwise the gate drive remains at off state to minimize the switching loss thus reduce the standby power consumption to the greatest extend. The nature of high frequency switching also reduces the audio noise at any loading conditions.

## Oscillator Operation

A resistor connected between RI and GND sets the constant current source to charge/discharge

the internal cap and thus the PWM oscillator frequency is determined. The relationship between RI and switching frequency follows the below equation within the specified RI in Kohm range at nominal loading operational condition.

$$F_{OSC} = \frac{6500}{RI(Kohm)}(Khz)$$

## Current Sensing and Leading Edge Blanking

Cycle-by-Cycle current limiting is offered in OB2278 current mode PWM control. The switch current is detected by a sense resistor into the sense pin. An internal leading edge blanking circuit chops off the sense voltage spike at initial MOSFET on state due to snubber diode reverse recovery so that the external RC filtering on sense input is no longer needed. The current limit comparator is disabled and cannot turn off the external MOSFET during the blanking period. The PWM duty cycle is determined by the current sense input voltage and the FB input voltage.

# Internal Synchronized Slope Compensation

Built-in slope compensation circuit adds voltage ramp onto the current sense input voltage for PWM generation. This greatly improves the close loop stability at CCM and prevents the subharmonic oscillation and thus reduces the output ripple voltage.

#### Over Temperature Protection with Latch Shutdown

A NTC resistor in series with a regular resistor should be connected between RT and GND for temperature sensing and protection. NTC resistor value becomes lower when the ambient temperature rises. With the fixed internal current  $I_{RT}$  flowing through the resistors, the voltage at RT pin becomes lower at high temperature. The internal OTP circuit is triggered and shutdown the MOSFET when the sensed input voltage is lower than  $V_{TH}$ OTP.

OTP is a latched shutdown.

# RT Pin Used as Latch Shutdown Input Control

RT pin could also be used as a control input to implement system latch shutdown function.

An example is to implement system OVP protection with a latch shutdown function through



a photo coupler and affiliated circuits. When OVP detection signal connected to RT is lower than  $V_{TH}$ \_OTP, OB2278 controls system into latch shutdown. The recovery of the AC/DC system could only start by resetting internal latch when VDD voltage drops below VDD\_De-latch value. This could be achieved by unplugging/re-plugging of AC source in AC start-up configuration.

#### Gate Drive

OB2278 Gate is connected to the Gate of an external MOSFET for power switch control. Too weak the gate drive strength results in higher conduction and switch loss of MOSFET while too strong gate drive output compromises the EMI. Good tradeoff is achieved through the built-in totem pole gate drive design with right output strength and dead time control. The low idle loss and good EMI system design is easier to achieve with this dedicated control scheme. An internal 16.5V clamp is added for MOSFET gate protection at higher than expected VDD input.

#### Protection Controls

Good system reliability is achieved with OB2278's rich protection features including Cycle-by-Cycle current limiting (OCP), Over Load Protection (OLP) with auto-recovery(T version) or latch shutdown(L

version), over temperature protection (OTP) with latch shutdown, on-chip VDD over voltage protection (OVP) with latch shutdown and under voltage lockout (UVLO).

The OCP threshold value is self adjusted lower at higher current into VIN pin. This OCP threshold slope adjustment helps to compensate the increased output power limit at higher AC voltage caused by inherent Over-Current sensing and control delay. A constant output power limit is achieved with recommended OCP compensation scheme.

At output overload condition, FB voltage is set higher. When FB input exceeds power limit threshold value for more than 80mS, control circuit reacts to turnoff the power MOSFET. This is so called OLP shutdown. It is either autorecovery or latched shutdown depending on version of OB2278.

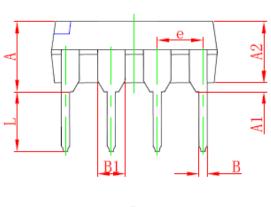
Similarly, control circuit shuts down the power MOSFET when an Over Temperature condition is detected. This shutdown is latched.

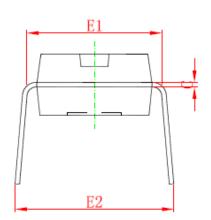
VDD is supplied with transformer auxiliary winding output. It is clamped when VDD is higher than 35V. MOSFET is shut down when VDD drops below UVLO(enter) limit and device enters power on start-up sequence thereafter.

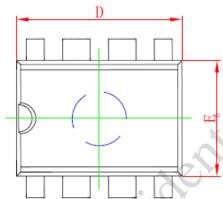


## **PACKAGE MECHANICAL DATA**

## 8-Pin Plastic DIP

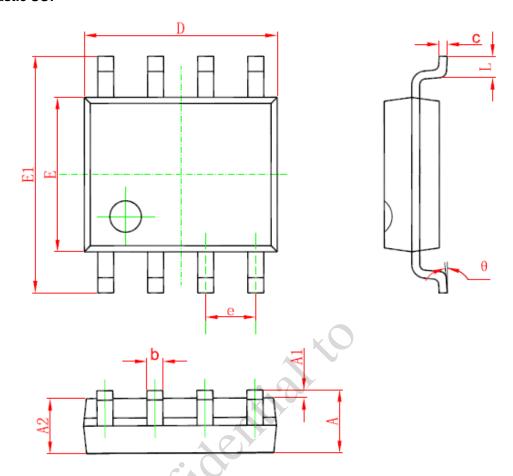






Cumbal	Dimensions	In Millimeters	Dimension	s In Inches
Symbol	Min	Max	Min	Max
Α	3.710	5.334	0.146	0.210
A1	0.381		0.015	
A2	2.921	4.953	0.115	0.195
В	0.350	0.650	0.014	0.026
B1 •	1.524 (BSC)		0.06 (BSC)	
C	0.200	0.360	0.008	0.014
D	9.000	10.160	0.354	0.400
E	6.096	7.112	0.240	0.280
E1	7.320	8.255	0.288	0.325
е	2.540 (BSC)		0.1 (1	BSC)
L	2.921	3.810	0.115	0.150
E2	7.620	10.920	0.300	0.430

## 8-Pin Plastic SOP



Symbol	Dimensions In Millimeters		Dimensions In Inches		
Syllibol	Min	Max	Min	Max	
Α	1.350	1.750	0.053	0.069	
A1	0.050	0.250	0.002	0.010	
A2	1.250	1.650	0.049	0.065	
b	0.310	0.510	0.012	0.020	
С	0.100	0.250	0.004	0.010	
D	4.700	5.150	0.185	0.203	
E	3.800	4.000	0.150	0.157	
Ę1	5.800	6.200	0.228	0.244	
е	1.270	(BSC)	0.050 (BSC)		
X ,	0.400	1.270	0.016	0.050	
θ	0°	8°	0°	8°	



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