



ALPHA & OMEGA
SEMICONDUCTOR

AOL1420

N-Channel Enhancement Mode Field Effect Transistor



General Description

The AOL1420 uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and low gate resistance. This device is ideally suited for use as a low side switch in CPU core power conversion.

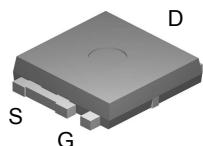
- RoHS Compliant
- Halogen and Antimony Free Green Device*

Features

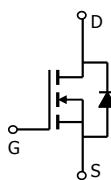
$V_{DS} (V) = 30V$
 $I_D = 85A (V_{GS} = 10V)$
 $R_{DS(ON)} < 3.7m\Omega (V_{GS} = 10V)$
 $R_{DS(ON)} < 5.5m\Omega (V_{GS} = 4.5V)$

UIS Tested
 $R_g, C_{iss}, C_{oss}, C_{rss}$ Tested

Ultra SO-8™ Top View



Bottom tab
connected to
drain



Absolute Maximum Ratings $T_A=25^\circ C$ unless otherwise noted

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	V_{DS}	30	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current ^{B,G}	I_D	85	A
$T_C=100^\circ C$ ^B		63	
Pulsed Drain Current	I_{DM}	150	
Continuous Drain Current ^G	I_{DSM}	19	
$T_A=70^\circ C$		15	
Avalanche Current ^C	I_{AR}	30	A
Repetitive avalanche energy $L=0.1mH$ ^C	E_{AR}	112	mJ
Power Dissipation ^B	P_D	100	W
$T_C=100^\circ C$		50	
Power Dissipation ^A	P_{DSM}	2.08	W
$T_A=70^\circ C$		1.3	
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 175	°C

Thermal Characteristics

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient ^A	$R_{\theta JA}$	19.6	25	°C/W
Maximum Junction-to-Ambient ^A		50	60	°C/W
Maximum Junction-to-Case ^C	$R_{\theta JC}$	0.9	1.5	°C/W

Electrical Characteristics ($T_J=25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	$I_D=250\mu\text{A}, V_{GS}=0\text{V}$	30			V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=24\text{V}, V_{GS}=0\text{V}$ $T_J=55^\circ\text{C}$		1	5	μA
I_{GSS}	Gate-Body leakage current	$V_{DS}=0\text{V}, V_{GS}=\pm 20\text{V}$		100		nA
$V_{GS(\text{th})}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu\text{A}$	1	1.8	3	V
$I_{D(\text{ON})}$	On state drain current	$V_{GS}=10\text{V}, V_{DS}=5\text{V}$	85			A
$R_{DS(\text{ON})}$	Static Drain-Source On-Resistance	$V_{GS}=10\text{V}, I_D=20\text{A}$ $T_J=125^\circ\text{C}$	2.9	3.7	5.5	$\text{m}\Omega$
		$V_{GS}=4.5\text{V}, I_D=20\text{A}$	4.4	4.4	5.5	$\text{m}\Omega$
g_{FS}	Forward Transconductance	$V_{DS}=5\text{V}, I_D=20\text{A}$	106			S
V_{SD}	Diode Forward Voltage	$I_S=1\text{A}, V_{GS}=0\text{V}$	0.72	1		V
I_S	Maximum Body-Diode Continuous Current			85		A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	$V_{GS}=0\text{V}, V_{DS}=15\text{V}, f=1\text{MHz}$		3700	4400	pF
C_{oss}	Output Capacitance			700		pF
C_{rss}	Reverse Transfer Capacitance			390		pF
R_g	Gate resistance	$V_{GS}=0\text{V}, V_{DS}=0\text{V}, f=1\text{MHz}$		0.54	0.7	Ω
SWITCHING PARAMETERS						
$Q_g(10\text{V})$	Total Gate Charge	$V_{GS}=4.5\text{V}, V_{DS}=15\text{V}, I_D=20\text{A}$		63	76	nC
$Q_g(4.5\text{V})$	Total Gate Charge			33	40	nC
Q_{gs}	Gate Source Charge			8.6		nC
Q_{gd}	Gate Drain Charge			17.6		nC
$t_{D(\text{on})}$	Turn-On DelayTime	$V_{GS}=10\text{V}, V_{DS}=15\text{V}, R_L=0.75\Omega, R_{\text{GEN}}=3\Omega$		12		ns
t_r	Turn-On Rise Time			15.5		ns
$t_{D(\text{off})}$	Turn-Off DelayTime			40		ns
t_f	Turn-Off Fall Time			14		ns
t_{rr}	Body Diode Reverse Recovery Time	$I_F=20\text{A}, dI/dt=100\text{A}/\mu\text{s}$		34	41	ns
Q_{rr}	Body Diode Reverse Recovery Charge	$I_F=20\text{A}, dI/dt=100\text{A}/\mu\text{s}$		30		nC

A: The value of $R_{\theta JA}$ is measured with the device in a still air environment with $T_A=25^\circ\text{C}$.B: The power dissipation P_D is based on $T_{J(\text{MAX})}=175^\circ\text{C}$, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.C: Repetitive rating, pulse width limited by junction temperature $T_{J(\text{MAX})}=175^\circ\text{C}$.D: The $R_{\theta JA}$ is the sum of the thermal impedance from junction to case $R_{\theta JC}$ and case to ambient.E: The static characteristics in Figures 1 to 6 are obtained using $<300\ \mu\text{s}$ pulses, duty cycle 0.5% max.F: These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(\text{MAX})}=175^\circ\text{C}$.

G: The maximum current rating is limited by bond-wires.

* This device is guaranteed green after date code 8P11 (June 1ST 2008)

Rev3: Jun 2008

THIS PRODUCT HAS BEEN DESIGNED AND QUALIFIED FOR THE CONSUMER MARKET. APPLICATIONS OR USES AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS ARE NOT AUTHORIZED. AOS DOES NOT ASSUME ANY LIABILITY ARISING OUT OF SUCH APPLICATIONS OR USES OF ITS PRODUCTS. AOS RESERVES THE RIGHT TO IMPROVE PRODUCT DESIGN, FUNCTIONS AND RELIABILITY WITHOUT NOTICE.

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

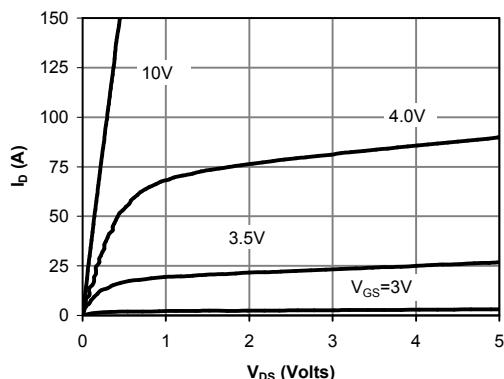


Fig 1: On-Region Characteristics

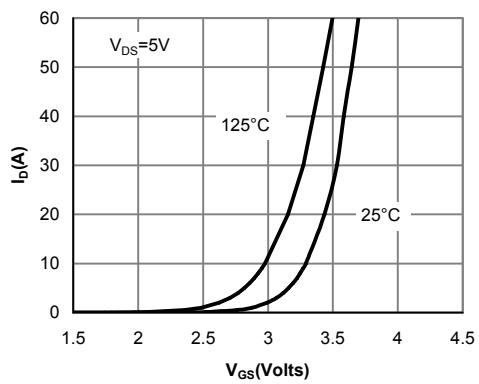


Figure 2: Transfer Characteristics

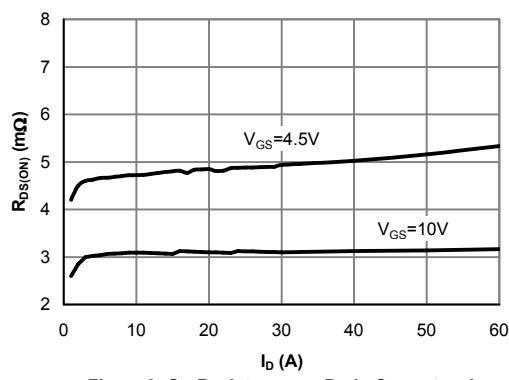


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

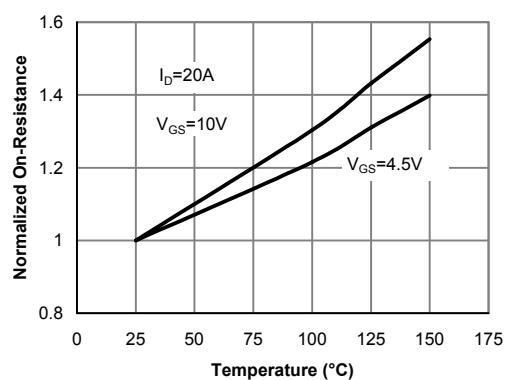


Figure 4: On-Resistance vs. Junction Temperature

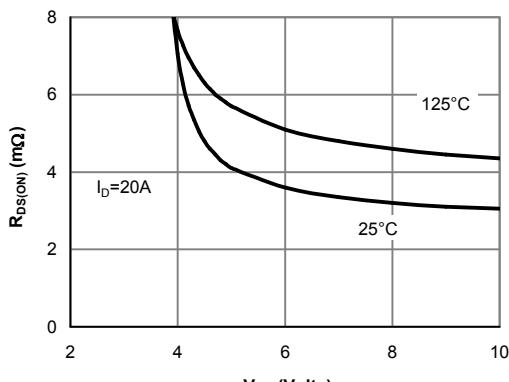


Figure 5: On-Resistance vs. Gate-Source Voltage

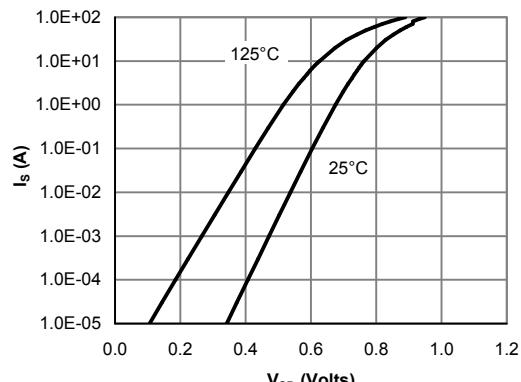


Figure 6: Body-Diode Characteristics

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

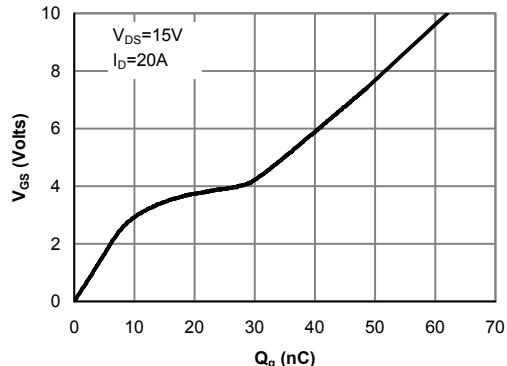


Figure 7: Gate-Charge Characteristics

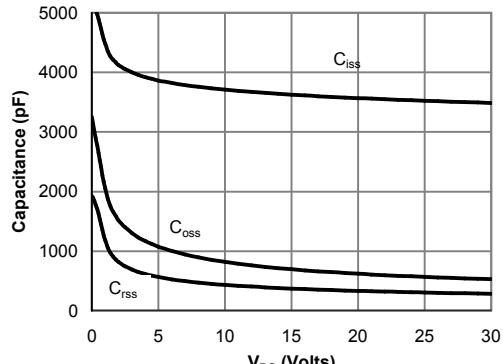


Figure 8: Capacitance Characteristics

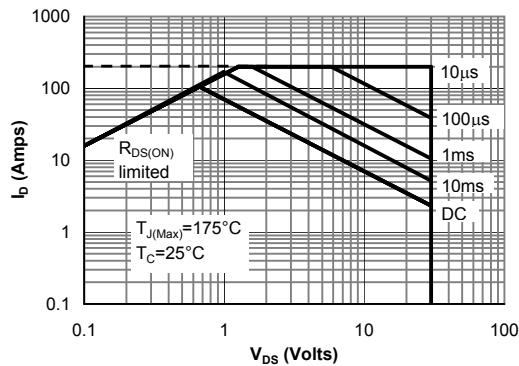


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

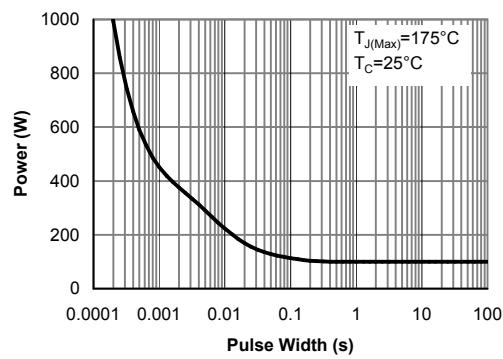


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note F)

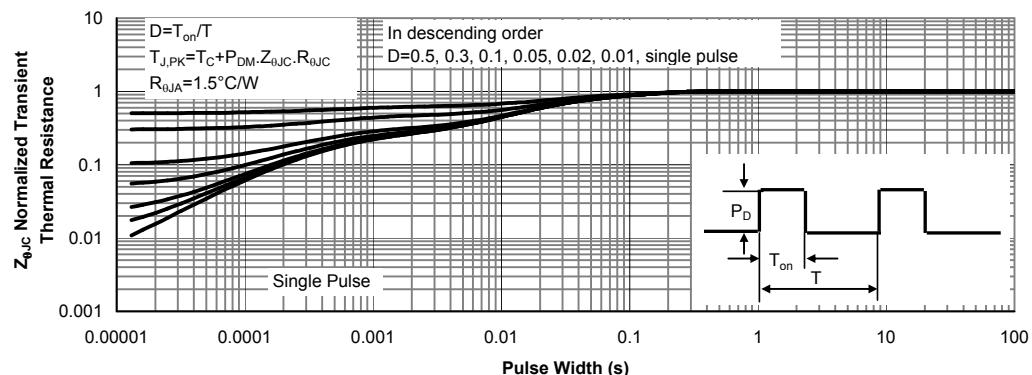


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

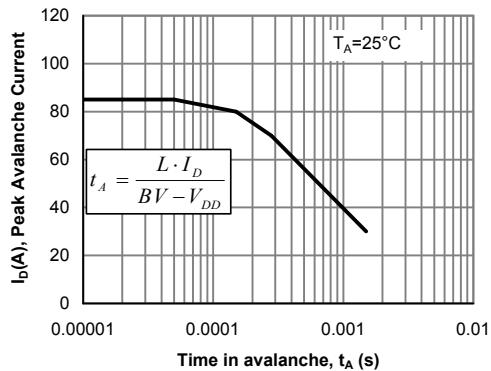
TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS


Figure 12: Single Pulse Avalanche capability

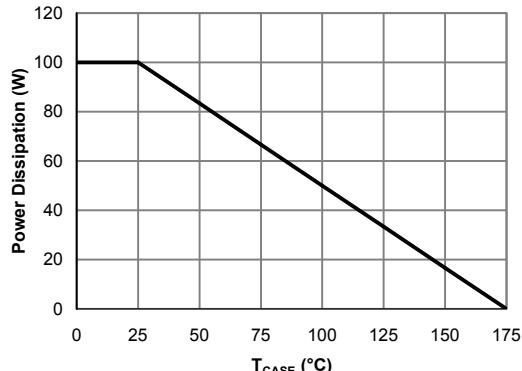


Figure 13: Power De-rating (Note B)

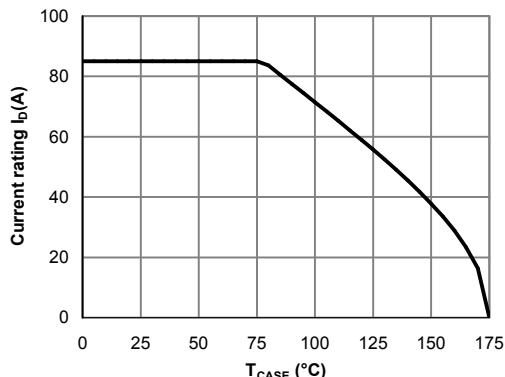


Figure 14: Current De-rating (Note B)

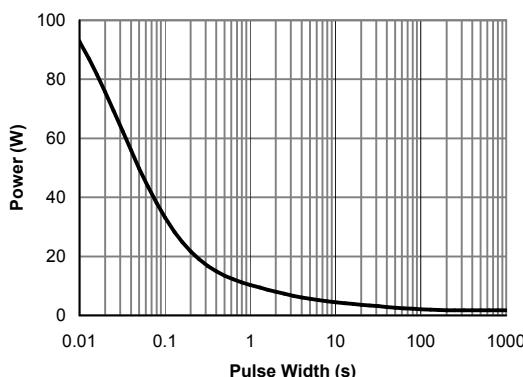


Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note H)

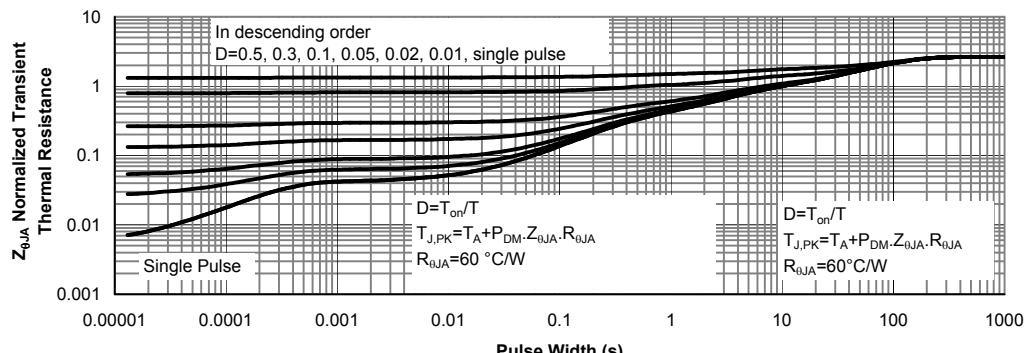
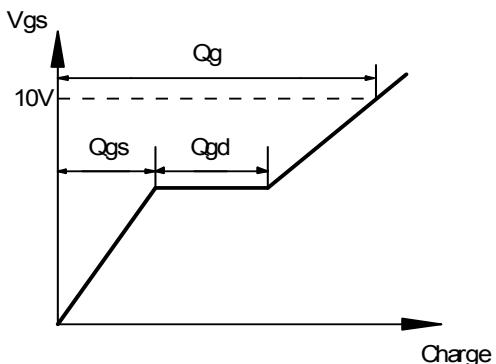
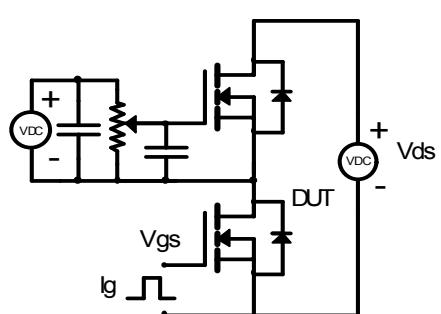
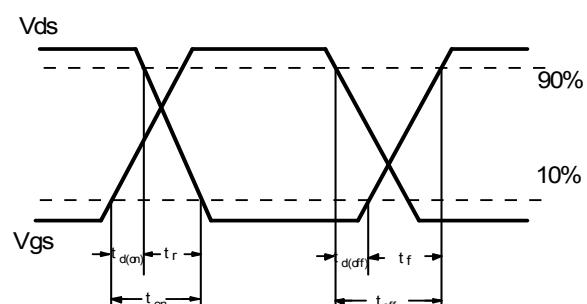
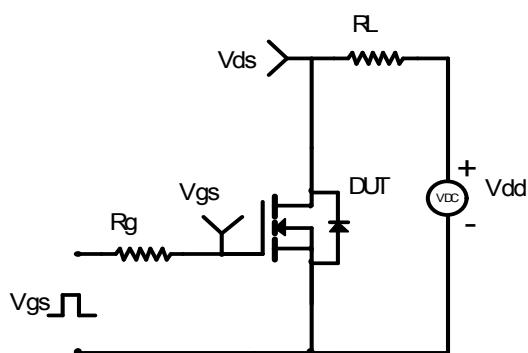


Figure 16: Normalized Maximum Transient Thermal Impedance (Note H)

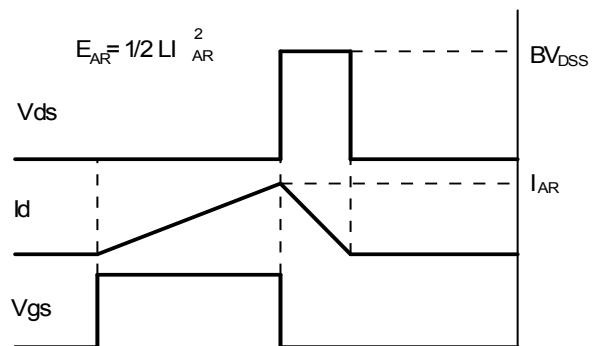
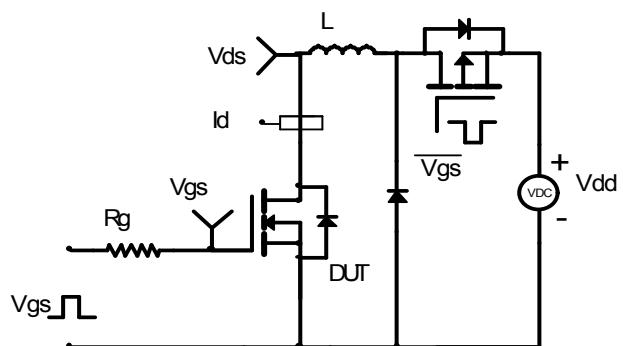
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms

