FAIRCHILD SEMICONDUCTOR®

September 2012

DAP024 / DAP024L
Highly Integrated Green-Mode PWM Controller

Features

- Low Startup Current: 8 µA
- Low Operating Current in Green Mode: 3 mA
- Peak-Current Mode Operation with Cycle-by-Cycle Current Limiting
- PWM Frequency Continuously Decreasing with Burst Mode at Light Loads
- V_{DD} Over-Voltage Protection (OVP)
- Constant Output Power Limit (Full AC Input Range)
- Internal Latch Circuit for OVP, OTP
- Fixed PWM Frequency (65 kHz) with Frequency Hopping
- Feedback Open-Loop Protection with 56 ms Delay
- Soft-Start Time: 4 ms
- 400 mA Driving Capability

Applications

General-purpose switched-mode power supplies and flyback power converters, including:

- Power Adapters
- Open-Frame SMPS
- SMPS with Surge-Current Output; such as for Printers, Scanners, and Motor Drivers

Description

A highly integrated PWM controller, DAP024/L provides several features to enhance the performance of flyback converters. To minimize standby power consumption, a proprietary Green Mode provides off-time modulation to continuously decrease the switching frequency under light-load conditions. Under zero-load conditions, the power supply enters Burst Mode, which completely shuts off PWM output. Output restarts just before the supply voltage drops below the UVLO lower limit. Green Mode enables power supplies to meet international power conservation requirements.

The DAP024/L is designed for SMPS and integrates a frequency-hopping function that helps reduce EMI emission of a power supply with minimum line filters. The built-in synchronized slope compensation is proprietary sawtooth compensation for constant output power limit over universal AC input range. The gate output is clamped at 18 V to protect the external MOSFET from over-voltage damage.

Other protection functions include V_{DD} over-voltage protection and over-temperature protection. For over-temperature protection, an external NTC thermistor can be applied to sense the ambient temperature. When V_{DD} OVP or OTP is activated, an internal latch circuit latches off the controller.

Part Number	OVP	OTP	OLP
DAP024	Latch	Latch	Auto Restart
DAP024L	Latch	Latch	Latch

Ordering Information

Part Number	Operating Temperature Range	Package	Packing Method
DAP024	-40 to +105°C	6-Lead, SOT23, JEDEC MO-178 Variation AB, 1.6 mm Wide	Tape & Reel
DAP024L			

This product is not recommended for shipping into the United States. It may be subject to court injunction. See http://www.fairchildsemi.com/about-fairchild/media-center/litigation.

Typical Application

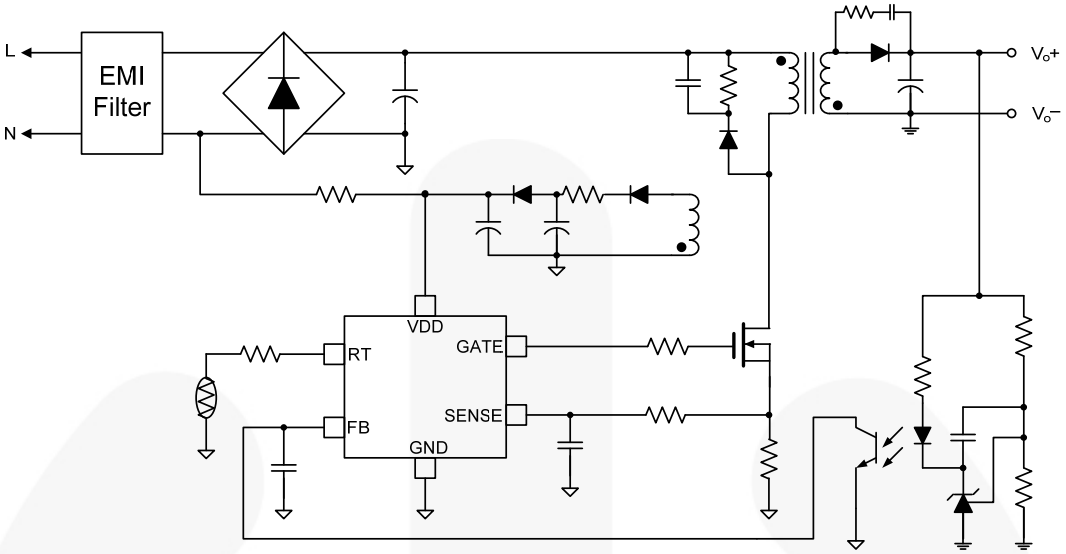


Figure 1. Typical Application

Block Diagram

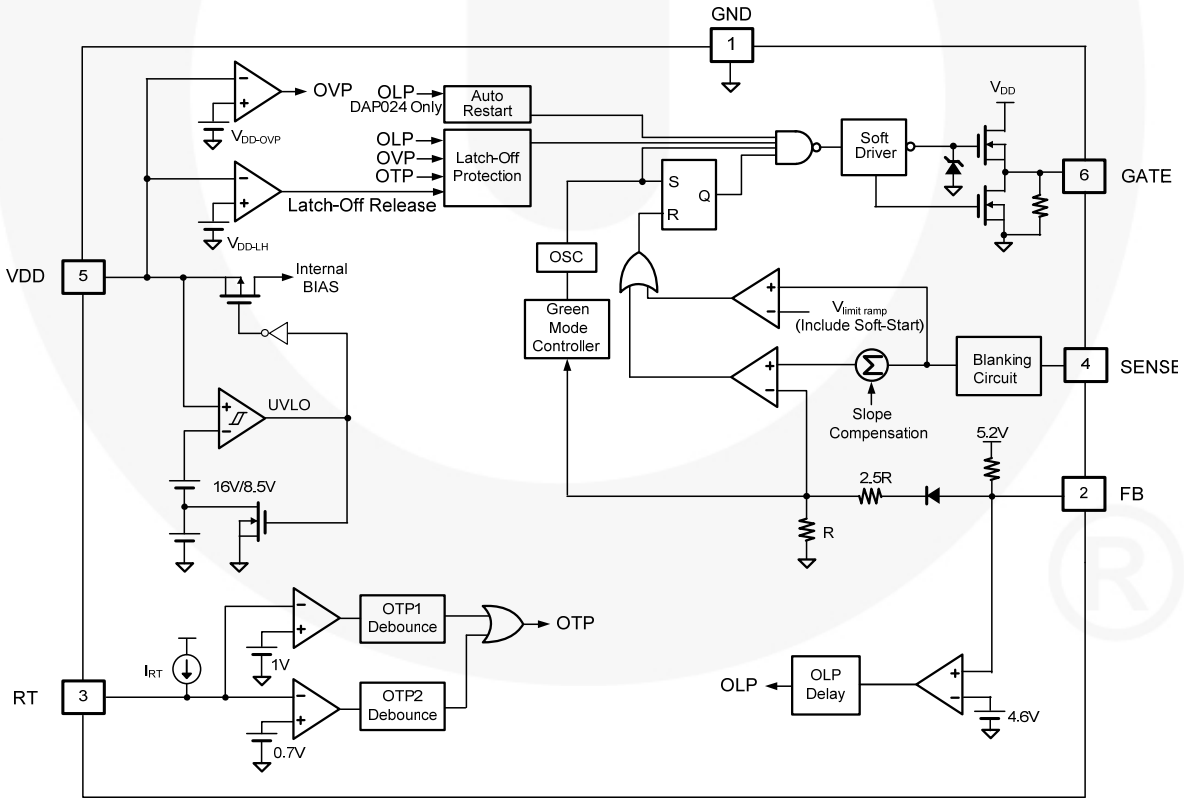
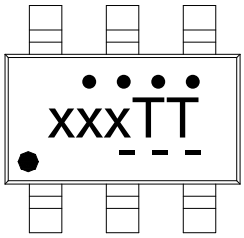


Figure 2. Block Diagram

Marking Information



xxx:	024: DAP024 24L: DAP024L
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Figure 3. Top Mark

Pin Configuration

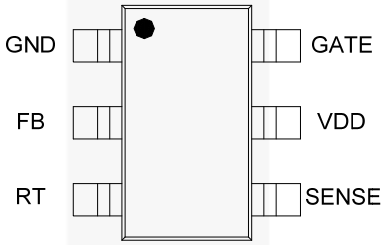


Figure 4. Pin Configuration

Pin Definitions

Pin #	Name	Function	Description
1	GND	Ground	Ground
2	FB	Feedback	The FB pin provides the output voltage regulation signal. It provides feedback to the internal PWM comparator, so that the PWM comparator can control the duty cycle. This pin also provides for OLP: if V_{FB} is larger than the trigger level with a long delay, the controller stops and restarts.
3	RT	Temperature Detection	An external NTC thermistor is connected from this pin to GND for over-temperature protection. The impedance of the NTC decreases at high temperatures. Once the voltage of the RT pin drops below a threshold, PWM output is disabled.
4	SENSE	Current Sense	This pin senses the voltage across a resistor. When the voltage reaches the internal threshold, PWM output is disabled. This activates over-current protection. This pin also provides current amplitude information for current-mode control.
5	VDD	Power Supply	Power supply
6	GATE	Driver Output	The totem-pole output driver for driving the power MOSFET.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. All voltage values, except differential voltages, are given with respect to GND pin.

Symbol	Parameter	Min.	Max.	Unit
V_{DD}	Supply Voltage		30	V
V_L	Input Voltage to FB, SENSE, RT Pin	-0.3	7.0	V
P_D	Power Dissipation at T_A<50°C		300	mW
Θ_{JC}	Thermal Resistance (Junction-to-Case)		208.4	°C/W
T_J	Operating Junction Temperature	-40	+150	°C
T_{STG}	Storage Temperature Range	-55	+150	°C
T_L	Lead Temperature, Wave Soldering, 10 Seconds		+260	°C
ESD	Human Body Model, JESD22-A114		3.00	kV
	Charge Device Model, JESD22-C101		1.25	

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Max.	Unit
T_A	Operating Ambient Temperature	-40	+105	°C

Electrical Characteristics

V_{DD} = 15 V, and T_A = 25°C, unless otherwise noted.

Symbol	Parameter		Condition	Min.	Typ.	Max.	Unit
V_{DD} Section							
V_{DD-OP}	Continuously Operating Voltage					24	V
V_{DD-ON}	Turn-On Threshold Voltage			15	16	17	V
V_{DD-OFF}	Turn-Off Voltage			7.5	8.5	9.5	V
V_{DD-OVP}	V_{DD} Over-Voltage Protection (Latch-Off)			24	25	26	V
V_{DD-LH}	Threshold Voltage for Latch-Off Release			3	4	5	V
I_{DD-ST}	Startup Current		V_{DD-ON}–0.16 V		8	30	µA
I_{DD-OP}	Normal Operating Supply Current		C_L=1 nF		3	4	mA
I_{DD-BM}	Green-Mode Operating Supply Current		GATE Open, V_{FB}=V_{FB-G}			2.5	mA
V_{DD-OVP}	V_{DD} Over-Voltage Protection			24	25	26	V
$t_{D-VDDOVP}$	V_{DD} OVP Debounce Time				30	50	µs
I_{DD-LH}	Latch-Off Holding Current		V_{DD}=5 V		40	65	µA
Feedback Input Section							
A_V	Input-Voltage to Current-Sense Attenuation			1/4.0	1/3.5	1/3.0	V/V
Z_{FB}	Input Impedance				5.5		kΩ
$V_{FB-OPEN}$	FB Pin Open Voltage			5.0	5.2	5.4	V
V_{FB-OLP}	Threshold Voltage for Open-Loop Protection			4.3	4.6	4.9	V
t_{D-OLP}	Open-Loop Protection Delay			53	56	60	ms
Current Sense Section							
t_{PD}	Delay to Output				100	250	ns
t_{LEB}	Leading-Edge Blanking Time			270	360		ns
V_{STHFL}	Flat Threshold Voltage for Current Limit		Duty>51%		0.5		V
V_{STHVA}	Valley Threshold Voltage for Current Limit		Duty=0%		0.44		V
V_{SLOPE}	Slope Compensation		Duty=DCY_{MAX}		0.273		V
$t_{SOFT-START}$	Period During Startup Time				4		ms
Oscillator Section							
f_{OSC}	Normal PWM Frequency	Center Frequency	V_{FB}>V_{FB-N}	62	65	68	kHz
		Hopping Range	V_{FB}≥V_{FB-N}		±4.2		
		Hopping Range	V_{FB}=V_{FB-G}		±2.9		
t_{hop-1}	Hopping Period 1		V_{FB}≥V_{FB-N}		4.4		ms
t_{hop-3}	Hopping Period 3		V_{FB}=V_{FB-G}		11.5		ms
f_{OSC-G}	Green Mode Minimum Frequency				22.5		kHz
V_{FB-N}	FB Threshold Voltage For Frequency Reduction				2.2		V
V_{FB-G}	FB Voltage at f_{OSC-G}				2.1		V
V_{FB-ZDC}	FB Threshold Voltage for Zero Duty				1.7		V
f_{DV}	Frequency Variation vs. V_{DD} Deviation		V_{DD}=11.5 V to 20 V	0	0.02	2.00	%
f_{DT}	Frequency Variation vs. Temperature Deviation		T_A= -40 to +105°C			2	%

Continued on the following page…

Electrical Characteristics (Continued)

V_{DD} = 15 V, and T_A = 25°C, unless otherwise noted.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
PWM Output Section						
DCY_{MAX}	Maximum Duty Cycle			70		%
V_{OL}	Output Voltage LOW	V_{DD}=15 V, I_O=50 mA			1.5	V
V_{OH}	Output Voltage HIGH	V_{DD}=8 V, I_O=50 mA	6			V
t_R	Rising Time	C_L=1 nF		150	200	ns
t_F	Falling Time	C_L=1 nF		35		ns
V_{CLAMP}	Gate Output Clamping Voltage	V_{DD}=20 V	15.0	16.5	18.0	V
Over-Temperature Protection (OTP) Section						
I_{RT}	Output Current of RT Pin			100		µA
V_{OTP}	Threshold Voltage for Over-Temperature Protection	T_A=25°C	0.97	1.02	1.07	V
t_{DOTP}	Over-Temperature Debounce Time	V_{FB}=V_{FB-N}		17		ms
		V_{FB}=V_{FB-G}		51		
V_{OTP2}	Second Threshold Voltage for Over-Temperature Protection	T_A=25°C	0.60	0.70	0.75	V
t_{DOTP2}	Second Over-Temperature Debounce Time			100		µs

Typical Performance Characteristics

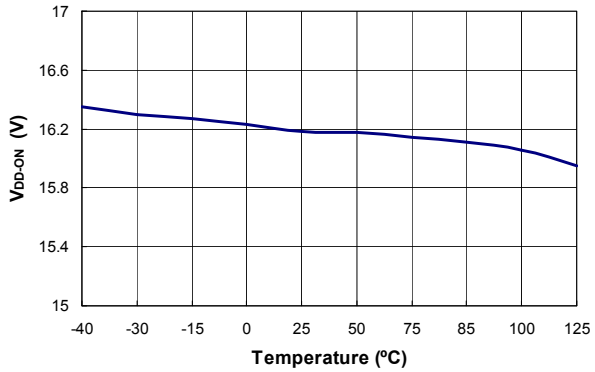


Figure 5. Turn-On Threshold Voltage (V_{DD-ON}) vs. Temperature

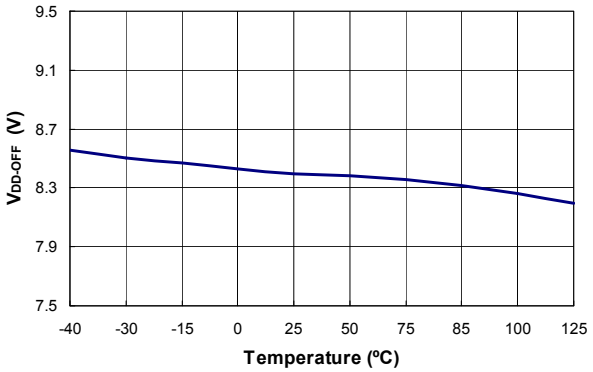


Figure 6. Turn-Off Threshold Voltage (V_{DD-OFF}) vs. Temperature

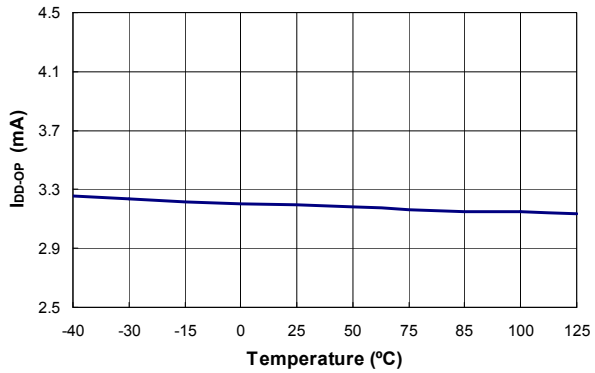


Figure 7. Operating Current (I_{DD-OP}) vs. Temperature

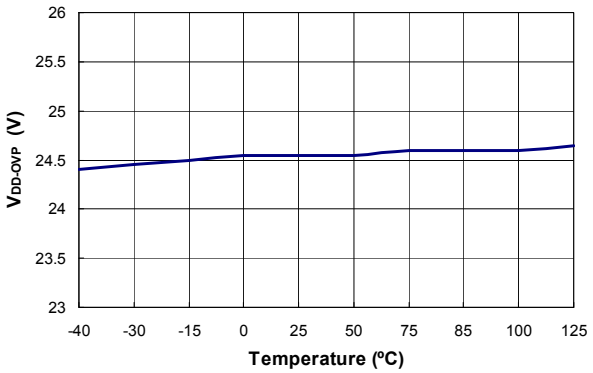


Figure 8. V_{DD} Over-Voltage Protection (V_{DD-OVP}) vs. Temperature

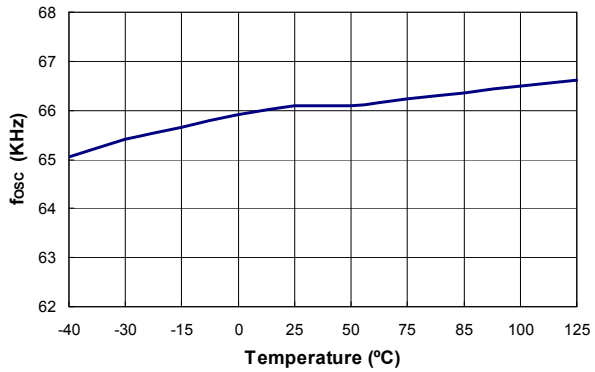


Figure 9. Center Frequency (f_{OSC}) vs. Temperature

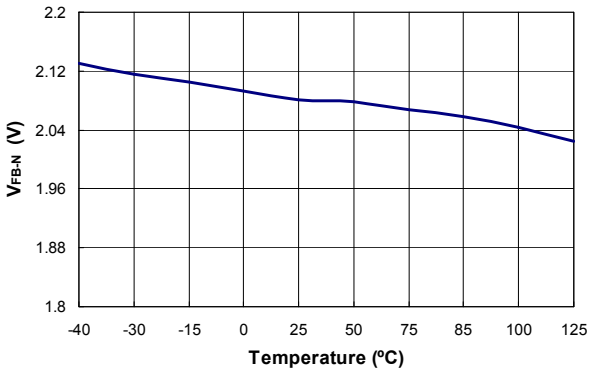


Figure 10. FB Threshold Voltage for Frequency Reduction (V_{FB-N}) vs. Temperature

Typical Performance Characteristics (Continued)

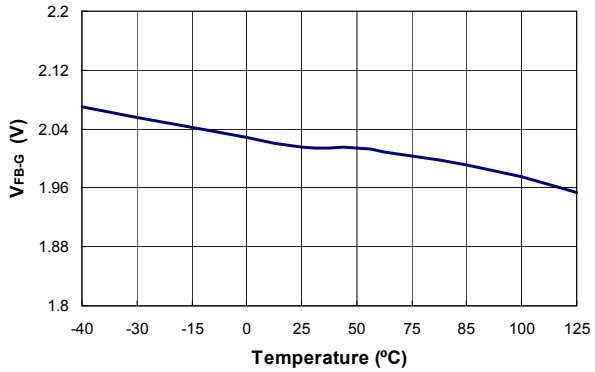


Figure 11. FB Voltage at f_{OSC-G} (V_{FB-G}) vs. Temperature

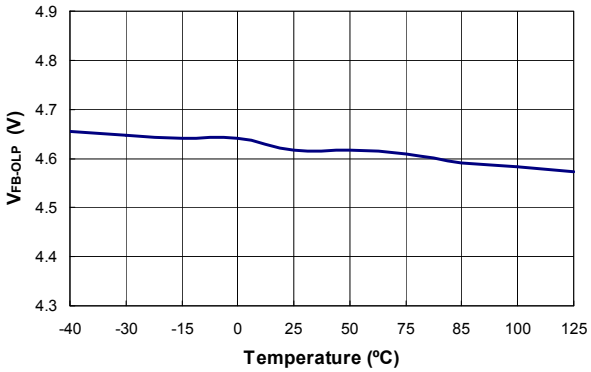


Figure 12. Threshold Voltage for Open-Loop Protection (V_{FB-OLP}) vs. Temperature

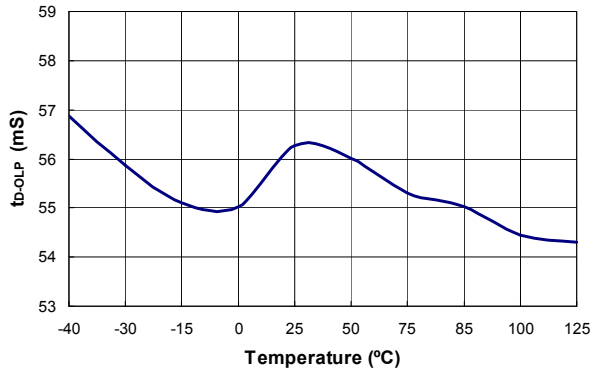


Figure 13. Open-Loop Protection Delay Time (t_{D-OLP}) vs. Temperature

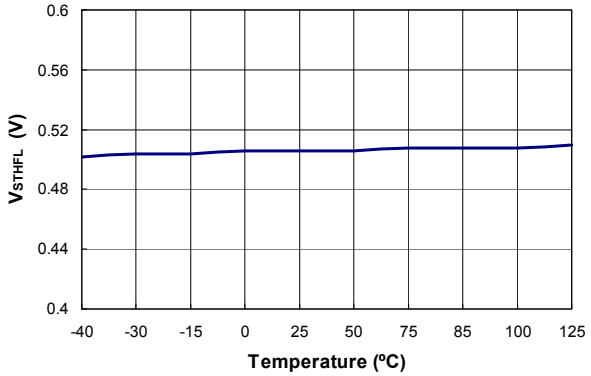


Figure 14. Flat Threshold Voltage for Current Limit (V_{STHFL}) vs. Temperature

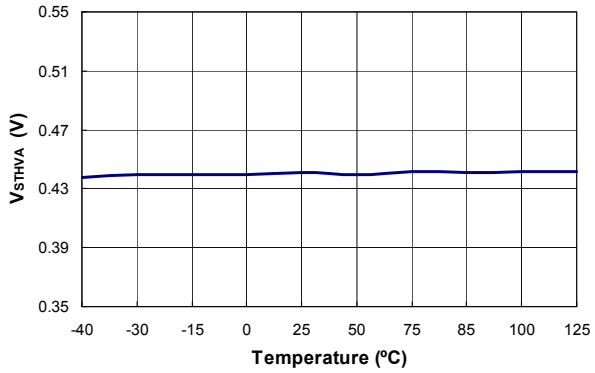


Figure 15. Valley Threshold Voltage for Current Limit (V_{STHVA}) vs. Temperature

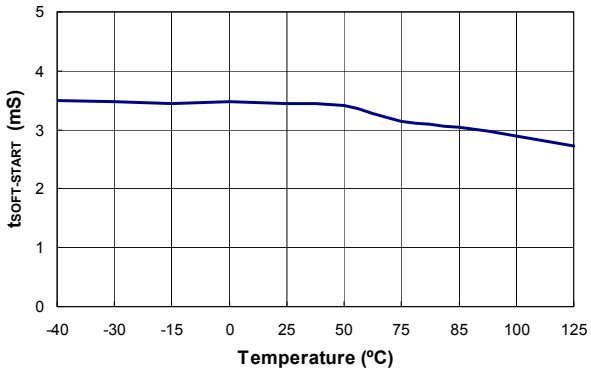


Figure 16. Period during Startup ($t_{SOFT-START}$) vs. Temperature

Typical Performance Characteristics (Continued)

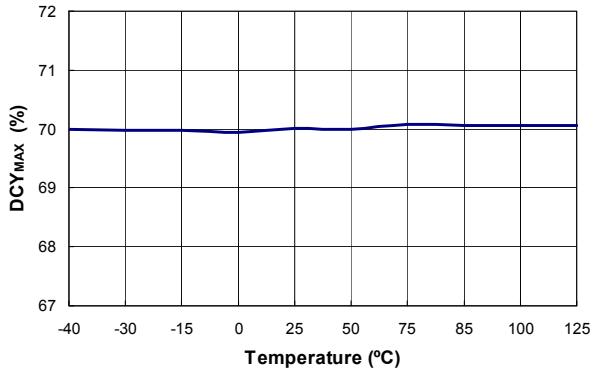


Figure 17. Maximum Duty Cycle (DCY_{MAX}) vs. Temperature

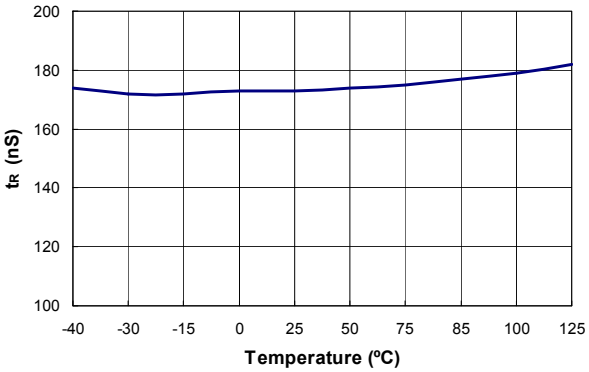


Figure 18. Rising Time (t_R) vs. Temperature

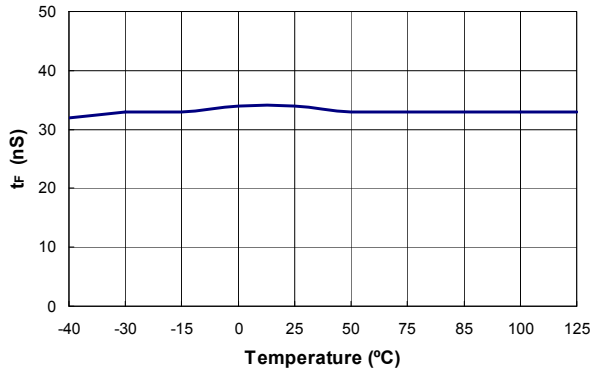


Figure 19. Falling Time (t_F) vs. Temperature

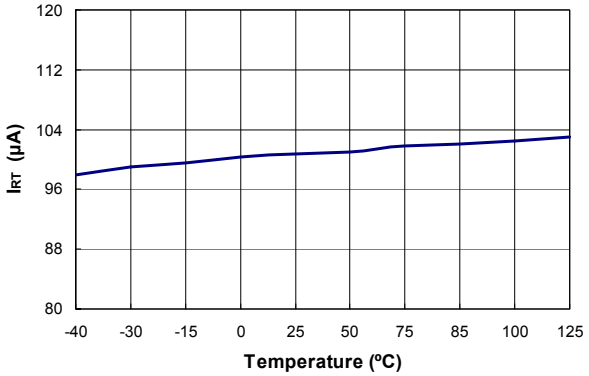


Figure 20. Output Current of RT Pin (I_{RT}) vs. Temperature

Operation Description

Startup Operation

Figure 21 shows a typical startup circuit and transformer auxiliary winding for a DAP024/L application. Before switching operation begins, it consumes only startup current (typically 8 μA) and the current supplied through the startup resistor charges the V_{DD} capacitor (C_{DD}). When V_{DD} reaches turn-on voltage of 16 V (V_{DD-ON}), the DAP024/L begins switching and the current consumed increases to 3 mA. Then the power required is supplied from the transformer auxiliary winding. The large hysteresis of V_{DD} (8.5 V) provides more holdup time, which allows using a small capacitor for V_{DD}. The startup resistor is typically connected to the AC line for a fast reset of latch protection.

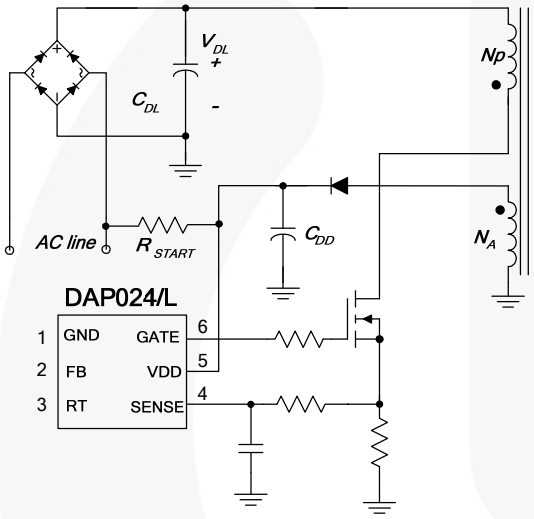


Figure 21. Startup Circuit

Green-Mode Operation

The DAP024/L uses feedback voltage (V_{FB}) as an indicator of the output load and modulates the PWM frequency, as shown in Figure 22, such that the switching frequency decreases as load decreases. In heavy load conditions, the switching frequency is 65 kHz. Once V_{FB} decreases below V_{FB-N} (2.2 V), the PWM frequency starts to linearly decrease from 65 kHz to 22.5 kHz to reduce the switching losses. As V_{FB} decreases below V_{FB-G} (2.1 V), the switching frequency is fixed at 22.5 kHz and DAP024/L enters "deep" Green mode, where the operating current decreases to 2.5 mA (maximum), further reducing the standby power consumption. As V_{FB} decreases below V_{FB-ZDC} (1.7 V), DAP024/L enters Burst Mode. When V_{FB} drops below V_{FB-ZDC}, DAP024 stops switching and the output voltage starts to drop, which causes the feedback voltage to rise. Once V_{FB} rises above V_{FB-ZDC}, switching resumes. Burst Mode alternately enables and disables switching, reducing switching loss in Standby Mode, as shown in Figure 23.

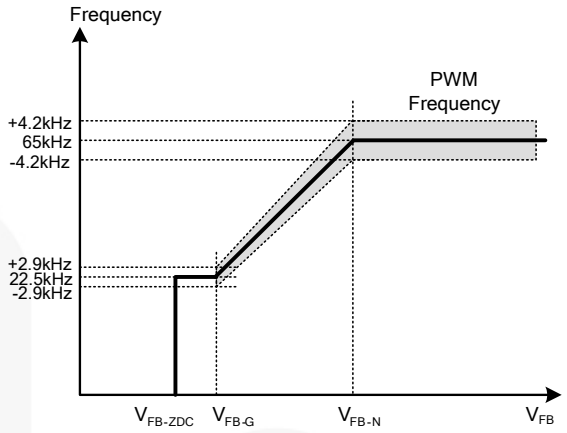


Figure 22. PWM Frequency

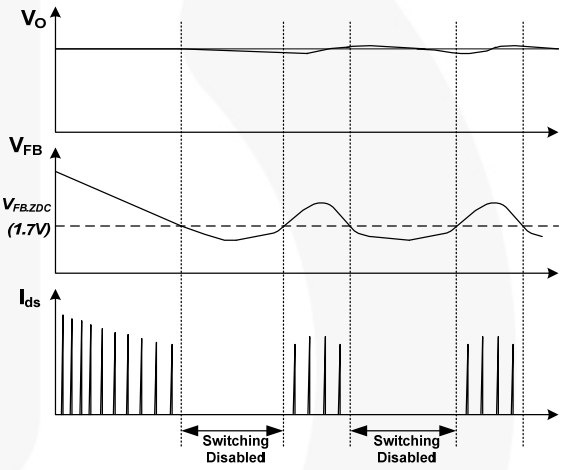


Figure 23. Burst Mode Operation

Frequency Hopping

Electromagnetic Interference (EMI) reduction is accomplished by frequency hopping, which spreads the energy over a wider frequency range than the bandwidth measured by the EMI test equipment. An internal frequency-hopping circuit changes the switching frequency between 60.8 kHz and 69.2 kHz with a period of 4.4 ms, shown in Figure 24.

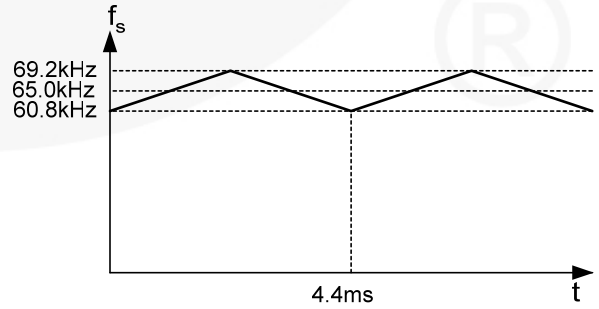


Figure 24. Frequency Hopping

Protections

Self-protective functions include V_{DD} Over-Voltage Protection (OVP), Open-Loop / Overload Protection (OLP), Over-Current Protection (OCP), Short-Circuit Protection, and Over-Temperature Protection (OTP). In DAP024; OLP, OCP, and SCP are Auto-Restart Mode protections. OVP and OTP are Latch-Mode protections with DAP024L.

Auto-Restart Mode Protection: Once a fault condition is detected, switching is terminated and the MOSFET remains off. This causes V_{DD} to fall because no more power is delivered from auxiliary winding. When V_{DD} falls to V_{DD-OFF} (8.5 V), the protection is reset and the operating current reduces to startup current, which causes V_{DD} to rise. Normal operation resumes when V_{DD} reaches V_{DD-ON} (16 V). In this manner, the auto-restart can alternately enable and disable the switching of the MOSFET until the fault condition is eliminated (*see Figure 25*).

Latch-Mode Protection: Once this protection is triggered, switching is terminated and the MOSFET remains off. The latch is reset only when V_{DD} is discharged below 4 V by unplugging the AC power line.

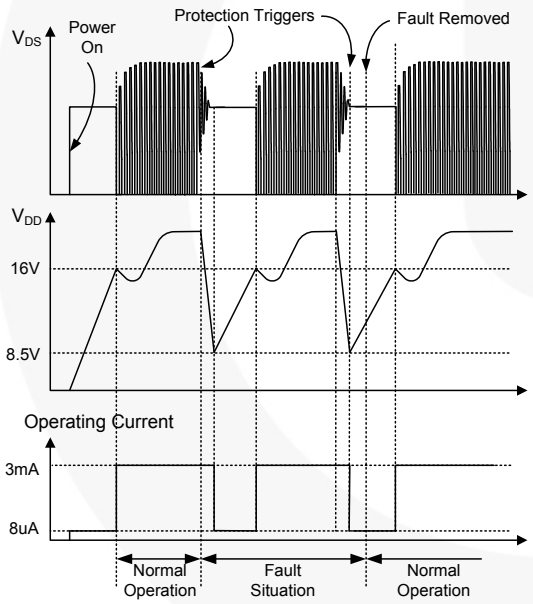


Figure 25. Auto-Restart Operation

Over-Current Protection (OCP)
DAP024/L has over-current protection thresholds. It is for pulse-by-pulse current limit, which turns off the MOSFET for the remainder of the switching cycle when the sensing voltage of the MOSFET drain current reaches the threshold. The other threshold is for the over-current protection, which shuts down the MOSFET gate when the sensing voltage of MOSFET drain current is above the threshold longer than the shutdown delay (56 ms).

Open-Loop / Overload Protection (OLP)
When the upper branch of the voltage divider for the shunt regulator (KA431 shown) is broken, as shown in Figure 26, no current flows through the opto-coupler transistor, which pulls up the feedback voltage to 5.2 V.

When the feedback voltage is above 4.6 V for longer than 56 ms, OLP is triggered. This protection is also triggered when the SMPS output drops below the nominal value longer than 56 ms due to overload condition.

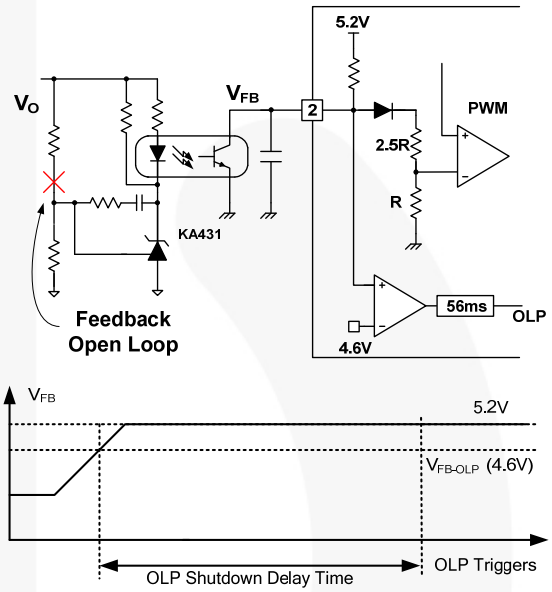


Figure 26. OLP Operation

V_{DD} Over-Voltage Protection (OVP)
V_{DD} over-voltage protection prevents IC damage caused by over voltage on the VDD pin. The OVP is triggered when V_{DD} reaches 25 V. A debounce time (typically 30 µs) prevents false triggering by switching noise.

Over-Temperature Protection (OTP)
The OTP circuit is composed of a current source and voltage comparators. Typically, an NTC thermistor is connected between the RT and GND pins. Once the voltage drops below a threshold of 1.0 V, PWM output is disabled after t_{DOTP} debounce time. If the RT pin drops below 0.7 V, it triggers the latch-off protection immediately after t_{DOTP2} debounce time.

Constant Output Power Limit

DAP024/L has saw-limiter for pulse-by-pulse current limit, which guarantees almost constant power limit over different line voltages of the universal input range.

The conventional pulse-by-pulse current limiting scheme has a constant threshold for current limit comparator, which results in a higher power limit for high line voltage. DAP024/L has a sawtooth current limit threshold that increases progressively within a switching cycle, which provides lower current limit for high line and makes the actual power limit level almost constant over different line voltages of universal input range, as shown in Figure 27.

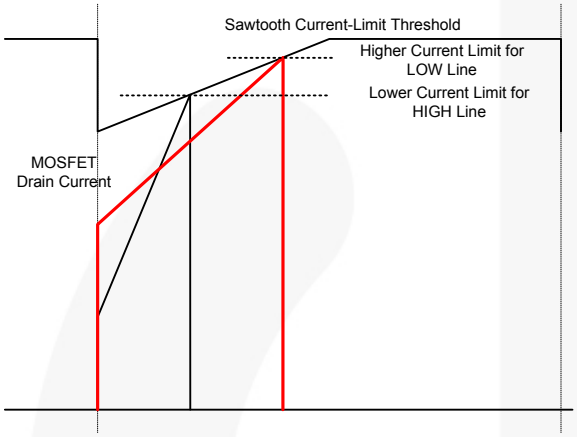


Figure 27. Sawtooth Current Limiter

Leading-Edge Blanking (t_{LEB})

Each time the power MOSFET is switched on, a turn-on spike occurs across the sense-resistor caused by primary-side capacitance and secondary-side rectifier reverse recovery. To avoid premature termination of the switching pulse, a leading-edge blanking time is built in. During this blanking period (360 ns), the PWM comparator is disabled and cannot switch off the gate driver. As a result, an RC filter with a small RC time constant is enough for current sensing.

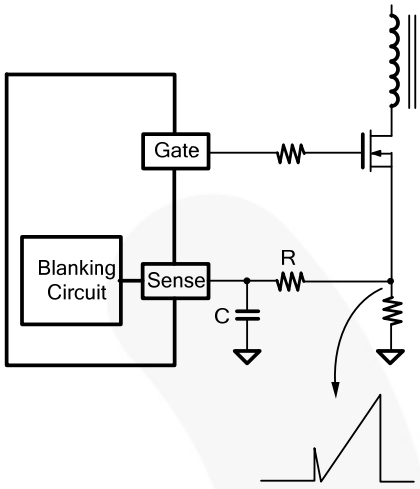


Figure 28. Current Sense R-C Filter

Soft-Start

The DAP024/L has an internal soft-start circuit that increases pulse-by-pulse current-limit comparator inverting input voltage slowly after it starts. The typical soft-start time is 4 ms. The pulsewidth to the power MOSFET is progressively increased to establish the correct working conditions for transformers, rectifier diodes, and capacitors. The voltage on the output capacitors is progressively increased with the intention of smoothly establishing the required output voltage. It also helps prevent transformer saturation and reduces the stress on the secondary diode during startup.

Typical Application Circuit (Netbook Adapter by Flyback)

Application	Fairchild Devices	Input Voltage Range	Output
Netbook Adapter	DAP024/L	90~265 V_{AC}	19 V / 2.1 A (40 W)

Features

- High efficiency (>85.3% at full load), meeting EPS regulation with enough margin
- Low standby (pin<0.15 W at no-load condition)
- Soft-start time: 5 ms

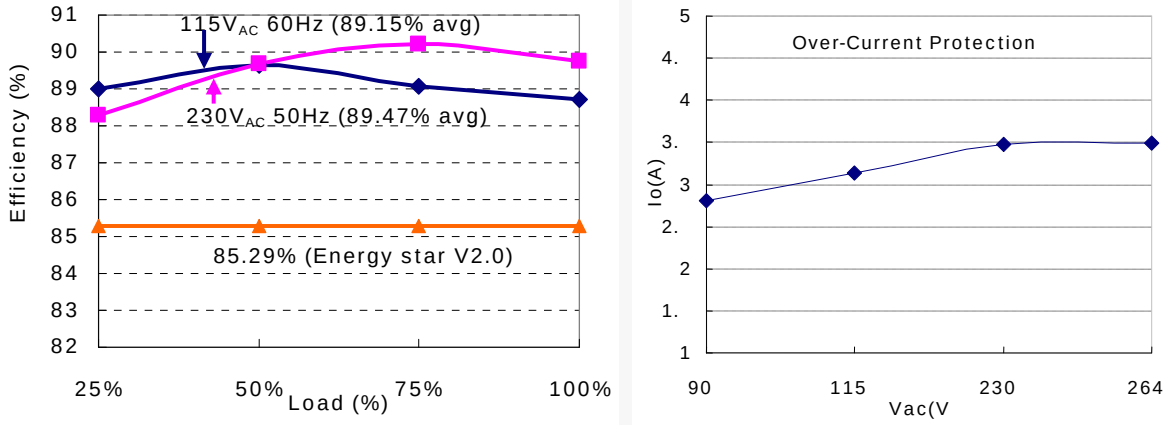


Figure 29. Measured Efficiency and Over-Current Protection

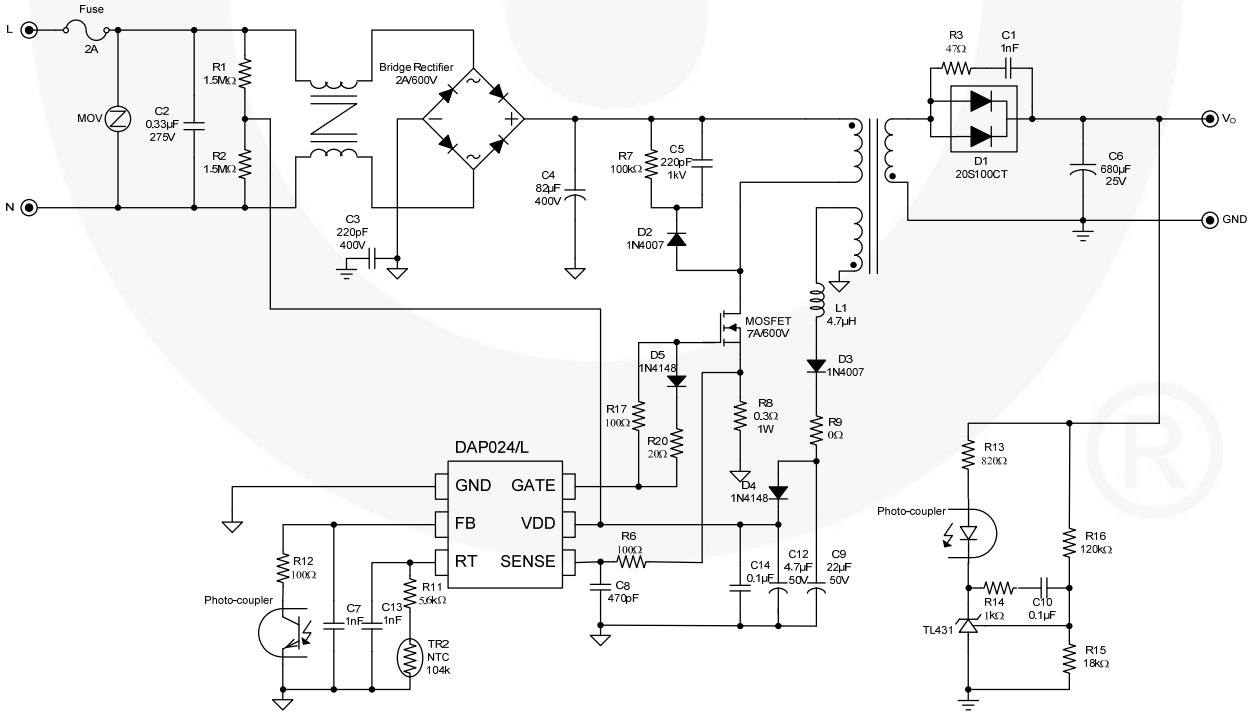
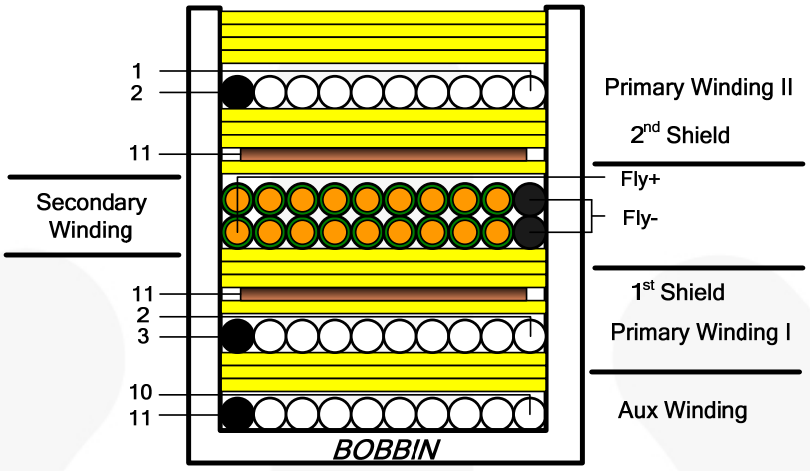


Figure 30. Typical Application Circuit Schematic

Typical Application Circuit (Continued)

Transformer Specification

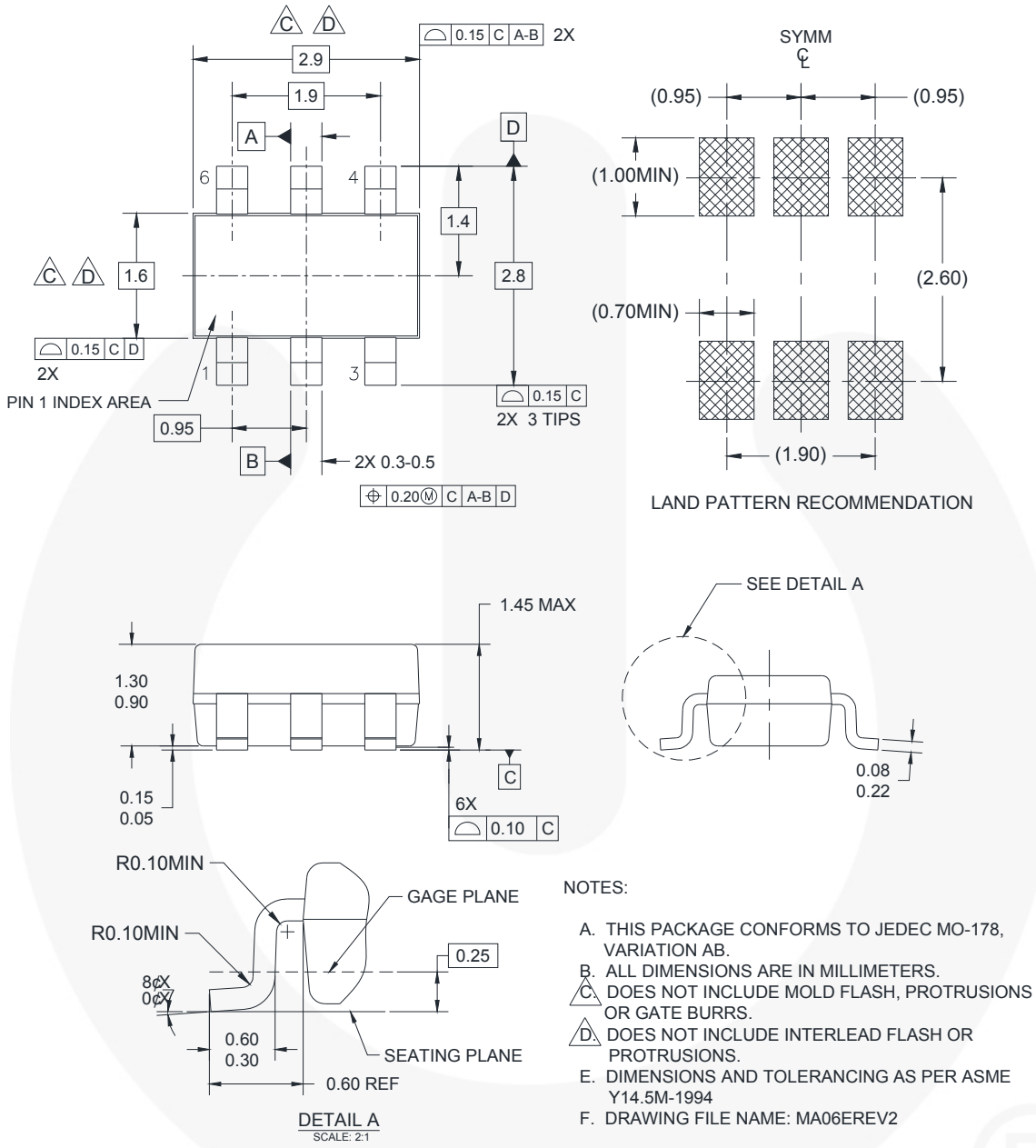
- Core: RM 8
- Bobbin: RM 8



No.	Terminal		WIRE	Ts	Insulation	Barrier	
	S	F			Ts	Primary	Secondary
N1	11	10	0.25*1	9	3		
N2	3	2	0.25* 1	33	1		
	11		COPPER SHIELD	1.2	3		
N3	Fly-	Fly+	0.5* 2	12	1		
	11		COPPER SHIELD	1.2	3		
N4	2	1	0.25 * 1	33	4		
			CORE ROUNDING TAPE		3		

	Pin	Specification	Remark
Primary-Side Inductance	3－1	920 μH ±5%	100kHz, 1V
Primary-Side Effective Leakage	3－1	15 μH Maximum	Short One of the Secondary Windings

Physical Dimensions



NOTES:

A. THIS PACKAGE CONFORMS TO JEDEC MO-178, VARIATION AB.
B. ALL DIMENSIONS ARE IN MILLIMETERS.
C. DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
D. DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
E. DIMENSIONS AND TOLERANCING AS PER ASME Y14.5M-1994
F. DRAWING FILE NAME: MA06EREV2

Figure 31. 6-Lead, SOT23, JEDEC MO-178 Variation AB, 1.6 mm Wide

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