TDA18273HN

Hybrid (analog and digital) Silicon Tuner for terrestrial and cable TV reception

Rev. 2 — 30 July 2010 Objective data sheet

1. General description

The TDA18273HN is a high performance Silicon Tuner designed for terrestrial and cable TV reception for both analog and digital signals.

The TDA18273HN supports all analog and digital TV standards and delivers a LOW IF (LIF) signal to a demodulator for analog TV and/or a channel demodulator for digital TV.

2. Features and benefits

- Fully integrated IF selectivity; eliminating the need for external SAW filters
- Worldwide multistandard terrestrial and cable
- Fully integrated oscillators
- Alignment free
- Single 3.3 V supply voltage
- Power level detector
- Integrated wideband gain control
- Crystal oscillator output buffer (16 MHz) for single crystal applications
- I^2C-bus interface compatible with 3.3 V microcontrollers
- Self AGC synchronization mode (VSYNC)
- Very fast tuning time
- LIF channel center frequency output ranging from 3 MHz to 5 MHz
- 1.7 MHz, 6 MHz, 7 MHz, 8 MHz and 10 MHz channel bandwidths
- Ready for DVB-T2 and DVB-C2
- RoHS compliant
- Strong immunity to spurious and field interferences

3. Applications

- Hybrid (analog and digital TV) for TV, STB, DVD-R and PCTV applications
- All analog (PAL, SECAM, NTSC) and digital (DVB-T/T2/C/C2/H, DTMB, ATSC, ISDB-T) standards supported
- Targeted specification (based on channel decoder or demodulator capabilities):
  - CENELEC EN55020 (EU)
  - NorDig 2.1 (EU TV)
  - Digital terrestrial ATSC A74 compliance (US)
  - NorDig cable (EU)
  - C-BOOK (Cable, EU)

- E-BOOK and D-BOOK 6.1
- ARIB STD-B21 for ISDB-T
- OCUR (US)

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{RF}	RF frequency	full range of RF input	42	-	870	MHz
NF_{tun}	tuner noise figure	75 Ω source; maximum gain	-	4.0	-	dB
φ_{jit}	phase jitter	UHF; integrated from 250 Hz to 4 MHz	-	0.4	0.6	degree
α_{image}	image rejection	worst case for image rejection and 4 MHz IF frequency for levels above 60 dBμV	57.5	63	-	dB
CSO	composite second-order distortion	worst interferer over RF frequency with respect to wanted carrier	-	−60	-	dBc
CTB	composite triple beat	worst interferer over RF frequency with respect to wanted carrier	-	−65	-	dBc
ICP_{1dB}	1 dB input compression point	at tuner input and minimum gain	122	-	-	dBμV

5. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
TDA18273HN/C1	HVQFN40	plastic thermal enhanced very thin quad flat package; no leads; 40 terminals; body 6 × 6 × 0.85 mm	SOT618-1

6. Block diagram

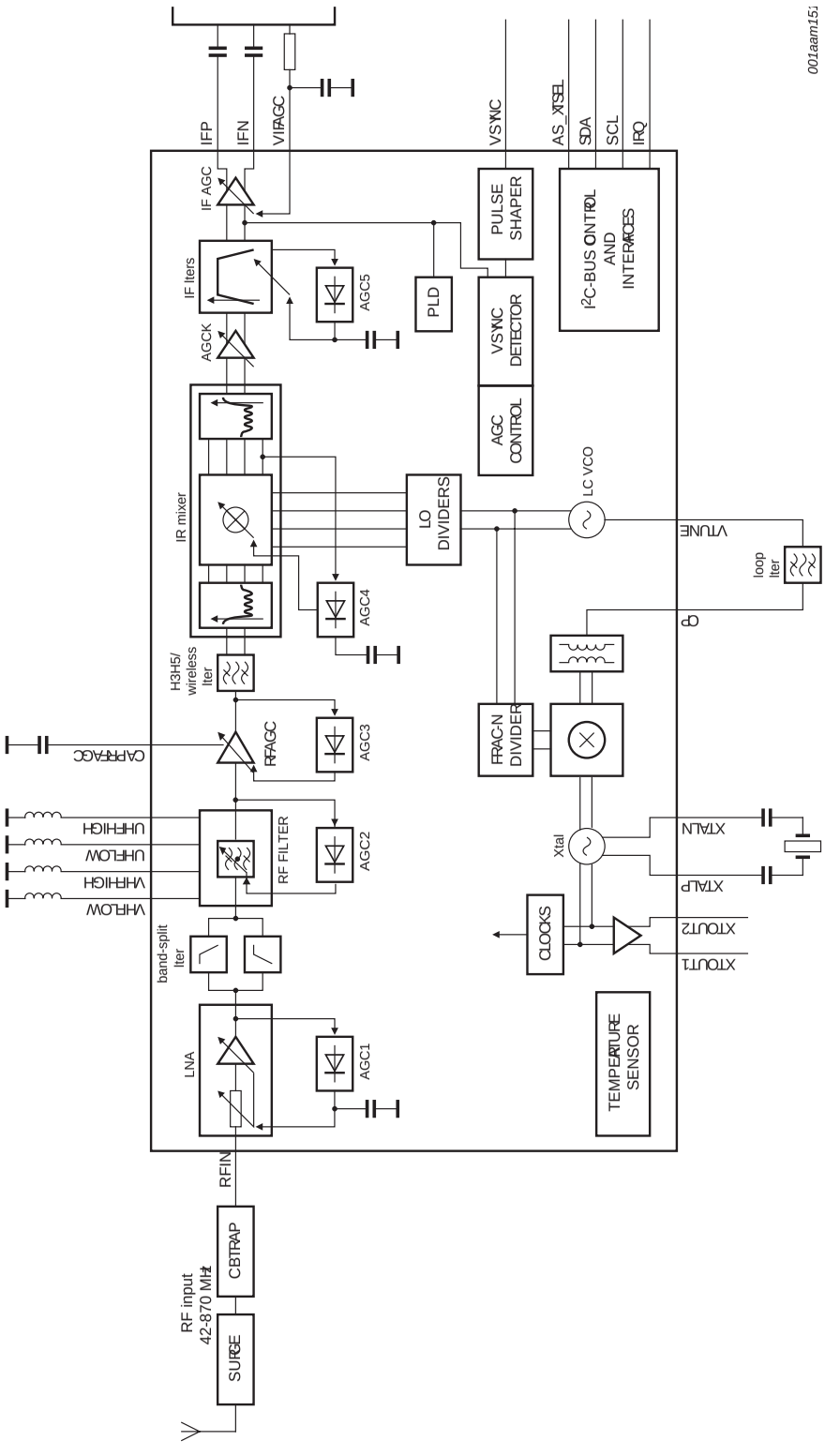
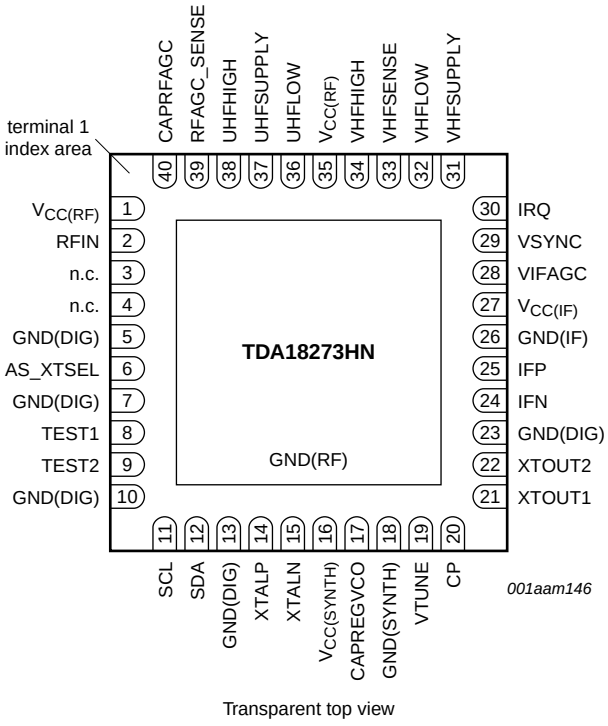


Fig 1. Block diagram

7. Pinning information

7.1 Pinning



Transparent top view

Fig 2. Pin configuration

7.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
$V_{CC(RF)}$	1	RF supply voltage
RFIN	2	unbalanced RF input
n.c.	3	not connected[1]
n.c.	4	not connected[1]
GND(DIG)	5	digital ground
AS_XTSEL	6	I^2C-bus address and XTOUT level selection input
GND(DIG)	7	digital ground
TEST1	8	test input 1, connect to ground for operation mode (GND(DIG))
TEST2	9	test input 2; leave open for operation mode
GND(DIG)	10	digital ground
SCL	11	I^2C-bus clock input
SDA	12	I^2C-bus data input/output
GND(DIG)	13	digital ground
XTALP	14	crystal oscillator positive input

Table 3. Pin description *…continued*

Symbol	Pin	Description
XTALN	15	crystal oscillator negative input
$V_{CC(SYNTH)}$	16	synthesizer supply voltage
CAPREGVCO	17	VCO regulator filtering input
GND(SYNTH)	18	synthesizer ground
VTUNE	19	VCO tuning voltage input
CP	20	charge pump output
XTOUT1	21	crystal oscillator buffer output 1
XTOUT2	22	crystal oscillator buffer output 2
GND(DIG)	23	digital ground
IFN	24	IF negative output
IFP	25	IF positive output
GND(IF)	26	IF ground
$V_{CC(IF)}$	27	IF supply voltage
VIFAGC	28	IF gain control input
VSYNC	29	AGCs synchronization input
IRQ	30	interrupt request output
VHFSUPPLY	31	RF filter VHF supply input
VHFLOW	32	RF filter VHF LOW input
VHFSENSE	33	RF filter VHF sense
VHFHIGH	34	RF filter VHF HIGH input
$V_{CC(RF)}$	35	RF filter supply voltage
UHFLOW	36	RF filter UHF LOW input
UHFSUPPLY	37	RF filter UHF supply input
UHFHIGH	38	RF filter UHF HIGH input
RFAGC_SENSE	39	RF AGC sensor
CAPRFAGC	40	RF AGC filtering
GND(RF)	die pad	RF ground

[1] Not internally connected (no wirebonding). Must not be connected to a fixed potential in the final application

8. Functional description

The Silicon Tuner is based on single down-conversion and LIF architecture that allows full integration of band-pass selectivity and eliminates the need for external SAW filters.

The RF input signal is fed to the Low Noise Amplifier (LNA). Then the signal is applied to an alignment free RF tuned filter to protect the rest of the tuner function against strong unwanted signals.

The LIF concept needs complex signals that highly suppress the N + 1 image channel thanks to image rejection calibration. A complex filter and a IF filter perform the IF selectivity. The IF filter depends on IF frequency choice and channel bandwidth. The IF

filter is built with a IF Low-Pass Filter (LPF), a IF notch filter and a programmable IF High-Pass Filter (HPF) for more flexibility on IF frequency selection. The IF notch filter when activated, suppress the residual adjacent N − 1 sound carrier.

Continuous gain control is performed after the RF filters and the IF selectivity. Stepped AGC is available at all stages (LNA, RF filter, mixer and IF LPF) in order to optimize the tuner signal-to-noise ratio. Internal broadband level detectors control gain settings of all stepped AGC and the RF AGC amplifier. The steps in the different stages are automatically compensated in IF with AGCK to keep a constant IF output level. The demodulator controls the gain of the IF AGC amplifier to take advantage of the full ADC dynamic range.

A single LC-VCO operating in the range from 6 GHz to 7 GHz is used within a FRAC-N phase lock-loop to generate the LO frequency. A crystal oscillator differential input provides the clock reference signal. Demodulators can use this signal through the crystal output buffer.

All the programming is performed via I^2C-bus transceiver. An embedded test tone generator is used for automatic calibration at Power-On-Reset (POR).

The power level indicator is used to indicate the RF input signal strengths of the received channel.

8.1 RF filter

The RF filter block is an alignment free tunable Band-Pass Filter (BPF). At power-up, a self-calibration is performed which compensates for the external and internal components frequency spread. The center frequency is automatically tuned to the frequency set using the I^2C-bus to suppress any unwanted interference across the broadband spectrum.

8.2 Crystal output mode

Pins XTOUT1 and XTOUT2 provide a symmetrical sine waveform which drives the channel demodulator and/or IF demodulator. The load on these outputs must be identical to ensure optimum performance matching. If only one crystal output is used, the unused output must be loaded with the same capacitance value. The XTOUT output level can be set to either 400 mV (p-p) or 800 mV (p-p) single ended, refer Table 32 “Pin AS_XTSEL decoding”.

8.3 AGC description

The tuner gain is composed of different variable gain stages spread according to the block diagram (see Figure 1 “Block diagram”). Using the different detectors at different stages, the gain is distributed to offer best trade-off between linearity and noise. Continuity gain variation is made in 3 dB steps. The AGCK stage compensates the 3 dB steps to ensure gain linearity.

The tuner gain is externally controlled via IFAGC voltage level applied to pin VIFAGC. The RF gain is set automatically, based on the defined AGCn_TOP values.

The different stages gain values are then a combination of the following input parameters:

- Input signal
- TOP values set via I^2C-bus

- IFAGC voltage level

The programmable Take Over Points (TOP) provide the optimal noise versus linearity trade-off during reception. The TOP values are carefully selected so that they do not overload the following stages or have too weak signal-to-noise ratio. They correspond to thresholds where the gain distribution changes inside the tuner.

In order to avoid instability of gain chain while working around thresholds, a hysteresis is implemented to avoid gain toggling. This is the reason why there are different values for TOP-up and/or TOP-down. Its main purpose is to make sure gain switch occurs to prevent signal distortion along the gain chain.

Fast AGC mode is integrated in the IC to speed up the variable gain convergence. The Fast AGC mode is set at channel change, for a large input level step and can be programmed via I^2C-bus for search mode.

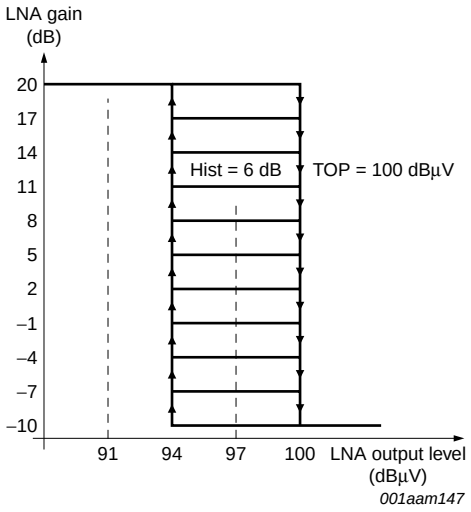


Fig 3. AGC1 TOP description example

The TOP values tuner settings are key for all tuner performance.

Table 4. AGC number/block correspondence

AGC number	corresponding AGC block	comment
AGC1	LNA AGC	
AGC2	RF Filter AGC	programmed after tuner init and must not be changed anymore afterwards
AGC3	RF AGC	
AGC4	Mixer AGC	
AGC5	LPF AGC	

8.4 Harmonic 3 and harmonic 5 filter (H3H5) and wireless network filter

In addition to the RF tuned filters, a H3H5 filter is implemented to prevent broadband down-conversion with third and fifth LO harmonics for off-air reception in case of presence of strong interferer.

In addition to the H3H5 filter, extra wireless network filter is implemented also to prevent broadband down-conversion with 1.7 GHz, 1.8 GHz and 2.4 GHz interferers. The filter is set automatically depending on RF input frequency.

8.5 Low-pass filter (LPF)

The programmable LPF avoids aliasing of demodulators Analog-to-Digital converters. In addition, it suppresses the remaining signals. The programming enables signal bandwidth of 1.7 MHz, 6 MHz, 7 MHz, 8 MHz and 10 MHz.

8.6 High-pass filter (HPF)

The HPF contributes to residual adjacent (N + 1) channel suppression after image rejection removal. It is intended mainly for digital reception.

8.7 Notch filter

This block is implemented in the IF filters to optionally provide additional robustness against adjacent analog channels. It reduces the adjacent channel sound carrier level to prevent overloading of IF output stage. The notch frequency is tracked with LPF settings.

8.8 Self AGC synchronization mode (VSYNC)

A vertical synchronization signal detector is implemented in the IC for negative and positive modulation. The signal is used for synchronization of stepped AGC amplifiers in case of analog TV. When the external VSYNC mode is selected (see Table 28), the external VSYNC signal available at VSYNC pin bypasses the internal generated VSYNC signal. When the internal VSYNC signal is detected, the synchronization is fully integrated.

8.9 VSYNC pulse shape

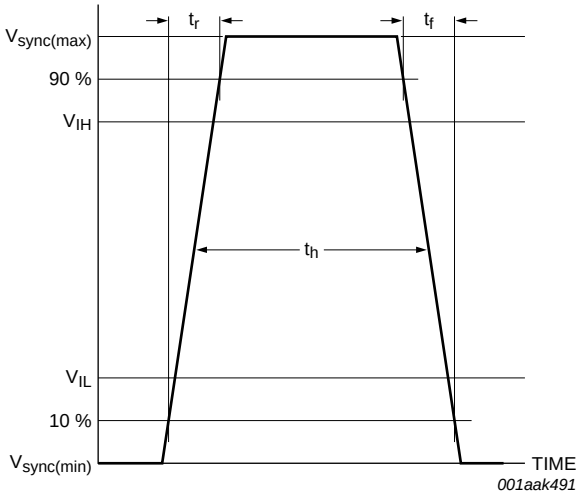


Fig 4. VSYNC pulse shape

Table 5. VSYNC signal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{sync(max)}$	maximum synchronization voltage		-	-	Min(3.6 V, V_{CC} + 0.3 V)	V
$V_{sync(min)}$	minimum synchronization voltage		−0.3	-	-	V
V_{IL}	LOW-level input voltage		-	-	$0.3V_{CC}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{CC}$	-	-	V
t_h	hold time	pulse shaper:				
		disabled	50	-	-	μs
		enabled	0.2	-	100	μs

VSYNC signal provided to the tuner allows tuner gain changes only during vertical synchronization to prevent picture quality degradation during analog reception.

A specific pulse shaper function is available to reshape the signal inside the tuner. The VSYNC signal duration must be according to Table 5.

If the pulse shaper is enabled, as long as t_h exceeds 0.2 μs, the pulse shaper reshapes the VSYNC signal. Should the signal at VSYNC pin be maintained longer than t_h max (100 μs) in Table 5, it would lead to unwanted tuner gain changes that could be visible on the picture during analog reception.

8.10 IR mixer

The LIF concept needs complex signals that highly suppress the N + 1 image channel thanks to image rejection calibration.

8.11 LO generation

A single LC-VCO operating in the range from 6 GHz to 7 GHz is used within a FRAC-N phase lock-loop to generate the LO frequency. A crystal oscillator differential input provides the clock reference signal. This signal is provided to demodulators through the crystal output buffer.

8.12 Temperature sensor

The temperature sensor can be used to indicate the junction temperature of the IC via I²C-bus for soldering check. Refer to Section 9.1.2 for detailed description and operation.

8.13 Power level detector

The power level detector indicates the RF input signal strengths of the received channel via I²C-bus. Refer to Section 9.1.4 for detailed description and operation. The available strength, in a range from 0 dBμV to 127 dBμV, refers to RMS value for digital TV signals channels, RMS value of unmodulated signal during synchronization level of the envelope signal for negative modulated analog TV signals or RMS value of unmodulated signal during black level of the envelope signal for positive modulated analog TV signals.

8.14 I²C-bus transceiver

The TDA18273HN is controlled via the two-wire I²C-bus. There is one device address (7-bit). The read or write mode is selected with the R/W bit. To be able to have more than one tuner in an I²C-bus system, one of two possible addresses is selected depending on the voltage applied to address selection pin AS_XTSEL see Table 32 “Pin AS_XTSEL decoding”.

9. Control interface

9.1 Register table description

Table 6. Register table description

Address (hex)	Name[1]	Bit							
		7	6	5	4	3	2	1	0
00	ID_byte_1	-	Ident[14:8]						
01	ID_byte_2	Ident[7:0]							
02	ID_byte_3	Major_rev[3:0]				Minor_rev[3:0]			
03	Thermo_byte_1	-	TM_D[6:0]						
04	Thermo_byte_2	-							TM_ON
05	Power_state_byte_1	POR	-				AGCs_Lock	VSYNC_Lock	LO_Lock
06	Power_state_byte_2	-						SM	SM_XT
07	Power_Level_byte_1	Power_Level[7:0]							
08	IRQ_status	IRQ_status	-						
09	IRQ_enable	1	-	0					
0A	IRQ_clear	IRQ_clear	-	0					
0B	IRQ_set	0	-	0					
0C	AGC1_byte_1	-				AGC1_TOP_I2C_DN_UP[3:0]			
0D	AGC1_byte_2	-			AGC1_Adapt_TOP_DN_UP[1:0]		AGC1_Mode[2:0]		
0E	AGC2_byte_1	-					1	0	1
0F	AGCK_byte_1	1	1		Pulse_Shape_Disable	0		AGCK_Time_Constant[1:0]	
10	RF_AGC_byte_1	AGC3_TOP_Adapt_Algorithm[1:0]		AGC3_Adapt_TOP[1:0]		1	AGC3_TOP_I2C[2:0]		
11	W_Filter_byte	VHF_III_Mode	RF_Atten_3dB	W_Filter_Enable	1	1	0	W_Filter_Offset[1:0]	
12	IR_MIXER_byte_1	-		S2D_Gain[1:0]		AGC4_TOP_DN_UP[3:0]			
13	AGC5_byte_1	-	1	1	AGC5_HPF	AGC5_TOP_DN_UP[3:0]			
14	IF_AGC_byte	IFnotchToRSSI	0	-			IF_Level[2:0]		
15	IF_byte_1	IF_HP_Fc[1:0]		IF_Notch	LP_FC_Offset[1:0]		LP_Fc[2:0]		

Table 6. Register table description *…continued*

Address (hex)	Name[1]	Bit							
		7	6	5	4	3	2	1	0
16	Reference_byte	Digital_Clock[1:0]		-	0	-		XTout_Mode[1:0]	
17	IF_Frequency_byte	IF_Freq[7:0]							
18	RF_Frequency_byte_1	-				RF_Freq[19:16]			
19	RF_Frequency_byte_2	RF_Freq[15:8]							
1A	RF_Frequency_byte_3	RF_Freq[7:0]							
1B	MSM_byte_1	0	RF_CAL_AV	RF_CAL	IR_CAL[1:0]		0	RC_CAL	Calc_PLL
1C	MSM_byte_2	-						0	MSM_Launch
1D	PowerSavingMode	0	1	0					
1E	Power_Level_byte_2	0							
1F	Adapt_TOP_byte	-	Fast_Mode_AGC	1	0	1	0	1	1
20	VSYNC_byte	Negative_Modulation	0		Internal_VSYNC	0			
21	VSYNC_Mgt_byte	0				1	0		1
22	IR_MIXER_byte_2	0	1	1	-			HI_Pass	DC_Notch_IF_PPF
23	AGC1_byte_3	0	1	0		1	0	1	0
24	RFAGCs_Gain_byte_1	1	0	1	1	-	RFAGC_Sense_Enable	0	
25	RFAGCs_Gain_byte_2	0							
26	AGC5_byte_2	0	1	1	-	0		1	0
27	RF_Cal_byte_1	0					1	0	
28	RF_Cal_byte_2	0	1	1	0	1	1	1	1
29	RF_Cal_byte_3	0	1	0					
2A	Bandsplit_Filter_byte	-						1	0
2B	RF_Filters_byte_1	0	-	0		1	1	1	1
2C	RF_Filters_byte_2	0							
2D	RF_Filters_byte_3	0	1	0					
2E	RF_Band_Pass_Filter_byte	0	-				1	1	0
2F	CP_Current_byte	0	1	0		1	1	0	1
30	AGCs_DetOut_byte	X	X	X	X	X	X	X	X

Table 6. Register table description *…continued*

Address (hex)	Name[1]	Bit							
		7	6	5	4	3	2	1	0
31	RFAGCs_Gain_byte_3	-		RF_Filter_Gain[1:0]		LNA_Gain[3:0]			
32	RFAGCs_Gain_byte_4	X	X	X	X	X	X	X	X
33	RFAGCs_Gain_byte_5	RFAGC_K_Read[8]	X	X	X	X	TOP_AGC3_Read[2:0]		
34	RFAGCs_Gain_byte_6	RFAGC_K_Read[7:0]							
35	IFAGCs_Gain_byte	-		LOWPASS_Gain[2:0]			Mixer_Gain[2:0]		
36	RSSI_byte_1	X	X	X	X	X	X	X	X
37	RSSI_byte_2	-		0	-	1	0		
38	Misc_byte_1	1	0			-		0	IRQ_Polarity
39	rfcal_log_0	rfcal_log_0[7:0]							
3A	rfcal_log_1	rfcal_log_1[7:0]							
3B	rfcal_log_2	rfcal_log_2[7:0]							
3C	rfcal_log_3	rfcal_log_3[7:0]							
3D	rfcal_log_4	rfcal_log_4[7:0]							
3E	rfcal_log_5	rfcal_log_5[7:0]							
3F	rfcal_log_6	rfcal_log_6[7:0]							
40	rfcal_log_7	rfcal_log_7[7:0]							
41	rfcal_log_8	rfcal_log_8[7:0]							
42	rfcal_log_9	rfcal_log_9[7:0]							
43	rfcal_log_10	rfcal_log_10[7:0]							
44	rfcal_log_11	rfcal_log_11[7:0]							
50	-	FORBIDDEN ACCESS							
6C	-	FORBIDDEN ACCESS							
FE	-	FORBIDDEN ACCESS							
FF	-	FORBIDDEN ACCESS							

[1] The settings optimization is bound to channel decoder or demodulator choice and has a high impact on the tuner performances within system environment. Refer to application note for optimal settings.

Remark:

- The values in Table 6 must be written as described for operation mode of the tuner.

- X means the tuner provides the value 0 or 1.
- - means the value is undefined. No internal bit corresponds to this address.

9.1.1 Device type address ID

Table 7. ID byte bit descriptions

Address	Register	Bit	Symbol	Access	Value	Description
00	ID_byte_1	6 to 0	Ident[14:8]	R	18273	type number information
01	ID_byte_2	7 to 0	Ident[7:0]			
02	ID_byte_3	7 to 4	Major_rev[3:0]	R	1	current major releases
		3 to 0	Minor_rev[3:0]	R	1	current minor releases

9.1.2 Temperature sensor

Table 8. Temperature sensor bit descriptions

Address	Register	Bit	Symbol	Access	Value		Description
03	Thermo_byte_1	6 to 0	TM_D[6:0]	R	-		a junction temperature measurement ranging from 22 °C to 127 °C is indicated through these bits
					16		temperature ≤ 22 °C
						[1]	22 °C < temperature < 127 °C
					7F		temperature ≥ 127 °C
04	Thermo_byte_2	0	TM_ON	W			temperature sensor ON or OFF
					0		temperature sensor switched OFF
					1		temperature sensor switched ON

[1] The temperature sensor value is read directly in binary on the byte Thermo_byte_1, if TM_ON is set to 1, with a 2 °C accuracy.

Remark: The temperature sensor value is updated each time a read is performed on the byte Thermo_byte_1, if TM_ON is set to 1. Otherwise, temperature sensor value is not updated.

9.1.3 Power state

Table 9. Power state bit descriptions

Address	Register	Bit	Symbol	Access	Value	Description
05	Power_state_byte_1	7	POR	R		detects when the tuner supply voltage went below POR threshold voltage. The tuner is then reset to its original settings (tuner not initialized).
					0	once it has been read
					1	the POR occurred on the tuner
		2	AGCs_Lock			flag indicator of AGC behavior
					0	indicates that the gain is being settled to the right value
					1	indicates that the gain is settled to the right value
		1	VSYNC_Lock			VSYNC flag
					0	indicates that the VSYNC signal is not detected during a delay of 40 ms
					1	VSYNC locked: VSYNC signal is available for analog TV standard
		0	LO_Lock	R		LO lock flag
					0	PLL unlocked
					1	PLL locked
06	Power_state_byte_2	1	SM[1]	R/W	[2]	sleep mode control bits
		0	SM_XT[1]	R/W	[2]	

[1] SM and SM_XT do not act directly on the circuit. Only the right combinations of both bits are meaningful.

[2] See Table 10.

Table 10. Mode selection

SM[1]	SM_XT[1]	Mode
0	0	operation mode = ON
1	0	Standby mode with Xtal ON; the chip is in Standby mode but it still delivers Xtal signal.
1	1	Standby mode with Xtal OFF; the chip is in Standby mode but it does not deliver Xtal signal.

[1] All others values are forbidden.

Remark:

- If the IC is in operation mode, to set the Standby mode:
  - Set the digital clock to 16 MHz (see Table 24)
  - Put the chip in Standby mode: SM = 1 and SM_XT = X
- If the IC is in Standby mode, to set the operation mode
  - Put the chip in operation mode: SM = 0 and SM_XT = 0
  - Set the required digital clock (see Table 24)

9.1.4 Power level detector

Table 11. Power level detector bit descriptions

Address	Register	Bit	Symbol	Access	Value	Description
07	Power_Level_byte_1	7 to 0	Power_Level[7:0]	R	-	gives the power value measured at antenna input[1]
					0	power < 0 dBμV (RMS)
					[2]	0 dBμV (RMS) ≤ power ≤ 127 dBμV (RMS)
					3F	power > 127 dBμV (RMS)

[1] Power_Level value can be used if the bit PD_PLD_read = 0 (bit: 7, address: 1E).

[2] The power level value is read in the range from 0 dBμV (RMS) to 127 dBμV (RMS) with 0.5 dBμV (RMS) step.

9.1.5 IRQ

Table 12. IRQ bit descriptions

Address	Register	Bit	Symbol	Access	Value	Description
08	IRQ_status	7	IRQ_status	R/W	0	IRQ_clear is set to 1
					1	all calibration sequences selected by MSM_byte_1 and launched by MSM_byte_2 are completed
0A	IRQ_clear	7	IRQ_clear	R/W	0	no action
					1	drops the bit IRQ_status

Remark: A level change is generated on IRQ pin that reflects the IRQ_status bit. The polarity of the IRQ pin is set with IRQ_Polarity bit (address: 38). In operation mode, the IRQ status raised at the end of the calibration sequence selected with MSM_byte_1 and MSM_byte_2 and at each programming of a new channel.

9.1.6 AGC and Take Over Points (TOP)

Table 13. AGC and Take Over Points bit descriptions

Address	Register	Bit	Symbol	Access	Value	Description
0C	AGC1_byte_1	3 to 0	AGC1_TOP_I2C_DN_UP[3:0]	R/W	[1]	sets the TOP of the LNA detection loop (AGC1) in accordance with the reception standard or the system settings
0D	AGC1_byte_2	4 to 3	AGC1_Adapt_TOP_DN_UP[1:0]	R/W		sets the TOP of the LNA detection loop (AGC1) in accordance with the AGC1 algorithm
		2 to 0	AGC1_Mode[2:0]	R/W	<tbd>	sets the AGC1 algorithm in accordance with the reception standard or the system settings
0F	AGCK_byte_1	4	Pulse_Shape_Disable	R/W	0	the pulse signal applied on VSYNC pin is directly transmitted to the digital part
					1	the pulse duration is internally increased to 500 μs
		1 to 0	AGCK_Time_Constant[1:0]	R/W	[2]	control AGC modes according to required reception mode. It sets the time reference for AGC changes

Table 13. AGC and Take Over Points bit descriptions *…continued*

Address	Register	Bit	Symbol	Access	Value	Description
10	RF_AGC_byte_1	7 to 6	AGC3_TOP_Adapt_Algorithm[1:0]	R/W	<tbd>	sets these bits according to the required reception standard and performances
		5 to 4	AGC3_Adapt_TOP[1:0]	R/W	<tbd>	AGC3_Adapt_TOP[1:0] changes the AGC3 TOP value if the AGC3 TOP adapt algorithm is activated. Sets these bits according to the required reception standard and performance.
		2 to 0	AGC3_TOP_I2C[2:0]	R/W	[3]	sets the RF AGC blocks TOP. Sets these bits according to the required reception standard and performances
11	W_Filter_byte	6	RF_Atten_3dB	R/W		Adds 3 dB attenuation out of RF AGC
					0	OFF
					1	ON
12	IR_MIXER_byte_1	5 to 4	S2D_Gain[1:0]	R/W	[4]	sets the gain of the single to balance block
		3 to 0	AGC4_TOP_DN_UP[3:0]	R/W	[5]	sets the MIXER blocks TOP. Sets these bits according to the required reception standard and performances
13	AGC5_byte_1	4	AGC5_HPF	R/W		turns HPF in AGC5 detection loop
					0	OFF
					1	ON
		3 to 0	AGC5_TOP_DN_UP[3:0]	R/W	[6]	sets the LPF blocks TOP. Sets these bits according to the required reception standard and performances
14	IF_AGC_byte	2 to 0	IF_Level[2:0]	R/W	[7]	sets the tuner required maximum output level. This enables internal computation of the best linearity to noise ratio based on required output level. Must be set in accordance with the ADC scale that will use IF outputs
1F	Adapt_TOP_byte	6	Fast_Mode_AGC	R/W		speed up the AGC settling time during search mode
					0	OFF
					1	ON

[1] See Table 15.

[2] See Table 14.

[3] See Table 16.

[4] See Table 20.

[5] See Table 17.

[6] See Table 18.

[7] See Table 19.

Table 14. AGCK Time Constant values

AGCK_Time_Constant[1:0] (hex)[1]	Reference signal
0	V_{SYNC}
1	0.5 ms
2	8 ms
3	32 ms

[1] All others values are forbidden.

Table 15. AGC1 TOP values

AGC1_TOP_I2C_DN_UP[3:0] (hex)[1]	AGC1 TOP Down (dBμV)	AGC1 TOP Up (dBμV)
1	90	84
2	91	86
4	95	89
5	96	84
A	100	94

[1] All others values are forbidden.

Table 16. AGC3 TOP values

AGC3_TOP_I2C[2:0] (hex)	AGC3 TOP (dBμV)
0	94
1	96
2	98
3	100
4	102
5	104
6	106
7	107

Table 17. AGC4 TOP values

AGC4_TOP_DN_UP[3:0] (hex)[1]	AGC4 TOP Down (dBμV)	AGC4 TOP Up (dBμV)
1	105	100
4	107	102
6	108	103
8	109	104
B	110	105
E	112	107

[1] All others values are forbidden.

Table 18. AGC5 TOP values

AGC5_TOP_DN_UP[3:0] (hex)[1]	AGC5 TOP Down (dBμV)	AGC5 TOP Up (dBμV)
1	105	100
4	107	102
6	108	103
8	109	104
B	110	105
E	112	107

[1] All others values are forbidden.

Table 19. Tuner output level

IF_Level[2:0] (hex)	Output level (V (p-p) differential)[1]	Minimum gain (dB)	Maximum gain (dB)
7	0.5	−12	+18
6	0.6	−10.3	+19.7
5	0.7	−9	+21
4	0.85	−7.5	+22.5
3	0.8	−8	+22
2	1	−6	+24
1	1.25	−4	+26
0	2	0	+30

[1] Output level depends on standard and ADC headroom.

Table 20. Single to balance gain

S2B_Gain[1:0] (hex)[1]	gain (dB)
0	3
1	6
2	9

[1] All others values are forbidden.

9.1.7 H3H5 and wireless network filter

Table 21. H3H5 and Wireless network filter bit descriptions

Address	Register	Bit	Symbol	Access	Value	Description
11	W_Filter_byte	7	VHF_III_Mode	R/W		switches the H3H5 filter in VHFIII mode from 174 MHz to 230 MHz
					0	OFF
					1	ON
		5	W_Filter_Enable	R/W		enables the wireless filter implemented in order to prevent down-conversion with 1.7 GHz, 1.8 GHz and 2.4 GHz interferers
					0	OFF
					1	ON
		1 to 0	W_Filter_Offset[1:0]	R/W		enables offset to wireless filter notch frequency
					00	+4 %
					01	0 %
					10	−4 %
					11	−8 %

9.1.8 IF Filtering

Table 22. IF Filtering bit descriptions

Address	Register	Bit	Symbol	Access	Value	Description
14	IF_AGC_byte	7	IFnotchToRSSI	R/W		rejects the sound carrier at the RSSI detector input
					0	OFF
					1	ON

Table 22. IF Filtering bit descriptions *…continued*

Address	Register	Bit	Symbol	Access	Value	Description
15	IF_byte_1	7 to 6	IF_HP_Fc[1:0]	R/W		tunes the IF HPF cut-off frequency. The high-pass frequency is set according to the required reception standard. High-pass frequency:
					00	0.4 MHz
					01	0.85 MHz
					10	1 MHz
					11	1.5 MHz
		5	IF_Notch	R/W		enables or disables a notch filter embedded for adjacent N − 1 sound carrier suppression. The notch frequency depends on LP_Fc[2:0].
					0	OFF
					1	ON
		4 to 3	LP_FC_Offset[1:0]	R/W		enables offset to LPF cut-off frequency providing further adjacent channel rejection
					00	0
					01	−4 %
					10	−8 %
					11	forbidden
		2 to 0	LP_Fc[2:0]	R/W	[1]	selects the IF LPF cut-off frequency. It is set according to required reception standard.
22	IR_MIXER_byte_2	1	HI_Pass	R/W	-	enables or disables an IF HPF implemented for adjacent N + 1 suppression
					0	OFF
					1	ON
		0	DC_Notch_IF_PPF	R/W		enables or disables a DC notch implemented in the IR MIXER
					0	OFF
					1	ON

[1] See Table 23.

Table 23. LPF bits descriptions

LP_Fc[2:0] (hex)[1]	LP cut-off frequency (MHz)	IF notch frequency (MHz)
4	1.7	-
0	6	6.5
1	7	7.25
2	8	8.25
3	9	-

[1] All others values are forbidden.

9.1.9 Digital clock and XTOUT

Table 24. Digital clock and XTOUT bit descriptions

Address	Register	Bit	Symbol	Access	Value	Description
16	Reference_byte	7 to 6	Digital_Clock[1:0]	R/W		selects the digital clock to improve tuner EMC behavior
					x0	Xtal 16 MHz
					11	Sub division of LO frequency
		1 to 0	XTout_Mode[1:0]	R/W		provides 16 MHz reference signal on the XTOUT1 and XTOUT2 pins. XTOUT mode:
					00	no signal
					01	forbidden
					10	forbidden
					11	16 MHz

9.1.10 IF and RF frequency

Table 25. IF and RF frequency bit descriptions

Address	Register	Bit	Symbol	Access	Value	Description
17	IF_Frequency_byte	7 to 0	IF_Freq[7:0]	R/W	-	sets the tuner to the required IF frequency by 50 kHz steps. For example, to set the IF frequency to 4 MHz, IF_Freq[7:0] value must be 4000 : 50 = 80
18	RF_Frequency_byte_1	3 to 0	RF_Freq[19:16]	R/W	-	sets the required RF frequency expressed in kHz
19	RF_Frequency_byte_2	7 to 0	RF_Freq[7:0]	R/W	-	
1A	RF_Frequency_byte_3	7 to 0	RF_Freq[15:8]	R/W	-	

9.1.11 Calibration controls

Table 26. Calibration control bit descriptions

Address	Register	Bit	Symbol	Access	Value	Description
1B	MSM_byte_1	6	RF_CAL_AV	R/W	-	sets these bits according to the programming flowchart (see Figure 5) to control the calibration and calculation state machines embedded in the chip
		5	RF_CAL	R/W	-	
		4 to 3	IR_CAL[1:0]	R/W	-	
		1	RC_CAL	R/W	-	
		0	Calc_PLL	R/W	-	
1C	MSM_byte_2	0	MSM_Launch	R/W	-	

9.1.12 Gain values

Table 27. AGC bit descriptions

Address	Register	Bit	Symbol	Access	Value	Description
24	RFAGCs_Gain_byte_1	2	RFAGC_Sense_Enable	R/W		enables to read the voltage VRFAGC on the pin RFAGC_SENSE (pin 39)
					0	OFF
					1	ON

Table 27. AGC bit descriptions *…continued*

Address	Register	Bit	Symbol	Access	Value	Description
31	RFAGCs_Gain_byte_3	5 to 4	RF_Filter_Gain[1:0]	R		RF FILTER gain value:
					00	−11 dB
					01	−8 dB
					10	−5 dB
					11	−2 dB
		3 to 0	LNA_Gain[3:0]	R	[1]	LNA gain value:
					0000	−10 dB
					0001	−7 dB
					0010	−4 dB
					0011	−1 dB
					0100	2 dB
					0101	5 dB
					0110	8 dB
					0111	11 dB
					1000	14 dB
					1001	17 dB
					1010	20 dB
33	RFAGCs_Gain_byte_5	7	RFAGC_K_Read[8]	R	-	RFAGCK_Read[8:0] gives the RFAGC gain values
		2 to 0	TOP_AGC3_Read[2:0]	R		gives the AGC3 TOP value:
					000	94 dBμV (RMS)
					001	96 dBμV (RMS)
					010	98 dBμV (RMS)
					011	100 dBμV (RMS)
					100	102 dBμV (RMS)
					101	104 dBμV (RMS)
					110	106 dBμV (RMS)
					111	107 dBμV (RMS)
34	RFAGCs_Gain_byte_6	7 to 0	RFAGC_K_Read[7:0]	R	-	RFAGCK_Read[8:0] gives the RFAGC gain values

Table 27. AGC bit descriptions *…continued*

Address	Register	Bit	Symbol	Access	Value	Description
35	IFAGCs_Gain_byte	5 to 3	LOWPASS_Gain[2:0]	R		LPF gain value:
					000	−6 dB
					001	−3 dB
					010	0 dB
					011	3 dB
					100	6 dB
					101	9 dB
					110	12 dB
					111	15 dB
		2 to 0	Mixer_Gain[2:0]	R	[1]	gives the IR MIXER gain value:
					000	2 dB
					001	5 dB
					010	8 dB
					011	11 dB
					100	14 dB

[1] Other values are forbidden.

9.1.13 VSYNC

Table 28. VSYNC bit descriptions

Address	Register	Bit	Symbol	Access	Value	Description
20	VSYNC_byte	7	Negative_Modulation	R/W		indicates that the input signal modulation is negative or positive
					0	positive modulation
					1	negative modulation
		4	Internal_VSYNC	R/W		selects the internal VSYNC generator
					0	external VSYNC
					1	internal VSYNC generator

9.1.14 IRQ polarity

Table 29. IRQ polarity bit descriptions

Address	Register	Bit	Symbol	Access	Value	Description
38	Misc_byte_1	0	IRQ_Polarity	R/W		selects the IRQ pin polarity. IRQ pin output voltage when IRQ raised:
					0	V_{CC}
					1	0

9.1.15 rfcal_log

These bytes provide the outcome of the RF filter calibration. It can be used as an indicator regarding RF filter robustness implementation on PCB.

Table 30. rfcal_log bit descriptions

Address	Register	Bit	Symbol	Access	Value	Description
39	rfcal_log_0	7 to 0	rfcal_log_0[7:0]	R	-	provides RF filter calibration results according to the following convention: Bit [7] are set to 1 in case of calibration error Bit [6:0] is a signed number indicating the number of switch capacitors
3A	rfcal_log_1	7 to 0	rfcal_log_1[7:0]	R	-	
3B	rfcal_log_2	7 to 0	rfcal_log_2[7:0]	R	-	
3C	rfcal_log_3	7 to 0	rfcal_log_3[7:0]	R	-	
3D	rfcal_log_4	7 to 0	rfcal_log_4[7:0]	R	-	
3E	rfcal_log_5	7 to 0	rfcal_log_5[7:0]	R	-	
3F	rfcal_log_6	7 to 0	rfcal_log_6[7:0]	R	-	
40	rfcal_log_7	7 to 0	rfcal_log_7[7:0]	R	-	
41	rfcal_log_8	7 to 0	rfcal_log_8[7:0]	R	-	
42	rfcal_log_9	7 to 0	rfcal_log_9[7:0]	R	-	
43	rfcal_log_10	7 to 0	rfcal_log_10[7:0]	R	-	
44	rfcal_log_11	7 to 0	rfcal_log_11[7:0]	R	-	

9.1.16 Forbidden

Table 31. Forbidden bit descriptions

Address	Register	Bit	Symbol	Access	Value	Description
50 to 6C	-	7 to 0	-	-	-	do not write or read these bytes. Any modification of these bits can lead to performance degradation.
FE	-	7 to 0	-	-	-	
FF	-	7 to 0	-	-	-	

9.2 Tuner programming sequences using IRQ

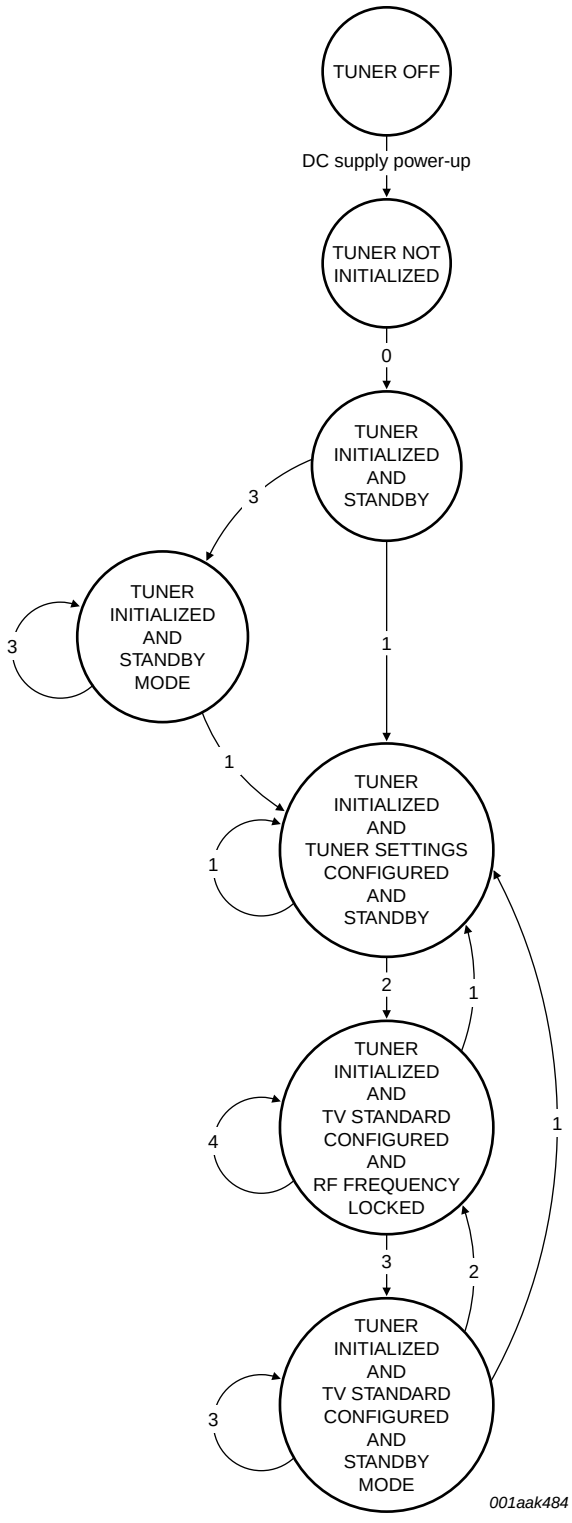


Fig 5. Tuner programming sequence with IRQ

9.3 Channel change programming required parameters

9.3.1 Same reception mode

The new channel to be programmed is within the same standard as the previous one (same channel demodulator).

To be programmed:

- RF frequency
- MSM byte

9.3.2 Different reception mode

The new channel to be programmed is from a different standard compared to the previous one (different channel demodulator).

To be programmed:

- AGC TOP
- IF frequency
- IF output level
- IF bandwidth
- RF frequency
- MSM byte

10. Hardware settings

10.1 XTOUT output level and I²C-bus address

Table 32. Pin AS_XTSEL decoding

Pin AS_XTSEL	Tuner write address (hex)	Tuner read address (hex)	Tuner status
0 V to 0.1 × V_{CC}	C0	C1	XTOUT 400 mV (p-p); single ended
0.2 × V_{CC} to 0.3 × V_{CC}	C0	C1	XTOUT 800 mV (p-p); single ended
0.4 × V_{CC} to 0.6 × V_{CC}	C6	C7	XTOUT 400 mV (p-p); single ended
0.9 × V_{CC} to V_{CC}	C6	C7	XTOUT 800 mV (p-p); single ended

11. Internal circuitry

Table 33. Internal circuits for each pin

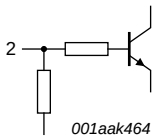
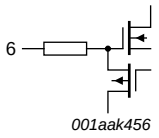
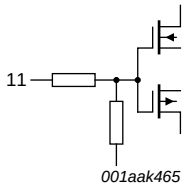
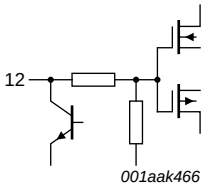
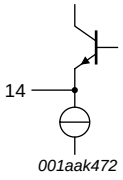
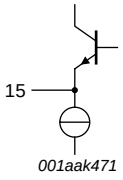
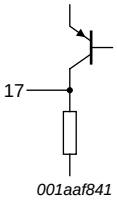
Symbol	Pin	Description[1]
RFIN	2	
AS_XTSEL	6	
SCL	11	
SDA	12	
XTALP	14	
XTALN	15	
CAPREGVCO	17	

Table 33. Internal circuits for each pin *…continued*

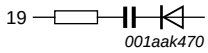
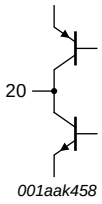
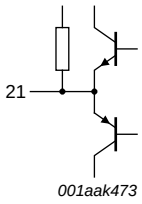
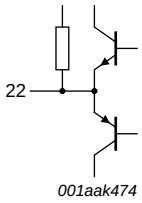
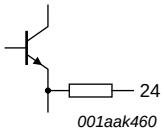
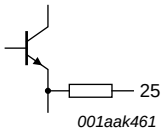
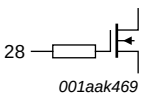
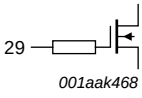
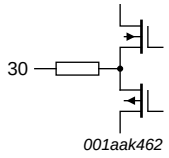
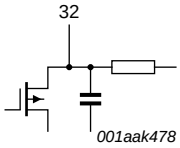
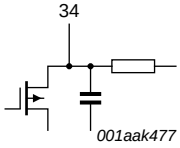
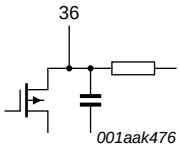
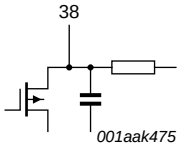
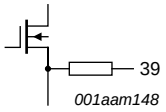
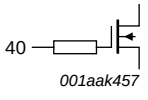
Symbol	Pin	Description[1]
VTUNE	19	
CP	20	
XTOUT1	21	
XTOUT2	22	
IFN	24	
IFP	25	
VIFAGC	28	
VSYNC	29	

Table 33. Internal circuits for each pin *…continued*

Symbol	Pin	Description[1]
IRQ	30	
VHFLOW	32	
VHFHIGH	34	
UHFLOW	36	
UHFHIGH	38	
RFAGC_SENSE	39	
CAPRFAGC	40	

[1] ESD protection components are not shown.

12. Limiting values

Table 34. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		–0.3	+3.6	V
V_I	input voltage	V_{CC} < 3.3 V	–0.3	V_{CC} + 0.3	V
		V_{CC} > 3.3 V	–0.3	+3.6	V
T_{stg}	storage temperature		–40	+150	°C
T_j	junction temperature		-	120	°C
T_{amb}	ambient temperature		–20	[1]	°C
V_{ESD}	electrostatic discharge voltage	EIA/JESD22-A114 (HBM)	–2	+2	kV
		EIA/JESD22-C101-C (FCDM) class III[2]	750	-	V

[1] The maximum allowed ambient temperature $T_{amb(max)}$ depends on the assembly conditions of the package and especially on the design of the Printed-Circuit Board (PCB) and die connection. The application mounting must be done in such a way that the maximum junction temperature is never exceeded. The junction temperature can be obtained by reading the temperature sensor bit via I^2C-bus as explained in Section 9.1.2 “Temperature sensor”. The junction temperature: $T_j = T_{amb} + \Delta T_{j-c}$. where ΔT_{j-c} = power × R_{th}.

[2] Class III: 500 V to 1000 V

13. Thermal characteristics

Table 35. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	according to JEDEC specification 4L board with 9 thermal vias[1][2][3]	31.4	K/W

[1] Measured in free air as defined by JEDEC standard.

[2] These values are given for information only. The thermal resistance depends strongly on the nature and design of the PCB used in the application. The thermal resistance given corresponds to the value that can be measured on a multilayer PCB (4 layers) as defined by JEDEC standard.

[3] The junction temperature influences strongly the reliability of an IC. The PCB used in the application contributes in a large part to the overall thermal characteristic. It must therefore be ensured that the junction temperature of the IC never exceeds $T_{j(max)}$ = 125 °C at the maximum ambient temperature.

14. Characteristics

Table 36. General characteristics for TV reception (RF input to IF output)

T_{amb} = 25 °C; V_{CC} = 3.3 V; IF output level option 1 V (p-p); IF output load of 1 kΩ/1 pF; AGC1 TOP: 95 dBμV/89 dBμV; AGC3 TOP: 96 dBμV; AGC4 TOP: 105 dBμV/100 dBμV; AGC5 TOP: 105 dBμV/100 dBμV; IF_Level[2:0]: –6 dB/+24 dB; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		3.13	3.30	3.47	V
$V_{O(p-p)(max)}$	maximum peak-to-peak output voltage	differential IF output	0.5	-	2	V
I_{CC}	supply current	operation mode	250	300	330	mA
		Standby mode:				
		only crystal oscillator ON	<tbd>	14	<tbd>	mA

Table 36. General characteristics for TV reception (RF input to IF output) *...continued*

T_{amb} = 25 °C; V_{CC} = 3.3 V; IF output level option 1 V (p-p); IF output load of 1 kΩ/1 pF; AGC1 TOP: 95 dBμV/89 dBμV; AGC3 TOP: 96 dBμV; AGC4 TOP: 105 dBμV/100 dBμV; AGC5 TOP: 105 dBμV/100 dBμV; IF_Level[2:0]: −6 dB/+24 dB; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{RF}	RF frequency	full range of RF input		42	-	870	MHz
		analog TV reception; picture		43.25	-	863.25	MHz
		center of channel		45	-	866	MHz
f_{lo}	local oscillator frequency	for respective IF frequency		50	-	870.25	MHz
VSWR	voltage standing wave ratio	RF input; 75 Ω nominal impedance, level below 95 dBμV		-	2.6	3	-
NF_{tun}	tuner noise figure	75 Ω source; maximum gain		-	4.0	-	dB
		75 Ω source; 60 dBμV condition	[1]	-	-	-	dB
$G_{v(max)}$	maximum voltage gain	all bands		<tbd>	94	<tbd>	dB
$G_{v(min)}$	minimum voltage gain	all bands		<tbd>	−32	<tbd>	dB
ΔG_{rsd}	residual gain variation	in case of RF gain change	[2]	-	-	0.8	dB
$\Delta G_{AGC(tun)}$	tuner AGC gain range			-	131	-	dB
$\Delta G_{AGC(IF)}$	IF AGC gain range	range measured between 0 V to 2 V	[3]	29	30	31	dB
ICP_{1dB}	1 dB input compression point	at tuner input and minimum gain		122	-	-	dBμV
φ_n	phase noise	UHF and VHF bands:					
		at 250 Hz frequency offset		-	−90	-	dBc/Hz
		at 1 kHz frequency offset		-	−94	−85	dBc/Hz
		at 10 kHz frequency offset		-	−93	−87	dBc/Hz
		at 100 kHz frequency offset		-	−106.5	−103	dBc/Hz
$t_{startup(tun)}$	tuner start-up time	end of hardware initialization, using a 400 kHz I^2C-bus speed	[4]	-	600	1500	ms
t_{set}	setting time	tuner channel change		-	-	5	ms
$IP3_I$	input third-order intercept point	gain corresponding to 100 dBμV	[5]	120	132	-	dBμV
$IP2_I$	input second-order intercept point	gain corresponding to 100 dBμV	[5]	150	165	-	dBμV
φ_{jit}	phase jitter	UHF; integrated from 250 Hz to 4 MHz		-	0.4	0.6	degree
$f_{-3dB(hpf)}$	high-pass filter cut-off frequency	3 dB cut-off frequency:	[6]				
$f_{-3dB(lpf)}$	low-pass filter cut-off frequency	for a 1.7 MHz channel		-	1.59	-	MHz
		for a 6 MHz channel		-	6.58	-	MHz
		for a 7 MHz channel		-	7.35	-	MHz
		for a 8 MHz channel		-	8.35	-	MHz
		for a 10 MHz channel		-	9.35	-	MHz
α_{lpf}	low-pass filter attenuation	N − 1 sound carrier	[7]	14	-	-	dB
		N − 1	[8]	23	-	-	dB
		N ± 2		60	-	-	dB
		> 18 MHz		60	-	-	dB

Table 36. General characteristics for TV reception (RF input to IF output) *...continued*

T_{amb} = 25 °C; V_{CC} = 3.3 V; IF output level option 1 V (p-p); IF output load of 1 kΩ/1 pF; AGC1 TOP: 95 dBμV/89 dBμV; AGC3 TOP: 96 dBμV; AGC4 TOP: 105 dBμV/100 dBμV; AGC5 TOP: 105 dBμV/100 dBμV; IF_Level[2:0]: −6 dB/+24 dB; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$f_{c(notch)}$	notch center frequency	for 6 MHz LPF		-	6.5	-	MHz
		for 7 MHz LPF		-	7.25	-	MHz
		for 8 Mhz LPF		-	8.25		MHz
$\Delta t_{d(grp)}$	group delay time variation	f_c = 1.7 MHz, from 1 MHz to 1.7 MHz		-	628	-	ns
		f_c = 6 MHz, from 1 MHz to 6 MHz		-	220	-	ns
		f_c = 7 MHz, from 1 MHz to 7 MHz		-	225	-	ns
		f_c = 8 MHz, from 1 MHz to 8 MHz		-	240	-	ns
		f_c = 10 MHz, from 1 MHz to 10 MHz		-	280	-	ns
α_H	harmonic rejection	H2 (50 MHz to 435 MHz)		66	92	-	dB
		H3 (50 MHz to 290 MHz)		85	96	-	dB
		H5 (50 MHz to 174 MHz)		85	92	-	dB
$\alpha_{beat(PCS)}$	picture color sound beat	Picture = Color = Sound = 60 dBμV	[1]	50	63	-	dB
G_{tlt}	tilt gain	in band, 6 MHz, 7 MHz and 8 MHz channels		-	1	3	dB
Xmod	cross modulation	1 %; N + 2 channel; wanted = 60 dBμV	[1]	81	-	-	dBμV
α_{image}	image rejection	worst case for image rejection and 4 MHz IF frequency for levels above 60 dBμV		57.5	63	-	dB
CSO	composite second-order distortion	worst interferer over RF frequency with respect to wanted carrier	[9]	-	−60	-	dBc
CTB	composite triple beat	worst interferer over RF frequency with respect to wanted carrier	[9]	-	−65	-	dBc

[1] Single wanted analog channel, 60 dBμV level, at tuner input.

[2] If this residual gain variation is too high for the demodulator being used, refer to the associated Application Note for details of how to overcome this.

[3] See Figure 15.

[4] Corresponding to the time needed to launch and complete “tmbslTDA18273HNInit” and “tmbslTDA18273HNReset” functions in driver reference code.

[5] Single wanted analog channel, 100 dBμV level, at tuner input.

[6] See Table 37.

[7] Wanted channel being N, rejection of the N + n channel sound carrier for analog reception.

[8] Adjacent channel power rejection.

[9] Channel loading assumptions: 129 channels at 75 dBμV each.

Table 37. High Pass Filter cut-off frequencies descriptions

DC_Notch_IF_PPF	IF_HP_Fc[1:0]	HI_Pass	Min	Typ	Max	Unit
0	XX	0	-	130	-	kHz
1	XX	0	-	250	-	kHz
1	00	1	-	290	-	kHz

Table 37. High Pass Filter cut-off frequencies descriptions

DC_Notch_IF_PPF	IF_HP_Fc[1:0]	HI_Pass	Min	Typ	Max	Unit
1	01	1	-	610	-	kHz
1	10	1	-	720	-	kHz
1	11	1	-	1080	-	kHz

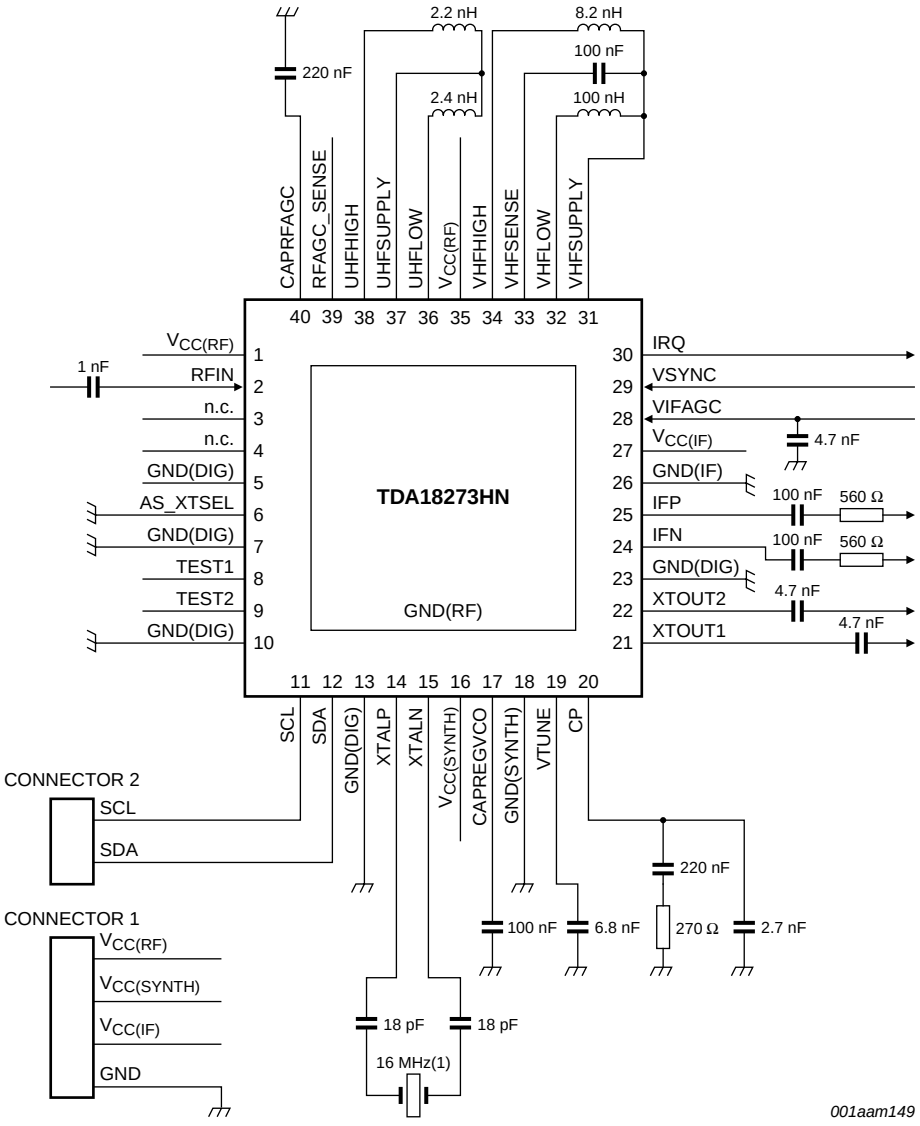
Table 38. Pins Characteristics

T_{amb} = 25 °C; V_{CC} = 3.3 V; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
IF AGC input						
V_{AGC}	AGC voltage		0	-	V_{CC}	V
dG_{AGC}/dV	rate of change of AGC gain with voltage		-	50	65	dB/V
Crystal oscillator						
f_{xtal}	crystal frequency		-	16	-	MHz
Crystal oscillator output buffer						
R_o	output resistance	16 MHz output frequency	-	460	-	Ω
Digital levels (I^2C-bus)[1]						
Pin SCL						
V_{IL}	LOW-level input voltage	V_{CC} related input levels	-	-	$0.3V_{CC}$	V
V_{IH}	HIGH-level input voltage	V_{CC} related input levels	$0.7V_{CC}$	-	-	V
f_{SCL}	SCL clock frequency		-	-	400	kHz
Pin SDA						
V_{IL}	LOW-level input voltage	V_{CC} related input levels	-	-	$0.3V_{CC}$	V
V_{IH}	HIGH-level input voltage	V_{CC} related input levels	$0.7V_{CC}$	-	-	V
V_{OL}	LOW-level output voltage	I_O = 3 mA (sink current)	-	-	0.4	V

[1] Devices that use non-standard supply voltages, which do not conform the intended I^2C-bus system levels, must relate their input levels to the supply voltage (V_{CC}) to which the pull-up resistors are connected.

Measurement method is available on request. These performances are measured in putting the tuner in the following configuration:



Remark: Decoupling capacitors are not depicted.

(1) Quartz references are: NX5032GA and NX3225GA

Fig 6. Measurement schematic

Table 39. Used coils

Band	Coil reference
UHF HIGH COIL	LQW5AN2N2C10
UHF LOW COIL	LQP15MN2N4W02
VHF HIGH COIL	LQP15MN8N2B02
VHF LOW COIL	LQG15HNR10J02

Remark: All following curves represent typical results observed on samples.

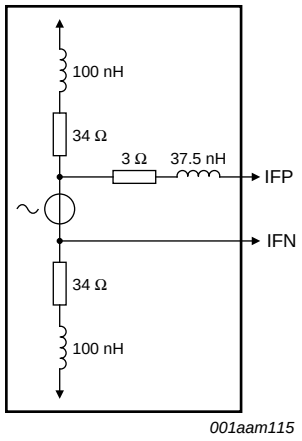


Fig 7. Typical IF output impedance at 10 MHz

14.1 IF filtering curves

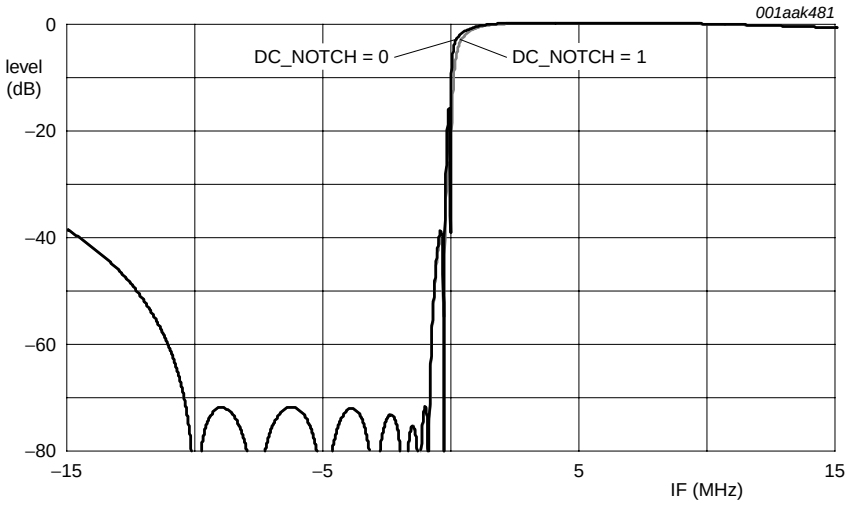


Fig 8. DC notch

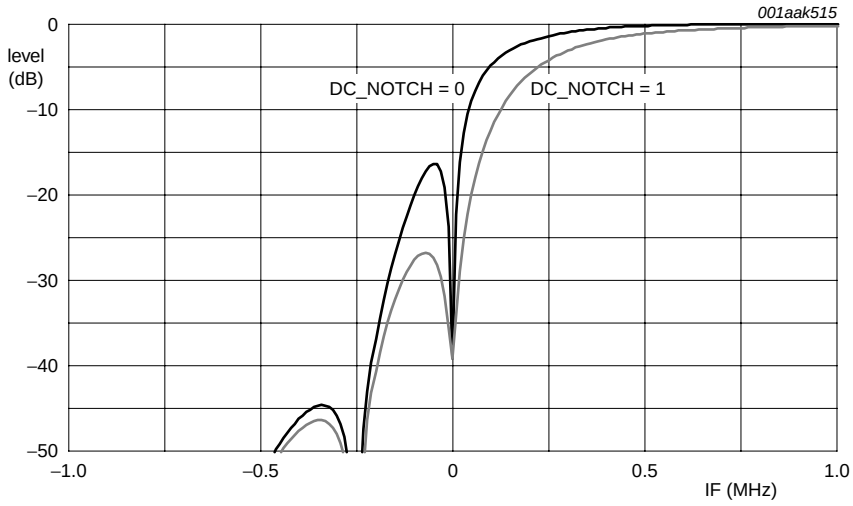


Fig 9. DC notch zoom

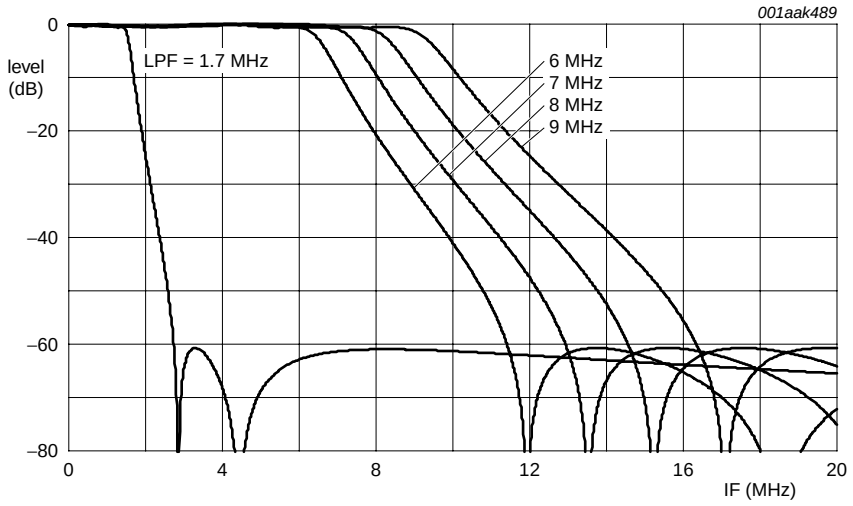


Fig 10. Low-pass filter

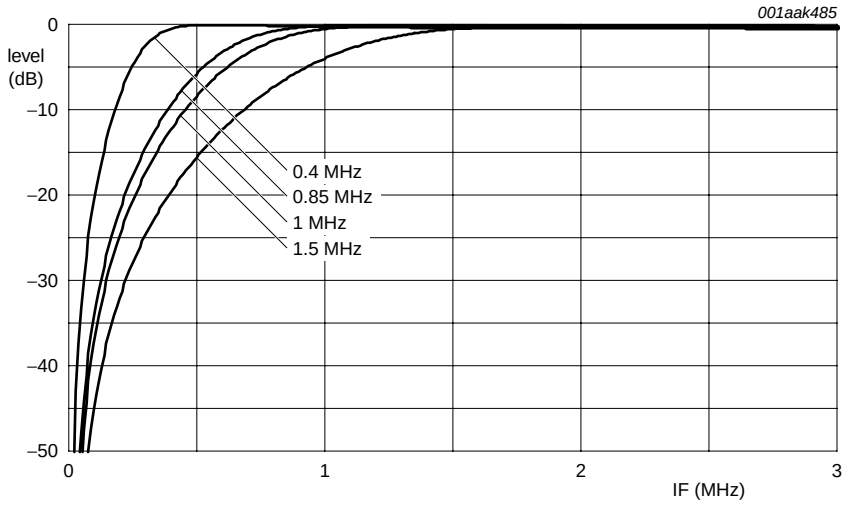


Fig 11. High-pass filter

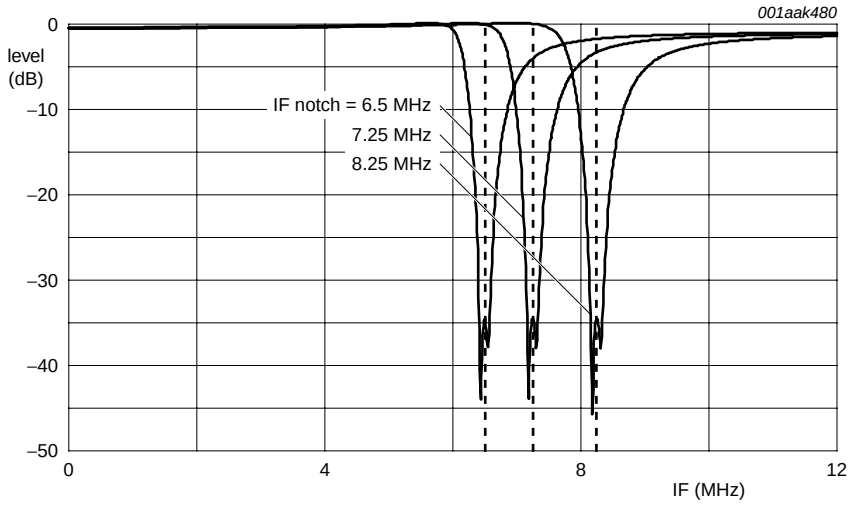


Fig 12. IF notches

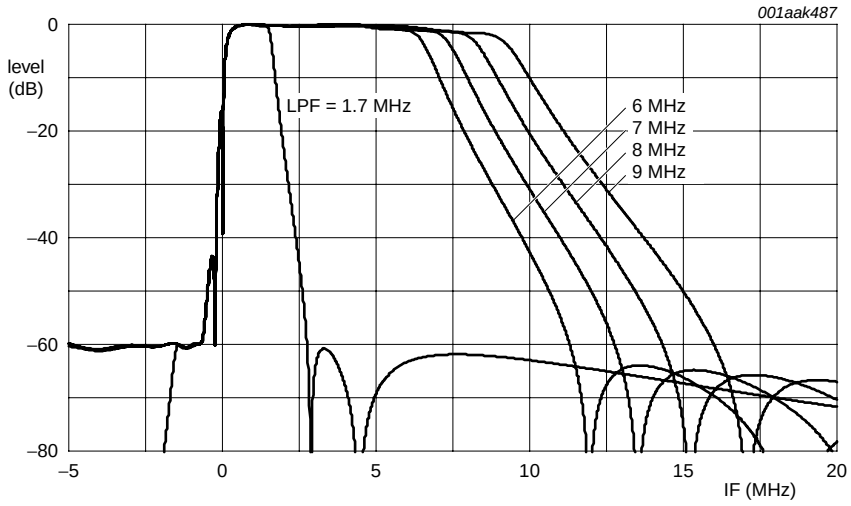


Fig 13. IF selectivity without notch

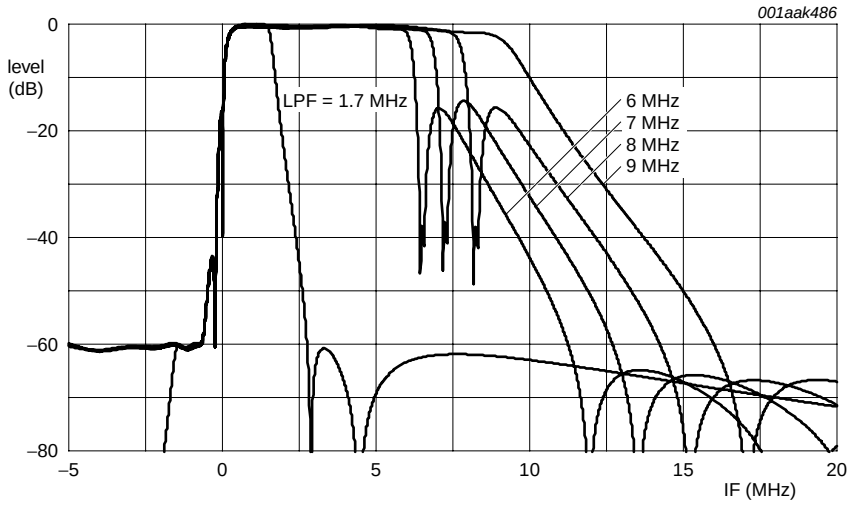


Fig 14. IF selectivity with notch

14.2 IF AGC gain versus IF AGC voltage

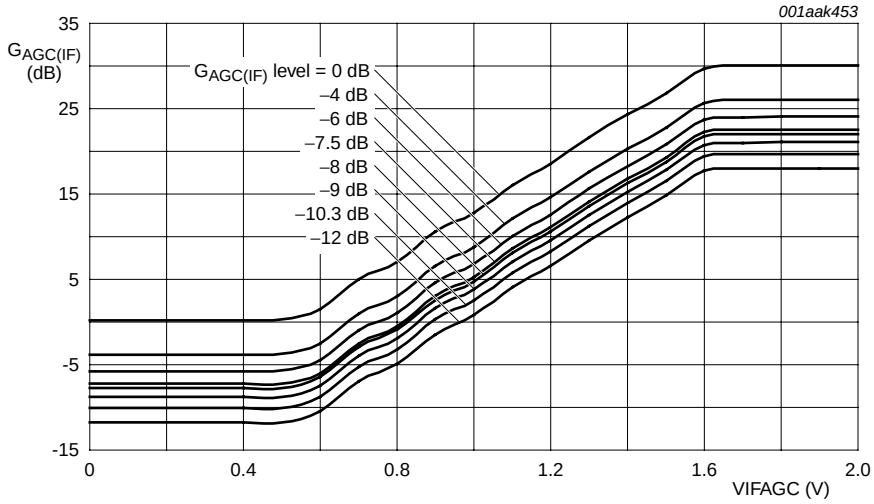


Fig 15. IF AGC gain versus IF AGC voltage

15. Application information

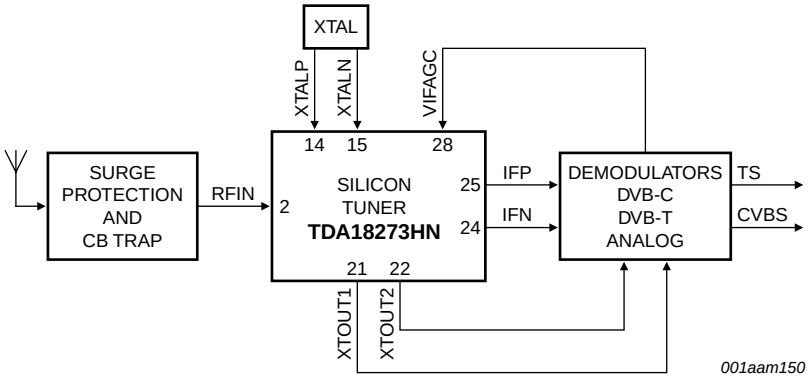
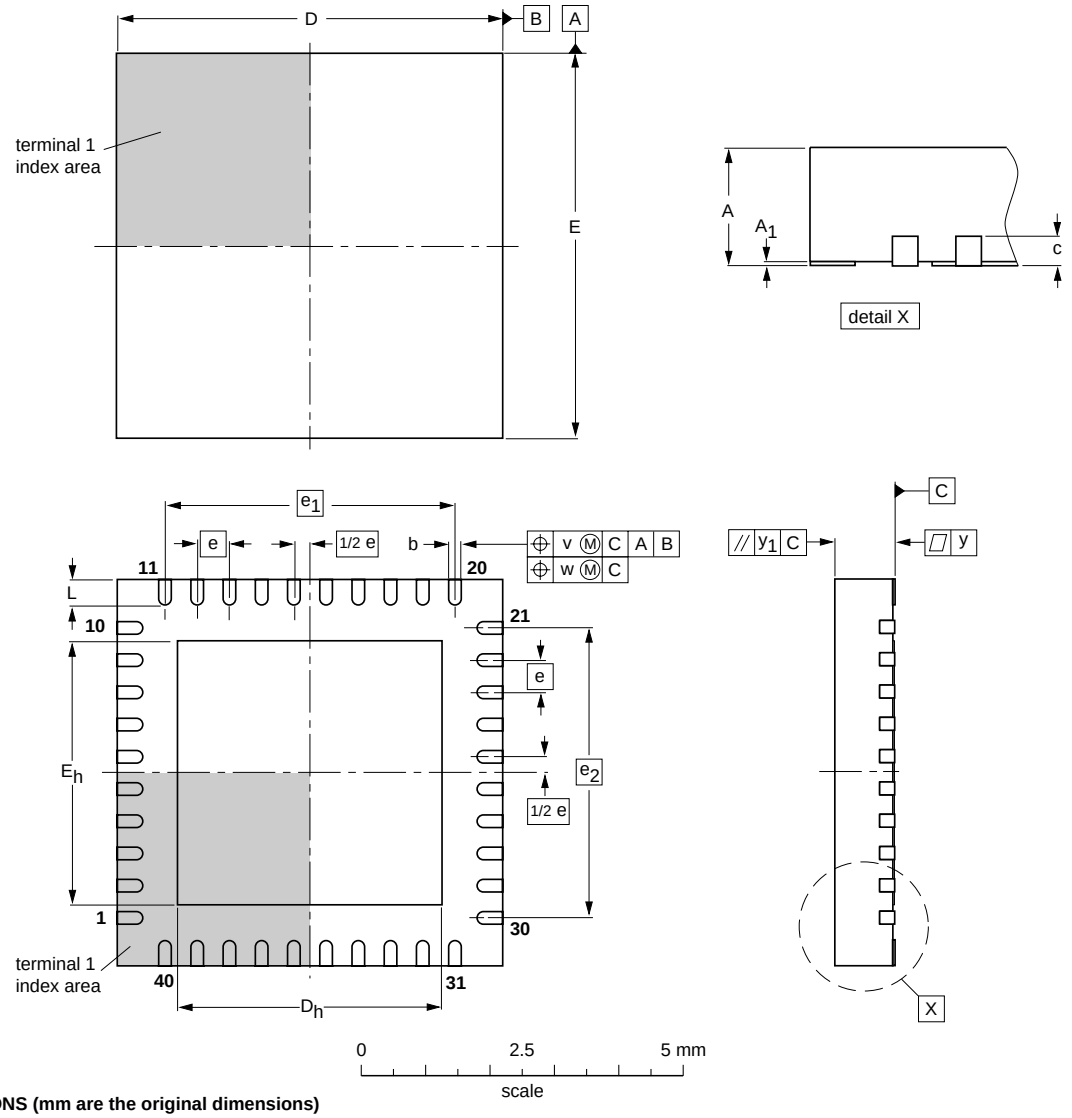


Fig 16. Tuner application diagram

16. Package outline

HVQFN40: plastic thermal enhanced very thin quad flat package; no leads; 40 terminals; body 6 x 6 x 0.85 mm **SOT618-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A(1) max.	A1	b	c	D(1)	Dh	E(1)	Eh	e	e1	e2	L	v	w	y	y1
mm	1	0.05 0.00	0.30 0.18	0.2	6.1 5.9	4.25 3.95	6.1 5.9	4.25 3.95	0.5	4.5	4.5	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT618-1	- - -	MO-220	- - -			~~01-08-08~~ 02-10-22

Fig 17. Package outline SOT618-1 (HVQFN40)

17. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

17.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

17.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

17.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

17.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 18) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 40 and 41

Table 40. SnPb eutectic process (from J-STD-020C)

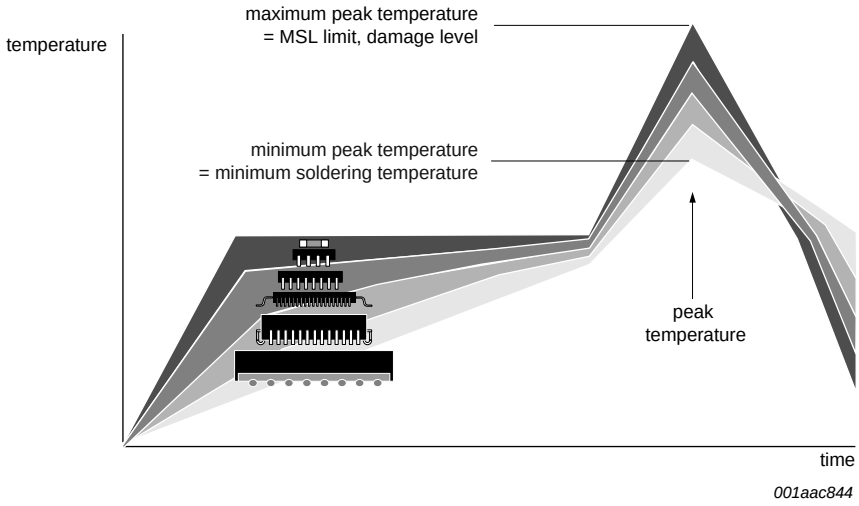
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 41. Lead-free process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 18.



MSL: Moisture Sensitivity Level

Fig 18. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

18. Abbreviations

Table 42. Abbreviations

Acronym	Description
ACI	Adjacent Channel Interferer
ADC	Analog-to-Digital Converter
AGC	Automatic Gain Control
AGCK	Automatic Gain Control step Killer
CB	Citizen Band
D-BOOK	Digital Terrestrial Television Requirements for Interoperability issued by the Digital Television Group in UK
DTMB	Digital Terrestrial Multimedia Broadcast
DVB	Digital Video Broadcasting
DVB-T/T2/C/C2/H	DVB-Terrestrial/Terrestrial second generation/Cable/Handheld
DVD-R	DVD-Recorder
EMC	ElectroMagnetic Compatibility
ESD	ElectroStatic Discharge
EU	European Union
FCDM	Field-induced Charged-Device Model
FM	Frequency Modulation
FRAC-N	Fractional-N
HBM	Human Body Model
HPF	High-Pass Filter
IC	Integrated Circuit

Table 42. Abbreviations *…continued*

Acronym	Description
IF	Intermediate Frequency
IR	Image Rejection
IRQ	Interrupt ReQuest
ISDB-T	Integrated Services Digital Broadcasting - Terrestrial
LC-VCO	Inductors and Capacitors - Voltage Controlled Oscillator
LNA	Low-Noise Amplifier
LO	Local Oscillator
LPF	Low-Pass Filter
MSM	Main State Machine
NTSC	National Television System Committee
OCUR	OpenCable Unidirectional Receiver
PAL	Phase Alternated Line
PCB	Printed Circuit Board
PCTV	Personal Computer Television
PLD	Power Level Detector
PLL	Phase-Locked Loop
POR	Power-On Reset
PPF	Poly Phase Filter
QAM	Quadrature Amplitude Modulation
RC CAL	Resistors and Capacitors calibrations
RF	Radio Frequency
RoHS	Restriction on Hazardous Substances
SAW	Surface Acoustic Wave
SECAM	Sequential Color A Memory
STB	Set-Top Box
TOP	Take Over Point
UHF	Ultra High Frequency
US	United States
VCO	Voltage Controlled Oscillator
VHF	Very High Frequency

19. Revision history

Table 43. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
TDA18273 v.2	<tbd>	Objective data sheet	-	TDA18273 v.1
Modifications:	• Section 2: updated. • Section 3: updated. • Figure 1: added the AGC2 block. • Table 3: added the note. • Table 4: updated the comment line AGC2 • Table 32: added the third column 'Tuner read address (hex)'. • Table 36: updated • Figure 7: added			
TDA18273HN v.1	20100728	Objective data sheet	-	-

20. Legal information

20.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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ICs with DVB-T or DVB-T2 functionality

Use of this product in any manner that complies with the DVB-T or the DVB-T2 standard may require licenses under applicable patents of the DVB-T respectively the DVB-T2 patent portfolio, which license is available from Sisvel S.p.A., Via Sestriere 100, 10060 None (TO), Italy, and under applicable patents of other parties.

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21. Contact information

For more information, please visit: **http://www.nxp.com**

For sales office addresses, please send an email to: **salesaddresses@nxp.com**

22. Tables

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