

Training Manual



42PJ350 Plasma Display



LG
Life's Good

**Advanced Single Scan Troubleshooting
42" Class HD 720p Plasma TV
(41.6" diagonally)**

Published August 12th, 2010

OUTLINE

Overview of Topics to be Discussed

Preliminary:

Contact Information, Preliminary Matters, Specifications,
Plasma Overview, General Troubleshooting Steps,
Disassembly Instructions, Voltage and Signal Distribution

No Main Power Switch (Vacation Switch).

Troubleshooting:

Circuit Board Operation, Troubleshooting and Alignment of :

- Switch Mode Power Supply *No VS On command input to SMPS*
- Y-SUS Board *Delivers Logic Signals and FG5V to Y-Drive board.*
- Y-Drive Board
- Z-SUS Output Board (Also uses one Z-SUB board for bottom panel connector)
- Control Board
- X Drive Boards (2)
- Main Board
- Interconnect Diagram: 11X17 Foldout Section used as a quick reference sheet.

Overview of Topics to be Discussed

42PJ350 Plasma Display

The first section will cover Contact Information and Important Safety Precautions for the Customers Safety as well as the Technician and the Equipment.

Basic Troubleshooting Techniques which can save time and money sometimes can be overlooked. These techniques will also be presented.

The next section will get the Technician familiar with the Disassembly, Identification and Layout of the Plasma Display Panel.

At the end of this Section the Technician should be able to Identify the Circuit Boards and have the ability and knowledge necessary to safely remove and replace any Circuit Board or Assembly.

LG Contact Information

Customer Service (and Part Sales) (800) 243-0000

Technical Support (and Part Sales) (800) 847-7597

USA Website (GSFS) <http://gsfs-america.lge.com>

Customer Service Website us.lgservice.com

Knowledgebase Website lgtechassist.com ← *New: Software Downloads
Technical Assistance*

LG Web Training lge.webex.com ← *Presentations with Audio/Video
and Screen Marks*

LG CS Academy lgcsacademy.com ← **<http://136.166.4.200>**

LCD-DV:	32LG40, 32LH30, 37LH55, 42LG60, 42LG70, 42LH20, 42LH40, 42LH50, 42LH90, 42SL80, 47LG90, 47LH85, 47LE8500
PLASMA:	42PG20, 42PQ20, 42PQ30, 50PG20, 42PJ350, 50PK750, 50PS80, 50PS60, 60PK750, 60PS11, 60PS60, 60PS80

Also available on the Plasma Page:
PDP Panel Alignment Handbook, Schematics with Bookmarks
Plasma Control Board ROM Update (Jig required)

***New Training Materials on
the Learning Academy site***

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LG Electronics Alabama, Inc.
201 James Record Road, Huntsville, AL, 35813.**



Preliminary Matters (The Fine Print)

IMPORTANT SAFETY NOTICE

The information in this training manual is intended for use by persons possessing an adequate background in electrical equipment, electronic devices, and mechanical systems. In any attempt to repair a major Product, personal injury and property damage can result. The manufacturer or seller maintains no liability for the interpretation of this information, nor can it assume any liability in conjunction with its use. When servicing this product, under no circumstances should the original design be modified or altered without permission from LG Electronics. Unauthorized modifications will not only void the warranty, but may lead to property damage or user injury. If wires, screws, clips, straps, nuts, or washers used to complete a ground path are removed for service, they must be returned to their original positions and properly fastened.

CAUTION

To avoid personal injury, disconnect the power before servicing this product. If electrical power is required for diagnosis or test purposes, disconnect the power immediately after performing the necessary checks. Also be aware that many household products present a weight hazard. At least two people should be involved in the installation or servicing of such devices. Failure to consider the weight of an product could result in physical injury.

ESD Notice (Electrostatic Static Discharge)

Today's sophisticated electronics are electrostatic discharge (ESD) sensitive. ESD can weaken or damage the electronics in a manner that renders them inoperative or reduces the time until their next failure. Connect an ESD wrist strap to a ground connection point or unpainted metal in the product. Alternatively, you can touch your finger repeatedly to a ground connection point or unpainted metal in the product. Before removing a replacement part from its package, touch the anti-static bag to a ground connection point or unpainted metal in the product. Handle the electronic control assembly by its edges only. When repackaging a failed electronic control assembly in an anti-static bag, observe these same precautions.

Regulatory Information

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a residential installation. This equipment generates, uses, and can radiate radio frequency energy, and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures: Reorient or relocate the receiving antenna; Increase the separation between the equipment and the receiver; Connect the equipment to an outlet on a different circuit than that to which the receiver is connected; or consult the dealer or an experienced radio/TV technician for help.

Safety and Handling, Checking Points

Safety & Handling Regulations

1. Approximately 10 minute pre-run time is required before any adjustments are performed.
2. Refer to the Voltage Sticker inside the Panel when making adjustments on the Power Supply, Y-SUS and Z-SUS Boards.
3. Always adjust to the specified voltage level (+/- ½ volt) unless otherwise specified.
4. Be cautious of electric shock from the PDP module since the PDP module uses high voltage, check that the Power Supply and Drive Circuits are completely discharged because of residual current stored before Circuit Board removal.
4. C-MOS circuits are used extensively for processing the Drive Signals and should be protected from static electricity.
5. The PDP Module must be carried by two people. **Always carry vertical NOT horizontal.**
6. **The Plasma television should be transported vertically NOT horizontally.**
7. Exercise care when making voltage and waveform checks to prevent costly short circuits from damaging the unit.
8. Be cautious of lost screws and other metal objects to prevent a possible short in the circuitry.
9. **New Panels and Frames are much thinner than previous models. Be Careful with flexing these panels. Be careful with lifting Panels from a horizontal position. Damage to the Frame mounts or panel can occur.**
10. **New Plasma models have much thinner cabinet assemblies and mounts. Be extremely careful when moving the set around as damage can occur.**

Checking Points to be Considered

1. Check the appearance of the Replacement Panel and Circuit Boards for both physical damage and part number accuracy.
2. Check the model label. Verify model names and board model matches.
3. Check details of defective condition and history. Example: Y-SUS or Y-Drive Board Failure, Mal-discharge on screen, etc.



Basic Troubleshooting Steps

Define, Localize, Isolate and Correct

- **Define** Look at the symptom carefully and determine what circuits could be causing the failure. Use your senses Sight, Smell, Touch and Hearing. Look for burned parts and check for possible overheated components. Capacitors will sometimes leak dielectric material and give off a distinct odor. Frequency of power supplies will change with the load, or listen for relay closing etc. **Observation of the front Power LEDs may give some clues.**
- **Localize** After carefully checking the symptom and determining the circuits to be checked and after giving a thorough examination using your senses the first check should always be the DC Supply Voltages to those circuits under test. Always confirm the supplies are not only the proper level but be sure they are noise free. If the supplies are missing check the resistance for possible short circuits.
- **Isolate** To further isolate the failure, check for the proper waveforms with the Oscilloscope to make a final determination of the failure. Look for correct Amplitude Phasing and Timing of the signals also check for the proper Duty Cycle of the signals. Sometimes “glitches” or “road bumps” will be an indication of an imminent failure.
- **Correct** The final step is to correct the problem. Be careful of ESD and make sure to check the DC Supplies for proper levels. Make all necessary adjustments and lastly always perform a Safety AC Leakage Test before returning the product back to the Customer.

42PJ350 PRODUCT INFORMATION SECTION



This section of the manual will discuss the specifications of the 42PJ350 Advanced Single Scan Plasma Display Television.

42PJ350 Specifications

1080P PLASMA HDTV **42" Class (41.6" diagonal)**

- **600Hz Sub Field Driving**
- **High Definition Resolution**
- **3M:1 Dynamic Contrast Ratio**
- **TruSlim Frame**
- **Picture Wizard II (Easy Picture Calibration)**
- **Smart Energy Saving**
- **Intelligent Sensor**
- **Dual XD™ Engine**
- **AV Mode (Cinema, Sports, Game)**
- **Clear Voice II**
- **ISFccc® Ready**
- **24P Real Cinema**
- **USB 2.0 (JPEG, MP3)**
- **3 HDMI™ 1.3 Inputs**
- **SIMPLINK™ Connectivity**
- **Dolby® Digital 5.1 Decoder**
- **Infinite Sound**

***For Full Specifications
See the Specification Sheet***

42PJ350 Logo Familiarization Page 1 of 3



600Hz Sub Field Firing:

Capture every moment. Tired of streaky action or unclear plays during the game? See sports, fast action and video games like never before. The 600Hz refresh rate virtually eliminates motion blur.



3,000,000 : 1 Contrast Ratio

Stunning detail. No more worrying about dark scenes or dull colors. The Mega Contrast ratio of 3,000,000:1 delivers more stunning colors and deeper blacks than you can imagine.



TruSlim Design:

At less than 1" thick the new TruSlim Frame trims away distraction without compromising screen size.



USB 2.0:

View videos and photos and listen to music on your TV through USB 2.0.



42PJ350 Logo Familiarization Page 2 of 3



HD RESOLUTION 720P HD Resolution Pixels: 1365 (H) × 768 (V)
See and experience more. Pictures are sharper.
Colors are more vibrant. Entertainment is more real.
Everything looks better on an HDTV.



HDMI (1.3 Deep Color) Digital multi-connectivity
HDMI (1.3 Deep color) provides a wider bandwidth (340MHz, 10.2Gbps) than that of HDMI 1.2, delivering a broader range of colors, and also drastically improves the data-transmission speed.



Invisible Speaker

Personally tuned by Mr. Mark Levinson for LG

TAKE IT TO THE EDGE newly introduces 'Invisible Speaker' system, guaranteeing first class audio quality personally tuned by Mr. Mark Levinson, world renowned as an audio authority. It provides Full Sweet Spot and realistic sound equal to that of theaters with its Invisible Speaker.



Dual XD Engine

Realizing optimal quality for all images

One XD Engine optimizes the images from RF signals as another XD Engine optimizes them from External inputs. Dual XD Engine presents images with optimal quality two times higher than those of previous models.



42PJ350 Logo Familiarization Page 3 of 3



AV Mode "One click" Cinema, Sports, Game mode.

AV Mode is three preset picture and audio settings. It allows the viewer to quickly switch between common settings. It includes Cinema, Sports, and Game Modes.



Clear Voice Clearer dialogue sound

Automatically enhances and amplifies the sound of the human voice frequency range to provide high-quality dialogue when background noise swells.



Save Energy, Save Money

It reduces the plasma display's power consumption. The default factory setting complies with the Energy Star requirements and is adjusted to the comfortable level to be viewed at home. (Turns on Intelligent Sensor).



Save Energy, Save Money

Home electronic products use energy when they're off to power features like clock displays and remote controls. Those that have earned the ENERGY STAR use as much as 60% less energy to perform these functions, while providing the same performance at the same price as less-efficient models. Less energy means you pay less on your energy bill. Draws less than 1 Watt in stand by.

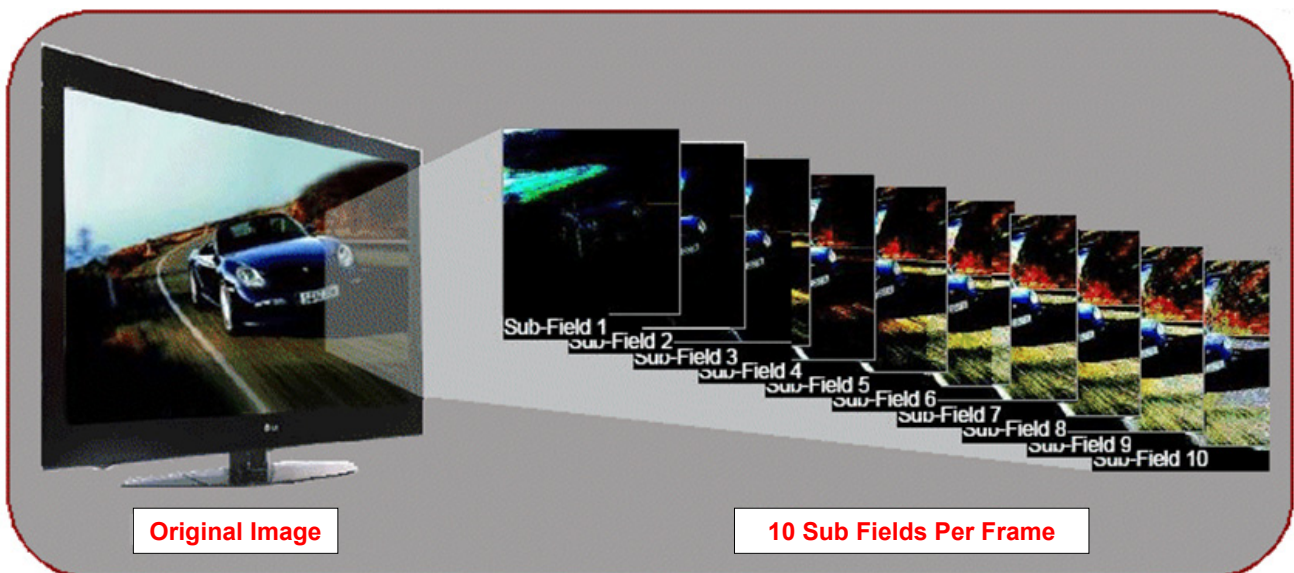


600Hz Sub Field Driving



(600 Hz Sub Field Driving)

- 600 Hz Sub Field Driving is achieved by using 10 sub-fields per frame process (vs. Comp. 8 sub-field/frame)
- No smeared images during fast motion scenes



Sub Field firing occurs using wall charge and polarity differences between Y-SUS and Z-SUS signals.

42PJ350 Remote Control

p/n AKB72914201

TOP PORTION



BOTTOM PORTION



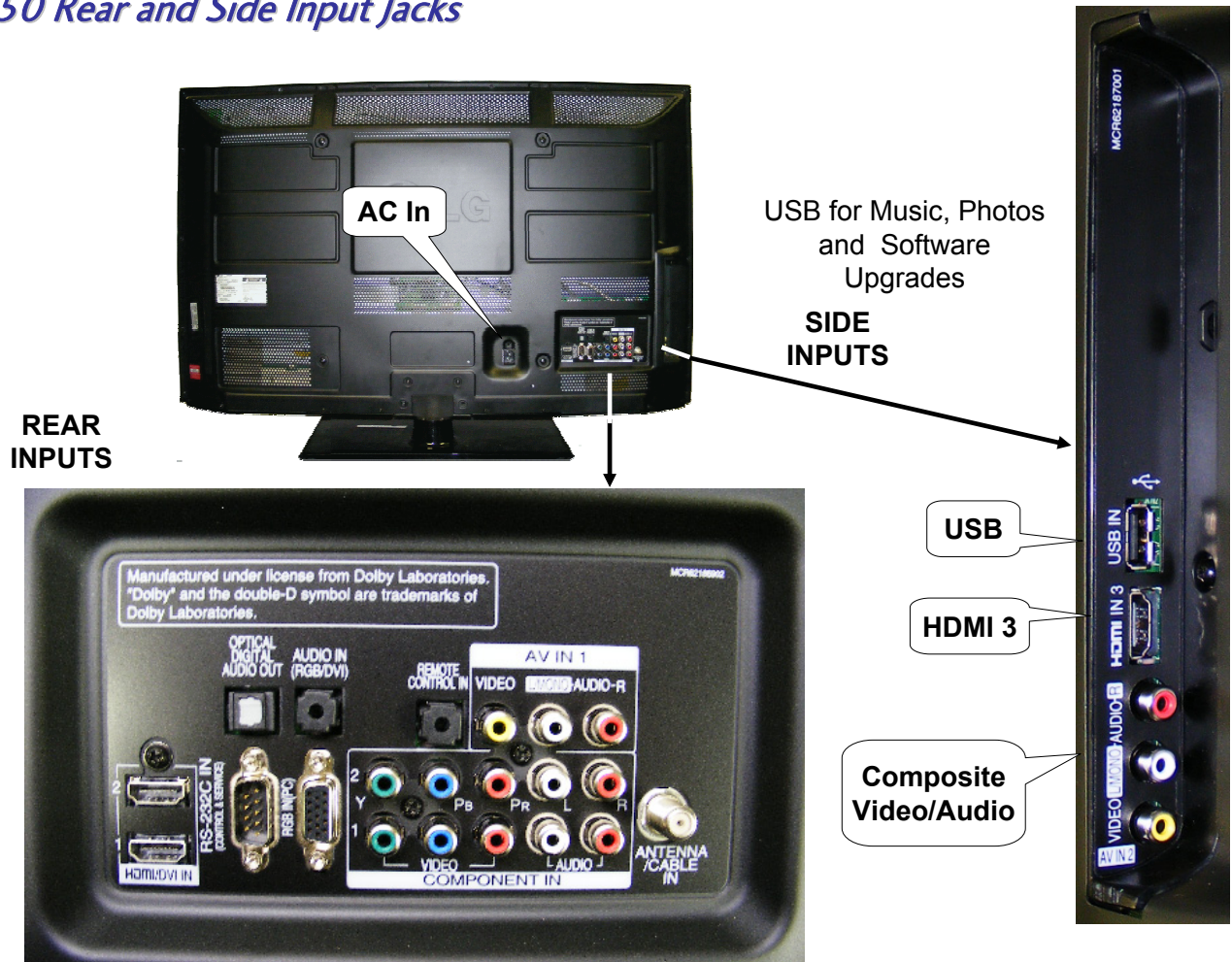
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August 2010

42PJ350

Plasma

42PJ350 Rear and Side Input Jacks

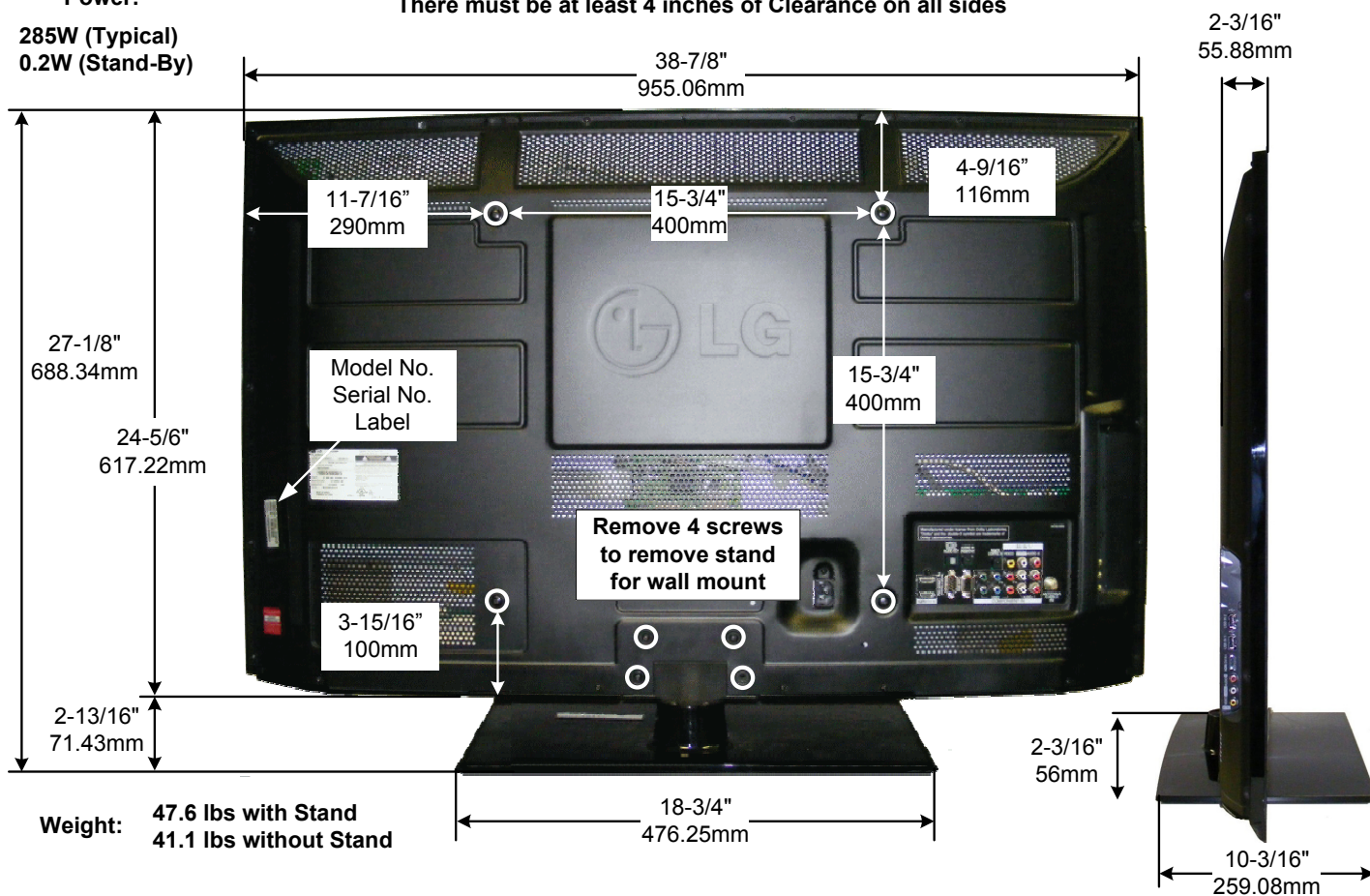


42PJ350 Dimensions

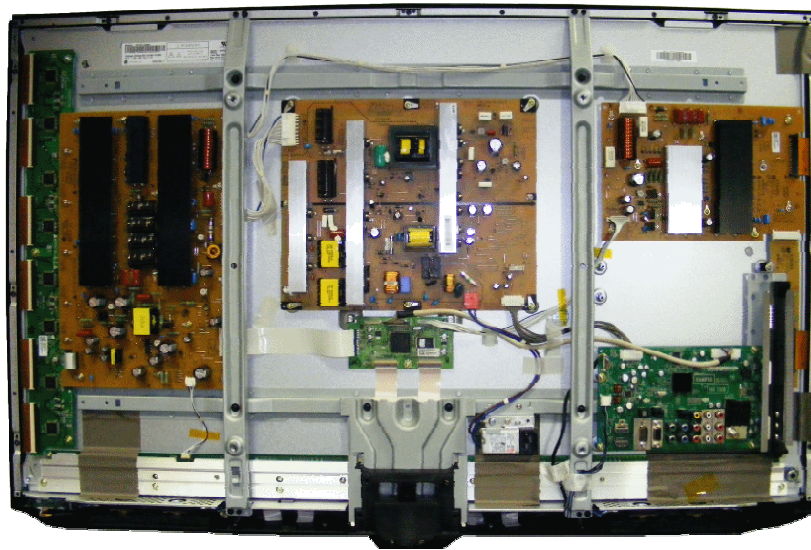
Power:

285W (Typical)
0.2W (Stand-By)

There must be at least 4 inches of Clearance on all sides



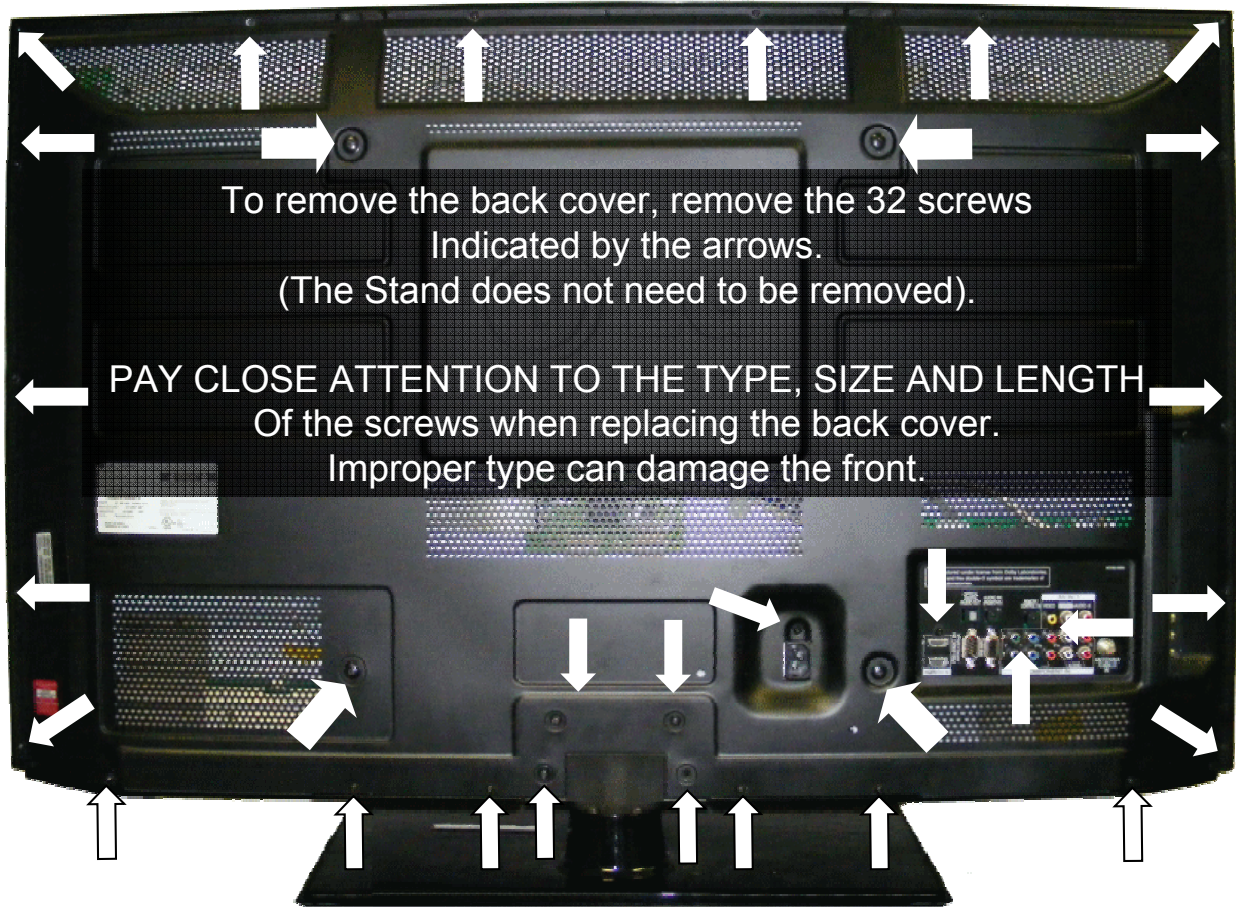
DISASSEMBLY SECTION



This section of the manual will discuss Disassembly, Layout and Circuit Board Identification, of the 42PJ350 Advanced Single Scan Plasma Display Panel.

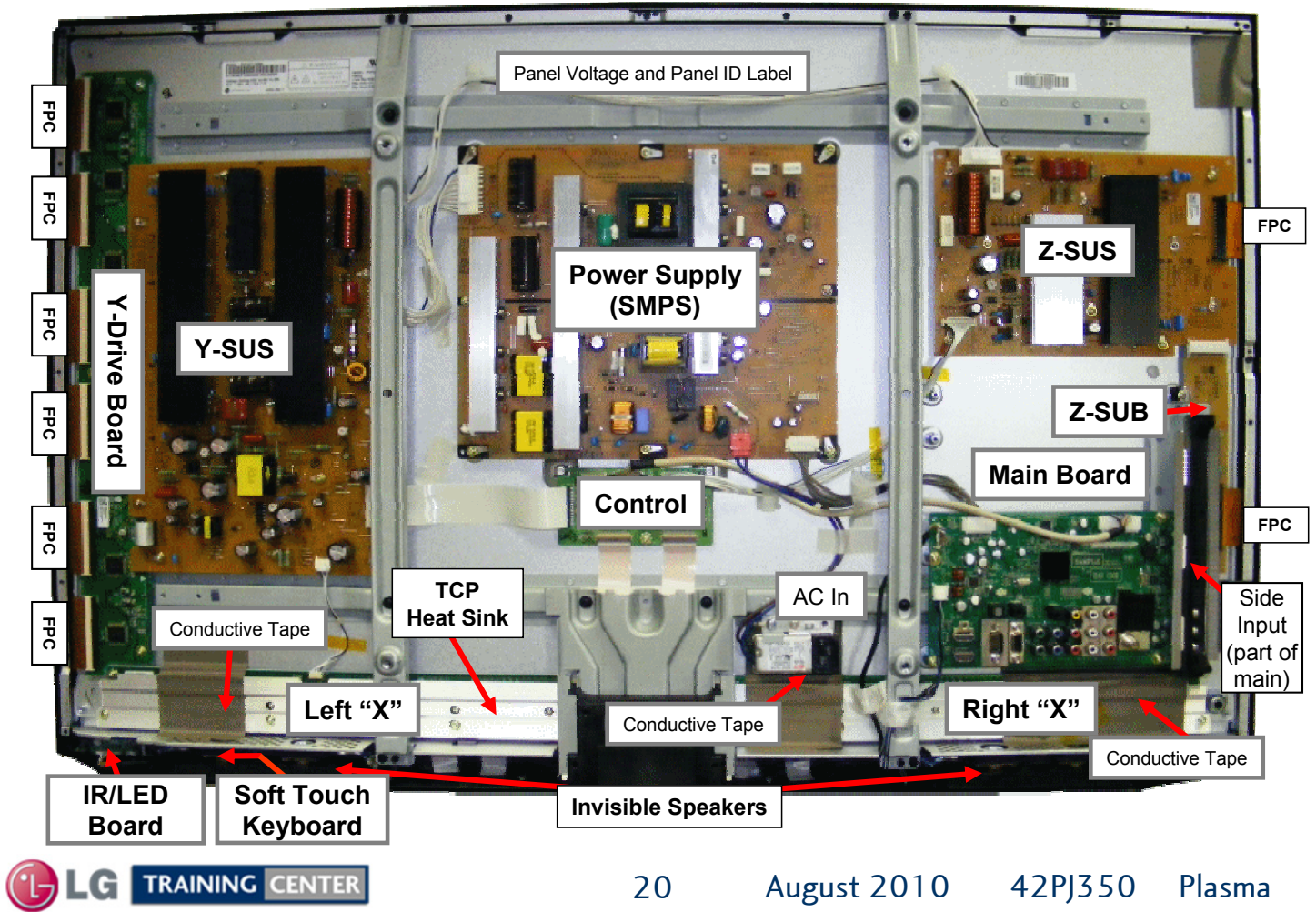
Upon completion of this section the Technician will have a better understanding of the disassembly procedures, the layout of the printed circuit boards and be able to identify each board.

Removing the Back Cover

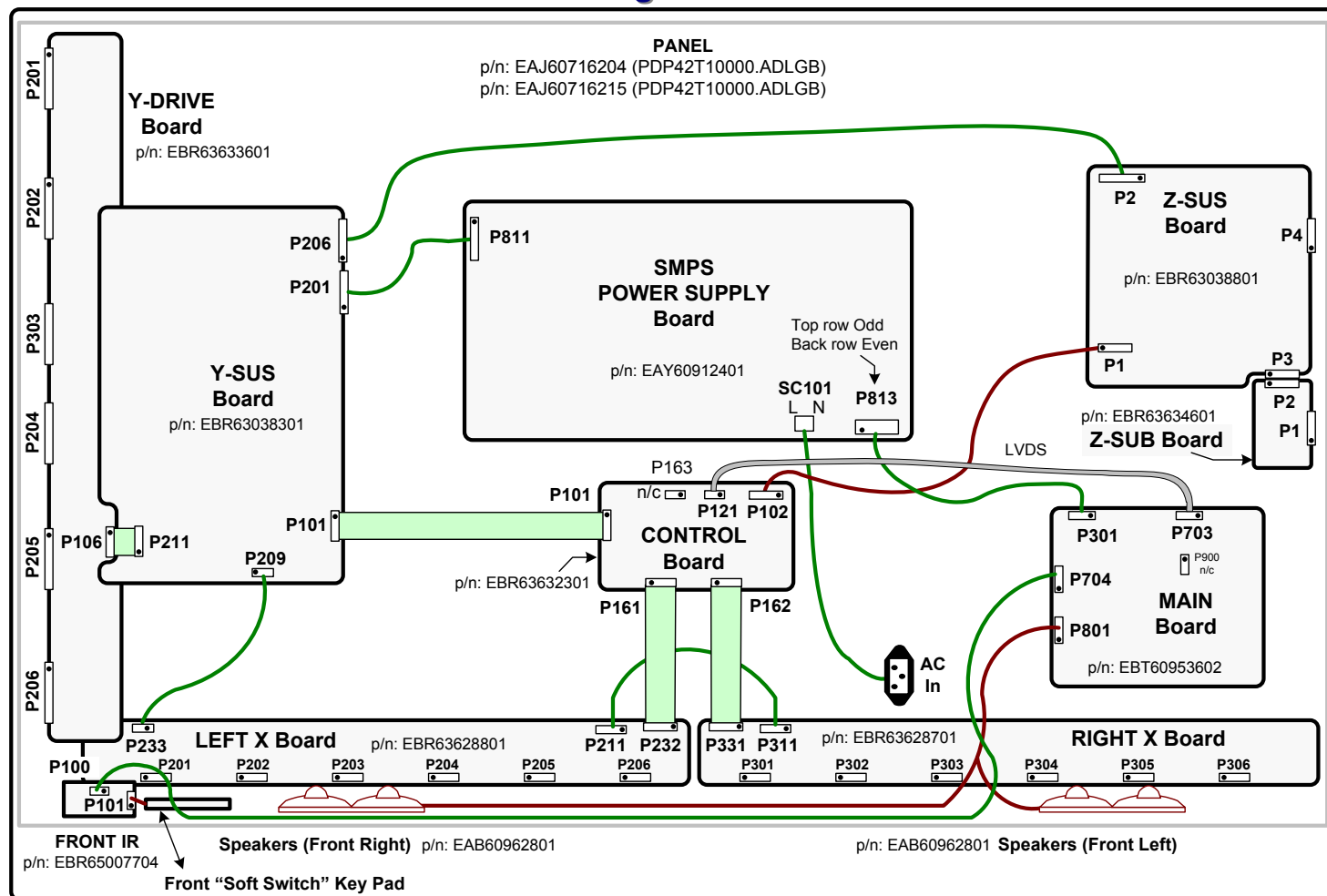


Circuit Board Layout

Identifying the Circuit Boards



42PJ350 Connector Identification Diagram



Disassembly Procedure for Circuit Board Removal

Note: 1) Remember to be cautious of ESD as some semiconductors are CMOS and prone to static failure.

Switch Mode Power Supply Board Removal

Disconnect the following connectors: P811, P813 and SC101.

Remove the 8 screws holding the SMPS in place.

Remove the board. When replacing, be sure to readjust the Va/Vs voltages in accordance with the Panel Label. Also, re-confirm VSC, -Vy and Z-Bias as well.

Y-SUS Board Removal

Note: The Y-SUS does not come with the connector to the Lower Y-Drive

Remove the Left Vertical Brace. 4 screws, 2 metal tap and 2 plastic tap.

Disconnect the following connectors: P201, P203, P206, P211 and Ribbon Cable P101.

To remove P101, lift up on the locking mechanism and pull the ribbon cable out.

Remove the 16 screws holding the Y-SUS in place. **Do not run the set with P211 removed.**

Remove the Y-SUS board. When replacing, be sure to readjust the Va/Vs voltages in accordance with the Panel Label.

Confirm VSC, -Vy and Z-bias as well.

Y-Drive Board Removal

Note: The Y-SUS does not come with the connectors between the Y-SUS and Y-Drive

Disconnect P101~P106 Connectors to the Panel

Remove P106 by lifting up on the locking mechanism and pull the ribbon cable out.

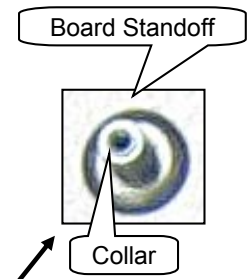
Do not run the set with P106 connector removed.

Remove the 7 screws holding the Y-Drive board in place.

Lift up slightly, the slide to the left. Remove the Y-Drive Board.

Note: Y-SUS, Z-SUS and Y-Drive boards are mounted on board stand-offs that have a small collar.

The board must be lifted slightly to clear these collars. Behind each board are "Chocolate" (dense rubber like material) that act as shock absorbers. They may make the board stick when removing.



Disassembly Procedure for Circuit Board Removal (2)

Z-SUS Board Removal

Disconnect the following connectors: P1 and P2, then P4 by pulling out the locking mechanism and pulling out the FPC to the panel. Note, slide a thin object (top side) between ribbon and connector to remove.

Remove the 9 screws holding the board in place.

Lift up slightly to clear the screw stand-offs and pull the Z-SUS upward to unseat P3/P2 from the Z-SUB board and remove the Z-SUS board.

When replacing, be sure to readjust the Va/Vs voltages in accordance with the Panel Label.

Confirm VS, -Vy and Z-bias (VZB) as well.

Z-SUB Board Removal

Remove the two screws in the Z-SUB board. Remove P1 by pulling out the locking mechanism and pulling out the FPC to the panel, See note above concerning P4 removal. Pull down and remove Z-SUB.

Main Board Removal

Disconnect the following connectors: P703 LVDS and P301 (press gently inward on the locking tabs) and pull out, P704 and P801. Remove 1 screw in the decorative plastic piece and remove.

Remove the 4 screws holding the Main board in place and Remove the board.

Control Board Removal

Disconnect the following connectors: P121 LVDS, P101 Ribbon and P102. Then P161, P162 Ribbons by lifting up the locking tab. Remove the 1 screws holding the Control board in place. Lift up the bottom and pull down to unseat it from the two metal supports at the top and Remove the board. Pay attention to the top right back side of the board. There is a piece of rubber (Chocolate) that may fall off. Be sure to replace the rubber piece.

Front IR and Key Pad Removal

FRONT IR/INTELLIGENT SENSOR and POWER BUTTON:

Disconnect P100 and P101. Note: P101 is a ribbon connector. Lift up the locking mechanism and slide the ribbon cable out. Remove the Board by lifting up on the top tabs, lift the board and remove.

KEY PAD:

The Key Pad is a thin strip of static sensitive material attached to the front glass. It is not removable.

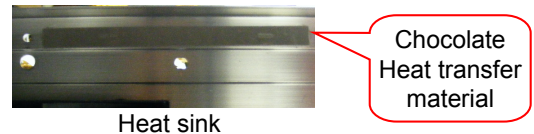
X Drive Circuit Board Removal Continued

Make sure AC is removed.

Lay the Television down carefully on a padded surface.

Make sure to use at least two people for this process so as not to flex the panel glass.

- a) Remove the Back Cover.
- b) Remove the Stand (4 Stand Screws were removed during back removal).
- c) Disconnect the two connector on the left side of the Main board, P704 and P801.
- d) Remove the Stand Metal Support Bracket (5 Screws) 2 Plastic tap thread and 3 Metal thread.
- e) Remove the two Vertical support Braces marked "E".
Note: There are 4 Screws per/brace, 2 Plastic tap thread and 2 Metal thread.
(Note, the right brace has a Grounding wire from the AC input which must also be removed).
- f) Remove the 7 screws holding the Heat Sink. (Warning: Never run the set with this heat sink removed).
To remove the heat sink, lift up to release the tacky Chocolate (heat transfer material) and slide the heat sink to the left to clear the connector wires on the right side.
Note: There are three large pieces of conductive tape on the heat sink that must be removed.
Also, note that there several pieces of Chocolate heat transfer material attached all the way across the underside of the heat sink. There is a mark on either side of the tape on the heat sink which shows its locations.



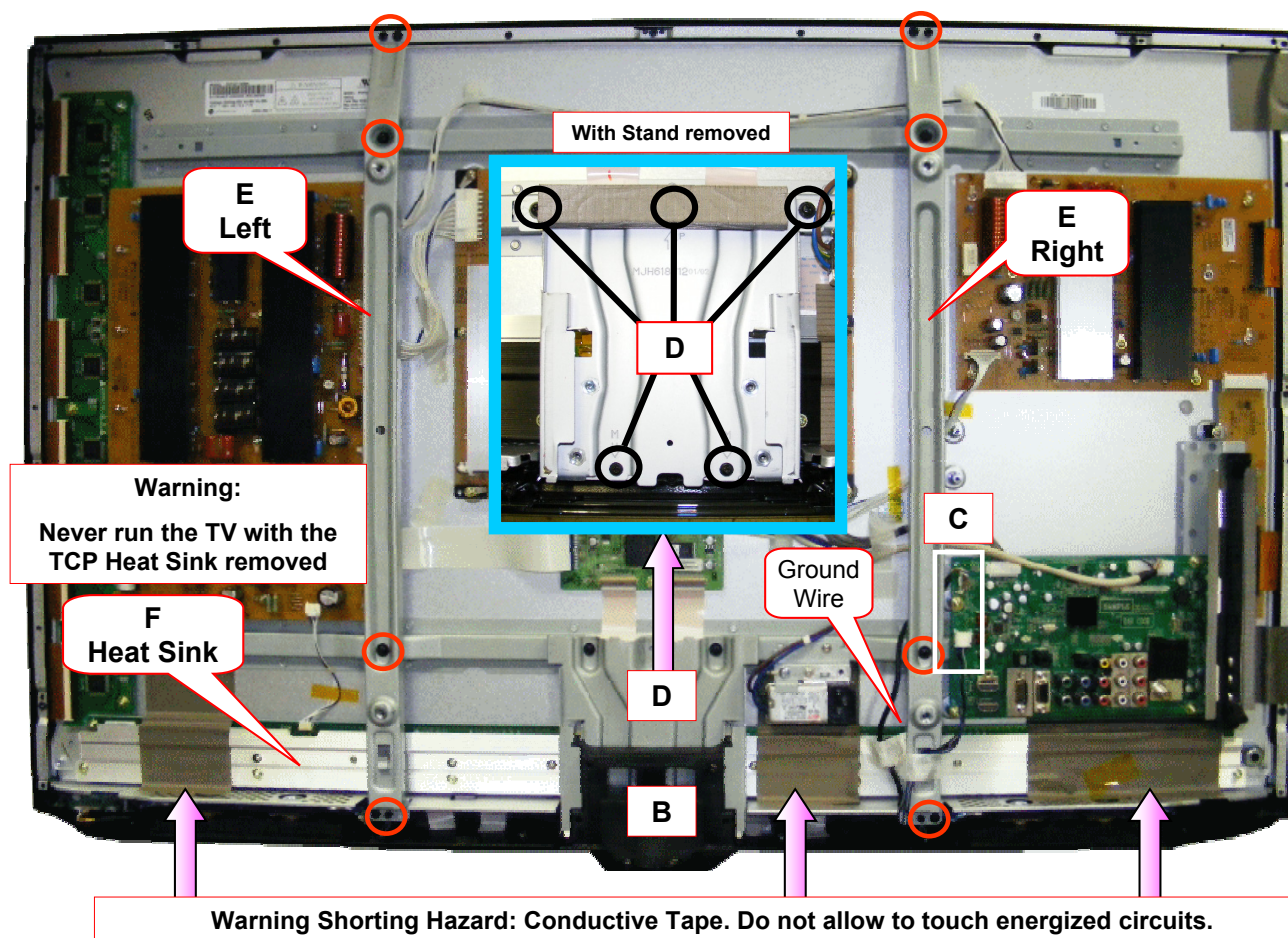
X-DRIVE LEFT, AND X-DRIVE RIGHT REMOVAL:

Disconnect all TCP ribbon cables from the defective X-Drive board and all other Ribbon cables going to the board.

Remove the (3 Left or Right X) or (5 Center X) screws holding the defective X-Drive board in place.

Remove the board. Reassemble in reverse order. Recheck Va / Vs / VScan / -VY / Z-Drive.

Getting to the X Circuit Boards

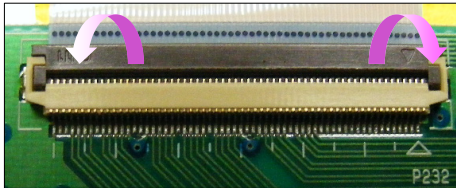


Left and Right X Drive Connector Removal

See below to Remove the Connections on the X-Boards.

From the X-Boards to the Control Board.
There may be tape on these connectors.

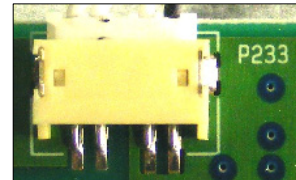
P232, P331
Are the same



Remove tape (if present) and Gently pry the locking mechanism upward and remove the ribbon cable from the connector.

Disconnect connector P233

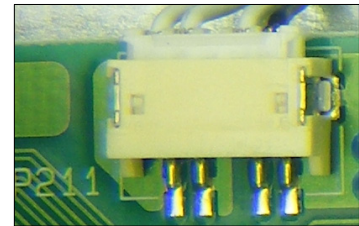
Va from the
Y-SUS to
Left X Only



Connectors from Left and Right X Boards

P211 to P311
Left X to Right X

P211, P311
Are the same



Removing Connectors to the TCPs.

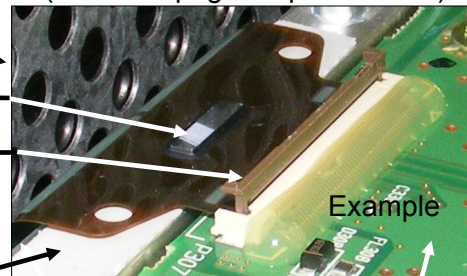
Gently lift the locking mechanism
upward on all TCP connectors
Left X: P201~206
Right X: P301~306

Carefully lift the TCP ribbon up and off.
It may stick, be careful not to crack TCP.
(See next page for precautions)

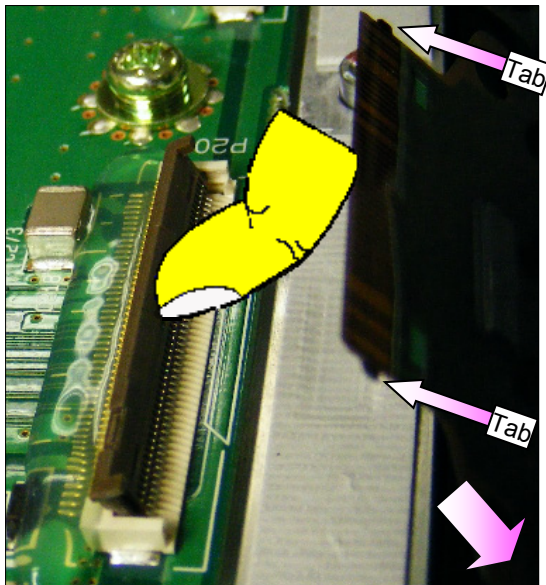
TCP

Cushion (Chocolate)

Flexible ribbon cable connector



TCP (Tape Carrier Package) Generic Removal Precautions

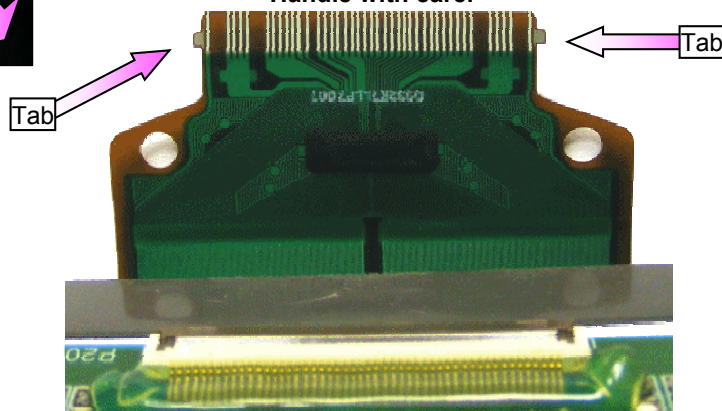


Lift up the lock as shown using your fingernail.
**(The Lock can be easily broken.
It needs to be handled carefully.)**

The TCP has two small tabs on each side which lock the ribbon cable fully into the connector. They have to be lifted up slightly to pull the connector out.

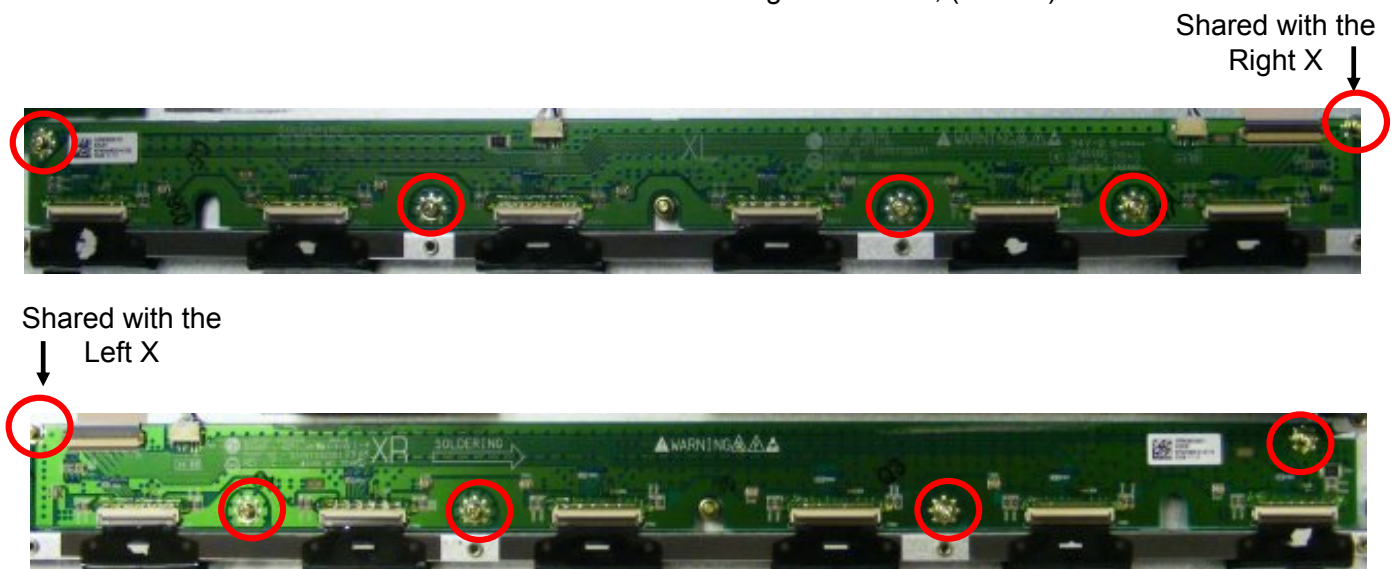
Note: TCP is usually stuck down to the Chocolate heat transfer material, be Very Careful when lifting up on the TCP ribbon cable.

Separate the TCP from the connector as shown.
**TCP Film can be easily damaged.
Handle with care.**



Left and Right X Drive Removal

Remove the 4 screws in Left or Right X-Boards, (9 Total)

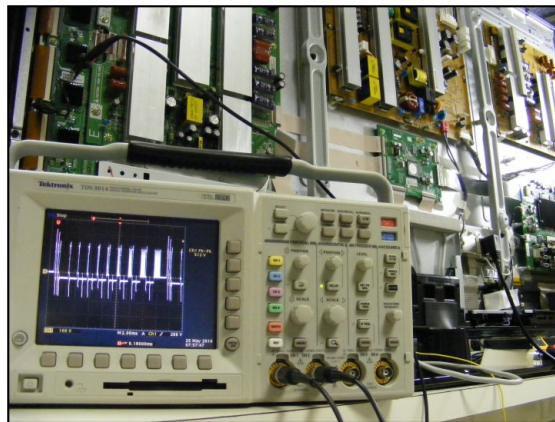


The Left X Board drives the Right 5/16 of the side of the screen vertical electrodes
The Center X Board drives the Center 3/8 of the of the screen vertical electrodes
The Right X Board drives the Left 5/16 of the side of the screen vertical electrodes

CIRCUIT OPERATION, TROUBLESHOOTING AND CIRCUIT ALIGNMENT SECTION

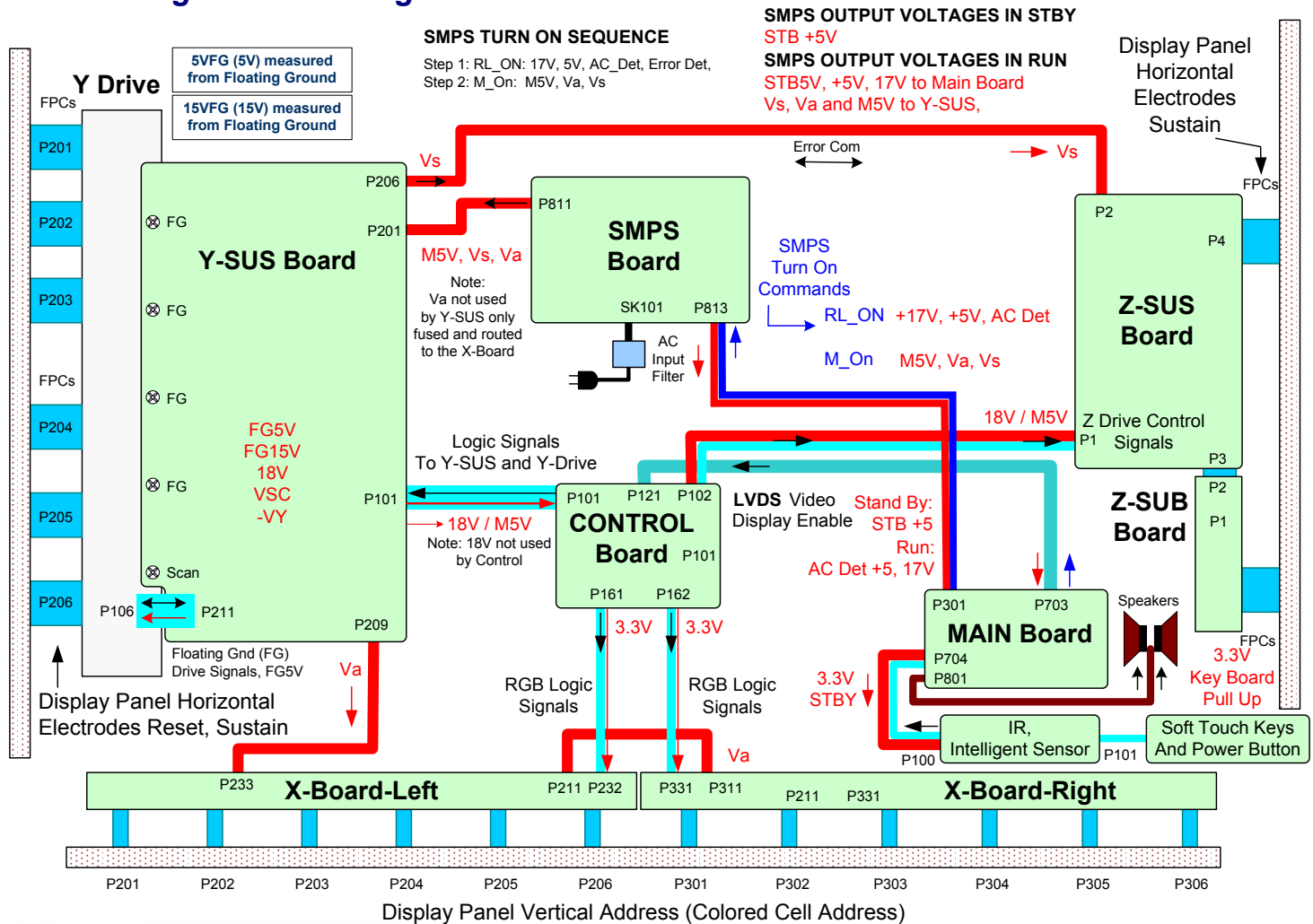
42PJ350 Plasma Display

This Section will cover Circuit Operation, Troubleshooting and Alignment of the Power Supply, Y-SUS Board, Y-Drive Boards, Z-SUS Board, Control Board, Main Board and the X Drive Boards.

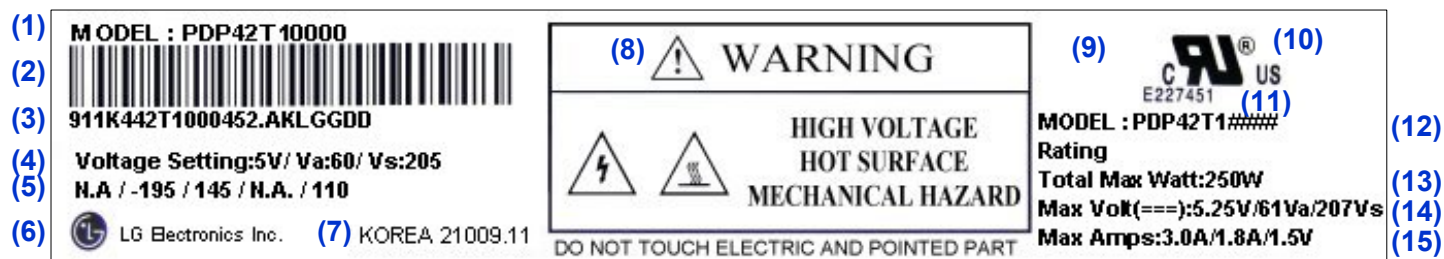


At the end of this Section the technician should understand the operation of each circuit board and how to adjust the controls. The technician should be able with confidence to troubleshoot a circuit board failure, replace the defective circuit and perform all necessary adjustments.

42PJ350 Signal and Voltage Distribution Block



Panel Label Explanation



- | | |
|--|----------------------------------|
| (1) Panel Model Name | (9) TUV Approval Mark (Not Used) |
| (2) Bar Code | (10) UL Approval Mark |
| (3) Manufacture No. | (11) UL Approval No. |
| (4) Adjusting Voltage DC, Va, Vs | (12) Panel Model Name |
| (5) Adjusting Voltage (Set Up / -Vy / Vsc / Ve / Vz) | (13) Max. Watt (Full White) |
| (6) Trade name of LG Electronics | (14) Max. Volts |
| (7) Manufactured date (Year & Month) | (15) Max. Amps |
| (8) Warning | |

Adjustment Notice

All adjustments (DC or Waveform) are adjusted in WHITE WASH.
Customer's Menu, Select "Options", select "ISM" select "WHITE WASH".

It is critical that the DC Voltage adjustments be checked when;

- 1) SMPS, Y-SUS or Z-SUS board is replaced.
- 2) Panel is replaced, Check Va/Vs since the SMPS does not come with new panel
- 3) A Picture issue is encountered
- 4) As a general rule of thumb when ever the back is removed

ADJUSTMENT ORDER "IMPORTANT"

DC VOLTAGE ADJUSTMENTS

- 1) POWER SUPPLY: VS, VA (Always do first)
- 2) Y-SUS: Adjust -Vy, VSC
- 3) Z-SUS: Adjust Z-Bias (VZB)

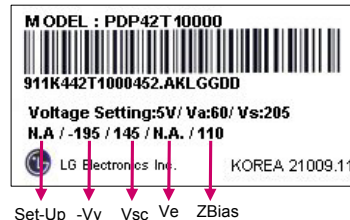
WAVEFORM ADJUSTMENTS

- 1) Y-SUS: Set-Up, Set-Down

The Waveform adjustment is only necessary

- 1) When the Y-SUS board is replaced
- 2) When a "Mal-Discharge" problem is encountered
- 3) When an abnormal picture issues is encountered

Remember, the Voltage Label MUST be followed,
it is specific to the panel's needs.



Power Supply

Panel
"Rear View"

All label references are from a specific panel.
They are not the same for every panel encountered.

SWITCH MODE POWER SUPPLY SECTION

This Section of the Presentation will cover troubleshooting the Switch Mode Power Supply for the Single Scan Plasma. Upon completion of the section the technician will have a better understanding of the operation of the Power Supply Circuit and will be able to locate voltage and test points needed for troubleshooting and alignments.

- DC Voltages developed on the SMPS
- Adjustments VA and VS.

Always refer to the Voltage Sticker located on the back of the panel, in the upper Left Hand side for the correct voltage levels for the VA, VS, -VY, VSC, and Z Bias as these voltages will vary from Panel to Panel even in the same size category.

Set-Up and Ve are just for Label location identification and are not adjusted in this panel.

SMPS p/n: EAY60912401

Check the silk screen label on the top center of the Power Supply board to identify the correct part number. (It may vary in your specific model number).

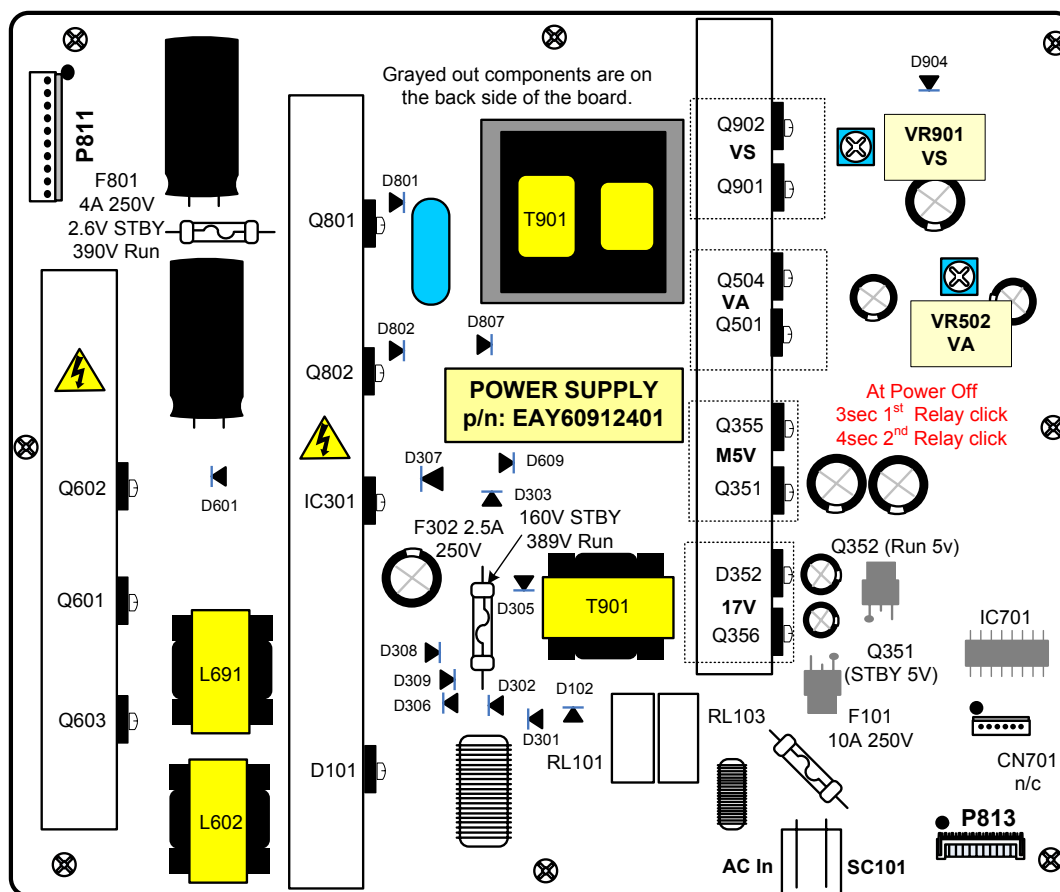
On the following pages, we will examine the Operation of this Power Supply.

Switch Mode Power Supply Overview

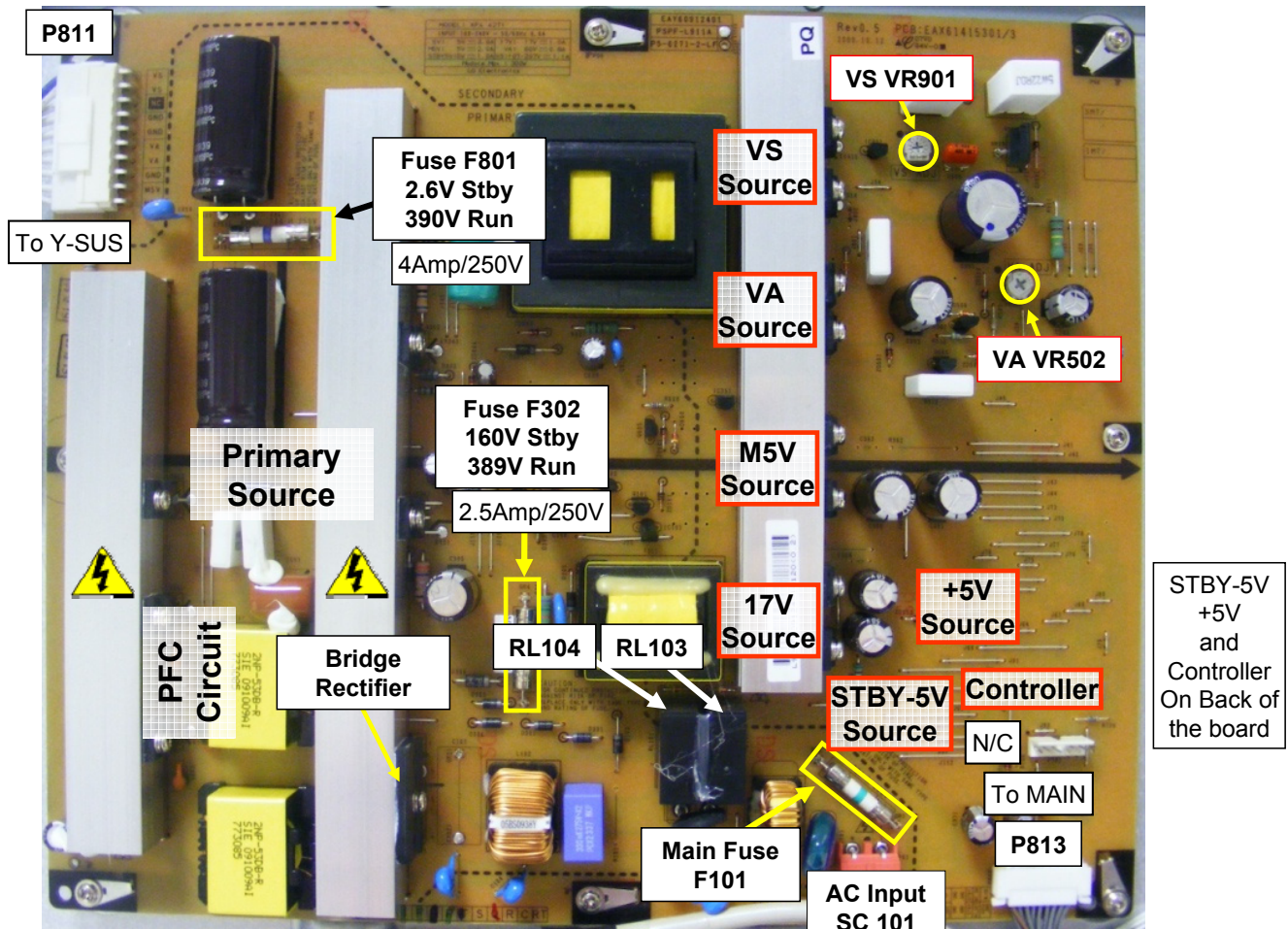
The Switch Mode Power Supply Board Outputs to the :

Y-SUS Board	VS	Drives the Display Panel's Horizontal Electrodes. (From Y-SUS to Z-SUS).
	VA	To Y-SUS, fused then to the X-Boards. (Not used by Z-SUS). Primarily responsible for Display Panel Vertical Electrodes.
	M5V	Used to develop Bias Voltages on the Y-SUS then routed to the Control board and then to the Z-SUS Board.
<hr/>		
Main Board	STBY 5V	Microprocessor Circuits
	17V	Audio B+ Supply, Tuner B+ Circuits
	5V	Signal Processing Circuits
	Also AC_Det (if missing, shuts of TV in 10 seconds) and Error_Det (not used)	
<hr/>		
Adjustments	There are 2 adjustments located on the Power Supply Board VA and VS. The M5V is pre-adjusted and fixed. All adjustments are made referenced to Chassis Ground. Use "Full White Raster" 100 IRE	
	VS	VR901
	VA	VR502

42PJ350 SMPS Layout Drawing



Power Supply Circuit Layout



Power Supply Basic Operation

AC Voltage is supplied to the SMPS Board at Connector SC101 from the AC Input assembly. Rectified by the Bridge rectifier D101 generates a primary B+. The Power factor circuit generates a Primary supply which can be read at Fuse F302 160V. This primary voltage is routed through T301 and routed to the Standby 5V supply. The STBY5V (standby) is B+ for the Controller chip on the back of the board (IC701) on the SMPS and output at P813 pins 13 and 14 then sent to the Main board for Microprocessor (IC1) operation (STBY 3.49V RUN 5.23V).

When the Microprocessor (IC1) on the Main Board receives a "POWER ON" Command from either the Power button or the Remote IR Signal, it outputs a high (2.43V) called **RL_ON** at Pin 15 of P813. This command causes the Relay Circuit to close both Relays RL101 and RL103 routing AC to the Bridge Rectifier D101 which then routes the primary voltage to the PFC circuit (Power Factor Controller) 390V which can be read measuring voltage at Fuses F302 (390V) and F801 (389V) from "Hot" Ground. AC Detection (AC Det) is generated on the SMPS, by rectifying a small sample of the A/C Line and routed to the Controller (IC701) where it outputs at P813 pin 16 (4.45V) and sent to P301 to the Main Board where it is sensed and monitored by the Main Microprocessor (IC1). If AC Det is missing the set will come on, but shut off in 10 seconds.

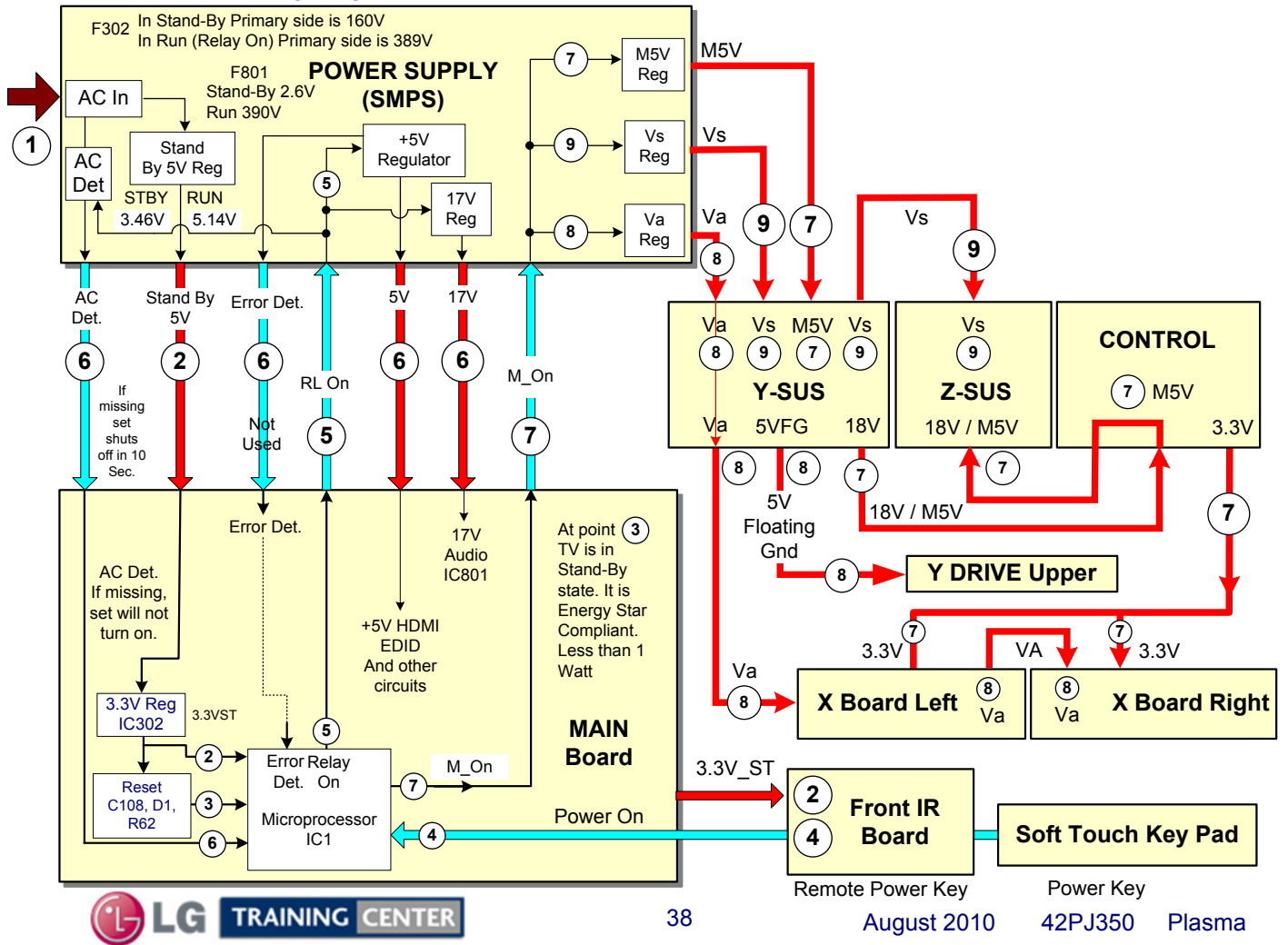
When **RL_ON** arrives, the run voltage +5V source becomes active and is sent to the Main Board via P813 (5.24V at pin 5, 6 and 7). The (Error Det) from the SMPS Board to the Main Board can be measured at pin 8 of P813 (2.88V STBY and 4.93V RUN), but it is not used. The **RL-ON** command also turns on the 17V (Audio B+ 16.79V) which is also sent to the Main Board. The 17V Audio supply outputs to the Main board at P813 pins 1 and 2 and used for Audio processing and amplification.

The next step is for the Microprocessor IC1 on the Main Board to output a high (3.27V) on **M_ON** Line to the SMPS at P813 Pin 17 which is sensed by the Controller IC701, turning on the M5V line and outputs at P811 pins 9 and 10 to the Y-SUS board.

The Controller (IC701) also uses the **M_ON** line to turn on the VA and the VS supplies. (Note there is no VS On Command in this set). VS is output at P811 to the Y-SUS board P201. (VA pins 6 and 7 and VS pins 1 and 2). Note: The Va is fused on the Y-SUS then routed out P209 to the X-Board Left. VS is also routed out of the Y-SUS P206 pins 1 and 2 to the Z-SUS P2.

AUTO GND Pin 18 of P813: This pin is grounded on the Main board. When it is grounded, the Controller (IC701) works in the normal mode, meaning it turns on the power supply via commands sent from the Main board. When **AUTO GND** is floated (opened), it pulls up and places the Controller (IC701) into the Auto mode. In this state, the Controller turns on the power supply in stages automatically. A load is necessary to perform a good test of the SMPS if the Main board is suspect.

42PJ350 Television Start Up Sequence



Power Supply Va and Vs Adjustments

**Important: Use the Panel Label
Not this book for all voltage adjustments.**

Use Full White Raster "White Wash"

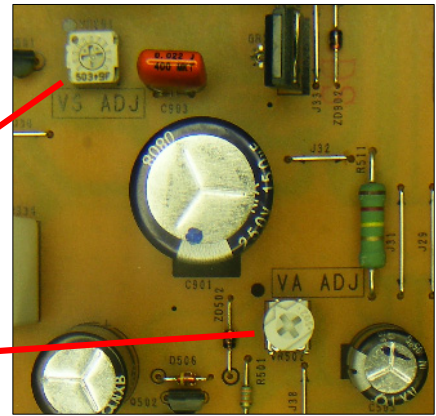
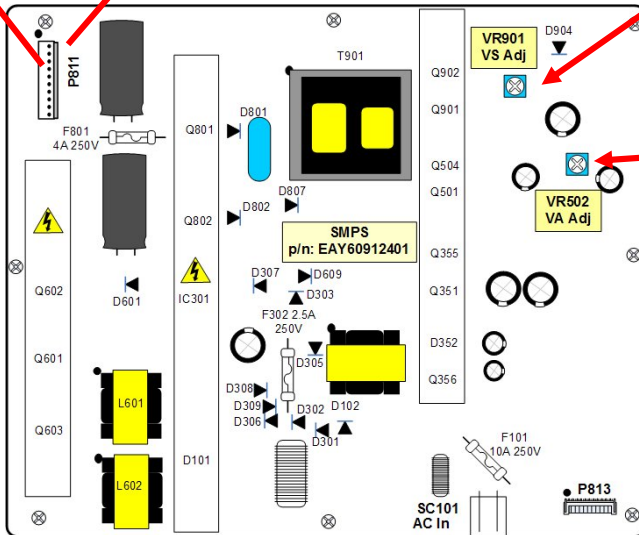
**Example
Voltage Label**

Model : PDP 42T1###
Voltage Setting: 5V/ **Va:60** / **Vs:205**
N.A. / -195 / 145 / N.A. / 110
Max Watt : 250 W (Full White)

VA VS

**Vs TP
Pin 1 or 2**

**Va TP
Pin 6 or 7**



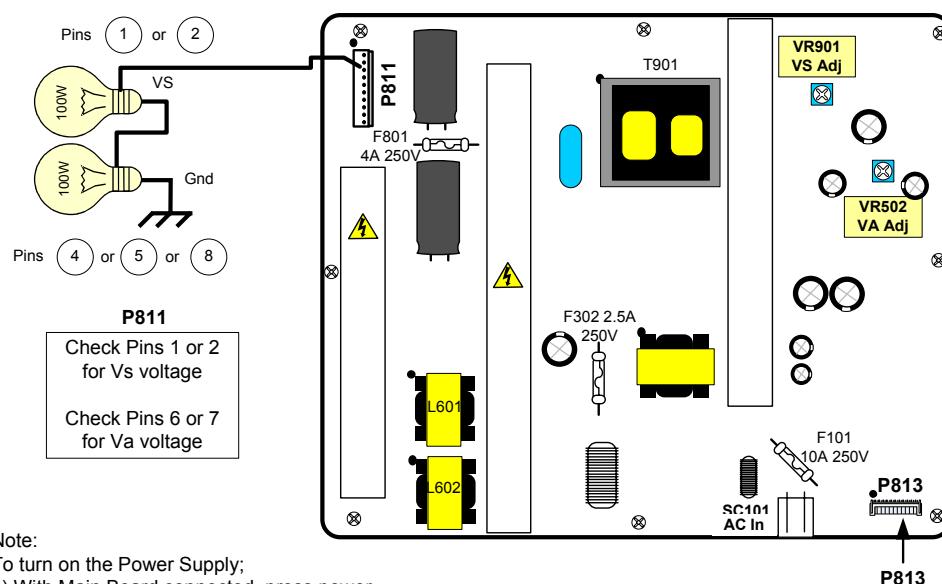
Vs Adjust:
Place voltmeter on VS TP.
Adjust VR901 until the reading
matches your Panel's label.

Va Adjust:
Place voltmeter on VA TP.
Adjust VR502 until the reading
matches your Panel's label.

42PJ350 Power Supply Static Test with Light Bulb Load

Using two 100 Watt light bulbs, attach one end to Vs and the other end to ground. Apply AC to SC101. If the light bulbs turn on and VS is the correct voltage, allow the SMPS to run for several minutes to be sure it will operate under load. If this test is successful and all other voltages are generated, you can be fairly assured the power supply is OK.

Note: To be 100% sure, you would need to read the current handling capabilities of each power supply listed on the silk screen on the SMPS and place each supply voltage under the appropriate load.



Power Supply Static Test (Forcing on the SMPS in stages)

WARNING: Remove AC when adding or removing any plug or resistor.

TEST CONDITIONS:

Connector going to the Y-SUS P811 is disconnected.

P301 on the Main board disconnected (coming in on P813).

Use the holes on the connector P301 (Main Board side) to insert the resistors or jumper leads.

Connect (2) 100 Watt light bulbs in series between VS and Ground.

When the supply is operational in its normal state the Auto Ground line at Pin 18 of P813 is held at ground by the Main Board.

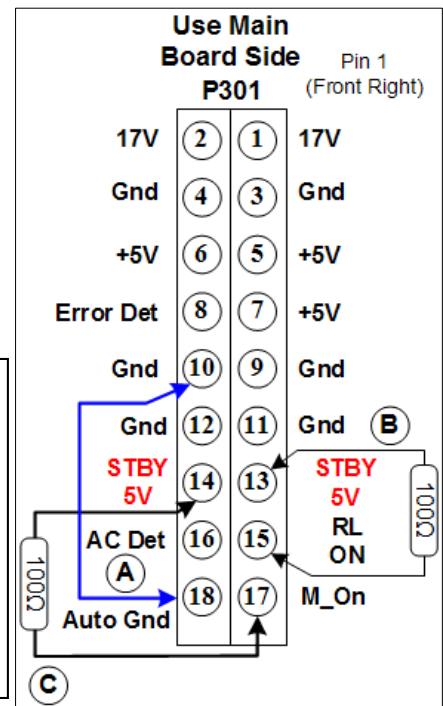
This Power Supply can be powered on sequentially to test the Controller Chip IC701 operational capabilities and for troubleshooting purposes.

By disconnecting P301, pin 18 is opened. To return the SMPS to the normal state for this test procedure, this pin must be grounded.

(See first step A below).

Note: Leave previous installed 100Ω resistor in place when adding the next resistor.

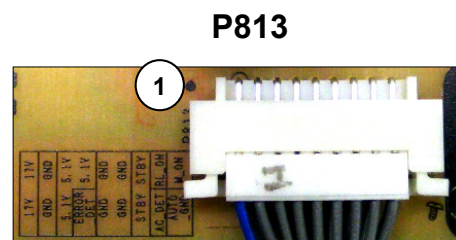
- (A) Ground the Auto Gnd Line (Pin 18) will allow the supply to be powered up one section at a time.
- (B) Add a 100Ω ¼ watt resistor from 5V Standby to RL_ON and the 17V and 5V Run Lines on P813 will become active. Also AC-Det and Error_Det will go high.
- (C) Add a 100Ω ¼ watt resistor from any 5V line to M_ON (Monitor On) to make the M5V, VS and VA lines operational. P811 (VS pins 1 and 2) (VA pins 6 and 7) and the (M5V pins 9 and 10).



SMPS Connector P813 Identification, Voltages and Diode Check

P813 Connector "SMPS" to "Main" P301

Pin	Label	STBY	Run	No Load	Diode
1~2	^a 17V	0V	16.8V	16.79V	Open
3~4	Gnd	Gnd	Gnd	Gnd	Gnd
5~7	5V	0.47V	5.24V	5.25V	1.29V
8	^c Error_Det	2.88V	4.93V	4.91V	2.96V
9~12	Gnd	Gnd	Gnd	Gnd	Gnd
13~14	STBY_5V	3.49V	5.23V	5.25V	2.43V
15	RL_ON	0V	2.43V	0.0V	Open
16	^d AC Det	0V	4.45V	4.93V	2.95V
17	^b M_ON	0V	3.27V	0.0V	Open
18	^e Auto_Gnd	Gnd	Gnd	4.84V	2.34V



Note: This connector has two rows of pins.
Odd on bottom row.

^a Note: The 17V, 5V, AC_Det and Error Det turn on when the RL_On command arrives.

^b Note: The M5V, Va and Vs turn on when the M_On (Monitor On) command arrives.

^c Note: The Error Det line is not used in this model.

^d Note: If the AC Det line is Missing, the TV will shut off after 10 seconds of operation.

^e Note: Pin 18 is grounded on the Main board. If this line is floated, the SMPS turns on Automatically when AC is applied.

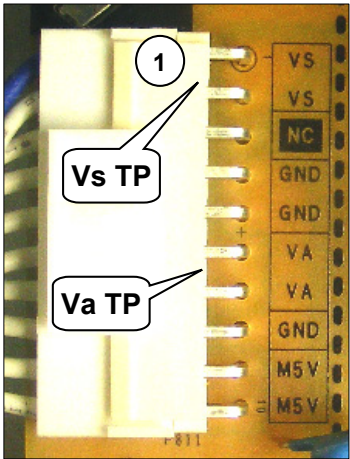
Diode Mode Readings taken with all connectors Disconnected. DVM in Diode Mode.

SMPS Connector SC101 and P811 Identification, Voltages and Diode Check

SC101 AC INPUT

Connector	Pin Number	Standby	Run	Diode Mode
SC101	L and N	120VAC	120VAC	Open

P811



P811 "Power Supply" to Y-SUS "P201"

Pin	Label	Run	Diode Mode
1, 2	*Vs	*206V	Open
3	n/c	n/c	n/c
4, 5	Gnd	Gnd	Gnd
6, 7	*Va	*60V	Open
8	Gnd	Gnd	Gnd
9, 10	M5V	5.25V	2.12V

* Note: This voltage will vary in accordance with Panel Label

Y-SUS routes Va to bottom X-Left. Vs routed to Z-SUS from P206.
M5V routed through Y-SUS to Control board and then to Z-SUS.

Diode Mode Readings taken with all connectors Disconnected. DVM in Diode Mode.

Y-SUS BOARD SECTION (Overview)

Y-SUS Board develops the V-Scan drive signal to the Y-Drive boards.

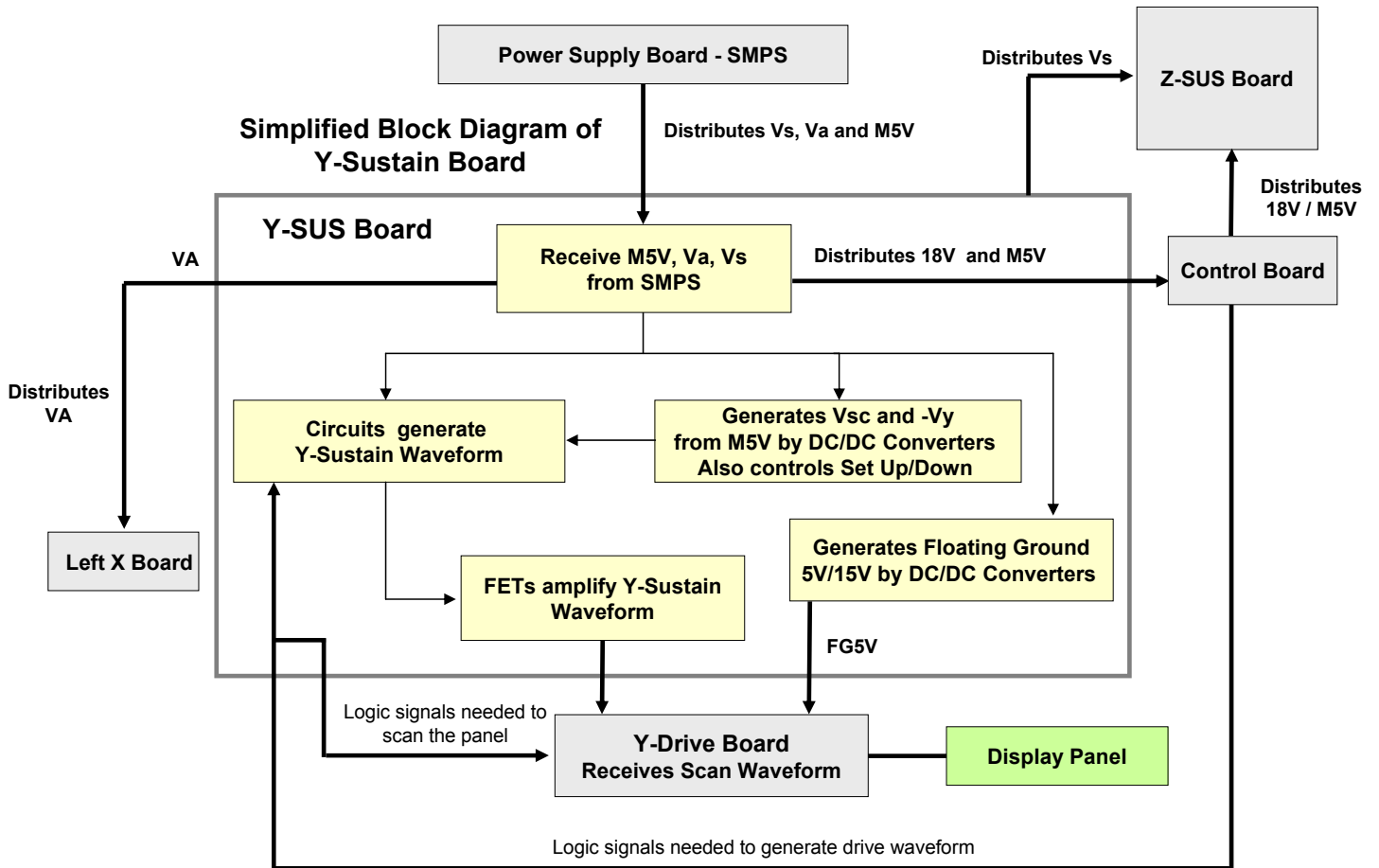
This Section of the Presentation will cover alignment and troubleshooting the Y-SUS Board for the Single Scan Plasma. Upon completion of the Section the technician will have a better understanding of the operation of the circuit and will be able to locate voltage and Diode mode test points needed for troubleshooting and alignments.

- Adjustments
- DC Voltage and Waveform Checks
- Diode Mode Measurements

OPERATING VOLTAGES

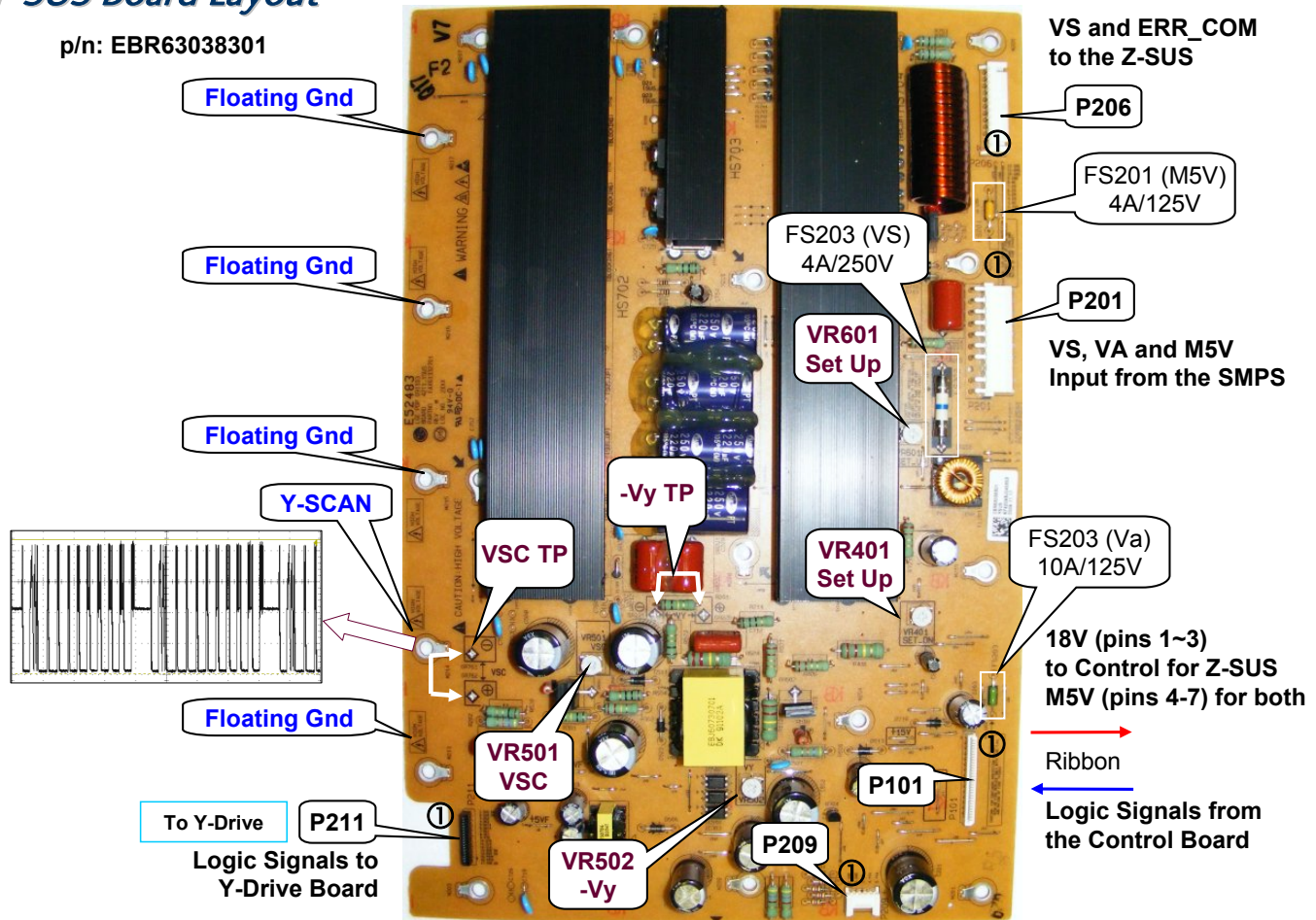
<u>SMPS Supplied</u>	VA	VA supplies the Panel's Vertical Electrodes (Routed to the Left X-Board)
	VS	VS Supplies the Panel's Horizontal Electrodes. Also Routed to the Z-SUS board.
	M5V	M5V Supplies Bias to Y-SUS. (Also routed to the Control Board then Z-SUS).
<u>Y-SUS Developed</u>	-VY VR502	-VY Sets the Negative excursion of Reset in the Drive Waveform
	VSC VR501	VSC Sets the amplitude of the complex waveform.
	V SET UP VR601	SET UP sets amplitude of the Top Ramp of Reset in the Drive Waveform
	V SET DN VR401	SET DOWN sets the Pitch of the Bottom Ramp for Reset in the Waveform
	18V	Used internally to develop the Y-Drive signal. (Also routed to the Control Board then routed to the Z-SUS board).
<u>Floating Ground</u>	FG 5V	Used on the Y-Drive board (Measured from Floating Gnd)
	FG 15V	Used in the Development of the Y-Drive Waveform (Measured from Floating Gnd)

Y-SUS Block Diagram



Y-SUS Board Layout

p/n: EBR63038301



Va to Left X Board Pins 5~7

42PJ350 Y-SUS Layout Drawing

Example:

Model : PDP 42T1###
Voltage Setting: 5V/ Va:60/ Vs:205
N.A. / -195/ 145 / N.A. / 110
Max Watt : 250 W (Full White)

-Vy VSC

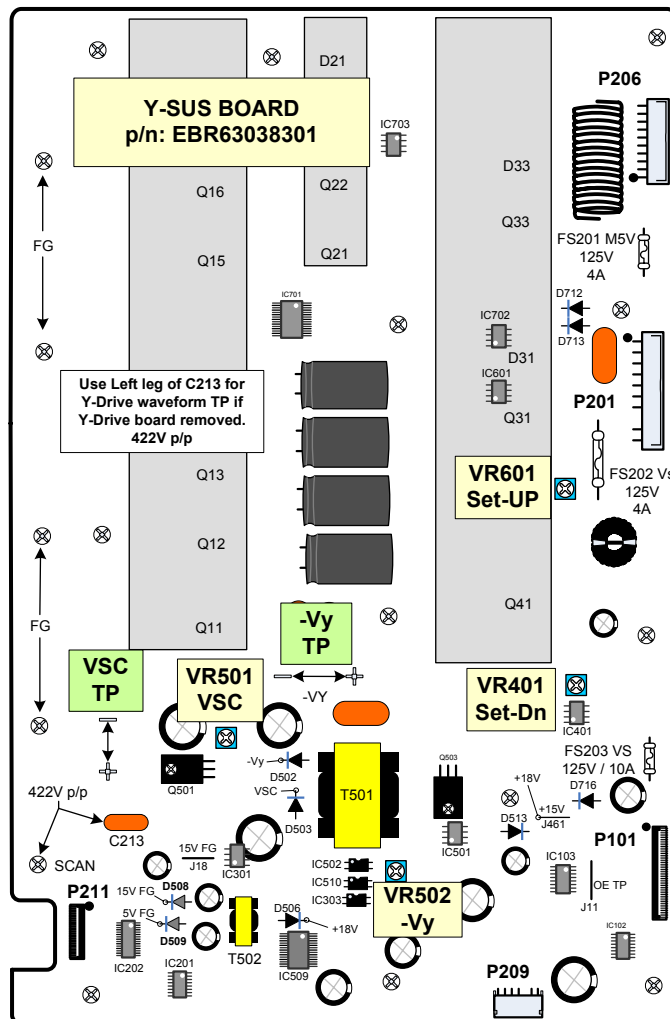
WARNING:
The Y-DRIVE Board has to be removed completely if P211 is removed.

P211 Connector Y-SUS to Y-Drive P106

Pin	Label	Run	Diode Check
1	SUS_DN (FG)	FG	FG
2	SUS_DN (FG)	FG	FG
3	OC2	2.63V	1.46V
4	OC2	2.63V	1.45V
5	DATA	0V	1.36V
6	DATA	0V	1.37V
7	OC1	2.2V	1.45V
8	OC1	2.2V	1.45V
9	STB	2.8V	1.36V
10	STB	2.8V	1.36V
11	CLK	0.86V	1.36V
12	CLK	0.86V	1.36V
13	SUS_DN (FG)	FG	FG
14	SUS_DN (FG)	FG	FG
15	FG5V	4.9V	1.97V
16	FG5V	4.9V	1.96V
17	SUS_DN (FG)	FG	FG

From VS
T501 Driver IC501
-Vy - D502
VSC - D503 to Q501

From MSV
T502 Driver IC509
18V - D506
FG 5V - D509
FG 15V - D508



P206 Connector Y-SUS to Z-SUS P2

Pin	Label	Run	Diode Check
1~2	+Vs	*206V	Open
3	n/c	n/c	n/c
4~7	ER_PASS	133V	Open
6	n/c	n/c	n/c
9~12	Gnd	Gnd	Gnd

P201 Connector Y-SUS to SMPS P811

Pin	Label	Run	Diode Check
1~2	VS	*206V	Open
3	n/c	n/c	n/c
4~5	Gnd	Gnd	Gnd
6~7	VA	*60V	Open
8	Gnd	Gnd	Gnd
9~10	M5V	5.25V	2.12V

P101 Connector Y-SUS to Control P101

Pin	Label	Run	Diode Check
1~3	+15V	18.24V	1.14V
4~7	+5V	5V	1.11V
8~11	Gnd	Gnd	Gnd
12	Dummy_2	2.14V	2.80V
13	Y-OE	0.02V	1.81V
14	OC2	1.85V	2.81V
15	ER_DN	1.05V	2.81V
16	DATA	0V	2.81V
17	ER_UP	0.26V	2.81V
18	BLK	1.4V	2.81V
19	SET_UP	0.24V	2.81V
20	STB	1.5V	2.81V
21	Dummy_5	1.05V	3.19V
22	CLK	0.59V	2.81V
23	SUS_DN	2.75V	2.81V
24	Dummy_3	1.97V	2.81V
25	Dummy_1	1.04V	2.81V
26	Dummy_4	1.23V	3.19V
27	SUS_UP	0.05V	2.81V
28	CTL_OE	0.23V	3.18V
29	SET_DN	2.10V	2.81V
30	Gnd	Gnd	Gnd

VSC and -VY Adjustments

CAUTION: Use the actual panel label and not the book for exact voltage settings.

These are DC level Voltage Adjustments

This is just for example

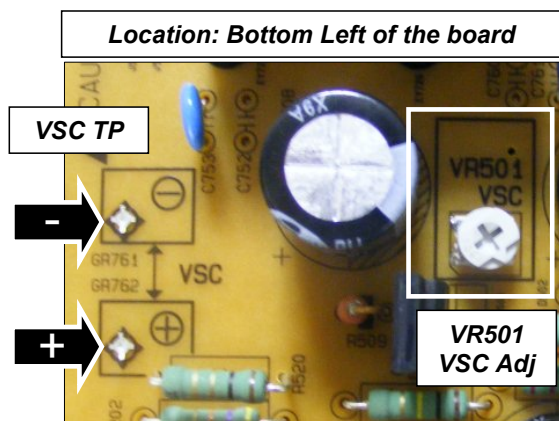
Model : PDP 42T1###
Voltage Setting: 5V/ Va:60/ Vs:205
N.A. / -195 / 145 / N.A. / 110
Max Watt : 250 W (Full White)

-Vy

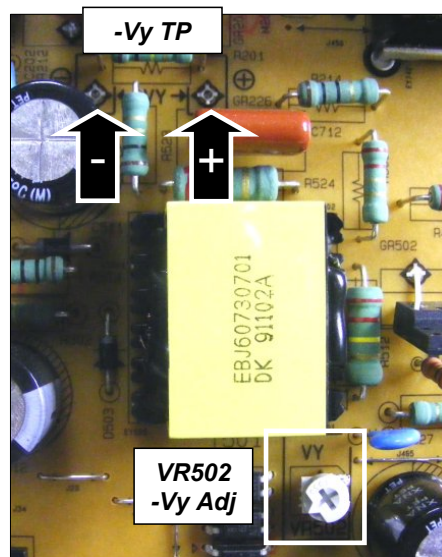
VSC

Set should run for 15 minutes, this is the "Heat Run" mode.
Set screen to "White Wash".

- 1) Adjust -Vy VR502 to Panel's Label voltage (+/- 1V)
- 2) Adjust VSC VR501 to Panel's Label voltage (+/- 1V)



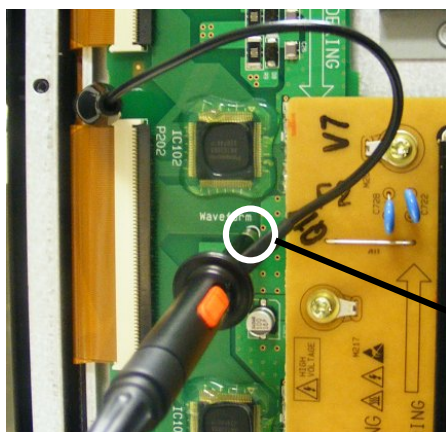
Voltages Reads
Positive



Location: Bottom Center of board
Just above Transformer

Y-Drive Signal Overview

**Y-Drive Test Point
(Under 2nd Buffer)**



NOTE: The Waveform Test Points are fragile. If by accident the land is torn and the run lifted, make sure there are no lines left to right in the screen picture.

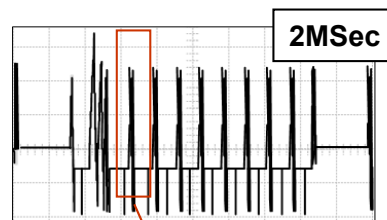
There are several other test points on either the Upper or Lower Y-Drive boards that can be used. Basically any output pin on any of the FPC to the panel are OK to use.

① Overall signal observed 2mS/div

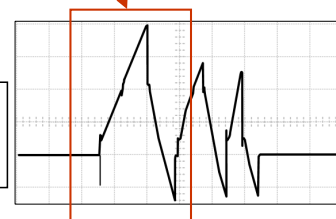
69 to 72 Vrms

540V p/p

White to Black

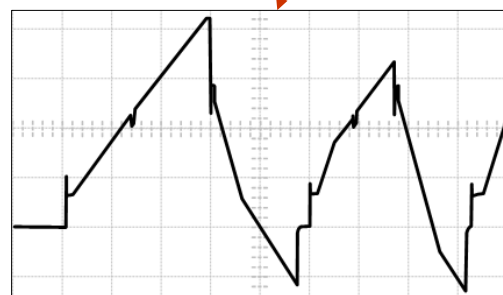


② Highlighted signal from waveform above observed 200uS/div



200uSec

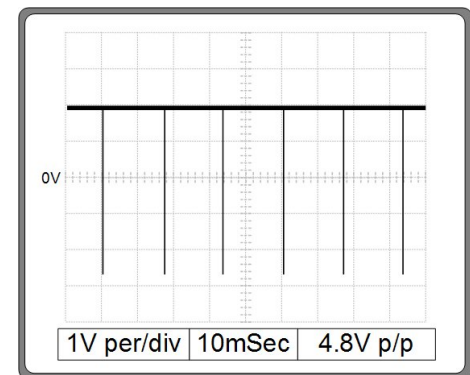
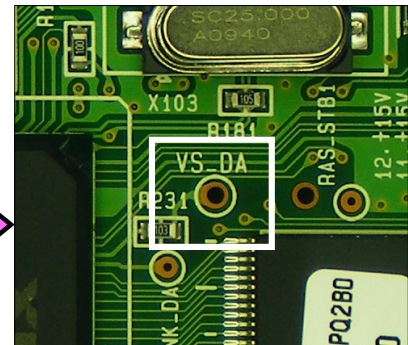
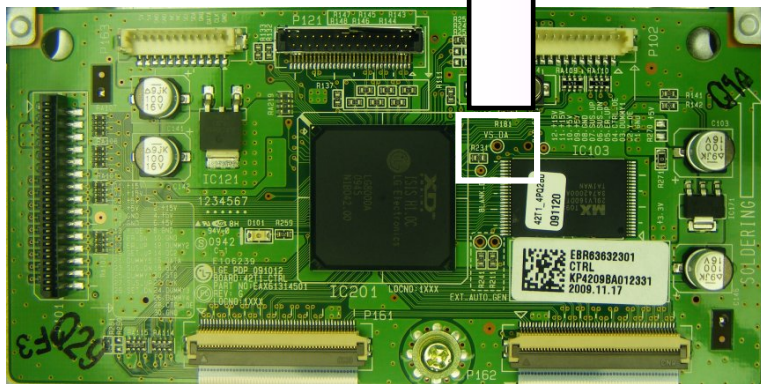
③ Highlighted signal from waveforms above observed 100uS/div



100uSec

Locking on to the Y-Drive Waveform Tip

Note, this TP (VS_DA) can be used as an External Trigger for scope when locking onto the Y-Drive (Scan) or the Z-Drive signal.



This signal can also be used to help lock the scope when observing the LVDS video signals.

Observing (Capturing) the Y-Drive Signal for Set Up Adjustment

Set must be in "WHITE WASH"
All other DC Voltage adjustments should have already been made.

Fig 1:

As an example of how to lock in to the Y-Drive Waveform.
Fig 1 shows the signal locked in at 2ms per/div.
Note the 2 blanking sections.
The area for adjustment is pointed out within the Waveform

Fig 2:

At 200uSec per/division, the area of the waveform to use for **SET-UP** or **SET-DN** is now becoming clear.
Now the only two blanking signals are present.

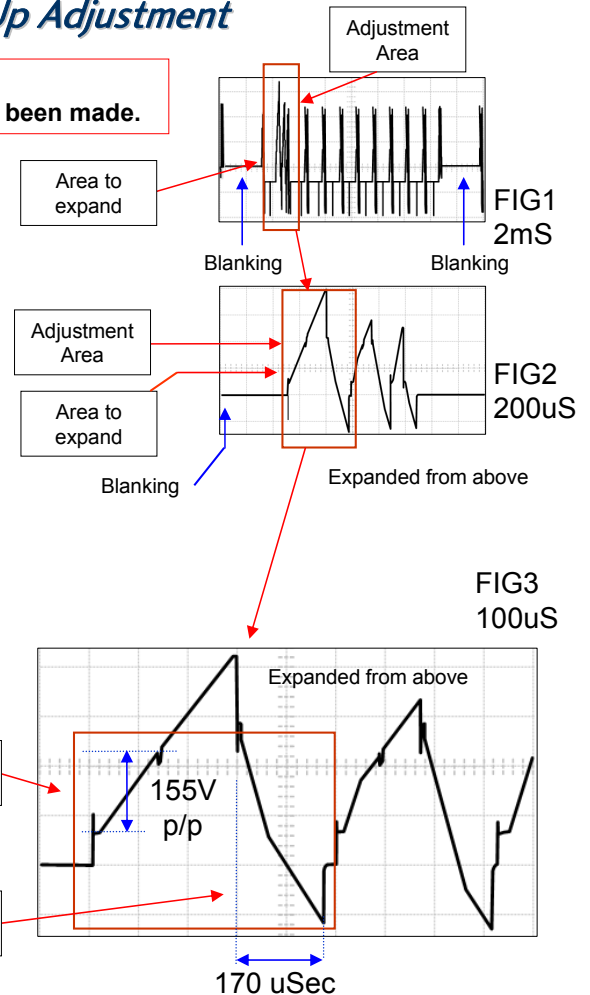
Fig 3:

At 100us per/div the area for adjustment of **SET-UP** or **SET-DN** is now easier to recognize. It is outlined within the Waveform.
Remember, this is the 1st large signal to the right of blanking.

TIP: If you expand to 40uSec per/division, the adjustment for:

SET-UP can be made using **VR601** and the
SET-DN can be made using **VR401**.

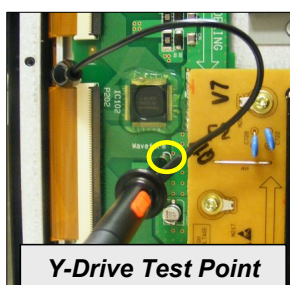
It will make this adjustment easier if you use the "Expanded" mode of your scope.



Set Up and Set Down Adjustments

Set must be in "WHITE WASH"
All other DC Voltage adjustments should have already been made.

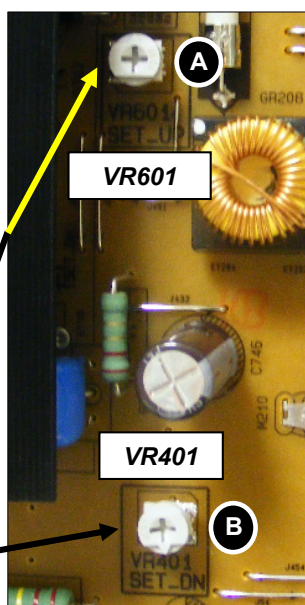
Observe the Picture while making these adjustments. Normally, they do not have to be done.



Y-Drive Test Point

Under 2nd Buffer from top

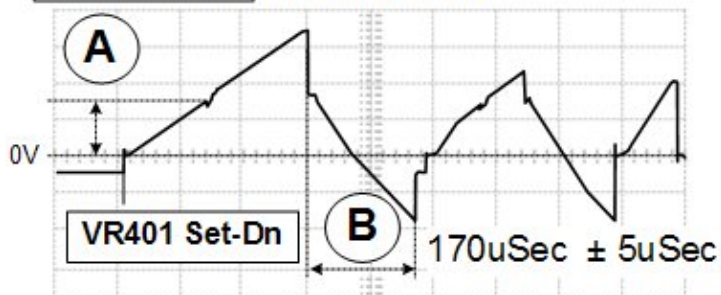
ADJUSTMENT LOCATION:
Center Right of the board.



ADJUSTMENT LOCATION:
Lower Center Right
of the board.

Waveform TP on the Y-Drive Board

VR601 Set-up 155V p/p \pm 5V



69VAC rms "White"
72VAC rms "Black"

100V 100uS 540V p/p

SET-UP ADJUST:

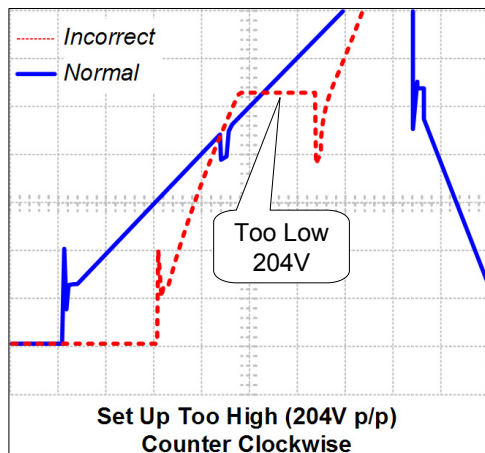
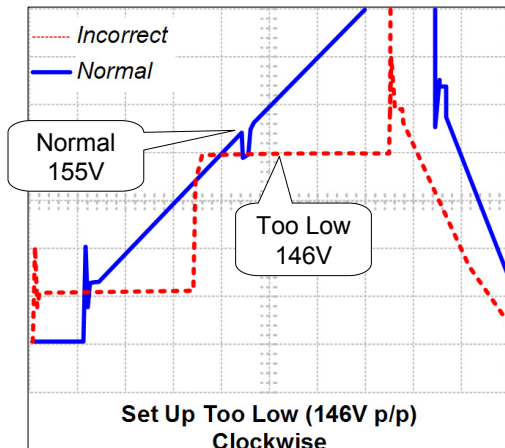
1) Adjust **VR601** and set the (A) portion of the signal to match the waveform above. (155V p/p \pm 5V)

SET-DN ADJUST:

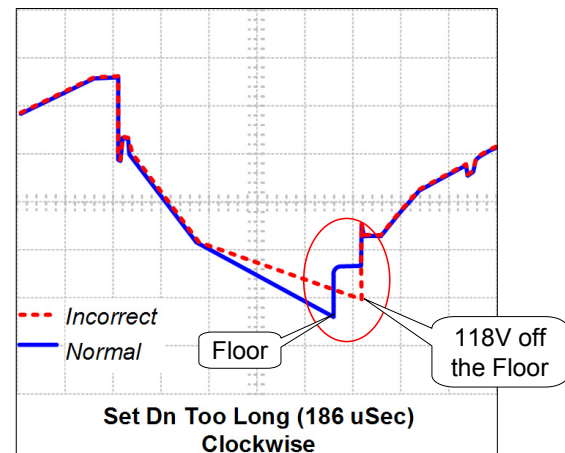
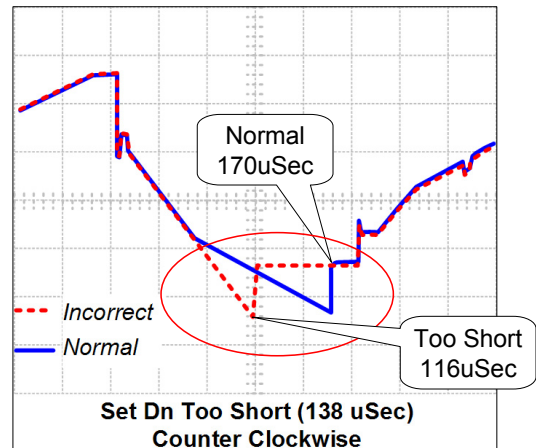
2) Adjust **VR401** and set the (B) time of the signal to match the waveform above. (170uSec \pm 5uSec)

Set Up or Down Adjustment Extremes

Set Up swing is Minimum 146V Max 204V p/p



Set Dn swing is Minimum 138uSec Max 186uSec



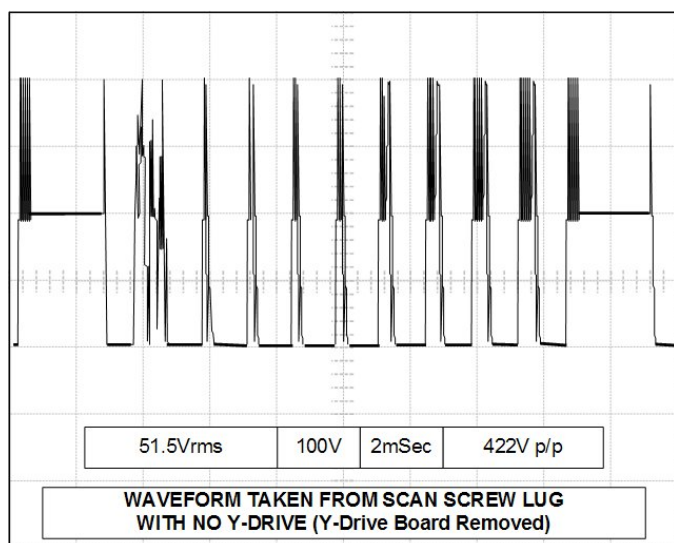
Y-SUS Board Troubleshooting Y-Scan

TIP: Use the Scan Output Screw Lug to test for V-Scan signal when the Y-Drive board is removed

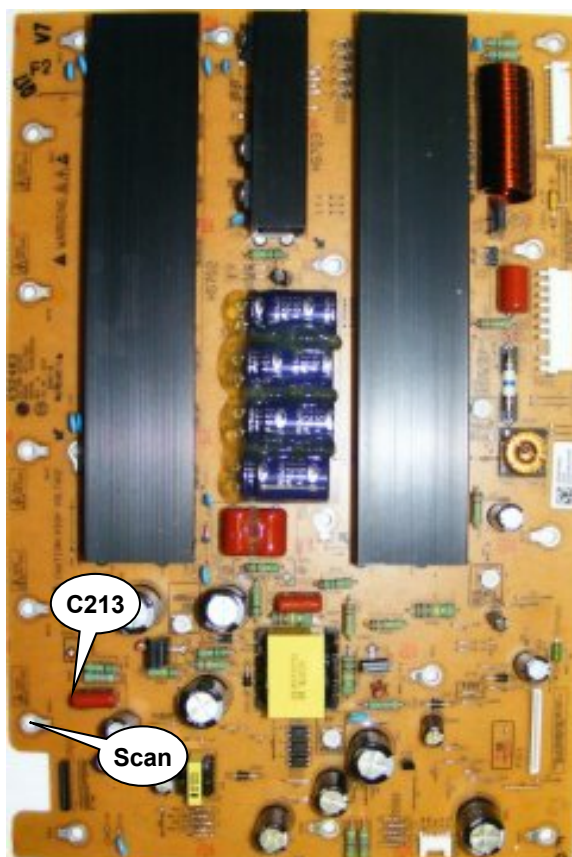
Y-SUS Board develops the Y-Scan drive signal to the Y-Drive board.

The Y-SUS (Y-Scan) signal can be checked (422V p/p) if the Y-Drive board is removed.

Warning: Never run the Y-SUS with P211 (Y-SUS) or P106 (Y-Drive) removed unless the Y-Drive board is removed completely. Board Failures will occur.



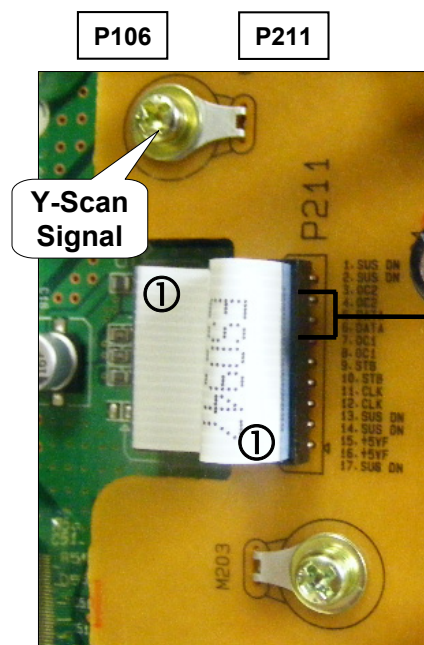
TIP: You can also use C213 left leg to test for V-Scan signal when the Y-Drive board is removed



Y-SUS Board P211 Connector to P106 Y-Drive (Logic and FG5V)

TIP: This Connector do not come with a new Y-SUS or Y-Drive.

TIP: Use Scan Screw Lug to test for Y-Scan signal if the Y-Drive board is removed.



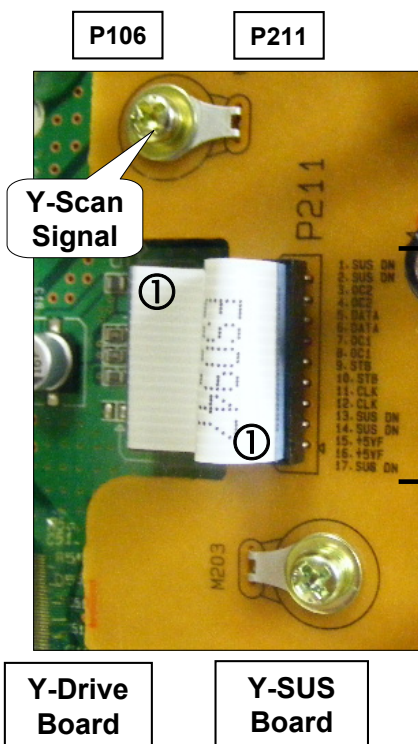
FG5V (4.9V) measured from Pins 15 or 16 to Floating Gnd.

For Floating Ground, use any screw on the far left hand side of the Y-SUS board except the one just above P211, this is the Y-Scan output.

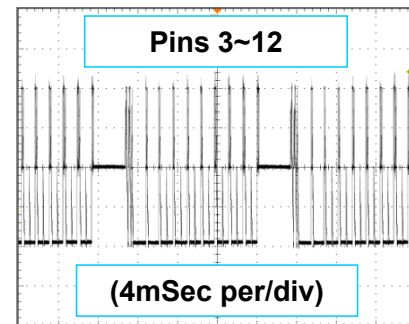
Y-Drive Board

Y-SUS Board

Y-SUS Board P211 to Y-Drive P106 Logic Signals Explained



P211 Connector	
Pin	Label
17	SUS_DN (FG)
15-16	FG5V
13-14	SUS_DN (FG)
11-12	CLK
9-10	STB
7-8	OC1
5-6	DATA
3-4	OC2
1-2	SUS_DN (FG)

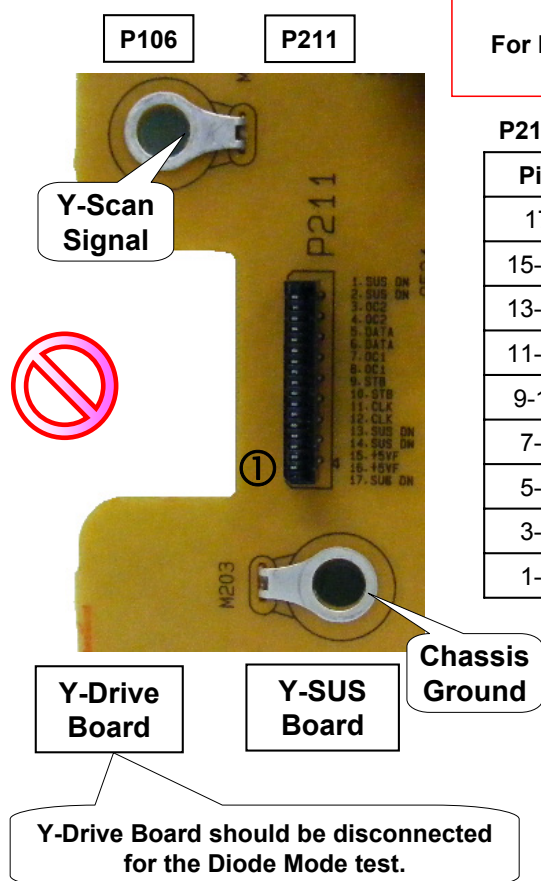


The signal for these pins look very similar due to the fact they are read from Chassis Gnd, but they are actually Floating Ground related. **DO NOT** hook scope Gnd to Floating Gnd TP without an Isolation Transformer.

All logic pins about (420V p/p)

Pins 3~12 are Logic (Drive) Signals to the Y-Drive Upper.

Y-SUS P211 Connector Diode Mode Testing



Measurements taken from Floating Gnd.
For Floating Ground, use any screw on the far left hand side of the Y-SUS board except the one just above P211, this is the Y-Scan output.

P211 "Y-SUS" to "Y-Drive" P106

Red Lead on FG

Pin	Label	Run	Diode Check	Diode Check
17	SUS_DN (FG)	FG	FG	FG
15-16	FG5V	4.9V	1.97V	0.59V
13-14	SUS_DN (FG)	FG	FG	FG
11-12	YB_CLK	0.86V	1.36V	0.53V
9-10	YB_STB	2.8V	1.36V	0.53V
7-8	YTB_OC1	2.2V	1.45V	0.68V
5-6	YT_DATA	0V	1.36V	0.53V
3-4	YB_OC2	2.63V	1.46V	0.68V
1-2	SUS_DN (FG)	FG	FG	FG

Red Lead

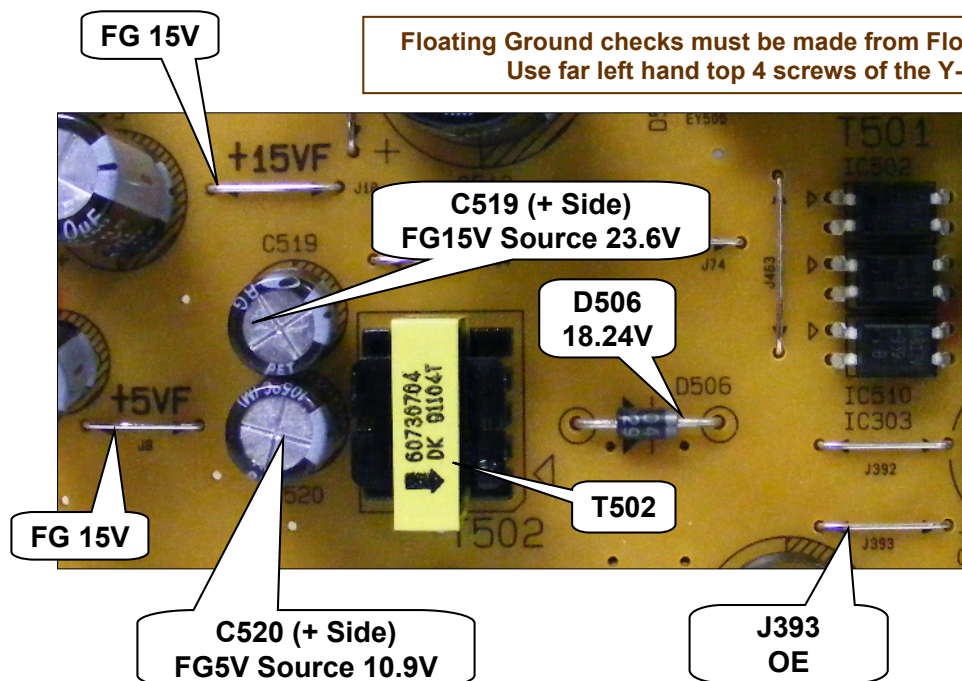
Black Lead

Diode Mode Readings taken with all connectors Disconnected.
DVM in Diode Mode.

Y-SUS Floating Ground (FG 15V) and (FG 5V) Checks

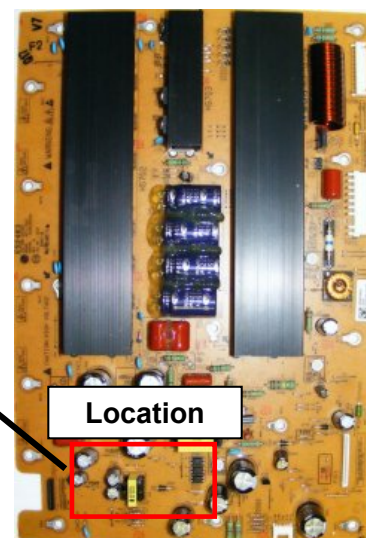
**TIP: Some Circuit components are on the back of the board. To Test these voltages, remove the board completely, supply Ground and any 5V supply to M5V fuse FS201.
Ground OE Jumper J393.**

**Floating Ground checks must be made from Floating Ground.
Use far left hand top 4 screws of the Y-SUS.**



Source FG5V (Floating Ground 5V). D509 cathode.
Source FG15V (Floating Ground 15V). D508 cathode.

Location Back Side of Board



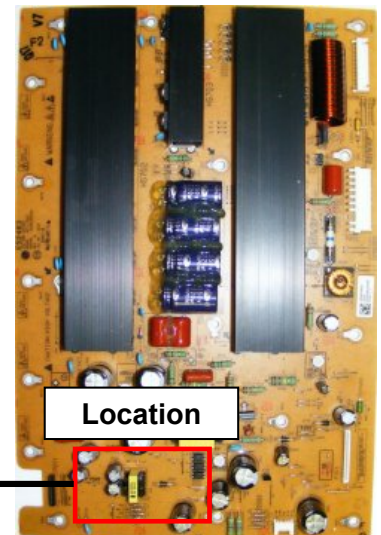
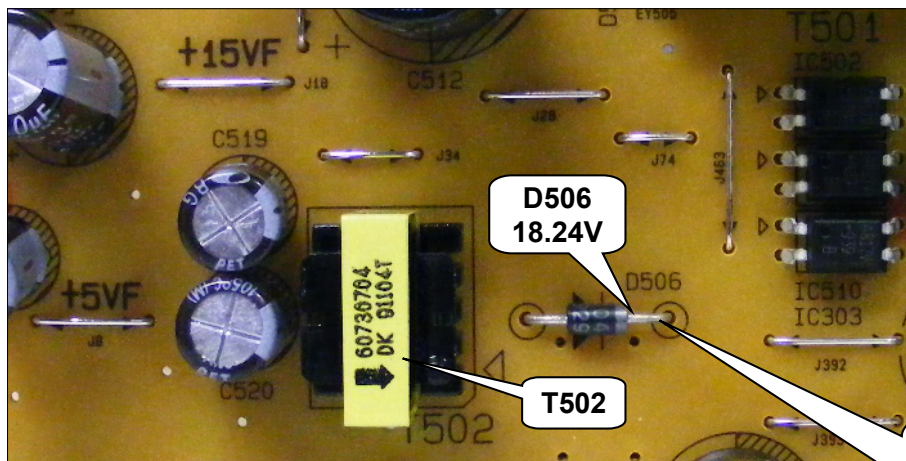
Y-SUS 18V Generation Checks

Voltage Measurements for the Y-SUS Board

18V Test Point

Used in the Y-SUS for Waveform Creation and Leaves the Y-SUS board on P101 pins 1~3 to the Control Board.
Checked at Cathode Side D506.

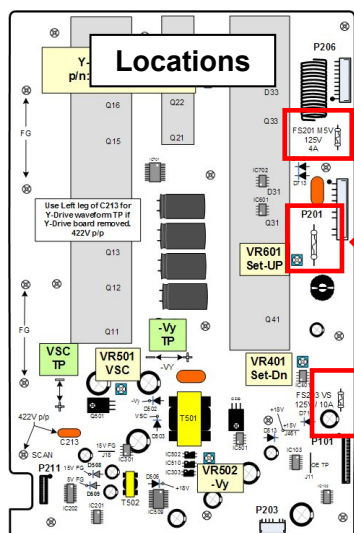
Standby: 0V Run: 18.24V Diode Check: 1.14V



Location

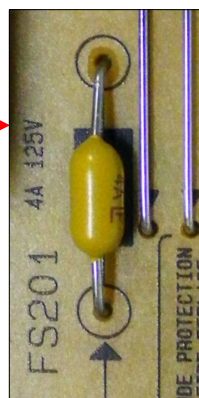
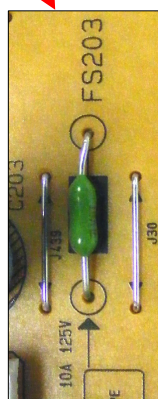
D506
18V Source
Cathode Right Side
Just to the right of T502

Y-SUS Fuse Information



FS203
(VA)
10A/125V

FS203 Protects VA which leaves
the Y-SUS on P203.
Diode Check Open
With Board
Disconnected or Connected.



FS201 Protects M5V
Used for 18V, (D506),
FG5V and FG15V Creation
(D508 and D509).
Also, M5V leaves the Y-SUS
on P101 for the Control board
and for the Z-SUS.

FS201 (M5V)
4V/125V

Diode Check 1.19V
With Board Disconnected. 0.65V
with board connected.



FS202 Protects VS

FS202 (VS)
4V/250V

Diode Check Open
With Board
Disconnected or Connected.

Y-SUS P201 and P206 Plug Information

Voltage and Diode Mode Measurement

P206 "Y-SUS" to "Z-SUS" P2

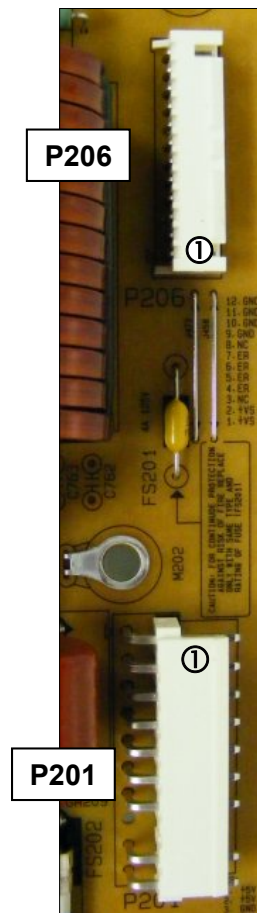
Pin	Label	Run	Diode Check
9~12	Gnd	Gnd	Gnd
8	n/c	n/c	Open
4~7	ER_PASS	133V	Open
3	n/c	n/c	Open
1~2	Vs	*206V	Open

P201 Connector "Y-SUS" to "Power Supply" P811

Pin	Label	Run	Diode Check
1~2	Vs	*206V	Open
3	n/c	n/c	n/c
4~5	Gnd	Gnd	Gnd
6~7	Va	*60V	Open
8	Gnd	Gnd	Gnd
9~10	M5V	5.25V	2.12V

* Note: These voltages will vary in accordance with Panel Label

Diode Mode Readings taken with all connectors Disconnected. DVM in Diode Mode.

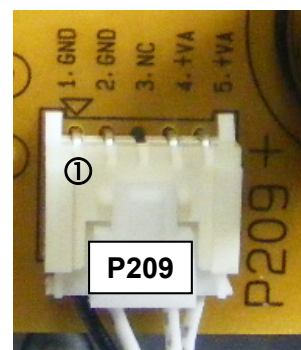


Y-SUS P209 Plug Information

Voltage and Diode Mode Measurement

P211 Connector "Y-SUS" to "Z-SUS" P2

Pin	Label	Run	Diode Check
1~2	Gnd	Gnd	Gnd
3	n/c	n/c	n/c
4~5	*Va	*60V	Open



* Note: This voltage will vary in accordance with Panel Label

Diode Mode Readings taken with all connectors Disconnected. DVM in Diode Mode.

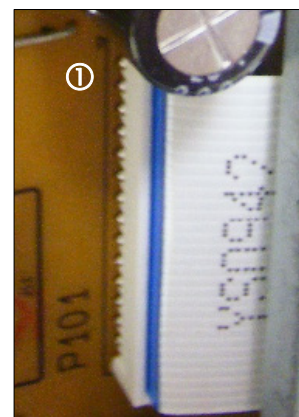
Y-SUS P101 to Control P101 Plug Voltage Checks

There are No Stand By Voltages on this Connector

P101 Connector "Y-SUS" to P111 "Control"

Pin	Label	Run	Diode	Pin	Label	Run	Diode
1	+15V	18.24V	1.24V	16	DATA	0V	2.81V
2	+15V	18.24V	1.24V	17	ER_UP	0.26V	2.81V
3	+15V	18.24V	1.24V	18	BLK	1.40V	2.81V
4	+5V	5V	1.11V	19	SET_UP	0.24V	2.81V
5	+5V	5V	1.11V	20	STB	1.50V	2.81V
6	+5V	5V	1.11V	21	Dummy_5	1.05V	3.19V
7	+5V	5V	1.11V	22	CLK	0.59V	2.81V
8	Gnd	Gnd	Gnd	23	SUS_DN	2.75V	2.81V
9	Gnd	Gnd	Gnd	24	Dummy_3	1.97V	2.81V
10	Gnd	Gnd	Gnd	25	Dummy_1	1.04V	2.81V
11	Gnd	Gnd	Gnd	26	Dummy_4	1.23V	3.91V
12	Dummy_2	2.14V	2.80V	27	SUS_UP	0.05V	2.81V
13	Y_OE	0.02V	1.81V	28	CTL_OE	0.23V	3.19V
14	OC2	1.85V	2.81V	29	SET-DN	0.05V	2.81V
15	ER_DN	1.05V	2.81V	30	Gnd	Gnd	Gnd

TIP: Use the Control Board (P101) side of this connector to make voltage readings.



Diode Mode Readings
taken with all connectors
Disconnected.
DVM in Diode Mode.

Y-DRIVE BOARD SECTION (Y-Drive Explained)

p/n: EBR63633601



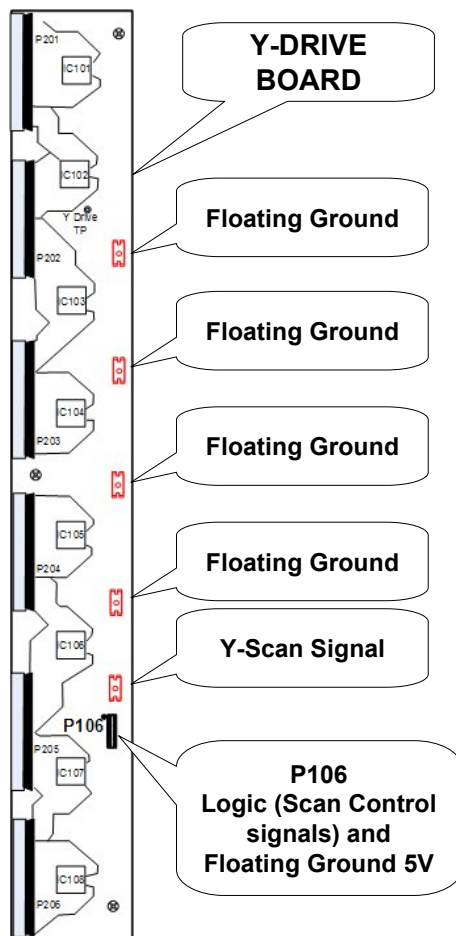
Y-DRIVE BOARD

Y-Drive Board works as a path supplying the Sustain and Reset waveforms which are made in the Y-Sustain board and sent to the Panel through Scan Driver IC's.

The Y-Drive Boards receive a waveform developed on the Y-SUS board then selects the horizontal electrodes sequentially starting at the top and scanning down the panel. Scanning is synchronized by receiving Logic scan signals from the Control board.

The 42PJ350 uses 8 Driver ICs on one Y-Drive Board commonly called "Y-Drive Buffers" but are actually Gate Arrays.

Y-Drive Board Layout



Key Points of interest are;

There are 6 FPC (Flexible Ribbon Cables) connecting the Y-Drive board to the Panel. These FPC connect to a total of 768 individual electrodes determining Vertical resolution.

If the connector P106 is removed and the unit is powered up with the lugs for Floating Gnd and Scan making contact with the Y-SUS board, the Y-SUS or Y-Drive or both boards will fail.

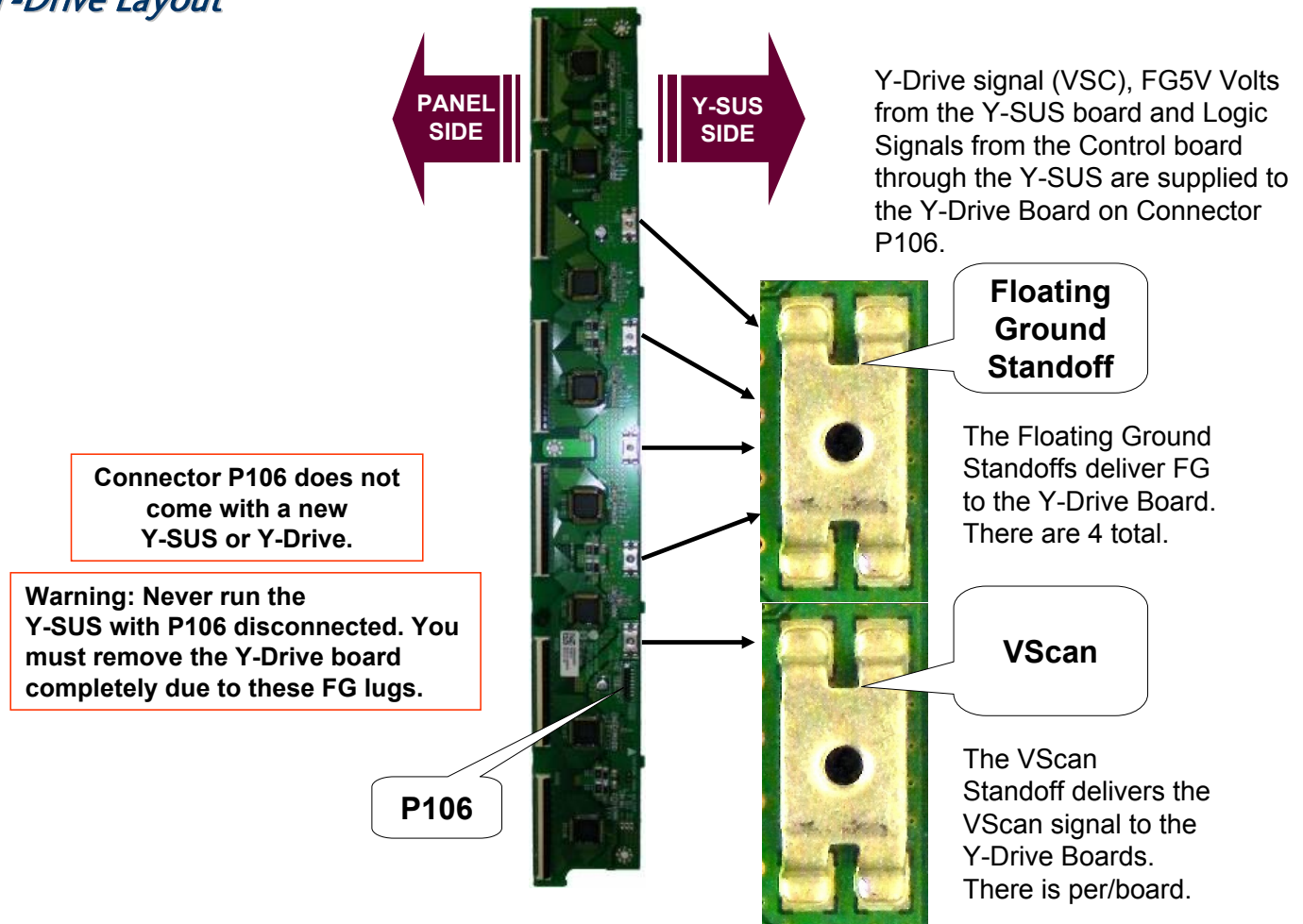
Floating Ground is delivered to the Y-Drive board by 4 screw lugs.

Scan is delivered to the Y-Drive board by 1 screw lugs.

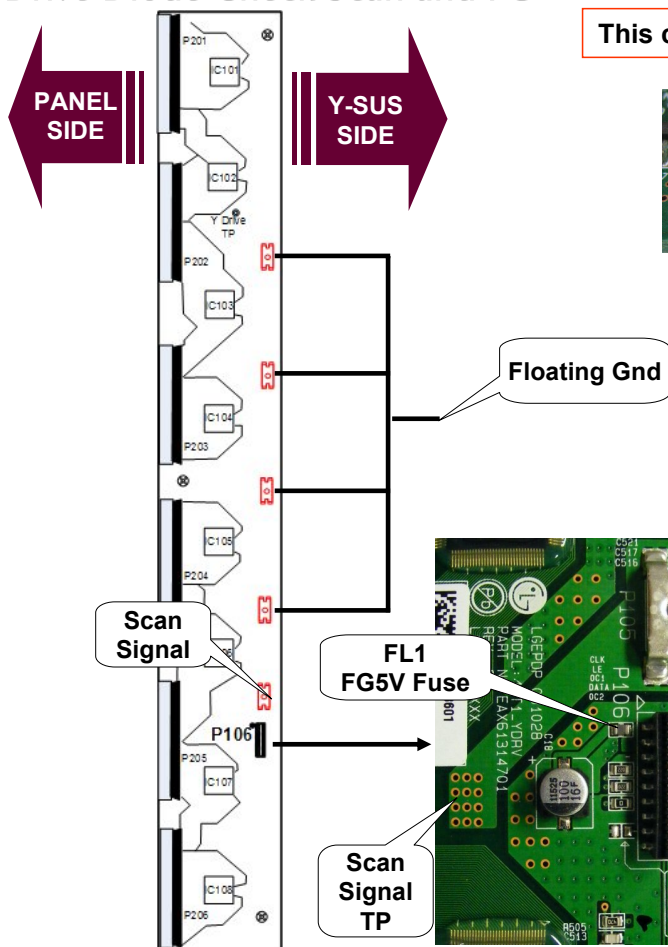
The Y-Drive board operates from Floating Ground, (no reference to Chassis Gnd).

Floating Gnd 5V can be measured across C18 or C523 surface mount electrolytic capacitors.

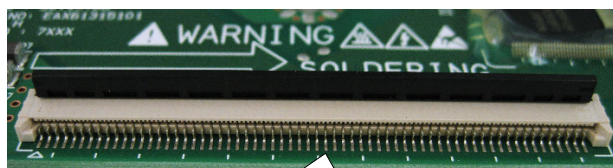
Y-Drive Layout



Y-Drive Diode Check Scan and FG



This checks the output Buffers.



Any Connector to the Panel
(Buffer Output TP)

Diode Mode Reading from Floating Ground

Scan Signal TP

Open with Red Lead on Scan
0.68V with Black Lead on Scan

FG5V TP (P106 pins 2 and 3)

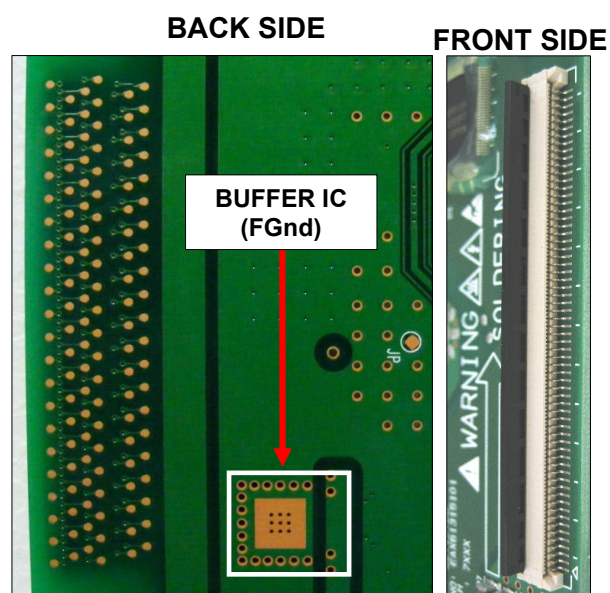
2.57V with Red Lead on Scan
0.53V with Black Lead on Scan

Any Output Buffer TP

Open with Red Lead on Scan
0.80V with Black Lead on Scan

Y-Drive Buffer Troubleshooting

YOU CAN CHECK FOR A SHORTED BUFFER ICs OUTPUT USING THIS PROCEDURE



Using the “Diode Test” on the DVM, check the pins for shorts or abnormal loads.



**RED LEAD On
Floating Ground**

Indicated by white outline



**BLACK LEAD On “ANY”
Output Lug Reads 0.80V**



**BLACK LEAD On
Floating Ground**

Indicated by white outline



**RED LEAD On “ANY”
Output Lug Reads Open**

Any of these output lugs can be checked from floating ground. Look for shorts indicating a defective Buffer IC

6 Ribbon cables communicating with the Panel's (Horizontal Electrodes) totaling 768 lines determining the Panel's Vertical resolution pixel count.

Removing (Panel) Flexible Ribbon Cables from Y-Drive Upper or Lower

Flexible Ribbon Cables shown are from a different model, but process is the same.

To remove the Ribbon Cable from the connector first carefully lift the Locking Tab from the back and tilt it forward (lift from under the tab as shown in Fig 1).

The locking tab must be standing straight up as shown in Fig 2.

Lift up the entire Ribbon Cable gently to release the Tabs on each end. (See Fig 3)

Gently slide the Ribbon Cable free from the connector.

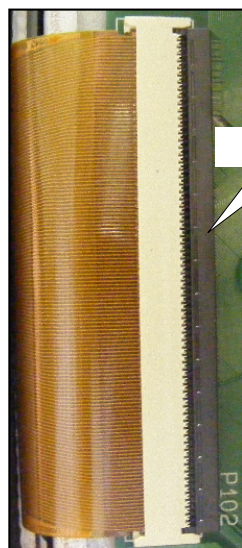


Fig 1

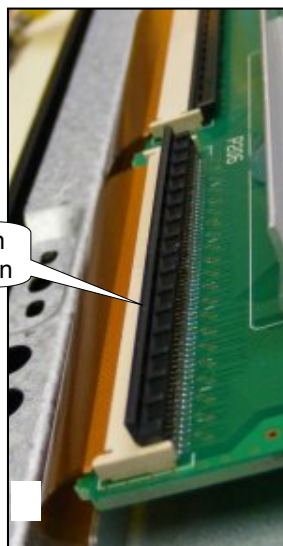


Fig 2

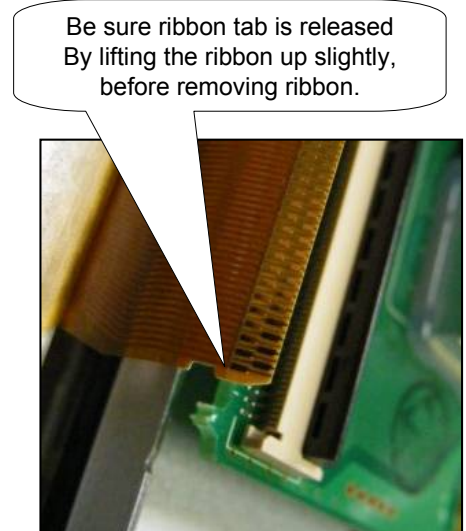


Fig 3

To reinstall the Ribbon Cable, carefully slide it back into the slot see (Fig 3), be sure the Tab is seated securely and press the Locking Tab back to the locked position see (Fig 2 then Fig 1).

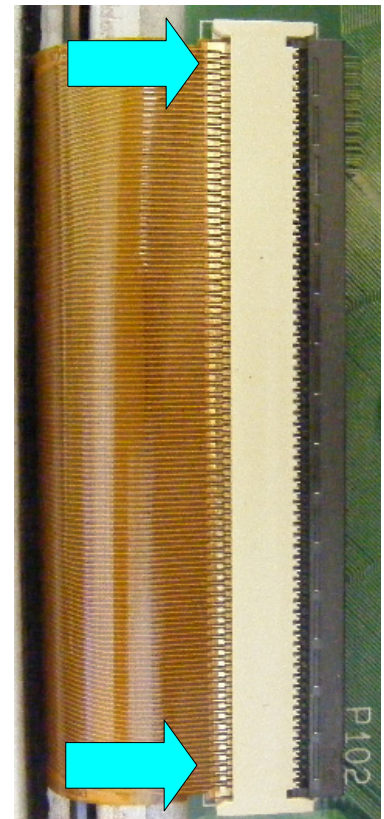
Incorrectly Seated Y-Drive Flexible Ribbon Cables

The Ribbon Cable is clearly improperly seated into the connector. You can tell by observing the line of the connector compared to the FPC, they should be parallel.

The Locking Tab will offer a greater resistance to closing in the case.

Note the cable is crooked. In this case the Tab on the Ribbon cable was improperly seated at the top. This can cause bars, lines, intermittent lines abnormalities in the picture.

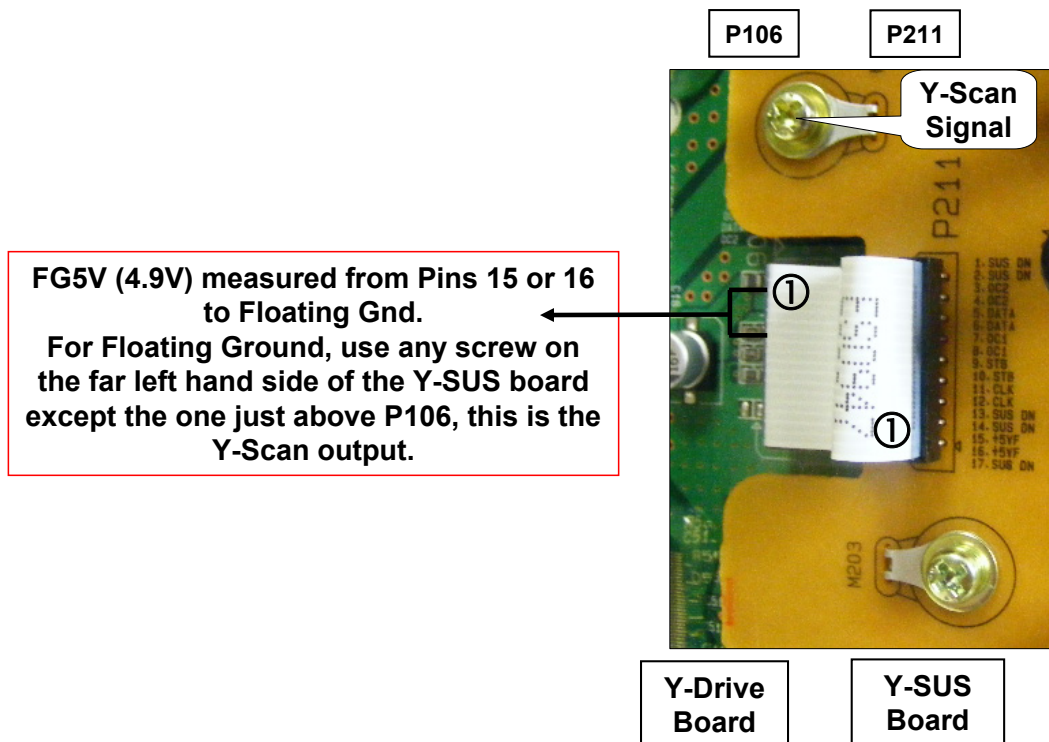
Remove the ribbon cable and re-seat it correctly.



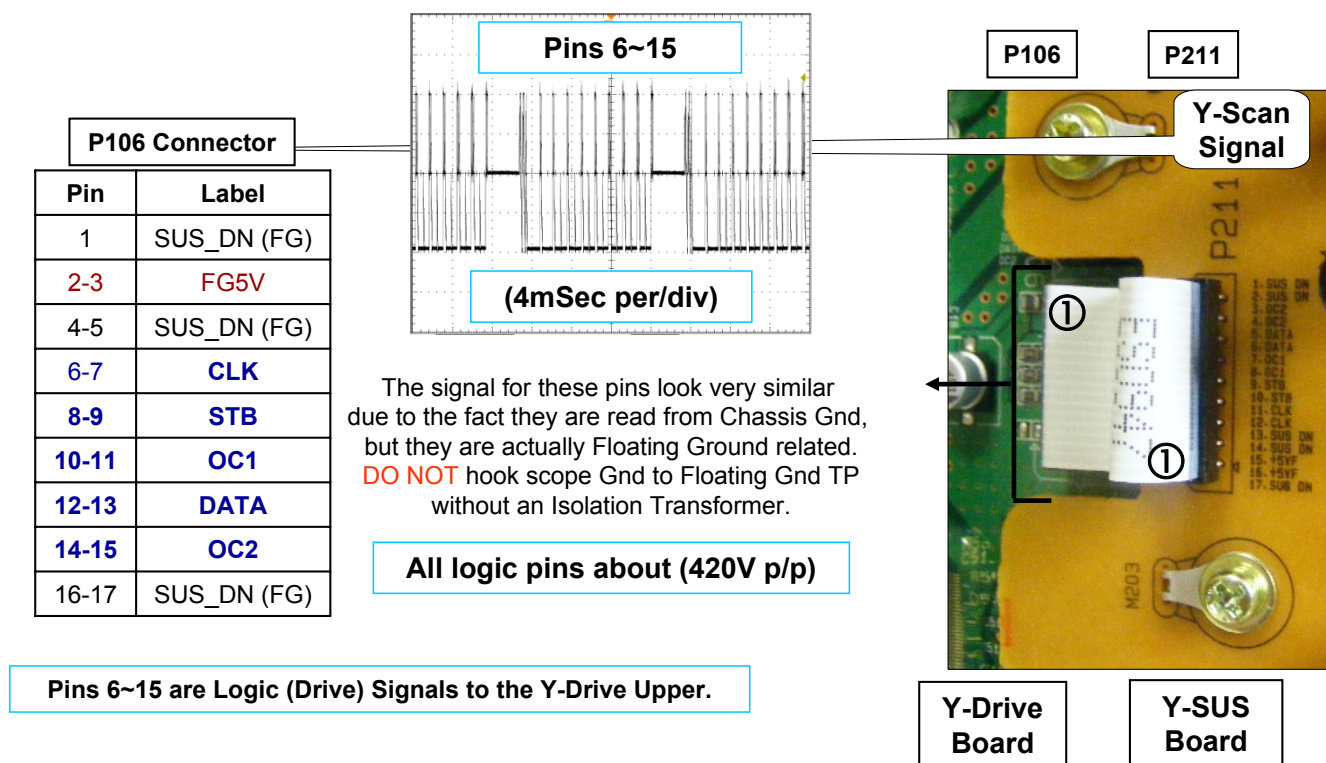
Y-Drive Board P106 Connector to P211 Y-SUS (Logic and FG5V)

TIP: This Connector does not come with a new Y-SUS or Y-Drive.

TIP: Use Scan Screw Lug on the Y-SUS to test for Y-Scan signal if the Y-Drive board is removed.



Y-Drive P106 to Y-SUS Board P211 Logic Signals Explained



Y-Drive P106 Connector Diode Mode Testing

Measurements taken from Floating Gnd.
For Floating Ground, use any screw Lug on the far right hand side of the Y-Drive board except the one just above P106, this is the Y-Scan output.



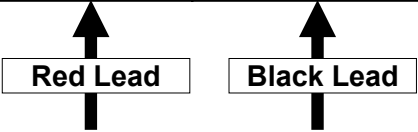
Y-Drive Board

Y-SUS Board should be disconnected for the Diode Mode test.

P106 "Y-Drive" to "Y-SUS" P211

Red Lead on FG

Pin	Label	Run	Diode Check	Diode Check
1	SUS_DN (FG)	FG	FG	FG
2-3	FG5V	4.9V	2.57V	0.53V
4-5	SUS_DN (FG)	FG	FG	FG
6-7	CLK	0.86V	Open	0.62V
8-9	STB	2.8V	Open	0.62V
10-11	OC1	2.2V	Open	0.62V
12-13	DATA	0V	3.28V	0.76V
14-15	OC2	2.63V	Open	0.62V
16-17	SUS_DN (FG)	FG	FG	FG



Diode Mode Readings taken with all connectors Disconnected.
DVM in Diode Mode.

Z-SUS SECTION

This Section of the Presentation will cover troubleshooting the Z-SUS Board Assembly. Upon completion of this section the Technician will have a better understanding of the circuit and be able to locate voltage and diode mode test points needed for troubleshooting and all alignments.

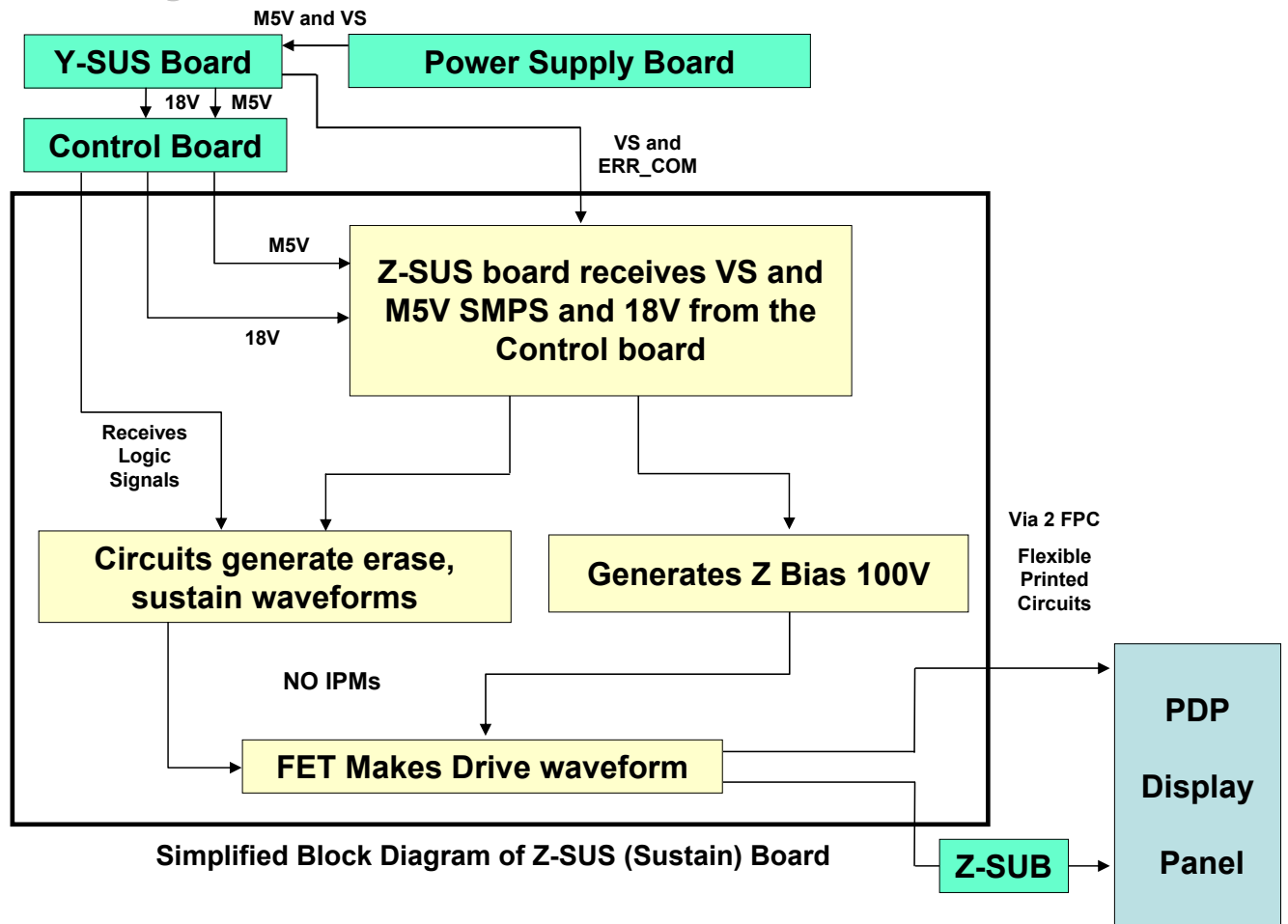
Note: The Z-SUS can not be run “Stand-Alone” in the 42T1 Panel Models.

- Locations
- DC Voltage and Waveform Test Points
 - Z BIAS Alignment
 - Diode Mode Test Points

Operating Voltages

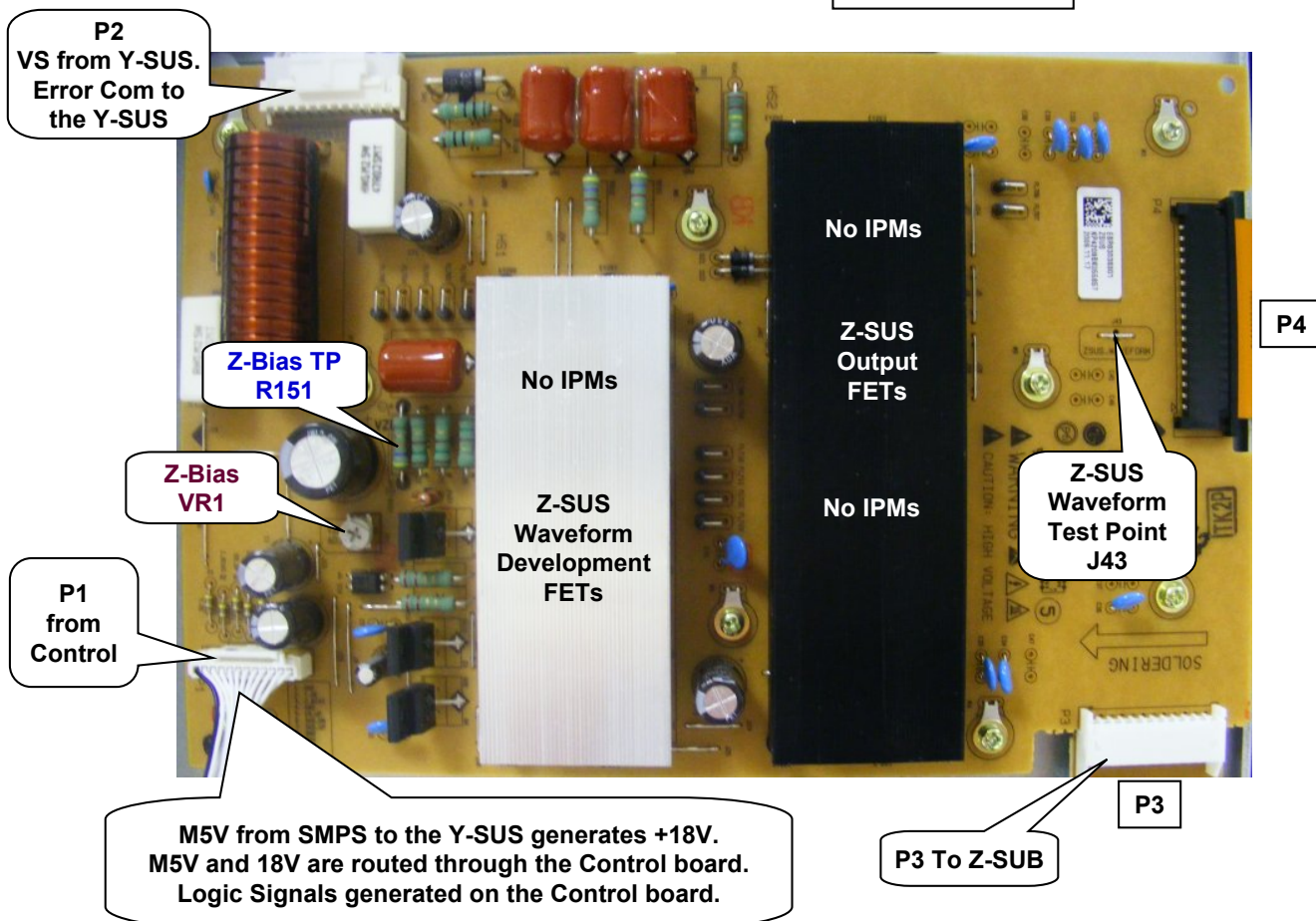
<u>Power Supply Supplied</u>	VS M5V <u>Routed through Control Board</u>
<u>Y-SUS Supplied</u>	18V <u>Routed through Control Board</u>
<u>Developed on Z-SUS</u>	Z Bias

Z-SUS Block Diagram



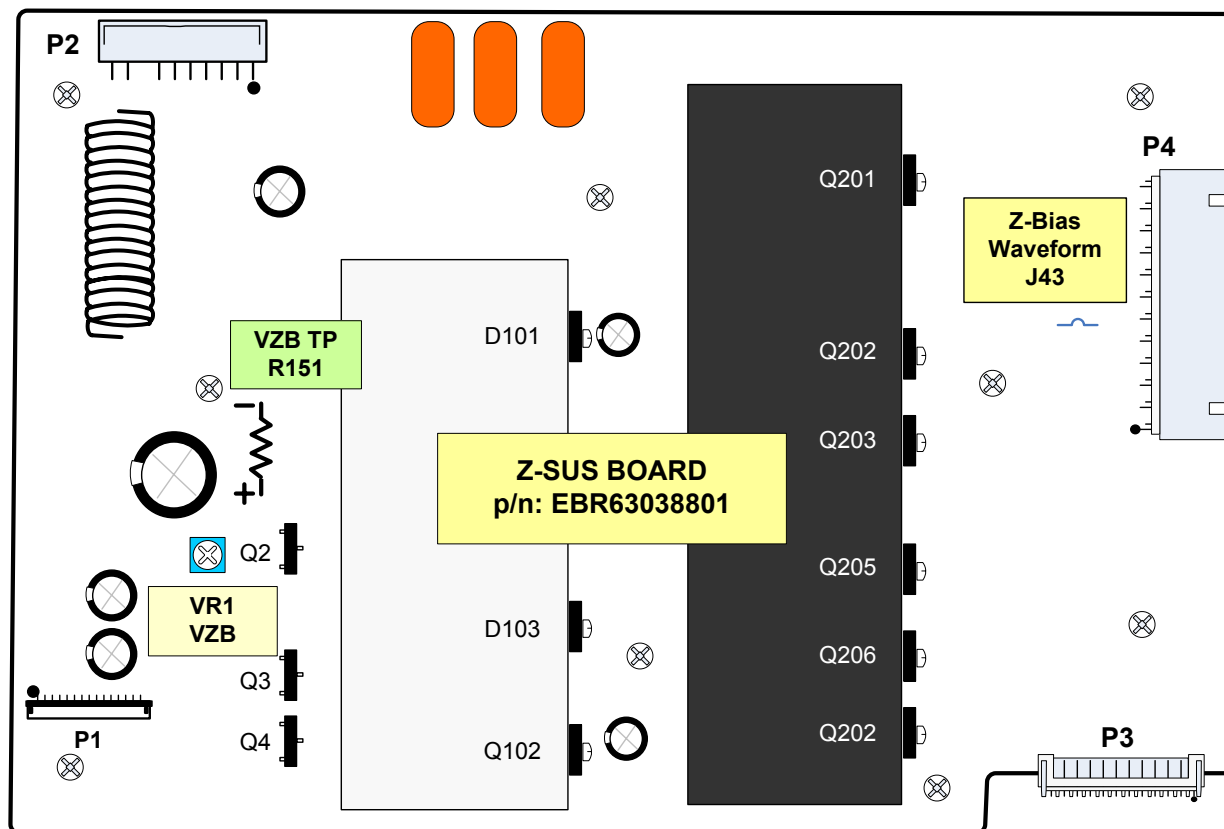
Z-SUS Board Component Identification

P/N EBR63038801



42PJ350 Z-SUS Layout Drawing

1~2 (VS), 4~7 (ER_COM 133V RMS)

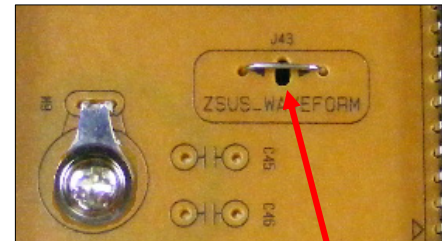
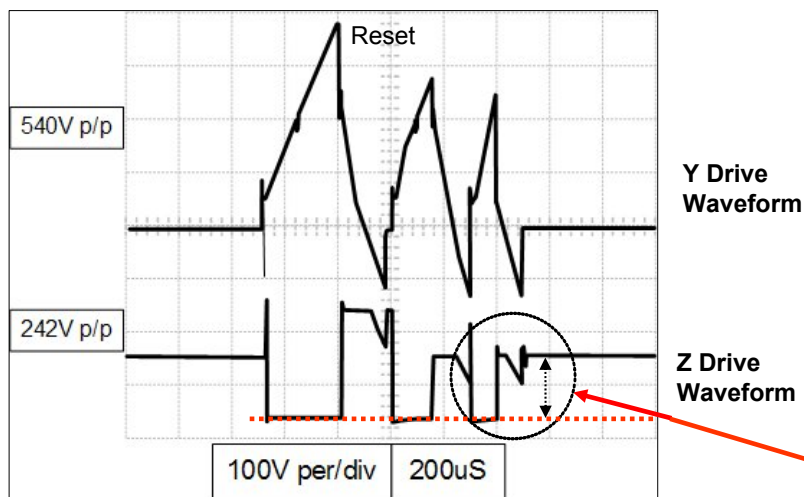


11~12 (18V) 9~10 (M5V)

Z-SUS Waveform

The Z-SUS (in combination with the Y-SUS) generates a SUSTAIN Signal and an ERASE PULSE for generating SUSTAIN and DISCHARGE in the Panel.

This waveform is supplied to the panel through two FPC (Flexible Printed Circuit) connections P4 and to the Z-SUB P3 to P2 and to P1.



Oscilloscope Connection Point.
J43 to check Z Output waveform.
Right Hand Side Center.

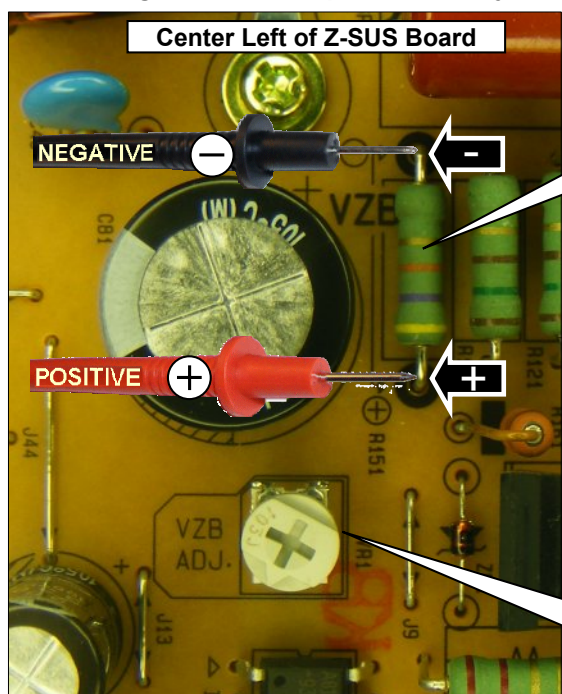
(Vzb) Z Bias VR1 manipulates the offset of this waveform segment.
Vzb voltage 110V \pm 1V

**TIP: The Z-Bias (VZB) Adjustment is a DC level adjustment.
This is only to show the effects of Z-Bias on the waveform.**

This Waveform is just for reference to observe the effects of Zbz adjustment

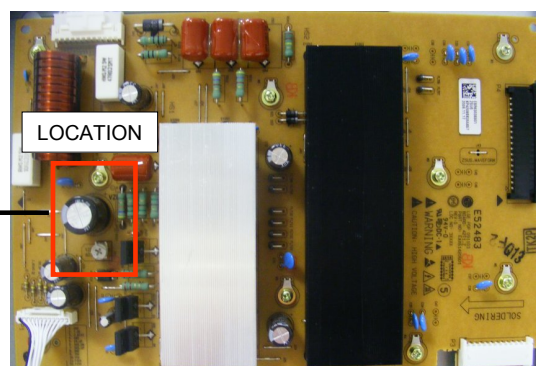
VZB (Z-Bias) VR1 Adjustment

Read the Voltage Label on the panel when adjusting



Model : PDP 42T1###
 Voltage Setting: 5V/ ~~Va:60~~ Vs:205
 N.A. / -195 / 145 / N.A. / 110
 Max Watt : 250 W (Full White)

VZB (Z Bias)



Set should run for 15 minutes, this is the "Heat Run" mode.

Set screen to "White Wash" mode or 100 IRE White input.

All SMPS adjustments should have been completed.

1. Place DC Volt meter between VZB TPs.

2. Adjust VZB (Z Bias) VR1 in accordance with your Panel's voltage label.

Connector P2 to Y-SUS P206 Voltages and Diode Checks

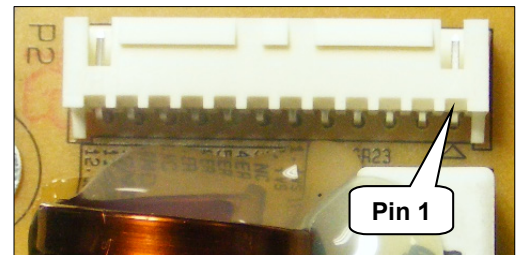
Voltage and Diode Mode Measurements

There are no Stand-By voltages on this connector

P2 "Z-SUS" to "Y-SUS" P206

Pin	Label	Run	Diode Check
1~2	+Vs	*205V	Open
3	n/c	n/c	n/c
4~5	ER_COM	98V~102V	Open
6	n/c	n/c	n/c
7~11	Gnd	Gnd	Gnd

P2 Location: Top Left



* Note: This voltage will vary in accordance with Panel Label

Diode Mode Readings taken with all connectors Disconnected. DVM in Diode Mode.

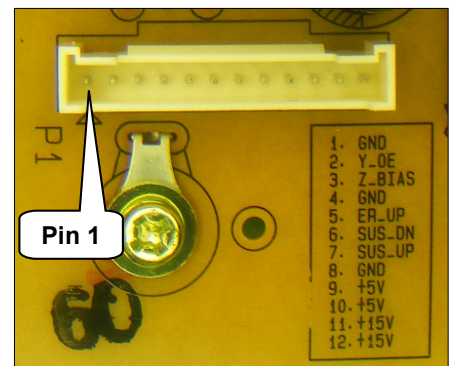
Connector P1 to Control P102 Voltages and Diode Checks

Voltage and Diode Mode Measurements

P1 "Z-SUS Board" to "Control" P102

Pin	Label	Run	Diode Check
1	Gnd	Gnd	Gnd
2	Y-OE	0.0V	Open
3	Z_BIAS	1.9V	2.82V
4	Gnd	Gnd	Gnd
5	ER_UP	0.1V	2.82V
6	ZSUS_DN	0.86V	2.82V
7	ZSUS_UP	0.15V	2.82V
8	Gnd	Gnd	Gnd
9	+5V	5V	Open
10	+5V	5V	Open
11	+15V	18.24V	1.9V
12	+15V	18.24V	1.9V

P1 Location:
Bottom Left hand side



There are no Stand-By voltages on this connector

Diode Mode Readings taken with all connectors Disconnected. DVM in Diode Mode.

CONTROL BOARD SECTION

This Section of the Presentation will cover troubleshooting the Control Board Assembly. Upon completion of this section the Technician will have a better understanding of the circuit and be able to locate voltage and diode mode test points needed for troubleshooting.

- DC Voltage and Waveform Test Points
- Diode Mode Test Points

Signals

Main Board Supplied Panel Control and LVDS (Video) Signals

Control Board Generated Y-SUS and Z-SUS Drive Signals (Sustain)
X Board Drive Signals (RGB Address)

Operating Voltages

From the Y-SUS Supplied +5V (M5V) Developed on the SMPS
+18V (Routed through the Control board to the Z-SUS)
(Not used by the Control Board)

Developed on the Control Board +1.8V for internal use
+3.3V for internal use
+3.3V for the X-Boards (TCPs)



Control Board Pictorial

p/n: EBR63632301

n/c (For ROM Updates)

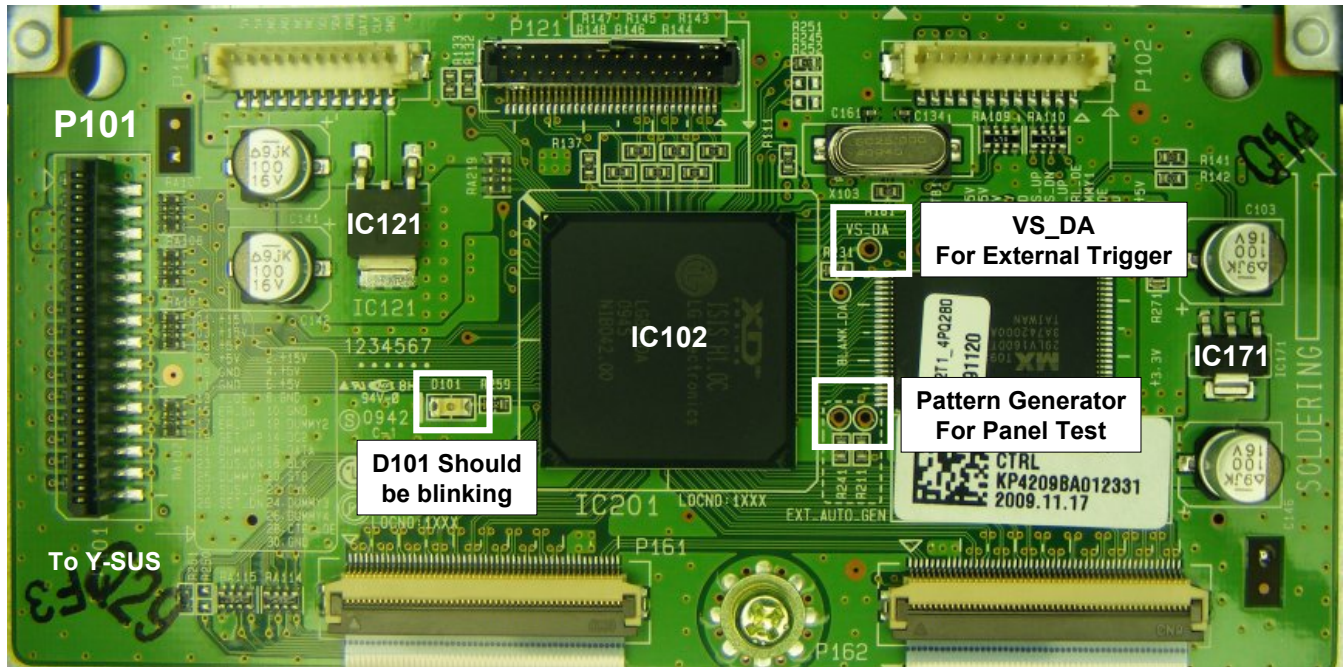
LVDS

To Z-SUS

P163

P121

P102



P161

To X-Left

P162

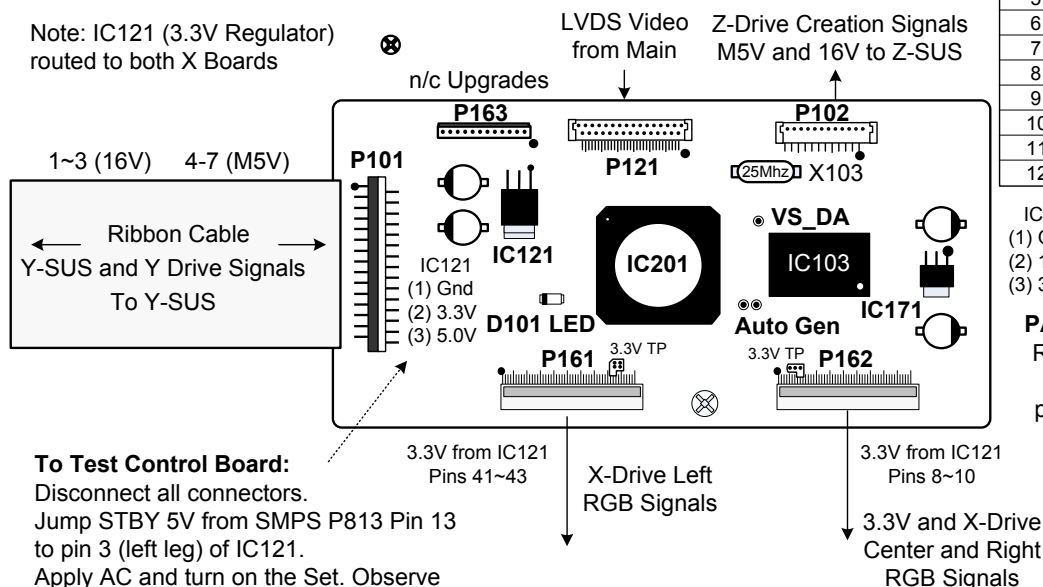
To X-Right

Control Board Component Identification and Checks

With the unit on, if D101 is not on, check 5V supply from FS201 on the Y-SUS.
Pins 4~7 of P101. If present replace the Control Board. If missing, see (To Test Control Board)

CONTROL BOARD
p/n: EBR63632301

Note: IC121 (3.3V Regulator) routed to both X Boards



To Test Control Board:
Disconnect all connectors.
Jump STBY 5V from SMPS P813 Pin 13 to pin 3 (left leg) of IC121.
Apply AC and turn on the Set. Observe Control board LED D101, if it's on, most likely Control board is OK.

* If the complaint is no video and shorting the points (AutoGen) causes video to appear suspect the Main board or LVDS cable.
Note: LVDS Cable must be removed for Auto Gen to work.

P102 "Control" to "Z-SUS Board" P1

Pin	Label	Run	Diode
1	Gnd	Gnd	Gnd
2	Y_OE	0.0V	Open
3	Dummy_1	1.9V	Open
4	CTL_OE	0.0V	Open
5	ER_UP	0.1V	Open
6	SUS_DN	0.86V	Open
7	ZSUS_UP	0.15V	Open
8	Gnd	Gnd	Gnd
9	(+5V)	5V	1.47V
10	(+5V)	5V	1.47V
11	(+15V)	18V	Open
12	(+15V)	18V	Open

IC171
(1) Gnd
(2) 1.2V
(3) 3.3V

18V generated by D506 on Y-SUS

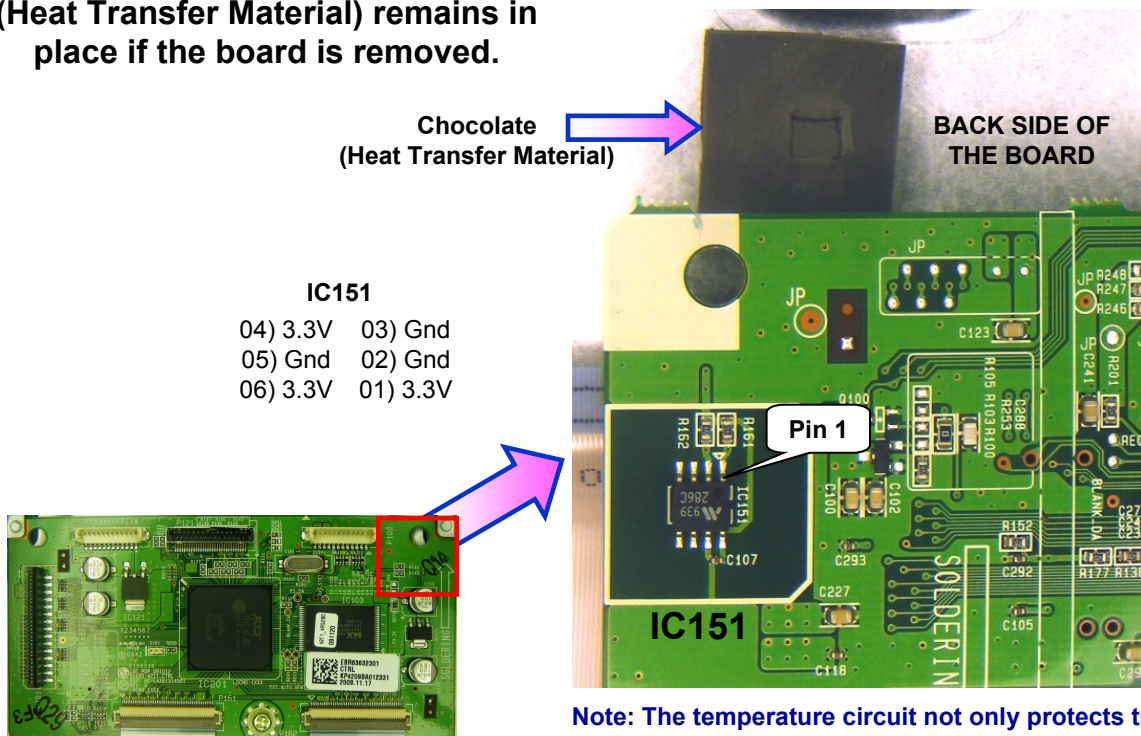
PANEL TEST: Disconnect P121 and Remove LVDS Cable. Short across Auto Gen TPs to generate a test pattern when A/C power is applied.

IC121 Diode Check Pin 2 (3.3V)
TCPs In
0.6V Red Lead
0.39V Blk Lead
All Connectors Removed
0.64V Red Lead
0.40V Blk Lead

IC171 Diode Check Pin 2 (1.2V)
All Connectors Removed
0.32V Red Lead
0.32V Blk Lead

Control Board Temperature Sensor Location (Chocolate)

Make sure the Chocolate
(Heat Transfer Material) remains in
place if the board is removed.



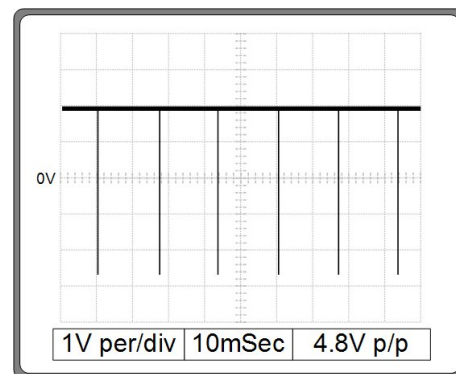
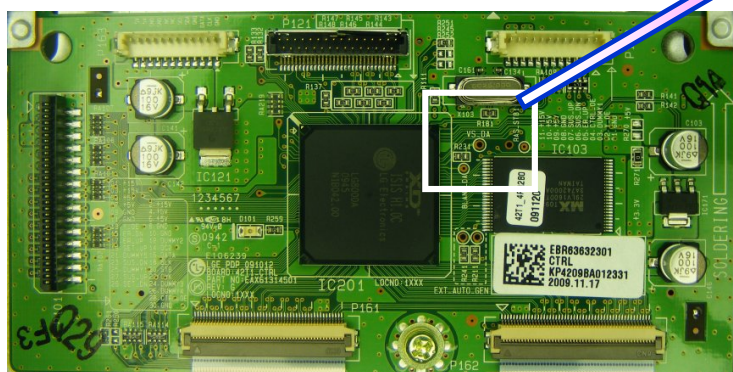
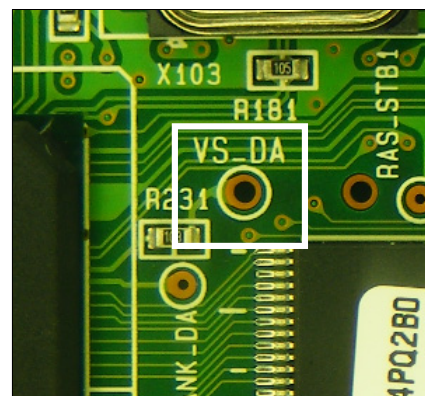
CONTROL BOARD TEMPERATURE
SENSOR LOCATION

Note: The temperature circuit not only protects the panel
from overheating, but it also is responsible for
manipulating the Y-Drive waveform as the panel changes
temperature.

Locking on to the Y-Drive or Z-Drive Waveform Tip

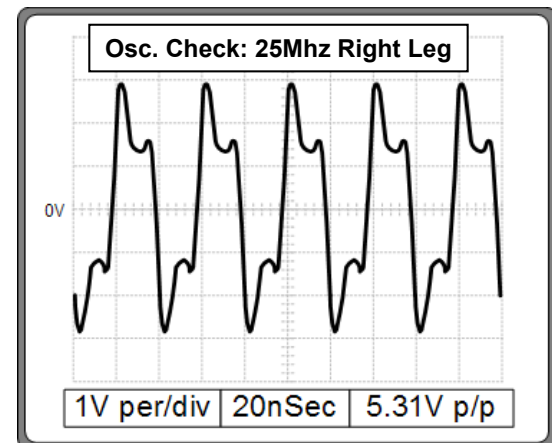
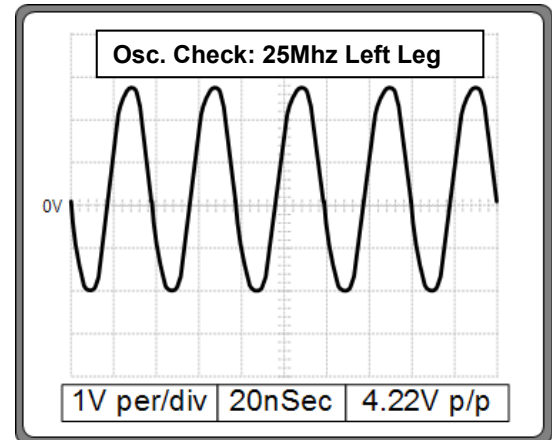
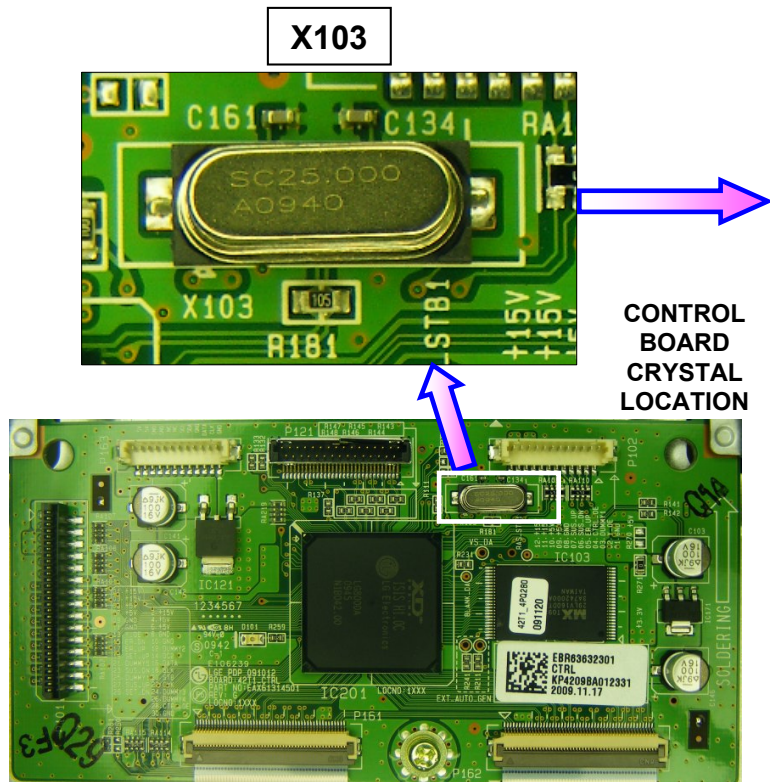
Note, this TP (VS_DA) can be used as an External Trigger for scope when locking onto the Y-Drive (Scan) or the Z-Drive signal.

This signal can also be used to help lock the scope when observing the LVDS video signals.



Checking the Crystal X103 "Clock" on the Control Board

Check the output of the Oscillator (Crystal) X103.
The frequency of the sine wave is 25 MHz.
Missing this clock signal will halt operation of the panel drive signals.



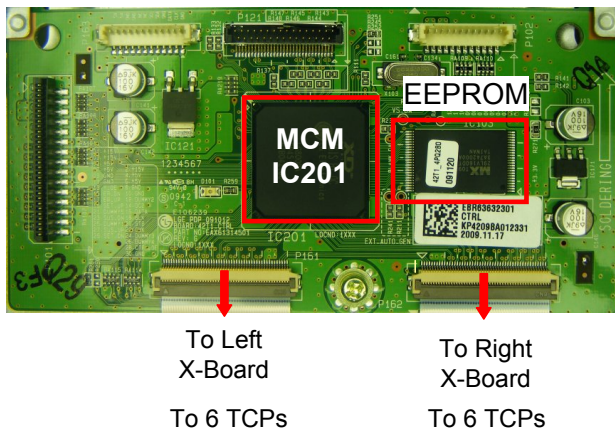
Control Board Signal (Simplified Block Diagram)

The Control Board supplies Video Signals to the TCP (Tape Carrier Package) ICs.

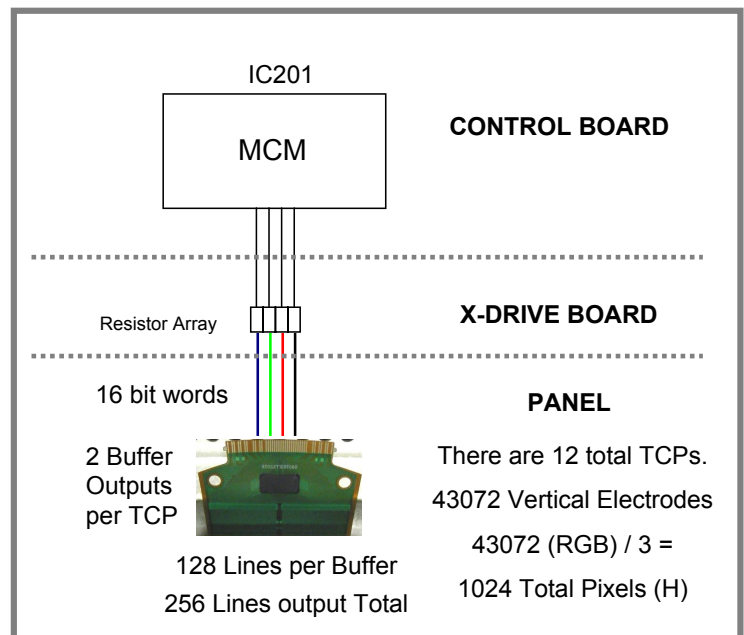
If there is a bar defect on the screen, it could be a Control Board problem.

Control Board to X Board Address Signal Flow

This Picture shows Signal Flow Distribution to help determine the failure depending on where the it shows on the screen.



Basic Diagram of Control Board



Control Board Connector P101 to Y-SUS P101 Voltages and Diode Mode Checks

These pins are very close together. Use Caution when taking Voltage measurements.

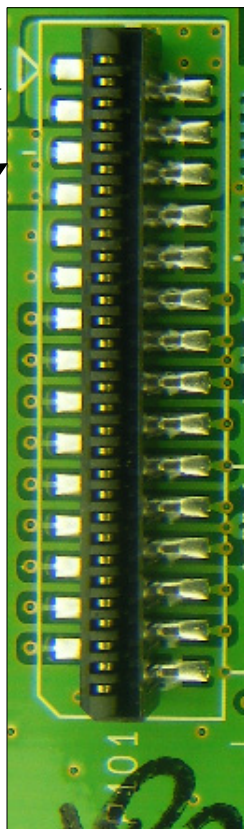
Note: 18V is labeled 15V on silk screen.

Pins 1 through 3
Receive 18V from the Y-SUS.
Developed by D506

Pin ①

Pins 4 through 7
Receive M5V from the Y-SUS.
Protected on Y-SUS by FS201

All the rest are delivering
Y-SUS Waveform development and
Y-Drive logic signals to the Y-SUS
Board (Y-Drive logic signals are simply
routed right through the Y-SUS to the
Y-Drive boards).



P101 Label Silk Screen

01. +15V	2. +15V
03. +15V	4. +15V
05. +5V	6. +5V
07. +5V	8. GND
09. GND	10. GND
11. GND	12. DUMMY2
13. Y_OE	14. OC2
15. ER_DN	16. DATA
17. ER_UP	18. BLK
19. SET_UP	20. STB
21. DUMMY5	22. CLK
23. SUS_DN	24. DUMMY3
25. DUMMY1	26. DUMMY4
27. SUS_UP	28. CTRL_OE
29. SET_DN	30. GND

Note: The +18V is not used by the Control board, it is routed to the Z-SUS leaving on P102 Pins 11~12.

The M5V also leaves on P102 Pins 9~10.

Control P101 to Y-SUS P101 Plug Information

Note: There are no voltages in Stand-By mode

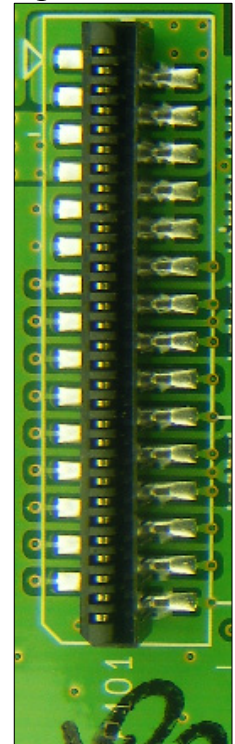
P101 "Control" Odd Pins to P101 "Y-SUS"

Pin	Label	Run	Diode Check
1	+15V	18.24V	Open
3	+15V	18.24V	Open
5	+5V	5V	1.47V
7	+5V	5V	1.47V
9	Gnd	Gnd	Gnd
11	Gnd	Gnd	Gnd
13	Y-OE	0.02V	Open
15	ER_DN	1.05V	2.83V
17	ER_UP	0.26V	2.81V
19	SET_UP	0.24V	2.83V
21	Dummy_5	1.05V	2.81V
23	SUS_DN	2.75V	2.82V
25	Dummy_1	1.04V	2.81V
27	SUS_UP	0.05V	2.82V
29	SET_DN	2.10V	2.82V

P101 "Control" Even Pins to P101 "Y-SUS"

Pin	Label	Run	Diode Check
2	+15V	18.24V	Open
4	+5V	5V	1.47V
6	+5V	5V	1.47V
8	Gnd	Gnd	Gnd
10	Gnd	Gnd	Gnd
12	Dummy_2	2.14V	2.83V
14	OC2	1.85V	Open
16	DATA	0V	2.83V
18	BLK	1.4V	2.82V
20	STB	1.5V	2.82V
22	CLK	0.59V	2.82V
24	Dummy_3	1.97V	2.82V
26	Dummy_4	1.23V	Open
28	CTL_OE	0.23V	Open
30	Gnd	Gnd	Gnd

Pin ①

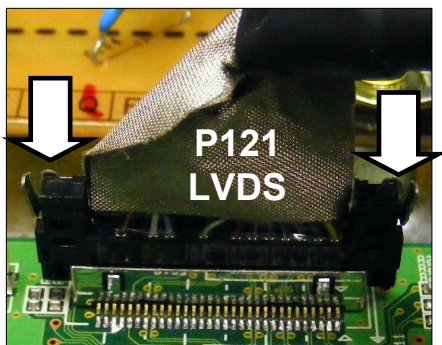


P101

Diode Mode Readings taken with all connectors Disconnected. Black lead on Gnd. DVM in Diode Mode.

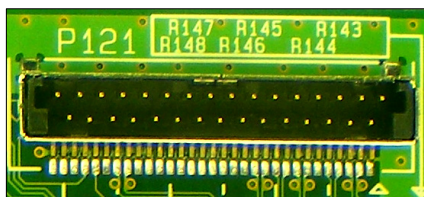
Control Board LVDS P121 Signals

LVDS Cable P121 on Control board shown.
Press two outside tabs inward to release.



LVDS

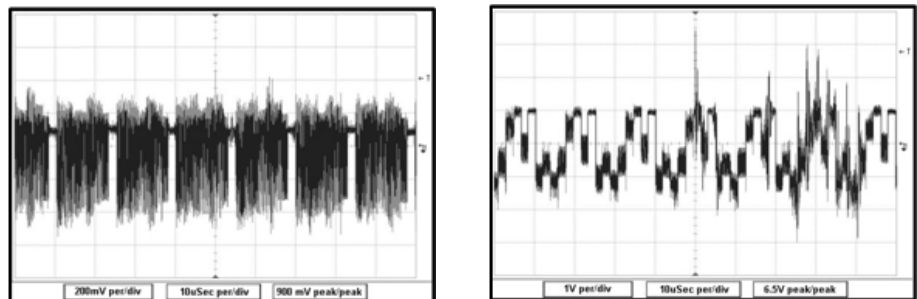
LVDS Removed



Pins are close together,
Use caution.

Video Signals from the Main Board to the Control Board are referred to as Low Voltage Differential Signals or LVDS. The video is delivered in 10 bit LVDS format. Their presence can be confirmed with the Oscilloscope by monitoring the LVDS signals with SMPTE Color Bar input. Loss of these Signals would confirm the failure is on the Main Board or the LVDS Cable itself.

Example of LVDS Video Signal



Example of Normal Signals measured at 1V p/p at 10 μ Sec

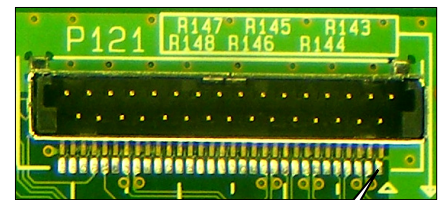
Pins 2~5, 7~8, 11~12, 24~25 are LVDS Video Signals.
Pins 9~10 and 22~23 are clock signals for the data.

Control Board LVDS P121 Connector Voltages and Diode Check

P121 Connector "Control Board" to "Main "P703"

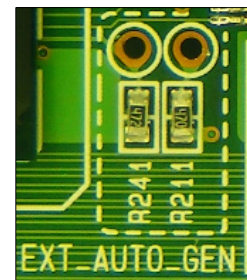
Pin	Label	Run	Diode Check
1	n/c	n/c	Gnd
2	RA1N	1.13V	1.23V
3	RA1P	1.37V	1.23V
4	RB1N	1.18V	1.23V
5	RB1P	1.31V	1.23V
6	Gnd	Gnd	Gnd
7	RC1N	1.27V	1.23V
8	RC1P	1.23V	1.23V
9	RCLK1N	1.29V	1.23V
10	RCLK1P	1.26V	1.23V
11	RD1N	1.23V	1.23V
12	RD1P	1.31V	1.23V
13	Gnd	Gnd	Gnd
14	Gnd	Gnd	Gnd
15	n/c	n/c	Open

Pin	Label	Run	Diode Check
16	n/c	n/c	Open
17	n/c	n/c	Open
18	n/c	n/c	Open
19	Gnd	Gnd	Gnd
20	n/c	n/c	Open
21	n/c	n/c	Open
22	CLK	0.59V	2.99V
23	DATA	3.24V	2.99V
24	RE1N	1.19V	1.23V
25	RE1P	1.29V	1.23V
26	Gnd	Gnd	Gnd
27	DISP_EN	2.79V	Open
28	Module_SDA1	3.29V	Open
29	Module_SCL1	3.29V	Open
30	n/c	n/c	Open
31	Gnd	Gnd	Gnd



Pin 27 is the reason the LVDS cable must be removed to use the EX_AUTO_GEN shorting pins to create multiple internal generated test patterns (Panel Test).

Enables the Control Board



Blue Pins indicate 10 bit differential video signal

Note: There are no voltages in Stand-By mode.

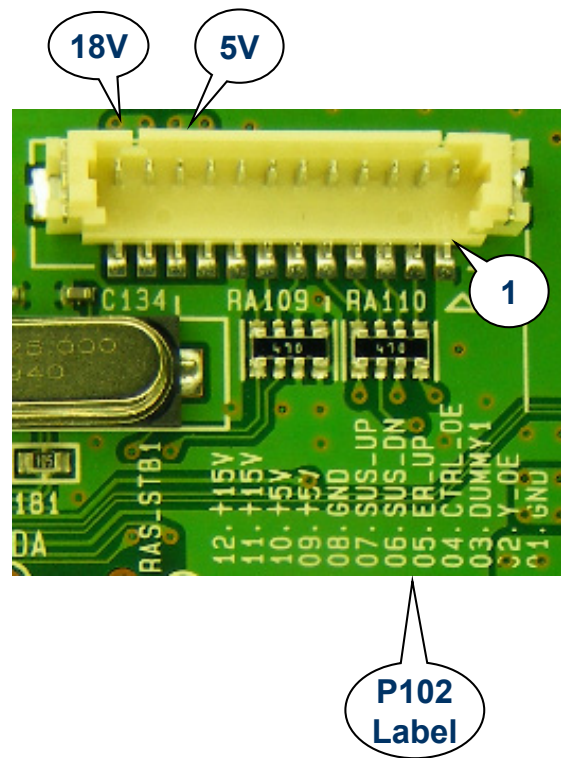
Control Board P102 Connector Pin ID and Voltages

Voltage and Diode Mode Measurements for the Control Board.

Note: There are no voltages in Stand-By mode.

P102 Connector "Control" to "Z-SUS Board" P1

Pin	Label	Run	Diode Check
1	Gnd	Gnd	Gnd
2	Y-OE	0.0V	Open
3	Dummy-1	1.9V	Open
4	CTL_OE	0.0V	Open
5	ER_UP	0.1V	Open
6	SUS_DN	0.86V	Open
7	SUS_UP	0.15V	Open
8	Gnd	Gnd	Gnd
9	+5V	5V	1.47V
10	+5V	5V	1.47V
11	+15V	18.24V	Open
12	+15V	18.24V	Open



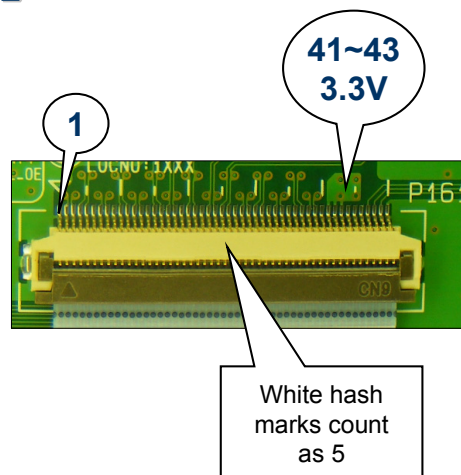
Diode Mode Readings taken with all connectors Disconnected. Black lead on Gnd. DVM in Diode Mode.

P161 Connector "Control Board" to "Left X Board" P232

P161 Connector to the Center X-Board P231

Pin	Label	Run	Diode Check
1	Gnd	Gnd	Gnd
2	A2_P_0	1.12V	1.35V
3	A2_N_0	1.18V	1.31V
4	A1_P_0	1.12V	1.35V
5	A1_N_0	1.18V	1.31V
6	Gnd	Gnd	Gnd
7	CLK_P_0	1.12V	1.35V
8	CLK_N_0	1.18V	1.31V
9	Gnd	Gnd	Gnd
10	A2_P_1	1.12V	1.35V
11	A2_N_1	1.18V	1.31V
12	A1_P_1	1.12V	1.35V
13	A1_N_1	1.18V	1.31V
14	Gnd	Gnd	Gnd
15	A2_P_2	1.12V	1.35V
16	A2_N_2	1.18V	1.31V
17	A1_P_2	1.12V	1.35V
18	A1_N_2	1.18V	1.31V
19	Gnd	Gnd	Gnd
20	CLK_P_1	1.12V	1.35V
21	CLK_N_1	1.18V	1.31V
22	Gnd	Gnd	Gnd
23	A2_P_3	1.12V	1.35V
24	A2_N_3	1.18V	1.31V
25	A1_P_3	1.12V	1.35V

Pin	Label	Run	Diode Check
26	A1_N_3	1.18V	1.31V
27	Gnd	Gnd	Gnd
28	A2_P_4	1.12V	1.35V
29	A2_N_4	1.18V	1.31V
30	A1_P_4	1.12V	1.35V
31	A1_N_4	1.18V	1.31V
32	Gnd	Gnd	Gnd
33	CLK_P_2	1.12V	1.35V
34	CLK_N_2	1.18V	1.31V
35	Gnd	Gnd	Gnd
36	A2_P_5	1.12V	1.35V
37	A2_N_5	1.18V	1.31V
38	A1_P_5	1.12V	1.35V
39	A1_N_5	1.18V	1.31V
40	Gnd	Gnd	Gnd
41	3.3V	3.3V	0.64V
42	3.3V	3.3V	0.64V
43	3.3V	3.3V	0.64V
44	Gnd	Gnd	Gnd
45	STB0	3.24V	Open
46	STB1	3.27V	Open
47	X_BLK	3.24V	Open
48	X_POL	1.86V	Open
49	HTZ	0V	Open
50	Gnd	Gnd	Gnd

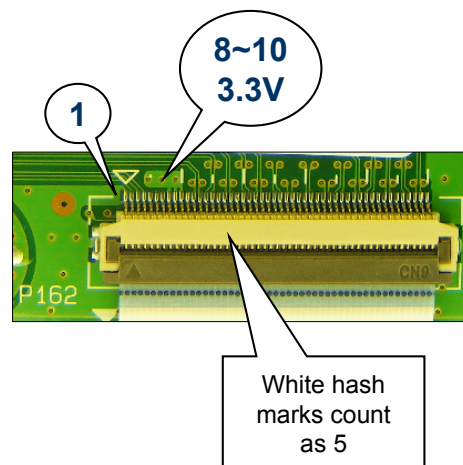


P162 Connector "Control Board" to "Left X Board" P331

P162 Connector to the Center X-Board P331

Pin	Label	Run	Diode Check
1	Gnd	Gnd	Gnd
2	HTZ	0V	Open
3	X_POL	1.86V	Open
4	X_BLK	3.24V	Open
5	STB2	3.24V	Open
6	STB3	3.27V	Open
7	Gnd	Gnd	Gnd
8	3.3V	3.3V	0.64V
9	3.3V	3.3V	0.64V
10	3.3V	3.3V	0.64V
11	Gnd	Gnd	Gnd
12	A2_P_6	1.12V	1.35V
13	A2_N_6	1.18V	1.31V
14	A1_P_6	1.12V	1.35V
15	A1_N_6	1.18V	1.31V
16	Gnd	Gnd	Gnd
17	CLK_P_3	1.12V	1.35V
18	CLK_N_3	1.18V	1.31V
19	Gnd	Gnd	Gnd
20	A2_P_7	1.12V	1.35V
21	A2_N_7	1.18V	1.31V
22	A1_P_7	1.12V	1.35V
23	A1_N_7	1.18V	1.31V
24	Gnd	Gnd	Gnd
25	A2_P_8	1.12V	1.35V

Pin	Label	Run	Diode Check
26	A2_N_8	1.18V	1.31V
27	A1_P_8	1.12V	1.35V
28	A1_N_8	1.18V	1.31V
29	Gnd	Gnd	Gnd
30	CLK_P_4	1.12V	1.35V
31	CLK_N_4	1.18V	1.31V
32	Gnd	Gnd	Gnd
33	A2_P_9	1.12V	1.35V
34	A2_N_9	1.18V	1.31V
35	A1_P_9	1.12V	1.35V
36	A1_N_9	1.18V	1.31V
37	Gnd	Gnd	Gnd
38	A2_P_10	1.12V	1.35V
39	A2_N_10	1.18V	1.31V
40	A1_P_10	1.12V	1.35V
41	A1_N_10	1.18V	1.31V
42	Gnd	Gnd	Gnd
43	CLK_P_5	1.12V	1.35V
44	CLK_N_5	1.18V	1.31V
45	Gnd	Gnd	Gnd
46	A2_P_11	1.12V	1.35V
47	A2_N_11	1.18V	1.31V
48	A1_P_11	1.12V	1.35V
49	A1_N_11	1.18V	1.31V
50	Gnd	Gnd	Gnd



X BOARD (LEFT and RIGHT) SECTION

The following section gives detailed information about the X boards. These boards deliver the Color information signal developed on the Control board to the TCPs, (Taped Carrier Packages). The TCPs are attached to the vertical FPCs, (Flexible Printed Circuits) which are attached directly to the panel. The X boards are the attachment points for these FPCs. These boards have no adjustment.

X-BOARD VOLTAGES:

- **VA:** Originally developed on the Switched Mode Power Supply VA (Voltage for Address) is routed through the Y-SUS board, out on P209 pins 4~9 to the Left X-Board via P233 pins 4~5. VA leaves the Left X-Board P211 pins 4~5 and is sent to the Right X-Board via P311 pins 4~5.
- **3.3V:** Control board develops 3.3V (IC121) and routes to the Left X-Board via ribbon connector P232 pins 9~11.
- **3.3V:** Control board develops 3.3V (IC121) and routes to the Right X-Board via ribbon connector P331 pins 42~44.

X Board Additional Information

**There are two X-Boards, the Left and the Right.
(As viewed from the rear of the set).**

The two X-Boards have very little circuitry. They are basically signal and voltage routing boards.

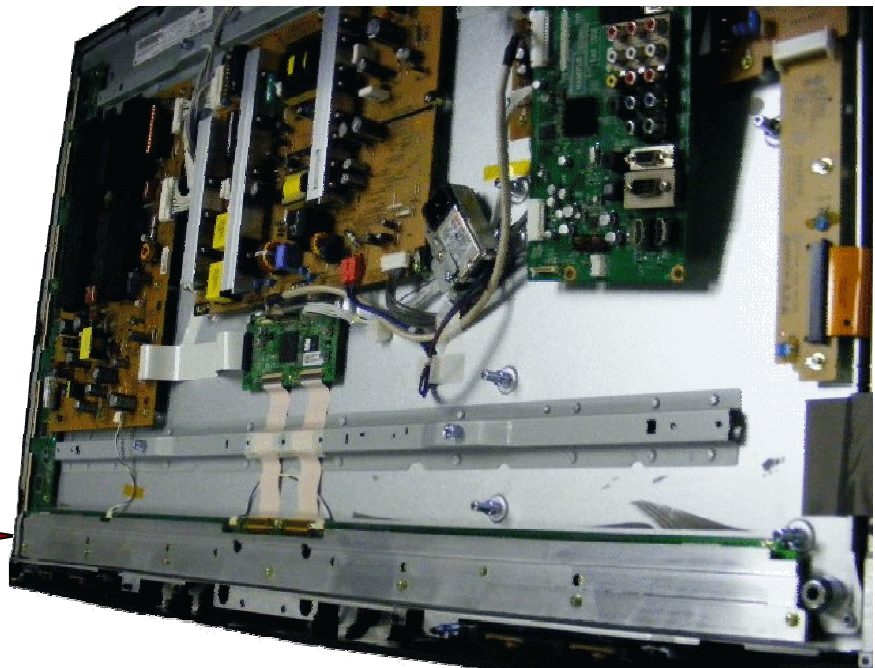
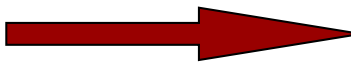
- They route Va voltage to all of the Taped Carrier Packages (TCPs). Va is introduced to the Left X board first, then the Left X-Board sends Va to the Right X-Board.**
- The X-Boards also route the Logic (Color) signals from the Control board to all of the Taped Carrier Packages (TCPs).**
- The X-Boards have connectors to 12 TCPs, 6 on the left and right.**
- There are a total of 12 TCPs and each TCP has 2 gate arrays, so there are a total of 24 buffers feeding the panel's 3072 vertical electrodes.**

X Board TCP Heat Sink Warning

**NEVER run the television with this heat sink removed.
Damage to the TCPs will occur and cause a defective panel.**

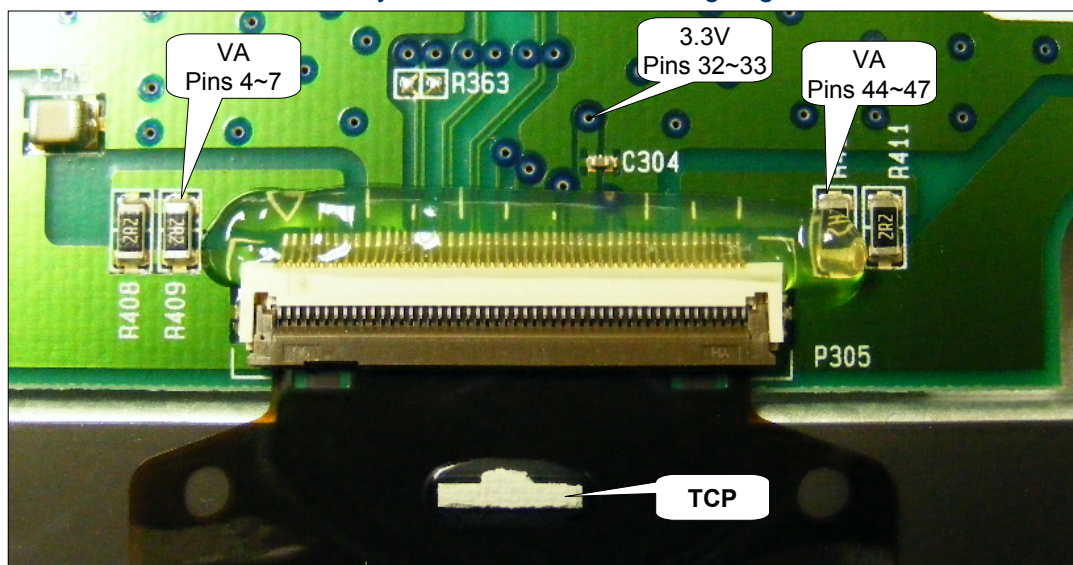
**The Vertical Address
buffers (TCPs) have
one heat sink
indicated by the arrow.**

It protects all 12 TCPs.




X Board Layout Primary Circuit Diode Check

The two X-Boards have similar circuit layouts for the connections going to the TCPs, as shown below.



⊕  On Gnd

⊖  On the below:

On any Va (0.52V) TCPs connected.
On any Va (Open) TCPs disconnected.
On 3.3V (0.39V) TCPs connected.
On 3.3V (Open) TCPs disconnected.

*VA from Y-SUS
disconnected
from Left X board*

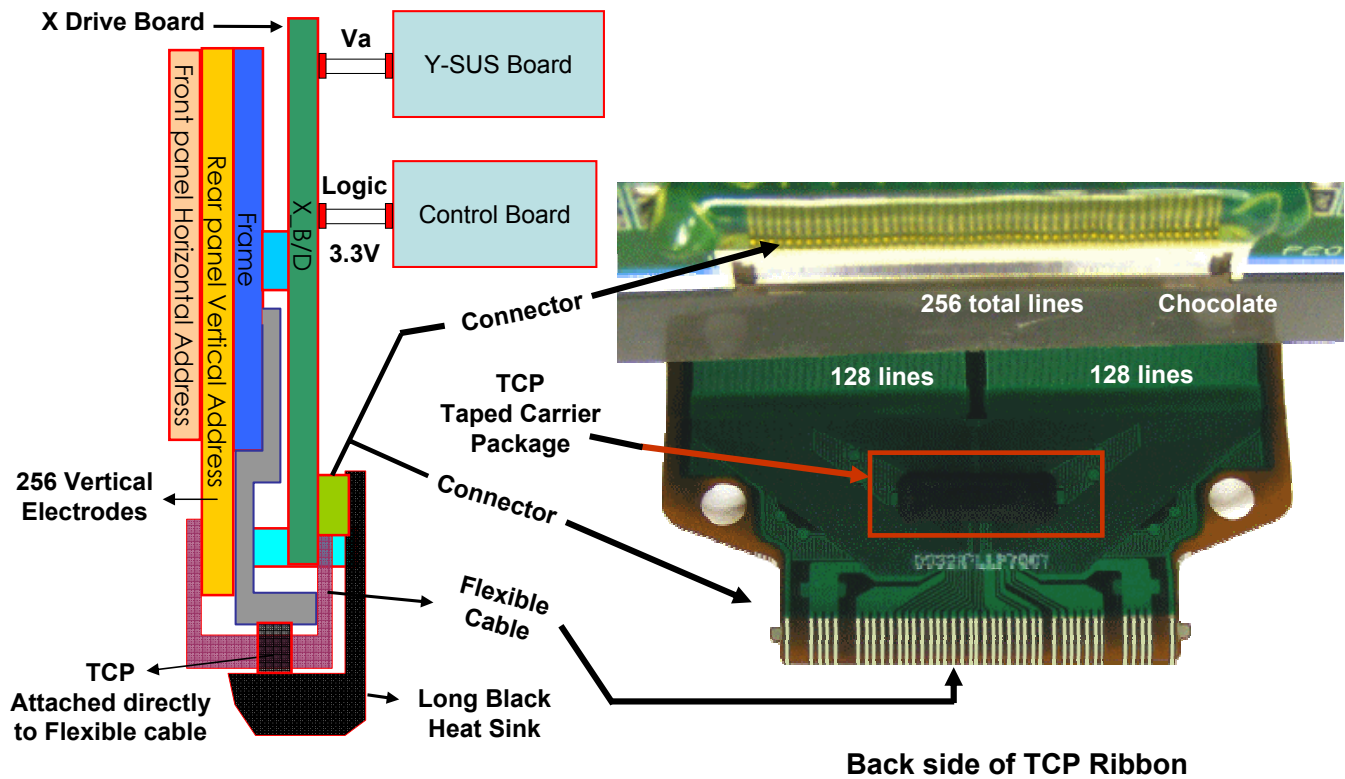
⊖  On Gnd

⊕  On the below:

On any Va (Open) TCPs connected.
On any Va (Open) TCPs disconnected.
On 3.3V (0.6V) TCPs connected.
On 3.3V (Open) TCPs disconnected.

TCP (Tape Carrier Package)

This shows the layout of the bottom ribbon cables connecting to the Panel's Vertical electrodes, (Address Bus). Note that each ribbon cable has a solid state device called a TCP attached.



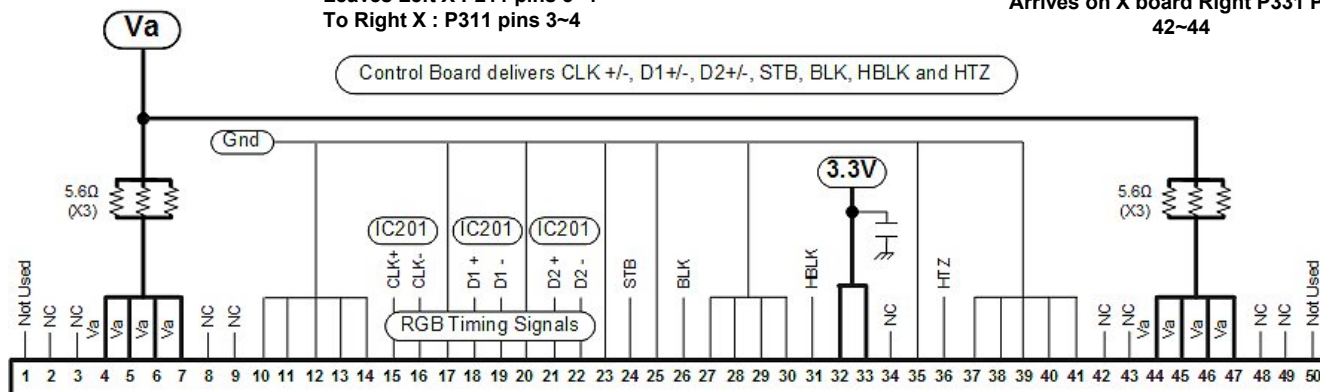
TCP Testing

TCP Connector Pin Description Any X Board to Any TCP P201~P206 or P301~P306

Va: P233 3~4 from Y-SUS P209
Va: Routes to:

Leaves Left X P211 pins 3~4
To Right X : P311 pins 3~4

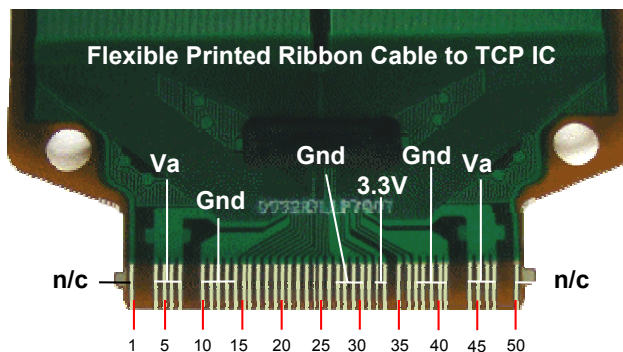
3.3V Origination
From Control board IC121 center leg.
Leaves P161 to P232 and P162 to P331
Arrives on X board Left P232 Pins 9~11
Arrives on X board Right P331 Pins
42~44



Must be checked on flexible cable.

⊕ — On any Gnd
⊖ — On the below:

On Va (0.59V) Reversed
On 3.3V (1.08V) On Va (Open)
 On 3.3V (Open)



Look for any TCPs
being discolored.
Ribbon Damage.
Cracks, folds
Pinches, scratches,
etc...

TCP 3.3V B+ Check

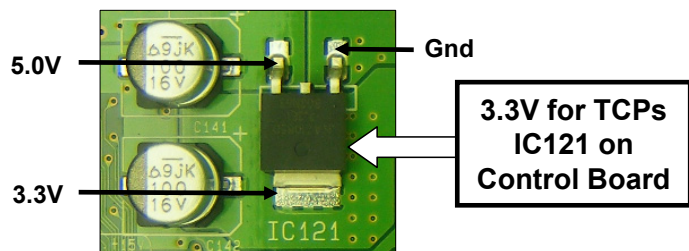
For Connectors P162 on the Control board, see Control board section.

With all connectors connected, place the Red Lead On 3.3V = Diode Check (0.60V)
Black Lead On 3.3V = Diode Check (0.39V)

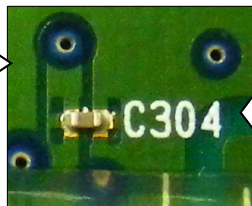
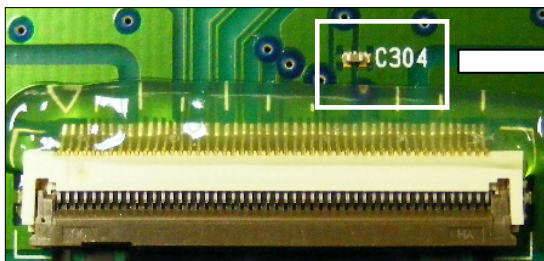
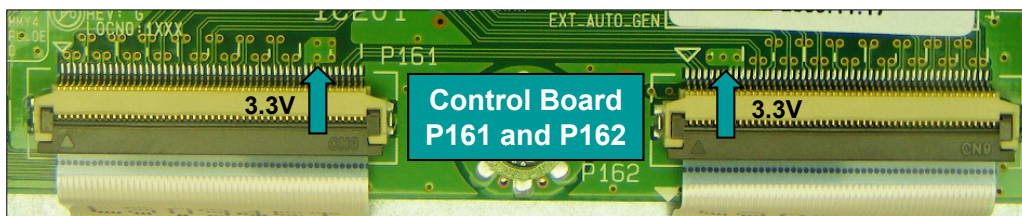
With all connectors removed, place the Red Lead On 3.3V = Diode Check (0.64V)
Black Lead On 3.3V = Diode Check (0.4V)

Warning: DO NOT attempt to run the set with the Heat Sink over the TCPs removed.

Checking IC121 for 3.3V, use center pin or Case of component.



3.3V in on Pins 1 ~ 5 only on P232 connector from the Control board



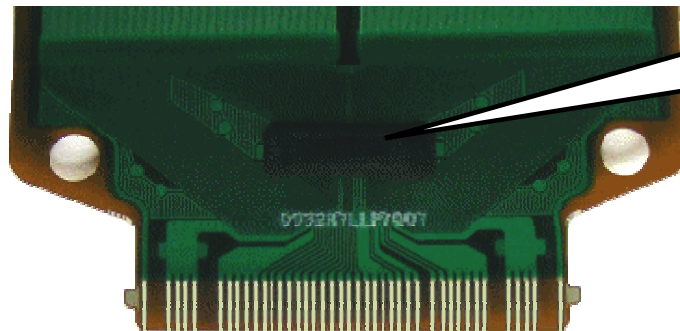
All Connectors to All TCPs look very similar for the 3.3V test point. The trace at pins 32 and 33 of each connector. There is a small feed trough and a Cap, you can use for Test Points. Example here from P305. You can only check for continuity back to IC231, you can not run the set with heat sink removed.

TCP Visual Observation. Damaged TCP

Warning: DO NOT attempt to run the set with the Heat Sink over the TCPs removed. After a very short time, these ICs will begin to self destruct due to overheating.

This damaged TCP can, (at the location of the TCP).

- a) Cause the Power Supply to shutdown. (VA shorted, 3.3V shorted).
- b) Generate abnormal vertical bars, (colored noise).
- c) Cause the entire area driven by the TCP to be "All White" or "ALL BLACK".
- d) Cause a "Single Pixel Width Line" defect. The line can be Red, Green or Blue.
- e) A dirty contact at the connector can cause b, c and d also.



"TCP"
Tapped
Carrier
Package

Look for burns, pin
holes, damage, etc.

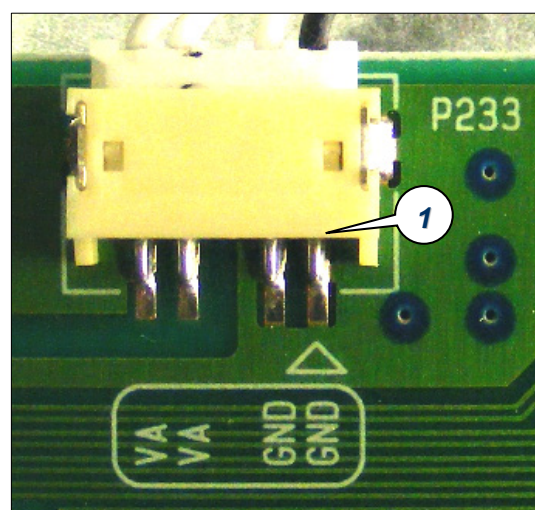
Left X Drive P233 Connector from Y-SUS P209 Information

Voltage and Diode Mode Measurement (No Stand-By Voltages)

P233 "X Drive Left" to "Y-SUS" P209

Pin	Label	Run	Diode Check
1	Gnd	Gnd	Gnd
2	Gnd	Gnd	Gnd
3	n/c	n/a	n/a
4	VA	*60V	Open
5	VA	*60V	Open

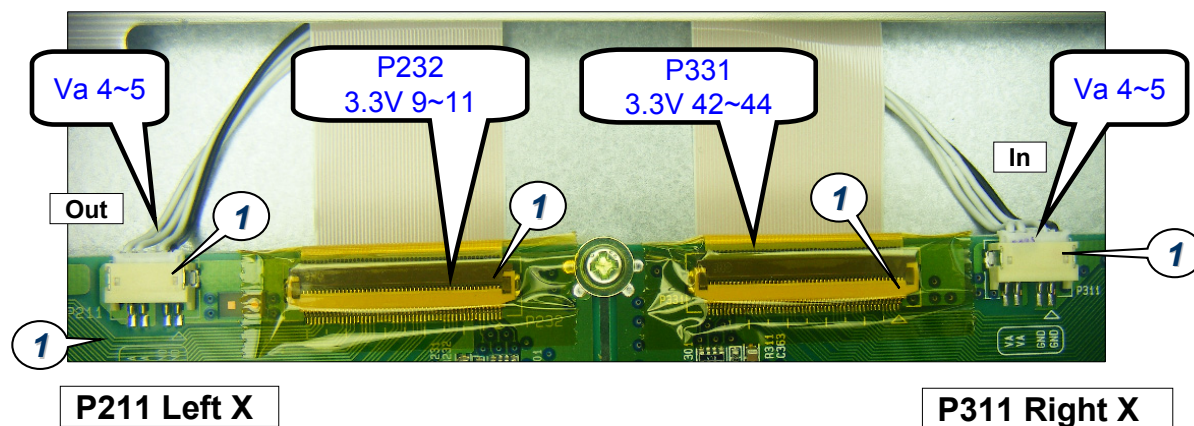
With Heat Sink



*** Note:** This voltage will vary in accordance with Panel Label.
There are no Stand-By voltages on this connector.


Diode Mode Readings taken with all connectors Disconnected. Black lead on Gnd. DVM in Diode Mode.


P211, P232, P311 and P331 X Board Connector (VA Diode Check)



⊖  On Chassis Gnd

⊕  On Chassis Gnd

⊕  On Va (Open) Y-SUS connector removed, TCPs connected.
On Va (Open) all connectors removed, TCPs disconnected.

⊖  On Va (0.52) Y-SUS connector removed, TCPs connected.
On Va (Open) all connectors removed, TCPs disconnected.

MAIN BOARD SECTION

The following section gives detailed information about the Main board. This board contains the Microprocessor, Audio section, video section and all input, outputs. It also receives all input signals and processes them to be delivered to the Control board via the LVDS cable. The main tuner (Silicon Tuner using discrete components) which provides VSB (NTSC), 8VSB (Over the Air Digital Broadcast) and QAM (Cable Digital) is located on the main board. This board is also where the television's software upgrades are accomplished through the USB input. This board has no mechanical adjustments.

The Main Board Receives its operational voltage from the SMPS:

DURING STAND-BY: From SMPS

- STBY 5V

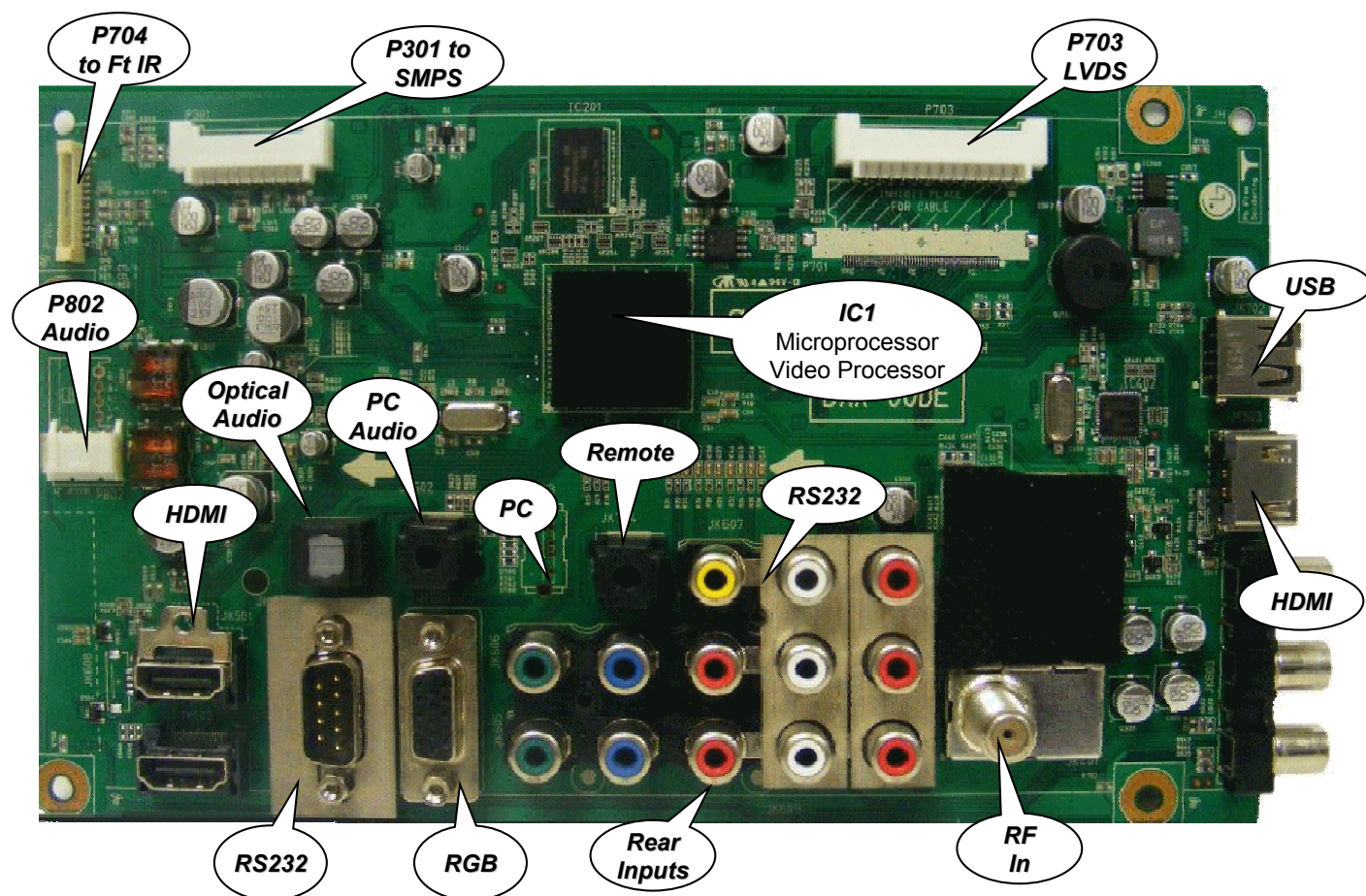
DURING RUN From SMPS : (STBY 5V remains):

- +5V for Video processing
- 17V for Audio

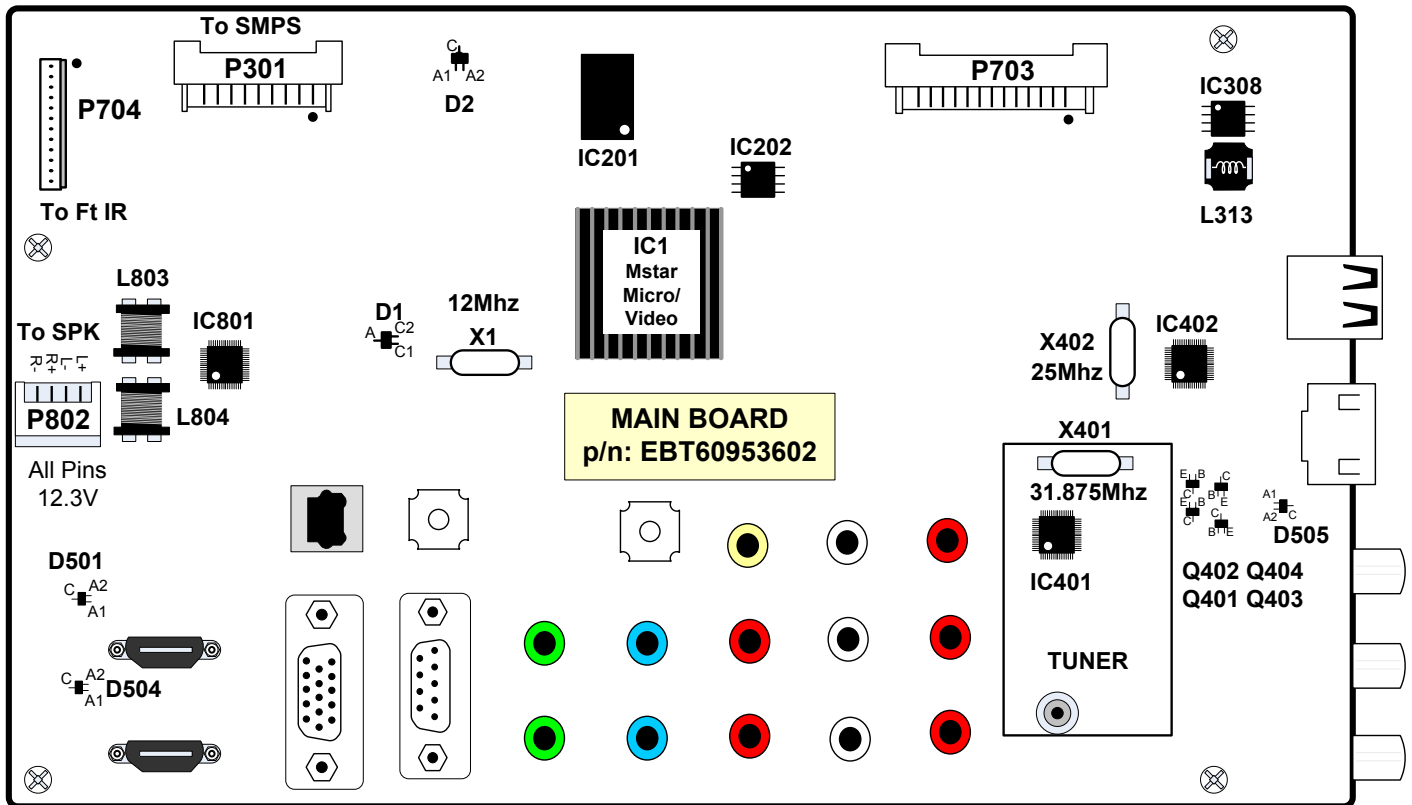
OUTPUTS:

- Distributes power supply turn on commands to the SMPS.
- Distributes Key 1 and Key 2 to the Front IR Board then to the Front Key Pad.
- Receives Intelligent Sensor data from the Front IR Board (via SCL/SDA).
- Drives front Power LEDs.
- Distributes +3.3V_ST and +3.3V_MST to the Front IR Board.
- Routes 10 bit LVDS video signals to the Control Board.

Main Board Layout and Identification



42PJ350 Main Front Layout Drawing



42PJ350 Main Board Front Side Component Voltages

IC202 7V (to IC405)

Pin Regulator



- [1] Gnd
- [2] Gnd
- [3] Gnd
- [4] Gnd
- [5] 3.3V
- [6] 3.3V
- [7] Gnd
- [8] 3.3V

IC308 1.3V_VDDC

Pin Regulator



- [1] Do not measure
- [2] Gnd
- [3] 5.04V
- [4] 6.07V
- [5] 4.99V
- [6] 1.28V
- [7] 1.28V
- [8] 4.27V

Use scope:
Pin 1: 1.4~1.7V P/P
Using DVM, set shuts off.

Use scope:
Pin 8: 600mV P/P
Using DVM, set shuts off.

Q401 Tuner CVBS

Pin Buffer (Analog)



- [B] 1.19V
- [E] 1.86V
- [C] Gnd

Q402 IF_P Buffer

Pin (Digital)



- [B] 1.18V
- [E] 1.18V
- [C] Gnd

Q403 Tuner SIF

Pin Buffer (Digital)



- [B] 1.32V
- [E] 1.99V
- [C] Gnd

Q404 IF_N Buffer

Pin (Digital)



- [B] 1.32V
- [E] 1.99V
- [C] Gnd

Q502 HDMI CEC

Pin Buffer



- [1 B] Gnd
- [2 S] 3.18V
- [3 D] 3.29V
- [4 G] 3.3V

D1 Reset

Pin Speed Up



- [A1] Gnd
- [A] 0V
- [A2] Gnd

D2 LED-R

Pin Routing



- [A1] 0V
- [C] 0.13V
- [A2] 0.28V

D501 B+ Routing

Pin to IC502



- [A1] 0V
- [A] 4.54V
- [A2] 5.0V

D504 B+ Routing

Pin to IC504



- [A1] 0V
- [A] 4.54V
- [A2] 5.0V

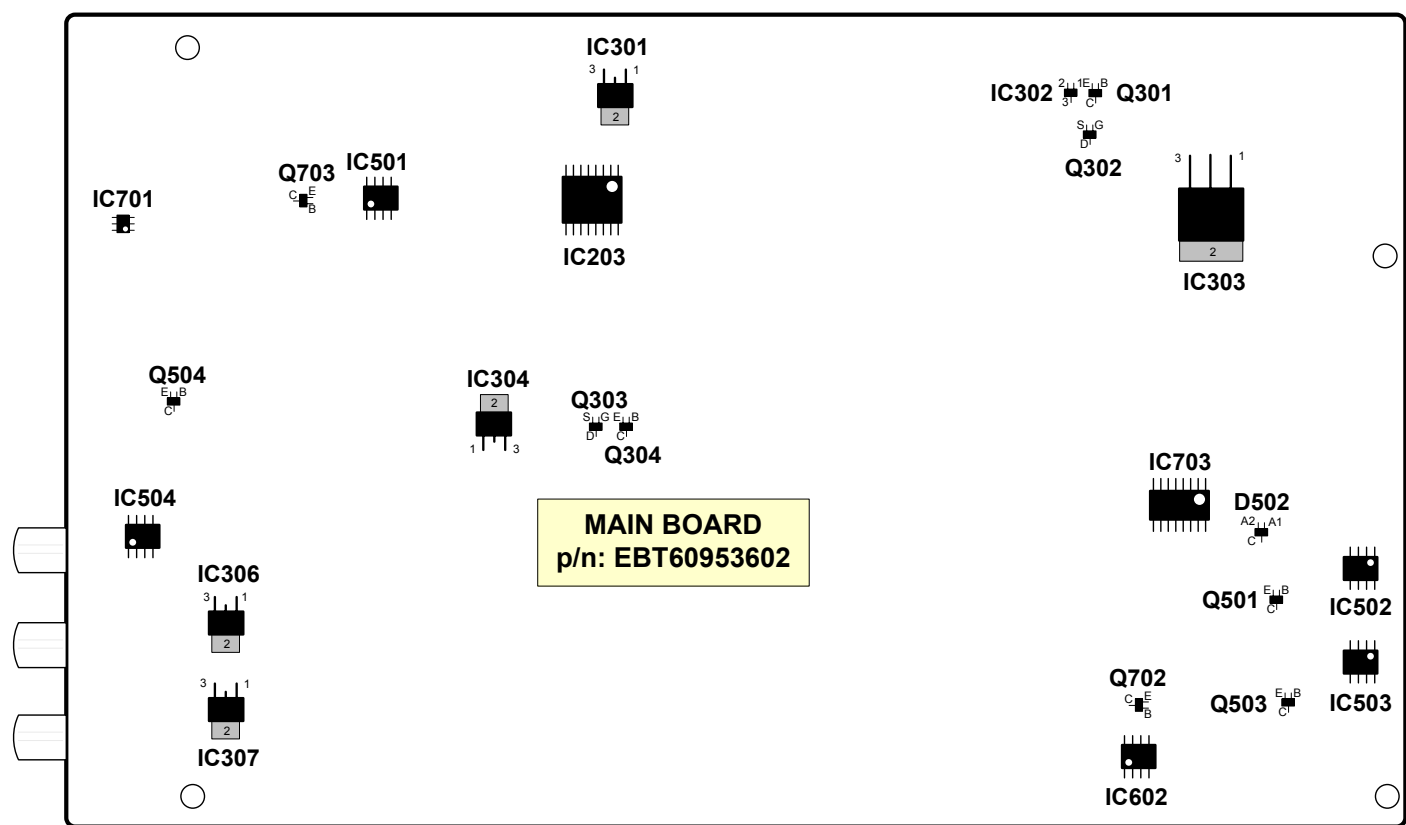
D505 B+ Routing

Pin to IC503



- [A1] 0V
- [A] 4.54V
- [A2] 5.0V

42PJ350 Main Back Layout Drawing



42PJ350 Main Board Back Side Component Voltages

IC203 Winbond Serial

Pin Flash
[1] 0V
[2] 3.30V
[3] n/c
[4] n/c
[5] n/c
[6] n/c
[7] 0V
[8] 3.3V
[9] 0V
[10] Gnd
[11] n/c
[12] n/c
[13] n/c
[14] n/c
[15] 0V
[16] 0V

IC301 1.8V_MST

Pin Regulator
[1] 0.6V
[2] 1.85V (Out)
[3] 3.3V (In)

IC302 3.3V_VST

Pin Regulator
[1] Gnd
[2] 3.3V (Out)
[3] 5.09V (In)

IC303 3.3V_MST

Pin Regulator
[1] Gnd
[2] 3.3V (Out)
[3] 5.04V (In)

IC304 1.2V_DVDD Reg

Pin Dig Ch Only
[1] Gnd
[2] 1.2V (Out)
[3] 3.3V (In)

Only on
with Dig
Channel

IC306 3.3V_TU

Pin Regulator
[1] Gnd
[2] 3.3V (Out)
[3] 4.97V (In)

IC307 1.8V_TU

Pin Regulator
[1] Gnd
[2] 1.8V (Out)
[3] 3.3V (In)

IC501 HDCP Data

Pin EEPROM
[1] Gnd
[2] Gnd
[3] 3.3V
[4] Gnd
[5] 3.3V
[6] 3.3V
[7] 3.3V
[8] 3.3V

IC502 IC503, IC504

EDID Data
Pin For HDMI
[1] Gnd
[2] Gnd
[3] Gnd
[4] Gnd
[5] 4.52V
[6] 4.52V
[7] 3.33V
[8] 4.53V

IC602 RGB

Pin EEPROM
[1] Gnd
[2] Gnd
[3] Gnd
[4] Gnd
[5] 5.09V
[6] 5.09V
[7] 3.33V
[8] 5.09V

IC701 USB 5V

Pin Limiter
[1] 4.97V (In)
[2] Gnd
[3] 3.3V (Enable)
[4] 0V
[5] 0V
[6] 4.97V (Out)

IC703 RS232 Tx/Rx

Pin
[1] 3.3V
[2] 5.45V
[3] 0V
[4] 0V
[5] (-5.37V)
[6] (-5.4V)
[7] (-5.4V)
[8] 0V
[9] 3.3V
[10] 3.3V
[11] n/c
[12] n/c
[13] 0V
[14] 5.45V
[15] Gnd
[16] 3.3V (B+)

Q301 Driver for 5V_MST

Pin Switch Q302
[B] 0.6V
[C] 0V
[E] Gnd

Q302 5V_MST

Pin Switch
[G] 0V
[S] 5.09V
[D] 5.04V

Q303 3.3V_PVSB Sw

Pin Dig Ch Only
[G] 0V
[S] 3.3V
[D] 3.3V

Only on
with Dig
Channel

Q304 Driver for 3.3V_PVSB

Pin Switch Q303
[B] 0.64V
[C] 0V
[E] Gnd

Only on
with Dig
Channel

Q501, Q503

Hot Swap
Pin Switch for HDMI
[B] 0V
[C] 0V
[E] Gnd

Q702 RS232

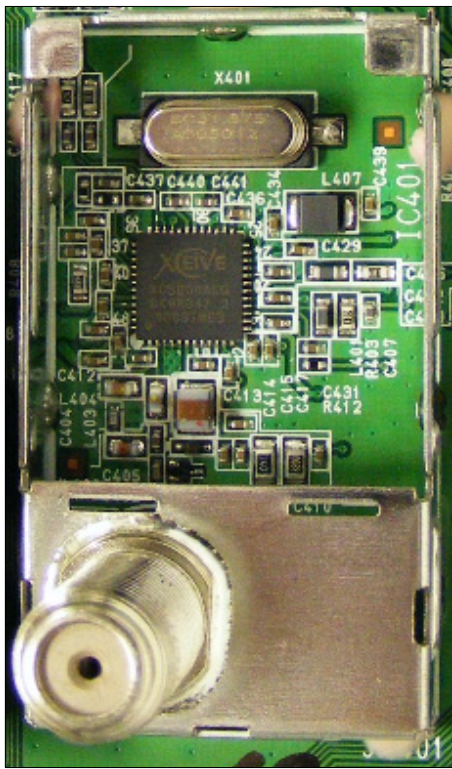
Pin Tx Buffer
[B] 0.6V
[C] 0V
[E] Gnd

D502 HDMI CEC Limiter

Pin
[A1] 0V
[A2] 3.28V
[C] 3.1V

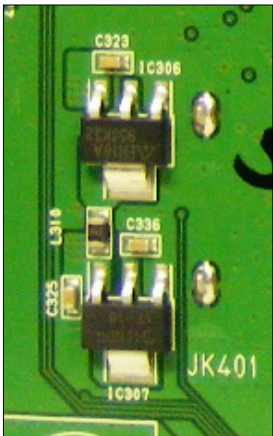
Main Board Tuner Explained

The Tuner in this set is discreet components (Silicon Tuner) and no longer a self contained unit (can).



Front bottom right hand side

Check for Tuner B+:
3.3V on IC306 and 1.8V on IC307



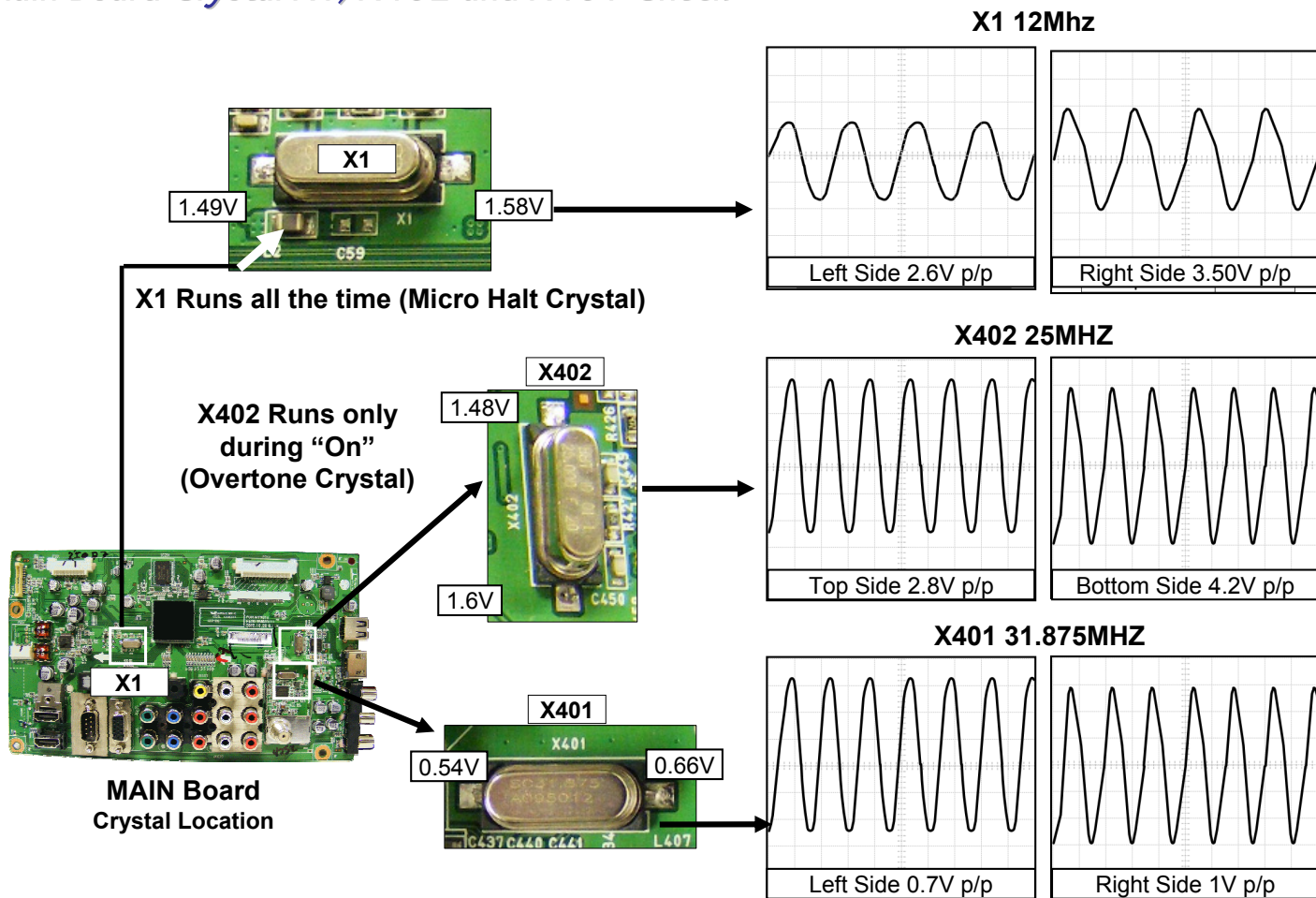
- IC306** 3.3V_TU
Pin Regulator

3	1
[1] Gnd	
[2] 3.3V (Out)	
[3] 4.97V (In)	
- IC307** 1.8V_TU
Pin Regulator

3	1
[1] Gnd	
[2] 1.8V (Out)	
[3] 3.3V (In)	

Back Side bottom left hand side

Main Board Crystal X1, X402 and X401 Check

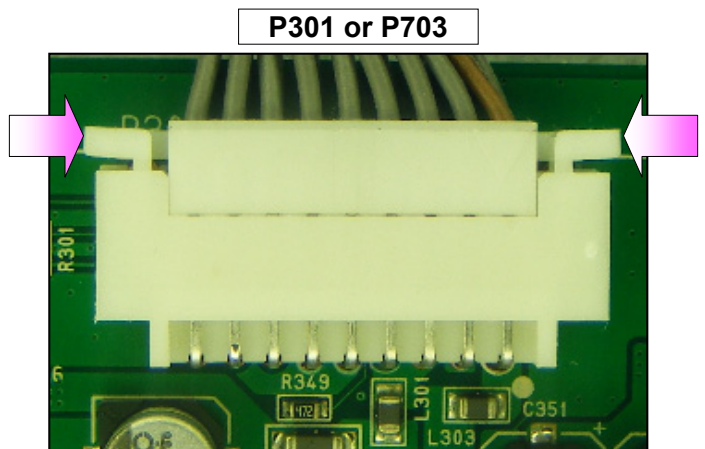
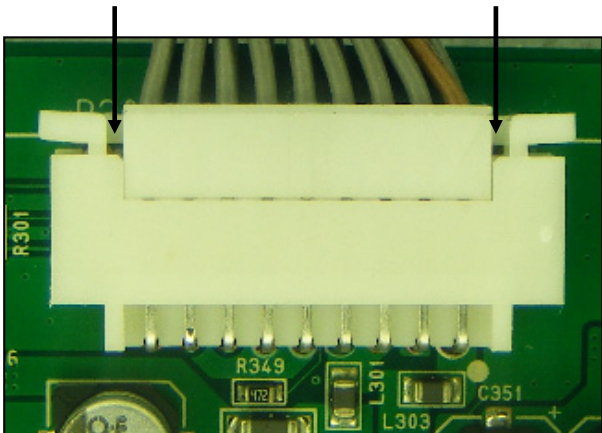


Main Board Removing the LVDS Cable or Power Supply Connector

(1) Using your fingers and press in gently on the two locking tabs.
Then rock the connector out of the plug.

(2) Pull the Cable from the Connector
by rocking back and forth.

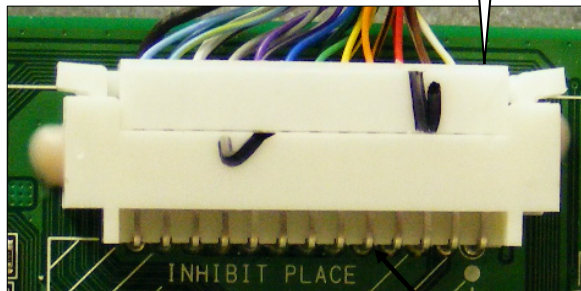
If the Connector Locks have been damaged and will not release, use a thin object and slide straight down (as indicated by the arrows below) and release the locks.



Main Board P703 LVDS Video Signal Test Points

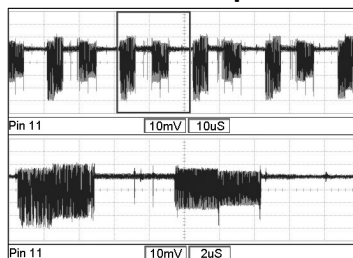
Pin 1 front row right side
Note: There are no wires
into pins 1 and 2.

1



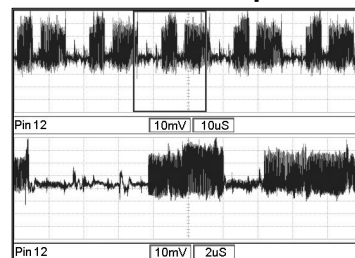
Waveforms Taken from P703 pins 11 and 12, but there
are actually 10 pins carrying video.
Input Signal SMPT Color Bar. 10mV per/div.

Pin 11 10uSec per/div



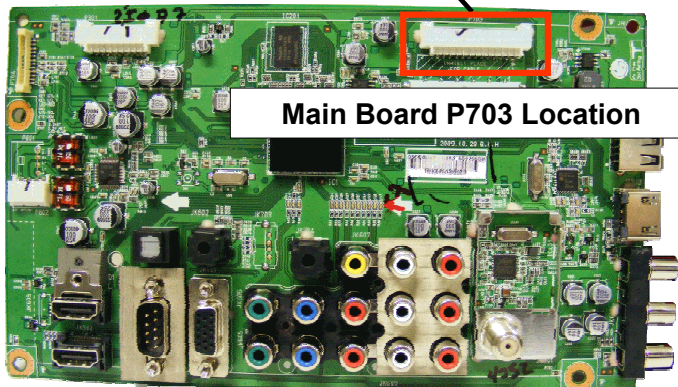
Pin 11 2uSec per/div

Pin 12 10uSec per/div



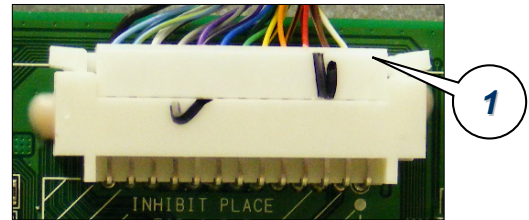
Pin 12 2uSec per/div

Main Board P703 Location



Main Board Plug P703 "LVDS" Voltages

Voltage and Diode Test for the Main Board



P703 "Main Board" Connector to P121 "Control Board"

Pin	Label	Run	Diode Check	Pin	Label	Run	Diode Check
1	n/c	n/c	Open	2	n/c	n/c	Open
3	ROM_RX	3.29V	2.6V	4	ROM_TX	3.29V	2.59V
5	Gnd	Gnd	Gnd	6	Gnd	Gnd	Gnd
7	Gnd	Gnd	Gnd	8	Gnd	Gnd	Gnd
9	Module_SCL1	3.29V	2.6V	10	Module_SDA1	3.29V	2.6V
11	RE2+	1.29V	0.86V	12	RE2-	1.19V	0.86V
13	RD2+	1.31V	0.86V	14	RD2-	1.23V	0.86V
15	RCLK2+	1.26V	0.86V	16	RCLK2-	1.29V	0.86V
17	RC2+	1.23V	0.86V	18	RC2-	1.27V	0.86V
19	RB2+	1.31V	0.86V	20	RB2-	1.18V	0.86V
21	RA2+	1.37V	0.86V	22	RA2-	1.13V	0.86V
23	PC_SER_CLK	0.59V	1.02V	24	PC_SER_DATA	3.24V	1.52V
25	DISP_EN	2.79V	0.49V	26	Gnd	Gnd	Gnd

Pin 1 front row right side
Note: There are no wires
into pins 1 and 2.

Blue Pins indicate 10 bit
differential video signal

Note:
There are no voltages in
Stand-By mode.

Diode Mode Check with the Board Disconnected.

Main Board Plug P704 to IR Board

Voltage and Diode Mode Measurements for the Main Board

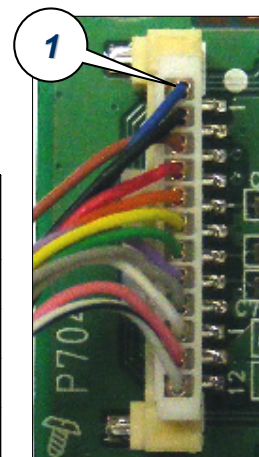
P704 Connector "Main Board" to P100 "Front Keys"

Pin	Label	STBY	Run	Diode Check
1	IR	3.43V	4.9V	Open
2	Gnd	Gnd	Gnd	Gnd
3	Key_CTL_0	3.29V	3.29V	1.73V
4	Key_CTL_1	3.29V	3.29V	1.73V
5	LED_RED	2.72V	0V	Open
6	Gnd	Gnd	Gnd	Gnd
7	EYE_SCL	0V	3.29V	2.63V
8	EYE_SDA	0.23V	3.29V	2.63V
9	Gnd	Gnd	Gnd	Gnd
10	3.3VST	3.29V	3.29V	1.09V
11	3.3V_MST	0V	3.29V	0.55V
12	LED_BLUE	0V	0V	Open

3 & 4
Soft Touch
Key Board

7 & 8
Intelligent
Sensor

Stand-By
3.3V

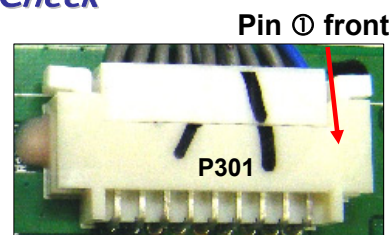


Diode Mode Readings taken with all connectors Disconnected. DVM in Diode Mode.

Main Board Plug P301 to Power Supply Voltages and Diode Check

P301 Connector "Main" to "SMPS Board" P813

Pin	Label	STBY	Run	Diode Check
1_2	17V	0V	16.8V	Open
3-4	Gnd	Gnd	Gnd	Gnd
5-7	5V	0.47V	5.24V	0.94V
8	^c Error_Det	2.88V	4.93V	3.04V
9-12	Gnd	Gnd	Gnd	Gnd
13-14	STBY_5V	3.49V	5.23V	1.1V
15	^a RL_ON	0V	2.43V	2.52V
16	^d AC Det	0V	4.45V	2.93V
17	^b M_ON	0V	3.27V	Open
18	^e Auto_Gnd	Gnd	Gnd	Gnd



Front pins are odd
Back pins are even

a Note: The RL_On turns on +5V, 17V Error Det. and AC_DET.

b Note: The M5-On command turns on M5V, Va and Vs.

c Note: The Error Det line is not used in this model.

d Note: If the AC Det line is Missing, the TV will turn off in 10 Seconds.

e Note: Pin 18 is grounded on the Main. If opened, the power supply turns on automatically.

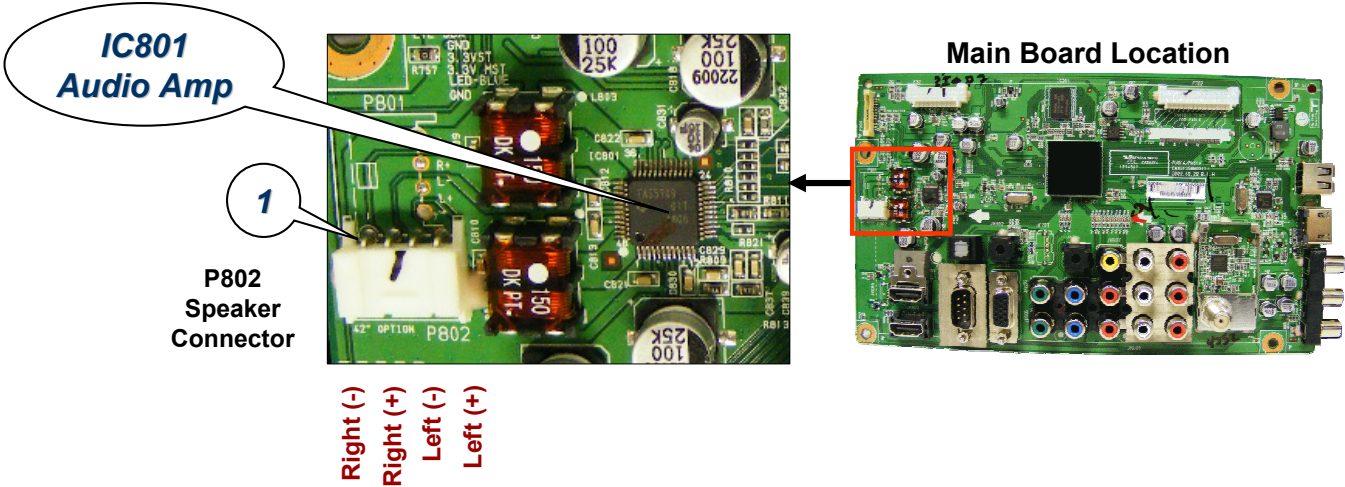
Diode Mode Check with the Board Disconnected. DVM in the Diode mode.

Main Board Speaker Plug P802 Voltage and Diode Check

Voltage and Diode Mode Measurements for the Main Board Speaker Plug

P802 Connector "Main" to "Speakers"

Pin	Label	SBY	Run	Diode Mode
1	R-	0V	8.39V	Open
2	R+	0V	8.39V	Open
3	L-	0V	8.39V	Open
4	L+	0V	8.39V	Open



Diode Mode Check with the Board Disconnected. DVM in the Diode mode.

FRONT IR, POWER LED and SOFT TOUCH KEY PAD SECTION

The following section gives detailed information about the Front IR and Soft Touch Key Pad. These boards contains the Infrared Receiver, Intelligent Sensor and Power LEDs section. The Soft Touch Function Keys is actually a thin pad adhered to the front protective shield.

The Power LED Driver and Intelligent Sensor IC communicate with the Main Board Microprocessor (IC1) via Clock and Data lines.

These boards have no adjustments.

The Front Control Board (IR and Intelligent Sensor) receives its operational B+ from the Main Board:

- 3.3V_ST from the Main Board. This voltage is generated on the Main Board (IC302)
- 3.3V_MST generated on the Main Board (IC303).

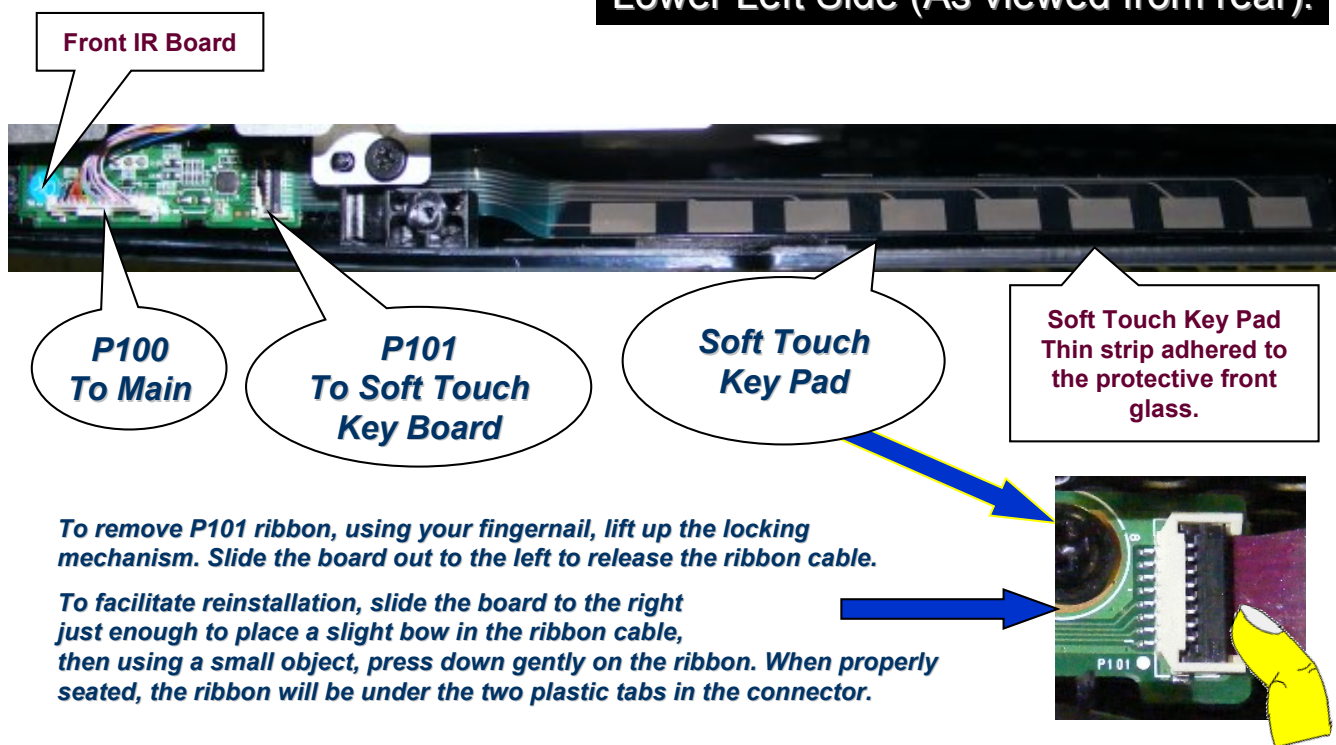
The Intelligent Sensor sends its data from the IR board to the Video Processor by 2 separate pins from the Main board SCL/SDA pins 7 and 8.

The IR signal is routed back to the Main Board via pin 1.

Also, the Soft Touch Key Pad is routed through the Front IR board and out P100 to P704 pins 3 and 4.

Front Control (IR and Intelligent Sensor) Board and Power LED Board Location

Lower Left Side (As viewed from rear).



Front Control Board Connector P100 Voltage and Pin Identification

P100 Connector "Front Keys" to P704 "Main Board"

Pin	Label	STBY	Run	Diode Check
1	IR	3.43V	4.9V	Open
2	Gnd	Gnd	Gnd	Gnd
3	Key_CTL_0	3.29V	3.29V	2.52V
4	Key_CTL_1	3.29V	3.29V	2.52V
5	LED_RED	2.72V	0.0V	3.13V
6	Gnd	Gnd	Gnd	Gnd
7	EYE_SCL	0V	3.29V	2.22V
8	EYE_SDA	0.23V	3.29V	2.21V
9	Gnd	Gnd	Gnd	Gnd
10	3.3VST	3.29V	3.29V	2.17V
11	3.3V_MST	0V	3.29V	2.25V
12	LED_BLUE	0V	0V	Open

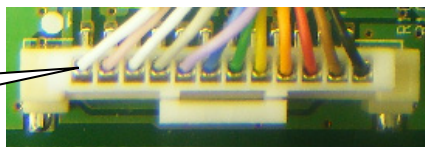
For the Soft Touch
Key Pad section.

7 & 8
Front LEDs
and
Intelligent
Sensor

Stand-By
3.3V

For Readings when any Key is
touched, see Soft Key Pad Section
For Key 1 and Key 2.

1



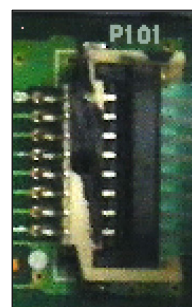
Diode Mode Readings taken with all connectors Disconnected. Black lead on Gnd. DVM in Diode Mode.

Front IR Board Plug P101 to Soft Touch Keys (Voltages and Pin Identification)

Voltage and Diode Mode Measurements for the Main Board

P101 CONNECTOR "Ft IR Board" to "Ft Key Pad"

Pin	STBY	Run	Diode Check
1	0.07	0.16	2.4V
2	0.07	0.16	2.4V
3	0.07	0.16	2.4V
4	0.07	0.16	2.4V
5	0.07	0.16	2.4V
6	0.07	0.16	2.4V
7	0.07	0.16	2.4V
8	0.07	0.16	2.4V



Voltage Measured with a Scope

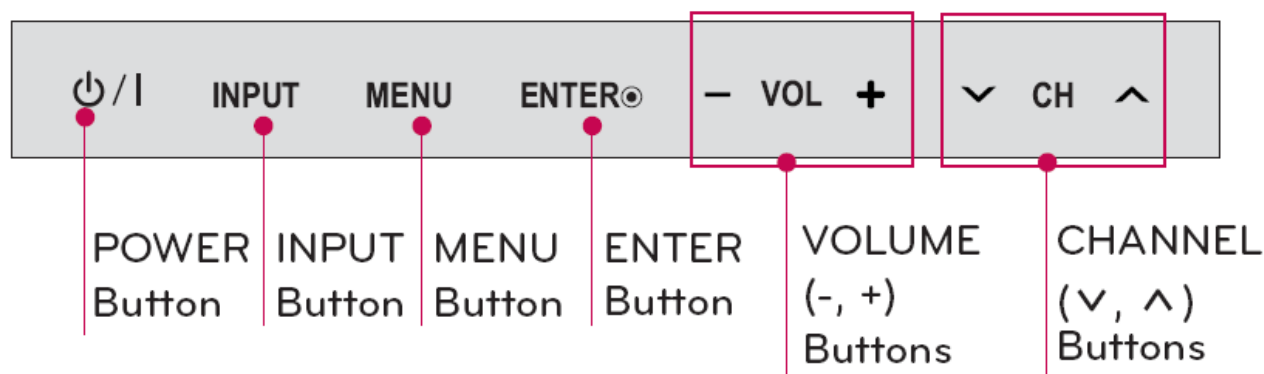
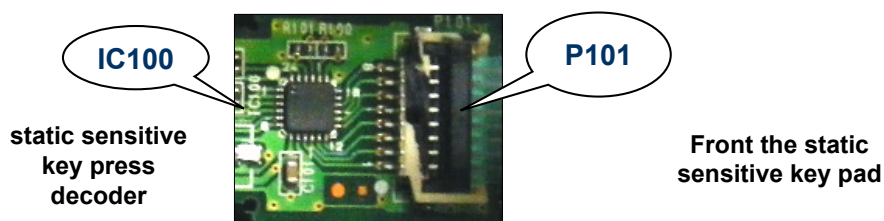
Measuring Voltage on Pin 1 with DVM turns the TV on. If TV is on, Input Menu pops up.

Diode Mode Readings taken with all connectors Disconnected. Black lead on Gnd. DVM in Diode Mode.



SOFT TOUCH KEY PAD SECTION (Board Layout and Identification)

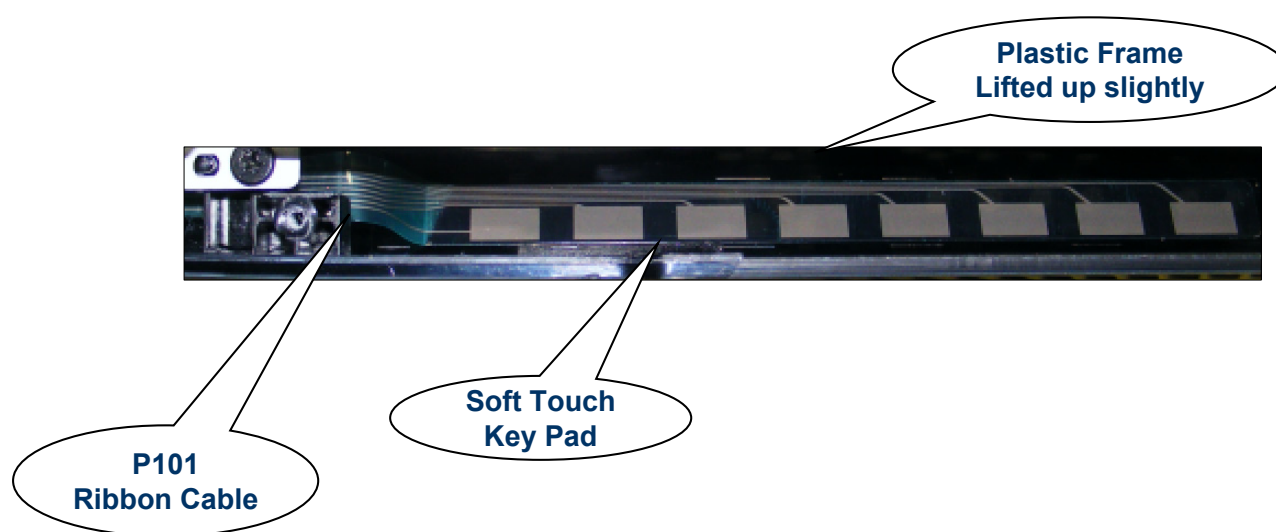
The Soft Touch Key Pad is a thin “Static” sensitive pad that is adhered to the front protective shield. The Soft Touch Key Pad requires a static sensitive key press decoder IC to change the key press data into R2 Ladder (Resistive data) which the Microprocessor can understand. This IC is on the Front IR board IC100 which receives key press data from P101. The output from this IC simply selects the appropriate resistor to inject into the Key 1 or Key 2 line which is then interpreted by the Microprocessor in the Main board IC1.



Button Identification for the Front the static sensitive key pad

Soft Touch Key Pad

The Soft Touch Key Pad is a thin “Static” sensitive pad that is adhered to the inside of the front protective shield.



Soft Touch Key Pad Resistance and Diode Mode Checks

IC100 on the Front IR Board is generating these Resistance changes when a Soft Touch Key is touched. This in turn pulls down the Key 1 and Key 2 lines to be interpreted by the Microprocessor.

P100 (Key 1, Key 2) Resistance Reading with Soft Touch Key pressed.

KEY	Pin 3 measured from Gnd		KEY	Pin 4 measured from Gnd
CH (Up)	0.61K Ohms		Volume (+)	3.6K Ohms
CH (Dn)	9K Ohms		Volume (-)	0.62K Ohms
Input	3.66K Ohms		Enter	22K Ohms
			Menu	9K Ohms

P100 Voltage Measurements with Soft Touch Key pressed.

KEY	Pin 3 measured from Gnd		KEY	Pin 4 measured from Gnd
CH (Up)	2.1V		Volume (+)	0.89V
CH (Dn)	1.619V		Volume (-)	0.214V
Input	0.88V		Enter	2.42V
			Menu	1.667V

P100 Connector "IR/LED Control Board" to P703 "Main" (No Key Pressed)

Diode Mode
Readings taken with all connectors Disconnected. Black lead on Gnd. DVM in Diode Mode.

Pin	Label	STBY	Run	Diode Mode
3	KEY 1	3.29V	3.29V	2.58V
4	KEY 2	3.29V	3.29V	1.58V

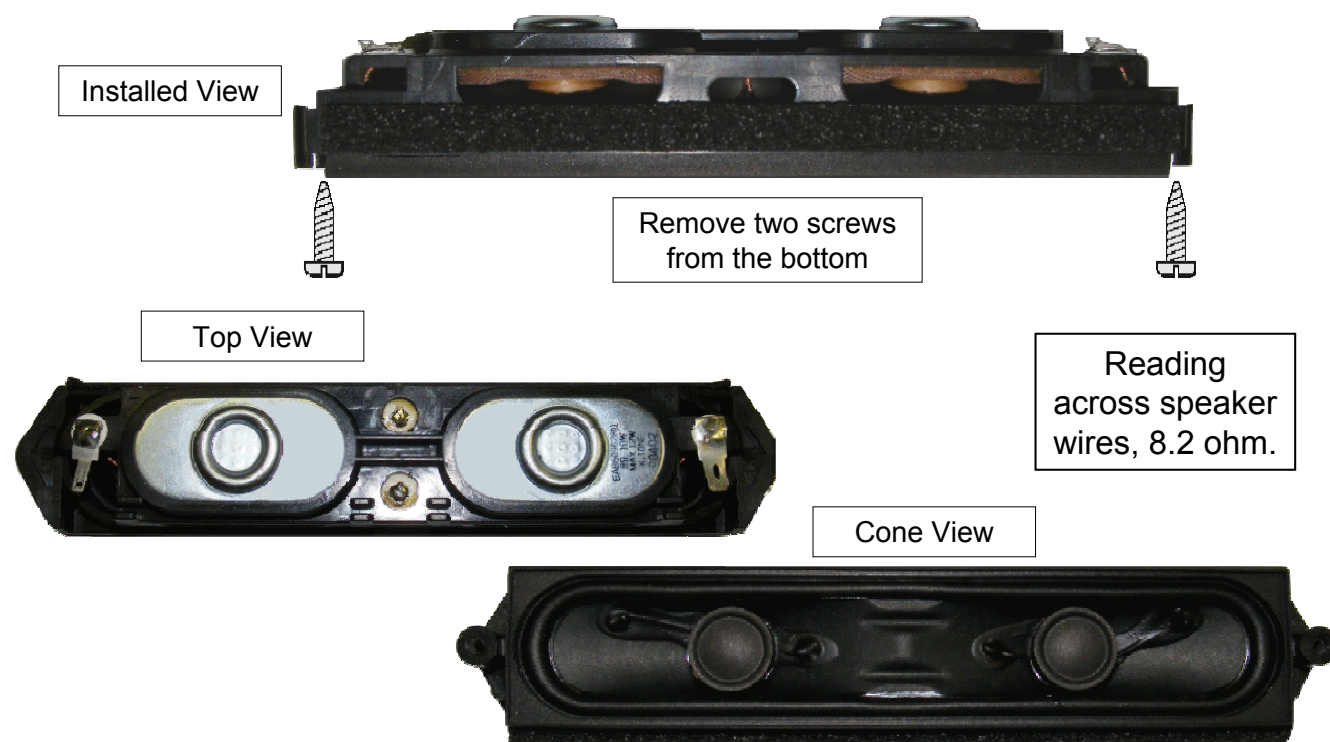
INVISIBLE SPEAKER SYSTEM SECTION

Invisible Speaker System Overview (Full Range Speakers)

p/n: EAB60962801

The 42PJ350 contains the Invisible Speaker system.

The Full Range Speakers point downward, so there are no front viewable speaker grills or air ports.



INTERCONNECT DIAGRAM (11 X 17 Foldout) SECTION

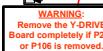
This section shows the Interconnect Diagram called the 11X17 foldout that's available in the Paper and Adobe version of the Training Manual.

Use the Adobe version to zoom in for easier reading.















When Printing the Interconnect diagram, print from the Adobe version and print onto 11X17 size paper for best results.

NOTE: Diode tests are conducted with the board disconnected.
NOTE: Grayed components are on the back of the PWB.




















NOTE: Diode tests are conducted with the board disconnected
NOTE: Grayed components are on the back of the PWB.



42PJ350 Main Board (Front Side) Component Voltages

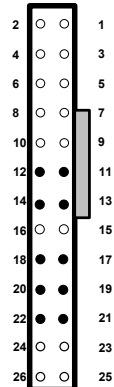
IC202 7V (to IC405) Pin Regulator  <ul style="list-style-type: none"> [1] Gnd [2] Gnd [3] Gnd [4] Gnd [5] 3.3V [6] 3.3V [7] Gnd [8] 3.3V 	Q401 Tuner CVBS Pin Buffer (Analog)  <ul style="list-style-type: none"> [B] 1.19V [E] 1.86V [C] Gnd 	Q502 HDMI CEC Pin Buffer  <ul style="list-style-type: none"> [1 B] Gnd [2 S] 3.18V [3 D] 3.29V [4 G] 3.3V 	D501 B+ Routing Pin to IC502  <ul style="list-style-type: none"> [A1] 0V [A] 4.54V [A2] 5.0V
IC308 1.3V_VDDC Pin Regulator  <ul style="list-style-type: none"> [1] Do not measure [2] Gnd [3] 5.04V [4] 6.07V [5] 4.99V [6] 1.28V [7] 1.28V [8] 4.27V 	Q402 IF_P Buffer Pin (Digital)  <ul style="list-style-type: none"> [B] 1.18V [E] 1.18V [C] Gnd 	D1 Reset Pin Speed Up  <ul style="list-style-type: none"> [A1] Gnd [A] 0V [A2] Gnd 	D504 B+ Routing Pin to IC504  <ul style="list-style-type: none"> [A1] 0V [A] 4.54V [A2] 5.0V
IC308 1.3V_VDDC Pin Regulator  <ul style="list-style-type: none"> [1] Do not measure [2] Gnd [3] 5.04V [4] 6.07V [5] 4.99V [6] 1.28V [7] 1.28V [8] 4.27V 	Q403 Tuner SIF Pin Buffer (Digital)  <ul style="list-style-type: none"> [B] 1.32V [E] 1.99V [C] Gnd 	D2 LED-R Pin Routing  <ul style="list-style-type: none"> [A1] 0V [C] 0.13V [A2] 0.28V 	D505 B+ Routing Pin to IC503  <ul style="list-style-type: none"> [A1] 0V [A] 4.54V [A2] 5.0V
IC308 1.3V_VDDC Pin Regulator  <ul style="list-style-type: none"> [1] Do not measure [2] Gnd [3] 5.04V [4] 6.07V [5] 4.99V [6] 1.28V [7] 1.28V [8] 4.27V 	Q404 IF_N Buffer Pin (Digital)  <ul style="list-style-type: none"> [B] 1.32V [E] 1.99V [C] Gnd 		

42PJ350 Main Board (Back Side) Component Voltages

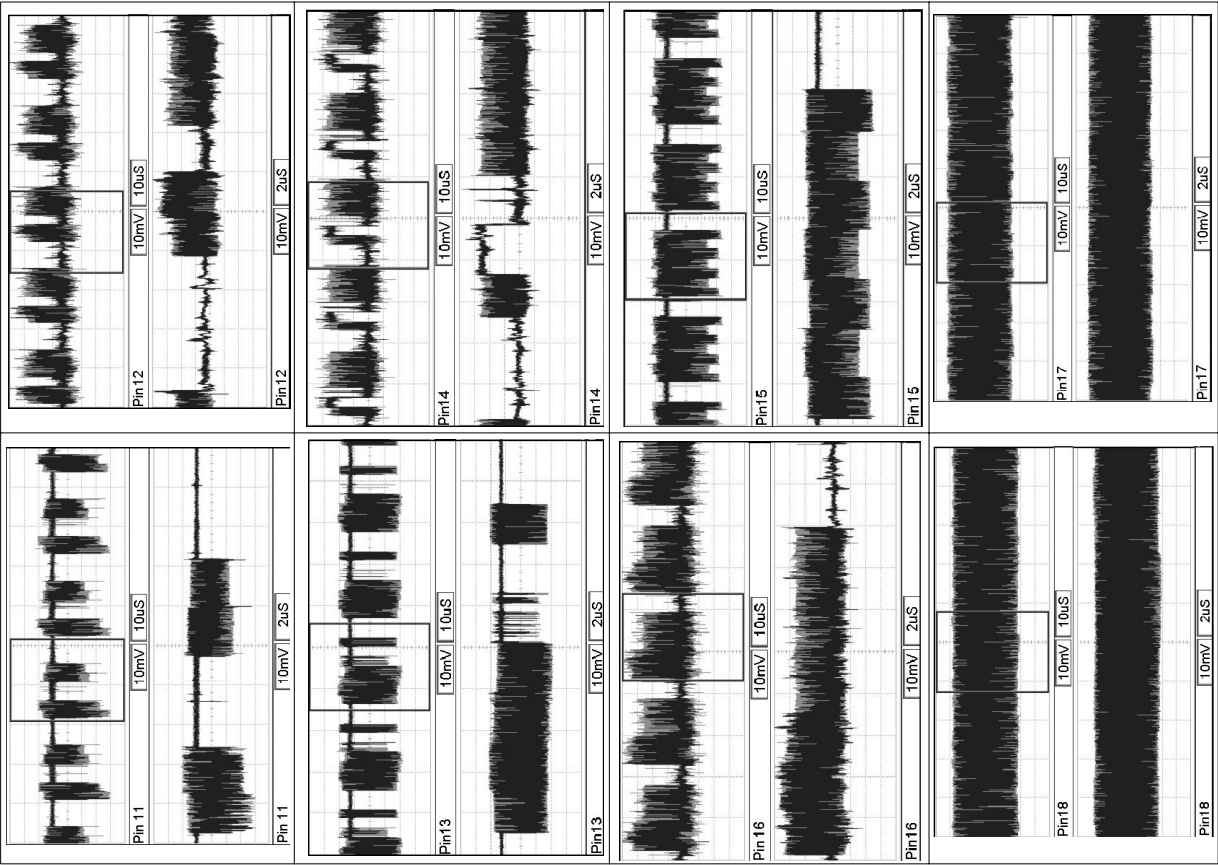
IC203 Winbond Serial Pin Flash  <ul style="list-style-type: none"> [1] 0V [2] 3.30V [3] n/c [4] n/c [5] n/c [6] n/c [7] 0V [8] 3.3V [9] 0V [10] Gnd [11] n/c [12] n/c [13] n/c [14] n/c [15] 0V [16] 0V 	IC303 3.3V_MST Pin Regulator  <ul style="list-style-type: none"> [1] Gnd [2] 3.3V (Out) [3] 5.04V (In) 	IC501 HDCP Data Pin EEPROM  <ul style="list-style-type: none"> [1] Gnd [2] Gnd [3] 3.3V [4] Gnd [5] 3.3V [6] 3.3V [7] 3.3V [8] 3.3V 	IC701 USB 5V Pin Limiter  <ul style="list-style-type: none"> [1] 4.97V (In) [2] Gnd [3] 3.3V (Enable) [4] 0V [5] 0V [6] 4.97V (Out) 	Q301 Driver for 5V_MST Pin Switch Q302  <ul style="list-style-type: none"> [B] 0.6V [C] 0V [E] Gnd 	Q702 RS232 Pin Tx Buffer  <ul style="list-style-type: none"> [B] 0.6V [C] 0V [E] Gnd
IC304 1.2V_DVDD Reg Pin Dig Ch Only  <ul style="list-style-type: none"> [1] Gnd [2] 1.2V (Out) [3] 3.3V (In) 	IC306 3.3V_TU Pin Regulator  <ul style="list-style-type: none"> [1] Gnd [2] 3.3V (Out) [3] 4.97V (In) 	IC502 IC503, IC504 EDID Data Pin For HDMI  <ul style="list-style-type: none"> [1] Gnd [2] Gnd [3] Gnd [4] Gnd [5] 4.52V [6] 4.52V [7] 3.33V [8] 4.53V 	IC703 RS232 Tx/Rx Pin  <ul style="list-style-type: none"> [1] 3.3V [2] 5.45V [3] 0V [4] 0V [5] (-5.37V) [6] (-5.4V) [7] (-5.4V) [8] 0V [9] 3.3V [10] 3.3V [11] n/c [12] n/c [13] 0V [14] 5.45V [15] Gnd [16] 3.3V (B+) 	Q302 5V_MST Pin Switch  <ul style="list-style-type: none"> [G] 0V [S] 0V [S] 5.09V [D] 5.04V 	D502 HDMI CEC Limiter Pin  <ul style="list-style-type: none"> [A1 A2] 0V [A1] 0V [A2] 3.28V [C] 3.1V
IC301 1.8V_MST Pin Regulator  <ul style="list-style-type: none"> [1] 0.6V [2] 1.85V (Out) [3] 3.3V (In) 	IC307 1.8V_TU Pin Regulator  <ul style="list-style-type: none"> [1] Gnd [2] 1.8V (Out) [3] 3.3V (In) 	IC602 RGB Pin EEPROM  <ul style="list-style-type: none"> [1] Gnd [2] Gnd [3] Gnd [4] Gnd [5] 5.09V [6] 5.09V [7] 3.33V [8] 5.09V 	Q303 3.3V_PVSB Sw Pin Dig Ch Only  <ul style="list-style-type: none"> [G] 0V [S] 3.3V [D] 3.3V 	Q304 Driver for 3.3V_PVSB Pin Switch Q303  <ul style="list-style-type: none"> [B] 0.64V [C] 0V [E] Gnd 	Q501, Q503 Hot Swap Pin Switch for HDMI  <ul style="list-style-type: none"> [B] 0V [C] 0V [E] Gnd
IC302 3.3V_VST Pin Regulator  <ul style="list-style-type: none"> [1] Gnd [2] 3.3V (Out) [3] 5.09V (In) 					

42PJ350 LVDS
Video Waveforms

Connector P703 Configuration
● - indicates signal pins.



15 and 16
are the Video Clock and
Data lines



End of Presentation

This concludes the Presentation

Thank You



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August 2010

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Plasma