512Mb (8Mx4Banks×16) DDR2 SDRAM

Descriptions

The H2A35121656B is a high speed Double Date Rate 2 (DDR2) Synchronous DRAM fabricated with ultra high performance CMOS process containing 536,870,912 bits which organized as 8Mbits x 4 banks by 16 bits. This synchronous device achieves high speed double-data-rate transfer rates of up to 1066 Mb/sec/pin (DDR2-1066) for general applications. The chip is designed to comply with the following key DDR2 SDRAM features: (1) posted CAS with additive latency, (2) write latency = read latency -1, (3) Off-Chip Driver (OCD) impedance adjustment and On Die Termination (4) normal and weak strength data output driver. All of the control and address inputs are synchronized with a pair of externally supplied differential clocks. Inputs are latched at the cross point of differential clocks (CK rising and /CK falling). All I/Os are synchronized with a pair of bidirectional strobes (DQS and /DQS) in a source synchronous fashion. The address bus is used to convey row, column and bank address information in a /RAS and /CAS multiplexing style. The 512 Mb DDR2 devices operate with a single power supply: 1.8V ± 0.1V VDD and VDDQ. Available package: TFBGA-84Ball.

Features

- JEDEC Standard VDD/VDDQ = 1.8V±0.1V.
- All inputs and outputs are compatible with SSTL_18 interface.
- Fully differential clock inputs (CK, /CK) operation.
- Four Banks
- Posted CAS
- Bust length: 4 and 8.
- Programmable CAS Latency (CL): 3, 4, 5, 6 & 7.
- Programmable Additive Latency (AL):0, 1, 2, 3, 4, 5 & 6.
- Write Latency (WL) =Read Latency (RL) -1.
- Read Latency (RL) = Programmable Additive Latency (AL) + CAS Latency (CL)
- Bi-directional Differential Data Strobe (DQS).
- Data inputs on DQS centers when write.
- Data outputs on DQS, /DQS edges when read.
- On chip DLL align DQ, DQS and /DQS transition with CK transition.
- DM mask write data-in at the both rising and falling edges of the data strobe.
- Sequential & Interleaved Burst type available.
- Off-Chip Driver (OCD) Impedance Adjustment
- On Die Termination (ODT)
- Auto Refresh and Self Refresh
- 8,192 Refresh Cycles / 64ms
- Average Refresh Period 7.8us at lower than Tcase 85 °C, 3.9us at 85°C < Tcase ≦ 95°C
- RoHS Compliance
- Partial Array Self-Refresh (PASR)
- High Temperature Self-Refresh rate enable

Ordering Information

Part No	Organization	Max. Freq	Package	Grade
H2A35121656BA6C	32M X 16	DDR2-667 (5-5-5)	84Ball BGA, 8x12.5mm	Commercial
H2A35121656BB6C	32M X 16	DDR2-800 (6-6-6)	84Ball BGA, 8x12.5mm	Commercial
H2A35121656BC6C	32M X 16	DDR2-1066 (7-7-7)	84Ball BGA, 8x12.5mm	Commercial

Note: Speed (tck*) is in order of CL-T_{RCD}-T_{RP}

Ball Assignments and Descriptions

84-Ball FBGA – x16 (Top View)

1	2	3		7	8	9
VDD	NC	VSS	A	VSSQ	/UDQS	VDDQ
DQ14	VSSQ	UDM	B	UDQS	VSSQ	DQ15
VDDQ	DQ9	VDDQ	C	VDDQ	DQ8	VDDQ
DQ12	VSSQ	DQ11	D	DQ10	VSSQ	DQ13
VDD	NC	VSS	E	VSSQ	/LDQS	VDDQ
DQ6	VSSQ	LDM	F	LDQS	VSSQ	DQ7
VDDQ	DQ1	VDDQ	G	VDDQ	DQ0	VDDQ
DQ4	VSSQ	DQ3	H	DQ2	VSSQ	DQ5
VDDL	VREF	VSS	J	VSSDL	CK	VDD
	CKE	/WE	K	/RAS	/CK	ODT
NC	BA0	BA1	L	/CAS	/CS	
	A10/AP	A1	M	A2	A0	VDD
VSS	A3	A5	N	A6	A4	
	A7	A9	P	A11	A8	VSS
VDD	A12	NC	R	NC	NC	

84-Ball FBGA – x16 Ball Descriptions

Pin	Symbol	Description
M8,M3,M7,N2, N8,N3,N7,P2, P8,P3,M2,P7, R2	A0−A12	**(Address)** Provide the row address for active commands, and the column address and Auto-precharge bit for Read/Write commands to select one location out of the memory array in the respective bank. Row address: A0−A12. Column address: A0−A9. (A10 is used for Auto-precharge)
L2,L3	BA0−BA1	**(Bank Select)** BA0−BA1 define to which bank an ACTIVE, READ, WRITE or PRECHARGE command is being applied.
G8,G2,H7,H3, H1,H9,F1,F9, C8,C2,D7,D3, D1,D9,B1,B9	DQ0−DQ15	**(Data Input / Output)** Bi-directional data bus.
K9	ODT	**(On Die Termination Control)** ODT (registered HIGH) enables termination resistance internal to the DDR2 SDRAM.
F7,E8	LDQS, /LDQS	**(LOW Data Strobe)** Data Strobe for Lower Byte: Output with read data, input with write data for source synchronous operation. Edge-aligned with read data, centeraligned with write data. LDQS corresponds to the data on DQ0−DQ7. /LDQS is only used when differential data strobe mode is enabled via the control bit at EMR (1)[A10 EMRS command].
B7,A8	UDQS, /UDQS	**(UP Data Strobe)** Data Strobe for Upper Byte: Output with read data, input with write data for source synchronous operation. Edge-aligned with read data, centeraligned with write data. UDQS corresponds to the data on DQ8−DQ15. /UDQS is only used when differential data strobe mode is enabled via the control bit at EMR (1)[A10 EMRS command].
L8	/CS	**(Chip Select)** All commands are masked when /CS is registered HIGH. /CS provides for external rank selection on systems with multiple ranks. CS is considered part of the command code.
K7,L7,K3	/RAS , /CAS , /WE	**(Command Inputs)** /RAS , /CAS and /WE (along with /CS) define the command being entered.

B3,F3	UDM, LDM	**(Input Data Mask)** DM is an input mask signal for write data. Input data is masked when DM is sampled high coincident with that input data during a Write access. DM is sampled on both edges of DQS. Although DM pins are input only, the DM loading matches the DQ and DQS loading.
J8,K8	CLK, /CLK	**(Differential Clock Inputs)** CLK and /CLK are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CLK and negative edge of /CLK . Output (read) data is referenced to the crossings of CLK and /CLK (both directions of crossing).
K2	CKE	**(Clock Enable)** CKE (registered HIGH) activates and CKE (registered LOW) deactivates clocking circuitry on the DDR2 SDRAM.
J2	VREF	**(Reference Voltage)** VREF is reference voltage for inputs
A1,E1,J9,M9,R1	VDD	**(Power Supply)** Power Supply: 1.8V ± 0.1V.
A3,E3,J3,N1,P9	VSS	**(Ground)** Ground.
A9,C1,C3,C7, C9,E9,G1,G3, G7,G9	VDDQ	**(DQ Power Supply)** DQ Power Supply: 1.8V ± 0.1V.
A7,B2,B8,D2, D8,E7,F2,F8, H2,H8	VSSQ	**(DQ Ground)** DQ Ground. Isolated on the device for improved noise immunity
A2,E2,L1,R3, R7,R8	NC	**(No Connection)** No connection
J7	VSSDL	**(DLL Ground)** DLL Ground
J1	VDDL	**(DLL Power Supply)** DLL Power Supply: 1.8V ± 0.1V.

Note: Input balls only BA0~BA2, A0~A15, /RAS, /CAS, /WE, /CS, CKE, ODT and /RESET do not supply termination.

Absolute Maximum Ratings

Symbol	Item	Rating		Units
V_{IN}, V_{OUT}	Input, Output Voltage	-0.5 ~ +2.3		V
V_{DD}	Power Supply Voltage	-1.0 ~ +2.3		V
V_{DDQ}	Power Supply Voltage	-0.5 ~ +2.3		V
VDDL	DLL Power Supply Voltage	-0.5 ~ +2.3		V
T_{OP}	Operating Temperature Range	Commercial	0 ~ +85	°C
T_{STG}	Storage Temperature Range	-55 ~ +100		°C
P_D	Power Dissipation	1		W

Note: Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification.

Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Units
V_{DD}	Power Supply Voltage	1.7	1.8	1.9	V
V_{DDL}	Power Supply for DLL Voltage	1.7	1.8	1.9	V
V_{DDQ}	Power Supply for I/O Voltage	1.7	1.8	1.9	V
V_{REF}	I/O Reference Voltage	0.49 x V_{DDQ}	0.5 x V_{DDQ}	0.51 x V_{DDQ}	V
V_{TT}	I/O Termination Voltage	V_{REF} - 0.04	V_{REF}	VREF + 0.04	V
V_{ID}	DC Differential Input Voltage	0.25	-	VDDQ + 0.6	V
V_{IH}	Input Logic High Voltage	V_{REF} + 0.125	-	VDDQ + 0.3	V
V_{IL}	Input Logic Low Voltage	-0.3	-	VREF - 0.125	V

Input / Output Capacitance

Symbol	Parameters	Min.	Max.	Unit
C_{CK}	Input Capacitance , CLK and /CLK	1.0	2.0	pF
CD_{CK}	Input Capacitance delta , CLK and /CLK	-	0.25	pF
C_I	Input Capacitance, all other input-only pins	1.0	1.75	pF
CD_I	Input Capacitance delta, all other input-only pins	-	0.25	pF
C_{IO}	Input/output Capacitance, DQ, LDM, UDM, LDQS,/LDQS , UDQS, /UDQS	2.5	3.5	pF
CD_{IO}	Input/output Capacitance delta, DQ, LDM, UDM,LDQS, /LDQS , UDQS, /UDQS	-	0.5	pF

Recommended DC Operating Conditions

Symbol	Parameter & Test Conditions	1066	800	667	Units	NOTES
		Max				
IDD0	**Operating Current - One Bank Active-Precharge** tCK = tCK(IDD), tRC = tRC (IDD), tRAS = tRASmin(IDD); CKE is HIGH, /CS is HIGH between valid commands; Address and control inputs are SWITCHING;Databus inputs are SWITCHING.	105	90	80	mA	1,2,3, 4,5,6
IDD1	**Operating Current - One Bank Active-Read-Precharge** IOUT = 0 mA;BL = 4, CL = CL(IDD), AL = 0;tCK = tCK(IDD), tRC = tRC(IDD), tRAS = tRASmin(IDD), tRCD = tRCD (IDD);CKE is HIGH, /CS is HIGH between valid commands; Address and control inputs are SWITCHING;Data bus inputs are SWITCHING.	115	100	90	mA	1,2,3, 4,5,6
IDD2P	**Precharge Power-Down Current** All banks idle;tCK = tCK(IDD); CKE is LOW;Other control and address inputs are STABLE; Data Bus inputs are FLOATING. (TCASE ≤ 85°C)	8	8	8	mA	1,2,3,4, 5,6,7
IDD2N	**Precharge Standby Current** All banks idle;tCK = tCK(IDD);CKE is HIGH, /CS is HIGH;Other control and address inputs are SWITCHING; Data bus inputs are SWITCHING.	50	45	40	mA	1,2,3, 4,5,6
IDD2Q	**Precharge Quiet Standby Current** All banks idle;tCK = tCK(IDD);CKE is HIGH, /CS is HIGH; Other control and address inputs are STABLE; Data bus inputs are FLOATING.	40	35	35	mA	1,2,3, 4,5,6

IDD3PF	**Active Power Down Current** All banks open; tCK = tCK(IDD); CKE is LOW; Other control and address input are STABLE; Data bus inputs are FLOATING. (TCASE≤85°C)	Fast PDN Exit MRS(12) = 0	15	15	15	mA	1,2,3, 4,5,6
IDD3PS		Slow PDN Exit MRS(12) = 1	12	12	12	mA	1,2,3,4, 5,6,7
IDD3N	**Active Standby Current** All banks open; tCK = tCK(IDD); tRAS = tRASmax(IDD), tRP = tRP(IDD); CKE is HIGH, /CS is HIGH between valid commands; Other control and address inputs are SWITCHING; Data bus inputs are SWITCHING.		75	65	60	mA	1,2,3, 4,5,6
IDD4R	**Operating Burst Read Current** All banks open, Continuous burst reads, IOUT = 0 mA; BL = 4, CL = CL(IDD), AL = 0; tCK = tCK(IDD); tRAS = tRASmax(IDD),tRP = tRP(IDD); CKE is HIGH, /CS is HIGH between valid commands; Address inputs are SWITCHING;Data Bus inputs are SWITCHING.		165	140	125	mA	1,2,3, 4,5,6
IDD4W	**Operating Burst Write Current** All banks open, Continuous burst writes;BL = 4, CL = CL (IDD), AL = 0;tCK = tCK(IDD); tRAS = tRASmax(IDD), tRP = tRP(IDD); CKE is HIGH, /CS is HIGH between valid commands;Address inputs are SWITCHING;Data Bus inputs are SWITCHING.		200	165	150	mA	1,2,3, 4,5,6

IDD5B	**Burst Refresh Current** tCK = tCK(IDD);Refresh command every tRFC(IDD) interval;CKE is HIGH, /CS is HIGH between valid commands;Other control and address inputs are SWITCHING; Data bus inputs are SWITCHING.	105	95	90	mA	1,2,3, 4,5,6
IDD6	**Self Refresh Current** CKE ≤ 0.2 V, external clock off, CLK and /CLK at 0 V;Other control and address inputs are FLOATING; Data bus inputs are FLOATING. (TCASE ≤ 85°C)	6	6	6	mA	1,2,3,4, 5,6,7
IDD7	**Operating Bank Interleave Read Current** All bank interleaving reads, IOU T = 0mA;BL = 4, CL = CL(IDD), AL = tRCD(IDD) - 1 x tCK(IDD);tCK = tCK(IDD),tRC = tRC(IDD), tRRD =tRRD(IDD), tFAW= tFAW(IDD), tRCD = tRCD(IDD);CKE is HIGH, /CS is HIGH between valid commands;Address bus inputs are STABLE during deselects;Data Bus inputs are SWITCHING.	245	200	180	mA	1,2,3, 4,5,6

Note 1: VDD = 1.8 V ± 0.1V; VDDQ = 1.8 V ± 0.1V.
Note 2: IDD specifications are tested after the device is properly initialized.
Note 3: Input slew rate is specified by AC Parametric Test Condition.
Note 4: IDD parameters are specified with ODT disabled.
Note 5: Data Bus consists of DQ, LDM, UDM, LDQS, /LDQS , UDQS and /UDQS
Note 6: Definitions for IDD

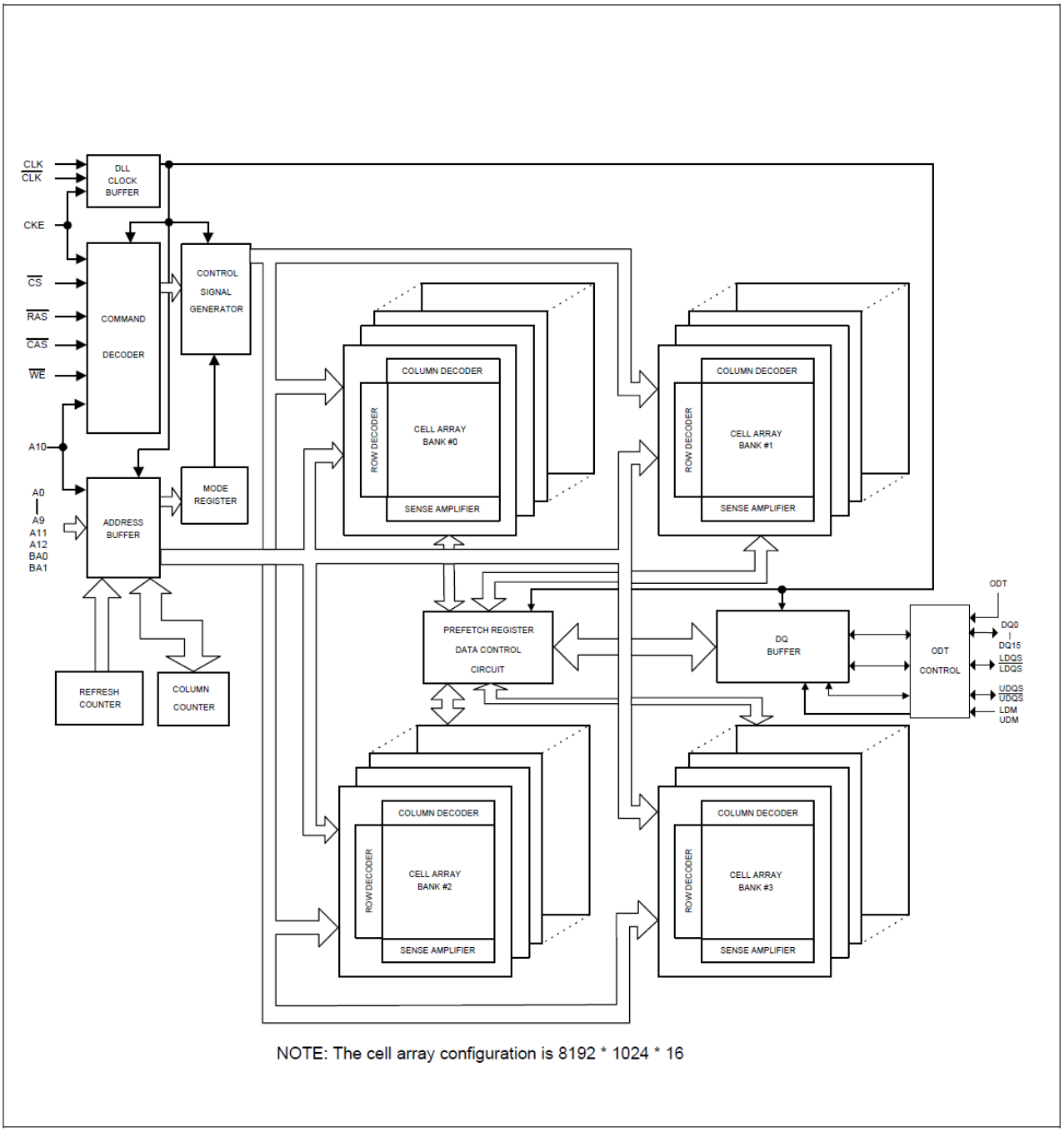
LOW = Vin ≤ VIL (ac) (max)
HIGH = Vin ≥ VIH (ac) (min)
STABLE = inputs stable at a HIGH or LOW level
FLOATING = inputs at VREF = VDDQ/2
SWITCHING = inputs changing between HIGH and LOW every other clock cycle (once per two clocks) for address and control signals, and inputs changing between HIGH and LOW every other data transfer (once per clock)for DQ signals not including masks or strobes.

Note 7: The following IDD values must be derated (IDD limits increase), when TCASE ≥ 85°C IDD2P must be derated by 20%;IDD3P(slow) must be derated by 30% and IDD6 must be derated by 80%. (IDD6 will increase by this amount if TCASE < 85°C and the 2X refresh option is still enabled)

Recommended DC Operating Conditions (Continued)

Symbol	Parameter	Test Conditions	Min.	Max.	Units
VOH	High Level Output Voltage	IO= -13.4mA	VTT+0.57		V
VOL	Low Level Output Voltage	IO= +13.4mA		VTT-0.57	V

Block Diagram



NOTE: The cell array configuration is 8192 * 1024 * 16

OCD Default Setting Table

Parameter	Min.	Typ.	Max.	Units
Output Impedance	-	-	-	Ω
Pull-up / Pull-down mismatch	0	-	4	Ω
Output Impedance step size for OCD calibration	0	-	1.5	Ω
Output Slew Rate	1.5	-	5.0	V/ns

AC Operating Test Conditions

Symbol	Parameter	Value	Units
VSWING (max.)	Input Signal Maximum Peak to Peak Swing	1.0	V
SLEW	Input Signal Minimum Slew Rate	1.0	V/ns
VREF	Input Reference Level	0.5*VDDQ	V

AC Operating Test Conditions

Symbol	Parameter	Min.	Max.	Units
VID	AC Differential Input Voltage	0.5	VDDQ+0.6	V
VIX	AC Differential Cross Point Input Voltage	0.5*VDDQ-0.175	0.5*VDDQ+0.175	V
VOX	AC Differential Cross Point Output Voltage	0.5*VDDQ-0.125	0.5*VDDQ+0.125	V
VIH	Input Logic High Voltage (DDR2-400/533)	VREF+0.25	-	V
VIH	Input Logic High Voltage (DDR2-667)	VREF+0.20	-	V
VIL	Input Logic High Voltage (DDR2-400/533)	-	VREF-0.25	V
VIL	Input Logic High Voltage (DDR2-667)	-	VREF-0.20	V

AC Operating Test Characteristics

DDR2-1066 Speed Bins

VDD/VDDQ = 1.8V±0.1V

Symbol	Speed Bin		-18/18I (DDR2-1066)		Units	Notes
	CL-tRCD-tRP		7-7-7			
	Parameter		Min.	Max.		
tRCD	Active to Read/Write Command Delay Time		13.125	-	ns	23
tRP	Precharge to Active Command Period		13.125	-	ns	23
tRC	Active to Ref/Active Command Period		58.125	-	ns	23
tRAS	Active to Precharge Command Period		45	70000	ns	4,23
tRFC	Auto Refresh to Active/Auto Refresh command period		105	-	ns	5
tRAFI	Average periodic refresh Interval	-40°C ≤ TCASE ≤ 85°C*		7.8	μs	5
		0°C ≤ TCASE ≤ 85°C	-	7.8	μs	5
		85°C < TCASE ≤ 95°C	-	3.9	μs	5,6
tCCD	/CAS to /CAS command delay		2	-	nCK	
tCK (AVG)	Average clock period	tCK(avg) @ CL=4	3.75	7.5	ns	30,31
		tCK(avg) @ CL=5	3	7.5	ns	30,31
		tCK(avg) @ CL=6	2.5	7.5	ns	30,31
		tCK(avg) @ CL=7	1.875	7.5	ns	30,31
tCH (AVG)	Average clock high pulse width		0.48	0.52	tCK(AVG)	30,31
tCL (AVG)	Average clock low pulse width		0.48	0.52	tCK(AVG)	30,31
tAC	DQ output access time from CLK/ /CLK		-350	350	ps	35
tDQSCK	DQS output access time from CLK / /CLK		-325	325	ps	35
tDQSQ	DQS-DQ skew for DQS & associated DQ signals		-	175	ps	13
tCKE	CKE minimum high and low pulse width		3		nCK	7
tRRD	Active to active command period for 2KB page size		10	-	ns	8,23
tFAW	Four Activate Window for 2KB page size		45	-	ns	23
tWR	Write recovery time		15	-	ns	23
tDAL	Auto-precharge write recovery + precharge time		WR + tnRP	-	nCK	24
tWTR	Internal Write to Read command delay		7.5	-	ns	9,23
tRTP	Internal Read to Precharge command delay		7.5	-	ns	4,23

AC Operating Test Characteristics

VDD/VDDQ = 1.8V±0.1V

Symbol	Speed Bin	-18/18I (DDR2-1066)		Units	Notes
	CL-tRCD-tRP	7-7-7			
	Parameter	Min.	Max.		
tIH (ref)	Address and control input hold time	325	-	ps	11,26,40,42,43
tIPW	Address and control input pulse width for each input	0.6	-	tCK(avg)	
tDQSS	DQS latching rising transitions to associated clock edges	-0.25	0.25	tCK(avg)	28
tDSS	DQS falling edge to CLK setup time	0.2	-	tCK(avg)	28
tDSH	DQS falling edge hold time from CLK	0.2	-	tCK(avg)	28
tDQSH	DQS input high pulse width	0.35	-	tCK(avg)	
tDQSL	DQS input low pulse width	0.35	-	tCK(avg)	

*** -40°C ≤ TCASE ≤ 85°C is for 18I grade only.**

AC Operating Test Characteristics

VDD/VDDQ = 1.8V±0.1V

Symbol	Speed Bin	-18/18I (DDR2-1066)		Units	Notes
	CL-tRCD-tRP	7-7-7			
	Parameter	Min.	Max.		
tWPRE	Write preamble	0.35	-	tCK(AVG)	
tWPST	Write preamble	0.4	0.6	tCK(AVG)	12
tRPRE	Read preamble	0.9	1.1	tCK(AVG)	14,36
tRPST	Read preamble	0.4	0.6	tCK(AVG)	14,37
DS(base)	DQ and DM input setup time	0	-	ps	16,27,29, 41,42,44
DH(base)	DQ and DM input hold time	75	-	ps	17,27,29, 41,42,44
tDS(ref)	DQ and DM input setup time	200	-	ps	16,27,29, 41,42,44
tDH(ref)	DQ and DM input hold time	200	-	ps	17,27,29, 41,42,44
tDIPW	DQ and DM input pulse width for each input	0.35	-	tCK(AVG)	
tHZ	Data-out high-impedance time from CLK/ /CLK	-	tAC,max	ps	15,35
tLZ(DQS)	DQS/ /DQS -low-impedance time from CLK/ /CLK	tAC,min	tAC,max	ps	15,35
tLZ(DQ)	DQ low-impedance time from CLK/ /CLK	2 x tAC,min	tAC,max	ps	15,35
tHP	Clock half pulse width	Min. (tCH(abs), tCL(abs))	-	ps	32
tQHS	Data hold skew factor	-	250	ps	33
tQH	DQ/DQS output hold time from DQS	tHP - tQHS	-	ps	34
tXSNR	Exit Self Refresh to a non-Read command	tRFC + 10	-	ns	23
tXSRD	Exit Self Refresh to a Read command	200	-	nCK	
tXP	Exit precharge power down to any command	3	-	nCK	
tXARD	Exit active power down to Read command	3	-	nCK	18
tXARDS	Exit active power down to Read command (slow exit, lower power)	10 - AL	-	nCK	18,19
tAOND	ODT turn-on delay	2	2	nCK	20
tAON	ODT turn-on	tAC,min	tAC,max + 2.575	ns	20,35

AC Operating Test Characteristics

VDD/VDDQ = 1.8V±0.1V

Symbol	Speed Bin	-18/18I (DDR2-1066)		Units	Notes
	CL-tRCD-tRP	7-7-7			
	Parameter	Min.	Max.		
tAONPD	ODT turn-on (Power Down mode)	tAC,min + 2	3 x tCK(avg) + tAC,max+1	ns	
tAOFD	ODT turn-off delay	2.5	2.5	nCK	21,39
tAOF	ODT turn-off	tAC,min	tAC,max + 0.6	ns	21,38,39
AOFPD	ODT turn-off (Power Down mode)	tAC,min + 2	2.5 x tCK(avg) + tAC,max + 1	ns	
tANPD	ODT to power down Entry Latency	4	-	nCK	
tAXPD	ODT Power Down Exit Latency	11		nCK	
tMRD	Mode Register Set command cycle time	2	-	nCK	
tMOD	MRS command to ODT update delay	0	12	ns	23
tOIT	OCD Drive mode output delay	0	12	ns	23
tDELAY	Minimum time clocks remain ON after CKE asynchronously drops LOW	tIS+tCK(avg)+tIH	-	ns	22

AC Operating Test Characteristics

DDR2-800 & DDR2-667 Speed Bins

VDD/VDDQ = 1.8V±0.1V

Symbol	Speed Bin		-25/25L/25I (DDR2-800)		-3 (DDR2-667)		Units	Notes
	CL-tRCD-tRP		6-6-6		5-5-5			
	Parameter		Min.	Max.	Min.	Max.		
tRCD	Active to Read/Write Command Delay Time		12.5	-	15	-	ns	23
tRP	Precharge to Active Command Period		12.5	-	15	-	ns	23
tRC	Active to Ref/Active Command Period		57.5	-	60	-	ns	23
tRAS	Active to Precharge Command Period		45	70000	45	70000	ns	4,23
tRFC	Auto Refresh to Active/Auto Refresh command period		105	-	105	-	ns	5
tREFI	Average periodic refresh Interval	-40°C ≤ TCASE ≤ 85°C*	-	7.8	-	-	µs	5
		0°C < TCASE ≤ 85°C		7.8	-	7.8	µs	5
		85°C < TCASE ≤ 95°C	-	3.9	-	3.9	µs	5,6
tCCD	/CAS to /CAS command delay		2	-	2	-	nCK	
tCK(avg)	Average clock period	tCK(avg) @ CL=3	5	8	5	8	ns	30,31
		tCK(avg) @ CL=4	3.75	8	3.75	8	ns	30,31
		tCK(avg) @ CL=5	2.5	8	3	8	ns	30,31
		tCK(avg) @ CL=6	2.5	8	-	-	ns	30,31
tCH(avg)	Average clock high pulse width		0.48	0.52	0.48	0.52	tCK (AVG)	30,31
tCL(avg)	Average clock low pulse width		0.48	0.52	0.48	0.52	tCK (AVG)	30,31
tAC	DQ output access time from CLK/ /CLK		-400	400	-450	450	ps	35
tDQSCK	DQS output access time from CLK / /CLK		-350	350	-400	400	ps	35
tDQSQ	DQS-DQ skew for DQS & associated DQ signals		-	200	-	240	ps	13
tCKE	CKE minimum high and low pulse width		3	-	3	-	nCK	7
tRRD	Active to active command period for 2KB page size		10	-	10	-	ns	8,23
tFAW	Four Activate Window for 2KB page size		45	-	50	-	ns	23
tWR	Write recovery time		15	-	15	-	ns	23
tDAL	Auto-precharge write recovery + precharge time		WR + tnRP	-	WR + tnRP	-	nCK	24

AC Operating Test Characteristics

VDD/VDDQ = 1.8V±0.1V

Symbol	Speed Bin	-25/25L/25I (DDR2-800)		-3 (DDR2-667)		Units	Notes
	CL-tRCD-tRP	6-6-6		5-5-5			
	Parameter	Min.	Max.	Min.	Max.		
tWTR	Internal Write to Read command delay	7.5	-	7.5	-	ns	9,23
tRTP	Internal Read to Precharge command delay	7.5	-	7.5	-	ns	4,23
tIS (base)	Address and control input setup time	175	-	200	-	ps	10,26, 40,42,43
tIH (base)	Address and control input hold time	250	-	275	-	ps	11,26, 40,42,43
tIS (ref)	Address and control input setup time	375	-	400	-	ps	10,26, 40,42,43
tIH (ref)	Address and control input hold time	375	-	400	-	ps	11,26, 40,42,43
tIPW	Address and control input pulse width for each input	0.6	-	0.6	-	tCK (AVG)	
tDQSS	DQS latching rising transitions to associated clock edges	-0.25	0.25	-0.25	0.25	tCK (AVG)	28
tDSS	DQS falling edge to CLK setup time	0.2	-	0.2	-	tCK (AVG)	28
tDSH	DQS falling edge hold time from CLK	0.2	-	0.2	-	tCK (AVG)	28
tDQSH	DQS input high pulse width	0.35	-	0.35	-	tCK (AVG)	
tDQSL	DQS input low pulse width	0.35	-	0.35	-	tCK (AVG)	

* -40°C ≤ TCASE ≤ 85°C is for 25I grade only.

AC Operating Test Characteristics

VDD/VDDQ = 1.8V±0.1V

Symbol	Speed Bin	-25/25L/25I (DDR2-800)		-3 (DDR2-667)		Units	Notes
	CL-tRCD-tRP	6-6-6		5-5-5			
	Parameter	Min.	Max.	Min.	Max.		
tWPRE	Write preamble	0.35	-	0.35	-	tCK (AVG)	
tWPST	Write postamble	0.4	0.6	0.4	0.6	tCK (AVG)	12
tRPRE	Read preamble	0.9	1.1	0.9	1.1	tCK (AVG)	14,36
tRPST	Read postamble	0.4	0.6	0.4	0.6	tCK (AVG)	14,37
tDS(base)	DQ and DM input setup time	50	-	100	-	ps	16,27,29, 41,42,44
tDH(base)	DQ and DM input hold time	125	-	175	-	ps	17,27,29, 41,42,44
tDS(ref)	DQ and DM input setup time	250	-	300	-	ps	16,27,29, 41,42,44
tDH(ref)	DQ and DM input hold time	250	-	300	-	ps	17,27,29, 41,42,44
tDIPW	DQ and DM input pulse width for each input	0.35	-	0.35	-	tCK (AVG)	
tHZ	Data-out high-impedance time from CLK/ /CLK	-	tAC,max	-	tAC,max	ps	15,35
tLZ(DQS)	DQS/ /DQS -low-impedance time from CLK/ /CLK	tAC,min	tAC,max	tAC,min	tAC,max	ps	15,35
tLZ(DQ)	DQ low-impedance time from CLK/ /CLK	2 x tAC,min	tAC,max	2 x tAC,min	tAC,max	ps	15,35
tHP	Clock half pulse width	Min. (tCH(abs), tCL(abs))		Min. (tCH(abs), tCL(abs))		ps	32
tQHS	Data hold skew factor	-	300	-	340	ps	33
tQH	DQ/DQS output hold time from DQS	tHP-tQHS	-	tHP-tQHS	-	ps	34
tXSNR	Exit Self Refresh to a non-Read command	tRFC+10	-	tRFC+10	-	ns	23
tXSRD	Exit Self Refresh to a Read command	200	-	200	-	nCK	

AC Operating Test Characteristics

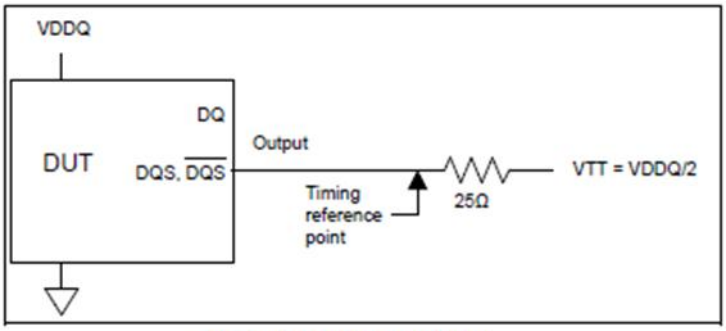
VDD/VDDQ = 1.8V±0.1V

Symbol	Speed Bin	-25/25L/25I (DDR2-800)		-3 (DDR2-667)		Units	Notes
	CL-tRCD-tRP	6-6-6		5-5-5			
	Parameter	Min.	Max.	Min.	Max.		
tXP	Exit precharge power down to any command	2	-	2	-	nCK	
tXARD	Exit active power down to Read command	2	-	2	-	nCK	18
tXARDS	Exit active power down to Read command (slow exit, lower power)	8 - AL	-	7 - AL	-	nCK	18,19
tAOND	ODT turn-on delay	2	2	2	2	nCK	20
tAON	ODT turn-on	tAC,min	tAC,max+ 0.7	tAC,min	tAC,max+ 0.7	ns	20,35
tAONPD	ODT turn-on (Power Down mode)	tAC,min + 2	2 x tCK(avg)+ tAC,max+ 1	tAC,min + 2	2 x tCK(avg)+ tAC,max+ 1	ns	
tAOFD	ODT turn-off delay	2.5	2.5	2.5	2.5	nCK	21,39
tAOF	ODT turn-off	tAC,min	tAC,max+ 0.6	tAC,min	tAC,max+ 0.6	ns	21,38,39
tAOFPD	ODT turn-off (Power Down mode)	tAC,min + 2	2.5xtCK (avg)+tAC, max+1	tAC,min + 2	2.5xtCK (avg)+tAC, max+1	ns	
tANPD	ODT to power down Entry Latency	3	-	3	-	nCK	
tAXPD	ODT Power Down Exit Latency	8		8		nCK	
tMRD	Mode Register Set command cycle time	2	-	2	-	nCK	
tMOD	MRS command to ODT update delay	0	12	0	12	ns	23
tOIT	OCD Drive mode output delay	0	12	0	12	ns	23
tDELAY	Minimum time clocks remain ON after CKE asynchronously drops LOW	tIS+tCK (avg)+tIH	-	tIS+tCK (avg)+tIH	-	ns	22

Note 1: All voltages are referenced to VSS.

Note 2: Tests for AC timing, IDD, and electrical AC and DC characteristics may be conducted at nominal reference/supply voltage levels, but the related specifications and device operation are guaranteed for the full voltage range specified. ODT is disabled for all measurements that are not ODT-specific.

Note 3: AC timing reference load:



AC timing reference load

Note 4: This is a minimum requirement. Minimum read to precharge timing is AL + BL / 2 provided that the tRTP and tRAS(min) have been satisfied.

Note 5: If refresh timing is violated, data corruption may occur and the data must be re-written with valid data before a valid READ can be executed.

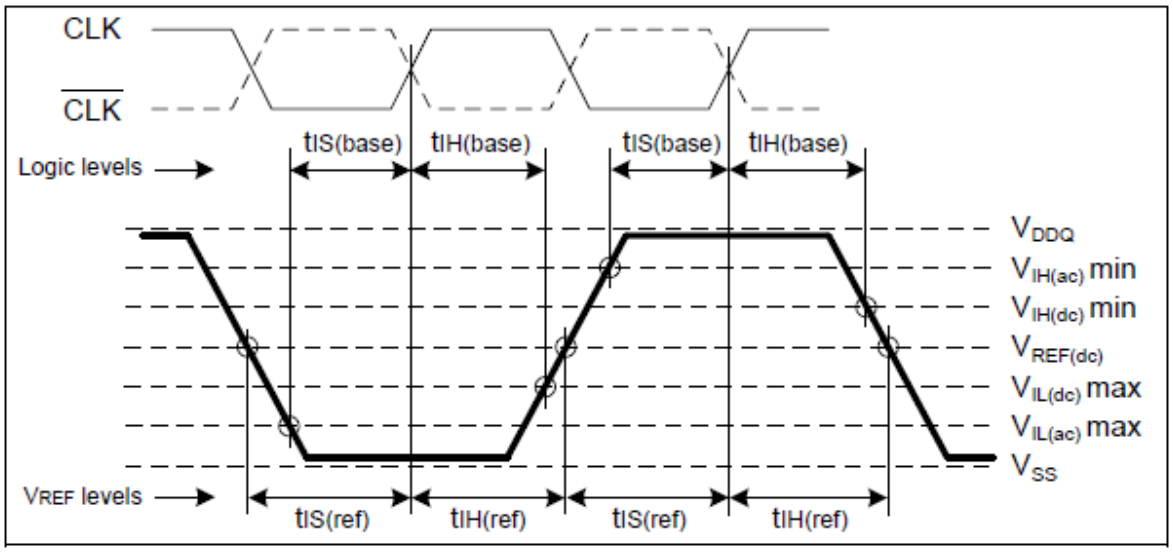
Note 6: This is an optional feature. For detailed information, please refer to **"Operating Temperature Condition"** section 10.2 in this data sheet.

Note 7: tCKE min of 3 clocks means CKE must be registered on three consecutive positive clock edges. CKE must remain at the valid input level the entire time it takes to achieve the 3 clocks of registration. Thus, after any CKE transition, CKE may not transition from its valid level during the time period of tIS + 2 x tCK + tIH.

Note 8: A minimum of two clocks (2 * nCK) is required irrespective of operating frequency.

Note 9: tWTR is at least two clocks (2 * nCK) independent of operation frequency.

Note 10: There are two sets of values listed for Command/Address input setup time: tIS(base) and tIS(ref). The tIS(ref) value (for reference only) is equivalent to the baseline value of tIS(base) at VREF when the slew rate is 1.0 V/nS. The baseline value tIS(base) is the JEDEC defined value, referenced from the input signal crossing at the VIH(ac) level for a rising signal and VIL(ac) for a falling signal applied to the device under test. See Figure 17. If the Command/Address slew rate is not equal to 1.0 V/nS, then the baseline values must be derated by adding the values from table of tIS/tIH derating values for DDR2-667, DDR2-800 and DDR2-1066



Differential input waveform timing – tIS and tIH

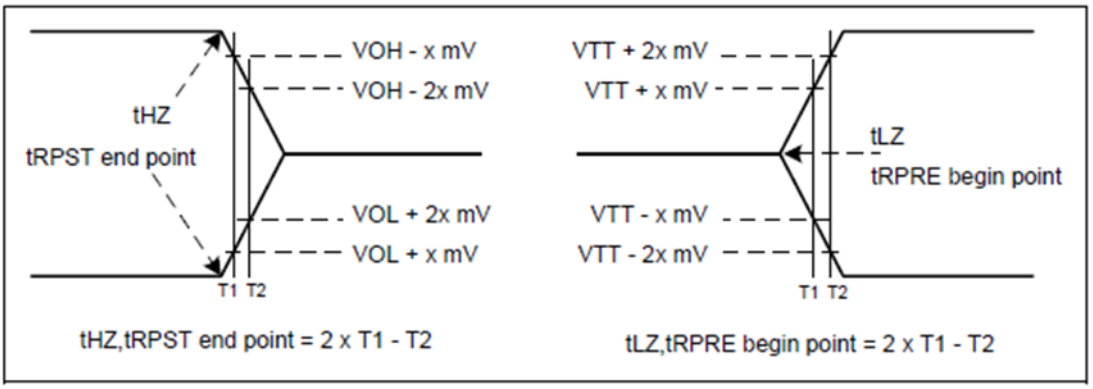
Note 11: There are two sets of values listed for Command/Address input hold time: tIH(base) and tIH(ref). The tIH(ref) value (for reference only) is equivalent to the baseline value of tIH(base) at VREF when the slew rate is 1.0 V/nS. The baseline value tIH(base) is the JEDEC defined value, referenced from the input signal crossing at the VIL(dc) level for a rising signal and VIH(dc) for a falling signal applied to the device under test. See Figure 17. If the Command/Address slew rate is not equal to 1.0 V/nS, then the baseline values must be derated by adding the values from table tIS/tIH derating values for DDR2-667, DDR2-800 and DDR2-1066

Note 12: The maximum limit for the tWPST parameter is not a device limit. The device operates with a greater value for this parameter, but system performance (bus turnaround) will degrades accordingly.

Note 13: tDQSQ: Consists of data pin skew and output pattern effects, and p-channel to n-channel variation of the output drivers as well as output Slew Rate mismatch between DQS / DQS and associated DQ in any given cycle.

Note 14: tRPST end point and tRPRE begin point are not referenced to a specific voltage level but specify when the device output is no longer driving (tRPST), or begins driving (tRPRE). Figure 18 shows a method to calculate these points when the device is no longer driving (tRPST), or begins driving (tRPRE) by measuring the signal at two different voltages. The actual voltage measurement points are not critical as long as the calculation is consistent.

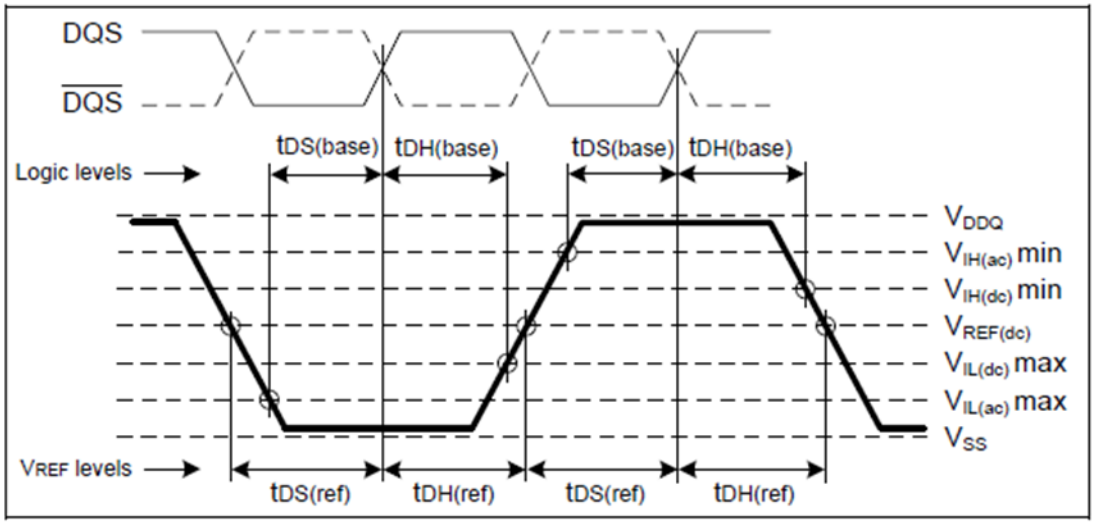
Note 15: tHZ and tLZ transitions occur in the same access time as valid data transitions. These parameters are referenced to a specific voltage level which specifies when the device output is no longer driving (tHZ), or begins driving (tLZ). Figure 18 shows a method to calculate the point when device is no longer driving (tHZ), or begins driving (tLZ) by measuring the signal at two different voltages. The actual voltage measurement points are not critical as long as the calculation is consistent. tLZ(DQ) refers to tLZ of the DQ's and tLZ(DQS) refers to tLZ of the (UDQS, LDQS,/UDQS and /LDQS) each treated as single-ended signal.



Method for calculating transitions and endpoints

Note 16: Input waveform timing tDS with differential data strobe enabled MR[bit10]=0. There are two sets of values listed for DQ and DM input setup time: tDS(base) and tDS(ref). The tDS(ref) value (for reference only) is equivalent to the baseline value tDS(base) at VREF when the slew rate is 2.0 V/nS, differentially. The baseline value tDS(base) is the JEDEC defined value, referenced from the input signal crossing at the VIH(ac) level to the differential data strobe crosspoint for a rising signal, and from the input signal crossing at the VIL(ac) level to the differential data strobe crosspoint for a falling signal applied to the device under test. DQS, /DQS signals must be monotonic between VIL(dc)max and VIH(dc)min. If the differential DQS slew rate is not equal to 2.0 V/nS, then the baseline values must be derated by adding the values from table of DDR2-667, DDR2-800 and DDR2-1066 tDS/tDH derating with differential data strobe

Note 17: Input waveform timing tDH with differential data strobe enabled MR[bit10]=0. There are two sets of values listed for DQ and DM input hold time: tDH(base) and tDH(ref). The tDH(ref) value (for reference only) is equivalent to the baseline value tDH(base) at VREF when the slew rate is 2.0 V/nS, differentially. The baseline value tDH(base) is the JEDEC defined value, referenced from the differential data strobe crosspoint to the input signal crossing at the VIH(dc) level for a falling signal and from the differential data strobe crosspoint to the input signal crossing at the VIL(dc) level for a rising signal applied to the device under test. DQS, /DQS signals must be monotonic between VIL(dc)max and VIH(dc)min. If the differential DQS slew rate is not equal to 2.0 V/nS, then the baseline values must be derated by adding the values from table of DDR2-667, DDR2-800 and DDR2-1066 tDS/tDH derating with differential data strobe



Differential input waveform timing – tDS and tDH

Note 18: User can choose which active power down exit timing to use via MRS (bit 12). tXARD is expected to be used for fast active power down exit timing. tXARDS is expected to be used for slow active power down exit timing.

Note 19: AL = Additive Latency.

Note 20: ODT turn on time min is when the device leaves high impedance and ODT resistance begins to turn on. ODT turn on time max is when the ODT resistance is fully on. Both are measure from tAOND, which is interpreted differently per speed bin. For DDR2-667/800/1066, tAOND is 2 clock cycles after the clock edge that registered a first ODT HIGH counting the actual input clock edges.

Note 21: ODT turn off time min is when the device starts to turn off ODT resistance. ODT turn off time max is when the bus is in high impedance. Both are measured from tAOFD, which is interpreted as 0.5 x tCK(avg) [nS] after the second trailing clock edge counting from the clock edge that registered a first ODT LOW and by counting the actual input clock edges. For DDR2-667/800: If tCK(avg) = 3 nS is assumed, tAOFD is 1.5 nS (= 0.5 x 3 nS) after the second trailing clock edge counting from the clock edge that registered a first ODT LOW and by counting the actual input clock edges. For DDR2-1066: tAOFD is 0.9375 [nS] (= 0.5 x 1.875 [nS]) after the second trailing clock edge counting from the clock edge that registered a first ODT LOW and by counting the actual input clock edges.

Note 22: The clock frequency is allowed to change during Self Refresh mode or precharge power-down mode. In case of clock frequency change during precharge power-down, a specific procedure is required as described in section 8.10.

Note 23: For these parameters, the DDR2 SDRAM device is characterized and verified to support tnPARAM = RU{tPARAM / tCK(avg)}, which is in clock cycles, assuming all input clock jitter specifications are satisfied.

Examples:

The device will support tnRP = RU{tRP / tCK(avg)}, which is in clock cycles, if all input clock jitter specifications are met. This means: For DDR2-667 5-5-5, of which tRP = 15nS, the device will support tnRP = RU{tRP / tCK(avg)} = 5, i.e. as long as the input clock jitter specifications are met, Precharge command at Tm and Active command at Tm+5 is valid even if (Tm+5 - Tm) is less than 15nS due to input clock jitter. For DDR2-1066 7-7-7, of which tRP = 13.125 nS, the device will support tnRP = RU{tRP / tCK(avg)} = 7, i.e. as long as the input clock jitter specifications are

met, Precharge command at Tm and Active command at Tm+7 is valid even if (Tm+7 - Tm) is less than 13.125 nS due to input clock jitter.

Note 24: tDAL [nCK] = WR [nCK] + tnRP [nCK] = WR + RU {tRP [pS] / tCK(avg) [pS] }, where WR is the value programmed in the mode register set and RU stands for round up.

Example:

For DDR2-1066 7-7-7 at tCK(avg) = 1.875 nS with WR programmed to 8 nCK, tDAL = 8 + RU {13.125 nS / 1.875 nS} [nCK] = 8 + 7 [nCK] = 15 [nCK].

Note 25: New units, 'tCK(avg)' and 'nCK', are introduced in DDR2-667, DDR2-800 and DDR2-1066. Unit 'tCK(avg)' represents the actual tCK(avg) of the input clock under operation. Unit 'nCK' represents one clock cycle of the input clock, counting the actual clock edges.

Examples:

For DDR2-667/800: tXP = 2 [nCK] means; if Power Down exit is registered at Tm, an Active command may be registered at Tm+2, even if (Tm+2 - Tm) is 2 x tCK(avg) + tERR(2per),min.

For DDR2-1066: tXP = 3 [nCK] means; if Power Down exit is registered at Tm, an Active command may be registered at Tm+3, even if (Tm+3 - Tm) is 3 x tCK(avg) + tERR(3per),min.

Note 26: These parameters are measured from a command/address signal (CKE, /CS , /RAS , /CAS , /WE, ODT, BA0, A0, A1, etc.) transition edge to its respective clock signal (CLK/ /CLK) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. tJIT(per), tJIT(cc), etc.), as the setup and hold are relative to the clock signal crossing that latches the command/address. That is, these parameters should be met whether clock jitter is present or not.

Note 27: If tDS or tDH is violated, data corruption may occur and the data must be re-written with valid data before a valid READ can be executed.

Note 28: These parameters are measured from a data strobe signal ((L/U)DQS/ /DQS) crossing to its respective clock signal (CLK/ /CLK) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. tJIT(per), tJIT(cc), etc.), as these are relative to the clock signal crossing. That is, these parameters should be met whether clock jitter is present or not.

Note 29: These parameters are measured from a data signal ((L/U)DM, (L/U)DQ0, (L/U)DQ1, etc.) transition edge to its respective data strobe signal ((L/U)DQS/ /DQS) crossing.

Note 30: Input clock jitter spec parameter. These parameters and the ones in the table below are referred to as 'input clock jitter spec parameters'. The jitter specified is a random jitter meeting a Gaussian distribution.

Input clock-Jitter specifications parameters for DDR2-667, DDR2-800 and DDR2-1066

PARAMETER	SYMBOL	DDR2-667		DDR2-800		DDR2-1066		UNIT
		Min.	Max.	Min.	Max.	Min.	Max.	
Clock period jitter	Duty cycle jitter	-125	125	-100	100	-90	90	ps
Clock period jitter during DLL locking period	tJIT(per,lck)	-100	100	-80	80	-80	80	ps
Cycle to cycle clock period	tJIT(cc)	-250	250	-200	200	-180	180	ps
Cycle to cycle clock period jitter during DLL locking period	tJIT(cc,lck)	-200	200	-160	160	-160	160	ps
Cumulative error across 2 cycles	tERR(2per)	-175	175	-150	150	-132	132	ps
Cumulative error across 3 cycles	tERR(3per)	-225	225	-175	175	-157	157	ps

Cumulative error across 4 cycles	tERR(4per)	-250	250	-200	200	-157	157	ps
Cumulative error across 5 cycles	tERR(5per)	-250	250	-200	200	-188	188	ps
Cumulative error across n cycles, n = 6 ... 10, inclusive	tERR(6-10per)	-350	350	-300	300	-250	250	ps
Cumulative error across n cycles, n = 11 ... 50, inclusive	tERR(11-50per	-450	450	-450	450	-425	425	ps
Duty cycle jitter	tJIT(duty)	-125	125	-100	100	-75	75	ps

Note 31: These parameters are specified per their average values, however it is understood that the following relationship between the average timing and the absolute instantaneous timing holds at all times. (Min and max of SPEC values are to be used for calculations in the table below.)

Parameter	SYMBOL	Min.	Max.	Units
Absolute clock period	tCK(abs)	tCK(avg),min+tJIT(per),min	tCK(avg),max + tJIT(per),max	ps
Absolute clock HIGH pulse width	tCH(abs)	tCH(avg),min x tCK(avg),min + tJIT(duty),min	tCH(avg),max x tCK(avg),max + tJIT(duty),max	ps
Absolute clock LOW pulse width	tCL(abs)	tCL(avg),min x tCK(avg),min + tJIT(duty),min	tCL(avg),max x tCK(avg),max + tJIT(duty),max	ps

Note 32: tHP is the minimum of the absolute half period of the actual input clock. tHP is an input parameter but not an input specification parameter. It is used in conjunction with tQHS to derive the DRAM output timing tQH. The value to be used for tQH calculation is determined by the following equation;
tHP = Min (tCH(abs), tCL(abs)), where, tCH(abs) is the minimum of the actual instantaneous clock HIGH time; tCL(abs) is the minimum of the actual instantaneous clock LOW time;

Note 33: tQHS accounts for:

1) The pulse duration distortion of on-chip clock circuits, which represents how well the actual tHP at the input is transferred to the output; and
2) The worst case push-out of DQS on one transition followed by the worst case pull-in of DQ on the next transition, both of which are independent of each other, due to data pin skew, output pattern effects, and p-channel to nchannel variation of the output drivers

Note 34: tQH = tHP – tQHS, where:
tHP is the minimum of the absolute half period of the actual input clock; and tQHS is the specification value under the max column. {The less half-pulse width distortion present, the larger the tQH value is; and the larger the valid data eye will be.} Examples:

1) If the system provides tHP of 1315 pS into a DDR2-667 SDRAM, the DRAM provides tQH of 975 pS minimum.
2) If the system provides tHP of 1420 pS into a DDR2-667 SDRAM, the DRAM provides tQH of 1080 pS minimum.
3) If the system provides tHP of 825 pS into a DDR2-1066 SDRAM, the DRAM provides tQH of 575 pS minimum.
4) If the system provides tHP of 900 pS into a DDR2-1066 SDRAM, the DRAM provides tQH of 650 pS minimum.

Note 35: When the device is operated with input clock jitter, this parameter needs to be derated by the actual tERR(6-10per) of the input clock. (output deratings are relative to the SDRAM input clock.) Examples:
1) If the measured jitter into a DDR2-667 SDRAM has tERR(6-10per),min = - 272 pS andtERR (6-10per),max = + 293 pS, then tDQSCK,min(derated) = tDQSCK,min - tERR(6-10per),max = - 400 pS - 293 pS = - 693 pS and tDQSCK,max(derated) = tDQSCK,max - tERR(6-10per),min = 400 pS + 272 pS = + 672 pS. Similarly, tLZ(DQ) for DDR2-667 derates to tLZ(DQ),min(derated) = - 900 pS - 293 pS = - 1193 pS and tLZ(DQ),max(derated) = 450 pS + 272 pS = + 722 pS. (Caution on the min/max usage!)
2) If the measured jitter into a DDR2-1066 SDRAM has tERR(6-10per),min = - 202 pS and tERR (6-10per),max = + 223 pS, then tDQSCK,min(derated) = tDQSCK,min - tERR(6-10per),max = - 300 pS - 223 pS = - 523 pS and tDQSCK,max(derated) = tDQSCK,max - tERR(6-10per),min = 300 pS + 202 pS = + 502 pS. Similarly, tLZ(DQ) for DDR2-1066 derates to tLZ(DQ),min(derated) = - 700 pS – 223 pS = - 923 pS and tLZ(DQ),max(derated) = 350 pS + 202 pS = + 552 pS. (Caution on the min/max usage!)

Note 36: When the device is operated with input clock jitter, this parameter needs to be derated by the actual tJIT(per) of the input clock. (output deratings are relative to the SDRAM input clock.) Examples:
1) If the measured jitter into a DDR2-667 SDRAM has tJIT(per),min = - 72 pS and tJIT(per),max = + 93 pS, then tRPRE,min(derated) = tRPRE,min + tJIT(per),min = 0.9 x tCK(avg) - 72 pS = + 2178 pS and tRPRE,max(derated) = tRPRE,max + tJIT(per),max = 1.1 x tCK(avg) + 93 pS = + 2843 pS. (Caution on the min/max usage!)
2) If the measured jitter into a DDR2-1066 SDRAM has tJIT(per),min = - 72 pS and tJIT(per),max = + 63 pS, then tRPRE,min(derated) = tRPRE,min + tJIT(per),min = 0.9 x tCK(avg) - 72 pS = + 1615.5 pS and tRPRE,max(derated)= tRPRE,max + tJIT(per),max = 1.1 x tCK(avg) + 63 pS = + 2125.5 pS. (Caution on the min/max usage!)

Note 37: When the device is operated with input clock jitter, this parameter needs to be derated by the actual tJIT(duty) of the input clock. (output deratings are relative to the SDRAM input clock.) Examples:
1) If the measured jitter into a DDR2-800 SDRAM has tJIT(duty),min = - 72 pS and tJIT(duty),max = + 93 pS, then tRPST,min(derated) = tRPST,min + tJIT(duty),min = 0.4 x tCK(avg) - 72 pS = + 928 pS and tRPST,max(derated) = tRPST,max + tJIT(duty),max = 0.6 x tCK(avg) + 93 pS = + 1593 pS. (Caution on the min/max usage!)
2) If the measured jitter into a DDR2-1066 SDRAM has tJIT(duty),min = - 72 pS and tJIT(duty),max = + 63 pS, then tRPST,min(derated) = tRPST,min + tJIT(duty),min = 0.4 x tCK(avg) - 72 pS = + 678 pS and tRPST,max(derated) = tRPST,max + tJIT(duty),max = 0.6 x tCK(avg) + 63 pS = + 1188 pS. (Caution on the min/max usage!)

Note 38: When the device is operated with input clock jitter, this parameter needs to be derated by { -tJIT(duty), max - tERR(6- 10per),max } and { - tJIT(duty),min - tERR(6-10per),min } of the actual input clock. (output deratings are relative to the SDRAM input clock.) Examples:
1) If the measured jitter into a DDR2-667 SDRAM has tERR(6-10per),min = - 272 pS, tERR(6-10per), max = + 293 pS, tJIT(duty),min = - 106 pS and tJIT(duty),max = + 94 pS, then tAOF,min(derated) = tAOF,min + { - tJIT(duty),max - tERR(6-10per),max } = - 450 pS + { - 94 pS - 293 pS} = - 837 pS and tAOF,max(derated) = tAOF,max + { - tJIT(duty),min - tERR(6-10per),min } = 1050 pS + { 106 pS + 272 pS } = + 1428 pS. (Caution on the min/max usage!)
2) If the measured jitter into a DDR2-1066 SDRAM has tERR(6-10per),min = - 202 pS, tERR(6-10per), max = + 223 pS, tJIT(duty),min = - 66 pS and tJIT(duty),max = + 74 pS, then tAOF,min(derated) = tAOF,min + { - tJIT(duty),max - tERR(6-10per),max } = - 350 pS + { - 74 pS - 223 pS} = - 647 pS and

tAOF,max(derated) = tAOF,max + { - tJIT(duty),min - tERR(6-10per),min } = 950 pS + { 66 pS + 202 pS } = + 1218 pS. (Caution on the min/max usage!)

Note 39: For tAOFD of DDR2-667/800/1066, the 1/2 clock of nCK in the 2.5 x nCK assumes a tCH(avg), average input clock HIGH pulse width of 0.5 relative to tCK(avg). tAOF,min and tAOF,max should each be derated by the same amount as the actual amount of tCH(avg) offset present at the DRAM input with respect to 0.5. Example:

If an input clock has a worst case tCH(avg) of 0.48, the tAOF,min should be derated by subtracting 0.02 x tCK(avg) from it, whereas if an input clock has a worst case tCH(avg) of 0.52, the tAOF,max should be derated by adding 0.02 x tCK(avg) to it. Therefore, we have; tAOF,min(derated) = tAC,min - [0.5 – Min (0.5, tCH(avg),min)] x tCK(avg) tAOF,max(derated) = tAC,max + 0.6 + [Max(0.5, tCH(avg),max) - 0.5] x tCK(avg)

or

tAOF,min(derated) = Min(tAC,min, tAC,min - [0.5 - tCH(avg),min] x tCK(avg))tAOF,max(derated) = 0.6 + Max(tAC,max, tAC,max + [tCH(avg),max - 0.5] x tCK(avg)) where tCH(avg),min and tCH(avg),max are the minimum and maximum of tCH(avg) actually measured at the DRAM input balls. Note that these deratings are in addition to the tAOF derating per input clock jitter, i.e. tJIT(duty) and tERR(6-10per). However tAC values used in the equations shown above are from the timing parameter table and are not derated. Thus the final derated values for tAOF are; tAOF,min(derated_final) = tAOF,min(derated) + { - tJIT(duty),max - tERR(6-10per),max } tAOF,max(derated_final) = tAOF,max(derated) + { - tJIT(duty) ,min - tERR(6-10per),min }

Note 40: Timings are specified with command/address input slew rate of 1.0 V/nS.

Note 41: Timings are specified with DQs and DM input slew rate of 1.0V/nS.

Note 42: Timings are specified with CLK/ /CLK differential slew rate of 2.0 V/nS. Timings are guaranteed for DQS signals with a differential slew rate of 2.0 V/nS in differential strobe mode.

Note 43: tIS and tIH (input setup and hold) derating.

Command/ Address Slew Rate (V/nS)	Δ tIS and ΔtIH Derating Values for DDR2-667, DDR2-800 and DDR2-1066						
	CLK/ /CLK Differential Slew Rate						
	2.0 V/nS		1.5 V/nS		1.0 V/nS		Unit
	Δ tIS	Δ tIH	Δ tIS	Δ tIH	Δ tIS	Δ tIH	
4.0	+150	+94	+180	+124	+210	+154	ps
3.5	+143	+89	+173	+119	+203	+149	ps
3.0	+133	+83	+163	+113	+193	+143	ps
2.5	+120	+75	+150	+105	+180	+135	ps
2,0	+100	+45	+130	+75	+160	+105	ps
1.5	+67	+21	+97	+51	+127	+81	ps
1.0	0	0	+30	+30	+60	+60	ps
0.9	-5	-14	+25	+16	+55	+46	ps
0.8	-13	-31	+17	-1	+47	+29	ps
0.7	-22	-54	+8	-24	+38	+6	ps
0.6	-34	-83	-4	-53	+26	-23	ps
0.5	-60	-125	-30	-95	0	-65	ps
0.4	-100	-188	-70	-158	-40	-128	ps
0.3	-168	-292	-138	-262	-108	-232	ps
0.25	-200	-375	-170	-345	-140	-315	ps

0.2	-325	-500	-295	-470	-265	-440	ps
0.15	-517	-708	-487	-678	-457	-648	ps
0.1	-1000	-1125	-970	-1095	-940	-1065	ps

For all input signals the total tIS (setup time) and tIH (hold time) required is calculated by adding the data sheet tIS(base) and tIH(base) value to the ΔtIS and ΔtIH derating value respectively. Example: tIS (total setup time) = tIS(base) + ΔtIS.

Setup (tIS) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of VREF(dc) and the first crossing of VIH(ac)min. Setup (tIS) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of VREF(dc) and the first crossing of VIL(ac)max. If the actual signal is always earlier than the nominal slew rate line between shaded 'VREF(dc) to AC region', use nominal slew rate for derating value. See Figure 1 Illustration of nominal slew rate for tIS. If the actual signal is later than the nominal slew rate line anywhere between shaded 'VREF(dc) to AC region', the slew rate of a tangent line to the actual signal from the AC level to DC level is used for derating value. See Figure 2 Illustration of tangent line for tIS.

Hold (tIH) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of VIL (dc)max and the first crossing of VREF(dc). Hold (tIH) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of VIH(dc)min and the first crossing of VREF(dc). If the actual signal is always later than the nominal slew rate line between shaded 'DC to VREF(dc) region', use nominal slew rate for derating value. See Figure 3 Illustration of nominal slew rate for tIH. If the actual signal is earlier than the nominal slew rate line anywhere between shaded 'DC to VREF(dc) region', the slew rate of a tangent line to the actual signal from the DC level to VREF(dc) level is used for derating value. See Figure 4 Illustration of tangent line for tIH.

Although for slow slew rates the total setup time might be negative (i.e. a valid input signal will not have reached VIH/IL(ac) at the time of the rising clock transition) a valid input signal is still required to complete the transition and reach VIH/IL(ac). For slew rates in between the values listed in above tIS/tIH derating values for DDR2-667, DDR2-800 and DDR2-1066 table, the derating values may obtained by linear interpolation.

These values are typically not subject to production test. They are verified by design and characterization.

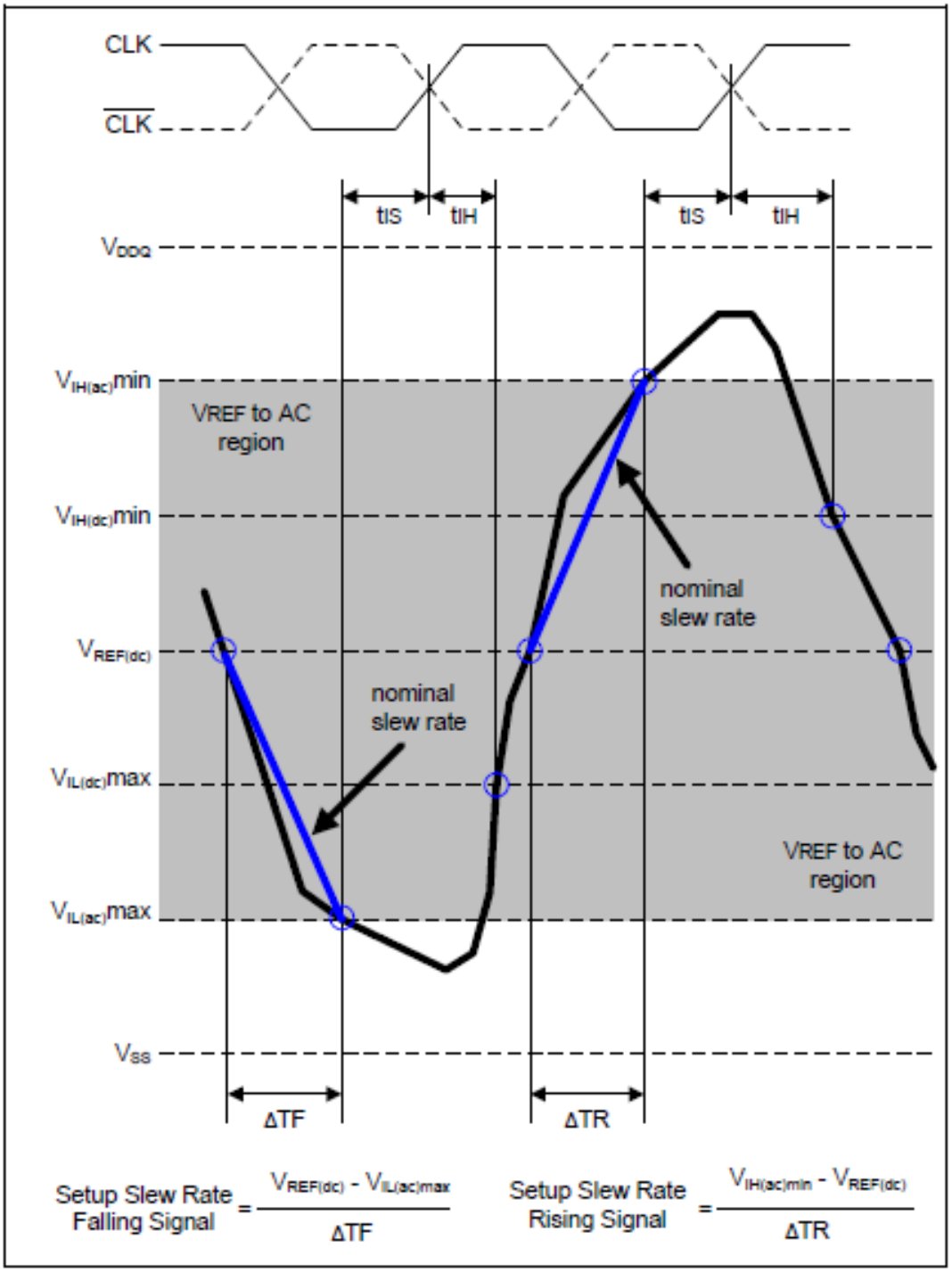


Figure 1 – Illustration of nominal slew rate for tIS

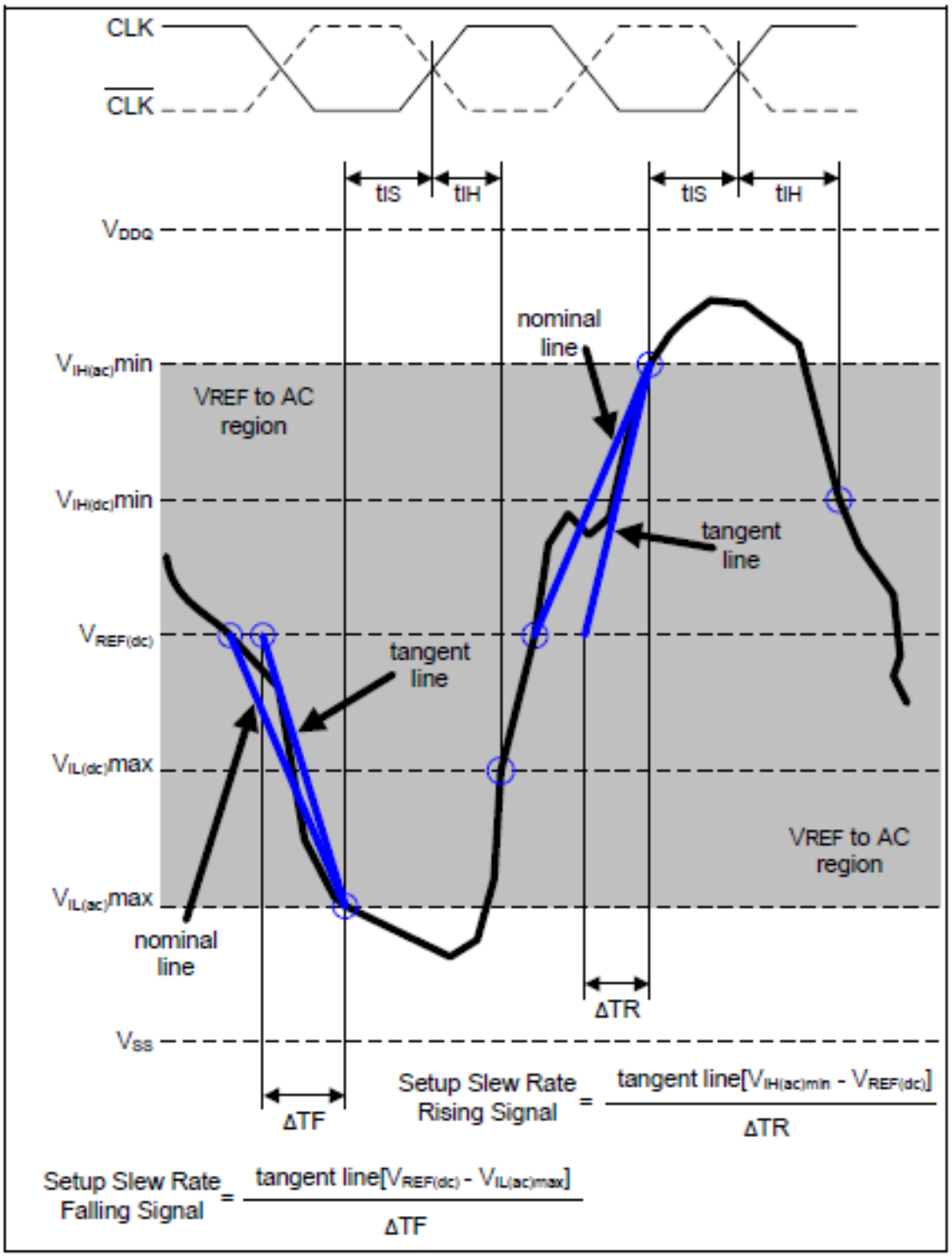


Figure 2 – Illustration of tangent line for tIS

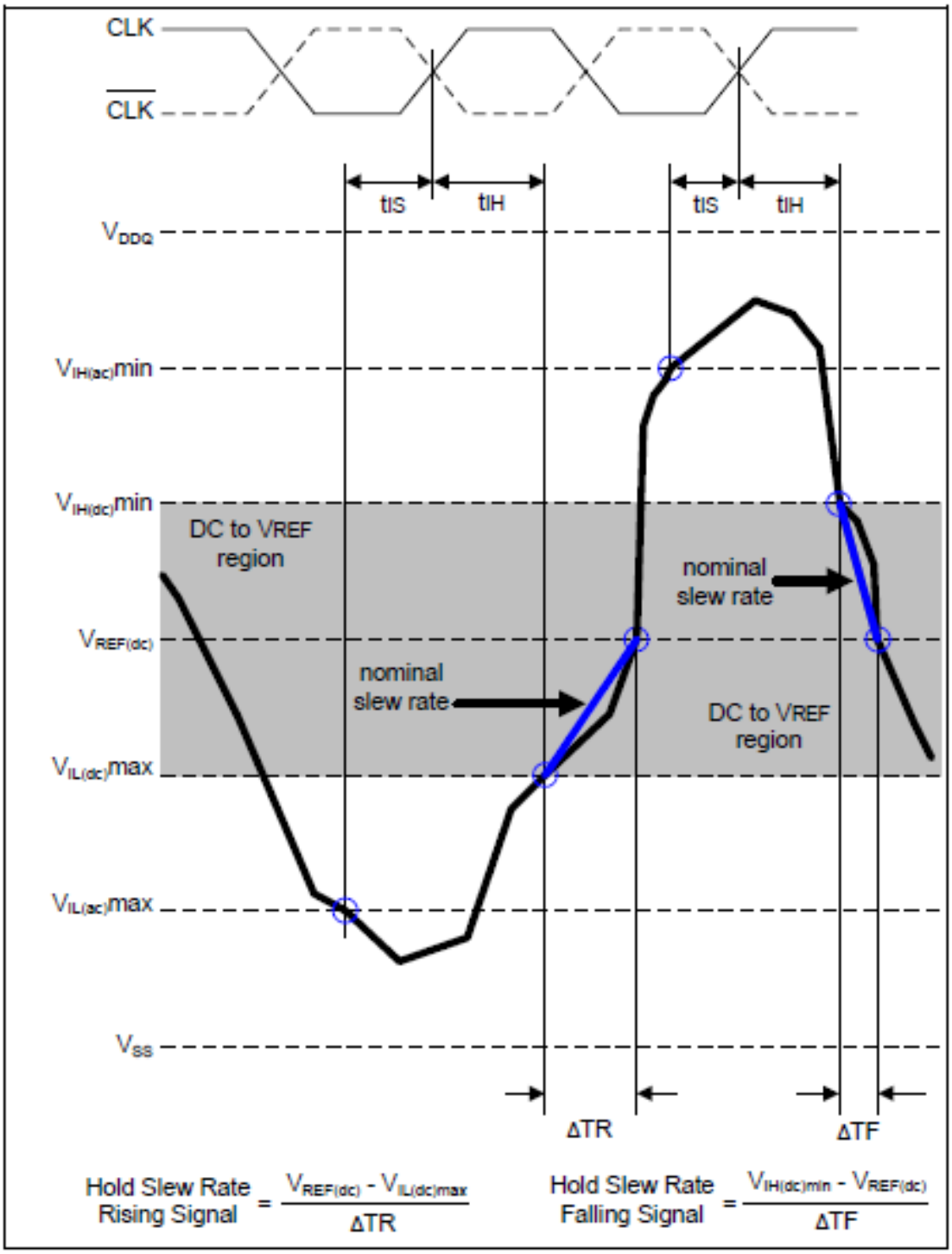


Figure 3 – Illustration of nominal slew rate for tIH

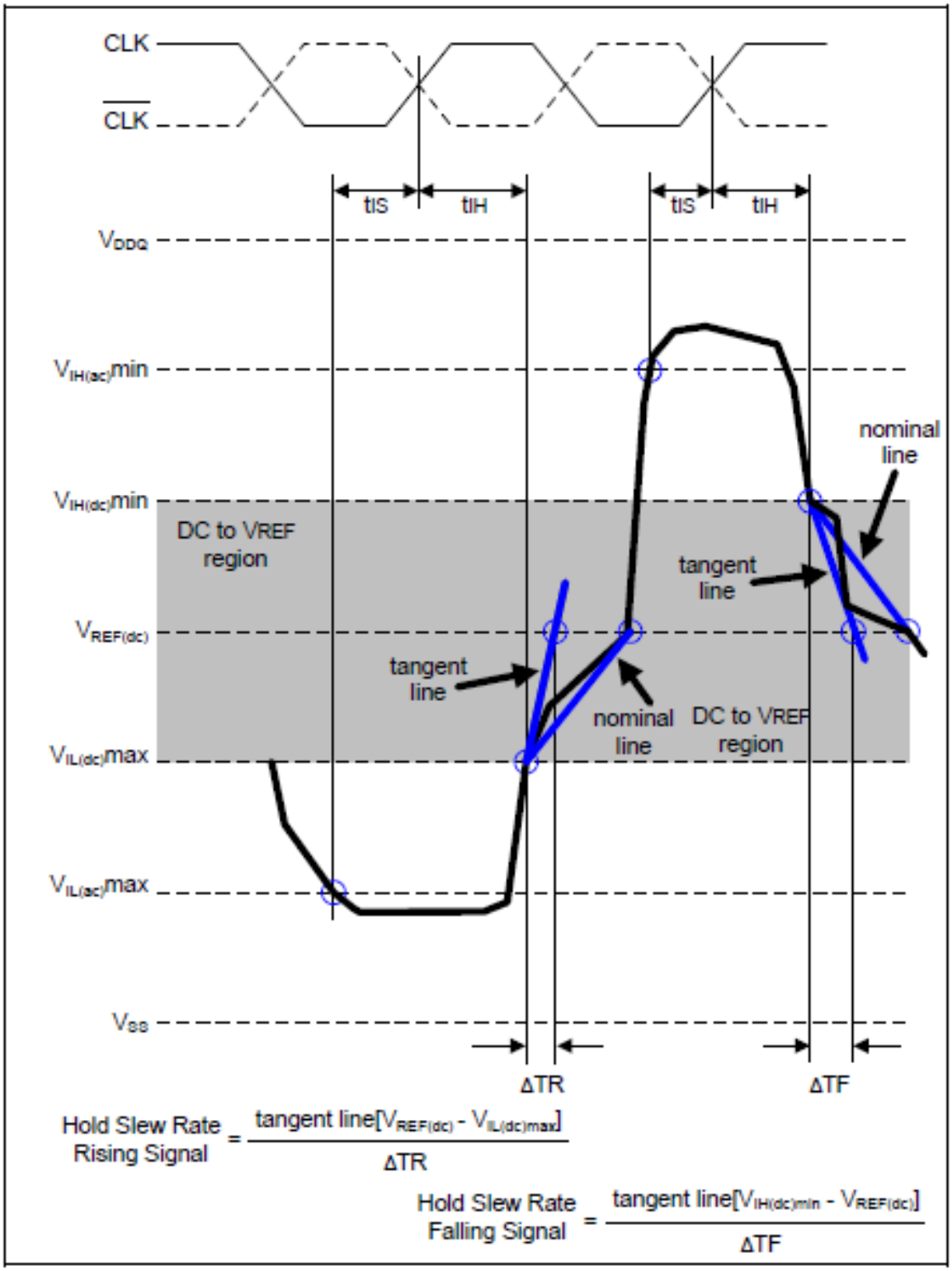


Figure 4 – Illustration of tangent line for tIH

Note 44: Data setup and hold time derating.

DQ Slew Rate (V/nS)	Δ tDS, ΔtDH Derating Values for DDR2-667, DDR2-800 and DDR2-1066 (All units in 'pS'; the note applies to the entire table)																	
	DQS/ /DQS Differential Slew Rate																	
	4.0 V/nS		3.0 V/nS		2.0 V/nS		1.8 V/nS		1.6 V/nS		1.4 V/nS		1.2 V/nS		1.0 V/nS		0.8 V/nS	
	Δ tDS	Δ tDH	Δ tDS	Δ tDH	Δ tDS	Δ tDH	Δ tDS	Δ tDH	Δ tDS	Δ tDH	Δ tDS	Δ tDH	Δ tDS	Δ tDH	Δ tDS	Δ tDH	Δ tDS	Δ tDH
2.0	100	45	100	45	100	45	-	-	-	-	-	-	-	-	-	-	-	-
1.5	67	21	67	21	67	21	79	33	-	-	-	-	-	-	-	-	-	-
1.0	0	0	0	0	0	0	12	12	24	24	-	-	-	-	-	-	-	-
0.9	-	-	-5	-14	-5	-14	7	-2	19	10	31	22	-	-	-	-	-	-
0.8	-	-	-	-	-13	-31	-1	-19	11	-7	23	5	35	17	-	-	-	-
0.7	-	-	-	-	-	-	-10	-42	2	-30	14	-18	26	-23	38	-11	-	-
0.6	-	-	-	-	-	-	-	-	-10	-59	2	-47	14	-35	26	-23	38	-11
0.5	-	-	-	-	-	-	-	-	-	-	-24	-89	-12	-77	0	-65	12	-53
0.4	-	-	-	-	-	-	-	-	-	-	-	-	-52	-140	-40	-128	-28	-116

For all input signals the total tDS (setup time) and tDH (hold time) required is calculated by adding the data sheet tDS(base) and tDH(base) value to the ΔtDS and ΔtDH derating value respectively. Example: tDS (total setup time) = tDS(base) + ΔtDS.

Setup (tDS) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of VREF(dc) and the first crossing of VIH(ac)min. Setup (tDS) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of VREF(dc) and the first crossing of VIL(ac)max. If the actual signal is always earlier than the nominal slew rate line between shaded 'VREF(dc) to AC region', use nominal slew rate for derating value. See Figure 5 Illustration of nominal slew rate for tDS (differential DQS,/DQS).

If the actual signal is later than the nominal slew rate line anywhere between shaded 'VREF(dc) to AC region', the slew rate of a tangent line to the actual signal from the AC level to DC level is used for derating value. See Figure 6 Illustration of tangent line for tDS (differential DQS,/DQS).

Hold (tDH) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of VIL (dc)max and the first crossing of VREF(dc). Hold (tDH) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of VIH(dc)min and the first crossing of VREF(dc). If the actual signal is always later than the nominal slew rate line between shaded 'DC level to VREF(dc) region', use nominal slew rate for derating value. See Figure 7 Illustration of nominal slew rate for tDH (differential DQS,/DQS).

If the actual signal is earlier than the nominal slew rate line anywhere between shaded 'DC to VREF(dc) region', the slew rate of a tangent line to the actual signal from the DC level to VREF(dc) level is used for derating value. See Figure 8 Illustration of tangent line for tDH (differential DQS,/DQS).

Although for slow slew rates the total setup time might be negative (i.e. a valid input signal will not have reached VIH/IL(ac) at the time of the rising clock transition) a valid input signal is still required to complete the transition and reach VIH/IL(ac). For slew rates in between the values listed in above DDR2-667, DDR2-800 and DDR2-1066 tDS/tDH derating with differential data strobe table, the derating values may be obtained by linear interpolation.

These values are typically not subject to production test. They are verified by design and characterization.

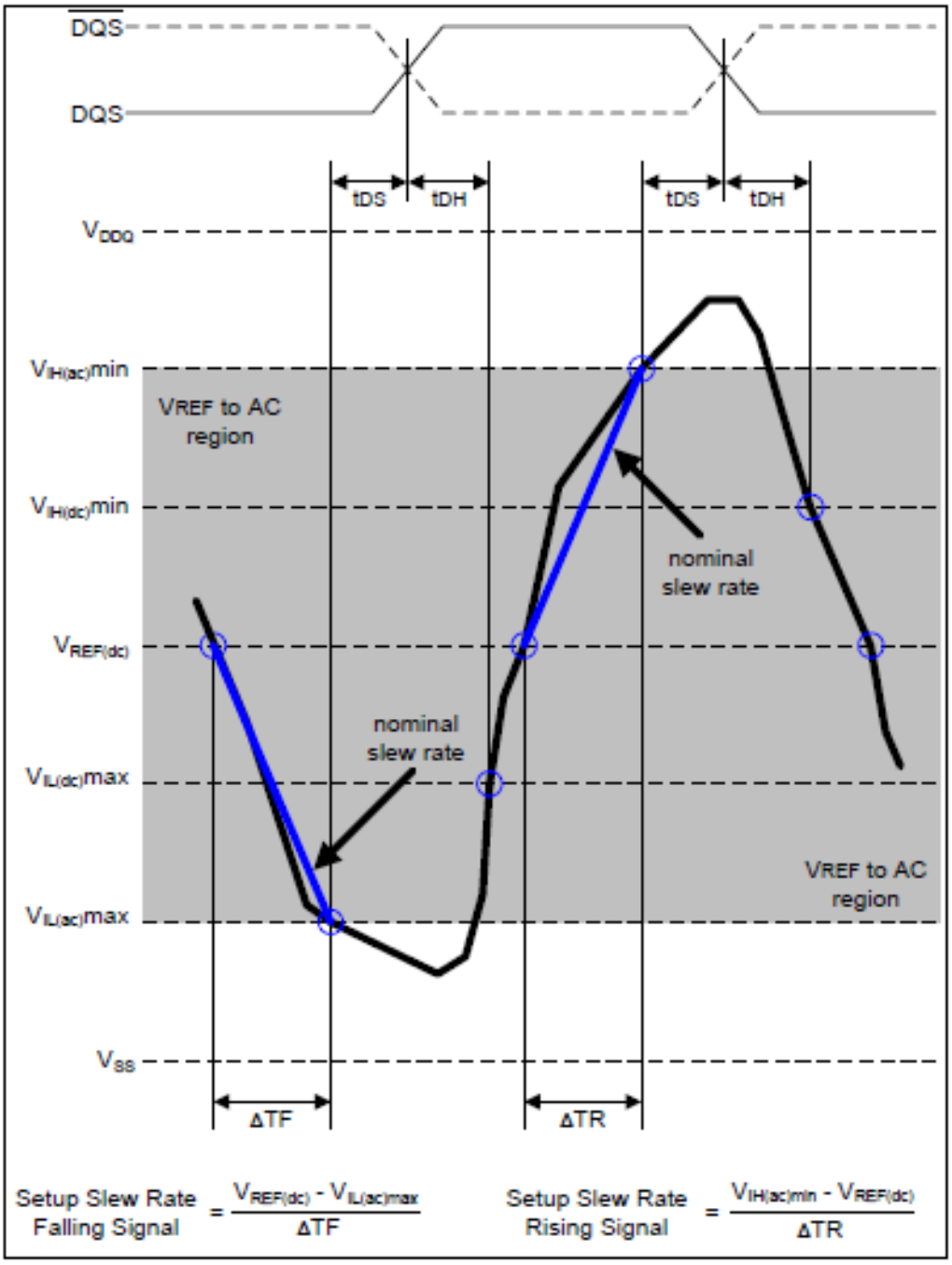


Figure 5 – Illustration of nominal slew rate for tDS (differential DQS, $\overline{DQS}$)

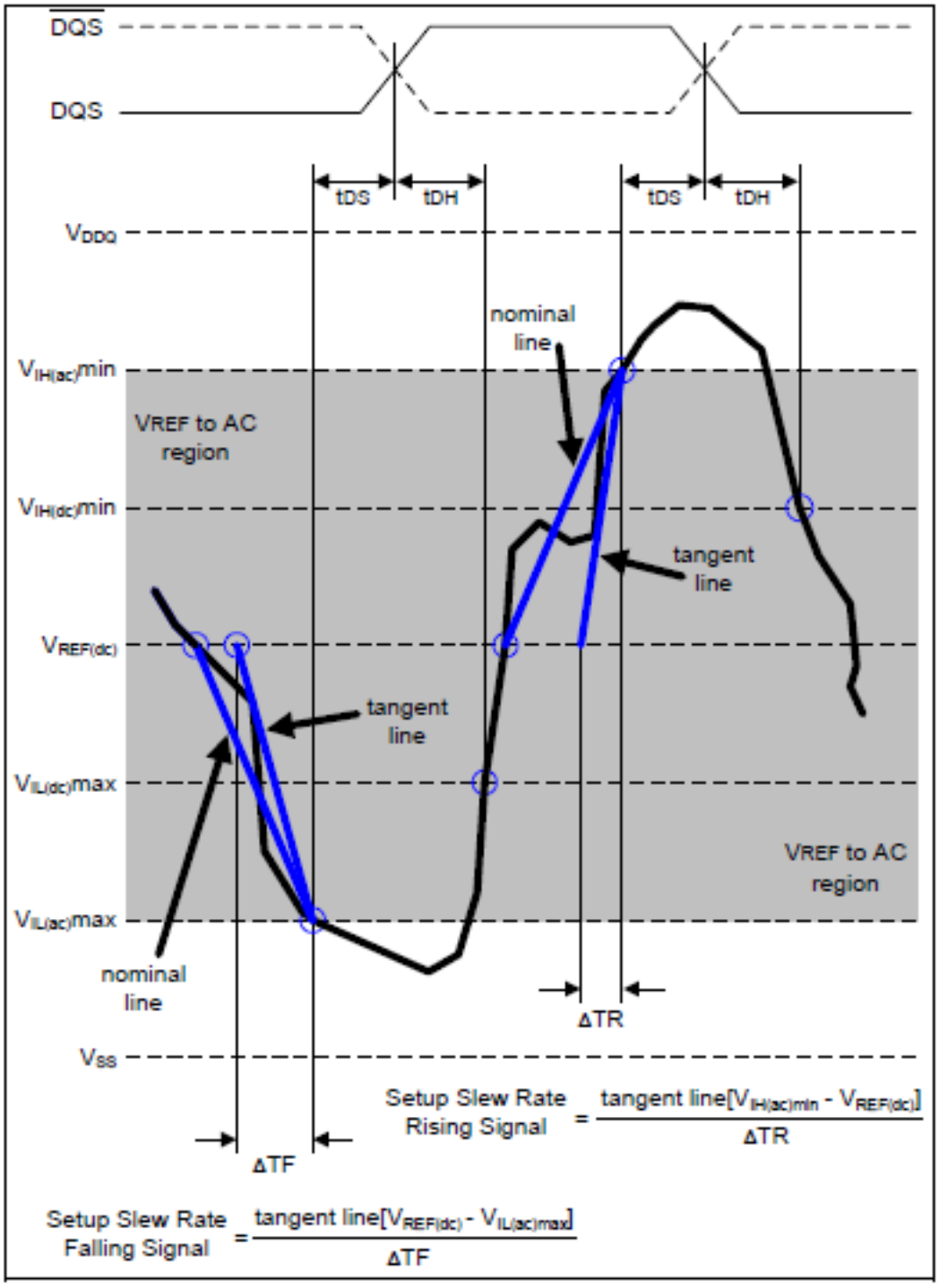


Figure 6 – Illustration of tangent line for tDS (differential DQS, $\overline{DQS}$)

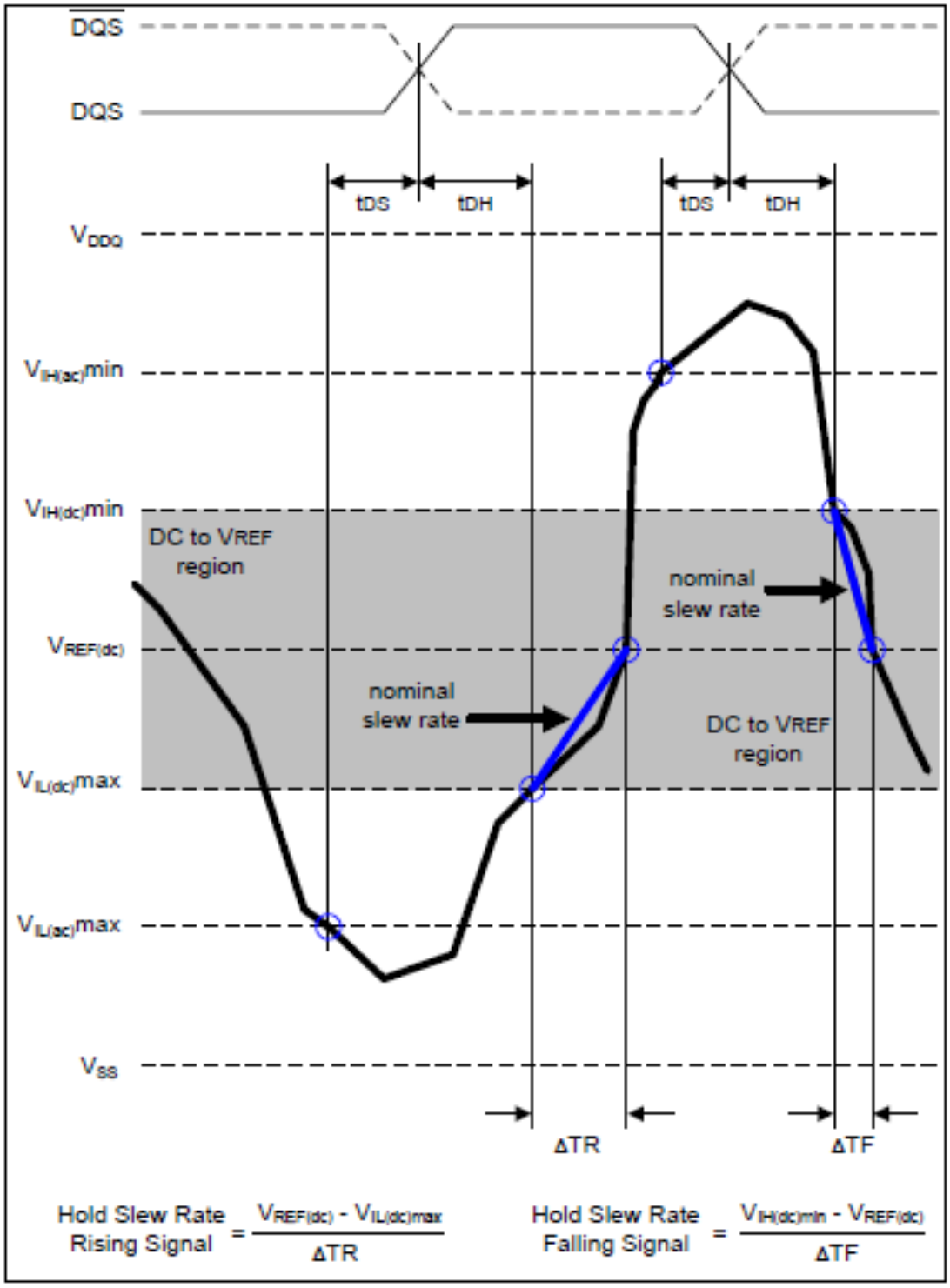


Figure 7 – Illustration of nominal slew rate for tDH (differential DQS, $\overline{DQS}$)

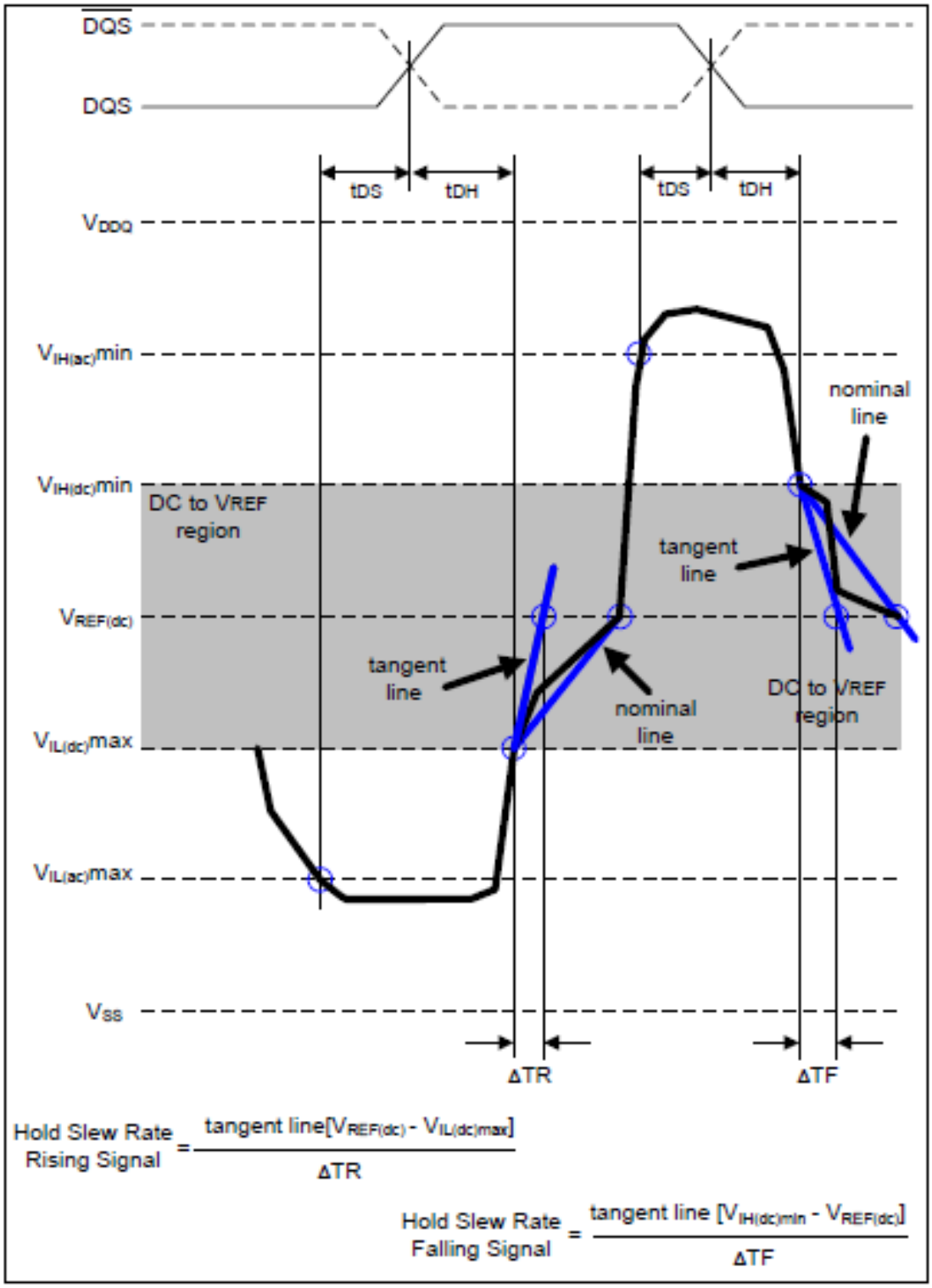
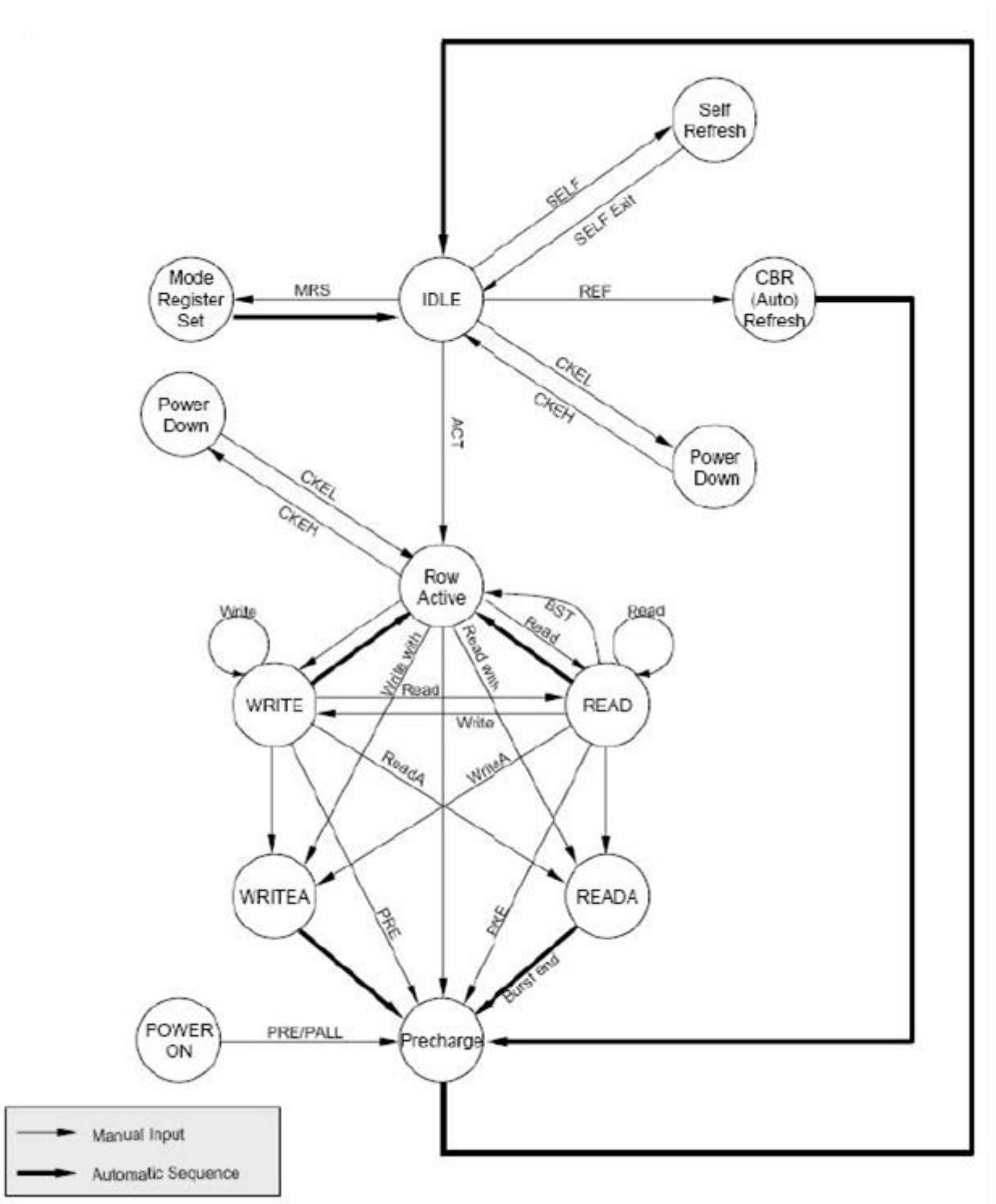


Figure 8 – Illustration tangent line for tDH (differential DQS, $\overline{DQS}$)

Simplified State Diagram



Command Truth Table

Command	CKE		/CS	/RAS	/CAS	/WE	BA1 BA0	A12 A11	A10	A9-A0
	n-1	N								
Bank Activate	H	H	L	L	H	H	BA	Row Address		
Single Bank Precharge	H	H	L	L	H	L	BA	X	L	X
Precharge All Banks	H	H	L	L	H	L	X	X	H	X
Write	H	H	L	H	L	L	BA	Column	L	Column
Write with Auto-precharge	H	H	L	H	L	L	BA	Column	H	Column
Read	H	H	L	H	L	H	BA	Column	L	Column
Read with Auto-precharge	H	H	L	H	L	H	BA	Column	H	Column
(Extended) Mode Register Set	H	H	L	L	L	L	BA	OP Code		
No Operation	H	X	L	H	H	H	X	X	X	X
Device Deselect	H	X	H	X	X	X	X	X	X	X
Refresh	H	H	L	L	L	H	X	X	X	X
Self Refresh Entry	H	L	L	L	L	H	X	X	X	X
Self Refresh Exit	L	H	H	X	X	X	X	X	X	X
			L	H	H	H				
Power Down Mode Entry	H	L	H	X	X	X	X	X	X	X
			L	H	H	H				
Power Down Mode Exit	L	H	H	X	X	X	X	X	X	X
			L	H	H	H				

H = High level, L = Low level, X = Don't care, BA=Bank Address

Note1: All DDR2 SDRAM commands are defined by states of /CS , /RAS , /CAS , /WE and CKE at the rising edge of the clock.

Note2: Bank addresses BA[1:0] determine which bank is to be operated upon. For (E)MRS BA selects an (Extended) Mode Register.

Note3: Burst reads or writes at BL = 4 can not be terminated or interrupted. See “Burst Interrupt” in section 8.5 for details.

Note4: VREF must be maintained during Self Refresh operation.

Note5: Self Refresh Exit is asynchronous.

Note6: The Power Down does not perform any refresh operations. The duration of Power Down Mode is therefore limited by the refresh requirements outlined in section 8.9.

CKE Truth Table

Current State	CKE		Command (n) /RAS, /CAS, /WE, /CS	Action (n)	Notes
	n-1	n			
Power Down	L	L	X	Maintain power down	11,13,15
	L	H	DESELECT or NOP	Power down exit	4,8,11,13
Self Refresh	L	L	X	Maintain power down	11,15,16
	L	H	DESELECT or NOP	Self refresh exit	4,5,9,16
Bank Active	H	L	DESELECT or NOP	Active power down entry	4,8,10,11,13,
All Banks Idle	H	L	DESELECT or NOP	Power power down entry	4,8,10,11,13,
	H	L	REFRESH	Self refresh entry	6,9,11,13
	H	L	Refer to the command truth table		7

Note1: CKE (N) is the logic state of CKE at clock edge N; CKE (N–1) was the state of CKE at the previous clock edge.

Note2: Current state is the state of the DDR2 SDRAM immediately prior to clock edge N.

Note3: COMMAND (N) is the command registered at clock edge N, and ACTION (N) is a result of COMMAND (N).

Note4: All states and sequences not shown are illegal or reserved unless explicitly described elsewhere in this document.

Note5: On Self Refresh Exit DESELECT or NOP commands must be issued on every clock edge occurring during the tXSNR period. Read commands may be issued only after tXSRD (200 clocks) is satisfied.

Note6: Self Refresh mode can only be entered from the All Banks Idle state.

Note7: Must be a legal command as defined in the Command Truth Table.

Note8: Valid commands for Power Down Entry and Exit are NOP and DESELECT only.

Note9: Valid commands for Self Refresh Exit are NOP and DESELECT only.

Note10: Power Down and Self Refresh can not be entered while Read or Write operations, (Extended) Mode Register Set operations or Precharge operations are in progress. See section 8.9 “Power Down Mode” and section 8.3.7/8.3.8 “Self Refresh Entry Command/Self Refresh Exit Command” for a detailed list of restrictions.

Note11: tCKEmin of 3 clocks means CKE must be registered on three consecutive positive clock edges. CKE must remain at the valid input level the entire time it takes to achieve the 3 clocks of registration. Thus, after any CKE transition, CKE may not transition from its valid level during the time period of tIS + 2 x tCK + tIH.

Note12: The state of ODT does not affect the states described in this table. The ODT function is not available during Self Refresh.

Note13: The Power Down does not perform any refresh operations. The duration of Power Down Mode is therefore limited by the refresh requirements outlined in section 8.9.

Note14: CKE must be maintained HIGH while the SDRAM is in OCD calibration mode.

Note15: “X” means “don’t care (including floating around VREF)” in Self Refresh and Power Down. However ODT must be driven high or low in Power Down if the ODT function is enabled (Bit A2 or A6 set to “1” in EMR (1)).

Note16: VREF must be maintained during Self Refresh operation.

Operative Command Table

Current State	/CS	/R	/C	/W	Addr.	Command	Action
Idle	H	X	X	X	X	DESL	NOP
	L	H	H	H	X	NOP	NOP
	L	H	H	L	X	TERM	NOP
	L	H	L	X	BA/CA/A10	READ/WRIT/BW	ILLEGAL ***(Note 1)***
	L	L	H	H	BA/RA	ACT	Bank active,Latch RA
	L	L	H	L	BA, A10	PRE/PREA	NOP***(Note 3)***
	L	L	L	H	X	REFA	Auto refresh***(Note 4)***
	L	L	L	L	Op-Code,	MRS	Mode register
Row Active	H	X	X	X	X	DESL	NOP
	L	H	H	H	X	NOP	NOP
	L	H	H	L	BA/CA/A10	READ/READA	Begin read,Latch CA, Determine auto-precharge
	L	H	L	L	BA/CA/A10	WRIT/WRITA	Begin write,Latch CA, Determine auto-prechar
	L	L	H	H	BA/RA	ACT	ILLEGAL ***(Note 1)***
	L	L	H	L	BA/A10	PRE/PREA	Precharge/Precharge all
	L	L	L	H	X	REFA	ILLEGAL
	L	L	L	L	Op-Code,	MRS	ILLEGAL
Read	H	X	X	X	X	DESL	NOP(Continue burst to end)
	L	H	H	H	X	NOP	NOP(Continue burst to end)
	L	H	H	L	X	TERM	Terminal burst
	L	H	L	H	BA/CA/A10	READ/READA	Terminate burst,Latch CA, Begin new read, Determine Auto-precharge
	L	L	H	H	BA/RA	ACT	ILLEGAL ***(Note 1)***
	L	L	H	L	BA, A10	PRE/PREA	Terminate burst, PrecharE
	L	L	L	H	X	REFA	ILLEGAL
	L	L	L	L	Op-Code,	MRS	ILLEGAL
Write	H	X	X	X	X	DESL	NOP(Continue burst to end)
	L	H	H	H	X	NOP	NOP(Continue burst to end)
	L	H	H	L	X	TERM	ILLEGAL
	L	H	L	H	BA/CA/A10	READ/READA	Terminate burst with DM=”H”,Latch CA, Begin read,Determine auto-precharge
	L	H	L	L	BA/CA/A10	WRIT/WRITA	Terminate burst,Latch CA,Begin new write, Determine auto-precharge ***(Note 2)***
	L	L	H	H	BA/RA	ACT	ILLEGAL ***(Note 1)***
	L	L	H	L	BA, A10	PRE/PREA	Terminate burst with DM=”H”, Precharge
	L	L	L	H	X	REFA	ILLEGAL
	L	L	L	L	Op-Code,	MRS	ILLEGAL

Operative Command Table (Contined)

Current State	/CS	/R	/C	/W	Addr.	Command	Action
Read with AP	H	X	X	X	X	DESL	NOP(Continue burst to end)
	L	H	H	H	X	NOP	NOP(Continue burst to end)
	L	H	H	L	BA/CA/A10	TERM	ILLEGAL
	L	H	L	X	BA/RA	READ/WRITE	ILLEGAL ***(Note 1)***
	L	L	H	H	BA/A10	ACT	ILLEGAL ***(Note 1)***
	L	L	H	L	X	PRE/PREA	ILLEGAL ***(Note 1)***
	L	L	L	H	X	REFA	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL
Write with AP	H	X	X	X	X	DESL	NOP(Continue burst to end)
	L	H	H	H	X	NOP	NOP(Continue burst to end)
	L	H	H	L	X	TERM	ILLEGAL
	L	H	L	X	BA/CA/A10	READ/WRITE	ILLEGAL ***(Note 1)***
	L	L	H	H	BA/RA	ACT	ILLEGAL ***(Note 1)***
	L	L	H	L	BA/A10	PRE/PREA	ILLEGAL ***(Note 1)***
	L	L	L	H	X	REFA	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL
Pre-charging	H	X	X	X	X	DESL	NOP(idle after tRP)
	L	H	H	H	X	NOP	NOP(idle after tRP)
	L	H	H	L	X	TERM	NOP
	L	H	L	X	BA/CA/A10	READ/WRITE	ILLEGAL ***(Note 1)***
	L	L	H	H	BA/RA	ACT	ILLEGAL ***(Note 1)***
	L	L	H	L	BA/A10	PRE/PREA	NOP(idle after tRP) ***(Note 3)***
	L	L	L	H	X	REFA	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL
Row Activating	H	X	X	X	X	DESL	NOP(Row active after tRCD)
	L	H	H	H	X	NOP	NOP(Row active after tRCD)
	L	H	H	L	X	TERM	NOP
	L	H	L	X	BA/CA/A10	READ/WRITE	ILLEGAL ***(Note 1)***
	L	L	H	H	BA/RA	ACT	ILLEGAL ***(Note 1)***
	L	L	H	L	BA/A10	PRE/PREA	ILLEGAL ***(Note 1)***
	L	L	L	H	X	REFA	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL

Remark H = High level, L = Low level, X = High or Low level (Don't care), AP = Auto Pre-charge

Operative Command Table (Contined)

Current State	/CS	/R	/C	/W	Addr.	Command	Action
Write Recovering	H	X	X	X	X	DESL	NOP
	L	H	H	H	X	NOP	NOP
	L	H	H	L	X	TERM	NOP
	L	H	L	H	BA/CA/A10	READ	ILLEGAL***(Note 1)***
	L	H	L	L	BA/CA/A10	WRIT/WRITA	New write, Determine AP
	L	L	H	H	BA/RA	ACT	ILLEGAL ***(Note 1)***
	L	L	H	L	BA/A10	PRE/PREA	ILLEGAL ***(Note 1)***
	L	L	L	H	X	REFA	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL
Refreshing	H	X	X	X	X	DESL	NOP(idle after t_{RP})
	L	H	H	H	X	NOP	NOP(idle after t_{RP})
	L	H	H	L	X	TERM	NOP
	L	H	L	X	BA/CA/A10	READ/WRIT	ILLEGAL
	L	L	H	H	BA/RA	ACT	ILLEGAL
	L	L	H	L	BA/A10	PRE/PREA	NOP(idle after t_{RP})
	L	L	L	H	X	REFA	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL

Remark H = High level, L = Low level, X = High or Low level (Don't care), AP = Auto Pre-charge

Note1: ILLEGAL to bank in specified states; Function may be legal in the bank indicated by Bank Address (BA), depending on the state of that bank.

Note2: Must satisfy bus contention, bus turn around, and/or write recovery requirements.

Note3: NOP to bank precharging or in idle state.May precharge bank indicated by BA.

Note4: ILLEGAL of any bank is not idl

Command Truth Table for CKE

Current State	C	KE	/CS	/R	/C	/W	Addr.	Action
Self Refresh	H	X	X	X	X	X	X	INVALID
	L	H	H	X	X	X	X	Exist Self-Refresh
	L	H	L	H	H	H	X	Exist Self-Refresh
	L	H	L	H	H	L	X	ILLEGAL
	L	H	L	H	L	X	X	ILLEGAL
	L	H	L	L	X	X	X	ILLEGAL
	L	L	X	X	X	X	X	NOP(Maintain self refresh)
Both bank precharge power down	H	X	X	X	X	X	X	INVALID
	L	H	H	X	X	X	X	Exist Power down
	L	H	L	H	H	H	X	Exist Power down
	L	H	L	H	H	L	X	ILLEGAL
	L	H	L	H	L	X	X	ILLEGAL
	L	H	L	L	X	X	X	ILLEGAL
	L	L	X	X	X	X	X	NOP(Maintain Power down)
All Banks Idle	H	H	X	X	X	X	X	Refer to function true table
	H	L	H	X	X	X	X	Enter power down mode***(Note 3)***
	H	L	L	H	H	H	X	Enter power down mode***(Note 3)***
	H	L	L	H	H	L	X	ILLEGAL
	H	L	L	H	L	X	X	ILLEGAL
	H	L	L	L	H	H	RA	Row active/Bank active
	H	L	L	L	L	H	X	Enter self-refresh***(Note 3)***
	H	L	L	L	L	L	Op-Code	Mode register access
	H	L	L	L	L	L	Op-Code	Special mode register access
	L	X	X	X	X	X	X	Refer to current state
Any State Other than Listed above	H	H	X	X	X	X	X	Refer to command truth table

Remark: H = High level, L = Low level, X = High or Low level (Don't care)

Notes 1: After CKE's low to high transition to exist self refresh mode.And a time of t_{RC}(min) has to be Elapse after CKE's low to high transition to issue a new command.

Notes 2: CKE low to high transition is asynchronous as if restarts internal clock.

Notes 3: Power down and self refresh can be entered only from the idle state of all banks.

Initialization

The following sequence is required for power-up and initialization and is shown in below Figure:

1. Apply power and attempt to maintain CKE below 0.2 × V_{DDQ} and ODT*1 at a LOW state (all other inputs may be undefined.) Either one of the following sequence is required for Power-up.
   A. The V_{DD} voltage ramp time must be no greater than 200 mS from when V_{DD} ramps from 300 mV to V_{DD} min; and during the V_{DD} voltage ramp, $|V_{DD} - V_{DDQ}| \leq 0.3$ volts.
      - V_{DD}, V_{DDL} and V_{DDQ} are driven from a single power converter output
      - V_{TT} is limited to 0.95V max
      - V_{REF}
      *2 tracks $V_{DDQ}/2$
      - $V_{DDQ} \geq V_{REF}$ must be met at all times

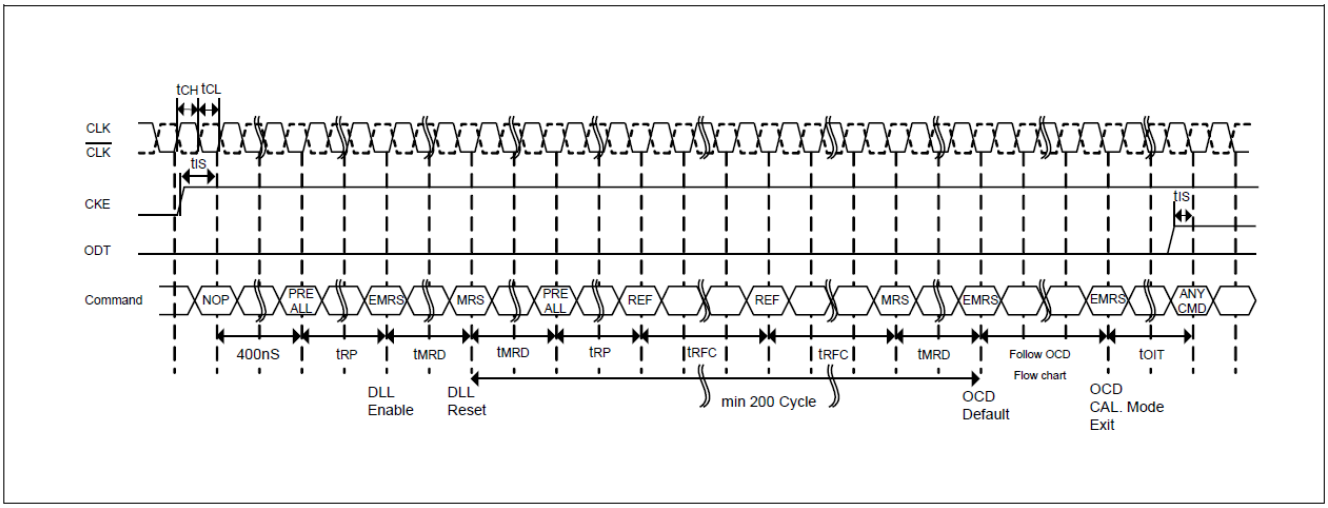
   B. Voltage levels at I/Os and outputs must be less than V_{DDQ} during voltage ramp time to avoid DRAM latch-up. During the ramping of the supply voltages, $V_{DD} \geq V_{DDL} \geq V_{DDQ}$ must be maintained and is applicable to both AC and DC levels until the ramping of the supply voltages is complete.
      - Apply V_{DD}/V_{DDL}
      *3 before or at the same time as V_{DDQ}
      - Apply V_{DDQ}
      *4 before or at the same time as V_{TT}
      - V_{REF}
      *2 tracks $V_{DDQ}/2$
      - $V_{DDQ} \geq V_{REF}$ must be met at all times
      - Apply V_{TT}
      - The V_{TT} voltage ramp time from when V_{DDQ} min is achieved on V_{DDQ} to when V_{TT} min is achieved on V_{TT} must be no greater than 500 mS
2. Start Clock and maintain stable condition for 200 µS (min.).
3. After stable power and clock (CLK,CLK), apply NOP or Deselect and take CKE HIGH.
4. Wait minimum of 400 nS then issue precharge all command. NOP or Deselect applied during 400 nS period.
5. Issue an EMRS command to EMR (2). (To issue EMRS command to EMR (2), provide LOW to BA0, HIGH to BA1.)
6. Issue an EMRS command to EMR (3). (To issue EMRS command to EMR (3), provide HIGH to BA0 and BA1.)
7. Issue EMRS to enable DLL. (To issue DLL Enable command, provide LOW to A0, HIGH to BA0 and LOW to BA1. And A9=A8=A7=LOW must be used when issuing this command.)
8. Issue a Mode Register Set command for DLL reset. (To issue DLL Reset command, provide HIGH to A8 and LOW to BA0 and BA1.)
9. Issue a precharge all command.
10. Issue 2 or more Auto Refresh commands.
11. Issue a MRS command with LOW to A8 to initialize device operation. (i.e. to program operating parameters without resetting the DLL.)
12. At least 200 clocks after step 8, execute OCD Calibration (Off Chip Driver impedance adjustment). If OCD calibration is not used, EMRS to EMR (1) to set OCD Calibration Default

(A9=A8=A7=HIGH) followed by EMRS to EMR (1) to exit OCD Calibration Mode

(A9=A8=A7=LOW) must be issued with other operating parameters of EMR(1).

13. The DDR2 SDRAM is now ready for normal operation.

Reset and Power up initialization sequence

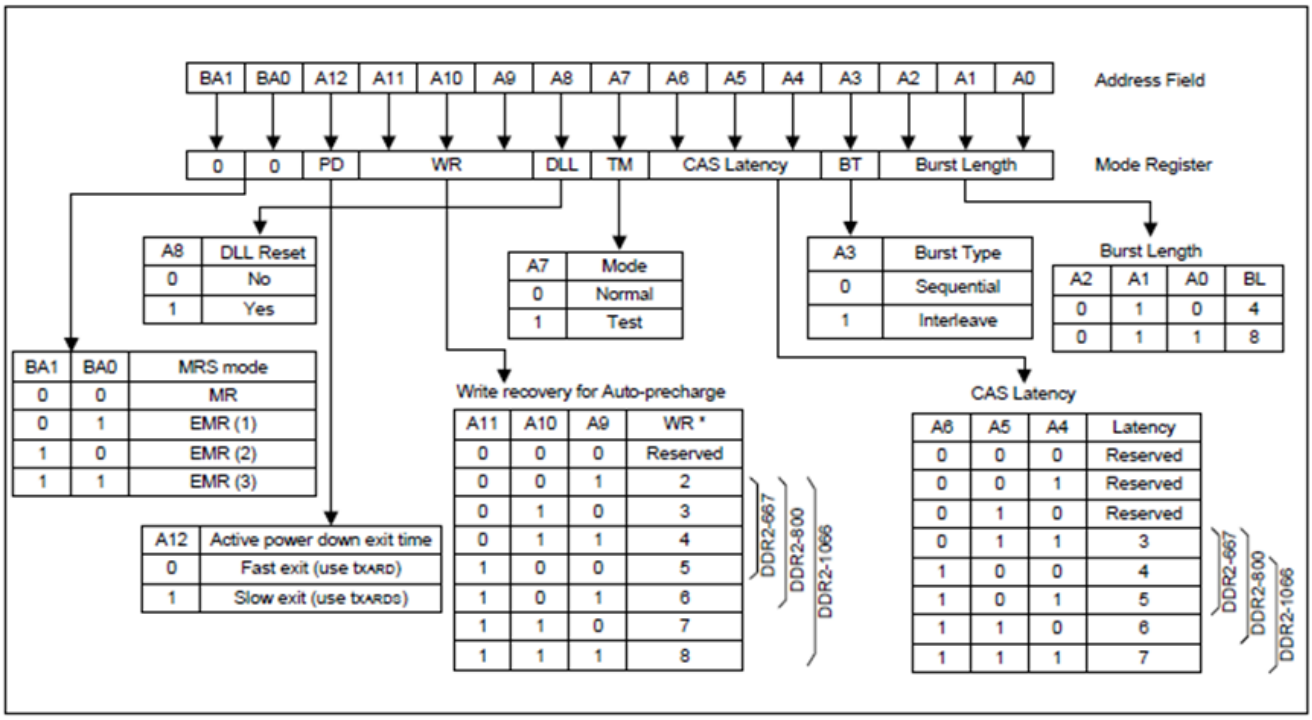


Mode Register Definition

Mode Register Set Command (MRS)

The mode register stores the data for controlling the various operating modes of DDR2 SDRAM. It programs CAS Latency, burst length, burst sequence, test mode, DLL reset, Write Recovery (WR) and various vendor specific options to make DDR2 SDRAM useful for various applications. The default value in the Mode Register after power-up is not defined, therefore the Mode Register must be programmed during initialization for proper operation.

The DDR2 SDRAM should be in all bank precharge state with CKE already HIGH prior to writing into the mode register. The mode register set command cycle time (tMRD) is required to complete the write operation to the mode register. The mode register contents can be changed using the same command and clock cycle requirements during normal operation as long as all banks are in the precharge state. The mode register is divided into various fields depending on functionality. Burst length is defined by A[2:0] with options of 4 and 8 bit burst lengths. The burst length decodes are compatible with DDR SDRAM. Burst address sequence type is defined by A3, CAS Latency is defined by A[6:4]. The DDR2 does not support half clock latency mode. A7 is used for test mode. A8 is used for DLL reset. A7 must be set to LOW for normal MRS operation. Write recovery time WR is defined by A[11:9]. Refer to the table for specific codes.



Note1: WR (write recovery for Auto-precharge) min is determined by tCK(avg) max and WR max is determined by tCK(avg) min. WR[cycles] = RU{ tWR[nS] / tCK(avg)[nS] }, where RU stands for round up. The mode register must be programmed to this value. This is also used with tRP to determine tDAL.

Burst Type (A3)

Burst Length	Starting Address (A2 A1 A0)	Sequential Addressing (decimal)	Interleave Addressing (decimal)
4	x00	0123TTTT	0123TTTT
	x01	1230TTTT	1032TTTT
	x10	2301TTTT	2301TTTT
	x11	3012TTTT	3210TTTT
8	000	01234567	01234567
	001	12305674	10325476
	010	23016745	23016745
	011	30127456	32107654
	100	45670123	45670123
	101	56741230	54761032
	110	67452301	67452301
	111	74563012	76543210

Write Recovery

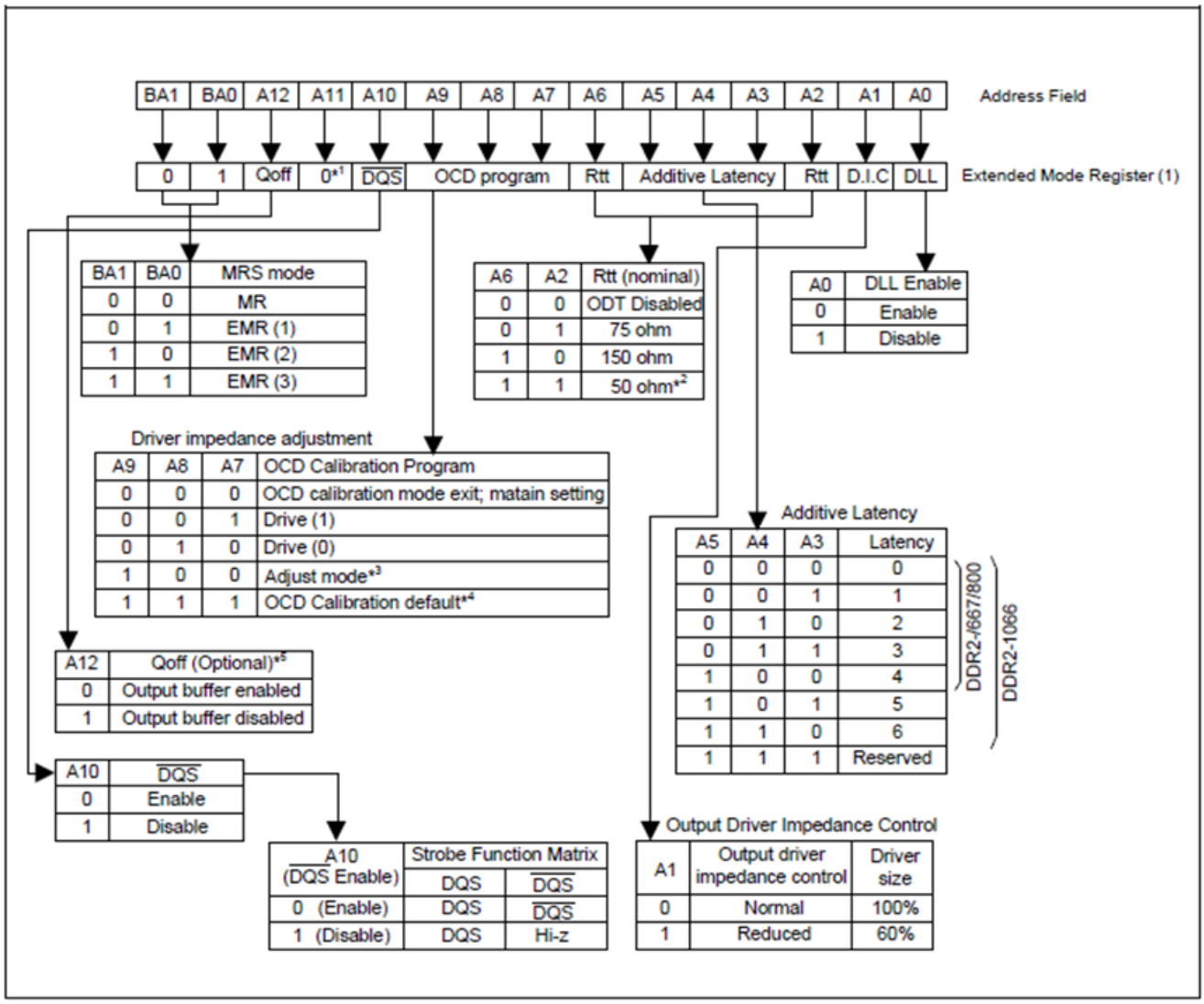
WR (Write Recovery) is for Writes with Auto-Precharge only and defines the time when the device starts pre-charge internally. WR must be programmed to match the minimum requirement for the analogue t_{WR} timing.

Power-Down Mode

Active power-down (PD) mode is defined by bit A12. PD mode allows the user to determine the active power-down mode, which determines performance vs. power savings. PD mode bit A12 does not apply to precharge power-down mode. When bit A12 = 0, standard Active Power-down mode or 'fast-exit' active power-down mode is enabled. The tXARD parameter is used for 'fast-exit' active power-down exit timing. The DLL is expected to be enabled and running during this mode. When bit M12 = 1, a lower power active power-down mode or 'slow-exit' active power-down mode is enabled. The tXARDS parameter is used for 'slow-exit' active power-down exit timing. The DLL can be enabled, but 'frozen' during active power-down mode since the exit-to-READ command timing is relaxed. The power difference expected between PD 'normal' and PD 'low-power' mode is defined in the IDD table.

Extend Mode Register EMR1

The EMR1 stores the data for enabling or disabling the DLL, output driver strength, additive latency, ODT, DQS disable, OCD program. The default value of the EMR1 is not defined, therefore the EMR1 must be programmed during initialization for proper operation. The DDR2 SDRAM should be in all bank precharge with CKE already high prior to writing into the EMR1. The mode register set command cycle time (t_{MRD}) must be satisfied to complete the write operation to the extended MR1. EMR1 contents can be changed using the same command and clock cycle requirements during normal operation as long as all banks are in the precharge state. A0 is used for DLL enable or disable. A1 is used for enabling a reduced strength output driver. A[5:3] determines the additive latency, A[9:7] are used for OCD control, A10 is used for DQS disable. A2 and A6 are used for ODT setting.



Note1: A11 default is “0” RDQS disabled.

Note2: Optional for DDR2-667, mandatory for DDR2-800 and DDR2-1066.

Note3: When Adjust mode is issued, AL from previously set value must be applied.

Note4: After setting to default, OCD calibration mode needs to be exited by setting A9-A7 to 000. Refer to the section 8.2.3 for detailed information.

Note5: Output disabled - DQs, LDQS, LDQS , UDQS, UDQS . This feature is used in conjunction with DIMM IDD measurements when IDDQ is not desired to be included.

DLL Enable

The DLL must be enabled for normal operation. DLL enable is required during power-up initialization, and upon returning to normal operation after having the DLL disabled. The DLL is automatically disabled when entering Self Refresh operation and is automatically re-enabled and reset upon exit of Self Refresh operation. Any time the DLL is enabled (and subsequently reset), 200 clock cycles must occur before a Read command can be issued to allow time for the internal clock to be synchronized with the external clock. Failing to wait for synchronization to occur may result in a violation of the tAC or tDQSCK parameters.

Output Drive Strength

The output drive strength is defined by bit A1. Normal drive strength outputs are specified to be SSTL_18.
Programming bit A1 = 0 selects normal (100 %) drive strength for all outputs.
Programming bit A1 = 1 will reduce all outputs to approximately 60 % of the SSTL_18 drive strength.
This option is intended for the support of the lighter load and/or point-to-point environments.

Single-ended and Differential Data Strobe Signals

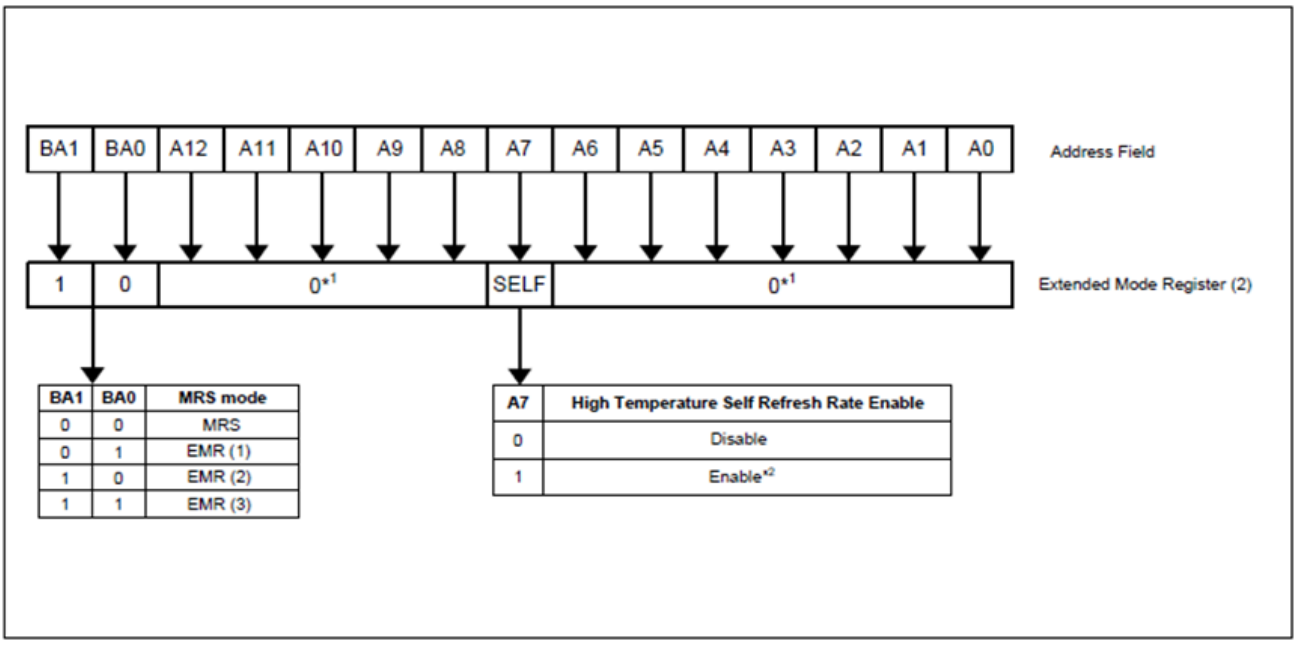
EMRS		Strobe Function Matrix				Signals
A11 (/RDQS Enable)	A10 (/DQS Enable)	RDQS DM	/RDQS	DQS	/DQS	
0 (Disable)	0 (Enable)	DM	Hi-Z	DQS	/DQS	Differential DQS signal
0 (Disable)	1 (Disable)	DM	Hi-Z	DQS	Hi-Z	Single-ended DQS signal
1 (Enable)	0 (Enable)	RDQS	/RDQS	DQS	/DQS	Differential DQS signal
1 (Enable)	1 (Disable)	RDQS	Hi-Z	DQS	Hi-Z	Single-ended DQS signal

Output Disable (Qoff)

Under normal operation, the DRAM outputs are enabled during Read operation for driving data (Qoff bit in the EMRS(1) is set to (0). When the Qoff bit is set to 1, the DRAM outputs will be disabled. Disabling the DRAM outputs allows users to measure IDD currents during Read operations, without including the output buffer current.

Extend Mode Register EMR2

The EMR 2 controls refresh related features. The default value of the EMR 2 is not defined, therefore the EMR 2 must be programmed during initialization for proper operation.
The DDR2 SDRAM should be in all bank precharge state with CKE already high prior to writing into the EMR 2.
The mode register set command cycle time (t_{MRD}) must be satisfied to complete the write operation to the EMR 2.
Mode register contents can be changed using the same command and clock cycle requirements during normal operation as long as all banks are in the precharge state.

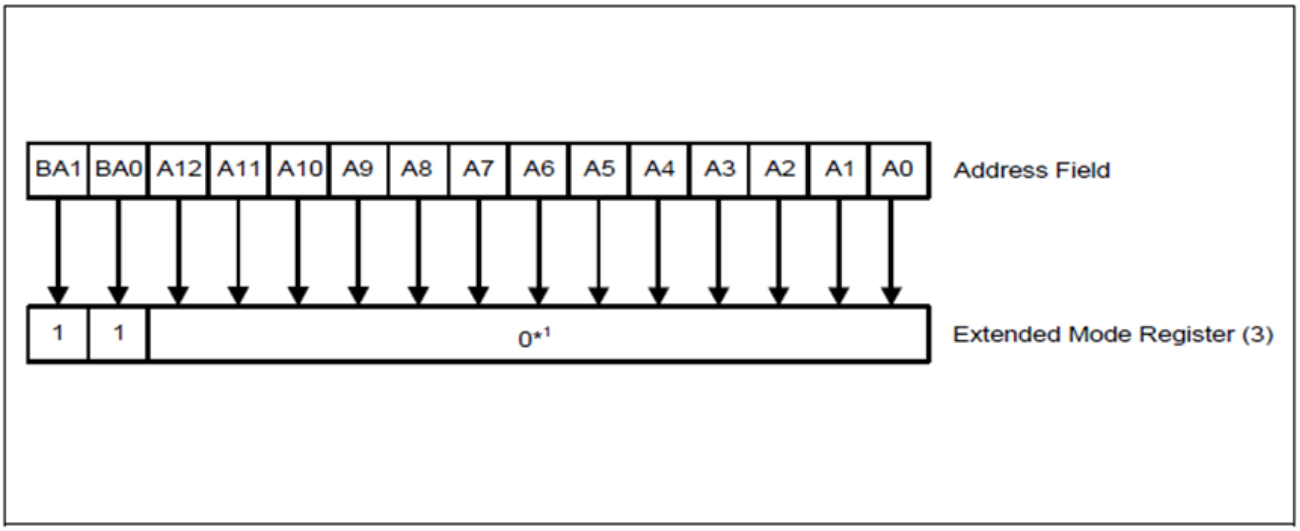


Note1: The rest bits in EMR 2 is reserved for future use and all bits in EMR 2 except A7, BA0 and BA1 must be programmed to 0 when setting the extended mode register 2 during initialization.

Note2: When DRAM is operated at 85°C < TCASE ≤ 95°C the extended Self Refresh rate must be enabled by setting bit A7 to "1" before the Self Refresh mode can be entered.

Extend Mode Register EMR3

No function is defined in extended mode register 3. The default value of the EMR 3 is not defined, therefore the EMR 3 must be programmed during initialization for proper operation.



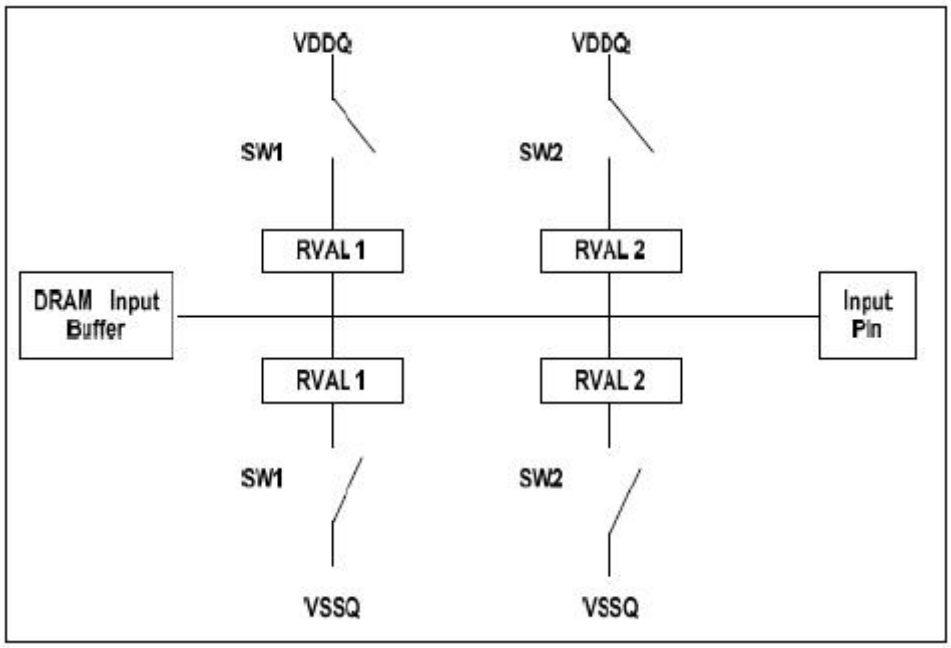
Note1: All bits in EMR 3 except BA0 and BA1 are reserved for future use and must be set to 0 when programming the EMR 3.

On-Die Termination (ODT)

ODT (On-Die Termination) is a new feature on DDR2 components that allows a DRAM to turn on/off termination resistance for each UDQ, LDQ, UDQS, UDQS, LDQS, LDQS, UDM and LDM signal via the ODT control pin for x16 configuration, where UDQS and LDQS are terminated only when enabled in the EMRS(1) by address bit A10 = 0.

The ODT feature is designed to improve signal integrity of the memory channel by allowing the DRAM controller to independently turn on/off termination resistance for any or all DRAM devices. The ODT function can be used for all active and standby modes. ODT is turned off and not supported in Self- Refresh mode.

ODT Function

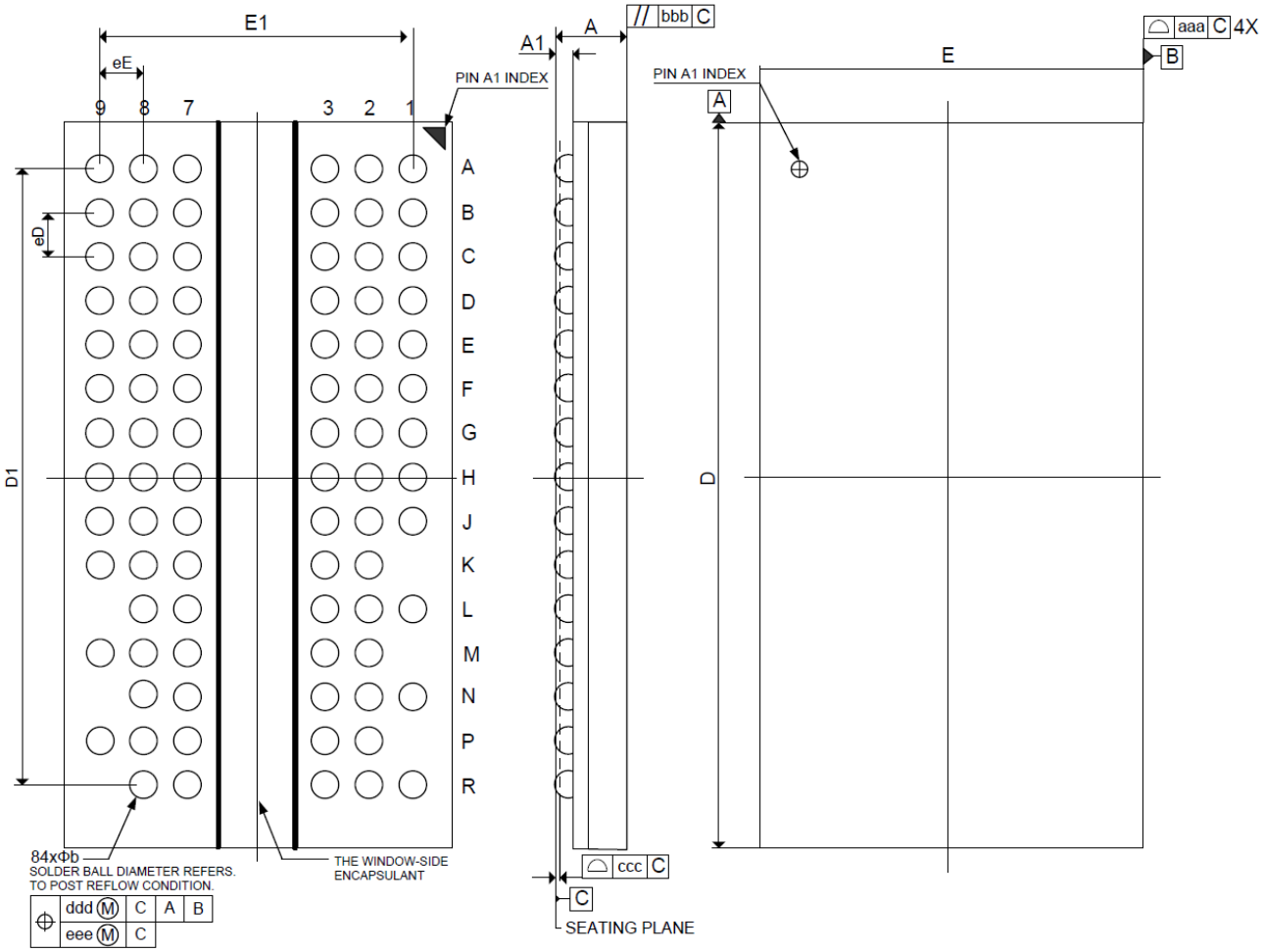


Switch sw1 or sw2 is enabled by the ODT pin. Selection between sw1 or sw2 is determined by “Rtt (nominal)” in EMRS(1) address bits A6 & A2. Target Rtt = 0.5 * Rval1 or 0.5 * Rval2.

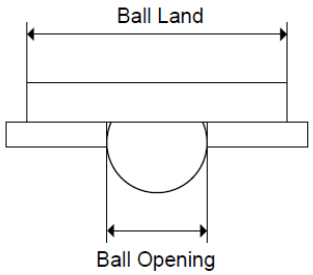
The ODT pin will be ignored if the EMRS(1) is programmed to disable ODT.

Package Description: 84Ball-FBGA

Solder ball: Lead free (Sn-Ag-Cu)



SYMBOL	DIMENSION (MM)		
	MIN.	NOM.	MAX.
A	---	---	1.20
A1	0.25	---	0.40
b	0.40	---	0.50
D	12.40	12.50	12.60
E	7.90	8.00	8.10
D1	11.20 BSC.		
E1	6.40 BSC.		
eE	0.80 BSC.		
eD	0.80 BSC.		
aaa	---	---	0.15
bbb	---	---	0.20
ccc	---	---	0.10
ddd	---	---	0.15
eee	---	---	0.08



Note: 1. Ball land : 0.5mm
2. Ball opening : 0.4mm
3. PCB Ball land suggested ≤ 0.4mm

Revision History

Revision No.	History	Draft Date	Editor	Remark
0.1	Initial Release.	Jul. 2014	Ternence Chen	N/A
1.0	First SPEC. release.	Aug. 2014	Ternence Chen	N/A