MS-7512

ATX Version: 0A

CPU: Intel Pentium 4, Pentium D, Core2 Duo, Wolfdale, Kentsfield and Yorkfield processors in LGA775 Package.

System Chipset:

Intel Eaglelake - G/P (G, P3North Bridge)
Intel ICH9/10 (South Bridge)

On Board Device:

CLOCK Gen -- ICS 9LPRS113
LPC Super I/O -- Fintek F71882F
LAN -- Realtek 8111C (PCIE)
HD Audio Codec -- RTL888/888T
1394 Controller -- JMB381
PCIE to PATA/SATA Bridge -- JMB-363 e-SATA X2/ IDE X1
PCIE to PATA/SATA Bridge -- Marvell 88SE6111 SATA X1

Main Memory:

Dual-channel DDR-II * 4

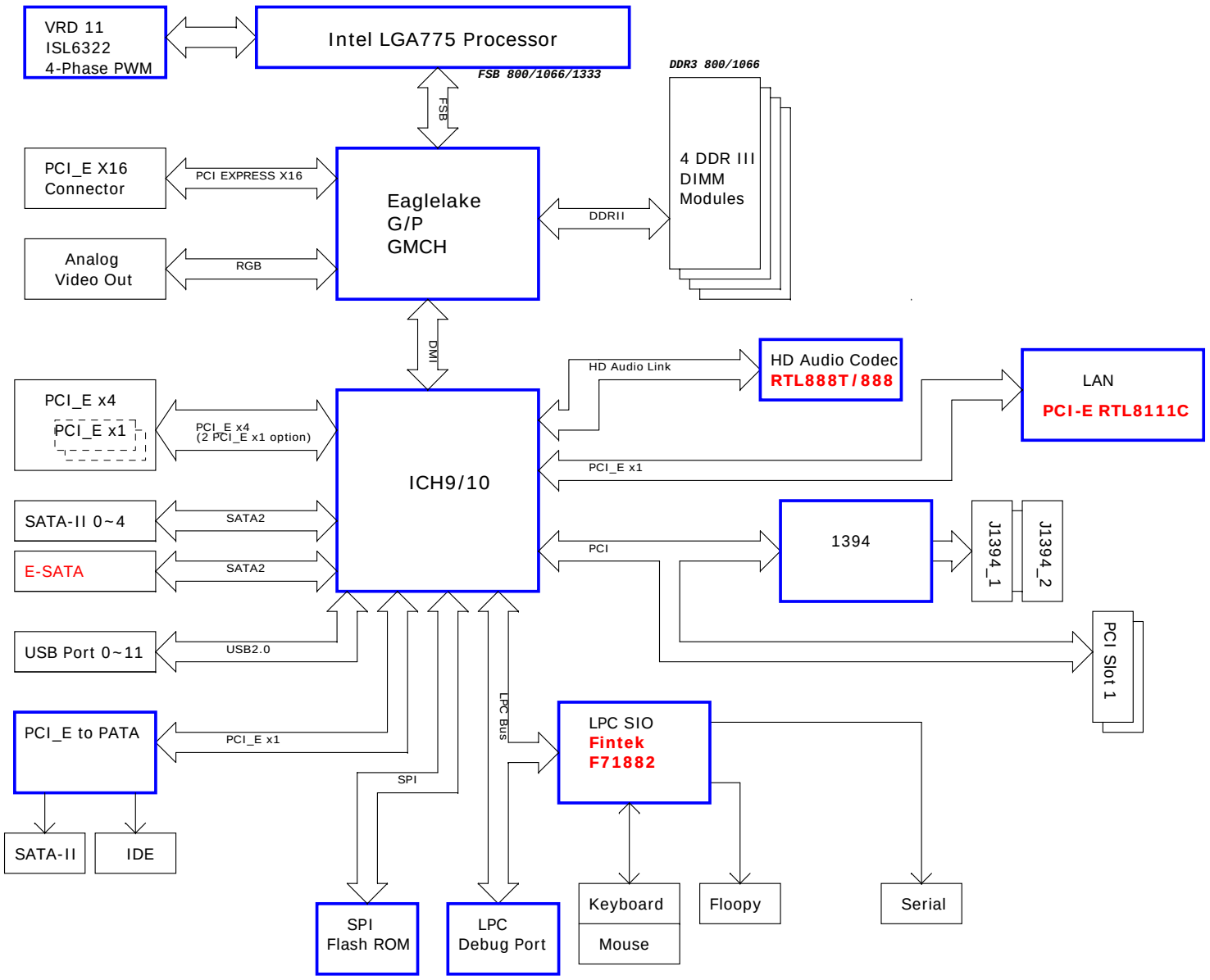
Expansion Slots:

PCI EXPRESS X16 SLOT *1 — Alternative
PCI EXPRESS X8 SLOT *1 — Alternative
PCI EXPRESS X1 SLOT * 2
PCI SLOT * 2

PWM: ISL6336+Dr.Mos

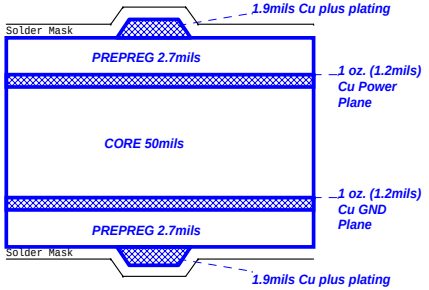
MICRO-STAR INT'L CO.,LTD
MS-7512
Size: Custom | Document Description: COVER SHEET | Rev: 0A
Date: Friday, December 14, 2007 | Sheet 1 of 36

Block Diagram



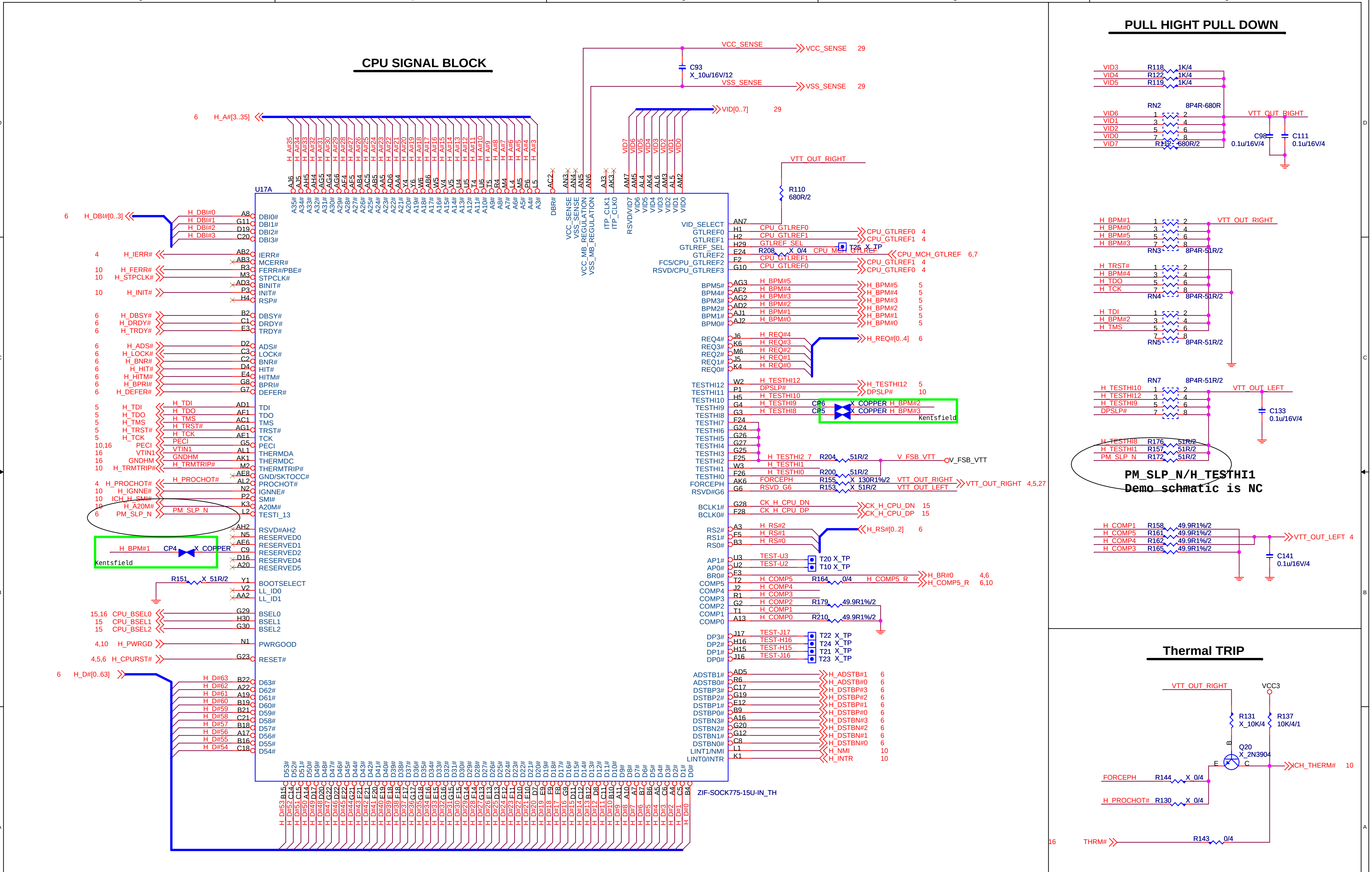
Board Stack-up

(1080 Prepreg Considerations)



Single End 50ohm Top/Bottom : 4mils
USB2.0 - 90ohm : 15/4.5/7.5/4.5/15
SATA - 95ohm : 15/4/8/4/15
LAN - 100ohm : 15/4/8/4/15
PCIE - 95ohm : 15/4/8/4/15
IEEE1394 - 110ohm : 15/4/9/4/15
IDE : 15/4/8/4/15

MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7512	
Size: Custom	Document Description: BLOCK DIAGRAM	Rev: 0A
Date: Friday, December 14, 2007	Sheet 2 of 36	

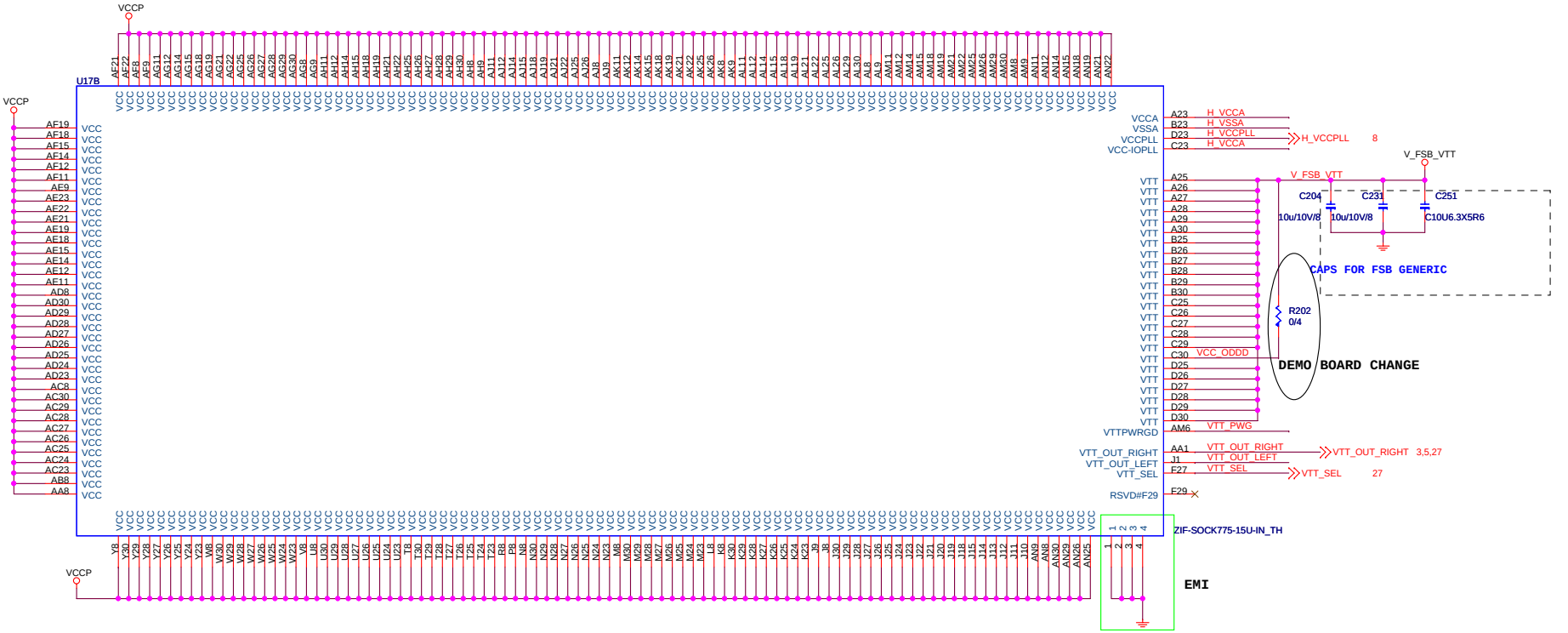


MICRO-STAR INT'L CO.,LTD

MS-7512

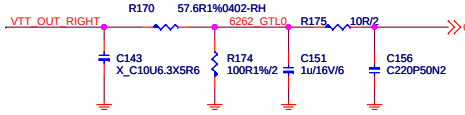
Size	Document Description	Rev
Custom	LGA775 - Signal	0A

Date: Friday, December 21, 2007 | Sheet 3 of 36

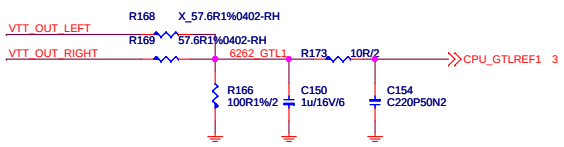


*GTLREF VOLTAGE SHOULD BE
0.635 * VTT = 0.735V (At VTT=1.2V)
0.635 * VTT = 0.7V (At VTT=1.1V)

UPI VOLTAGE CONSOLE

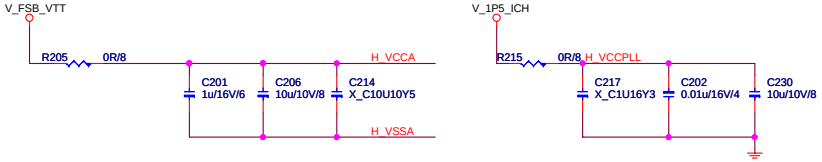


UPI VOLTAGE CONSOLE

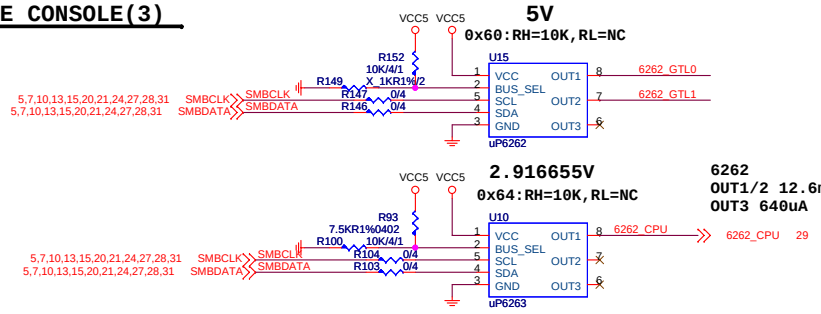


DEMO BOARD CHANGE
(GTLREF0+3/GTLREF1+2)

*PLACE COMPONENTS AS CLOSE AS POSSIBLE TO PROCESSOR SOCKET
*TRACE WIDTH TO CAPS MUST BE NO SMALLER THAN 12MILS

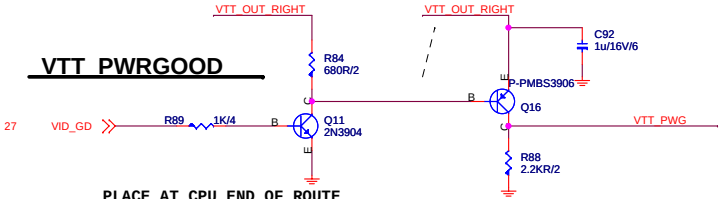


UPI VOLTAGE CONSOLE(3)

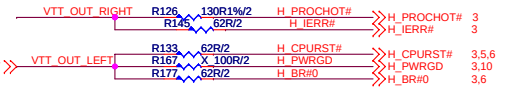


VTT_PWRGOOD

1.2V VTT_PWRGOOD



PLACE AT CPU END OF ROUTE



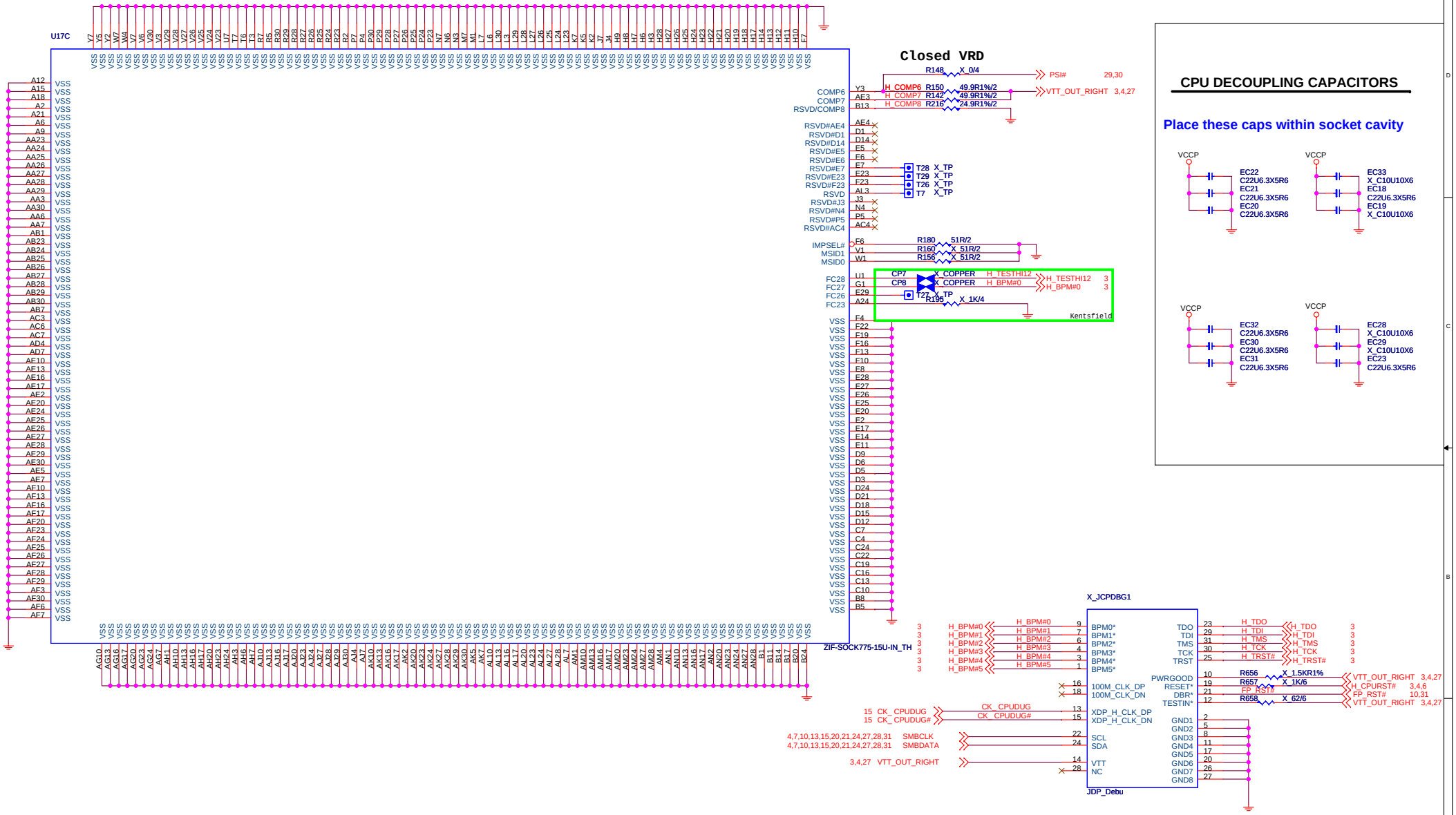
VTT_PWG SPEC :
High > 0.9V
Low < 0.3V
Trise < 150ns

MICRO-STAR INT'L CO.,LTD

MS-7512

Size	Document Description	Rev
Custom	LGA775 - Power	0A

Date: Friday, December 21, 2007 | Sheet 4 of 36


U17C
Closed VRD
R148 X_0/4
PSI# 29,30
H_COMP6 R150 49.9R1%/2
H_COMP7 R142 49.9R1%/2
H_COMP8 R216 24.9R1%/2
VTT_OUT_RIGHT 3,4,27
T28 X_TP
T29 X_TP
T26 X_TP
T7 X_TP
R180 51R/2
R160 X_51R/2
R156 X_51R/2
CP7 X_COPPER H_TESTHI12
CP8 X_COPPER H_BPM#0
T27 X_TP
R199 X_1K/4
H_TESTHI12 3
H_BPM#0 3
Kentsfield
ZIF-SOCK775-15U-IN_TH
X_JCPDBG1
JDP_Debu
BPM0*
BPM1*
BPM2*
BPM3*
BPM4*
BPM5*
100M_CLK_DP
100M_CLK_DN
XDP_H_CLK_DP
XDP_H_CLK_DN
SCL
SDA
VTT
NC
TDO
TDI
TMS
TCK
TRST
PWRGOOD
RESET*
DBR*
TESTIN*
H_TDO
H_TDI
H_TMS
H_TCK
H_TRST#
R656 X_1.5KR1%
R657 X_1K/6
R658 X_62/6
FP_RST#
H_CPURST# 3,4,6
FP_RST# 10,31
VTT_OUT_RIGHT 3,4,27
CK_CPUDUG
CK_CPUDUG#
SMBCLK
SMBDATA
GND1
GND2
GND3
GND4
GND5
GND6
GND7
GND8
CPU DECOUPLING CAPACITORS
Place these caps within socket cavity
VCCP
EC22 C22U6.3X5R6
EC21 C22U6.3X5R6
EC20 C22U6.3X5R6
EC33 X_C10U10X6
EC18 C22U6.3X5R6
EC19 X_C10U10X6
EC32 C22U6.3X5R6
EC30 C22U6.3X5R6
EC31 C22U6.3X5R6
EC28 X_C10U10X6
EC29 X_C10U10X6
EC23 C22U6.3X5R6
MICRO-STAR INT'L CO.,LTD
MS-7512
Size Custom
Document Description LGA775 - GND
Rev 0A
Date: Friday, December 21, 2007
Sheet 5 of 36

NB1A
EAGLELAKE_DDR2
SYM_REV = 1.5
FSB
1 OF 7

NB1B
EAGLELAKE_DDR2
SYM_REV = 1.5
PCIE
DMI
2 OF 7

NB1E
EAGLELAKE_DDR2
SYM_REV = 1.5
VGA
MISC
5 OF 7

ELK_CRB

A minimum of one (1) stitching cap can be shared by up to four different pairs as long as each pair is with in the distances stated above.

DEMO BOARD CHANGE

*GTLREF VOLTAGE SHOULD BE 0.67*VTT=0.8V (At VTT=1.2V)

UPI VOLTAGE CONSOLE

HXSWING SHOULD BE 1/4*VTT

CL_VREF_MCH = 0.35V Close to GMCH

Intel review CHANGE

ITPM_ENB
Itegrated TPM Enable:
0=Enable iTPM
1=Disable iTPM

DualX8_Enable
0=2X8 PCIe Ports Enable
1=1X16 PCIe Port Enable

Primary _PEG_Presence
Primary PCIe port Detect:
0=PCIe Card is in Primary Slot
1=PCIe Card is not in Primary Slot

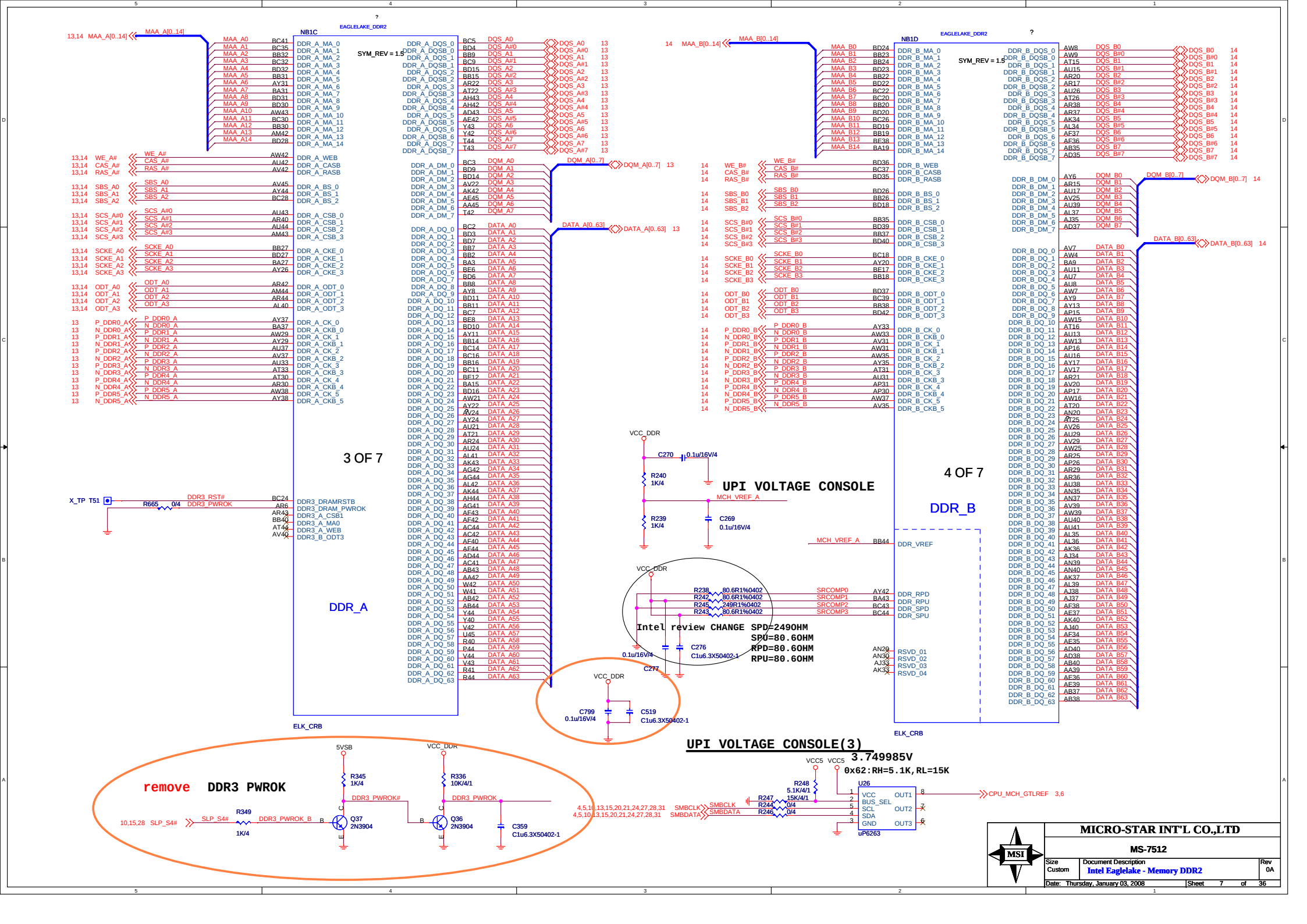
DEMO BOARD FOR NON AUDIO-CAPABLE DIGITAL DISPLAY

PIN	H	L	Description
EXP_SLR EXP_EN MCH_TCEN	Normal Concurrent Enable	Reverse Non-concurrent Disable	PCI_E Lane Reversal PCI_E/SDVO co-existence TLS confidentiality

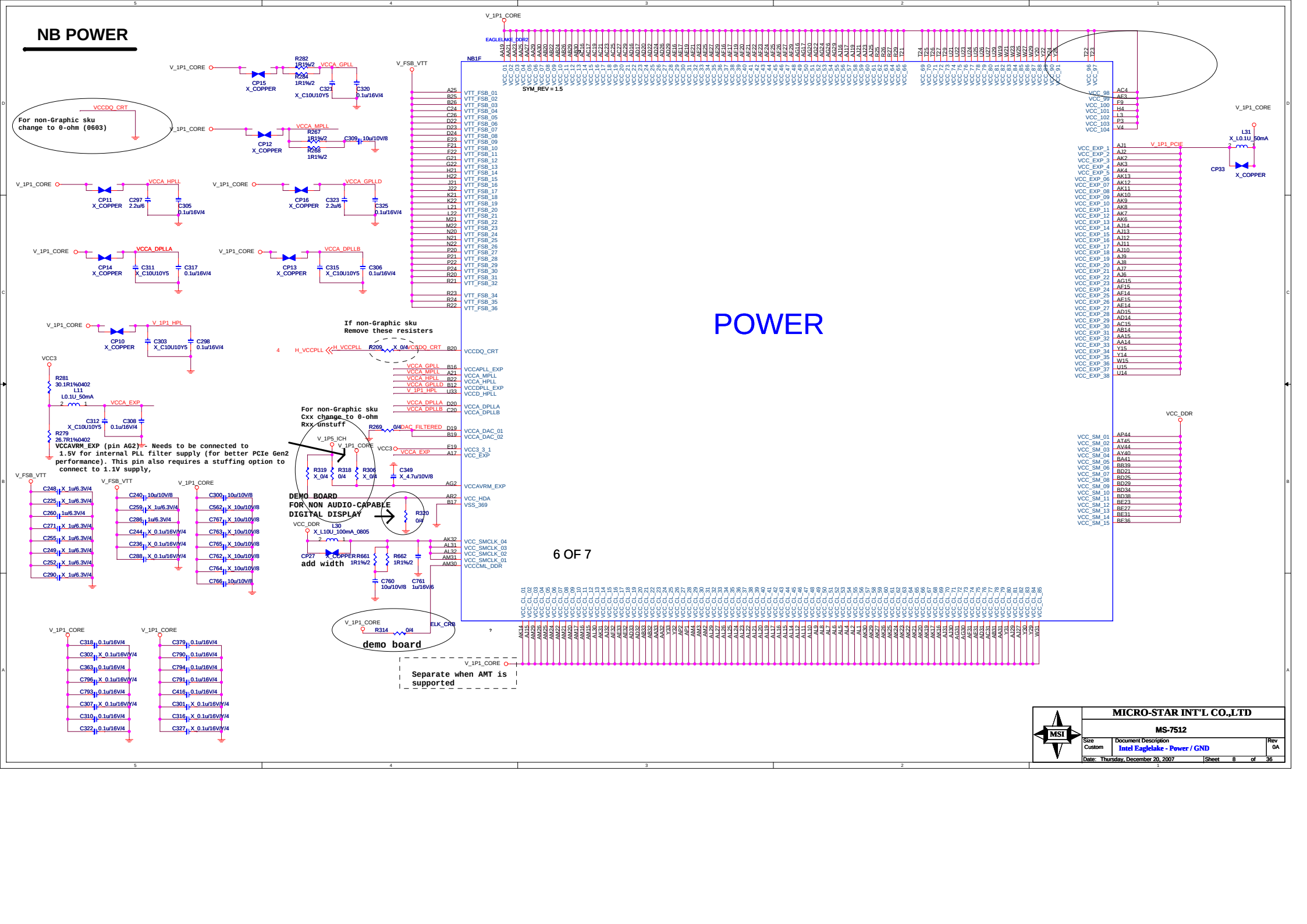
MICRO-STAR INT'L CO.,LTD

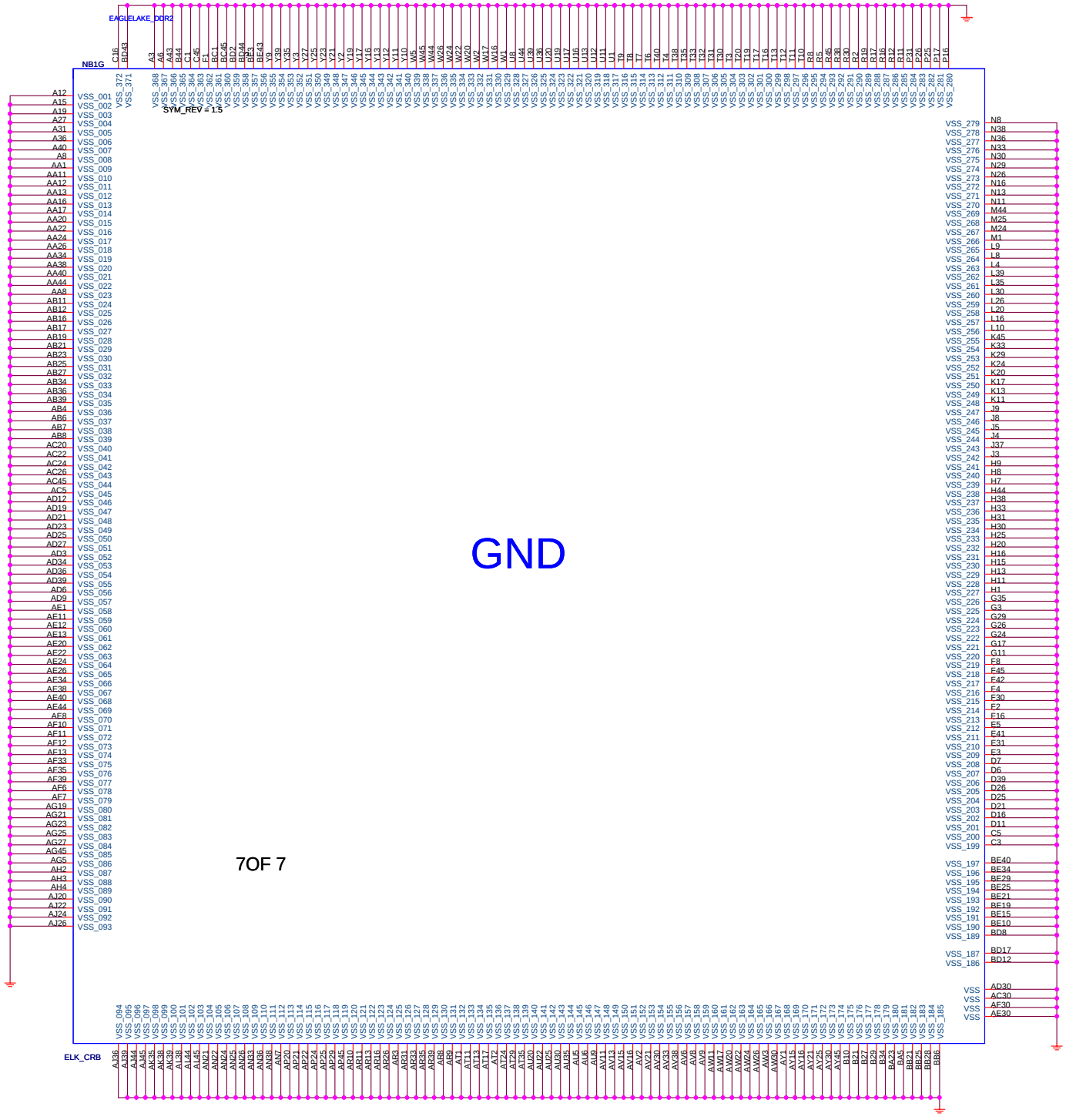
MS-7512

Size	Document Description	Rev
Custom	Intel Eaglelake - FSB, PCIE, DMI, VGA, MSIC	0A
Date: Wednesday, December 19, 2007	Sheet 6 of 36	

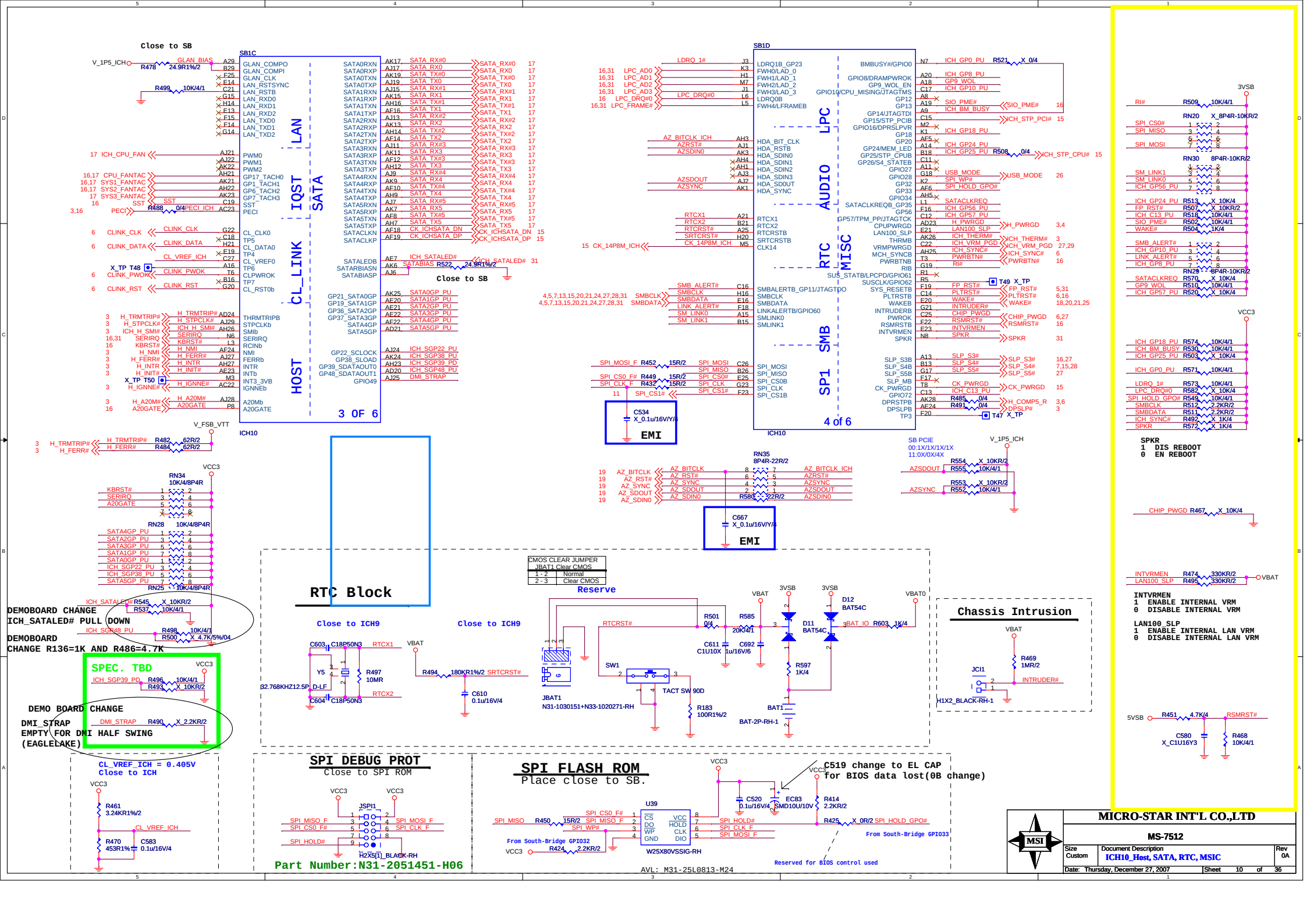

NB1C
EAGLELAKE_DDR2
SYM_REV = 1.5
3 OF 7
DDR_A
ELK_CRB
NB1D
4 OF 7
DDR_B
UPI VOLTAGE CONSOLE
Intel review CHANGE SPD=249OHM
SPU=80.6OHM
RPD=80.6OHM
RPU=80.6OHM
UPI VOLTAGE CONSOLE(3)
3.749985V
0x62:RH=5.1K,RL=15K
remove DDR3 PWROK
uP6263
MICRO-STAR INT'L CO.,LTD
MS-7512
Intel Eaglelake - Memory DDR2
Size Custom
Rev 0A
Date: Thursday, January 03, 2008
Sheet 7 of 36

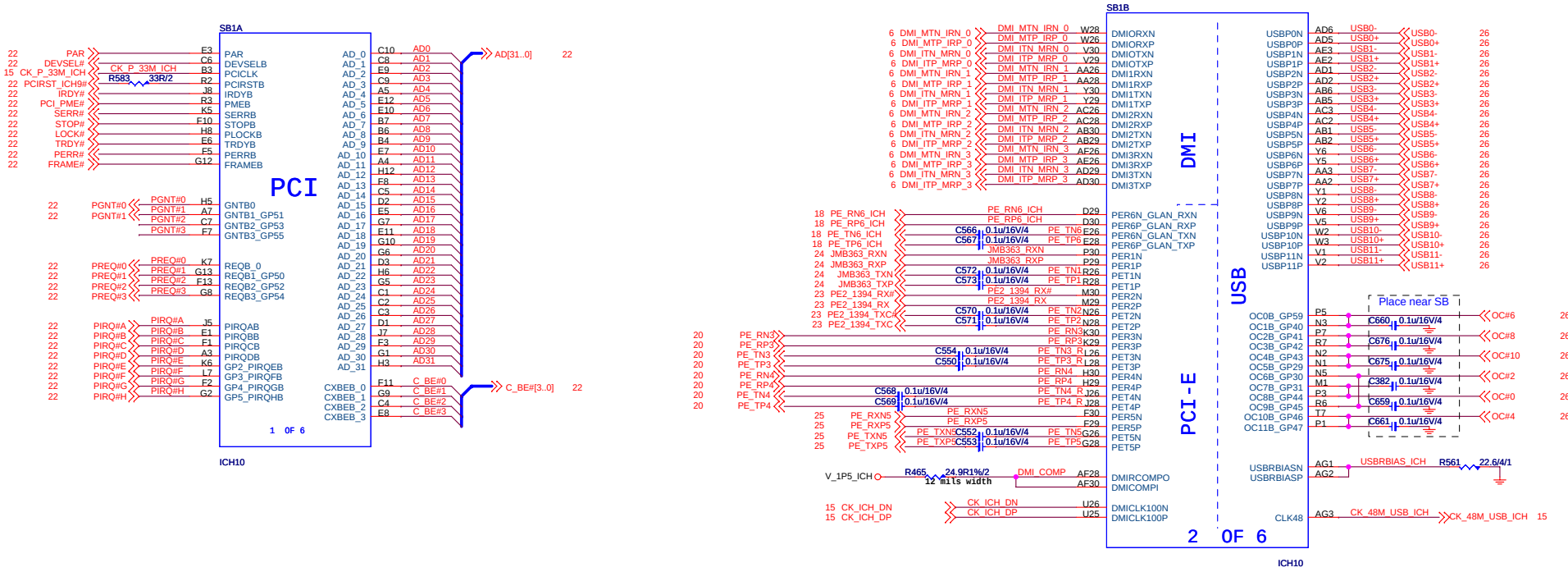
NB POWER


POWER
6 OF 7
NB1F
EAGLELAKE_DDR2
SYM_REV = 1.5
V_1P1_CORE
V_FSB_VTT
VCCDQ_CRT
For non-Graphic sku
change to 0-ohm (0603)
VCCA_GPLL
VCCA_MPLL
VCCA_HPLL
VCCA_GPLLD
VCCA_DPLLA
VCCA_DPLLB
V_1P1_HPL
VCC3
VCCA_EXP
If non-Graphic sku
Remove these resisters
For non-Graphic sku
Cxx change to 0-ohm
Rxx unstuff
VCCAVRM_EXP (pin AG2) - Needs to be connected to
1.5V for internal PLL filter supply (for better PCIe Gen2
performance). This pin also requires a stuffing option to
connect to 1.1V supply,
V_1P5_ICH
DEMO BOARD
FOR NON AUDIO-CAPABLE
DIGITAL DISPLAY
VCC_DDR
add width
demo board
V_1P1_PCIE
Separate when AMT is
supported
MICRO-STAR INT'L CO.,LTD
MS-7512
Intel Eaglelake - Power / GND
Date: Thursday, December 20, 2007
Sheet 8 of 36

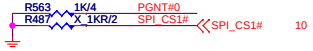


MICRO-STAR INT'L CO.,LTD	
MS-7512	
Size: Custom	Document Description: EagleLake-GND
Rev: 0A	
Date: Wednesday, December 19, 2007	Sheet 9 of 36

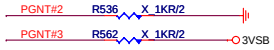

Close to SB
SB1C
LAN
IQST
SATA
CL_LINK
HOST
3 OF 6
ICH10
SB1D
LPC
AUDIO
RTC
MISC
SMB
SPI
4 of 6
Close to SB
EMI
C534 X_0.1u/16V/Y/4
C667 X_0.1u/16V/Y/4
RTC Block
Close to ICH9
Close to ICH9
Reserve
CMOS CLEAR JUMPER
JBAT1 Clear CMOS
1 - 2 Normal
2 - 3 Clear CMOS
JBAT1
N31-1030151+N33-1020271-RH
TACT SW 90D
BAT-2P-RH-1
Chassis Intrusion
H1X2_BLACK-RH-1
DEMOBOARD CHANGE
ICH_SATALED# PULL DOWN
DEMOBOARD
CHANGE R136=1K AND R486=4.7K
SPEC. TBD
DEMO BOARD CHANGE
DMI_STRAP
EMPTY FOR DMI HALF SWING
(EAGLELAKE)
CL_VREF_ICH = 0.405V
Close to ICH
SPI DEBUG PROT
Close to SPI ROM
Part Number:N31-2051451-H06
SPI FLASH ROM
Place close to SB.
C519 change to EL CAP
for BIOS data lost(0B change)
W25X80VSSIG-RH
From South-Bridge GPIO32
From South-Bridge GPIO33
Reserved for BIOS control used
AVL: M31-25L0813-M24
SPKR
1 DIS REBOOT
0 EN REBOOT
INTVRMEN
1 ENABLE INTERNAL VRM
0 DISABLE INTERNAL VRM
LAN100_SLP
1 ENABLE INTERNAL LAN VRM
0 DISABLE INTERNAL LAN VRM
MICRO-STAR INT'L CO.,LTD
MS-7512
ICH10_Host, SATA, RTC, MSIC
Size Custom
Rev 0A
Date: Thursday, December 27, 2007
Sheet 10 of 36



SB STRAPPING RESISTOR



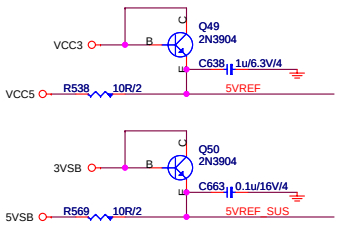
BOOT SELECT STRAPS		
BOOT DEVICE	GNT#0	SPI_CS1#
FWH	1	1
SPI	0	X
PCI	1	0



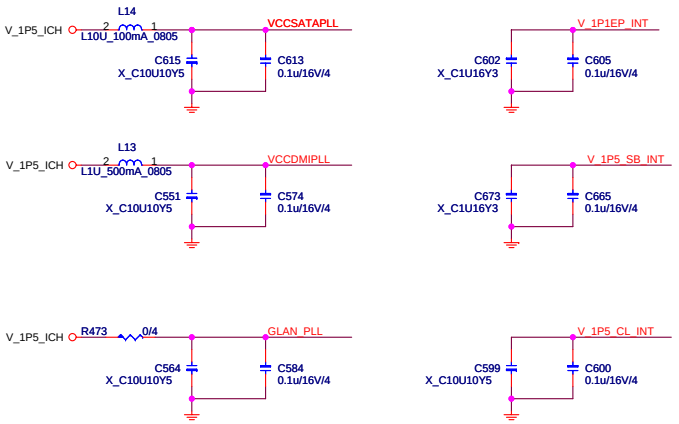
SIGNAL	H	L	DES.
GNT3	DIS	EN	A16 OVERIDE
GNT2	N/A	SET BIT	PCIE PORT CONFIG 2 BIT 0 (5-6)

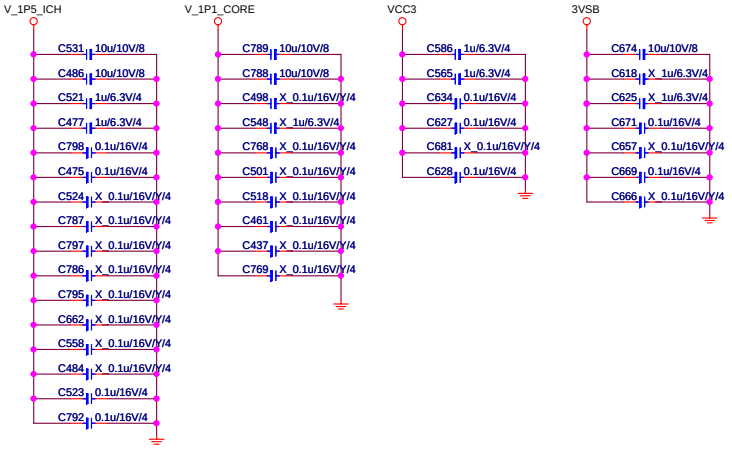
MICRO-STAR INT'L CO.,LTD		
MS-7512		
Size: Custom	Document Description: ICH10_PCI, USB, DMI, PCIEx1	Rev: 0A
Date: Wednesday, December 19, 2007	Sheet 11 of 36	

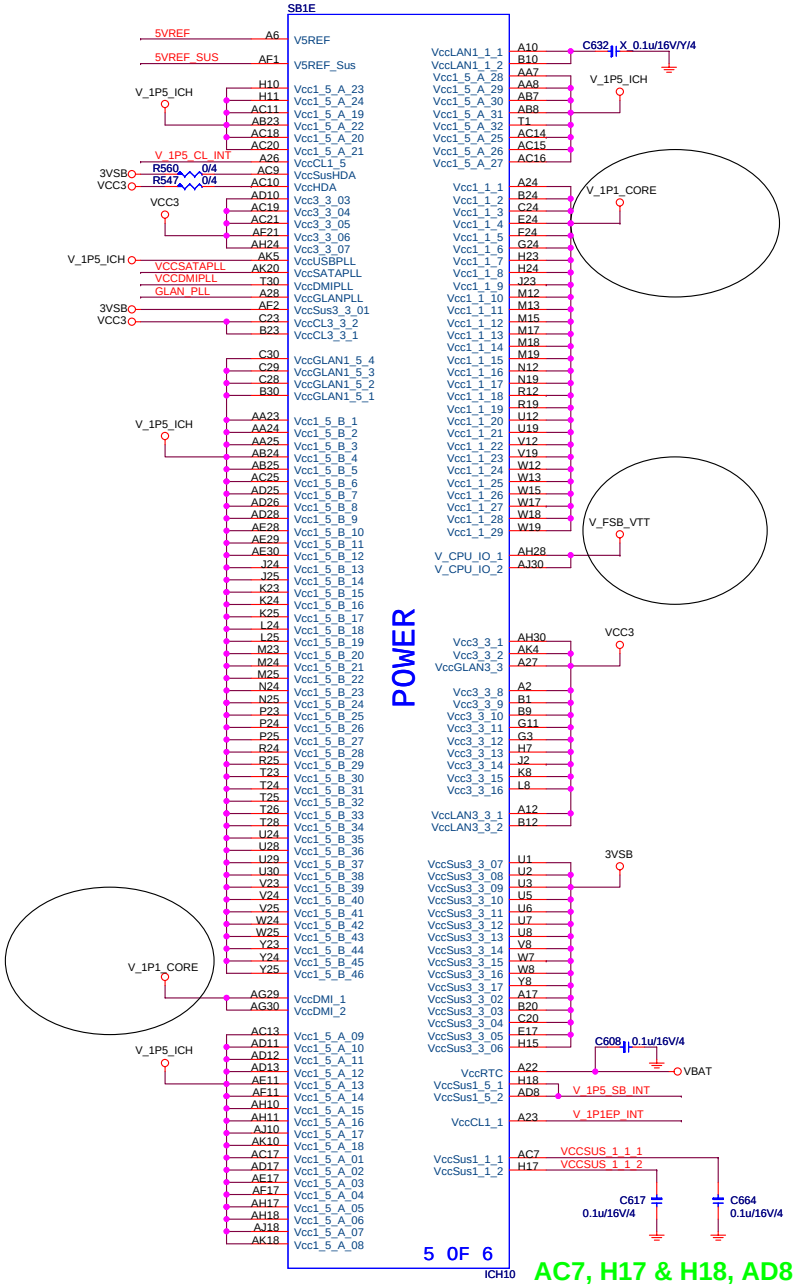
5VREF & 5VREF_SUS Sequencing Circuit

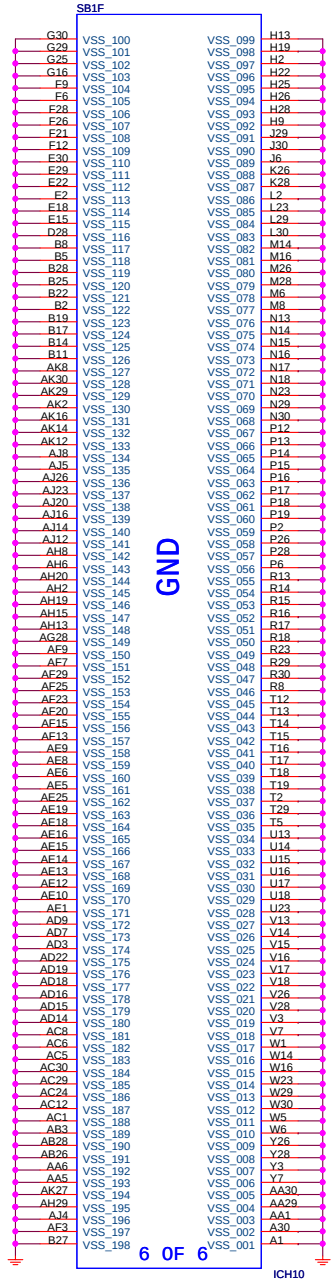


SB POWER







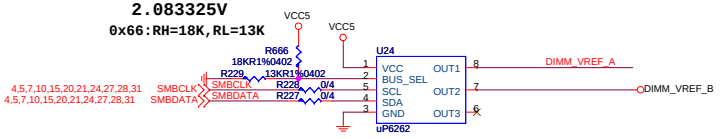


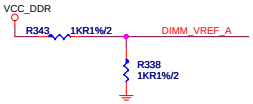
MICRO-STAR INT'L CO.,LTD		
MS-7512		
Size: Custom	Document Description: ICH9/10 - Power, GND	Rev: 0A
Date: Wednesday, December 19, 2007	Sheet 12 of 36	

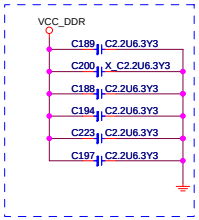
DDRII DIMM_A1

DDRII DIMM_A2

UPI VOLTAGE CONSOLE(3+1)

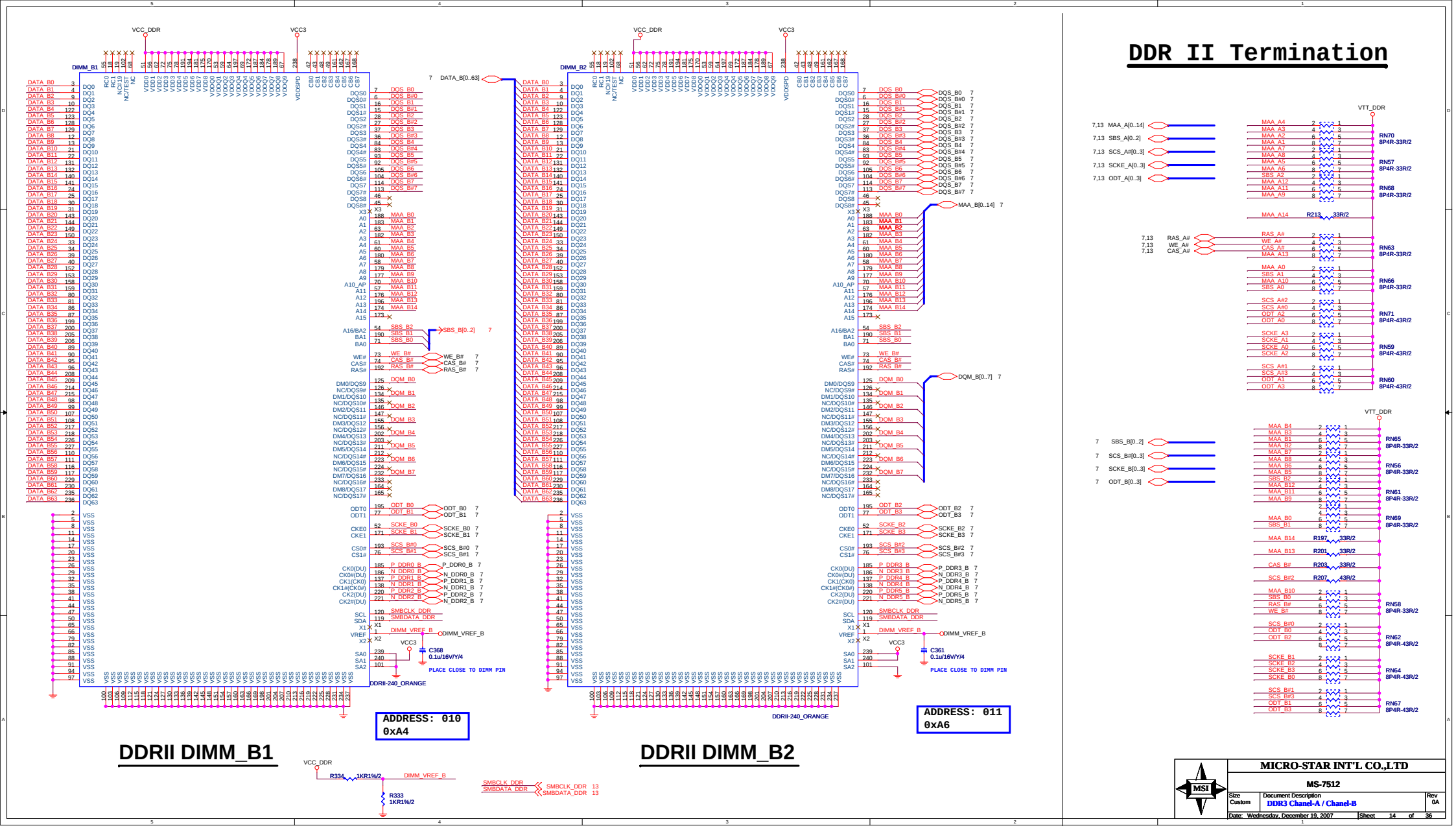






MICRO-STAR INT'L CO.,LTD		
MS-7512		
Size: Custom	Document Description: DDR3 Chanel-A / Chanel-B	Rev: 0A
Date: Thursday, December 27, 2007	Sheet 13 of 36	

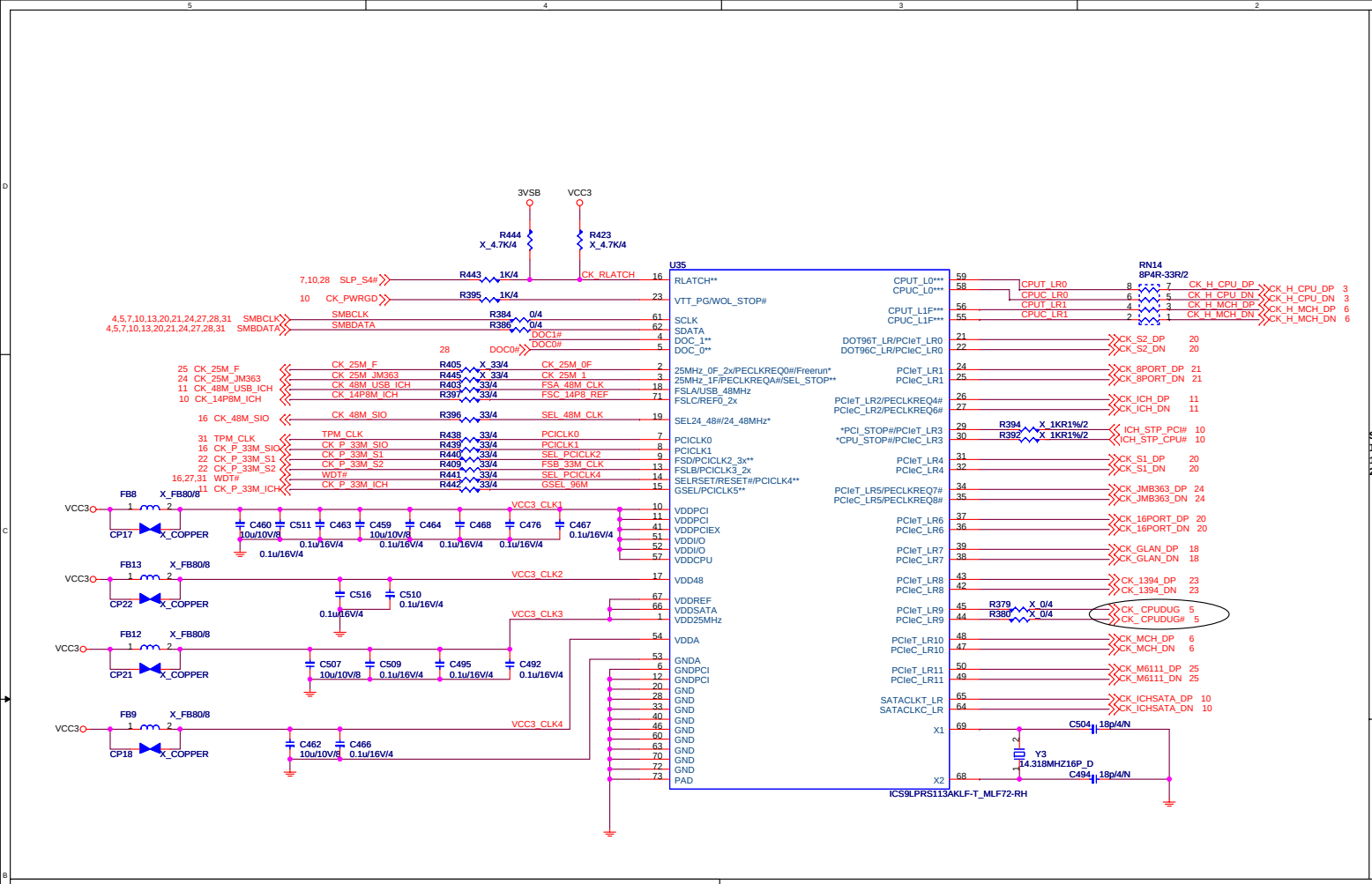
DDR II Termination



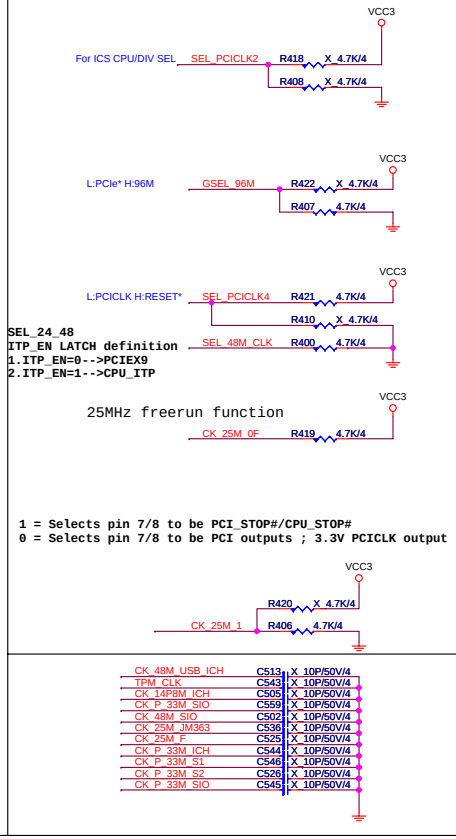
DDRII DIMM_B1

DDRII DIMM_B2

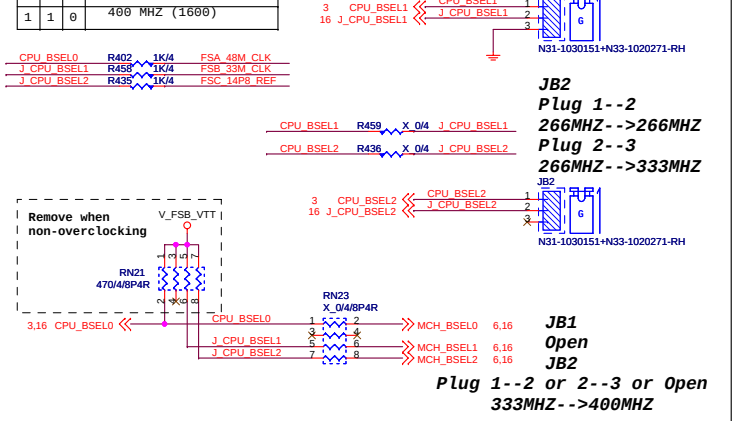
MICRO-STAR INT'L CO.,LTD	
MS-7512	
Size: Custom	Document Description: DDR3 Chanel-A / Chanel-B
Rev: 0A	
Date: Wednesday, December 19, 2007	Sheet 14 of 36

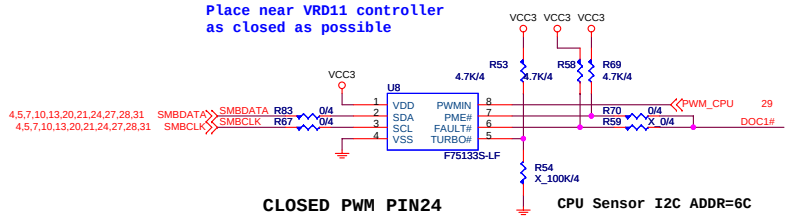


CLOCK GEN STRAPING



BSEL			TABLE
2	1	0	FSB FREQUENCY
0	0	0	266 MHz (1066)
1	0	0	333 MHZ (1333)
0	1	0	200 MHZ (800)
1	1	0	400 MHZ (1600)





EASY DOT FUNCTION

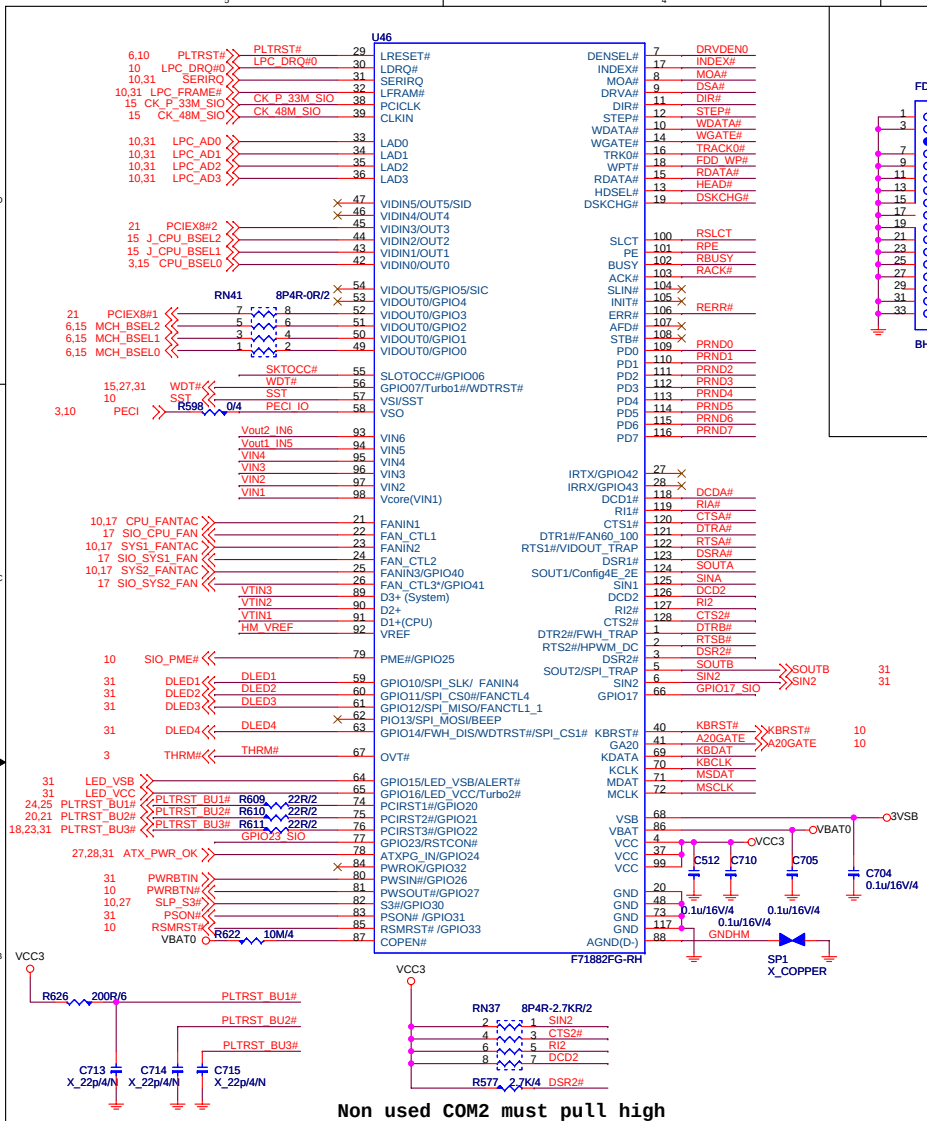
DOC#0	DOC#1	Over-clk
1	1	15%
0	1	10%
1	0	5%
0	0	Normal

MICRO-STAR INT'L CO.,LTD

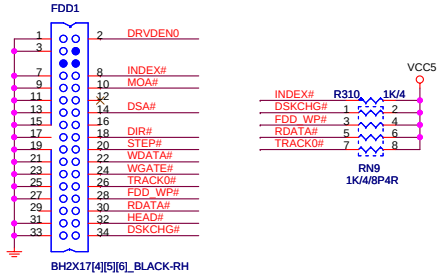
MS-7512

Size	Document Description	Rev
Custom	Clock Gen ICS9LPRS110	0A

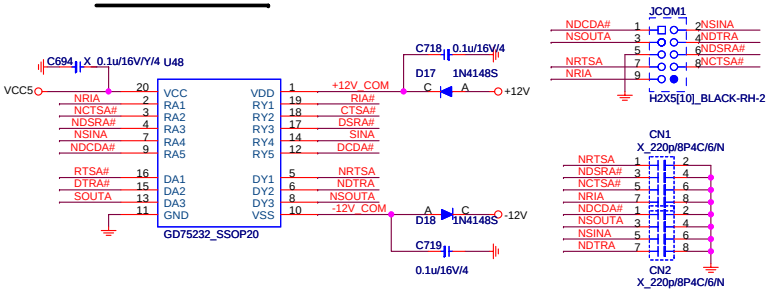
Date: Wednesday, December 19, 2007 Sheet 15 of 36



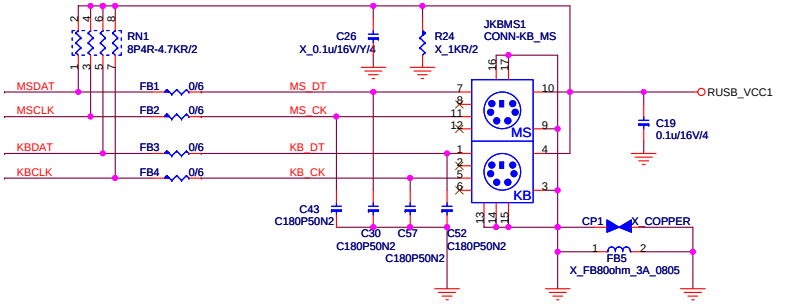
FLOPPY CONNECTOR



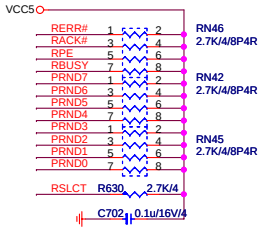
SERIAL PORT 1



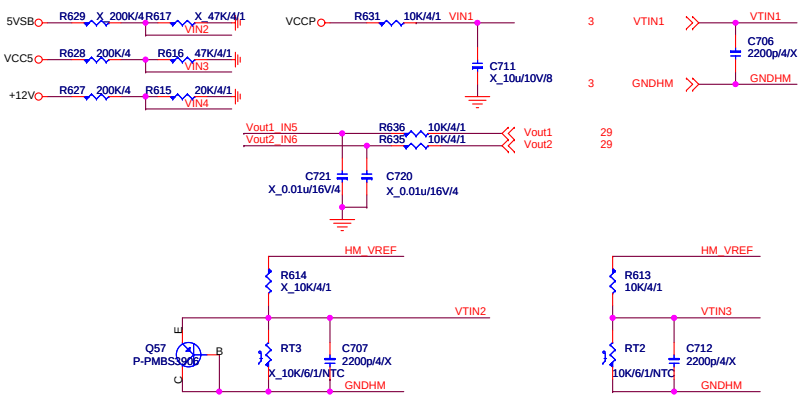
PS2 KEYBOARD & MOUSE CONNECTOR



PARALLAL PORT

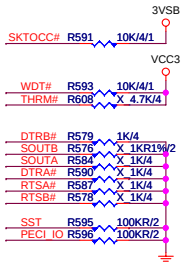


Thermal Resistor

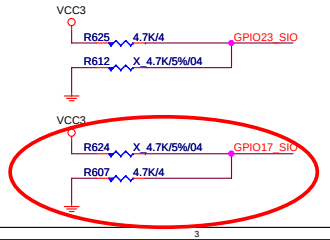


LPC I/O STRAPPING RESISTOR

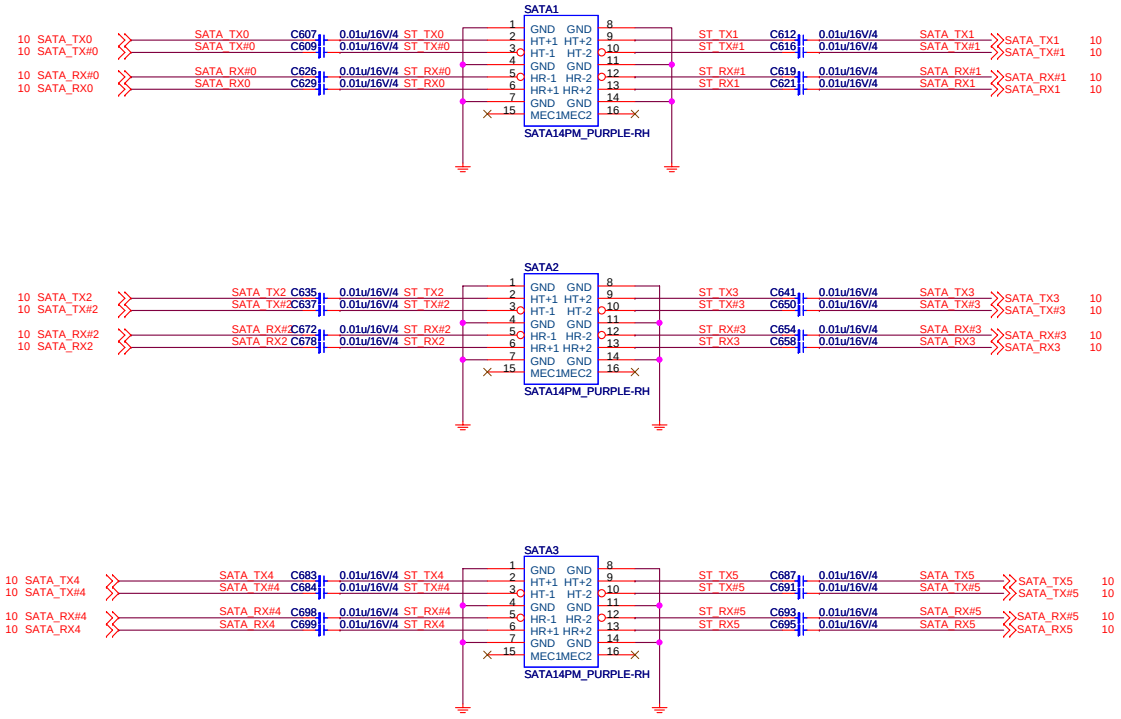
STRAP	Don't STUFF	STUFF
SOUTA	4E	2E
DTRA#	FAN START DUTY 60%	FAN START DUTY 100%
RTSA#	PIN49~54 = VID_OUT PIN42~47 = VID_IN	PIN49~54 = GPIO PIN42~47 = VIDIN/OUT
SOUTB	SPI_DISABLE	SPI_ENABLE
DTRB#	SPI_Backup	SPI_Primary
RTSB#	PWM_FAN	LINEAR_FAN

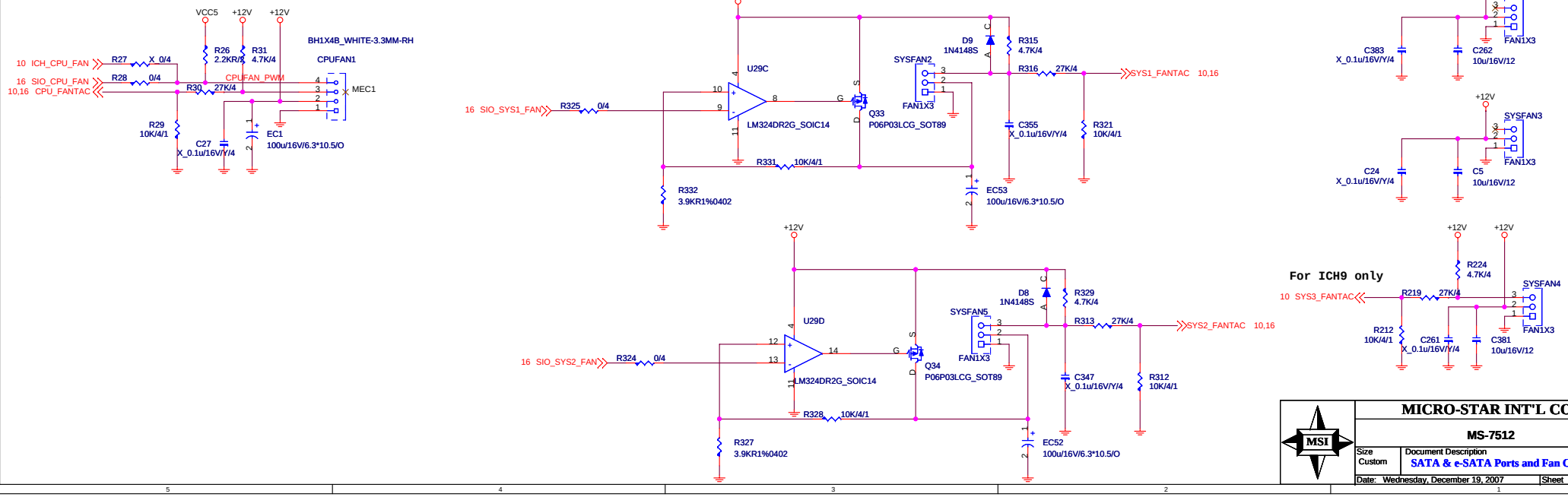


GPIO	GPIO17	GPIO23
ALC888	0	1
ALC888T	1	1



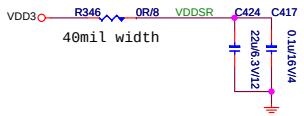
MICRO-STAR INT'L CO.,LTD	
MS-7512	
Size: Custom	Document Description: SIO-Fintek F17882F/COM
Rev: 0A	
Date: Thursday, December 27, 2007	Sheet 16 of 36



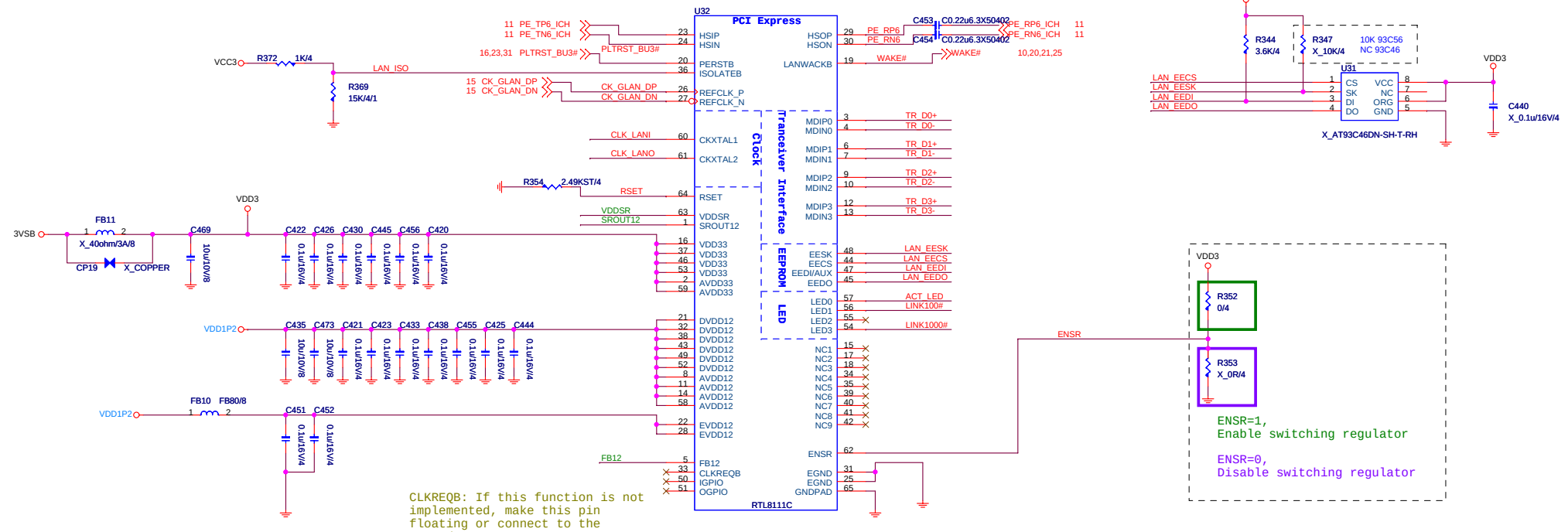


MICRO-STAR INT'L CO.,LTD		
MS-7512		
Size: Custom	Document Description: SATA & e-SATA Ports and Fan Control	Rev: 0A
Date: Wednesday, December 19, 2007	Sheet 17 of 36	

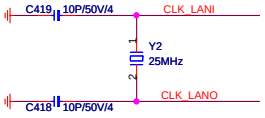
For the power pin of the switching regulator,
Disable switching regulator: Remove R27, C20, C21,D3

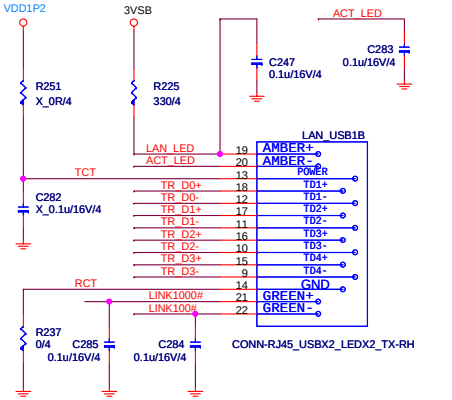


C657 C346 near Pin63 200mil,C346 must be nearly Pin63



CLKREQB: If this function is not implemented, make this pin floating or connect to the ground.





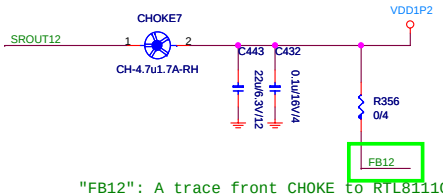
Giga-Lan
N58-22F0181-S42

Link	Yellow
Active	Blinking
1000	Orange
100	Green
10	None

19 — 20 Yellow

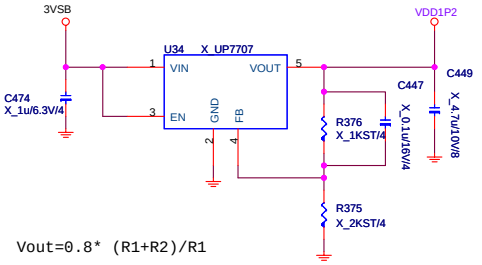
Orange — 21 — 22 Green

Choke C656 C345 near Pin1 200mil



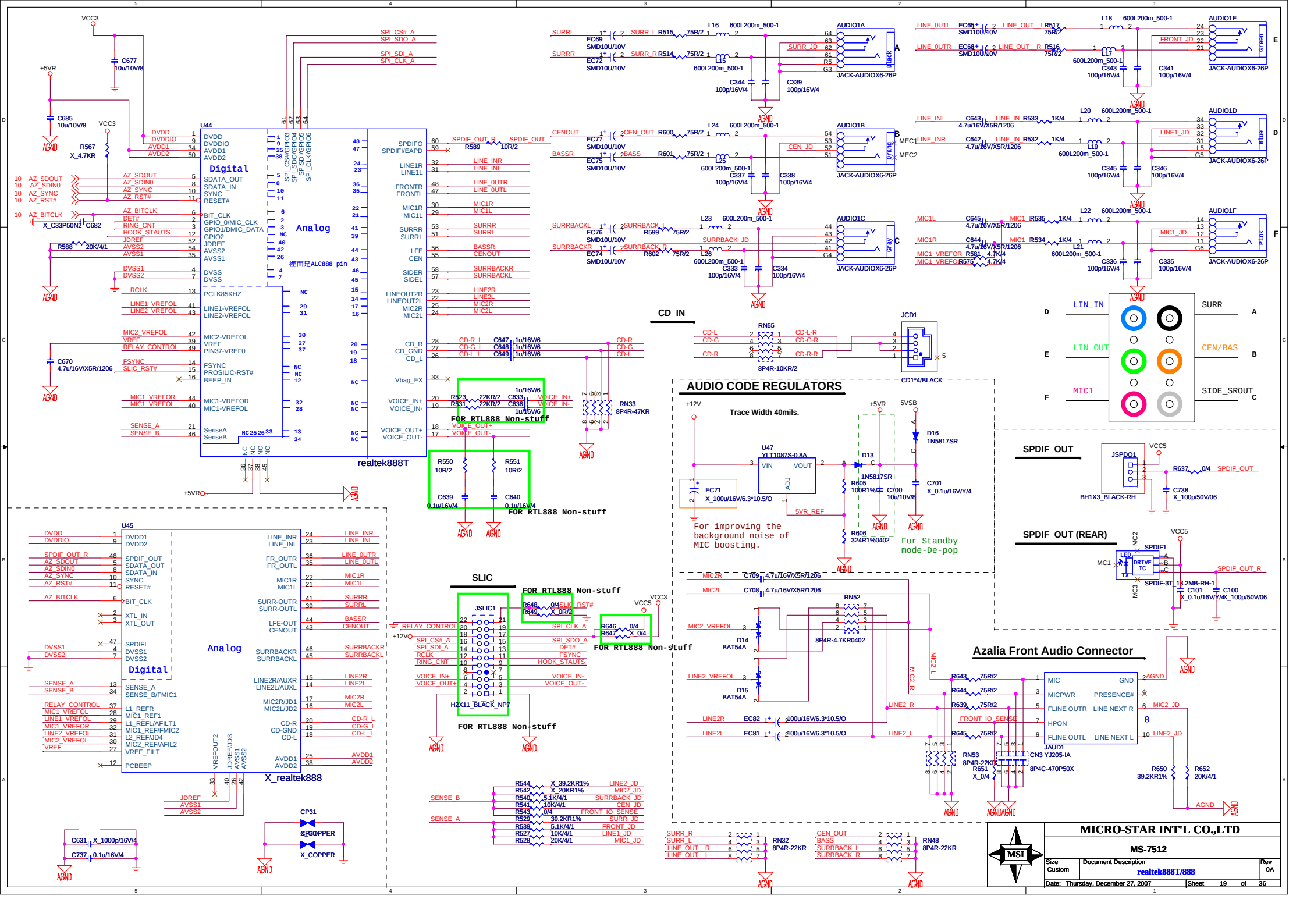
"FB12": A trace front CHOKE to RTL8111C pin5

8111C switching regulator disabled

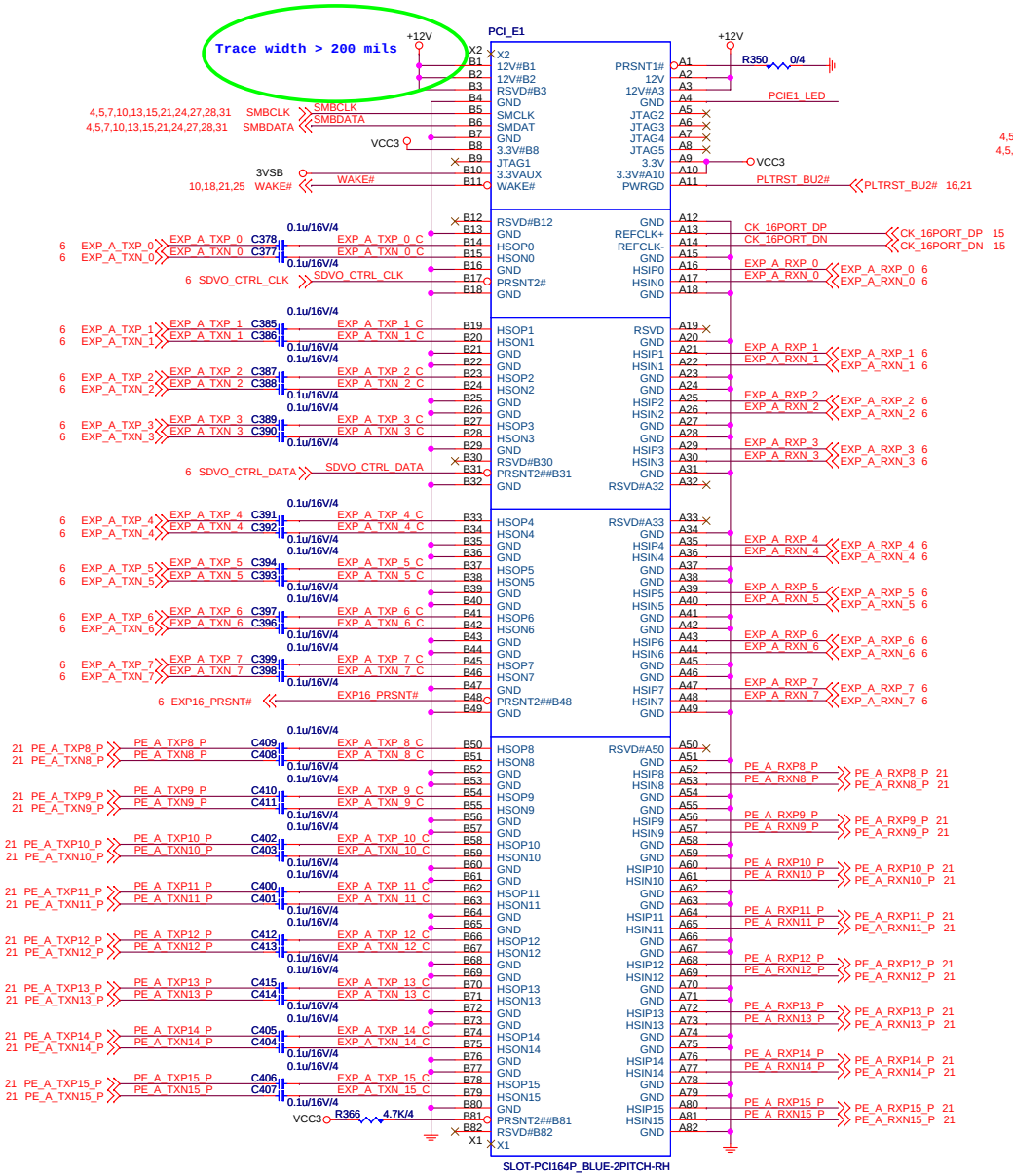


Vout=0.8* (R1+R2)/R1

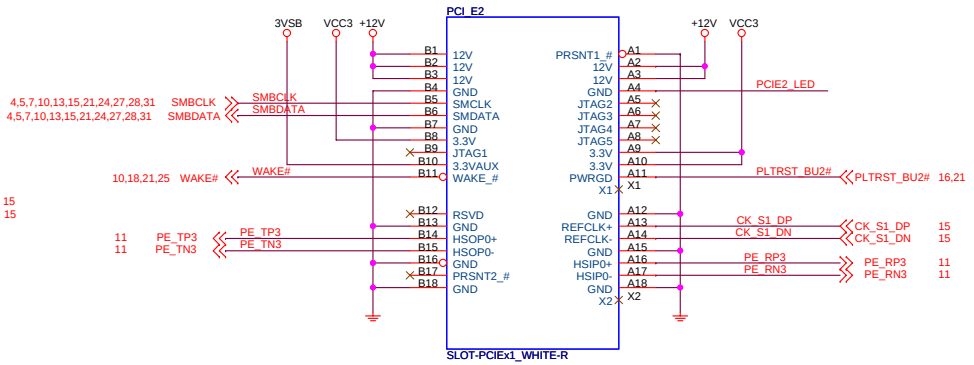
MICRO-STAR INT'L CO.,LTD			
MS-7512			
Size: Custom	Document Description: LAN Realtek RTL8111C(PCIE)		Rev: 0A
Date: Thursday, December 27, 2007		Sheet 18 of 36	


realtek888T
裡面是ALC888 pin
AUDIO CODE REGULATORS
Trace Width 40mils.
For improving the background noise of MIC boosting.
For Standby mode-De-pop
CD_IN
SLIC
FOR RTL888 Non-stuff
SPDIF OUT
SPDIF OUT (REAR)
Azalia Front Audio Connector
X_realtek888
MICRO-STAR INT'L CO.,LTD
MS-7512
realtek888T/888

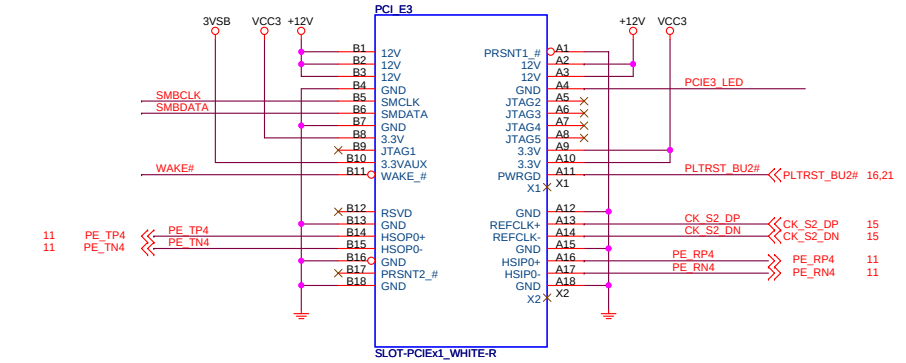
PCI_Express X16 Slot

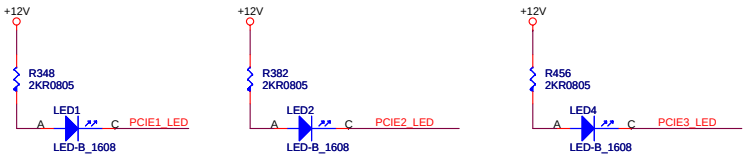


PCI EXPRESS x1-PORT



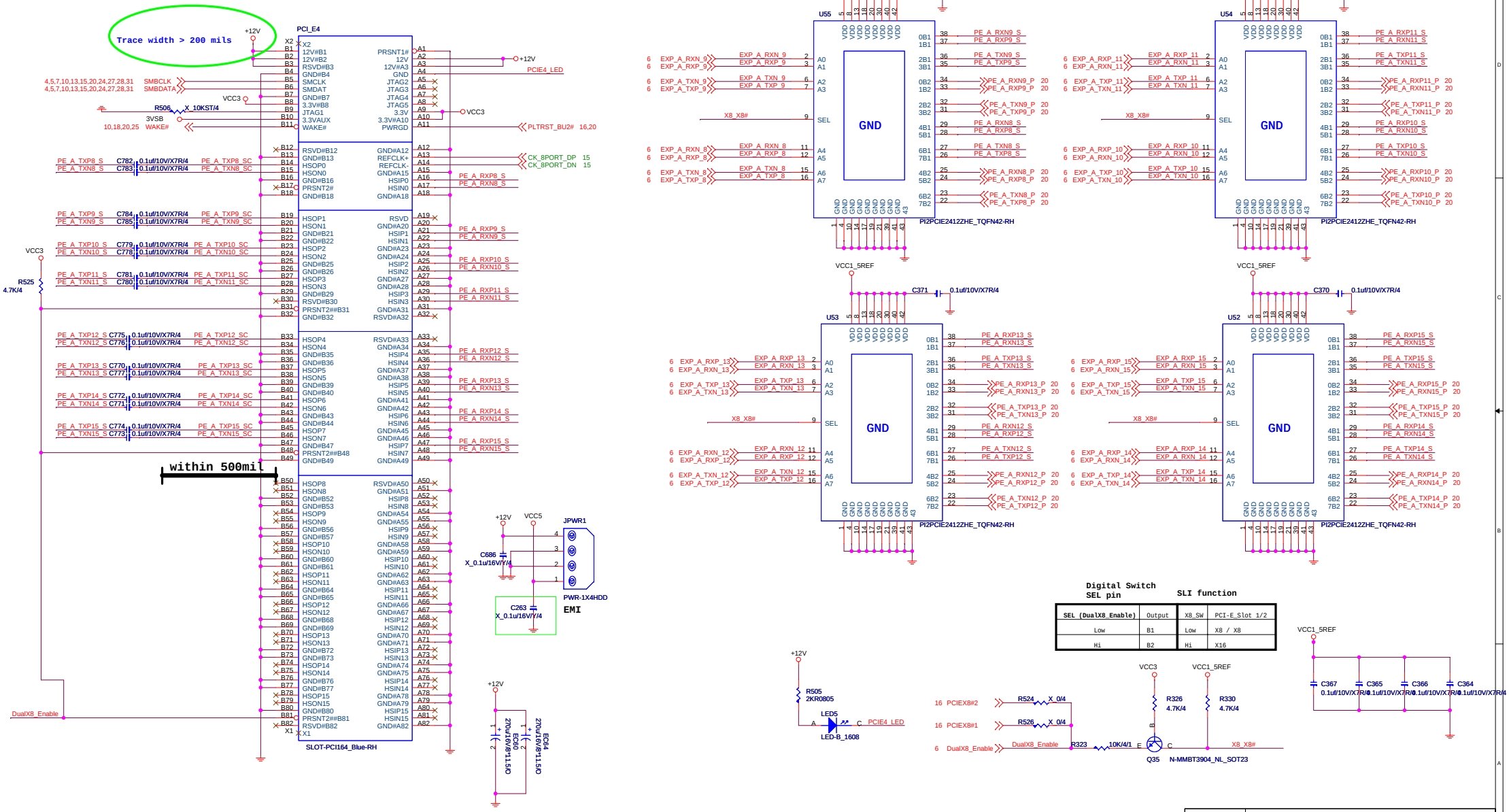
PCI EXPRESS x1-PORT





MICRO-STAR INT'L CO.,LTD		
MS-7512		
Size: Custom	Document Description: PCIE x16, x1	Rev: 0A
Date: Wednesday, December 19, 2007	Sheet 20 of 36	

PCI_Express X8 Slot
(Share with PCI_E x16 Slots)



Digital Switch SEL pin — SLI function

SEL (DualX8_Enable)	Output	X8_SW	PCI-E_Slot 1/2
Low	B1	Low	X8 / X8
Hi	B2	Hi	X16

C367 C365 C366 C364 0.1uf/10V/X7R/4

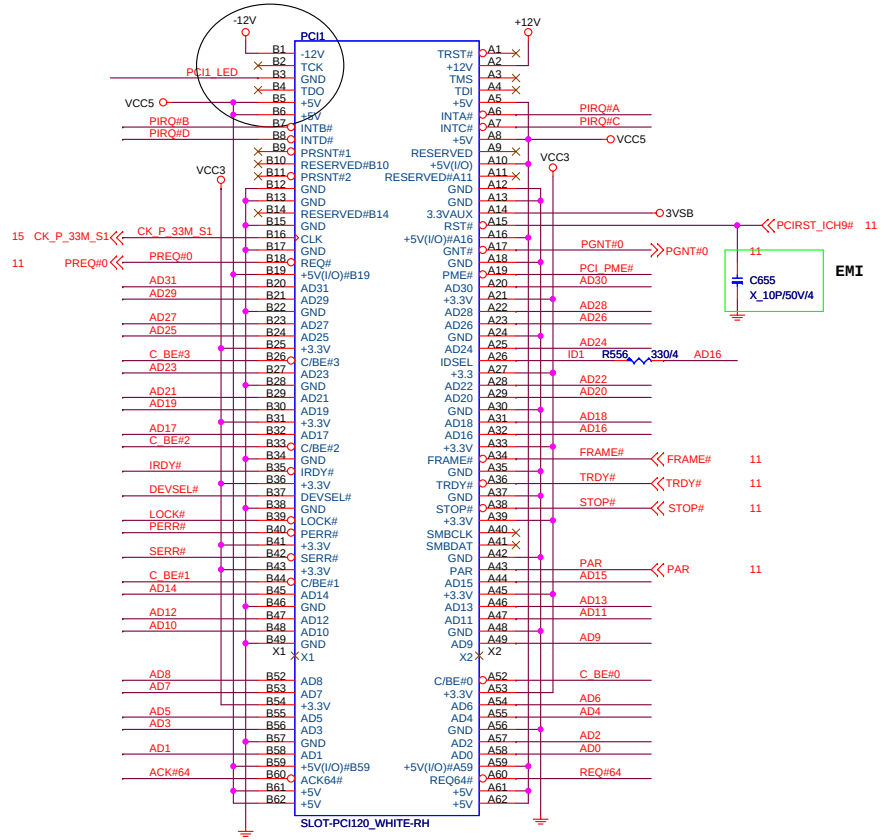
MICRO-STAR INT'L CO.,LTD

MS-7512

Size: Custom | Document Description: PCIEx8/Pericom switch | Rev: 0A

Date: Wednesday, December 19, 2007 | Sheet 21 of 36

PCI SLOT 1 (PCI VER: 2.2 COMPLY)

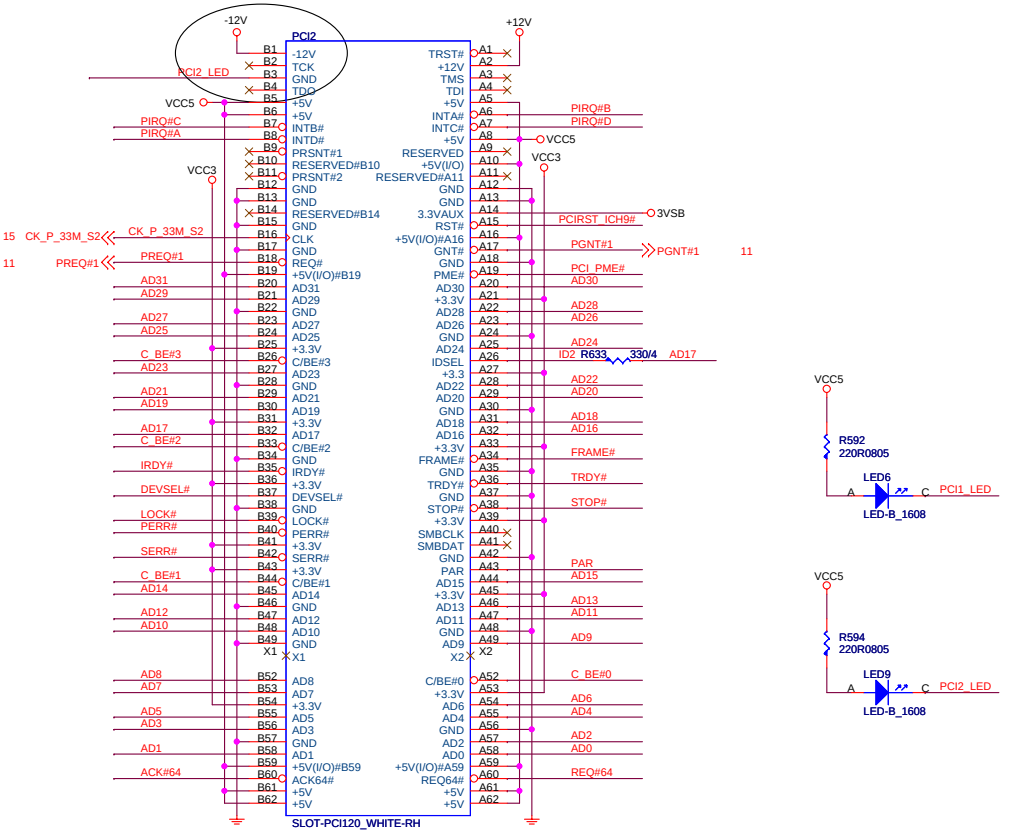


IDSEL = AD16
MASTER = PREQ#0
PIRQ#A

11 AD[31..0] AD[31..0]

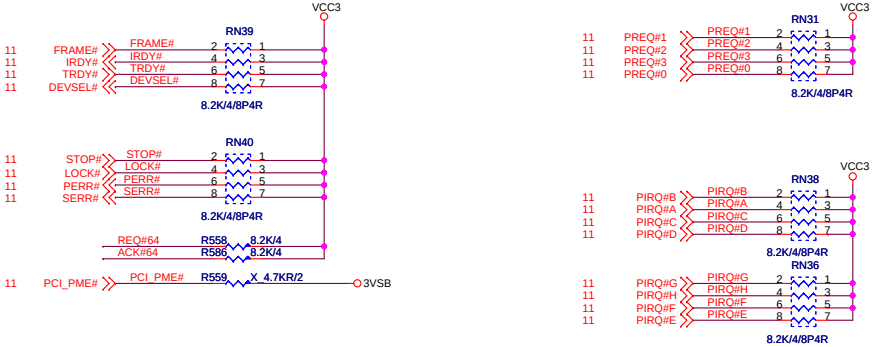
11 C_BE#[3..0] C_BE#[3..0]

PCI SLOT 2 (PCI VER: 2.2 COMPLY)

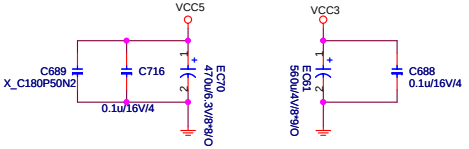


IDSEL = AD17
MASTER = PREQ#1
PIRQ#B

PCI PULL-UP / DOWN RESISTORS



PCI SLOT DECOUPLING CAPACITORS



MICRO-STAR INT'L CO.,LTD		
MS-7512		
Size: Custom	Document Description: PCI Slot 1 & 2	Rev: 0A
Date: Wednesday, December 19, 2007	Sheet 22 of 36	

1394 CONTROLLER

TX, RX 別接反

11 PE2_1394_RX
11 PE2_1394_RX#
11 PE2_1394_TXC
11 PE2_1394_TXC#
15 CK_1394_DP
15 CK_1394_DN
16,18,31 PLTRST_BU3#
EEDI
EECK
1394_GPIO2
1394_GPIO3

C538 0.1uf/10V/X7R/4 PE2_RXC
C542 0.1uf/10V/X7R/4 PE2_RXC#

U41 JMB381

APTXP APTXN APRXP APRXN APCLKP APCLKN XRSTN SEEDAT SEECLK APREXT XTEST GPIO0 GPIO1 GPIO2 GPIO3 TXIN TXOUT

DV33 DV33 DV18 DV18 APVDD APV18 TAV33 GND GND GND GND GND GND APGND

TPA0P TPA0N TPB0P TPB0N TPBIAS_0 TPA1P TPA1N TPB1P TPB1N TPBIAS_1 TCPS TREXT REG_CTL NC1 NC2 NC3 NC4

JMB381-LGBZ0A-A-RH

R472 10K/4/1
R430 390K/4 CPWR_F
R486 12K/4
R431 X_0R/4 1_8V_CTL

Internal push PNP BJT

C597 20P/50V/4 CLK_1394_XI
C598 20P/50V/4 CLK_1394_XO
Y6 24.576MHZ16P_D
R489 1M/6

L4 X_Common Chock

TPB0- TPB0+ TPA0- TPA0+ TPB1- TPB1+ TPA1- TPA1+

Rear 1394 port

C555 0.33u/16V/6
TPBIAS0
R457 4.99KST/4
1394TP0
C537 220P/16V/4
R466 56/4 TPA_0+
R462 56/4 TPA_0-
R453 56/4 TPB_0+
R446 56/4 TPB_0-

Place near JMB381

width 60mil

+12V
D4 DO214AC_40V,2A
CPWR
FS1 F-MF-MSMF150-24X-RH
CPWR_0
C73 X_102P/50V/4
C78 X_0.1u/50V/6
C77 0.01u/50V/6

J1 1394-6PMSTRAIGHT_BLACK-RH

Front 1394 pin header

C585 0.33u/16V/6
TPBIAS1
R481 4.99KST/4
1394TP1
C582 220P/16V/4
R483 56/4 TPA_1+
R480 56/4 TPA_1-
R479 56/4 TPB_1+
R471 56/4 TPB_1-

Place near JMB381

J1394_1 H2X5[9]M_GREEN

width 60mil

+12V
D24 DO214AC_40V,2A
CPWR_F
FS2 F-MF-MSMF150-24X-RH
CPWR_1
C740 X_102P/50V/4
C724 X_0.1u/50V/6

For Intel 1394 pinheader

CP23 X_COPPER

Reserver to AVCC1_8 noise

C601 X_10u/10V/8
C497 X_10u/10V/8

C532 0.1uf/10V/X7R/4
C596 0.1uf/10V/X7R/4
C499 0.1uf/10V/X7R/4
C556 0.1uf/10V/X7R/4
C500 10u/10V/8
C560 1u/6.3V/4
C561 X_10u/10V/8
C587 1u/6.3V/4
C533 1u/6.3V/4
C563 X_102P/50V/4

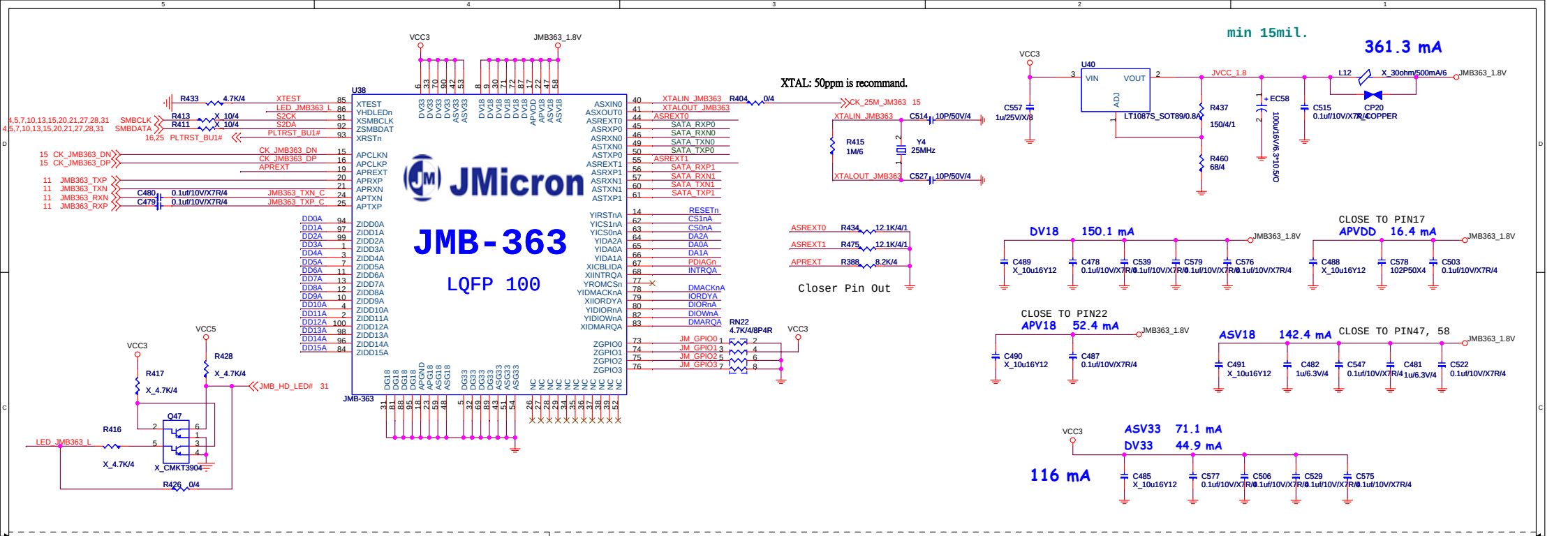
AVCC1_8 close Pin5 , Pin10

A1117 CO-LAY SOT223 (TO_261) PNP BJT

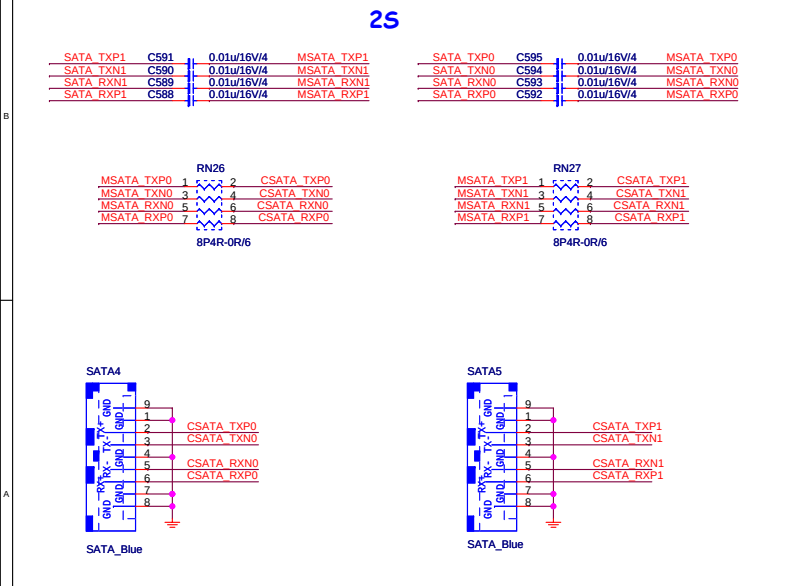
U37 RC1117S_SOT223
C535 1u/6.3V/4
R399 220RST/4
C549 X_10u/10V/8
EC59 100u/16V/6.3*10.5/O
R398 100R1%/2
1_8V_CTL

RN19 4.7K/4/8P4R
R427 X_510/4
U36 X_AT24C02BN-SH-T-RH

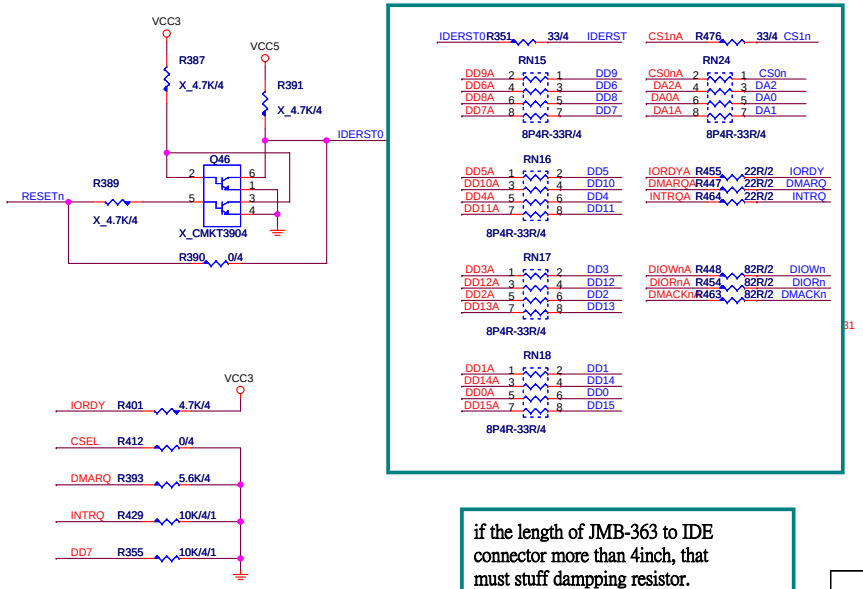
MICRO-STAR INT'L CO.,LTD	
MS-7512	
Size: Custom	Document Description: 1394 Controller - JMB381
Rev: 0A	
Date: Wednesday, December 19, 2007	Sheet 23 of 36



2S



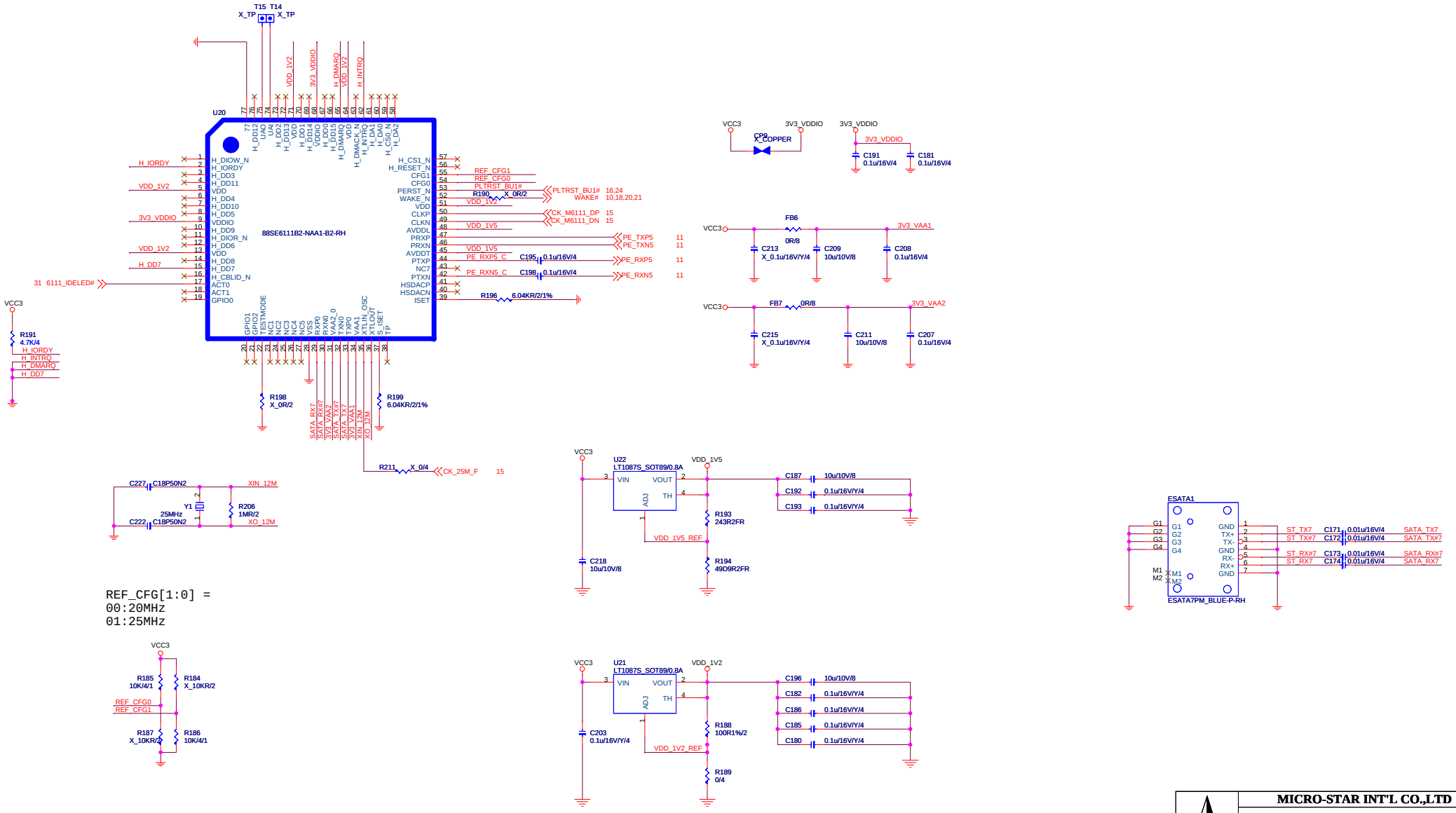
1P



if the length of JMB-363 to IDE connector more than 4inch, that must stuff dampping resistor.

MICRO-STAR INT'L CO.,LTD		
MS-7512		
Size: Custom	Document Description: JMB-363 e-SATA X2/ IDE X1	Rev: 0A
Date: Friday, December 21, 2007	Sheet 24 of 36	

Hi-Speed PCIE to SATA/PATA Bridge

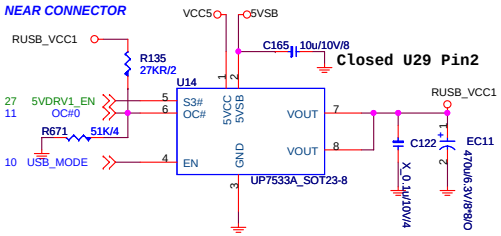


REF_CFG[1:0] =
00:20MHz
01:25MHz

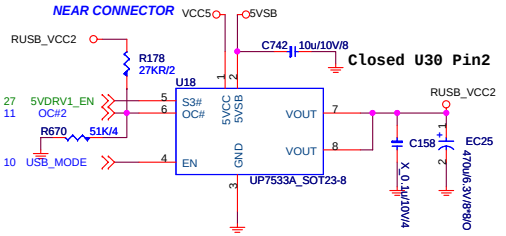
MICRO-STAR INT'L CO.,LTD		
MS-7512		
Size: Custom	Document Description: Marvell 88SE6111 PCIE to PATA/SATA	Rev: 0A
Date: Thursday, December 27, 2007	Sheet 25 of 36	

Rear USB Connector

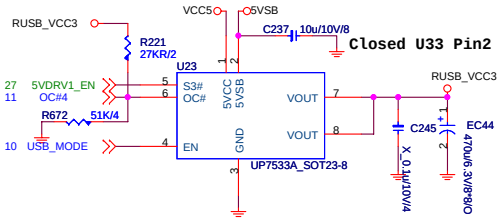
USB POWER FOR PORT 6,7



USB POWER FOR PORT 8,9



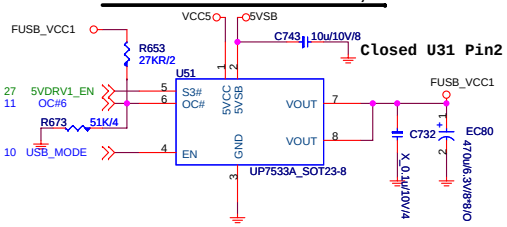
USB POWER FOR PORT 10,11



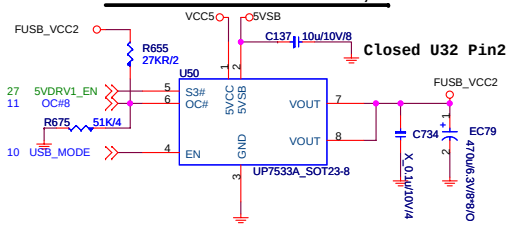
GPIO for USB voltage
H:Follow 5VSB
L:Always off

Front USB Connector

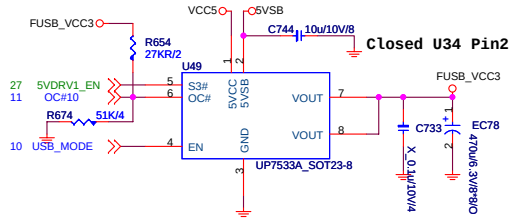
USB POWER FOR PORT 0,1



USB POWER FOR PORT 2,3

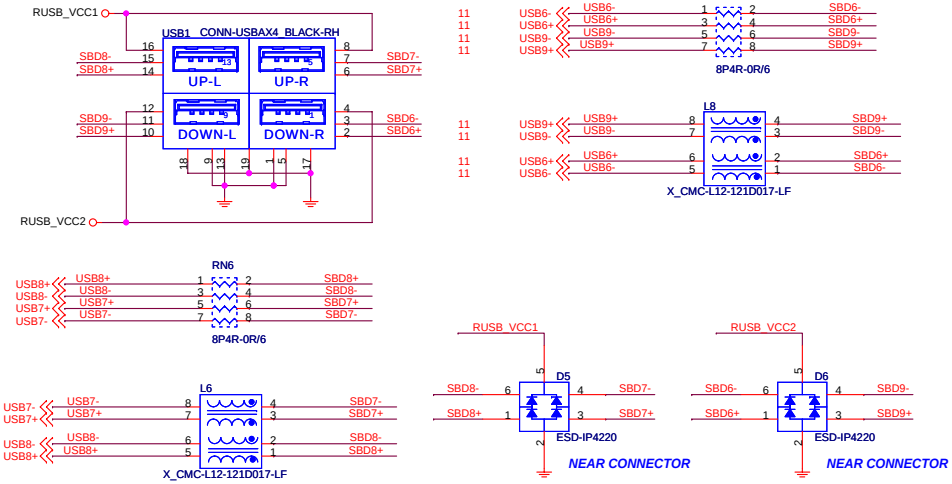


USB POWER FOR PORT 4,5

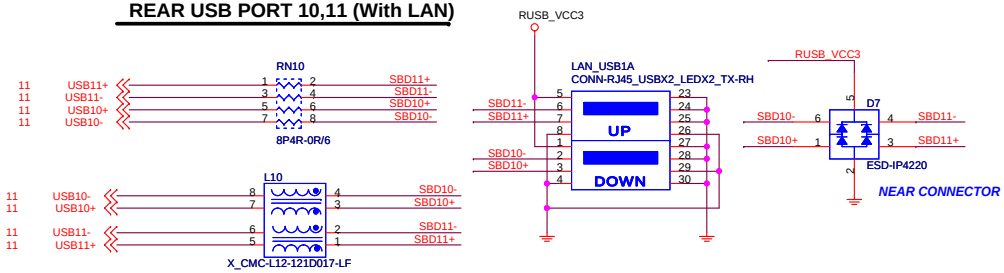


GPIO for USB voltage
H:Follow 5VSB
L:Always off

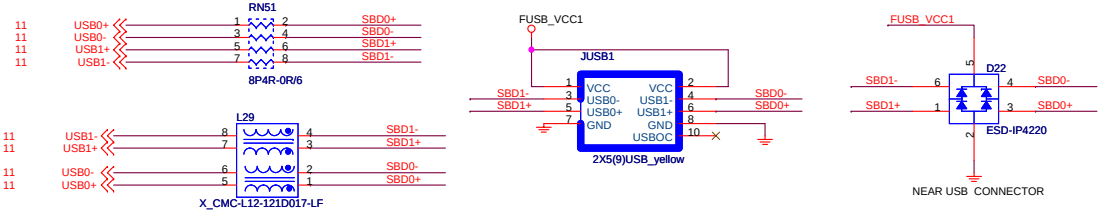
REAR USB PORT 6,7,8,9 (2x2)



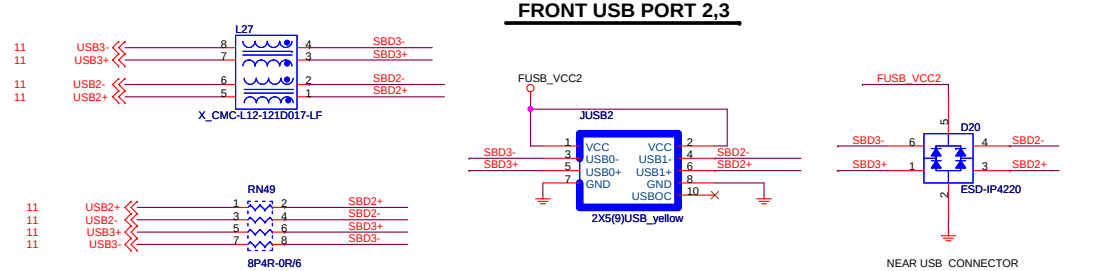
REAR USB PORT 10,11 (With LAN)



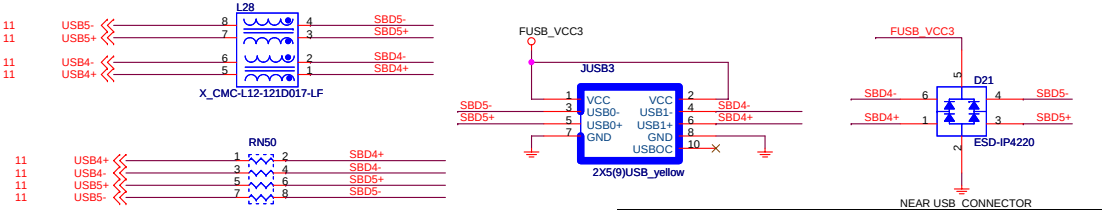
FRONT USB PORT 0,1



FRONT USB PORT 2,3



FRONT USB PORT 4,5

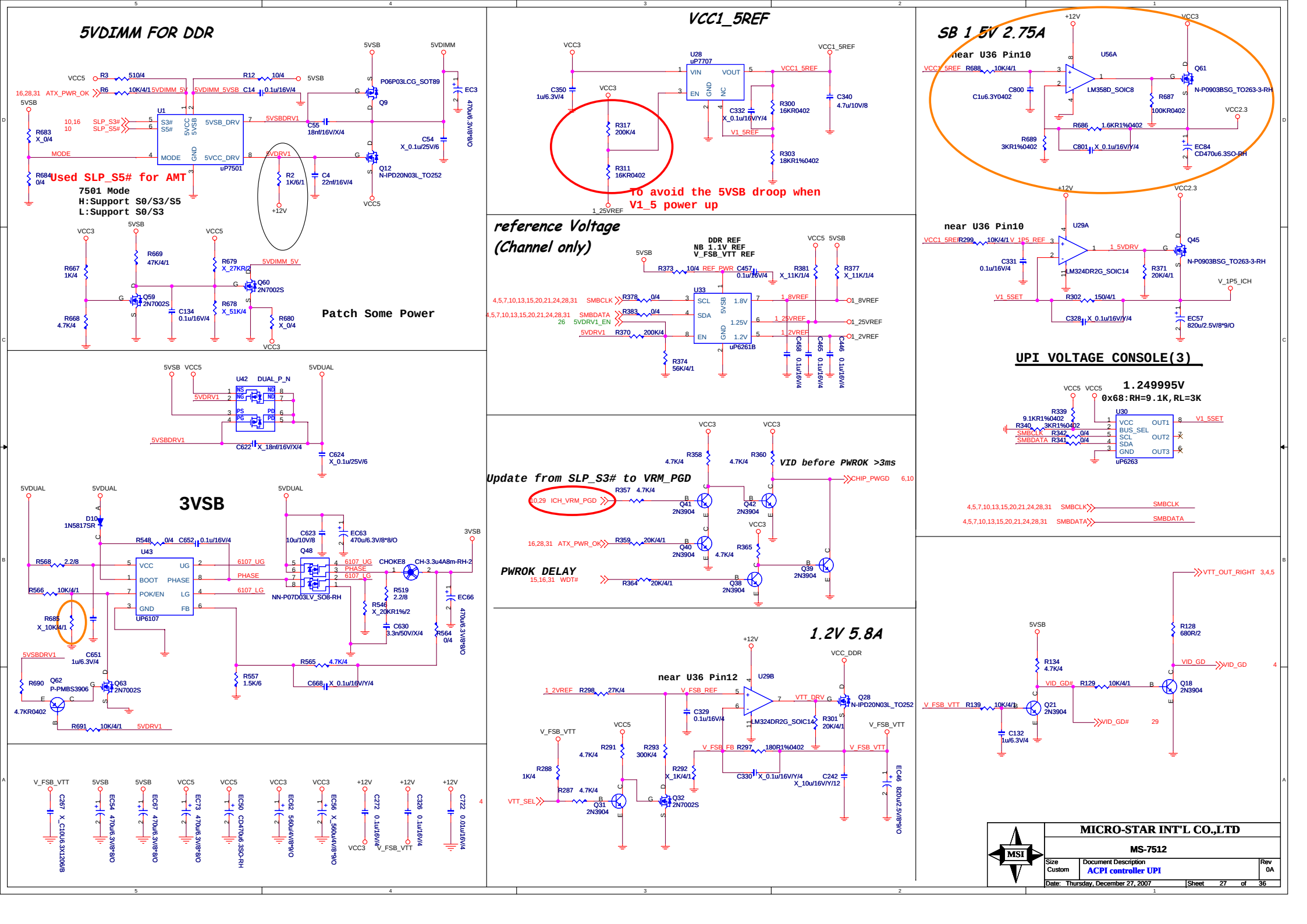


MICRO-STAR INT'L CO.,LTD

MS-7512

Size	Document Description	Rev
Custom	USB Connectors	0A

Date: Wednesday, December 19, 2007 Sheet 26 of 36

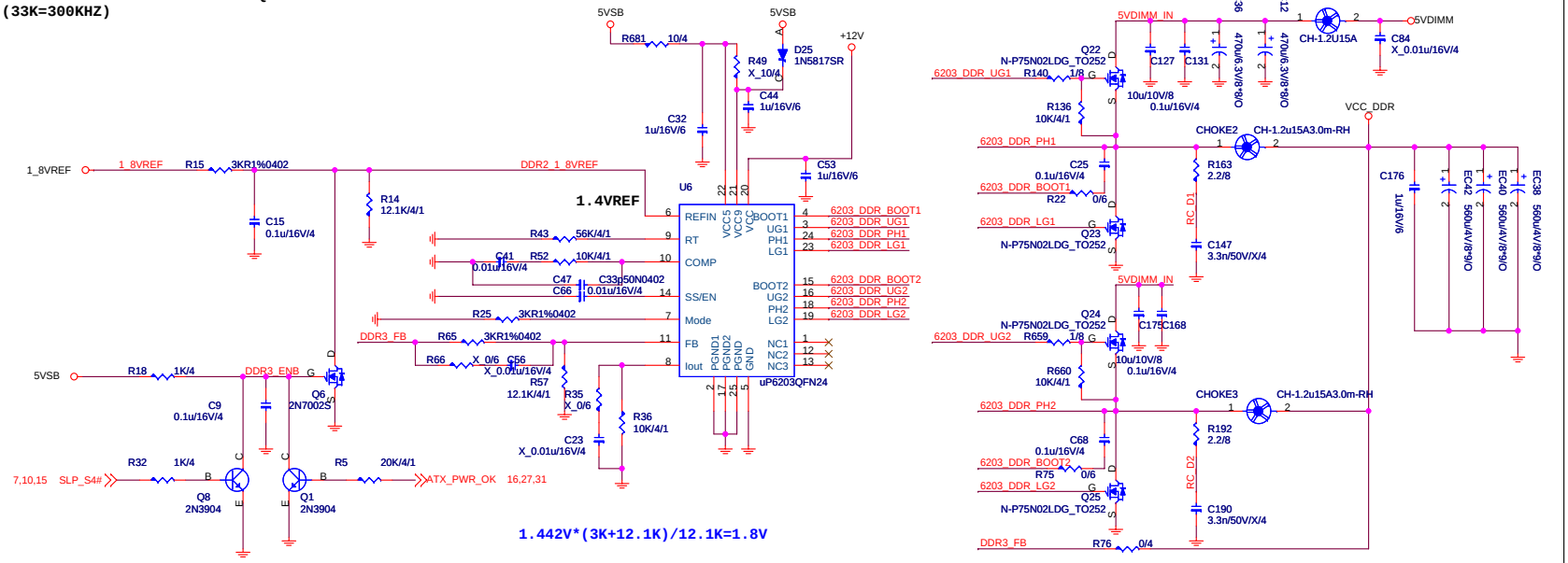

5VDIMM FOR DDR
Used SLP_S5# for AMT
7501 Mode
H:Support S0/S3/S5
L:Support S0/S3
Patch Some Power
VCC1_5REF
To avoid the 5VSB droop when V1_5 power up
reference Voltage
(Channel only)
DDR REF
NB 1.1V REF
V_FSB_VTT REF
SB 1.5V 2.75A
near U36 Pin10
near U36 Pin10
UPI VOLTAGE CONSOLE(3)
1.249995V
0x68:RH=9.1K,RL=3K
3VSB
Update from SLP_S3# to VRM_PGD
VID before PWROK >3ms
PWROK DELAY
1.2V 5.8A
near U36 Pin12
MICRO-STAR INT'L CO.,LTD
MS-7512
ACPI controller UPI

DDR II 1.8V POWER

7.2A+0.75A+3A+?A=18A
(DDRIII+V_SM_VTT+NB_VCC_CL+NB_V_SM)

R506 CHANGE R CAN CHANGE FREQUENCY
(33K=300KHZ)

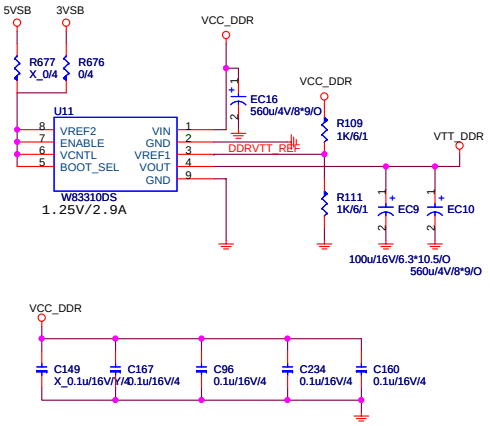
Iripple=18*0.6*0.8/1=8.64A
5.7*2*1=11.4A>8.64A



1.442V*(3K+12.1K)/12.1K=1.8V

DDR VTT Power

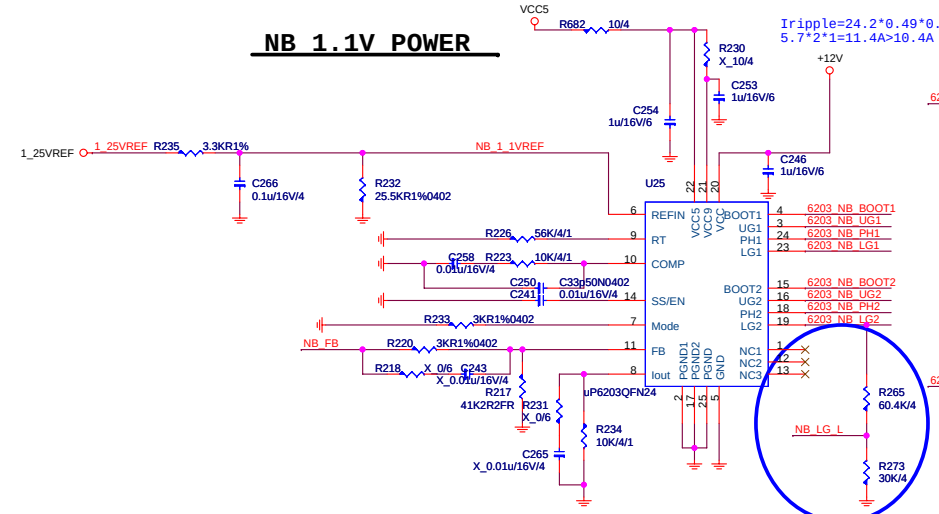
To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .



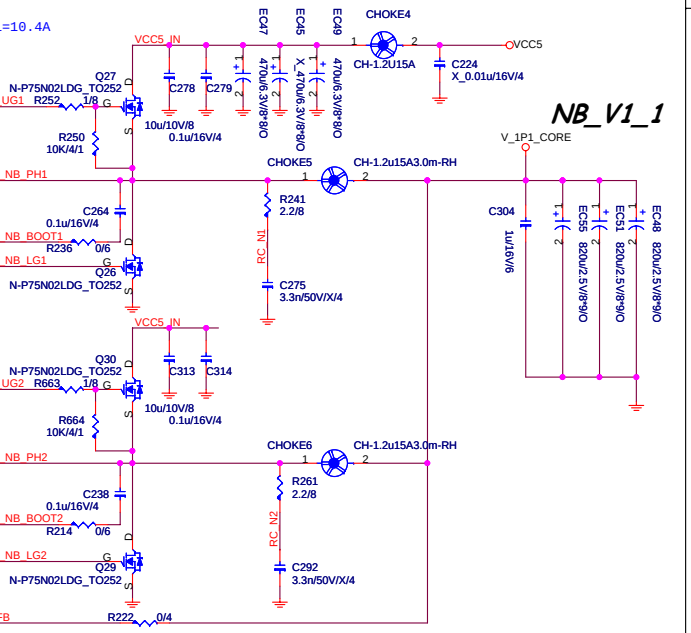
de- VCC_DDR high frequency noise.

NB 1.1V POWER

Iripple=24.2*0.49*0.878/1=10.4A
5.7*2*1=11.4A>10.4A

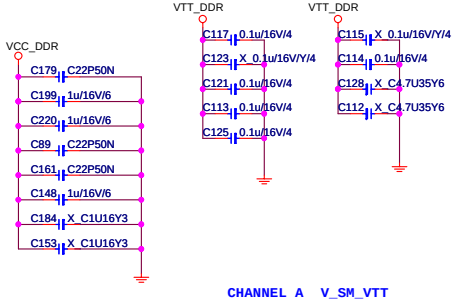


For channel DOT3 used.

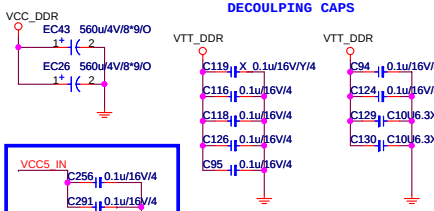


30A
Irms(MAX) of VCC1_1=30A
(30A-4.6A-1.2A=24.2A)
(Imax-V_FSB_VTT(CPU)-V_FSB_VTT(NB)-24.2A)

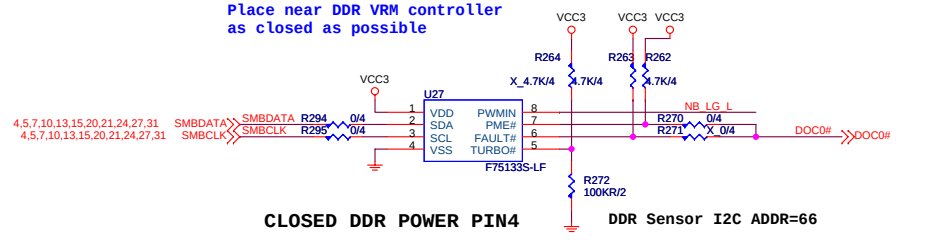
CHANNEL B V_SM_VTT DECOULPING CAPS



CHANNEL A V_SM_VTT DECOULPING CAPS



Place near DDR VRM controller as closed as possible

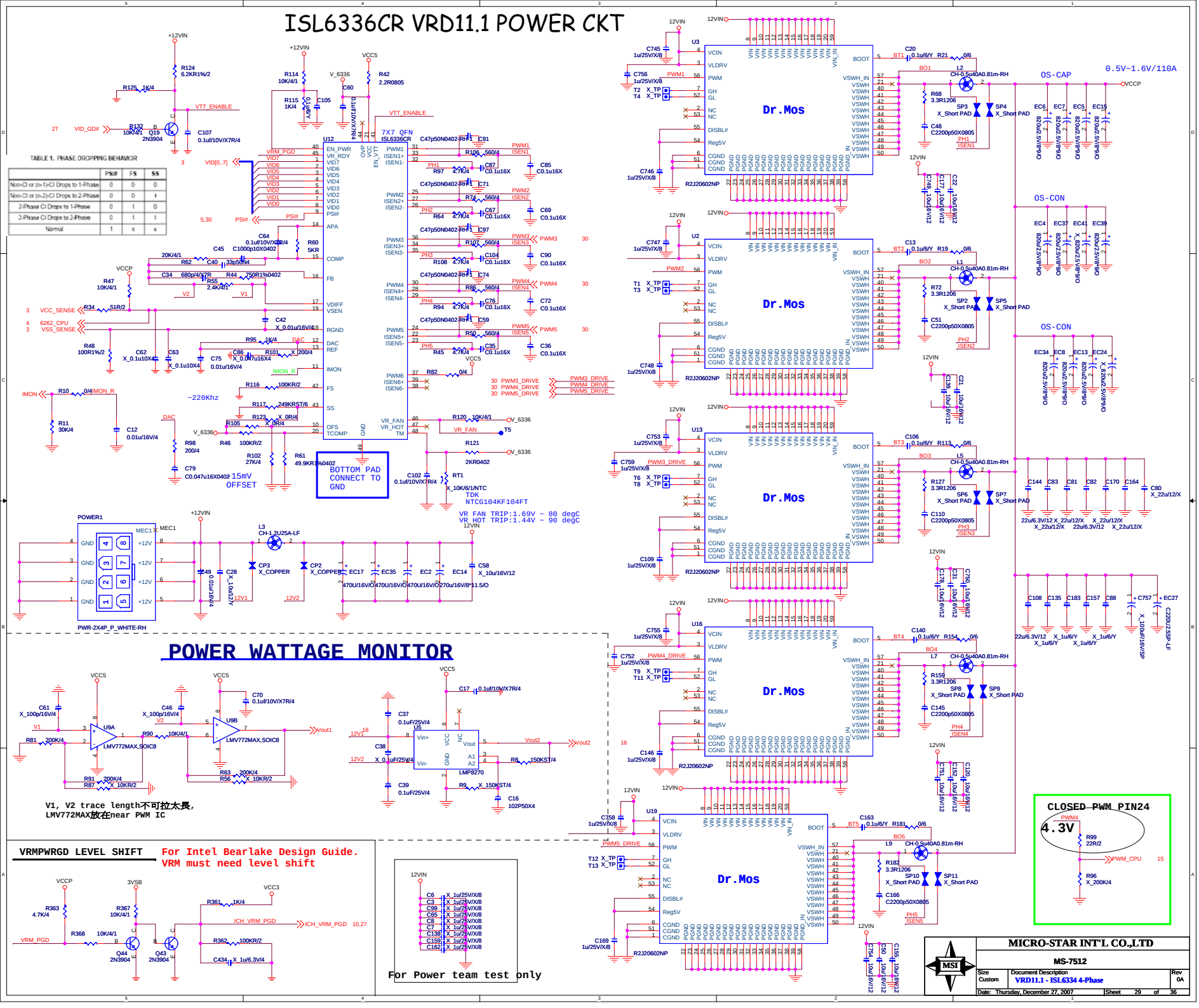


CLOSED DDR POWER PIN4

DDR Sensor I2C ADDR=66

MICRO-STAR INT'L CO.,LTD		
MS-7512		
Size: Custom	Document Description: NB Core Power & DDR Power	Rev: 0A
Date: Thursday, December 27, 2007	Sheet 28 of 36	

ISL6336CR VRD11.1 POWER CKT



POWER WATTAGE MONITOR

V1, V2 trace length不可拉太長,
LMV772MAX放在near PWM IC

VRMPWRGD LEVEL SHIFT

For Intel Bearlake Design Guide.
VRM must need level shift

For Power team test only

CLOSED PWM PIN24

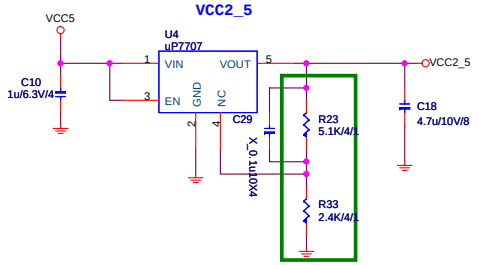
4.3V

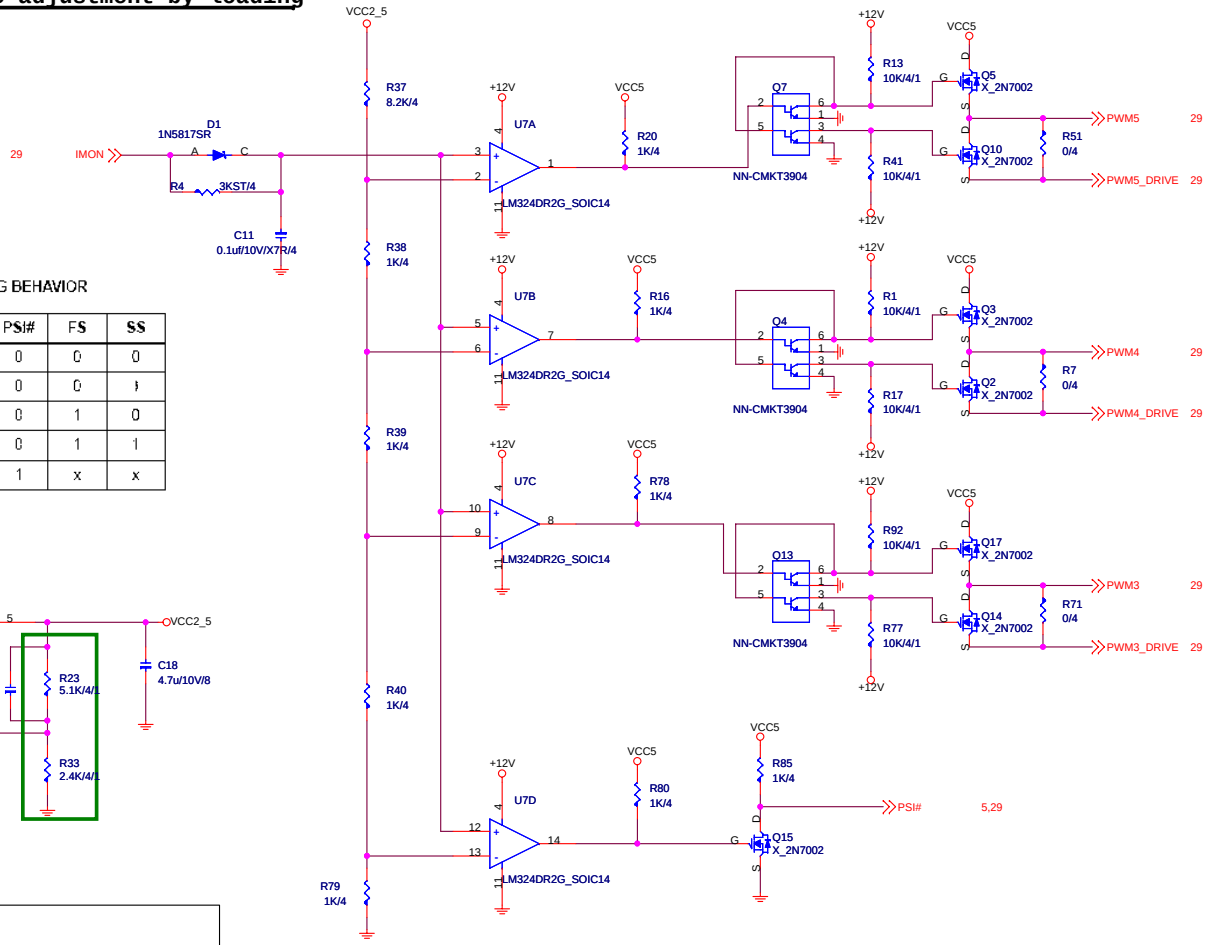
MICRO-STAR INT'L CO.,LTD	
MS-7512	
Size: Custom	Document Description: VRD11.1 - ISL6334 4-Phase
Rev: 0A	
Date: Thursday, December 27, 2007	Sheet 29 of 36

Phase adjustment by loading

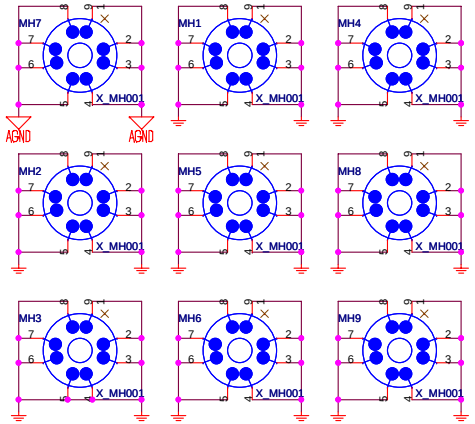
TABLE 1. PHASE DROPPING BEHAVIOR

	PSI#	FS	SS
Non-CI or (n-1)-CI Drops to 1-Phase	0	0	0
Non-CI or (n-2)-CI Drops to 2-Phase	0	0	1
2-Phase CI Drops to 1-Phase	0	1	0
2-Phase CI Drops to 2-Phase	0	1	1
Normal	1	x	x

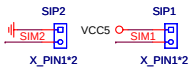




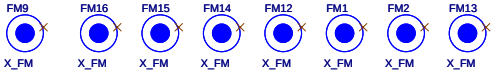
Mounting Holes



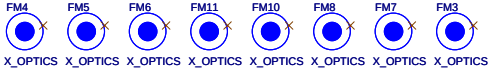
Simulation



Optical Fiducial Marks-120



Optical Fiducial Marks-100



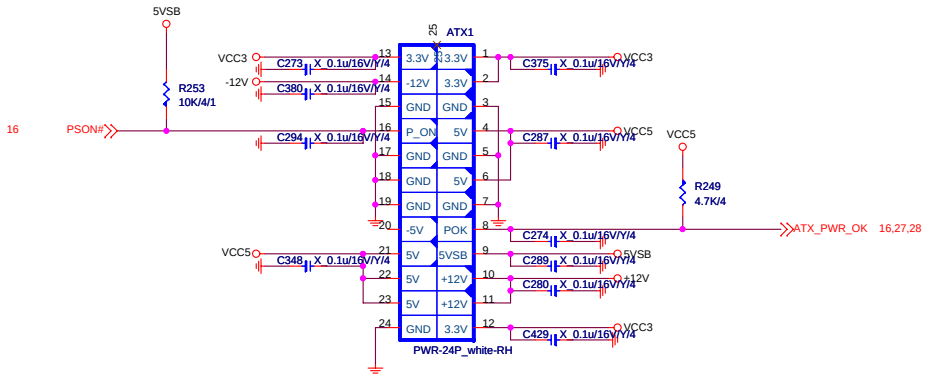
MICRO-STAR INT'L CO.,LTD

MS-7512

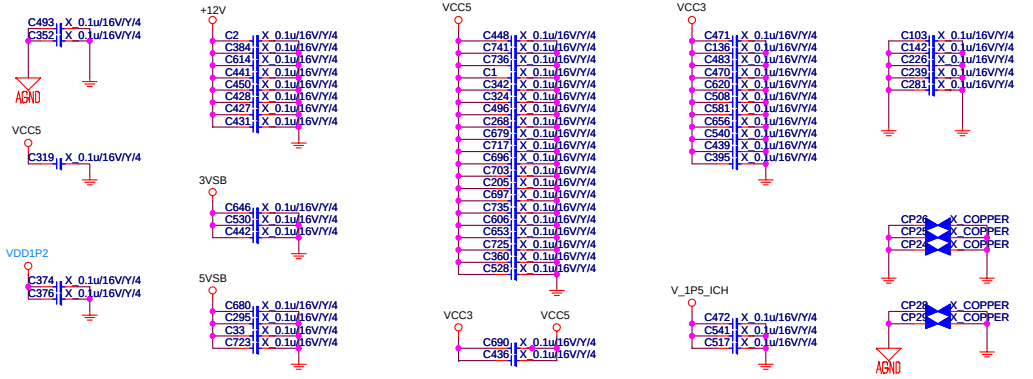
Size	Document Description	Rev
Custom	PSI/IMON	0A

Date: Friday, December 21, 2007 Sheet 30 of 36

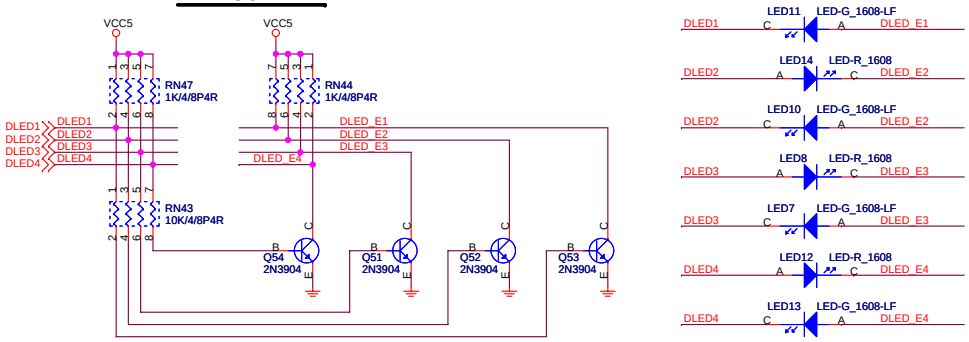
ATX POWER CONNECTOR



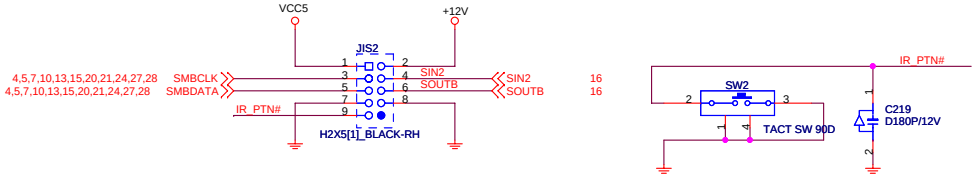
Cap. for EMI & Power



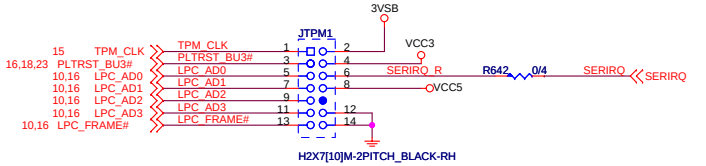
DEBUG LED



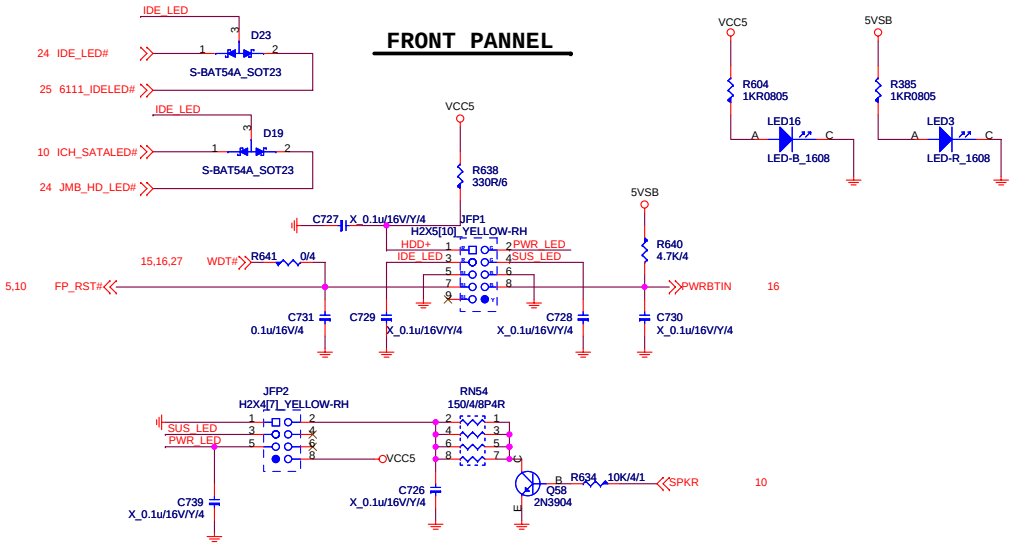
IR SENCE



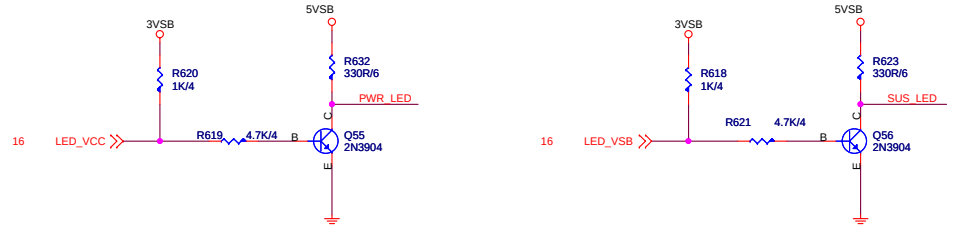
TPM



FRONT PANNEL



LED (for Fintek 71882)



MICRO-STAR INT'L CO.,LTD		
MS-7512		
Size: Custom	Document Description: ATX PWR-Connector & Front Panel & EMI	Rev: 0A
Date: Wednesday, December 19, 2007	Sheet 31 of 36	