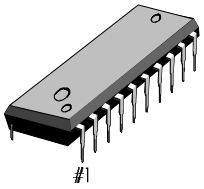
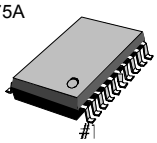
INTRODUCTION

The KDA0316 is a CMOS 16-bit digital-to-analog converter for compact disc player that uses a dynamic level shift conversion method combining R-string, Pulse Width Modulation and level shift.

20-DIP-300A



20-SOP-375A



FEATURES

- 2's complement serial data input
- Contains two-channel D/A converter
- Can output L out and R out in phase
- To 176.4KHz maximum sampling frequency
- (corresponding to four oversampling)
- Si-gate CMOS process (low power consumption)
- Single 5V supply voltage
- Built-in test clrcuit for PWM DAC
- Output swing level can be adjusted by the V_R input voltage
- MSB first and LSB first mode of input digital audio data is available

TYPICAL APPLICATIONS

- Portable cassette radios with CDP
- Home audio component systems
- Electronic keyboards
  Music centers
- Mini CDPs
- Car CDPs

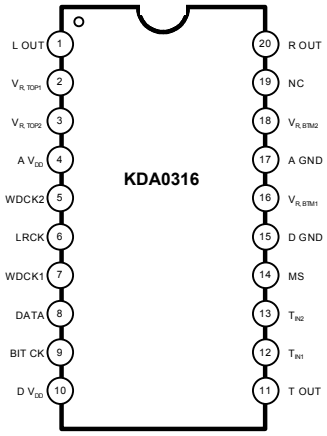
ORDERING INFORMATION

Device	THD(Max)(%)	Package	Tomperaturs Rang	Max Oversampling
KDA0316LN	0.05	20-DIP-300A	-30°C~ +75°C	4Fs
KDA0316N	0.08			
KDA0316LD	0.05	20-SOP-375		
KDA0316D	0.08			

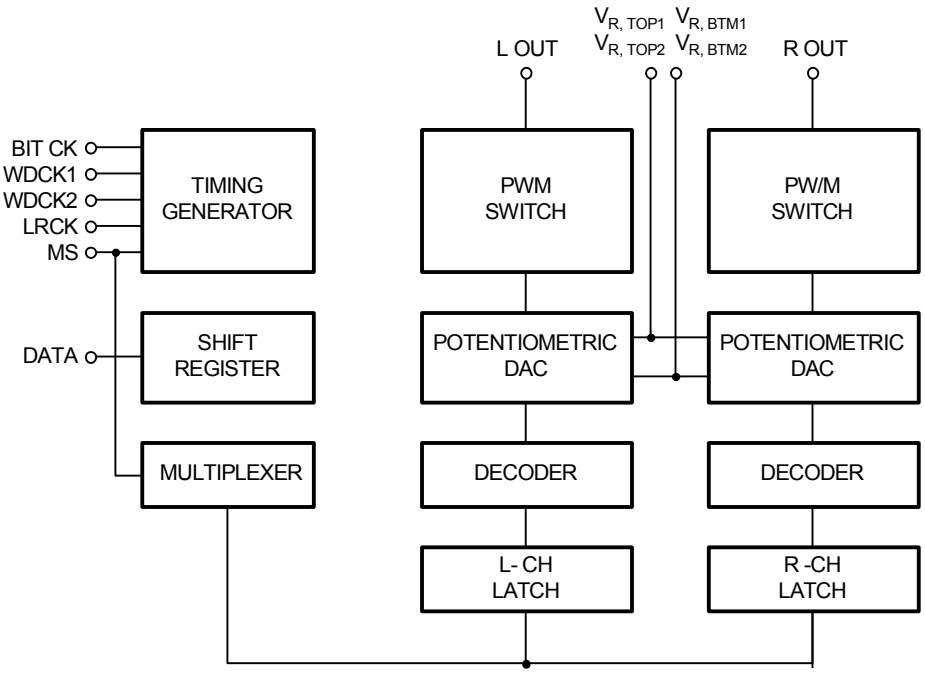
Fs: sampling frequency (44.1KHz)

PIN CONFIGURATION

Dual-in-line Package &
Small Outline Package



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Note 1 & 2)

Characteristics	Symbol	Value	Unit
Supply Voltage	V_{DD}	- 0.3 ~ +7.0	V
Input Voltage	V_{IN}	-0.3 ~ V_{DD} +0.3	V
Output Voltage	V_{OUT}	-0.3 ~ V_{DD} +0.3	V
Operating Temperature Range	V_{opr}	-30 ~ +75	°C
Storage Temperature Range	T_{stg}	-40 ~ +125	°C
ESD Susceptibility (Note 3)	V_{ESD}	± 900	V
Latch-up Current	V_{lat}	50	mA

RECOMMENDED OPERATING CONDITIONS

Characteristics	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{DD}	4.5	5.0	5.5	V
Operating Temperature Range	T_{opr}	-30		75	°C
Input "H" Voltage	V_{IH}	2.2		V_{DD} +0.3	V
Input "L" Voltage	V_{IL}	-0.3		0.8	V
Reference "H" Voltage	$V_{R,TOP}$	V_{DD}-0.5		V_{DD}	V
Reference "L" Voltage	$V_{R,BTM}$	0		0.5	V
Sampling Frequency	fs			176.4	KHz

ELECTRICAL CHARACTERISTICS

(Converter Specifications: V_{DD} = 5V, V_{ref} H = 5V, V_{ref} L = A GND, MS = 0V, fs = 176.4KHz, Ta = 25°C, unless otherwise noted.)

Characteristics	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Current	I_{CC}	V_{DD} = 5V		3.5	5.5	mA
		V_{DD} = 5.5V		4.0	7.0	
Total Harmonic Distortion	THD	MS = 0V or 5V Data = 1KHz, 0dB			0.05*1 0.08	%
		MS = 0V or 5V Data = 1KHz, -20dB			0.2	
Signal to Noise Ratio	SNR	Data = 1KHz, 0dB		92		dB
		V_{DD} = 4.5V Data =1KHz, 0dB		87		
		MS = 5V Data = 1KHz, 0dB		92		
		MS = 5V, V_{DD} = 4.5V Data = 1KHz, 0dB		87		
Crosstalk	CT	Data = 1KHz, 0dB		-85		dB

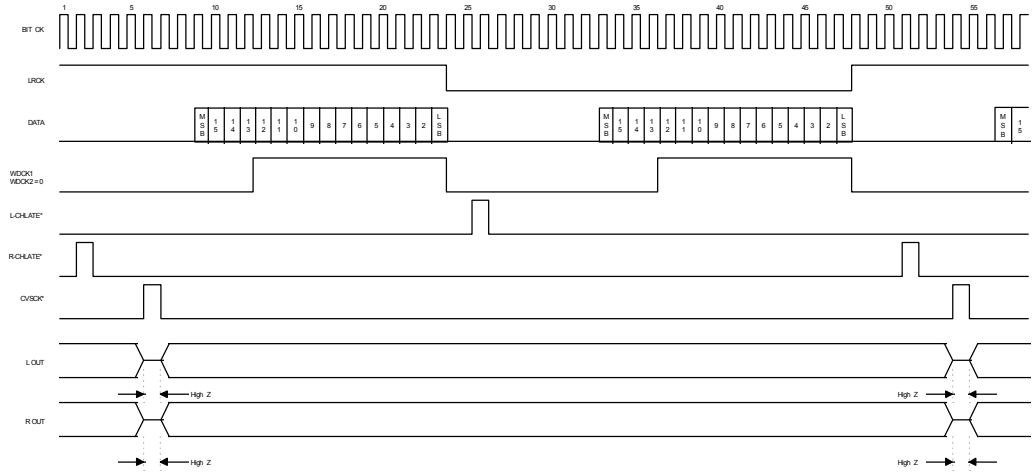
*1: User's option value (KDA0316LN, KDA0316LD)

Note 1: ABSOLUTE MAXIMUM RATINGS are those values beyond which the life of the device may be impaired. Normal operation is not guaranteed at these extremes.

Note 2: All voltage are measured with respect to the GND, unless otherwise noted. The separate A GND point should always be wired to the D GND.

Note 3: 100pF discharged through a 1.5KΩ resistor.

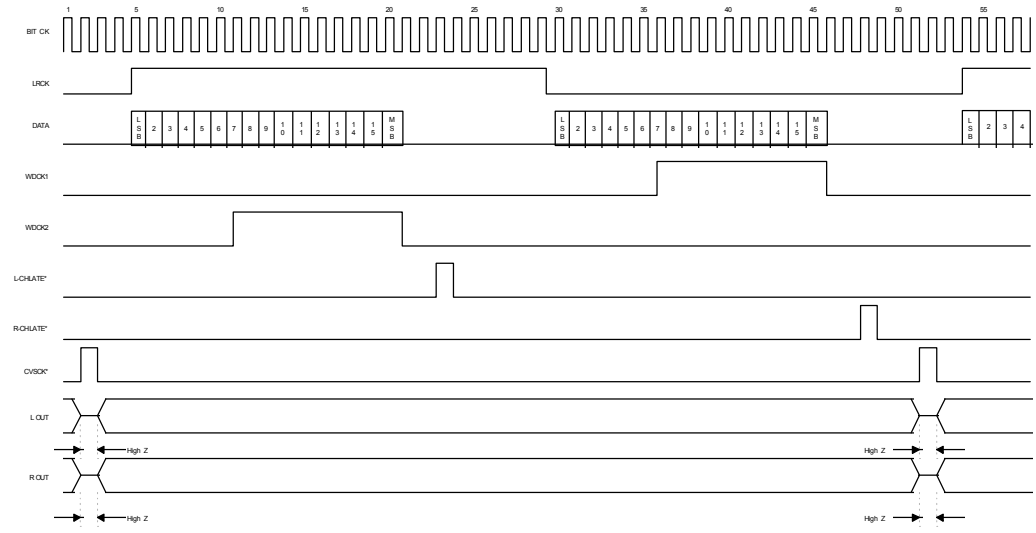
TIMING DIAGRAM 1 (When MS = "H")



* L-CHLATE, R-CHLATE, and CVSCK is internal signal.

BIT CK = 8.4672 MHz (fs = 176.4KHz)
4.2336 MHz (fs = 88.2KHz)
2.1168 MHz (fs = 44.1KHz)

TIMING DIAGRAM 2 (When MS = "L")



* L-CHLATE, R-CHLATE, and CVSCK is internal signal.

BIT CK = 8.6436 MHz (fs = 176.4KHz)
4.3218 MHz (fs = 88.2KHz)
2.1609 MHz (fs = 44.1KHz)

PIN DESCRIPTION

Pin No	Symbol	Function
1	L OUT	Left channel output pin
2	$V_{R,TOP}1$	Top reference voltage 1 pin
3	$V_{R,TOP}2$	Top reference voltage 2 pin
4	A V_{DD}	Analog supply voltage pin
5	WDCK2	Word clock 2 input pin
6	LRCK	Left/right clock input pin
7	WDCK1	Word clock 1 input pin
8	DATA	Digital audio data input pin
9	BIT CK	Bit clock input pin
10	D V_{DD}	Digital supply voltage pin
11	T OUT	Test output pin
12	$T_{IN}1$	Test input pin
13	$T_{IN}2$	Test input pin
14	MS	Mode selecting pin
15	D GND	Digital ground pin
16	$V_{R,BTM}1$	Bottom reference voltage 1 pin
17	A GND	Analog ground pin
18	$V_{R,BTM}2$	Bottom reference voltage 2 pin
19	NC	No connection
20	R OUT	Right channel output pin

FUNCTIONAL DESCRIPTION

1. Calling for Digital Audio Data

Digital audio data is a 16-bit serial 2's complement signal. The KDA0316 corresponds to MSB first code or LSB first code of digital audio data: the mode can be changed by the level of the MS pin. Data through the DATA pin is applied to the LCH latch and RCH latch of the two D/A converters built in the separate LCH and RCH.

(1) When MSB First (MS = "H" level) (see Timing Diagram 1)

Digital audio data is carried in MSB first sequence from the data pin to the Shift Register in synchronization with the BIT CK rising edge (Data transition occurs at the BIT CK falling edge.).
LCH data and RCH data are carried to the LCH latch and RCH latch by both the LCH latchable (L-CHLATE) and RCH latchable (R-CHLATE).

(2) When LSB First (MS = "L" level) (see Timing Diagram 2)

Digital audio data is carried in LSB first sequence from data pin to Shift Register in synchronization with BIT CK falling edge (Data transition is occurred at the BIT CK falling edge.).
LCH data and RCH data are carried to the LCH latch and RCH latch by both the LCH latchable (L-CHLATE) and RCH latchable (R-CHLATE).

2. D/A Conversion Circuit (see Fig. 1)

The KDA0316 has two D/A conversion circuits in the LCH and RCH independently. The two conversion methods are the same: a Complex Potentiometric Method, combining Resistor-Ladder D/A conversion, PWM (Pulse Width Modulation) D/A conversion, and Variable Resistor D/A conversion. After storing in the latch, the upper 9 bits of data (D15 ~ D7) inputs into the Resistor-Ladder DAC, the middle 3 bits of data (D6 ~ D4) into the PWM DAC and the lower 4 bits of data (D3 ~ D0) into the Variable Resistor DAC of the whole 16 bits of digital audio data (D15 ~ D0), respectively.
The Digital audio data of the LCH and RCH, which were inputted by the time division multiplexing method from the DATA pin, synchronize with the conversion clock and after being converted by the D/A converters the respective analog signals in phase are outputted from the L OUT and R OUT pins.

(1) Resistor-Ladder DAC

The 9-bit D/A conversion circuit, which has a 512 (= 2^9) unit resistor string, divides the whole voltage ($V_{R,TOP}$, $V_{R,BTM}$) across a Resistor-Ladder into 512 steps. The two adjoining Va and Vb of the whole voltage, which are divided into 512 steps according to the upper 9 bits of data (D15 ~ D7), are outputted by a switching circuit of PWM DAC, where $Vb - Va = (V_{R,TOP} - V_{R,BTM})/512$.

(2) PWM DAC

The 3-bit PWM DAC makes the differential voltage between Va and Vb, which is applied from a Resistor-Ladder DAC, divided into 8 steps by pulse width modulation.
According to the value of the upper 3 bits of data (D6 ~ D4), Va and Vb is outputted through the LCH or RCH terminal. A PWM DAC clock uses the BIT CK, and a relationship of sampling frequency and BIT CK frequency is shown in the Timing Diagrams.

(3) **Variable Resistor DAC**

The 4-bit Variable Resistor DAC has two variable resistors, VR_{TOP} and VR_{BTM}, in series with the Resistor-Ladder. According to the lower 4 bits of data (D3 ~ D0), VR_{TOP} and VR_{BTM} vary as follows:

1) Irrespective of the value of data, (VR_{TOP} + VR_{BTM}) is constant.
2) According to the value of data, VR_{TOP} and VR_{BTM} ranges from zero to 15R/128 (R is a unit resistor of the Resistor-Ladder): in R/128 steps. Therefore according to the lower 4 bits of data (D3 ~ D0), Va and Vb of an R-string DAC outputs range from zero to 15ΔV/128 {$\Delta V = (V_{TOP} - V_{BTM})/512$} in Δ V/128 steps.

3. How to Use V_R(see FIg. 1)

V_R, the reference voltage across a Resistor-Ladder, is usually recommended with $V_{R,TOP}1$ = 5V, $V_{R,BTM}1$ = 0V. One way of avoiding an amplitude mismatching between the V_R and OP amp input connected to the output of the KDA0316 is to reduce the analog output amplitude with $V_{R,TOP}2$ = 5V and $V_{R,BTM}2$ = 0V (at this time about 47μF ~ 100μF capacitors should be connected from $V_{R,TOP}1$ and $V_{R,BTM}1$ to GND.). By the effect of built-in R_{TOP} and R_{BTM} with this choice, the maximum analog output amplitude results in a narrow range of about 1.5 ~ 3.5V for 0dB playback.

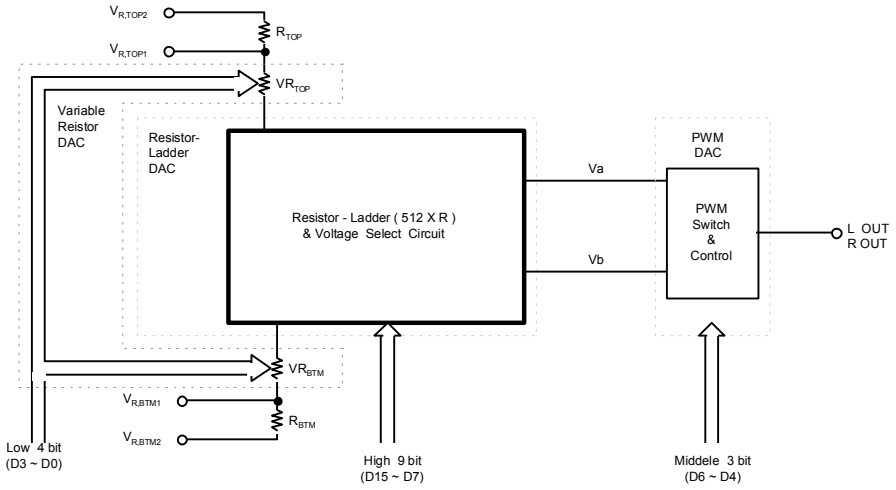
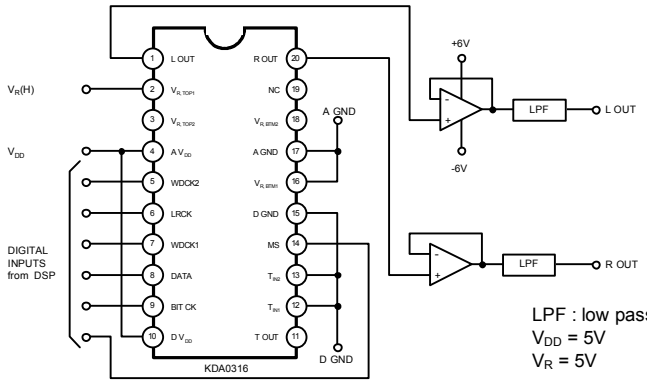


Fig. 1

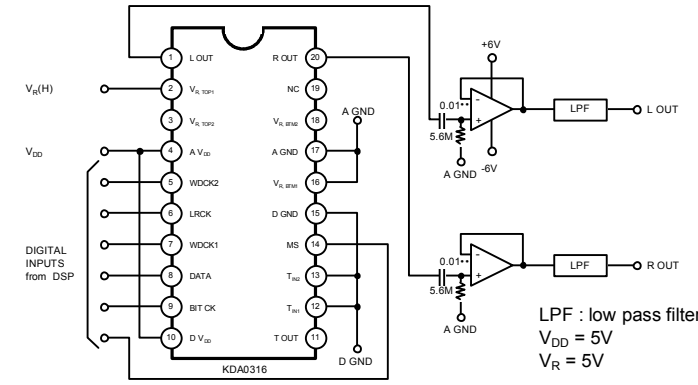
TYPICAL APPLICATIONS

(1)



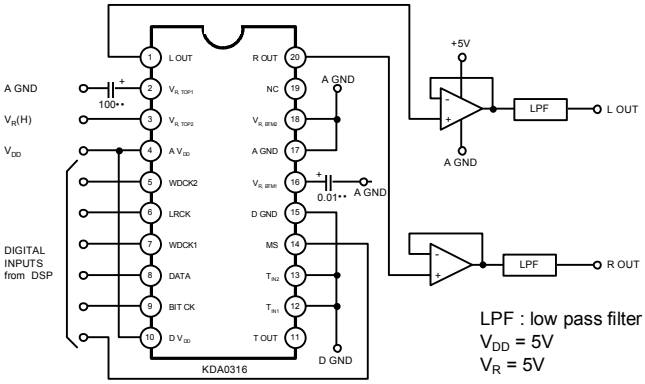
LPF : low pass filter (fc=20KHz)
V_{DD} = 5V
V_R = 5V

(2)



LPF : low pass filter (fc=20KHz)
V_{DD} = 5V
V_R = 5V

(3)



LPF : low pass filter (fc=20KHz)
V_{DD} = 5V
V_R = 5V